FM33256/FM3316

3V Integrated Processor Companion with Memory

Features

High Integration Device Replaces Multiple Parts
- Serial Nonvolatile Memory
- Real-time Clock (RTC) with Alarm
- Low V_{DD} Detection Drives Reset
- Watchdog Window Timer
- Early Power-Fail Warning/NMI
- 16-bit Nonvolatile Event Counter
- Serial Number with Write-lock for Security

Ferroelectric Nonvolatile RAM
- 256Kb and 16Kb versions
- Unlimited Read/Write Endurance
- 10 year Data Retention
- NoDelay™ Writes

Real-time Clock/Calendar
- Backup Current under 1 µA
- Seconds through Centuries in BCD format
- Tracks Leap Years through 2099
- Uses Standard 32.768 kHz Crystal
- Software Calibration
- Supports Battery or Capacitor Backup

Processor Companion
- Active-low Reset Output for V_{DD} and Watchdog
- Programmable Low-V_{DD} Reset Thresholds
- Manual Reset Filtered and Debounced
- Programmable Watchdog Window Timer
- Nonvolatile Event Counter Tracks System Intrusions or other Events
- Comparator for Power-Fail Interrupt or Other Use
- 64-bit Programmable Serial Number with Lock

Fast SPI Interface
- Up to 16 MHz Maximum Bus Frequency
- RTC, Supervisor Controlled via SPI Interface
- SPI Mode 0 & 3 (CPOL, CPHA=0,0 & 1,1)

Easy to Use Configurations
- Operates from 2.7 to 3.6V
- Small Footprint "Green" 14-pin SOIC (-G)
- Low Operating Current, 50µA Standby Current
- -40°C to +85°C Operation

Description

The FM33256 and FM3316 are devices that integrate FRAM memory with the most commonly needed functions for processor-based systems. Major features include nonvolatile memory, real-time clock, low-V_{DD} reset, watchdog timer, nonvolatile event counter, lockable 64-bit serial number area, and general purpose comparator that can be used for a power-fail (NMI) interrupt or other purpose. The devices operate from 2.7 to 3.6V.

Each FM33xx provides nonvolatile RAM available in memory capacity of 16Kb and 256Kb. Fast write speed and unlimited endurance allow the memory to serve as extra RAM or conventional nonvolatile storage. This memory is truly nonvolatile rather than battery backed.

The real-time clock (RTC) provides time and date information in BCD format. It can be permanently powered from external backup voltage source, either a battery or a capacitor. The timekeeper uses a common external 32.768 kHz crystal and provides a calibration mode that allows software adjustment of timekeeping accuracy.

The processor companion includes commonly needed CPU support functions. Supervisory functions include a reset output signal controlled by either a low V_{DD} condition or a watchdog timeout. /RST goes active when V_{DD} drops below a programmable threshold and remains active for 100 ms (max.) after V_{DD} rises above the trip point. A programmable watchdog timer runs from 60 ms to 1.8 seconds. The timer may also be programmed for a delayed start, which functions as a window timer. The watchdog timer is optional, but if enabled it will assert the reset signal for 100 ms if not restarted by the host within the time window. A flag-bit indicates the source of the reset.

A comparator on PFI compares an external input pin to the onboard 1.5V reference. This is useful for generating a power-fail interrupt (NMI) but can be used for any purpose. The family also includes a programmable 64-bit serial number that can be locked making it unalterable. Additionally it offers an event counter that tracks the number of rising or falling edges detected on a dedicated input pin. The counter can be programmed to be non-volatile under V_{DD} power or battery-backed using only V_{BAK}. If V_{BAK} is connected to a battery or capacitor, then events will be counted even in the absence of V_{DD}.

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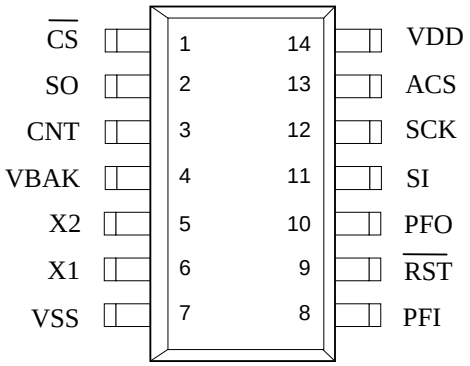
Pin Configuration



Pin Name	Function
/CS	Chip Select
SCK	Serial Clock
SI	Serial Data Input
SO	Serial Data Output
PFI	Power Fail Input
PFO	Power Fail Output (NMI)
CNT	Event Counter Input
ACS	Alarm/Calibration/SqWave
/RST	Reset Input/Output
X1, X2	Crystal Connections
VDD	Supply Voltage
VBAK	Battery-Backup Supply
VSS	Ground

Pin Descriptions

Pin Name	Type	Pin Description
/CS	Input	Chip Select: This active low input activates the device. When high, the device enters low-power standby mode, ignores the SCK and SI inputs, and the SO output is tri-stated. When low, the device internally activates the SCK signal. A falling edge on /CS must occur prior to every op-code.
SCK	Input	Serial Clock: All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Since the device is static, the clock frequency may be any value between 0 and 16 MHz and may be interrupted at any time.
SI	Input	Serial Input: All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet I_{DD} specifications. The SI pin may be connected to SO for a single pin data interface.
SO	Output	Serial Output: This is the data output pin. It is driven during a read and remains tri-stated at all other times. Data transitions are driven on the falling edge of the serial clock. The SO pin may be connected to SI for a single pin data interface.
CNT	Input	Event Counter Input: This input increments the counter when an edge is detected on this pin. The polarity is programmable and the counter value is nonvolatile or battery-backed, depending on the mode. This pin should be tied to ground if unused.
ACS	Output	Alarm/Calibration/SquareWave: This is an open-drain output that requires an external pullup resistor. In normal operation, this pin acts as the active-low alarm output. In Calibration mode, a 512 Hz square-wave is driven out. In SquareWave mode, the user may select a frequency of 1, 512, 4096, or 32768 Hz to be used as a continuous output. The SquareWave mode is entered by clearing the AL/SW and CAL bits in register 18h.
X1, X2	I/O	32.768 kHz crystal connection. When using an external oscillator, apply the clock to X1 and a DC mid-level to X2 (see Crystal Type section for suggestions).
/RST	I/O	Reset: This active-low output is open drain with weak pull-up. It is also an input when used as a manual reset. This pin should be left floating if unused.
PFI	Input	Early Power-fail Input: Typically connected to an unregulated power supply to detect an early power failure. This pin must be tied to ground if unused.
PFO	Output	Early Power-fail Output: This pin is the early power-fail output and is typically used to drive a microcontroller NMI pin. PFO drives low when the PFI voltage is <1.5V.
VBAK	Supply	Backup supply voltage: A 3V battery or a large value capacitor. If no backup supply is used, this pin should be tied to V_{SS}.
VDD	Supply	Supply Voltage.
VSS	Supply	Ground

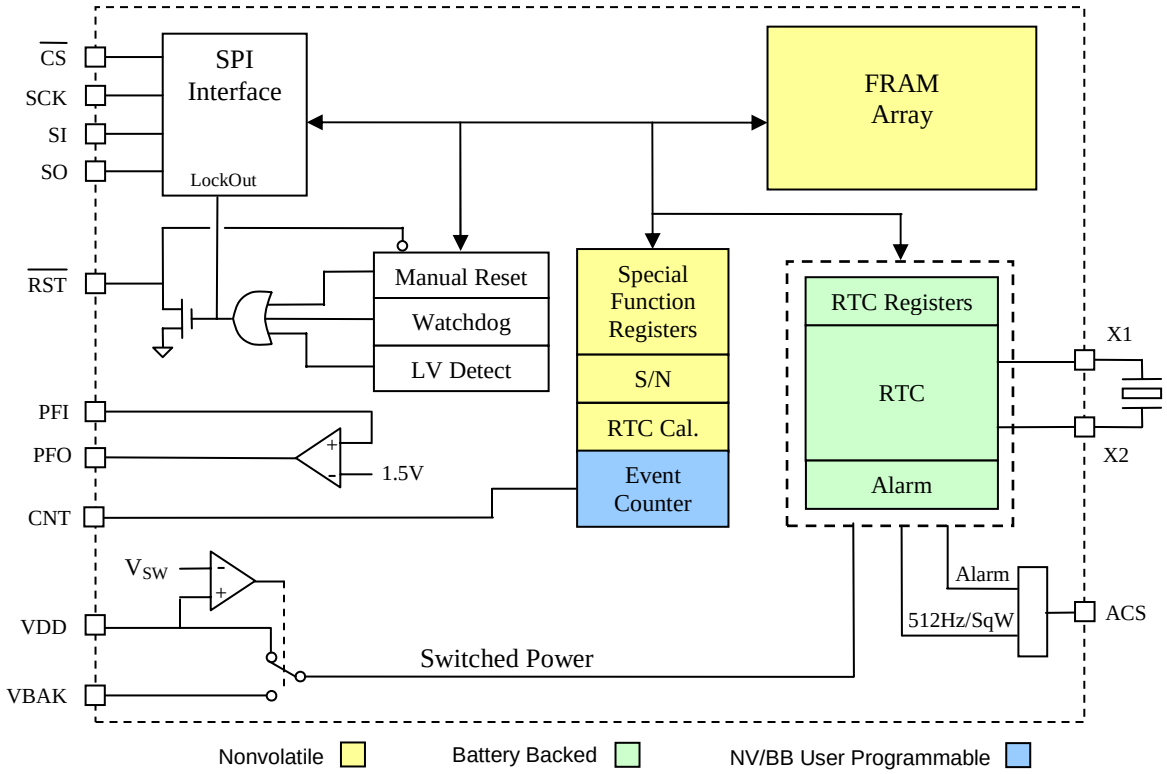


Figure 1. Block Diagram

Ordering Information					
Base Configuration	Memory Size	Operating Voltage	Max. Clock Freq.	Reset Thresholds	Ordering Part Number
FM33256	256Kb	2.7-3.6V	16 MHz	2.6V, 2.75, 2.9, 3.0V	FM33256-G
FM3316	16Kb	2.7-3.6V	16 MHz	"	FM3316-G

Other memory configurations may be available. Please contact the factory for more information.

Overview

The FM33xx devices combine a serial nonvolatile RAM with a real-time clock (RTC) and a processor companion. The companion is a highly integrated peripheral including a processor supervisor, analog comparator, a nonvolatile counter, and a serial number. The FM33xx integrates these complementary but distinct functions under a common interface in a single package. Although monolithic, the product is organized as two logical devices. The first is a memory and the second is the companion which includes all the remaining functions. From the system perspective they appear to be two separate devices with unique op-codes on the serial bus.

The memory is organized as a standalone nonvolatile SPI memory using standard op-codes. The real-time clock and supervisor functions are accessed under their own op-codes. The clock and supervisor functions are controlled by 30 special function registers. The RTC/alarm and some control registers are maintained by the power source on the VBAK pin, allowing them to operate from battery or backup capacitor power when V_{DD} drops below a set threshold. Each functional block is described below.

Memory Operation

The FM33xx products are available in memory sizes of 16Kb and 256Kb. The two devices are software compatible; that is, both versions use consistent two-byte addressing for the memory device. This makes both devices the same as its standalone memory counterparts, such as the FM25L16.

Memory is organized in bytes, for example the 256Kb memory is 32,768 x 8. The memory is based on FRAM technology. Therefore it can be treated as RAM and is read or written at the speed of the SPI bus with no delays for write operations. It also offers effectively unlimited write endurance unlike other nonvolatile memory technologies. The SPI protocol is described on page 18.

The memory array can be write-protected by software. Two bits in the Status Register control the protection setting. Based on the setting, the protected addresses cannot be written. The Status Register & Write Protection is described in more detail on page 20.

Processor Companion

In addition to nonvolatile RAM, the FM33xx devices incorporate a real-time clock with alarm and highly integrated processor companion. The companion includes a low-V_{DD} reset, a programmable watchdog timer, a 16-bit nonvolatile event counter, a comparator for early power-fail detection or other purposes, and a 64-bit serial number.

Processor Supervisor

Supervisors provide a host processor two basic functions: Detection of power supply fault conditions and a watchdog timer to escape a software lockup condition. Both FM33xx devices have a reset pin (/RST) to drive a processor reset input during power faults, power-up, and software lockups. It is an open drain output with a weak internal pull-up to V_{DD}. This allows other reset sources to be wire-OR'd to the /RST pin. When V_{DD} is above the programmed trip point, /RST output is pulled weakly to V_{DD}. If V_{DD} drops below the reset trip point voltage level (V_{TP}), the /RST pin will be driven low. It will remain low until V_{DD} falls too low for circuit operation which is the V_{RST} level. When V_{DD} rises again above V_{TP}, /RST continues to drive low for at least 50 ms (t_{RPU}) to ensure a robust system reset at a reliable V_{DD} level. After t_{RPU} has been met, the /RST pin will return to the weak high state. While /RST is asserted, serial bus activity is locked out even if a transaction occurred as V_{DD} dropped below V_{TP}. A memory operation started while V_{DD} is above V_{TP} will be completed internally.

Table 1 below shows how bits VTP(1:0) control the trip point of the low-V_{DD} reset. They are located in register 18h, bits 0 and 1. The reset pin will drive low when V_{DD} is below the selected V_{TP} voltage, and the SPI interface and FRAM array will be locked out. Figure 2 illustrates the reset operation in response to a low V_{DD}.

Table 1.

VTP Setting	VTP1	VTP0
2.6V	0	0
2.75V	0	1
2.9V	1	0
3.0V	1	1

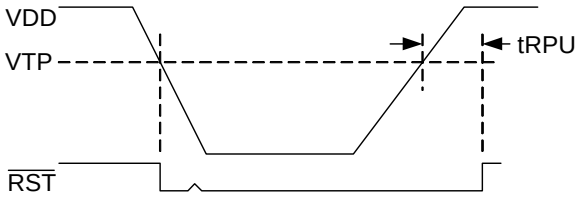


Figure 2. Low V_{DD} Reset

A watchdog timer can also be used to drive an active reset signal. The watchdog is a free-running programmable timer. The timeout period can be software programmed from 60 ms to 1.8 seconds in

60 ms increments via a 5-bit nonvolatile setting (register 0Ch).

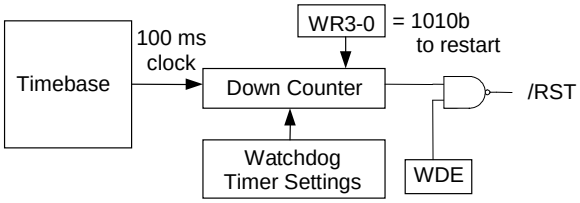


Figure 3. Watchdog Timer

The watchdog also incorporates a window timer feature that allows a delayed start. The starting time and ending time defines the window and each may be set independently. The starting time has 25 ms resolution and 0 ms to 775 ms range.

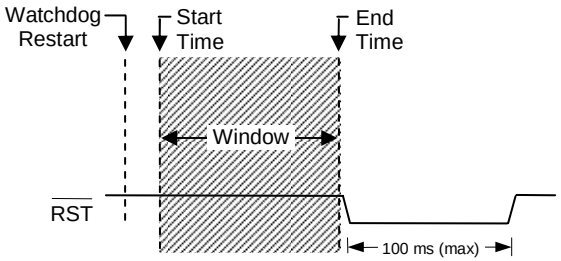


Figure 4. Window Timer

The watchdog EndTime value is located in register 0Ch, bits 4-0, the watchdog enable is bit 7. The watchdog is restarted by writing the pattern 1010b to the lower nibble of register 0Ah. Writing the correct pattern will also cause the timer to load new timeout values. Writing other patterns to this address will not affect its operation. Note the watchdog timer is free-running. Prior to enabling it, users should restart the timer as described above. This assures that the full timeout is provided immediately after enabling. The watchdog is disabled when V_{DD} drops below V_{TP}. Note setting the EndTime timeout setting to all zeroes (00000b) disables the timer to save power. The listing below summarizes the watchdog bits.

Watchdog StartTime	WDST4-0	0Bh, bits 4-0
Watchdog EndTime	WDET4-0	0Ch, bits 4-0
Watchdog Enable	WDE	0Ch, bit 7
Watchdog Restart	WR3-0	0Ah, bits 3-0
Watchdog Flags	EWDF,	09h, bit 7
	LWDF	09h, bit 6

The programmed StartTime value is a guaranteed maximum time while the EndTime value is a guaranteed minimum time, and both vary with temperature and V_{DD} voltage. The watchdog has two additional controls associated with its operation. The nonvolatile enable bit WDE allows the /RST to go active if the watchdog reaches the timeout without being restarted. If a reset occurs, the timer will restart on the rising edge of the reset pulse. If WDE is not enabled, the watchdog timer still runs but has no effect on /RST. The second control is a nibble that restarts the timer, thus preventing a reset. The timer should be restarted after changing the timeout value.

This procedure must be followed to properly load the watchdog registers:

		Address
1.	Write the StartTime value	0Bh
2.	Write the EndTime value and WDE=1	0Ch
3.	Issue a Restart command	0Ah

The restart command in step 3 must be issued before t_{DOG2}, which was programmed in step 2. The window timer starts counting when the restart command is issued.

Manual Reset

The /RST is a bi-directional signal allowing the FM33xx to filter and de-bounce a manual reset switch. The /RST input detects an external low condition and responds by driving the /RST signal low for 100 ms (max.). This effectively filters and de-bounces a reset switch. After this timeout (t_{RPW}), the user may continue pulling down on the /RST pin, but SPI commands will not be locked out.

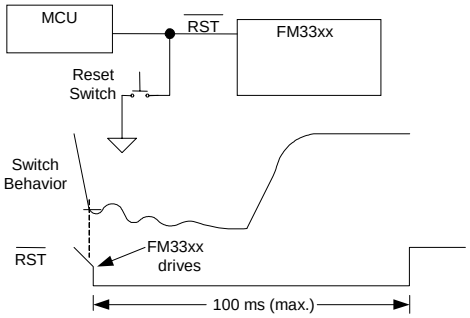


Figure 5. Manual Reset

Note the internal weak pull-up eliminates the need for additional external components.

Reset Flags

In case of a reset condition, a flag bit will be set to indicate the source of the reset. A low-V_{DD} reset is indicated by the POR bit, register 09h bit 5. There are two watchdog reset flags - one for an early fault (EWDF) and the other for a late fault (LWDF), located in register 09h bits 7 and 6. A manual reset will result in no flag being set, so the absence of a flag is a manual reset. Note that the bits are set in response to reset sources but they must be cleared by the user. It is possible to read the register and have

both sources indicated if both have occurred since the user cleared them.

Power Fail Comparator

An analog comparator compares the PFI input pin to an onboard 1.5V reference. When the PFI input voltage drops below this threshold, the comparator will drive the PFO pin to a low state. The comparator has 100 mV of hysteresis (rising voltage only) to reduce noise sensitivity. The most common application of this comparator is to create an early warning power fail interrupt (NMI). This can be accomplished by connecting the PFI pin to an upstream power supply via a resistor divider. An application circuit is shown below. The comparator is a general purpose device and its application is not limited to the NMI function.

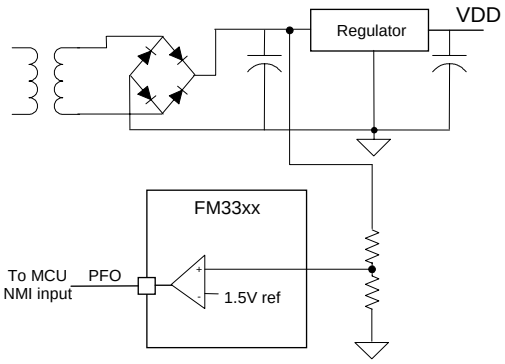


Figure 6. Comparator as a Power-Fail Warning

If the power-fail comparator is not used, the PFI pin should be tied to either V_{DD} or V_{SS}. Note that the PFO output will drive to V_{DD} or V_{SS} as well.

Event Counter

The FM33xx offers the user a nonvolatile 16-bit event counter. The input pin CNT has a programmable edge detector. The CNT pin clocks the counter. The counter is located in registers 0E-0Fh. When the programmed edge polarity occurs, the counter will increment its count value. The register value is read by setting the RC bit (register 0Dh, bit 3) to 1. This takes a snapshot of the counter byte allowing a stable value even if a count occurs during the read. The register value can be written by first setting the WC bit (register 0Dh, bit 2) to 1. The user then may clear or preset the counter by writing to registers 0E-0Fh. Counts are blocked when the WC bit is set, so the user must clear the bit to allow counts.

The counter polarity control bit is CP, register 0Dh bit 0. When CP is 0, the counter increments on a falling edge of CNT, and when CP is set to 1, the counter increments on a rising edge of CNT. The polarity bit CP is nonvolatile.

Figure 7. Event Counter

There is also a control bit that allows the user to define the counter as nonvolatile or battery-backed. The counter is nonvolatile when the NVC bit (register 0Dh, bit 7) is logic 1 and battery-backed when the NVC bit is logic 0. Setting the counter mode to battery-backed allows counter operation under V_{BAK} (as well as V_{DD}) power. The lowest operating voltage for battery-backed mode is 2.0V. When set to "nonvolatile" mode, the counter operates only when V_{DD} is applied and is above the V_{TP} voltage.

The event counter may be programmed to detect a tamper event, such as the system's case or access door being opened. A normally closed switch is tied to the CNT pin and the other contact to the case chassis, usually ground. The typical solution uses a pullup resistor on the CNT pin and will continuously draw battery current. The FM33xx chip allows the user to invoke a polled mode, which occasionally samples the pin in order to minimize battery drain. It internally tries to pull the CNT pin up and if open circuit will be pulled up to a V_{IH} level, which will trip the edge detector and increment the event counter value. Setting the POLL bit (register 0Dh, bit 1) places the CNT pin into this mode. This mode allows the event counter to detect a rising edge tamper event but the user is restricted to operating in battery-backed mode (NVC=0) and using rising edge detection (CP=1). The CNT pin is polled once every 125ms. The additional average I_{BAK} current is less than 5nA. The polling timer circuit operates from the RTC, so the oscillator must be enabled for this to function properly.

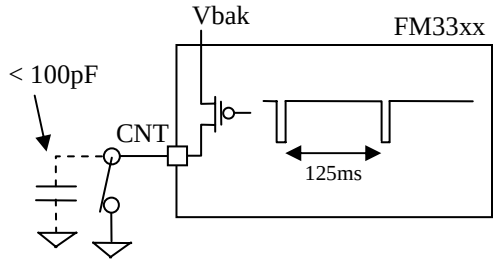


Figure 8. Polled Mode on CNT pin Detects Tamper to System Case

In the polled mode, the internal pullup circuit can source a limited amount of current. The maximum

capacitance (switch open circuit) allowed on the CNT pin is 100pF.

Serial Number

A memory location to write a 64-bit serial number is provided. It is a writeable nonvolatile memory block that can be locked by the user once the serial number is set. The 8 bytes of data and the lock bit are all accessed via unique op-codes for the RTC and Processor Companion registers. Therefore the serial number area is separate and distinct from the memory array. The serial number registers can be written an unlimited number of times, so these locations are general purpose memory. *However once the lock bit is set, the values cannot be altered and the lock cannot be removed.* Once locked the serial number registers can still be read by the system.

The serial number is located in registers 10h to 17h. The lock bit is SNL, register 18h bit 7. Setting the SNL bit to a 1 disables writes to the serial number registers, and *the SNL bit cannot be cleared.*

Alarm

The alarm function compares user-programmed values to the corresponding time/date values and operates under V_{DD} or V_{BAK} power. When a match occurs, an alarm event occurs. The alarm drives an internal flag AF (register 00h, bit 6) and may drive the ACS pin, if desired, by setting the AL/SW bit (register 18h, bit 6) in the Companion Control register. The alarm condition is cleared by writing a '0' to the AF bit.

There are five alarm match fields. They are Month, Date, Hours, Minutes, and Seconds. Each of these fields also has a Match bit that is used to determine if the field is used in the alarm match logic. Setting the Match bit to '0' indicates that the corresponding field will be used in the match process.

Depending on the Match bits, the alarm can occur as specifically as one particular second on one day of the month, or as frequently as once per second continuously. The MSB of each Alarm register is a Match bit. Examples of the Match bit settings are shown in Table 3. Selecting none of the match bits (all '1's) indicates that no match is required. The alarm occurs every second. Setting the match select bit for seconds to '0' causes the logic to match the seconds alarm value to the current time of day. Since a match will occur for only one value per minute, the alarm occurs once per minute. Likewise setting the seconds and minutes match select bits causes an exact match of these values. Thus, an alarm will occur once per hour. Setting seconds, minutes, and hours causes a match once per day. Lastly, selecting all match-values causes an exact time and date match. Selecting other bit combinations will not produce meaningful results, however the alarm circuit will follow the functions described.

There are two ways a user can detect an alarm event, by reading the AF flag or monitoring the ACS pin. The interrupt pin on the host processor may be used to detect an alarm event. The AF flag in register 00h (bit 6) will indicate that a time/date match has occurred. The AF flag will be set to '1' when a match occurs. The AEN bit must be set to enable the AF flag on alarm matches. The flag and ACS pin will remain in this state until the AF bit is cleared by writing it to a '0'. Clearing the AEN bit will prevent further matches from setting AF but will not automatically clear the AF flag.

The RTC alarm is integrated into the special function registers and shares its output pin with the 512Hz calibration and square wave outputs. When the RTC calibration mode is invoked by setting the CAL bit (register 00h, bit 2), the ACS output pin will be driven with a 512 Hz square wave and the alarm will continue to operate. Since most users only invoke the calibration mode during production this should have no impact on the otherwise normal operation of the alarm.

The ACS output may also be used to drive the system with a frequency other than 512 Hz. The AL/SW bit (register 18h, bit 6) must be '0'. A user-selectable frequency is provided by F0 and F1 (register 18h, bits 4 and 5). The other frequencies are 1, 4096, and 32768 Hz. If a continuous frequency output is enabled with CAL mode, the alarm function will not be available.

Following is a summary table that shows the relationship between register control settings and the state of the ACS pin.

Table 2.

State of Register Bit			Function of ACS pin
CAL	AEN	AL/SW	
0	1	1	/Alarm
0	X	0	Sq Wave out
1	X	X	512 Hz out
0	0	1	Hi-Z

Table 3. Alarm Match Bit Examples

Seconds	Minutes	Hours	Date	Months	Alarm condition
1	1	1	1	1	No match required = alarm 1/second
0	1	1	1	1	Alarm when seconds match = alarm 1/minute
0	0	1	1	1	Alarm when seconds, minutes match = alarm 1/hour
0	0	0	1	1	Alarm when seconds, minutes, hours match = alarm 1/date
0	0	0	0	1	Alarm when seconds, minutes, hours, date match = alarm 1/month

Real-time Clock Operation

The real-time clock (RTC) is a timekeeping device that can be capacitor- or battery-backed for permanently-powered operation. It offers a software calibration feature that allows high accuracy.

The RTC consists of an oscillator, clock divider, and a register system for user access. It divides down the 32.768 kHz time-base and provides a minimum resolution of seconds (1Hz). Static registers provide the user with read/write access to the time values. It includes registers for seconds, minutes, hours, day-of-the-week, date, months, and years. A block diagram shown in Figure 9 illustrates the RTC function.

The user registers are synchronized with the timekeeper core using R and W bits in register 00h. The R bit is used to read the time. Changing the R bit from 0 to 1 transfers timekeeping information from the core into the user registers 02-08h that can be read by the user. If a timekeeper update is pending when R is set, then the core will be updated prior to loading the user registers. The user registers are frozen and will not be updated again until the R bit is cleared to a '0'.

The W bit is used to write new time/date values. Setting the W bit to a '1' stops the RTC and allows the timekeeping core to be written with new data. Clearing it to '0' causes the RTC to start running based on the new values loaded in the timekeeper core. The RTC may be synchronized to another clock source. On the 8th clock of the write to register 00h (W=0), the RTC starts counting with a timebase that has been reset to zero milliseconds.

Note: Users should be certain not to load invalid values, such as FFh, to the timekeeping registers. Updates to the timekeeping core occur continuously except when locked.

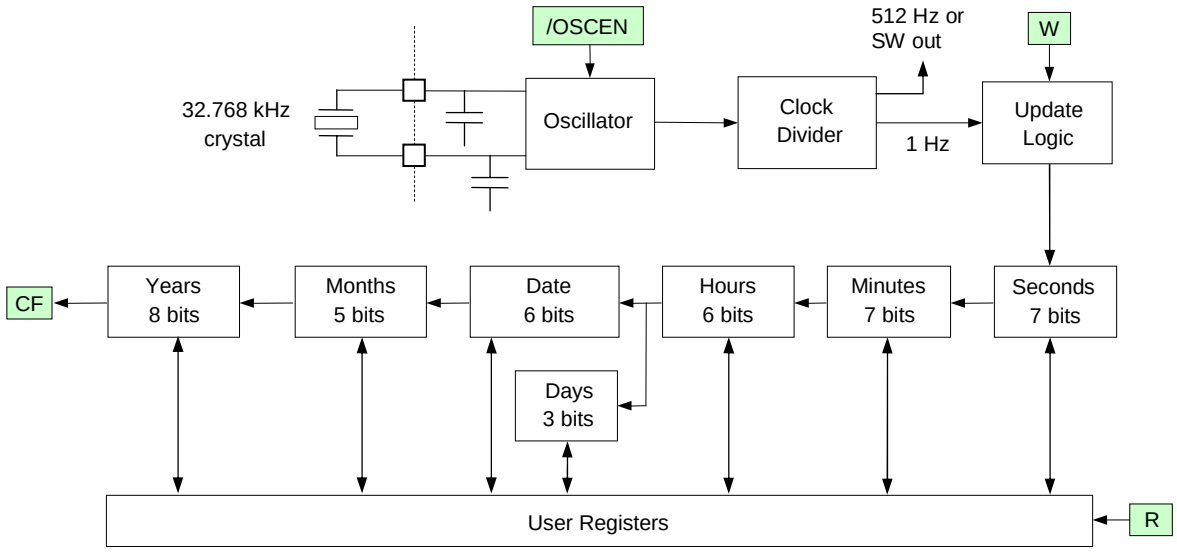


Figure 9. Real-time Clock Core Block Diagram

Backup Power

The real-time clock and alarm are intended to be permanently powered. When the primary system power fails, the voltage on the VDD pin will drop. When the VDD voltage is less than V_{SW}, the RTC (and event counter) will switch to the backup power supply on VBAK. The clock operates at extremely low current in order to maximize battery or capacitor life. However, an advantage of combining a clock function with FRAM memory is that data is not lost regardless of the backup power source.

Trickle Charger

To facilitate capacitor backup, the VBAK pin can optionally provide a trickle charge current. When the VBC bit (register 18h bit 3) is set to a '1', the V_{BAK} pin will source approximately 80 µA until V_{BAK} reaches V_{DD}. This charges the capacitor to V_{DD} without an external diode and resistor charger. There is a Fast Charge mode which is enabled by the FC bit (register 18h, bit 2). In this mode the trickle charger current is set to approximately 1 mA, allowing a large backup capacitor to charge more quickly.

- In the case where no battery is used, the V_{BAK} pin should be tied to V_{SS}.

Note: systems using lithium batteries should clear the VBC bit to 0 to prevent battery charging. The VBAK circuitry includes an internal 1 KΩ series resistor as a safety element.

Calibration

When the CAL bit in register 00h is set to a '1', the clock enters calibration mode. The FM33xx devices employ a digital method for calibrating the crystal oscillator frequency. The digital calibration scheme applies a digital correction to the RTC counters based on the calibration settings, CALS and CAL.4-0. In calibration mode (CAL=1), the ACS pin is driven with a 512 Hz (nominal) square wave and the alarm is temporarily unavailable. Any measured deviation from 512 Hz translates into a timekeeping error. The user measures the frequency and writes the appropriate correction value to the calibration register. The correction codes are listed in the table below. For convenience, the table also shows the frequency error in ppm. Positive ppm errors require a negative adjustment that removes pulses. Negative ppm errors require a positive correction that adds pulses. Positive ppm adjustments have the CALS (sign) bit set to 1, where as negative ppm adjustments have CALS = 0. After calibration, the clock will have a maximum error of ± 2.17 ppm or ± 0.09 minutes per month at the calibrated temperature.

The user will not be able to see the effect of the calibration setting on the 512 Hz output. The addition or subtraction of digital pulses occurs after the 512Hz output.

The calibration setting is stored in FRAM so it is not lost should the backup source fail. It is accessed with bits CAL.4-0 in register 01h. This value only can be written when the CAL bit is set to a 1. To exit the calibration mode, the user must clear the CAL bit to a logic 0. When the CAL bit is 0, the ACS pin will revert to the function according to Table 2.

Crystal Type

The crystal oscillator is designed to use a 12.5pF crystal without the need for external components, such as loading capacitors. The FM33xx device has built-in loading capacitors that match the crystal.

If a 32.768kHz crystal is not used, an external oscillator may be connected to the FM33xx. Apply the oscillator to the X1 pin. Its high and low voltage levels can be driven rail-to-rail or amplitudes as low as approximately 500mV p-p. To ensure proper operation, a DC bias must be applied to the X2 pin. It should be centered between the high and low levels on the X1 pin. This can be accomplished with a voltage divider.

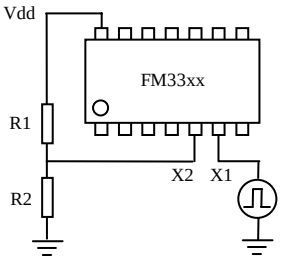


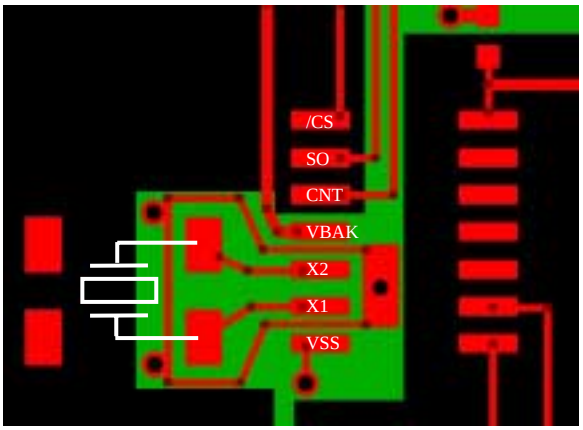
Figure 10. External Oscillator

In the example, R1 and R2 are chosen such that the X2 voltage is centered around the oscillator drive levels. If you wish to avoid the DC current, you may choose to drive X1 with an external clock and X2 with an inverted clock using a CMOS inverter.

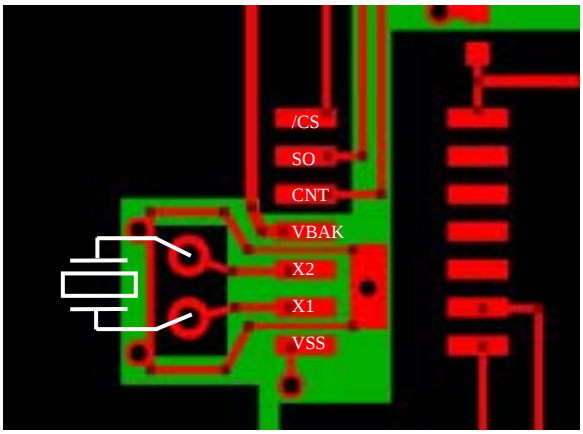
Layout Recommendations

The X1 and X2 crystal pins employ very high impedance circuits and the oscillator connected to these pins can be upset by noise or extra loading. To reduce RTC clock errors from signal switching noise, a guard ring should be placed around these pads and the guard ring grounded. High speed SPI traces should be routed away from the X1/X2 pads. The X1 and X2 trace lengths should be less than 5 mm. The

use of a ground plane on the backside or inner board layer is preferred. See layout example. Red is the top layer, green is the bottom layer.



Layout for Surface Mount Crystal
(red = top layer, green = bottom layer)



Layout for Through Hole Crystal
(red = top layer, green = bottom layer)

Table 4. Digital Calibration Adjustments

Positive Calibration for slow clocks: Calibration will achieve ± 2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	511.9989	0	2.17	000000
1	511.9989	511.9967	2.18	6.51	100001
2	511.9967	511.9944	6.52	10.85	100010
3	511.9944	511.9922	10.86	15.19	100011
4	511.9922	511.9900	15.20	19.53	100100
5	511.9900	511.9878	19.54	23.87	100101
6	511.9878	511.9856	23.88	28.21	100110
7	511.9856	511.9833	28.22	32.55	100111
8	511.9833	511.9811	32.56	36.89	101000
9	511.9811	511.9789	36.90	41.23	101001
10	511.9789	511.9767	41.24	45.57	101010
11	511.9767	511.9744	45.58	49.91	101011
12	511.9744	511.9722	49.92	54.25	101100
13	511.9722	511.9700	54.26	58.59	101101
14	511.9700	511.9678	58.60	62.93	101110
15	511.9678	511.9656	62.94	67.27	101111
16	511.9656	511.9633	67.28	71.61	110000
17	511.9633	511.9611	71.62	75.95	110001
18	511.9611	511.9589	75.96	80.29	110010
19	511.9589	511.9567	80.30	84.63	110011
20	511.9567	511.9544	84.64	88.97	110100
21	511.9544	511.9522	88.98	93.31	110101
22	511.9522	511.9500	93.32	97.65	110110
23	511.9500	511.9478	97.66	101.99	110111
24	511.9478	511.9456	102.00	106.33	111000
25	511.9456	511.9433	106.34	110.67	111001
26	511.9433	511.9411	110.68	115.01	111010
27	511.9411	511.9389	115.02	119.35	111011
28	511.9389	511.9367	119.36	123.69	111100
29	511.9367	511.9344	123.70	128.03	111101
30	511.9344	511.9322	128.04	132.37	111110
31	511.9322	511.9300	132.38	136.71	111111

Negative Calibration for fast clocks: Calibration will achieve ± 2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	512.0011	0	2.17	000000
1	512.0011	512.0033	2.18	6.51	000001

2	512.0033	512.0056	6.52	10.85	000010
3	512.0056	512.0078	10.86	15.19	000011
4	512.0078	512.0100	15.20	19.53	000100
5	512.0100	512.0122	19.54	23.87	000101
6	512.0122	512.0144	23.88	28.21	000110
7	512.0144	512.0167	28.22	32.55	000111
8	512.0167	512.0189	32.56	36.89	001000
9	512.0189	512.0211	36.90	41.23	001001
10	512.0211	512.0233	41.24	45.57	001010
11	512.0233	512.0256	45.58	49.91	001011
12	512.0256	512.0278	49.92	54.25	001100
13	512.0278	512.0300	54.26	58.59	001101
14	512.0300	512.0322	58.60	62.93	001110
15	512.0322	512.0344	62.94	67.27	001111
16	512.0344	512.0367	67.28	71.61	010000
17	512.0367	512.0389	71.62	75.95	010001
18	512.0389	512.0411	75.96	80.29	010010
19	512.0411	512.0433	80.30	84.63	010011
20	512.0433	512.0456	84.64	88.97	010100
21	512.0456	512.0478	88.98	93.31	010101
22	512.0478	512.0500	93.32	97.65	010110
23	512.0500	512.0522	97.66	101.99	010111
24	512.0522	512.0544	102.00	106.33	011000
25	512.0544	512.0567	106.34	110.67	011001
26	512.0567	512.0589	110.68	115.01	011010
27	512.0589	512.0611	115.02	119.35	011011
28	512.0611	512.0633	119.36	123.69	011100
29	512.0633	512.0656	123.70	128.03	011101
30	512.0656	512.0678	128.04	132.37	011110
31	512.0678	512.0700	132.38	136.71	011111

Register Map

The RTC and processor companion functions are accessed via 30 special function registers, which are mapped to unique op-codes. The interface protocol is described on page 17. The registers contain timekeeping data, alarm settings, control bits, and information flags. A description of each register follows the summary table.

Register Map Summary Table

Battery-backed = Nonvolatile = BB/NV User Programmable =

Address	D7	D6	D5	D4	D3	D2	D1	D0	Function	Range
1Dh	/Match	0	0	10 mo	Alarm months				Alarm Month	01-12
1Ch	/Match	0	10 date		Alarm date				Alarm Date	01-31
1Bh	/Match	0	Alarm 10 hours		Alarm hours				Alarm Hours	00-23
1Ah	/Match	Alarm 10 minutes			Alarm minutes				Alarm Minutes	00-59
19h	/Match	Alarm 10 seconds			Alarm seconds				Alarm Seconds	00-59
18h	SNL	AL/SW	F1	F0	VBC	FC	VTP1	VTP0	Companion Control	
17h	Serial Number Byte 7								Serial Number 7	FFh
16h	Serial Number Byte 6								Serial Number 6	FFh
15h	Serial Number Byte 5								Serial Number 5	FFh
14h	Serial Number Byte 4								Serial Number 4	FFh
13h	Serial Number Byte 3								Serial Number 3	FFh
12h	Serial Number Byte 2								Serial Number 2	FFh
11h	Serial Number Byte 1								Serial Number 1	FFh
10h	Serial Number Byte 0								Serial Number 0	FFh
0Fh	Event Counter Byte 1								Event Counter 1	FFh
0Eh	Event Counter Byte 0								Event Counter 0	FFh
0Dh	NVC	-	-	-	RC	WC	POLL	CP	Event Counter Control	
0Ch	WDE	-	-	WDSET4	WDET3	WDET2	WDET1	WDET0	Watchdog Control	
0Bh	-	-	-	WDST4	WDST3	WDST2	WDST1	WDST0	Watchdog Control	
0Ah	-	-	-	-	WR3	WR2	WR1	WR0	Watchdog Restart	
09h	EWDF	LWDF	POR	LB	-	-	-	-	Watchdog Flags	
08h	10 years				years				Years	00-99
07h	0	0	0	10 mo	months				Month	01-12
06h	0	0	10 date		date				Date	01-31
05h	0	0	0	0	0	day			Day	01-07
04h	0	0	10 hours		hours				Hours	00-23
03h	0	10 minutes			minutes				Minutes	00-59
02h	0	10 seconds			seconds				Seconds	00-59
01h	-	-	CALS	CAL4	CAL3	CAL2	CAL1	CAL0	CAL/Control	
00h	/OSCEN	AF	CF	AEN	reserved	CAL	W	R	RTC/Alarm Control	

Note: When the device is first powered up and programmed, all timekeeping registers must be written because the battery-backed register values cannot be guaranteed. The table below shows the default values of the non-volatile registers and some of the battery-backed bits. All other register values should be treated as unknown.

Default Register Values

Address	Hex Value
1Dh	0x81
1Ch	0x81
1Bh	0x80
1Ah	0x80
19h	0x80
18h	0x40
17h	0x00
16h	0x00
15h	0x00
14h	0x00
13h	0x00

Address	Hex Value
12h	0x00
11h	0x00
10h	0x00
0Fh	0x00
0Eh	0x00
0Dh	0x01
0Ch	0x00
0Bh	0x00
01h	0x00
00h	0x80

Register Description

Address **Description**

1Dh	**Alarm – Month**						
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	0	10 Month	Month.3	Month.2	Month.1	Month.0
	Contains the alarm value for the month and the mask bit to select or deselect the Month value.							
/M	Match. Setting this bit to 0 causes the Month value to be used in the alarm match logic. Setting this bit to 1 causes the match circuit to ignore the Month value. Battery-backed, read/write.							
1Ch	**Alarm – Date**						
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0
	Contains the alarm value for the date and the mask bit to select or deselect the Date value.							
/M	Match: Setting this bit to 0 causes the Date value to be used in the alarm match logic. Setting this bit to 1 causes the match circuit to ignore the Date value. Battery-backed, read/write.							
1Bh	**Alarm – Hours**						
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	10 hours.1	10 hours.0	Hours.3	Hours2	Hours.1	Hours.0
	Contains the alarm value for the hours and the mask bit to select or deselect the Hours value.							
/M	Match: Setting this bit to 0 causes the Hours value to be used in the alarm match logic. Setting this bit to 1 causes the match circuit to ignore the Hours value. Battery-backed, read/write.							
1Ah	**Alarm – Minutes**						
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0
	Contains the alarm value for the minutes and the mask bit to select or deselect the Minutes value							
/M	Match: Setting this bit to 0 causes the Minutes value to be used in the alarm match logic. Setting this bit to 1 causes the match circuit to ignore the Minutes value. Battery-backed, read/write.							
19h	**Alarm – Seconds**						
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0
	Contains the alarm value for the seconds and the mask bit to select or deselect the Seconds value.							
/M	Match: Setting this bit to 0 causes the Seconds value to be used in the alarm match logic. Setting this bit to 1 causes the match circuit to ignore the Seconds value. Battery-backed, read/write.							

18h	**Companion Control**						
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SNL	AL/SW	F1	F0	VBC	FC	VTP1	VTP0
SNL	Serial Number Lock: Setting to a '1' makes registers 10h to 17h and SNL read-only. SNL cannot be cleared once set to '1'. Nonvolatile, read/write.							
AL/SW	Alarm/Square Wave Select: When set to '1', the alarm match drives the ACS pin as well as the AF flag. When set to '0', the selected Square Wave Freq will be driven on the ACS pin, and an alarm match only sets the AF flag. Nonvolatile, read/write.							
F(1:0)	Square Wave Freq Select: These bits select the frequency on the ACS pin when the CAL and AL/SW bits are both '0'. Nonvolatile. Setting F(1:0) — Setting F(1:0) 1 Hz 00 (default) — 4096 Hz 10 512 Hz 01 — 32768Hz 11							
VBC	VBAK Charger Control: Setting VBC to '1' (and FC=0) causes a 80 µA (1 mA if FC=1) trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Battery-backed, read/write.							
FC	Fast Charge: Setting FC to '1' (and VBC=1) causes a ~1 mA trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Battery-backed, read/write.							
VTP(1:0)	VTP Select. These bits control the reset trip point for the low-V_{DD} reset function. When V_{DD} is below the selected V_{TP} voltage, the reset pin /RST will drive low and the SPI interface will be locked out. Nonvolatile, read/write.							

	Setting VTP(1:0) 2.60V 00 (factory default) 2.75V 01 2.9V 10 3.0V 11
17h	**Serial Number Byte 7**

D7	D6	D5	D4	D3	D2	D1	D0
SN.63	SN.62	SN.61	SN.60	SN.59	SN.58	SN.57	SN.56

16h	**Serial Number Byte 6**

D7	D6	D5	D4	D3	D2	D1	D0
SN.55	SN.54	SN.53	SN.52	SN.51	SN.50	SN.49	SN.48

15h	**Serial Number Byte 5**

D7	D6	D5	D4	D3	D2	D1	D0
SN.47	SN.46	SN.45	SN.44	SN.43	SN.42	SN.41	SN.40

14h	**Serial Number Byte 4**

D7	D6	D5	D4	D3	D2	D1	D0
SN.39	SN.38	SN.37	SN.36	SN.35	SN.34	SN.33	SN.32

13h	**Serial Number Byte 3**

D7	D6	D5	D4	D3	D2	D1	D0
SN.31	SN.30	SN.29	SN.28	SN.27	SN.26	SN.25	SN.24

12h	**Serial Number Byte 2**

D7	D6	D5	D4	D3	D2	D1	D0
SN.23	SN.22	SN.21	SN.20	SN.19	SN.18	SN.17	SN.16

11h	**Serial Number Byte 1**

D7	D6	D5	D4	D3	D2	D1	D0
SN.15	SN.14	SN.13	SN.12	SN.11	SN.10	SN.9	SN.8

10h	**Serial Number Byte 0**

D7	D6	D5	D4	D3	D2	D1	D0
SN.7	SN.6	SN.5	SN.4	SN.3	SN.2	SN.1	SN.0

All serial number bytes are read/write when SNL=0, read-only when SNL=1. Nonvolatile.

0Fh	**Event Counter Byte 1**

D7	D6	D5	D4	D3	D2	D1	D0
EC.15	EC.14	EC.13	EC.12	EC.11	EC.10	EC.9	EC.8

Event Counter Byte 1. Increments on programmed edge event on CNT input. Nonvolatile when NVC=1, Battery-backed when NVC=0, read/write.

0Eh	**Event Counter Byte 0**

D7	D6	D5	D4	D3	D2	D1	D0
EC.7	EC.6	EC.5	EC.4	EC.3	EC.2	EC.1	EC.0

Event Counter Byte 0. Increments on programmed edge event on CNT input. Nonvolatile when NVC=1, Battery-backed when NVC=0, read/write.

0Dh	**Event Counter Control**

D7	D6	D5	D4	D3	D2	D1	D0
NVC	-	-	-	RC	WC	POLL	CP

NVC	Nonvolatile/Volatile Counter: Setting this bit to 1 makes the counter nonvolatile and counter operates only when V_{DD} is greater than V_{TP}. Setting this bit to 0 makes the counter volatile, which allows counter operation under V_{BAK} or V_{DD} power. Nonvolatile, read/write.
RC	Read Counter. Setting this bit to 1 takes a snapshot of the two counter bytes allowing the system to read the values without missing count events. The RC bit will be automatically cleared.
WC	Write Counter. Setting this bit to a 1 allows the user to write the counter bytes. While WC=1, the counter is blocked from count events on the CNT pin. The WC bit must be cleared by the user to activate the counter.
POLL	Polled Mode: When POLL=1, the CNT pin is sampled for 30µs every 125ms. If POLL is set, the NVC bit is internally cleared and the CP bit is set to detect a rising edge. The RTC oscillator must be enabled (/OSCEN=0)

	to operate in polled mode. When POLL=0, CNT pin is continuously active. Nonvolatile, read/write.
CP	The CNT pin detects falling edges when CP = 0, rising edges when CP = 1. Nonvolatile, read/write.

0Ch **Watchdog Control**

D7	D6	D5	D4	D3	D2	D1	D0
WDE	-	-	WDET4	WDET3	WDET2	WDET1	WDET0

WDE: Watchdog Enable: When WDE=1, a watchdog timer fault will cause the /RST signal to go active. When WDE = 0 the timer runs but has no effect on the /RST pin. Nonvolatile, read/write.

WDET(4:0): Watchdog EndTime: Sets the ending time for the watchdog window timer with 60 ms (min.) resolution. The window timer allow independent leading and trailing edges (start and end of window) to be set. New watchdog timeouts are loaded when the timer is restarted by writing the 1010b pattern to WR(3:0). To save power (disable timer circuit), the EndTime may be set to all zeroes. Nonvolatile, read/write.

Watchdog EndTime		WDET4	WDET3	WDET2	WDET1	WDET0
Disables Timer		0	0	0	0	0
(min.)	(max.)					
60 ms	200 ms	0	0	0	0	1
120 ms	400 ms	0	0	0	1	0
180 ms	600 ms	0	0	0	1	1
⋮	⋮					
1200 ms	4000 ms	1	0	1	0	0
1260 ms	4200 ms	1	0	1	0	1
1320 ms	4400 ms	1	0	1	1	0
⋮	⋮					
1740 ms	5800 ms	1	1	1	0	1
1800 ms	6000 ms	1	1	1	1	0
1860 ms	6200 ms	1	1	1	1	1

0Bh **Watchdog Control**

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	WDST4	WDST3	WDST2	WDST1	WDST0

WDST(4:0): Watchdog StartTime. Sets the starting time for the watchdog window timer with 25 ms (max.) resolution. The window timer allow independent leading and trailing edges (start and end of window) to be set. New watchdog timer settings are loaded when the timer is restarted by writing the 1010b pattern to WR(3:0). Nonvolatile, read/write.

Watchdog StartTime		WDST4	WDST3	WDST2	WDST1	WDST0
0 ms (default)		0	0	0	0	0
(min.)	(max.)					
7.5 ms	25 ms	0	0	0	0	1
15.0 ms	50 ms	0	0	0	1	0
22.5 ms	75 ms	0	0	0	1	1
⋮	⋮					
150 ms	500 ms	1	0	1	0	0
157.5 ms	525 ms	1	0	1	0	1
165 ms	550 ms	1	0	1	1	0
⋮	⋮					
217.5 ms	725 ms	1	1	1	0	1
225 ms	750 ms	1	1	1	1	0
232.5 ms	775 ms	1	1	1	1	1

0Ah **Watchdog Restart**

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	WR3	WR2	WR1	WR0

WR(3:0): Watchdog Restart. Writing a pattern 1010b to WR(3:0) restarts the watchdog timer. The upper nibble contents do not affect this operation. Writing any pattern other than 1010b to WR3-0 has no effect on the watchdog. Write-only.

09h	**Watchdog Flags**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	EWDF	LWDF	POR	LB	-	-	-	-
EWDF	Early Watchdog Timer Fault Flag: When a watchdog restart occurs too early (before the programmed watchdog StartTime), the /RST pin is driven low and this flag is set. It must be cleared by the user. Note that both EWDF and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed, read/write.							
LWDF	Late Watchdog Timer Fault Flag: When either a watchdog restart occurs too late (after the programmed watchdog EndTime) or no restart occurs, the /RST pin is driven low and this flag is set. It must be cleared by the user. Note that both LWDF and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed, read/write.							
POR	Power-On Reset: When the /RST signal is activated by $V_{DD} < V_{TP}$, the POR bit will be set to 1. A manual reset will not set this flag. Note that one or both of the watchdog flags and the POR flag could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed, read/write. (internally set, user must clear bit)							
LB	Low Backup: If the V_{BAK} source drops to a voltage level insufficient to operate the RTC/alarm when $V_{DD}<V_{BAK}$, this bit will be set to '1'. All registers need to be re-initialized since the battery-backed register values should be treated as unknown. The user should clear it to 0 when initializing the system. Battery-backed. Read/Write (internally set, user must clear bit).							
08h	**Timekeeping – Years**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10 year.3	10 year.2	10 year.1	10 year.0	Year.3	Year.2	Year.1	Year.0
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0-99. Battery-backed, read/write.							
07h	**Timekeeping – Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10 Month	Month.3	Month.2	Month.1	Month.0
	Contains the BCD digits for the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1-12. Battery-backed, read/write.							
06h	**Timekeeping – Date of the month**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1-31. Battery-backed, read/write.							
05h	**Timekeeping – Day of the week**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day.2	Day.1	Day.0
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date. Battery-backed, read/write.							
04h	**Timekeeping – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 hours.1	10 hours.0	Hours.3	Hours2	Hours.1	Hours.0
	Contains the BCD value of hours in 24-hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0-23. Battery-backed, read/write.							
03h	**Timekeeping – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.							

02h	Timekeeping – Seconds							
	D7	D6	D5	D4	D3	D2	D1	D0
	0	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.							
01h	**CAL/Control**							
	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	CALS	CAL.4	CAL.3	CAL.2	CAL.1	CAL.0
CALS	Calibration Sign: Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base. This bit can be written only when CAL=1. Nonvolatile, read/write.							
CAL.4-0	Calibration Code: These five bits control the calibration of the clock. These bits can be written only when CAL=1. Nonvolatile, read/write.							
00h	**RTC/Alarm Control**							
	D7	D6	D5	D4	D3	D2	D1	D0
	$\overline{\text{OSCEN}}$	AF	CF	AEN	Reserved	CAL	W	R
/OSCEN	Oscillator Enable. When set to '1', the oscillator is halted. When set to '0', the oscillator runs. Disabling the oscillator can save battery power during storage. On a power-up without a V_{BAK} source or on a power-up after a V_{BAK} source has been applied, this bit is internally set to '1', which turns off the oscillator. Battery-backed, read/write.							
AF	Alarm Flag: This bit is set to 1 when the time and date match the values stored in the alarm registers with the Match bit(s) = 0. The user must clear it to '0'. Battery-backed. (internally set, user must clear bit)							
CF	Century Overflow Flag: This bit is set to a 1 when the values in the years register overflows from 99 to 00. This indicates a new century, such as going from 1999 to 2000 or 2099 to 2100. The user should record the new century information as needed. The user must clear the CF bit to '0'. Battery-backed. (internally set, user must clear bit)							
AEN	Alarm Enable: This bit enables the alarm function. When AEN is set (and CAL cleared), the ACS pin operates as an active-low alarm. The state of the ACS pin is detailed in Table 2. When AEN is cleared, no new alarm events that set the AF bit will be generated. Clearing the AEN bit does not automatically clear AF. Battery-backed.							
CAL	Calibration Mode: When CAL is set to 1, the clock enters calibration mode. When CAL is set to 0, the clock operates normally, and the ACS pin is controlled by the RTC alarm. Battery-backed, read/write.							
W	Write Time. Setting the W bit to 1 freezes updates of the user timekeeping registers. The user can then write them with updated values. Setting the W bit to 0 causes the contents of the time registers to be transferred to the timekeeping counters. Battery-backed, read/write.							
R	Read Time. Setting the R bit to '1' copies a static image of the timekeeping core and places it into the user registers. The user can then read them without concerns over changing values causing system errors. The R bit going from 0 to 1 causes the timekeeping capture, so the bit must be returned to 0 prior to reading again. Battery-backed, read/write.							
Reserved	Reserved bits. Do not use. Should remain set to 0.							

Serial Peripheral Interface – SPI Bus

The FM33xx employs a Serial Peripheral Interface (SPI) bus. It is specified to operate at speeds up to 16 MHz. This high-speed serial bus provides high performance serial communication to a host microcontroller. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The FM33xx devices operate in SPI Mode 0 and 3.

The SPI interface uses a total of four pins: clock, data-in, data-out, and chip select. A typical system configuration uses an FM33xx and a standalone SPI device with a microcontroller that has a dedicated SPI port, as Figure 10 illustrates. Note that the clock, data-in, and data-out pins are common among all devices. The /CS pins must be driven separately for the FM33xx and each additional SPI device.

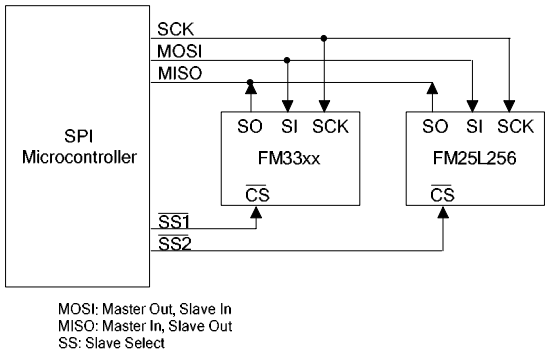


Figure 10. System Configuration with SPI port

For a microcontroller that has no dedicated SPI bus, a general purpose port may be used. To reduce hardware resources on the controller, it is possible to connect the two data pins together. Figure 11 shows a configuration that uses only three pins.

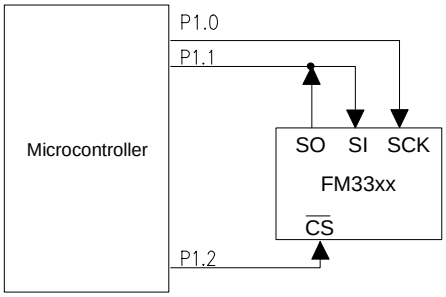
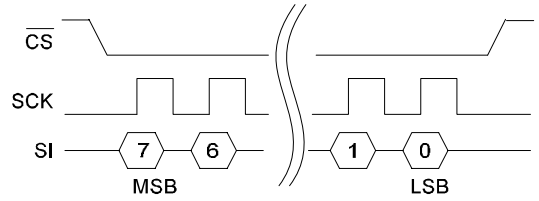


Figure 11. System Configuration without SPI port

Protocol Overview

The SPI interface is a synchronous serial interface using clock and data pins. It is intended to support multiple devices on the bus. Each device is activated using a chip select. Once chip select is activated by the bus master, the FM33xx will begin monitoring the clock and data lines. The relationship between the falling edge of /CS, the clock and data is dictated by the SPI mode. The device will make a determination of the SPI mode on the falling edge of each chip select. While there are four such modes, the FM33xx supports only modes 0 and 3. Figure 12 shows the required signal relationships for modes 0 and 3. For both modes, data is clocked into the FM33xx on the rising edge of SCK and data is expected on the first rising edge after /CS goes active. If the clock starts from a high state, it will fall prior to the first data transfer in order to create the first rising edge.

SPI Mode 0: CPOL=0, CPHA=0



SPI Mode 3: CPOL=1, CPHA=1

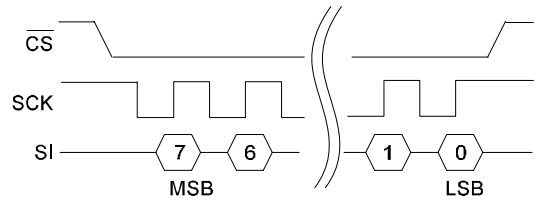


Figure 12. SPI Modes 0 & 3

The SPI protocol is controlled by op-codes. These op-codes specify the commands to the device. After /CS is activated the first byte transferred from the bus master is the op-code. Following the op-code, any addresses and data are then transferred. Note that the WREN and WRDI op-codes are commands with no subsequent data transfer.

Important: The /CS pin must go inactive after an operation is complete and before a new op-code can be issued. There is only one valid op-code per active chip select.

Data Transfer

All data transfers to and from the FM33xx occur in 8-bit groups. They are synchronized to the clock signal (SCK), and they transfer most significant bit (MSB) first. Serial inputs are registered on the rising edge of SCK. Outputs are driven from the falling edge of SCK.

Command Structure

There are eight commands called op-codes that can be issued by the bus master to the FM33xx. They are listed in the table below. These op-codes control the functions performed by the memory and Processor Companion. They can be divided into three categories. First, there are commands that have no subsequent operations. They perform a single function, such as, enabling a write operation. Second are commands followed by one data byte, either in or out. They operate on the Status Register. The third group includes commands for memory and Processor Companion transactions followed by address and one or more bytes of data.

Table 4. Op-code Commands

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110b
WRDI	Write Disable	0000 0100b
RDSR	Read Status Register	0000 0101b
WRSR	Write Status Register	0000 0001b
READ	Read Memory Data	0000 0011b
WRITE	Write Memory Data	0000 0010b
RDPC	Read Proc. Companion	0001 0011b
WRPC	Write Proc. Companion	0001 0010b

WREN – Set Write Enable Latch

The FM33xx will power up with writes disabled. The WREN command must be issued prior to any write operation. Sending the WREN op-code will allow the user to issue subsequent op-codes for write operations. These include writing the Status Register, writing the Processor Companion, and writing the memory.

Sending the WREN op-code causes the internal Write Enable Latch to be set. A flag bit in the Status Register, called WEL, indicates the state of the latch. WEL=1 indicates that writes are permitted. Attempting to write the WEL bit in the Status Register has no effect on the state of this bit. The WEL bit will automatically be cleared on the rising edge of /CS following a WRDI, WRSR, WRPC, or WRITE op-code. No other op-code affects the state of the WEL bit. This prevents further writes to the Status Register, FRAM memory, or the companion register space without another WREN command. Figure 13 below illustrates the WREN command bus configuration.

WRDI – Write Disable

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the Status Register and verifying that WEL=0. Figure 14 illustrates the WRDI command bus configuration.

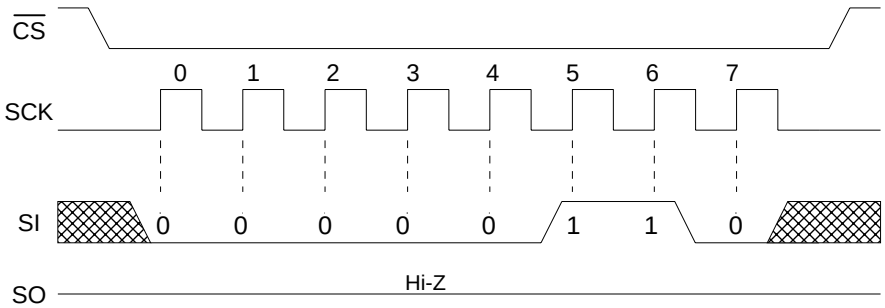


Figure 13. WREN Bus Configuration

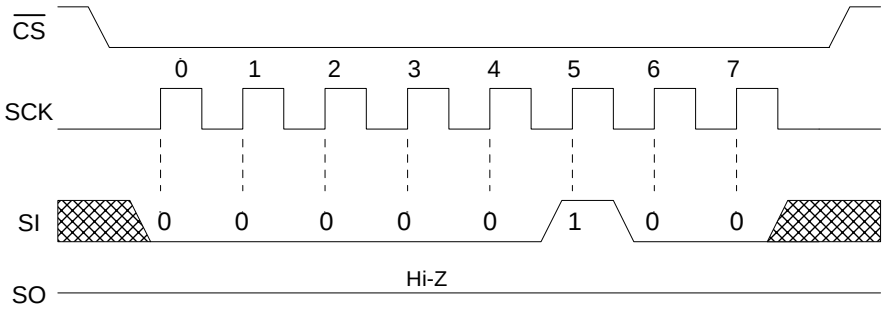


Figure 14. WRDI Bus Configuration

RDSR – Read Status Register

The RDSR command allows the bus master to verify the contents of the Status Register. Reading this register provides information about the current state of the write protection bits. Following the RDSR op-code, the FM33xx will return one byte with the contents of the Status Register. The Status Register is described in detail in a later section.

WRSR – Write Status Register

The WRSR command allows the user to select certain write protection features by writing a byte to the Status Register. Prior to sending the WRSR command, the user must send a WREN command to enable writes. Note that executing a WRSR command is a write operation and therefore clears the Write Enable Latch. The bus timings of RDSR and WRSR are shown below.

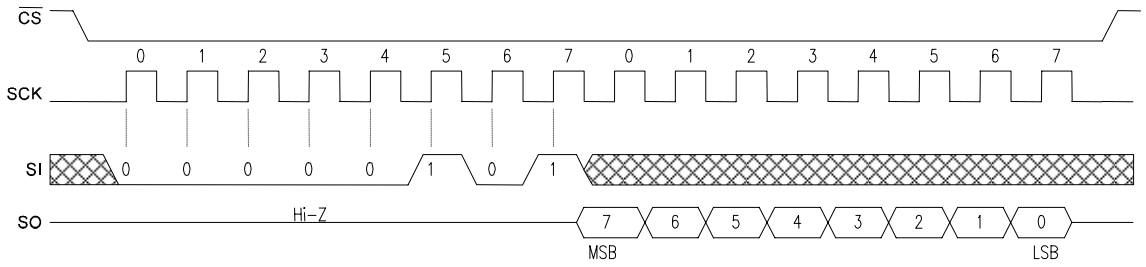


Figure 15. RDSR Bus Configuration

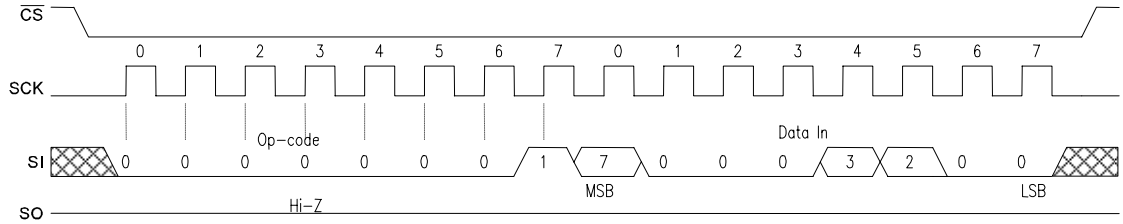


Figure 16. WRSR Bus Configuration

RDPC – Read Processor Companion

The RDPC command allows the bus master to verify the contents of the Processor Companion registers. Following the RDPC op-code, a single-byte register address is sent. The FM33xx will then return one or more bytes with the contents of the companion registers. When reading multiple data bytes, the internal register address will wrap around to 00h after 1Dh is reached.

WRPC – Write Processor Companion

The WRPC command is used to set companion control settings. A WREN command is required prior to sending the WRPC command. Following the WRPC op-code, a single-byte register address is sent. The controller then drives one or more bytes to program the companion registers. When writing multiple data bytes, the internal register address will wrap around to 00h after 1Dh is reached. The rising edge of /CS terminates a WRPC operation. See Figure 18.

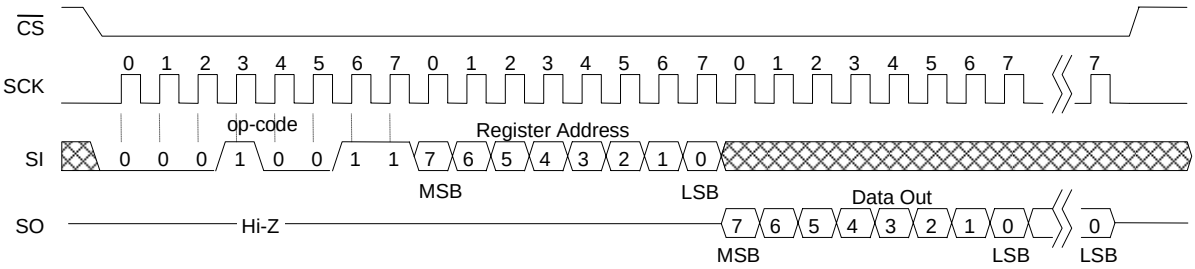


Figure 17. Processor Companion Read

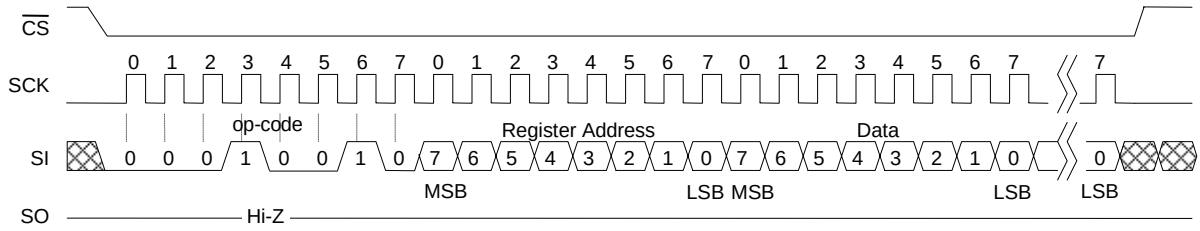


Figure 18. Processor Companion Write

Status Register & Write Protection

The write protection features of the FM33xx are multi-tiered. To write the memory, a WREN op-code must first be issued, followed by a WRITE op-code. A Status Register associated with the memory has a write enable latch bit (WEL) that is internally set when WREN is issued.

Writes to certain memory blocks are controlled by the Block Protect bits in the Status Register. The BP bits may be changed by using the WRSR command. The Status Register is organized as follows.

Table 5. Status Register

Bit	7	6	5	4	3	2	1	0
Name	0	1	0	0	BP1	BP0	WEL	0

Bits 7, 5, 4, and 0 are fixed at 0, bit 6 is fixed at 1, and none of these bits can be modified. Note that bit 0 (Ready in EEPROMs) is unnecessary as the FRAM writes in real-time and is never busy. The BP1 and BP0 control software write-protection features. They are nonvolatile (shaded yellow). The WEL flag indicates the state of the Write Enable Latch. Attempting to directly write the WEL bit in the Status Register has no effect on its state, since this bit is internally set and cleared via the WREN and WRDI commands, respectively. BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write-protected as shown in the following table.

Table 6. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	Upper ¼
1	0	Upper ½
1	1	All

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes.

Memory Operation

The SPI interface, which is capable of a relatively high clock frequency, highlights the fast write capability of the FRAM technology. Unlike SPI-bus EEPROMs, the FM33xx can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

Write Operation

All writes to the memory begin with a WREN op-code with /CS being asserted and deasserted. The next op-code is a WRITE. The WRITE op-code is followed by a two-byte address value. Table 7 shows the addressing scheme for each density. This is the starting address of the first data byte of the write operation. Subsequent bytes are data bytes, which are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and keeps /CS low. A write operation will be terminated when a write-protected address is directly accessed or when the device has internally incremented the address into a write-protected space. If the last address is reached (e.g. 7FFFh on the FM33256), the counter will roll over to 0000h. Data is written MSB first. The rising edge of /CS terminates a WRITE operation. A write operation is shown in Figure 19. Note: Although the WREN op-code is not shown in the timing diagram, it is required prior to sending the WRITE command.

EEPROMs use page buffers to increase their write throughput. This compensates for the technology's inherently slow write operations. FRAM memories do not have page buffers because each byte is written to the FRAM array immediately after it is clocked in (after the 8th clock). This allows any number of bytes to be written without page buffer delays.

Read Operation

After the falling edge of /CS, the bus master can issue a READ op-code. Following the READ command is a two-byte address value. Table 7 shows the addressing scheme for each density. This is the starting address of the first byte of the read operation.

After the op-code and address are issued, the device drives out the read data on the next 8 clocks. The SI input is ignored during read data bytes. Subsequent bytes are data bytes, which are read out sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and /CS is low. If the last address is reached (e.g. 7FFFh on the FM33256), the counter will roll over to 0000h. Data is read MSB first. The rising edge of /CS terminates a READ operation. A read operation is shown in Figure 20.

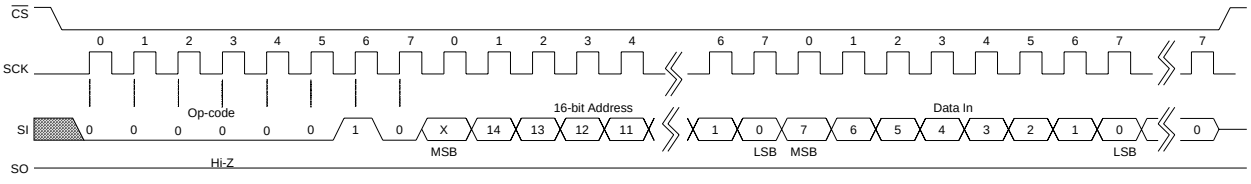


Figure 19. Memory Write

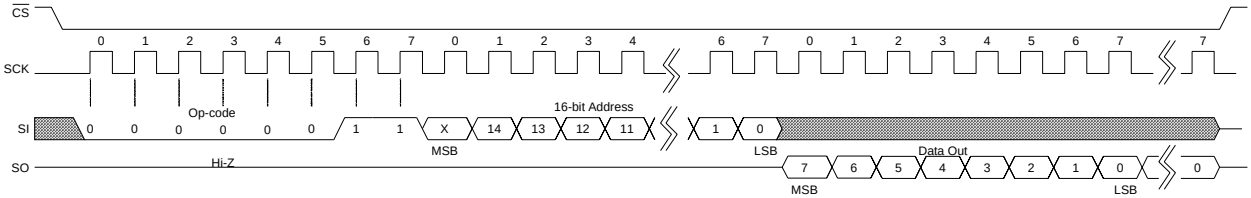


Figure 20. Memory Read

Addressing FRAM Array in the FM33xx Family

The FM33xx devices include 256Kb and 16Kb memory densities. The following 2-byte address field is shown for each density.

Table 7. Two-Byte Memory Address

Part #		1st Address Byte									2nd Address Byte							
FM33256		X	A14	A13	A12	A11	A10	A9	A8		A7	A6	A5	A4	A3	A2	A1	A0
FM3316		X	X	X	X	X	A10	A9	A8		A7	A6	A5	A4	A3	A2	A1	A0

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +5.0V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +5.0V and $V_{IN} < V_{DD}$+1.0V
V_{BAK}	Backup Supply Voltage	-1.0V to +4.5V
T_{STG}	Storage Temperature	-55°C to + 125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	300° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-B) - Charged Device Model (JEDEC Std JESD22-C101-A)	 TBD TBD
	Package Moisture Sensitivity Level	MSL-1

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Main Power Supply	2.7	-	3.6	V	1
I_{DD}	V_{DD} Supply Current (VBC=0) @ SCK = 1.0 MHz @ SCK = 16.0 MHz			 1.1 16.0	 mA mA	2
I_{SB}	Standby Current Trickle Charger Off (VBC=0)			 50	 µA	3
V_{BAK}	RTC Backup Voltage	2.0	3.0	3.6	V	4
I_{BAK}	RTC Backup Current			1	µA	5
I_{BAKTC}	Trickle Charge Current with V_{BAK}=0V Fast Charge Off (FC = 0) Fast Charge On (FC = 1)	 50 200		 120 2500	 µA µA	6
I_{QTC}	V_{DD} Quiescent Current (VBC=1)			70	µA	7
I_{QWD}	V_{DD} Quiescent Current (WDE=1)			25	µA	8
V_{TP0}	V_{DD} Trip Point Voltage, VTP(1:0) = 00b	2.55	2.6	2.70	V	9
V_{TP1}	V_{DD} Trip Point Voltage, VTP(1:0) = 01b	2.70	2.75	2.85	V	9
V_{TP2}	V_{DD} Trip Point Voltage, VTP(1:0) = 10b	2.80	2.9	2.97	V	9
V_{TP3}	V_{DD} Trip Point Voltage, VTP(1:0) = 11b	2.93	3.0	3.13	V	9
V_{RST}	V_{DD} for valid /RST @ I_{OL} = 80 µA at V_{OL} $V_{BAK} > V_{BAK}$ min $V_{BAK} < V_{BAK}$ min	 0 1.6			 V V	10
V_{SW}	Battery Switchover Voltage	2.0		2.7	V	
I_{LI}	Input Leakage Current			±1	µA	11
I_{LO}	Output Leakage Current			±1	µA	11
V_{IL}	Input Low Voltage All inputs except as listed below CNT battery-backed ($V_{DD} < V_{SW}$) CNT ($V_{DD} > V_{SW}$)	 -0.3 -0.3 -0.3		 0.3 V_{DD} 0.5 0.8	 V V V	12
V_{IH}	Input High Voltage All inputs except as listed below CNT battery-backed ($V_{DD} < V_{SW}$) CNT $V_{DD} > V_{SW}$ PFI	 0.7 V_{DD} V_{BAK} – 0.5 0.7 V_{DD} -		 V_{DD} + 0.3 V_{BAK} + 0.3 V_{DD} + 0.3 V_{DD} + 0.3	 V V V V	

Continued >>

DC Operating Conditions, continued (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{OL}	Output Low Voltage @ I_{OL} = 3 mA	-		0.4	V	
V_{OH}	Output High Voltage (SO, PFO) @ I_{OH} = -2 mA	V_{DD} – 0.8		-	V	
R_{RST}	Pull-up resistance for /RST inactive	50		400	KΩ	
V_{PFI}	Power Fail Input Reference Voltage	1.475	1.50	1.525	V	
V_{HYS}	Power Fail Input (PFI) Hysteresis (Rising)		-	100	mV	

Notes

1. Full complete operation. Supervisory circuits, RTC, etc operate to lower voltages as specified.
2. SCK toggling between V_{DD}-0.3V and V_{SS}, other inputs V_{SS} or V_{DD}-0.3V.
3. All inputs at V_{SS} or $V_{DD,}$ static. Trickle charger off (VBC=0).
4. The VBAK trickle charger automatically regulates the maximum voltage on this pin for capacitor backup applications.
5. V_{BAK} = 3.0V, $V_{DD} < V_{SW}$, oscillator running, CNT at VBAK.
6. V_{BAK} will source current when trickle charge is enabled (VBC bit=1), $V_{DD} > V_{BAK}$, and $V_{BAK} < V_{BAK}$ max.
7. This is the V_{DD} supply current contributed by enabling the trickle charger circuit, and does not account for I_{BAKTC}.
8. This is the V_{DD} supply current contributed by enabling the watchdog circuit, WDE=1 and WDET set to a non-zero value.
9. /RST is asserted active when $V_{DD} < V_{TP}$.
10. The minimum V_{DD} to guarantee the level of /RST remains a valid V_{OL} level.
11. V_{IN} or $V_{OUT} = V_{SS}$ to V_{DD}. Does not apply to PFI, X1, or X2.
12. Includes /RST input detection of external reset condition to trigger driving of /RST signal by FM33xx.

AC Parameters (T_A = -40°C to + 85°C, V_{DD} = 2.7V to 3.6V C_L = 30 pF)

Symbol	Parameter	Min	Max	Units	Notes
f_{CK}	SCK Clock Frequency	0	16	MHz	
t_{CH}	Clock High Time	28		ns	1
t_{CL}	Clock Low Time	28		ns	1
t_{CSU}	Chip Select Setup	10		ns	
t_{CSH}	Chip Select Hold	10		ns	
t_{OD}	Output Disable Time		20	ns	2
t_{ODV}	Output Data Valid Time		24	ns	
t_{OH}	Output Hold Time	0		ns	
t_D	Deselect Time	90		ns	
t_R	Data In Rise Time		50	ns	1,3
t_F	Data In Fall Time		50	ns	1,3
t_{SU}	Data Setup Time	6		ns	
t_H	Data Hold Time	6		ns	

Notes

1. $t_{CH} + t_{CL} = 1/f_{CK}$.
2. This parameter is characterized but not 100% tested.
3. Rise and fall times measured between 10% and 90% of waveform.

Supervisor Timing (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V)

Symbol	Parameter	Min	Max	Units	Notes
t_{RPW}	/RST Pulse Width (active low time)	30	100	ms	
t_{RNR}	/RST Response Time to $V_{DD}<V_{TP}$ (noise filter)	7	25	µs	1
t_{VR}	V_{DD} Rise Time	50	-	µs/V	1,2
t_{VF}	V_{DD} Fall Time	100	-	µs/V	1,2
t_{WDST}	Watchdog StartTime	$0.3*t_{DOG1}$	t_{DOG1}	ms	3
t_{WDET}	Watchdog EndTime	t_{DOG2}	$3.3*t_{DOG2}$	ms	3
f_{CNT}	Frequency of Event Counter	0	1	kHz	

Notes

1 This parameter is characterized but not tested.
2 Slope measured at any point on V_{DD} waveform.

3 t_{DOG1} is the programmed StartTime and t_{DOG2} is the programmed EndTime in registers 0Bh and 0Ch, $V_{DD} > V_{TP}$, and t_{RPU} satisfied. The StartTime has a resolution of 25ms. The EndTime has a resolution of 60ms.
4 The /RST pin will drive low for this amount of time after the internal reset circuit is activated due to a watchdog, low voltage, or manual reset event.

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 3.0V)

Symbol	Parameter	Typ	Max	Units	Notes
C_{IO}	Input/Output Capacitance	-	8	pF	1
C_{XTL}	X1, X2 Crystal pin Capacitance	25	-	pF	1, 2
C_{CNT}	Max. Allowable Capacitance on CNT (polled mode)	-	100	pF	

Notes
1 This parameter is characterized but not tested.
2 The crystal attached to the X1/X2 pins must be rated as 12.5pF.

Data Retention (V_{DD} = 2.7V to 3.6V)

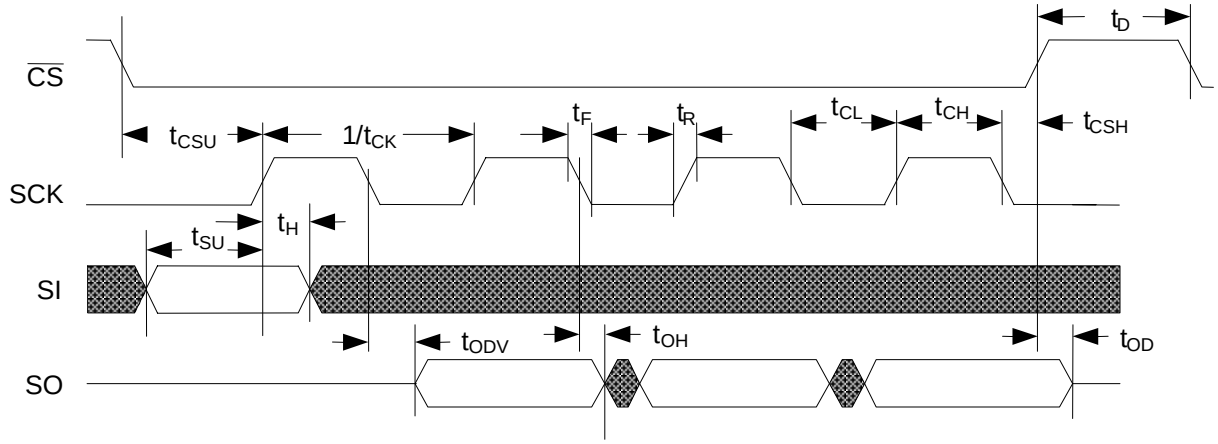
Parameter	Min	Units	Notes
Data Retention	10	Years	

AC Test Conditions

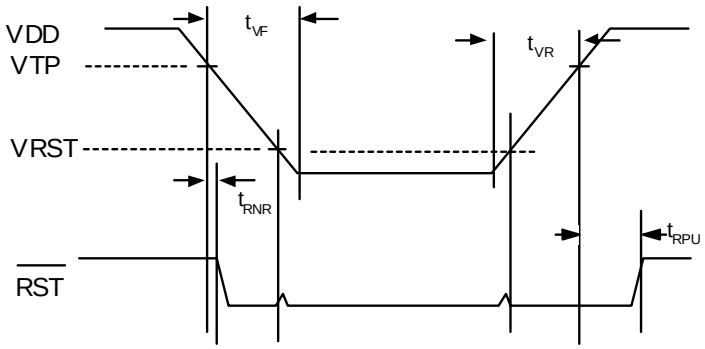
Input Pulse Levels	10% and 90% of V_{DD}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	0.5 V_{DD}
Output (SO) Load Capacitance	30 pF

Diagram Notes
All timing parameters apply to both read and write cycles. Clock specifications are identical for read and write cycles. Write timing parameters apply to op-code, word address, and write data bits. Functional relationships are illustrated in the relevant data sheet sections. These diagrams illustrate the timing parameters only.

Serial Data Bus Timing

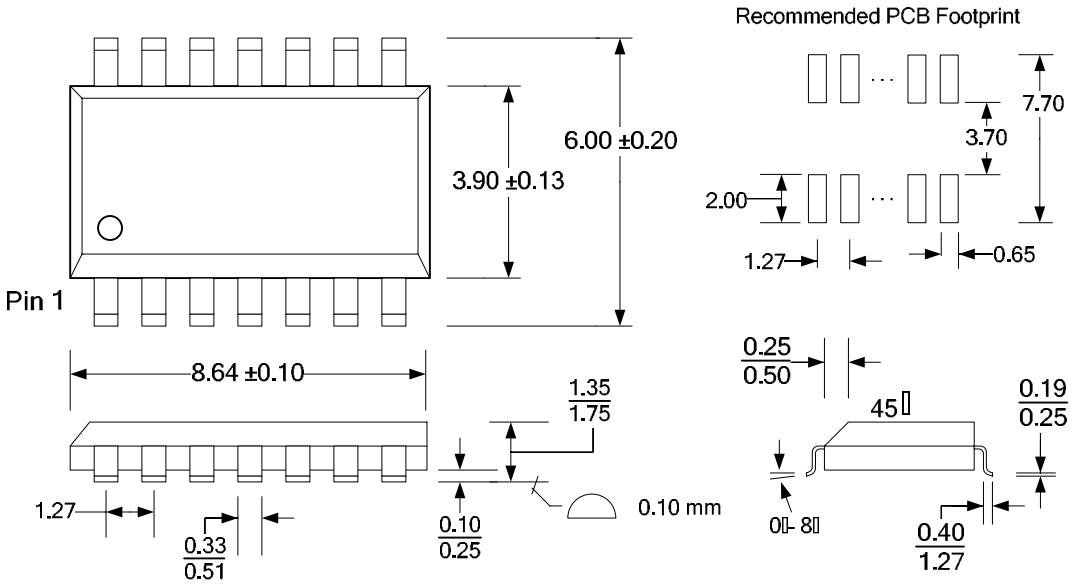


/RST Timing



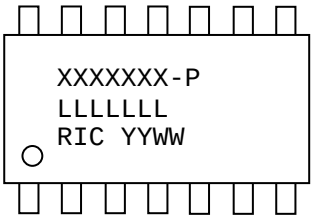
Mechanical Drawing

14-pin SOIC (JEDEC Standard MS-012 variation AB)



All dimensions in millimeters.
Conversions to inches are not exact.

SOIC Package Marking Scheme



Legend:
XXXX= part number, P= package type (-G)
LLLLLLL= lot code
RIC=Ramtron Int'l Corp, YY=year, WW=work week

Example: FM33256, "Green" SOIC package, Year 2006, Work Week 14
FM33256-G1
A70012G
RIC 0714

Revision History

Revision	Date	Summary
1.0	12/18/2006	Initial release.