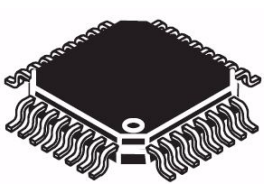
MC33696

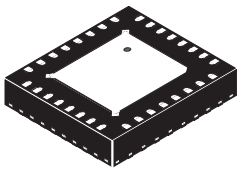
PLL Tuned UHF Transceiver for Data Transfer Applications

1 Overview

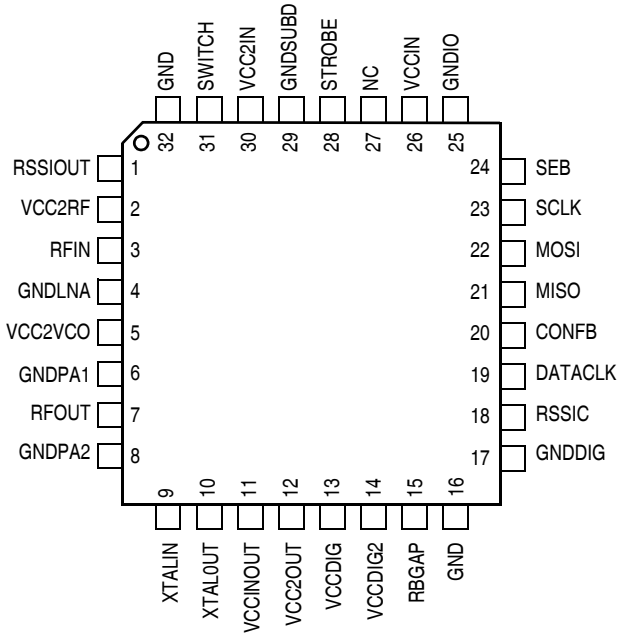
The MC33696 is a highly integrated transceiver designed for low-voltage applications. It includes a programmable PLL for multi-channel applications, an RSSI circuit, a strobe oscillator that periodically wakes up the receiver while a data manager checks the content of incoming messages. A configuration switching feature allows automatic changing of the configuration between two programmable settings without the need of an MCU.



LQFP32



QFN32



2 Features

General:

- 304 MHz, 315 MHz, 426 MHz, 434 MHz, 868 MHz, and 915 MHz ISM bands
- Choice of temperature ranges:
  - — –40°C to +85°C
  - — –20°C to +85°C
- OOK and FSK transmission and reception
- 20 kbps maximum data rate using Manchester coding
- 2.1 V to 3.6 V or 5 V supply voltage
- Programmable via SPI
- 6 kHz PLL frequency step

freescale™ semiconductor

- Current consumption:
  - 13.5 mA in TX mode
  - 10.3 mA in RX mode
  - Less then 1 mA in RX mode with strobe ratio = 1/10
  - 260 nA standby and 24 μA off currents
- Configuration switching — allows fast switching of two register banks

Receiver:

- –106.5 dBm sensitivity, up to –108 dBm in FSK 2.4 kbps
- Digital and analog RSSI (received signal strength indicator)
- Automatic wakeup function (strobe oscillator)
- Embedded data processor with programmable word recognition
- Image cancelling mixer
- 380 kHz IF filter bandwidth
- Fast wakeup time

Transmitter:

- Up to 7.25 dBm output power
- Programmable output power
- FSK done by PLL programming

Ordering information

Temperature Range	QFN Package	LQFP Package
–40°C to +85°C	MC33696FCE/R2	MC33696FJE/R2
–20°C to +85°C	MC33696FCAE/R2	MC33696FJAE/R2

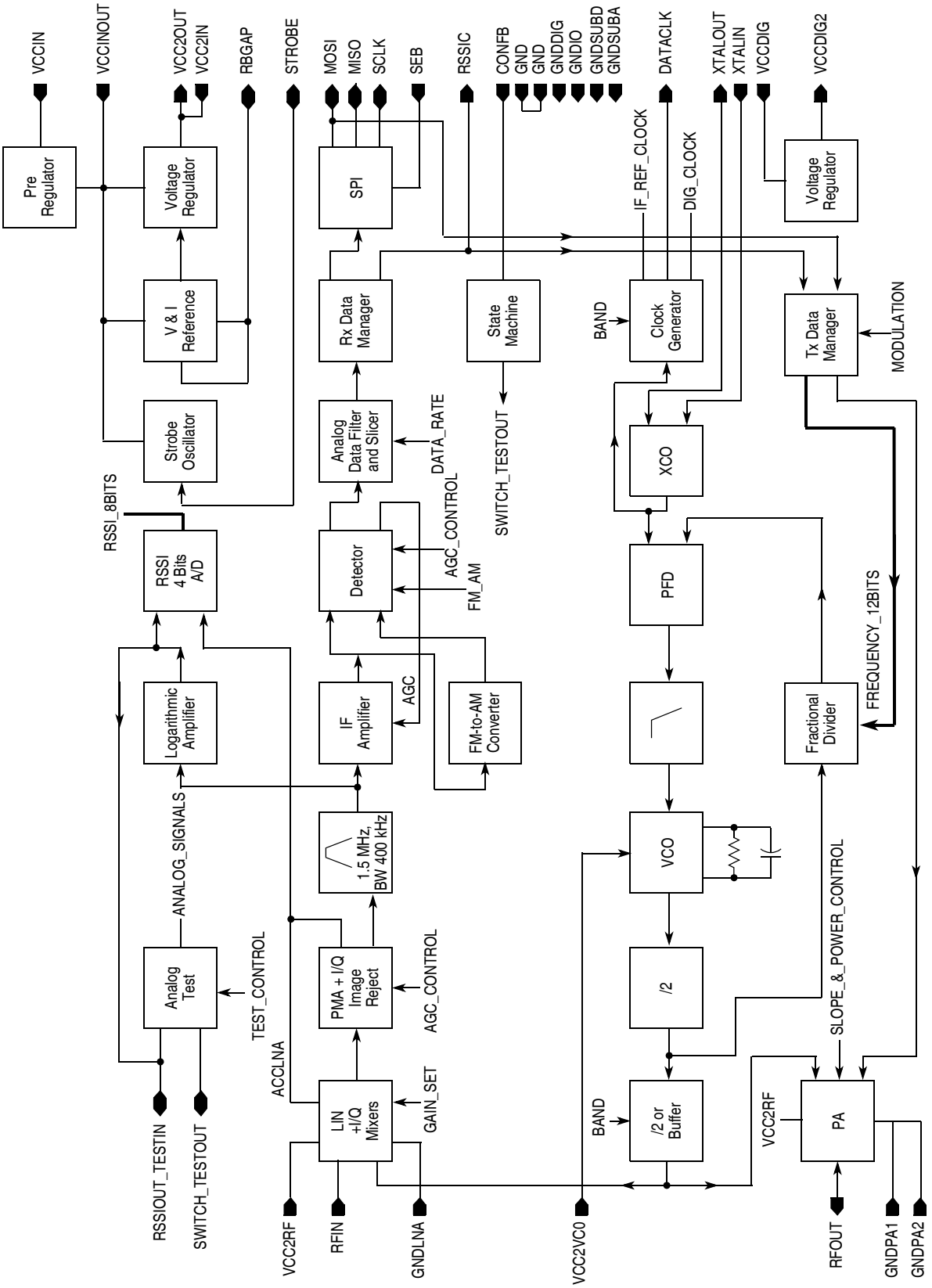


Figure 1. Block Diagram

3 Pin Functions

Table 1. Pin Functions

Pin	Name	Description
1	RSSIOUT	RSSI analog output
2	VCC2RF	2.1 V to 2.7 V internal supply for LNA
3	RFIN	RF input
4	GNDLNA	Ground for LNA (low noise amplifier)
5	VCC2VCO	2.1 V to 2.7 V internal supply for VCO
6	GNDPA1	PA ground
7	RFOUT	RF output
8	GNDPA2	PA ground
9	XTALIN	Crystal oscillator input
10	XTALOUT	Crystal oscillator output
11	VCCINOUT	2.1 V to 3.6 V power supply/regulator output
12	VCC2OUT	2.1 V to 2.7 V voltage regulator output for analog and RF modules
13	VCCDIG	2.1 V to 3.6 V power supply for voltage limiter
14	VCCDIG2	1.5 V voltage limiter output for digital module
15	RBGAP	Reference voltage load resistance
16	GND	General ground
17	GNDDIG	Digital module ground
18	RSSIC	RSSI control input
19	DATACLK	Data clock output to microcontroller
20	CONFB	Configuration mode selection input
21	MISO	Digital interface I/O
22	MOSI	Digital interface I/O
23	SCLK	Digital interface clock I/O
24	SEB	Digital interface enable input
25	GNDIO	Digital I/O ground
26	VCCIN	2.1 V to 3.6 V or 5.5 V input
27	NC	No connection
28	STROBE	Strobe oscillator capacitor or external control input
29	GNDSUBD	Ground
30	VCC2IN	2.1 V to 2.7 V power supply for analog modules for decoupling capacitor
31	SWITCH	RF switch control output
32	GND	General ground

4 Silicon Version

This data sheet describes the functional features of silicon version ES4.1.

5 Maximum Ratings

Table 2. Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage on pin: VCCIN	V_{CCIN}	V_{GND}–0.3 to 5.5	V
Supply voltage on pins: VCCINOUT, VCCDIG	V_{CC}	V_{GND}–0.3 to 3.6	V
Supply voltage on pins: VCC2IN, VCC2RF, VCC2VCO	V_{CC2}	V_{GND}–0.3 to 2.7	V
Voltage allowed on each pin (except RFOUT and digital pins)	—	V_{GND}–0.3 to V_{CC2}	V
Voltage allowed on pin: RFOUT	V_{CCPA}	V_{GND}–0.3 to $V_{CCINOUT}$+2	V
Voltage allowed on digital pins: SEB, SCLK, MISO, MOSI, CONFB, DATACLK, RSSIC, STROBE	V_{CCIO}	V_{GND}–0.3 to V_{CCIN}+0.3	V
ESD HBM voltage capability on each pin[1]	—	±2000	V
ESD MM voltage capability on each pin[2]	—	±200	V
Solder heat resistance test (10 s)	—	260	°C
Storage temperature	T_S	–65 to +150	°C
Junction temperature	T_J	150	°C

NOTES:
1 Human body model, AEC-Q100-002 rev. C.
2 Machine model, AEC-Q100-003 rev. C.

6 Power Supply

Table 3. Supply Voltage Range Versus Ambient Temperature

Parameter	Symbol	Temperature Range		Unit
		Full range[1]	–20°C to +60°C	°C
Supply voltage on VCCIN for 3 V operation	V_{CC3V}	3.0 to 3.6	2.1 to 3.6	V
Supply voltage on VCCIN for 5 V operation	V_{CC5V}	4.5 to 5.5	4.5 to 5.5	V
Supply voltage on VCCPA for 3 V or 5 V operation	V_{CCPA}	3.0 to 3.6	2.1 to 3.6	V
Supply voltage on VCCINOUT, VCCDIG	V_{CC}	3.0 to 3.6	2.1 to 3.6	V

NOTES:
1 –40°C to +85°C for MC33696FCE/FJE.
–20°C to +85°C for MC33696FCAE/FJAE.

The circuit can be supplied from a 3 V voltage regulator or battery cell by connecting VCCIN and VCCINOUT. It is also possible to use a 5 V power supply connected to VCCIN; in this case VCCINOUT should not be connected to VCCIN.

The RFOUT pin cannot be biased with a voltage higher than 3.6 V. For 5 V operation, biasing voltage is available on VCCINOUT.

An on-chip low drop-out voltage regulator supplies the RF and analog modules (except the strobe oscillator and the low voltage detector, which are directly supplied from VCCINOUT). This voltage regulator is supplied from pin VCCINOUT and its output is connected to VCC2OUT. An external capacitor must be inserted between VCC2OUT and GND for stabilization and decoupling. The analog and RF modules must be supplied by VCC2 by externally wiring VCC2OUT to VCC2IN, VCC2RF and VCC2VCO.

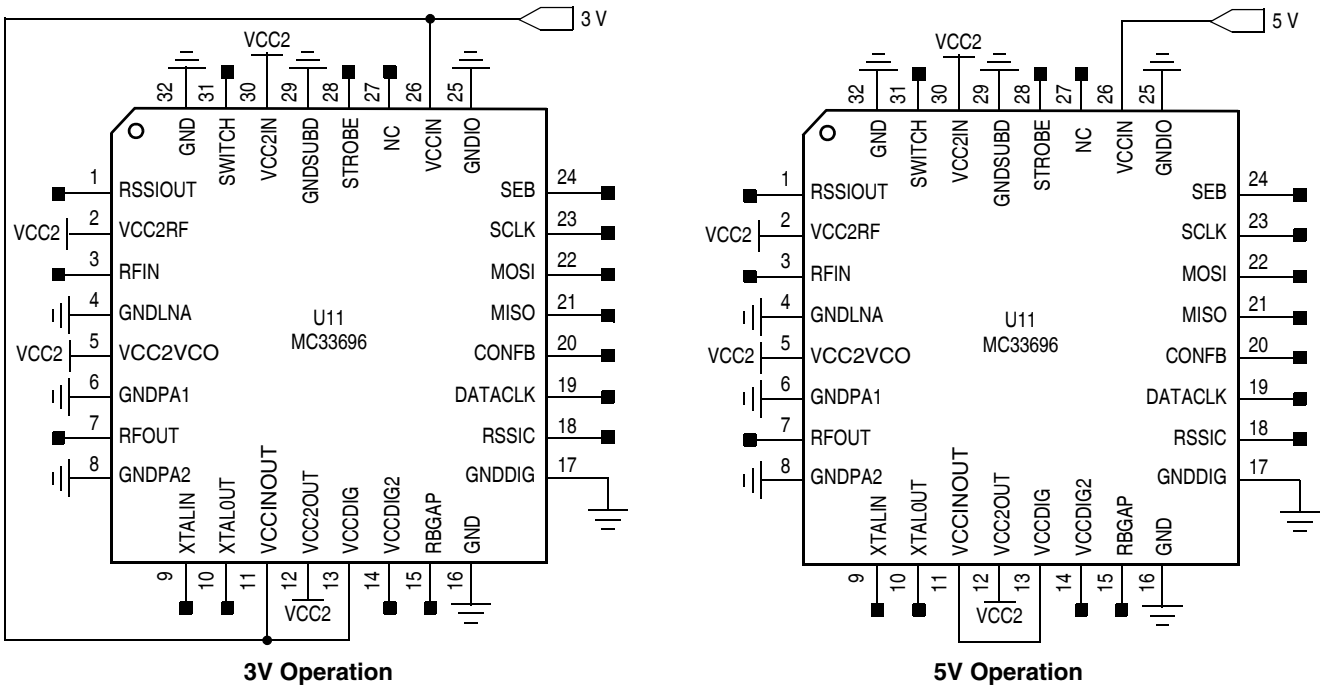


Figure 2. Wiring Diagrams

A second voltage regulator supplies the digital part. This regulator is powered from pin VCCDIG and its output is connected to VCCDIG2. An external capacitor must be inserted between VCCDIG2 and GNDDIG, for decoupling. The supply voltage VCCDIG2 is equal to 1.6 V. In standby mode, this voltage regulator goes into an ultra-low-power mode, but VCCDIG2 = 0.7 x V_{CCDIG}. This enables the internal registers to be supplied, allowing configuration data to be saved.

7 Supply Voltage Monitoring and Reset

At power-on, an internal reset signal is generated. All registers are reset.

When the LVDE bit is set, the low-voltage detection module is enabled. This block compares the supply voltage on VCCINOUT with a reference level of about 1.8 V. If the voltage on VCCINOUT drops below 1.8 V, status bit LVDS is set. The information in status bit LVDS is latched and reset after a read access.

NOTE

If LVDE = 1, the LVD module remains enabled. The circuit cannot be put in standby mode, but remains in LVD mode with a higher quiescent current, due to the monitoring circuitry. LVD function is not accurate in standby mode.

8 Receiver Functional Description

The receiver is based on a superheterodyne architecture with an intermediate frequency (IF) of 1.5 MHz (see Figure 1). Its input is connected to the RFIN pin. Frequency down conversion is done by a high-side

injection I/Q mixer driven by the frequency synthesizer. An integrated poly-phase filter performs rejection of the image frequency.

The low intermediate frequency allows integration of the IF filter providing the selectivity. The center frequency is tuned by automatic frequency control (AFC) referenced to the crystal oscillator frequency.

Sensitivity is met by an overall amplification of approximately 96 dB, distributed over the reception chain, comprising low-noise amplifier (LNA), mixer, post-mixer amplifier, and IF amplifier. Automatic gain control (AGC), on the LNA and the IF amplifier, maintains linearity and prevents internal saturation. Sensitivity can be reduced using four programmable steps on the LNA gain.

Amplitude demodulation is achieved by peak detection and comparison with a fixed or adaptive voltage reference selected during configuration. Frequency demodulation is achieved in two steps: the IF amplifier AGC is disabled and acts as an amplitude limiter; a filter performs a frequency-to-voltage conversion. The resulting signal is then amplitude demodulated in the same way as in the case of amplitude modulation with an adaptive voltage reference.

A low-pass filter improves the signal-to-noise ratio.

Shaped data are available if the integrated data manager is not used.

If used, the data manager performs clock recovery and decoding of Manchester coded data. Data and clock are then available on the serial peripheral interface (SPI). The configuration sets the data rate range managed by the data manager and the bandwidth of the low-pass filter.

An internal low-frequency oscillator can be used as a strobe oscillator to perform an automatic wakeup sequence.

It is also possible to define two different configurations for the receiver (frequency, data rate, data manager, modulation, etc.) that are automatically loaded during wakeup or under MCU control.

If the PLL goes out of lock, received data are ignored.

9 Transmitter Functional Description

The single-ended power amplifier is connected to the RFOUT pin.

In the case of amplitude modulation, coded data sent by the microcontroller unit (MCU) are used for on/off keying (OOK) the RF carrier. Rise and fall times of the RF signal are controlled to minimize spurious emission.

In the case of frequency modulation, coded data sent by the MCU are used for frequency shift keying (FSK) the RF carrier. RF output power can be reduced using four programmable steps.

Out-of-lock detection prevents any out-of-band emission, by stopping the transmission.

The logic output SWITCH enables control of an external RF switch for isolating the two RF pins. Its output toggles when the circuit changes from receive to transmit, and vice versa.

10 Frequency Planning

10.1 Clock Generator

All clocks running in the circuit are derived from the reference frequency provided by the crystal oscillator (frequency f_{ref}, period t_{ref}). The crystal frequency is chosen in relation to the band in which the MC33696 has to operate. Table 4 shows the value of the CF bits.

Table 4. Crystal Frequency and CF Values Versus Frequency Band

RF Frequency (MHz)	CF1	CF0	LOF1	LOF0	F_{REF} (Crystal Frequency) (MHz)	F_{IF} (IF Frequency) (MHz)	Dataclk Divider	$F_{dataclk}$ (kHz)	Digclk Divider	F_{digclk} (kHz)	T_{digclk} (µs)
304	0	0	0	0	16.96745	1.414	60	282.791	30	565.582	1.77
315	0	0	1	0	17.58140	1.465	60	293.023	30	586.047	1.71
426	0	1	0	1	23.74913	1.484	80	296.864	40	593.728	1.68
433.92	0	1	0	1	24.19066	1.512	80	302.383	40	604.767	1.65
868.3	1	1	0	1	24.16139	1.510	80	302.017	40	604.035	1.66
916.5	1	1	1	1	25.50261	1.594	80	318.783	40	637.565	1.57

10.2 Intermediate Frequency

The IF filter is controlled by the crystal oscillator to guarantee the frequency over temperature and voltage range. The IF filter center frequency, FIF, can be computed using the crystal frequency f_{ref} and the value of the CF bits:

- If CF[0] = 0 : FIF = f_{ref}/9*1.5/2
- If CF[0] = 1 : FIF = f_{ref}/12*1.5/2

The cut-off frequency given in the parametric section can be computed by scaling to the FIF.

Example 1. Cut-off Frequency Computation

Compute the low cut-off frequency of the IF filter for a 16.9683 MHz crystal oscillator. For this reference frequency, FIF = 1.414 MHz.

So, the 1.375[1] MHz low cut-off frequency specified for a 1.5 MHz IF frequency becomes 1.375[1]*1.414/1.5 = 1.296 MHz

10.3 Frequency Synthesizer Description

The frequency synthesizer consists of a local oscillator (LO) driven by a fractional N phase locked loop (PLL).

The LO is an integrated LC voltage controlled oscillator (VCO) operating at twice the RF frequency (for the 868 MHz frequency band) or four times the RF frequency (for the 434 MHz and 315 MHz frequency bands). This allows the I/Q signals driving the mixer to be generated by division.

1. Refer to parameter 3.3 found in Section 19.1, “General Parameters.”

The fractional divider offers high flexibility in the frequency generation for:

- Switching between transmit and receive modes.
- Achieving frequency modulation in FSK modulation transmission.
- Performing multi-channel links.
- Trimming the RF carrier.

Frequencies are controlled by means of registers. To allow for user preference, two programming access methods are offered (see Section 17.3, “Frequency Registers”).

- In friendly access, all frequencies are computed internally from the contents of the carrier frequency and deviation frequency registers.
- In direct access, the user programs direct all three frequency registers.

11 Register Access through SPI

11.1 SPI Interface

the MC33696 and the MCU communicate via a bidirectional serial digital interface. According to the selected mode, the MC33696 or the MCU manages the data transfer. The MC33696’s digital interface can be used as a standard SPI (master/slave) or as a simple interface (SPI deselected). In the latter case, the interface’s pins are used as standard I/O pins. However, the MCU has the highest priority, as it can control the MC33696 by setting CONFB pin to the low level.

The interface is operated by four I/O pins.

- SEB — Serial interface Enable

  When SEB is set high, pins SCLK, MOSI, and MISO are set to high impedance. This allows individual selection in a multiple device system, where all devices are connected via the same bus. The rest of the circuit remains in the current state, enabling fast recovery times, but the power amplifier is disabled to prevent any uncontrolled RF transmission.
- SCLK — Serial Clock

  Synchronizes data movement in and out of the device through its MOSI and MISO lines. The master and slave devices can exchange a byte of information during a sequence of eight clock cycles. Since SCLK is generated by the master device, this line is an input on a slave device.
- MOSI — Master Output Slave Input

  Transmits bytes when master, and receives bytes when slave, with the most significant bit first. When no data are output, SCLK and MOSI force a low level.
- MISO — (Master Input) Slave Output

  Transmits data when slave, with the MSB first. There is no master function. Data are valid on falling edges of SCLK. This means that the clock phase and polarity control bits of the microcontroller SPI have to be CPOL = 0 and CPHA = 1 (using Freescale acronyms).

Table 5 summarizes the serial digital interface feature versus the selected mode.

Table 5. Serial Digital Interface Feature versus Selected Mode (SEB = 1)

Selected Mode		MC33696 Digital Interface Use
Configuration		SPI slave, data received on MOSI, SCLK from MCU, MISO is output
Transmit		SPI deselected, MOSI receives encoded data from MCU
Receive	DME = 1	SPI master, data sent on MOSI with clock on SCLK
	DME = 0	SPI deselected, received data are directly sent to MOSI
Standby / LVD		SPI deselected, all I/O are high impedance

The data transfer protocol for each mode is described in the following sections.

11.2 Configuration Mode

This mode is used to write or read the internal registers of the MC33696.

As long as a low level is applied to CONFB (see Figure 29), the MCU is the master node driving the SCLK input, the MOSI line input, and the MISO line output. Whatever the direction, SPI transfers are 8-bit based and always begin with a command byte, which is supplied by the MCU on MOSI. To be considered as a command byte, this byte must come after a falling edge on CONFB. Figure 3 shows the content of the command byte.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	N1	N0	A4	A3	A2	A1	A0	R/W

Figure 3. Command Byte

Bits N[1:0] specify the number of accessed registers, as defined in Table 6.

Table 6. Number N of Accessed Registers

N[1:0]	Number N of Accessed Registers
00	1
01	2
10	4
11	8

Bits A[4:0] specify the address of the first register to access. This address is then incremented internally by N after each data byte transfer.

R/W specifies the type of operation:

0 = Read

1 = Write

Thus, this bit is associated with the presence of information on MOSI (when writing) or MISO (when reading).

Figure 4 and Figure 5 show write and read operations in a typical SPI transfer. In both cases, the SPI is a slave. A received byte is considered internally on the eighth falling edge of SCLK. Consequently, the last received bits, which do not form a complete byte, are lost.

NOTE

A low level applied to CONFB does not affect the configuration register contents.

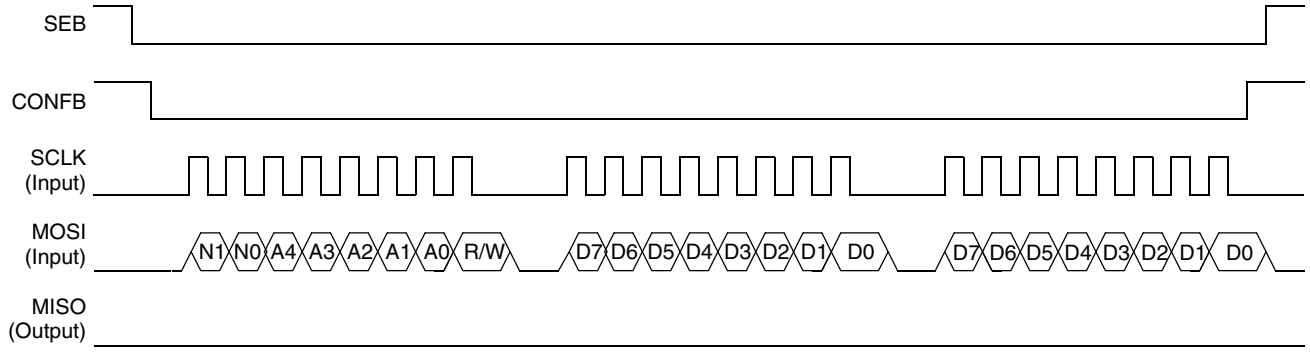


Figure 4. Write Operation in Configuration Mode (N[1:0] = 01)

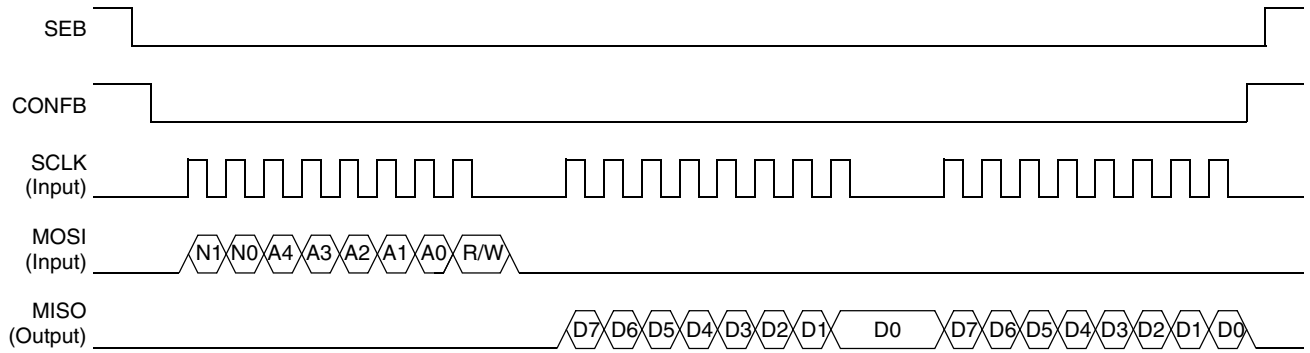


Figure 5. Read Operation in Configuration Mode (N[1:0] = 01)

11.3 Configuration Switching

This feature allows for defining two different configurations using two different banks, and for switching them automatically during wakeup when using a strobe oscillator, or by means of the strobe pin actuation by the MCU. This automatic feature may be used only in receiver mode; however, if one of the register banks is related to a transmitter configuration, it may be accessed directly by programing some bits to define the active bank, thus allowing fast switching between receiver mode and transmitter mode, or between any different possible configurations.

11.3.1 Bit Definition

Two sets of configuration registers are available. They are grouped in two different banks: Bank A and Bank B. Two bits are used to define which bank represents the state of the component.

Bit Name	Direction	Location
BANKA	R/W	Bank A
BANKB	R/W	Bank B

BANKA	BANKB	Actions
X	0	Bank A is active (TX or RX)
0	1	Bank B is active (TX or RX)
1	1	Bank A and Bank B are active and will be used one after the other (RX only)

At any time, it is possible to know what is the active bank by reading the status bit BANKS.

Bit Name	Direction	Location	Comment
BANKS	R	A & B	Bank status: indicates which register bank is active. This bit, available in Bank A and Bank B, returns the same value.

11.3.2 Bank Access and Register Mapping

Registers are physically mapped following a byte organization. The possible address space is 32 bytes. The base address is specified in the command byte. This is then incremented internally to address each register, up to the number of registers specified by N[1:0], also specified by this command byte. All registers can then be scanned, whatever the type of transmission (read or write); however, writing to read-only bits or registers has no effect. When the last implemented address is reached, the internal address counter automatically loops back to the first mapped address ($00).

At any time, it is possible to write or read the content of any register of Bank A and Bank B. Register access is defined as follows:

R/W	Bit can be read and written.
R	Bit can be read. Write has no effect on bit value.
RR	Bit can be read. Read or write resets the value.
R [A]	Bit can be read, this returns the same value as Bank A.
RR [A]	Bit can be read, this returns the same value as Bank A. Read or write resets the value.

Table 7. Access to Specific Bits

Bit	Bank	Byte	Access	Comment
RESET	A	CONFIG1	R/W	Available in BANKA.
OLS	A, B	CONFIG3	R-R[A]	Bit value is the real time status of the PLL, BANKA, and BANKB access reflect the same value.
LDVS	A, B	CONFIG3	RR-RR[A}	Bit value is the latched value of the low-voltage detector. Read or write from any bank resets value.
SOE	A, B	CONFIG2	R/W-R[A}	SOE can be modified in BANKA. Access from BANKB reflects BANKA value.
RSSIx	A, B	RSSI	R-R[A}	RSSI value is directly read from RSSI converter. Reflected value is the same whatever the active byte.

00h CONFIG1-A 91 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	LOF1	LOF0	CF1	CF0	RESET	SL	LVDE	CLKE
Reset Value	1	0	0	1	0	0	0	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0 =	304–434	304–315	315–434	314	No	T/R	No	No
1 =	315–916	434–916	868	434–868	Yes	R/T	Yes	Yes

01h CONFIG2-A 10 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	DSREF	FRM	MODU	DR1	DR0	TRXE	DME	SOE
Reset Value	0	0	0	1	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0 =	Fixed	Friendly	OOK	2.4–4.8	2.4–9.6	Standby	No	No
1 =	Adaptive	Direct	FSK	9.6–19.2	4.8–19.2	Enable	Yes	Yes

02h CONFIG3-A 30 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	AFF1	AFF0	OLS	LVDS	ILA1	ILA0	OLA1	OLA0
Reset Value	0	0	1	1	0	0	0	0
	R/W	R/W	R	RR	R/W	R/W	R/W	R/W
0 =	0.5–1 kHz	0.5–2 kHz	RAS	RAS	0–8 dB	0–14 dB	0–8 dB	0–14 dB
1 =	2–4 kHz	1–4 kHz	Unlocked	Low V	14–24 dB	8–24 dB	14–24 dB	8–24 dB

03h COMMAND-A 9 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	AFFC	IFLA	MODE	RSSIE	EDD	RAGC	FAGC	BANKS
Reset Value	0	0	0	0	1	0	0	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0 =	AFFx OFF	No	RX	No	Slow dec.	No	No	B Bank
1 =	AFFx ON	–20 dB	TX	Yes	Fast dec.	Yes	Yes	A Bank

04h F1-A 48 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	FSK3	FSK2	FSK1	FSK0	F11	F10	F9	F8
Reset Value	0	1	0	0	1	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

05h F2-A 0 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	F7	F6	F5	F4	F3	F1	F1	F0
Reset Value	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bank A Registers

0Dh CONFIG1-B 91 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	LOF1	LOF0	CF1	CF0	—	SL	LVDE	CLKE
Reset Value	1	0	0	1	0	0	0	1
	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
0 =	304–434	304–315	315–434	314	—	T/R	No	No
1 =	315–916	434–916	868	434–868	—	R/T	Yes	Yes

0Eh CONFIG2-B 10 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	DSREF	FRM	MODU	DR1	DR0	TRXE	DME	SOE
Reset Value	0	0	0	1	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R[A]
0 =	Fixed	Friendly	OOK	2.4–4.8	2.4–9.6	Standby	No	No
1 =	Adaptive	Direct	FSK	9.6–19.2	4.8–19.2	Enable	Yes	Yes

0Fh CONFIG3-B 30 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	AFF1	AFF0	OLS	LVDS	ILA1	ILA0	OLA1	OLA0
Reset Value	0	0	1	1	0	0	0	0
	R/W	R/W	R[A]	RR[A]	R/W	R/W	R/W	R/W
0 =	0.5–1 kHz	0.5–2 kHz	RAS	RAS	0–8 dB	0–14 dB	0–8 dB	0–14 dB
1 =	2–4 kHz	1–4 kHz	Unlocked	Low V	14–24 dB	8–24 dB	14–24 dB	8–24 dB

10h COMMAND-B 9 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	AFFC	IFLA	MODE	RSSIE	EDD	RAGC	FAGC	BANKS
Reset Value	0	0	0	0	1	0	0	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R[A]
0 =	AFFx OFF	No	RX	No	Slow dec.	No	No	B Bank
1 =	AFFx ON	–20 dB	TX	Yes	Fast dec.	Yes	Yes	A Bank

11h F1-B 4800 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	FSK3	FSK2	FSK1	FSK0	F11	F10	F9	F8
Reset Value	0	1	0	0	1	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12h F2-B 0 h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	F7	F6	F5	F4	F3	F1	F1	F0
Reset Value	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bank B Registers

Figure 6. Bank Registers

06h FT1-A	700701 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	FTA11	FTA10	FTA9	FTA8	FTA7	FTA6	FTA5	FTA4
Reset Value	0	1	1	1	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
07h FT2-A	7 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	FTA3	FTA2	FTA1	FTA0	FTB11	FTB10	FTB9	FTB8
Reset Value	0	0	0	0	0	1	1	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
08h FT3-A	1 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	FTB7	FTB6	FTB5	FTB4	FTB3	FTB2	FTB1	FTB0
Reset Value	0	0	0	0	0	0	0	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
09h RXONOFF-A	75 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	BANKA	RON3	RON2	RON1	RON0	ROFF2	ROFF1	ROFF0
Reset Value	0	1	1	1	1	1	1	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0Ah ID-A	C0 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	IDL1	IDL0	ID5	ID4	ID3	ID2	ID1	ID0
Reset Value	1	1	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0Bh HEADER-A	80 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	HDL1	HDL0	HD5	HD4	HD3	HD2	HD1	HD0
Reset Value	1	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0Ch RSSI-A	80 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	RSSI7	RSSI6	RSSI5	RSSI4	RSSI3	RSSI2	RSSI1	RSSI0
Reset Value	0	0	0	0	0	0	0	0
	R	R	R	R	R	R	R	R

Bank A Registers

13h FT1-B	700701 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	FTA11	FTA10	FTA9	FTA8	FTA7	FTA6	FTA5	FTA4
Reset Value	0	1	1	1	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
14h FT2-B	7 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	FTA3	FTA2	FTA1	FTA0	FTB11	FTB10	FTB9	FTB8
Reset Value	0	0	0	0	0	1	1	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15h FT3-B	1 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	FTB7	FTB6	FTB5	FTB4	FTB3	FTB2	FTB1	FTB0
Reset Value	0	0	0	0	0	0	0	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
16h RXONOFF-B	75 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	BANKB	RON3	RON2	RON1	RON0	ROFF2	ROFF1	ROFF0
Reset Value	0	1	1	1	1	1	1	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
17h ID-B	C0 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	IDL1	IDL0	ID5	ID4	ID3	ID2	ID1	ID0
Reset Value	1	1	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
18h HEADER-B	80 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	HDL1	HDL0	HD5	HD4	HD3	HD2	HD1	HD0
Reset Value	1	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
19h RSSI-B	80 h							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	RSSI7	RSSI6	RSSI5	RSSI4	RSSI3	RSSI2	RSSI1	RSSI0
Reset Value	0	0	0	0	0	0	0	0
	R[A]	R[A]	R[A]	R[A]	R[A]	R[A]	R[A]	R[A]

Bank B Registers

Figure 6. Bank Registers (continued)

11.3.3 Direct Switch Control

The conditions to enter direct switch control are:

- Strobe pin = V_{CC}
- SOE bit = 0

By simply writing BANKA and BANKB, the active bank will be defined:

BANKA	BANKB	
X	0	Bank A is active (TX or RX)
0	1	Bank B is active (TX or RX)
1	1	Not allowed in direct switch control

Defined bank is active after exiting the configuration mode, i.e., CONFB line goes high.

The direct switch control should be used when:

- One or both banks are in transmitter configuration (MODE = 1)
- When the strobe oscillator cannot be used to define the switch timing (for example, not periodic)
- When strobe pin use is not possible (no sleep mode between the two configurations)
- No automatic switching is required and MCU SPI access is possible

11.3.4 Strobe Pin Switch Control

The conditions to enter strobe pin switch control are:

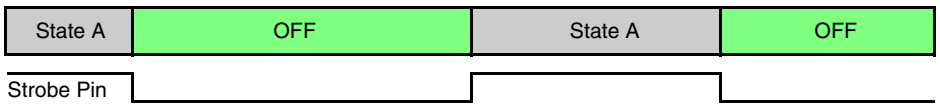
- Strobe pin: controlled by MCU I/O port
- SOE bit = 0

By simply writing BANKA and BANKB, the active banks will be defined.

BANKA	BANKB	
X	0	Bank A is active (TX or RX)
0	1	Bank B is active (TX or RX)
1	1	Bank A and Bank B are both active, configuration will toggle at each wakeup, not allowed with MODE = 1

The strobe pin will control the OFF/ON state of the MC33696. The various available sequences are described in the following subsections.

11.3.4.1 BANKA = X, BANKB = 0

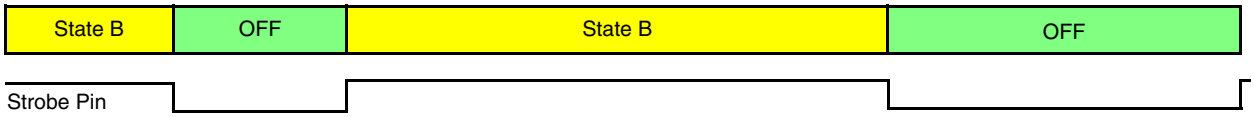


If strobe pin is 1, configuration is defined by Bank A, BANKS = 1

If strobe pin is 0, MC33696 configuration is OFF.

If a message is received during State A, current state remains State A up to end of message.

11.3.4.2 BANKA = 0, BANKB = 1

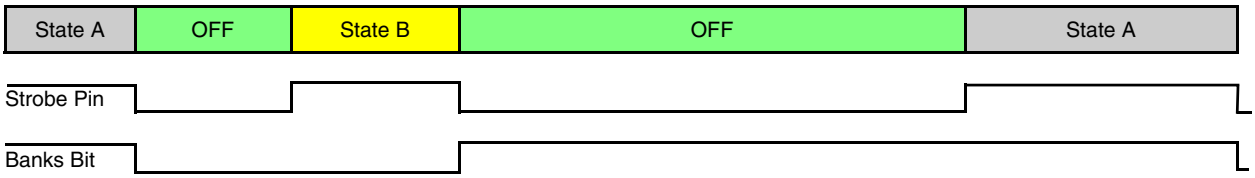


If strobe pin is 1, configuration is defined by Bank B, BANKS = 0.

If strobe pin is 0, MC33696 configuration is OFF.

If a message is received during State B, current state remains State B up to end of message.

11.3.4.3 BANKA = 1, BANK B = 1



If strobe pin is 1, configuration is defined by BANKS. BANKS is toggled at each falling edge of the strobe pin.

If strobe pin is 0, MC33696 configuration is OFF.

If a message is received during state A or state B, current state remains the same up to end of message.

If a read or write access is done using SPI, the next sequence will begin with state A whatever was the active state before SPI access by MCU.

11.3.5 Strobe Oscillator Switch Control

The conditions to enter strobe oscillator switch control are:

- Strobe pin connected to an external capacitor to define timing (see Section 14, “Receiver On/Off Control”)
- Strobe pin can also be connected to the MCU I/O port
- SOE bit = 1

By simply writing BANKA and BANKB, the active banks will be defined.

BANKA	BANKB	
X	0	Bank A is active (TX or RX)
0	1	Bank B is active (TX or RX)
1	1	Bank A and Bank B are both active, configuration will toggle at each wakeup, not allowed with MODE = 1

MCU can override strobe oscillator control by controlling strobe pin level. If MCU I/O port is in high impedance, strobe oscillator will control the OFF/ON state of the MC33696. The various available sequences are described in the following subsections.

11.3.5.1 BANKA = X, BANKB = 0

If strobe pin is 1, configuration is defined by Bank A, BANKS = 1.

If strobe pin is 0, MC33696 configuration is OFF.

If a message is received during State A, current state remains State A up to end of message.

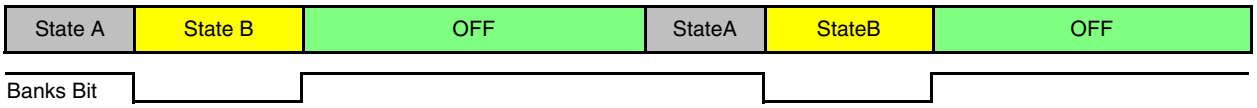
11.3.5.2 BANKA = 0, BANKB = 1

If strobe pin is 1, configuration is defined by Bank B, BANKS = 0.

If strobe pin is 0, MC33696 configuration is OFF.

If a message is received during State B, current state remains State B up to end of message.

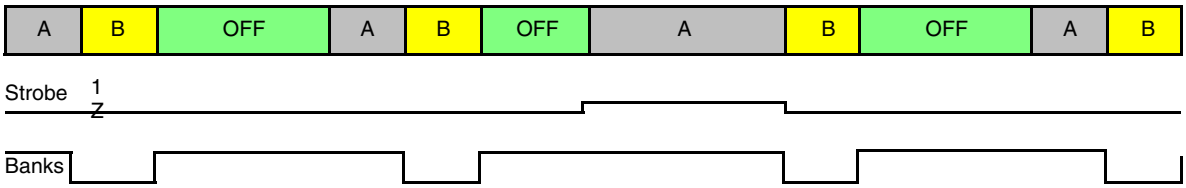
11.3.5.3 BANKA = 1, BANK B = 1



BANKS toggles at the end of each state A or state B.

If strobe is forced to 1, configuration is frozen according to BANKS value.

If a read or write access is done using SPI, the next sequence will begin with state A in whatever was the active state before SPI access by MCU.



For all available sequences:

- State A and State B are defined by Bank A and Bank B.
- State A duration, TonA is defined by Bank A RON[3–0].
- State B duration, TonB is defined by Bank B RON[3–0].
- OFF duration, TonB is defined by Bank A ROFF[2–0].
- If strobe pin is 1, the state is ON and defined by BANKS at that time and remains this state up to the release of strobe and end of message if a message is being received.
- If a message is being received during State A or B, current state remains State A or B up to end of message.

- If strobe pin is 0 the state is OFF.
- If strobe pin is released from 0 while state is OFF, the initial OFF period is completed.
- Whenever is the change of duration of one state due to STROBE pin level or a message being received, this has no influence on the timing of the following states (A, B, or OFF).

11.4 Standby: LVD Mode

The SPI is deselected. Nothing is sent and all incoming data are ignored until CONFB and SEB go low to switch back to configuration mode.

12 Communication Protocol

12.1 Manchester Coding Description

The MC33696 data manager is able to decode Manchester coded messages. For other codings, the data manager should be disabled (DME=0) for RAW data to be available on MOSI.

Manchester coding is defined as follows: data is sent during the first half-bit; and the complement of the data is sent during the second half-bit.

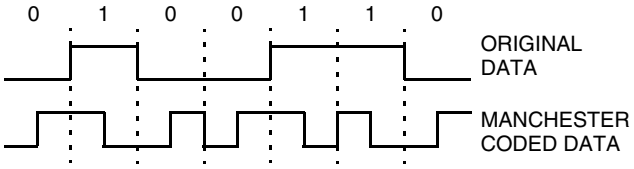


Figure 7. Example of Manchester Coding

The signal average value is constant. This allows clock recovery from the data stream itself. To achieve correct clock recovery, Manchester coded data must have a duty cycle between 47% and 53%.

12.2 Preamble, Identifier, Header, and Message

The following description applies if the data manager is enabled (DME = 1).

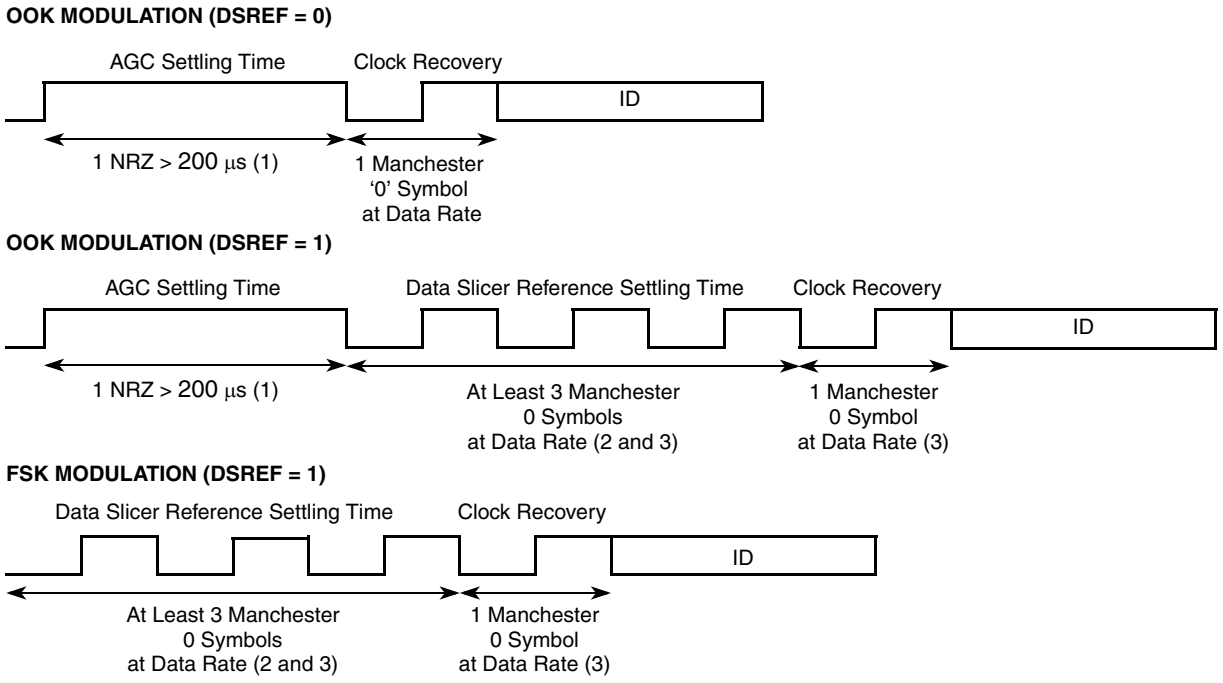
A complete telegram includes the following sequences: a preamble, an identifier (ID), the preamble again, a header, the message, and an end-of-message (EOM). These bit sequences are described below.

- Preamble: A preamble is required before the ID and before the header. It enables:
  - In the case of OOK modulation, the AGC to settle, and the data slicer reference voltage to settle if DSREF = 1
  - In the case of FSK modulation, the data slicer reference voltage to settle
  - Clock recovery

  The preamble content must be defined carefully, to ensure that it will not be decoded as the ID or the header. Figure 8 defines the preamble in OOK and FSK modulation.

- ID: The ID allows selection of the correct device in an RF transmission, as the content has been loaded previously in the ID register. Its length is variable, defined by the IDL[1:0] bits. The complement of the ID is also recognized as the identifier.
- Header: The header specifies the beginning of the message, as it is compared with the HEADER register. Its length is variable, defined by the HDL[1:0] bits. The complement of the header is also recognized as the header, in this case, output data are complemented.
- The ID and the header are sent at the same data rate as data.
- Message: Data must follow the header, with no delay.
- EOM: The message is completed with an end-of-message, consisting of two consecutive NRZ ones or zeroes (i.e., a Manchester code violation). Even in the case of FSK modulation, data must conclude with an EOM, and not simply by stopping the RF telegram.

Figure 9 shows a complete message comprising a 6-bit ID and a 4-bit header, followed by two data bits.



NOTES:
1. The AGC settling time pulse can be split over different pulses as long as the overall duration is at least 200 µs.
2. Table 15 defines the minimum number of Manchester symbols required for the data slicer operation versus the data and average filters cut-off frequencies.
3. The Manchester 0 symbol can be replaced by a 1.

Figure 8. Preamble Definition

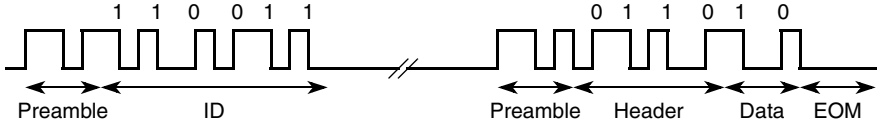


Figure 9. Complete Message Example

NOTE

It is possible to build a tone to form the detection sequence by programming the ID register with a full sequence of ones or zeroes. In this case, the header (or its complement) must not be found in this tone (i.e., it must not be a full sequence of ones or zeroes).

12.3 Message Protocol

When the strobe oscillator is enabled (SOE = 1), the receiver is continuously on/off cycling. The ID must be recognized for the receiver to stay on. Consequently, the transmitted ID burst must be long enough to include two consecutive receiver On cycles.

When the strobe oscillator is not enabled (SOE = 0), these timing constraints must be respected by the external control applied to pin STROBE.

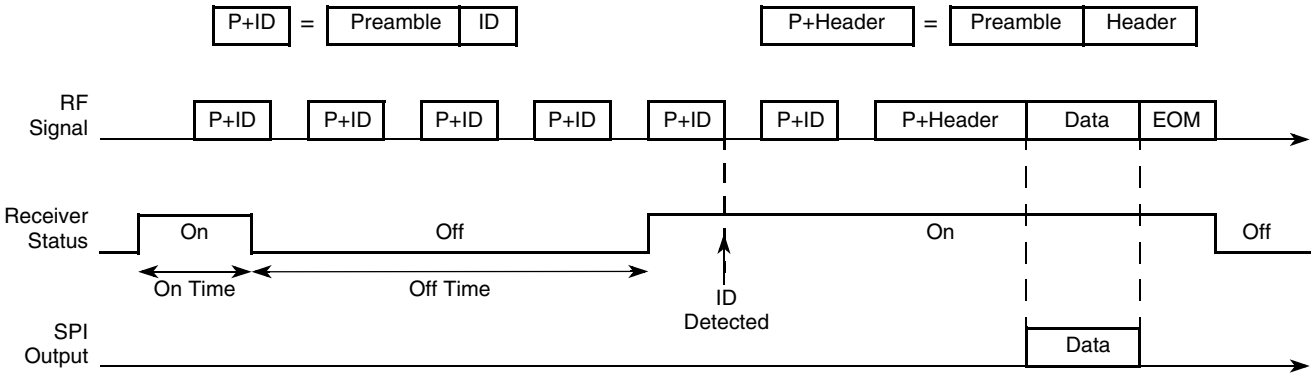


Figure 10. Complete Telegram with ID Detection

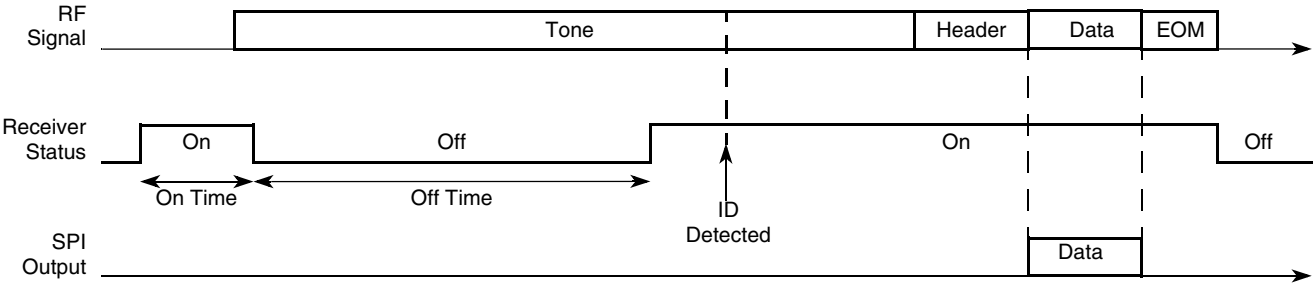


Figure 11. Complete Telegram with Tone Detection

12.4 Receiver Startup Delay

As shown in Figure 12, a settling time is required when entering the on state.

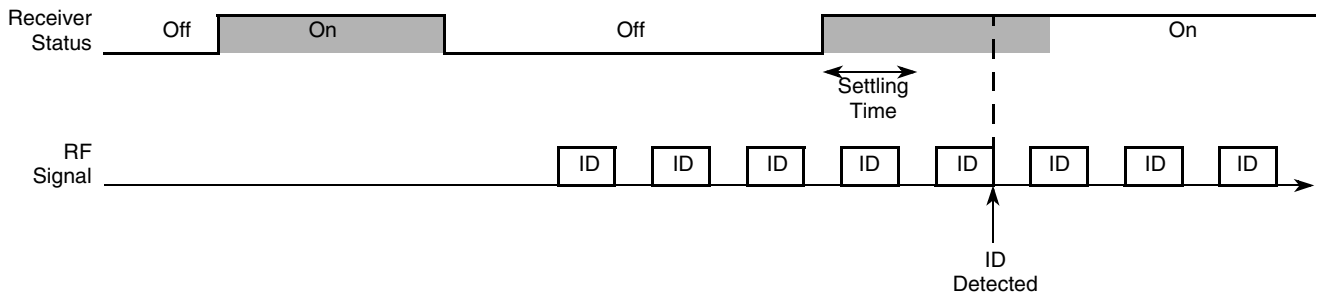


Figure 12. Receiver Usable Window

13 Data Manager

In receive mode, Manchester coded data can be processed internally by the data manager. After decoding, the data are output on the digital interface, in SPI format. This minimizes the load on the MCU.

The data manager, when enabled (DME = 1), has five purposes:

- ID detection: The received identifier is compared with the identifier stored in the ID register.
- Header recognition: The received header is compared with the one stored in the HEADER register.
- Clock recovery: The clock is recovered during reception of the preamble and is computed from the shortest received pulse. During the reception of the telegram, the recovered clock is constantly updated to the data rate of the incoming signal.
- Output data and recovered clock on digital interface: See Section 15.2, “Receive Mode.”
- End-of-message detection: An EOM consists of two consecutive NRZ ones or zeroes.

Table 8 details some MC33696 features versus DME values.

Table 8. the **MC33696 Features versus DME**

DME	Digital Interface Use	Data Format	Output
0	SPI deselected	Bit stream No clock	MOSI —
1	SPI master when CONFB = 1	Data bytes Recovered clock	MOSI SCLK

14 Receiver On/Off Control

In receive mode, on/off sequencing can be controlled internally, or managed externally by the MCU through the input pin STROBE.

If the internal timer is selected (SOE = 1),

- Off time is clocked by the strobe oscillator,
- On time is clocked by the crystal oscillator, enabling accurate control of the on time and, therefore, the current consumption of the whole system.

Each time is defined with the associated value found in the RXONOFF register.

- On time = RON[3:0] x 512 x T_{digclk} (see Table 20; begins after the crystal oscillator has started),
- Off time = receiver OFF time = N x T_{Strobe} + MIN (T_{Strobe} / 2, receiver On time), with N decoded from ROFF[2:0] (see Table 21).

The strobe oscillator is a relaxation oscillator in which an external capacitor C3 is charged by an internal current source (see Figure 47). When the threshold is reached, C3 is discharged and the cycle restarts. The strobe frequency is $F_{Strobe} = 1/T_{Strobe}$ with $T_{Strobe} = 10^6$ x C3.

In receive mode, setting the STROBE pin to V_{CCIO} at any time forces the circuit on. As V_{CCIO} is above the oscillator threshold voltage, the condition on which the STROBE pin is set to V_{CCIO} is detected internally, and the oscillator pulldown circuitry is disabled. This limits the current consumption. After a strobe forced at “1”, the external driver should pass via a “0” state to discharge the capacitor before going to high impedance state (otherwise, the ON time would last a long time after the driver release).

When the strobe oscillator is running (i.e., during an off time), forcing the STROBE pin to V_{GND} stops the strobe clock and, therefore, maintains the circuit off.

Figure 13 shows the associated timings.

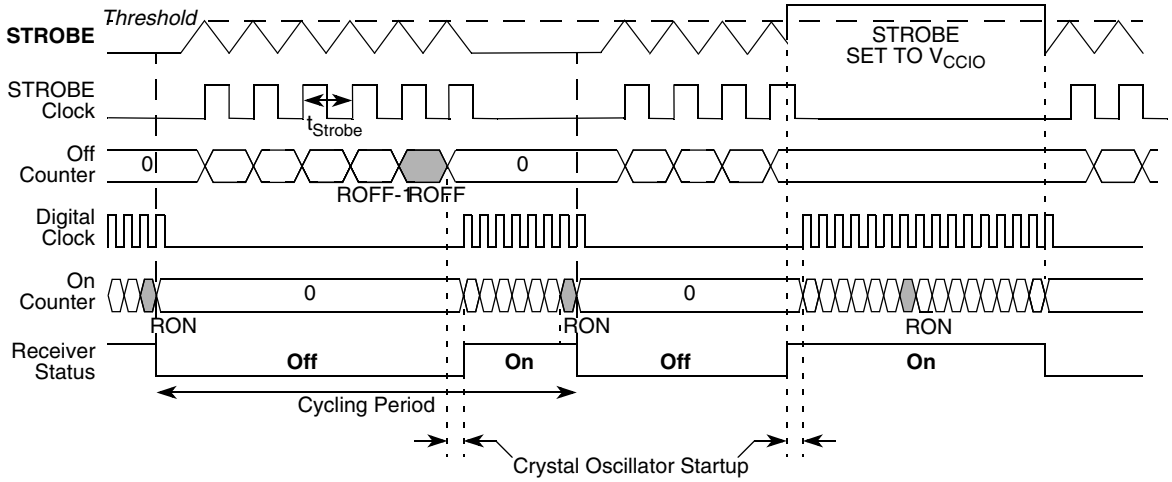


Figure 13. Receiver On/Off Sequence

15 Communication in Transmit and Receive Mode

15.1 Transmit Mode

The SPI is deselected. The MC33696 receives the telegram to transmit on the MOSI line (see Figure 14).

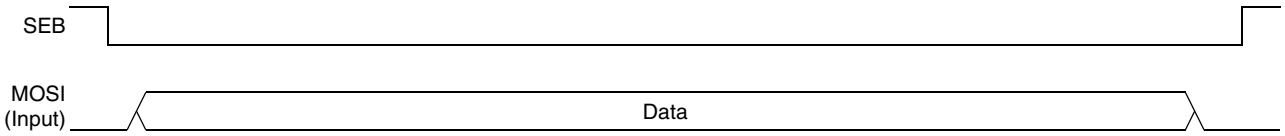


Figure 14. Transfer in Transmit Mode

In OOK modulation (MODU=0), modulation is performed by switching on and off the RF output stage.

MOSI = 0: output stage off

MOSI = 1: output stage on

In FSK modulation (MODU = 1), modulation is performed by switching the RF carrier between two values.

MOSI = 0: $f_{carrier0}$ corresponding to a logical 0

MOSI = 1: $f_{carrier1}$ corresponding to a logical 1

See the FRM bit description (Figure 20) and Section 17.3, “Frequency Registers,” for more details about setting carrier frequencies.

15.2 Receive Mode

The MC33696 is master and drives the digital interface in one of two ways, depending on the selection of the data manager.

1. DME = 1: The data manager is enabled. The SPI is master. The MC33696 sends the recovered clock on SCLK and the received data on the MOSI line. Data are valid on falling edges of SCLK. If an entire number of bytes is received, the data manager may add an extra byte. The content of this extra byte is random. If the data received do not fill an entire number of bytes, the data manager will fill the last byte randomly. Figure 15 shows a typical transfer.

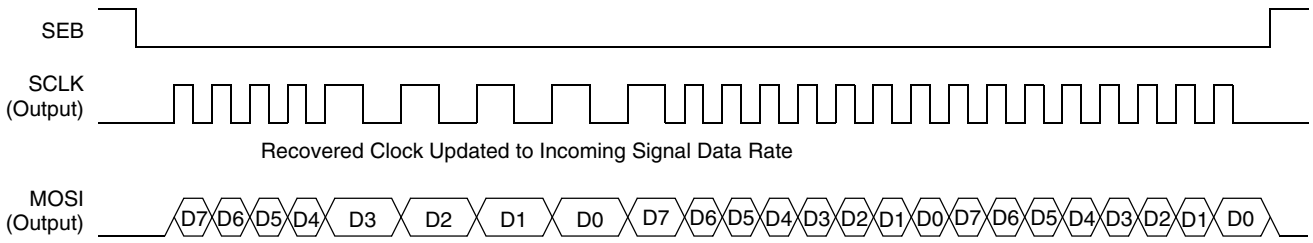


Figure 15. Typical Transfer in Receive Mode with Data Manager

2. DME = 0: The data manager is disabled. The SPI is deselected. Raw data are sent directly on the MOSI line, while SCLK remains at the low level.

16 Received Signal Strength Indicator (RSSI)

16.1 Module Description

In receive mode, a received signal strength indicator can be activated by setting bit RSSIE.

The input signal is measured at two different points in the receiver chain by two different means, as follows.

- At the IF filter output, a progressive compression logarithmic amplifier measures the input signal, ranging from the sensitivity level up to –50 dBm.

- At the LNA output, the LNA AGC control voltage is used to monitor input signals in the range –50 dBm to –20 dBm.

Therefore, the logarithmic amplifier provides information relative to the in-band signal, whereas the LNA AGC voltage senses the input signal over a wider band.

The RSSI information given by the logarithmic amplifier is available in:

- Analog form on pin RSSIOUT
- Digital form in the four least significant bits of the status register RSSI

The information from the LNA AGC is available in digital form in the four most significant bits of status register RSSI.

The whole content of status register RSSI provides 2 x 4 bits of RSSI information about the incoming signal (see Section 17.6, “RSSI Register”).

Figure 16 shows a simplified block diagram of the RSSI function.

The quasi peak detector (D1, R1, C1) has a charge time of about 20 µs to avoid sensitivity to spikes.

R2 controls the decay time constant of about 5 ms to allow efficient smoothing of the OOK modulated signal at low data rates. This time constant is useful in continuous mode when S2 is permanently closed.

To allow high-speed RSSI updating in peak pulse measurement, a discharge circuit (S1) is required to reset the measured voltage and to allow new peak detection.

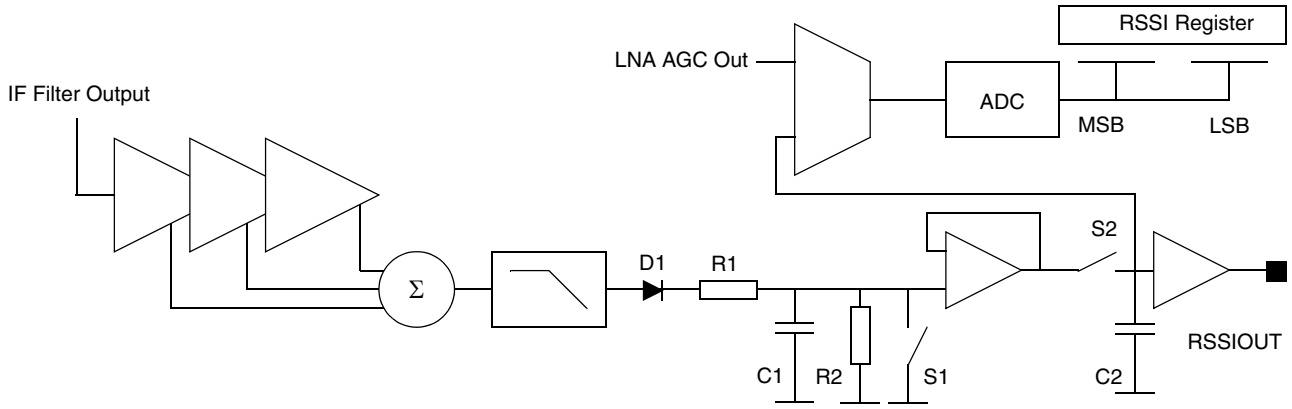


Figure 16. RSSI Simplified Block Diagram

S2 is used to sample the RSSI voltage to allow peak pulse measurement (S2 used as sample and hold), or to allow continuous transparent measurement (S2 continuously closed).

The 4-bit analog-to-digital convertor (ADC) is based on a flash architecture. The conversion time is 16 x T_{diglck}. As a single convertor is used for the two analog signals, the RSSI register content is updated on a 32 x T_{digclk} timebase.

If RSSIE is reset, the whole RSSI module is switched off, reducing the current consumption. The output buffer connected to RSSIOUT is set to high impedance.

16.2 Operation

Two modes of operation are available: sample mode and continuous mode.

16.2.1 Sample Mode

Sample mode allows the peak power of a specific pulse in an incoming frame to be measured.

The quasi peak detector is reset by closing S1. After 7 x T_{digclk}, S1 is released. S2 is closed when RSSIC is set high. On the falling edge of RSSIC, S2 is opened. The voltage on RSSIOUT is sampled and held. The last RSSI conversion results are stored in the RSSI register and no further conversion is done.

The RSSI register is updated every 32 x T_{digclk}. Therefore, the minimum duration of the high pulse on RSSIC is 32 x T_{digclk}.

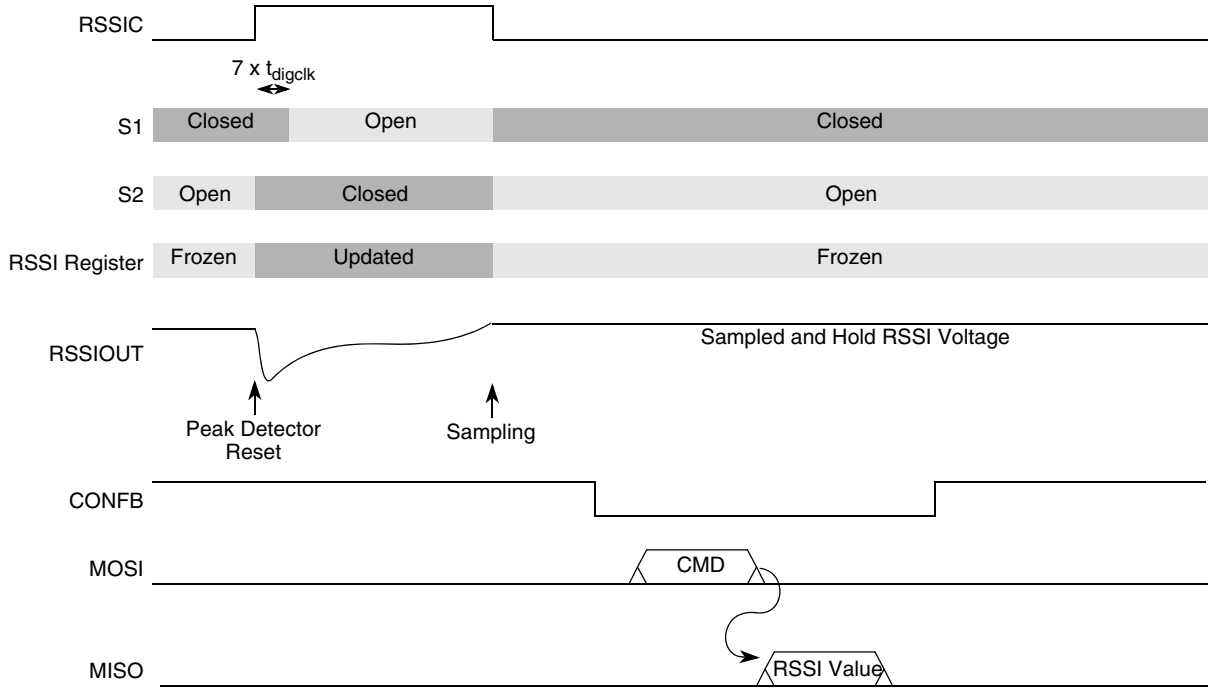


Figure 17. RSSI Operation in Sample Mode

16.2.2 Continuous Mode

Continuous mode is used to make a peak measurement on an incoming frame, without having to select a specific pulse to be measured.

The quasi peak detector is reset by closing S1. After 7 x T_{digclk}, S1 is opened. S2 is closed when RSSIC is set high. As long as RSSIC is kept high, S2 is closed, and RSSIOUT follows the peak value with a decay time constant of 5 ms.

The ADC runs continuously, and continually updates the RSSI register. Thus, reading this register gives the most recent conversion value, prior to the register being read. The minimum duration of the high pulse on CONFB is 32 x T_{digclk}.

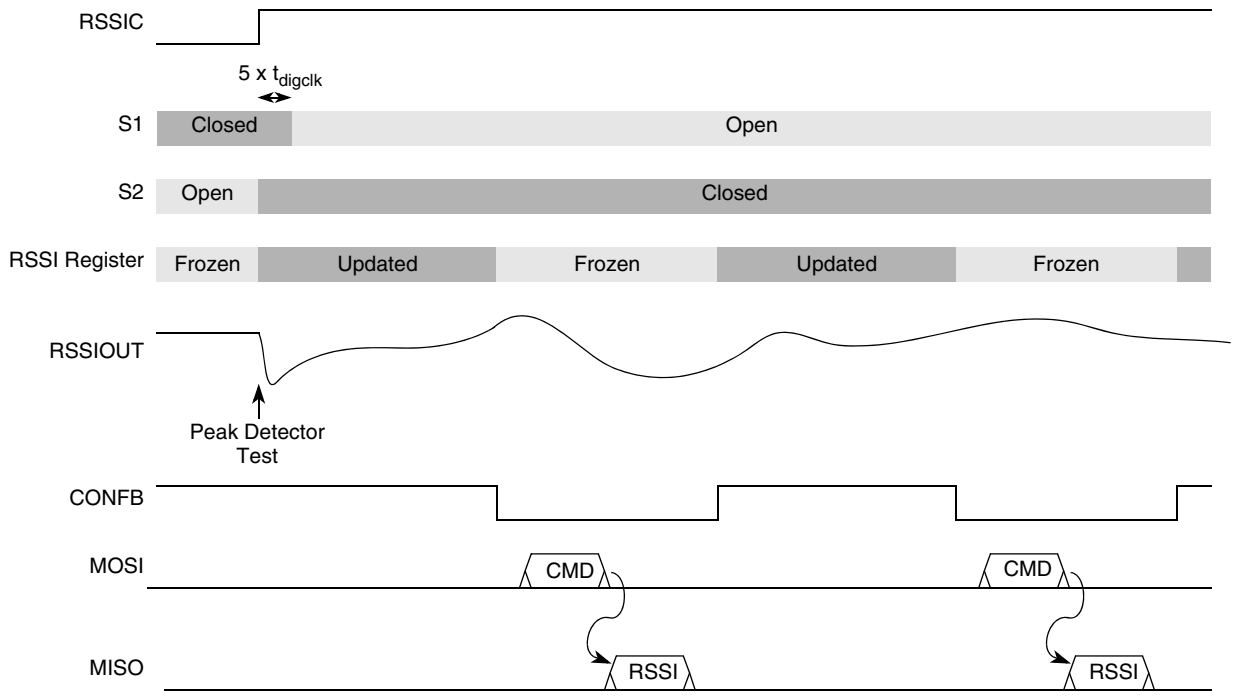


Figure 18. RSSI Operation in Continuous Mode

17 Configuration, Command, and Status Registers

This section discusses the internal registers, which are composed of two classes of bits.

- Configuration and command bits allow the MC33696 to operate in a suitable configuration.
- Status bits report the current state of the system.

All registers can be accessed by the SPI; these registers are described below.

At power-on, the POR resets all registers to a known value (in the shaded rows in the following tables). This defines the MC33696's default configuration.

After POR, CONFB forces a low level. Therefore, an external pullup resistor is required to avoid entering configuration mode.

17.1 Configuration Registers

Figure 19 describes configuration register 1, CONFIG1.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
Bit Name	LOF1	LOF0	CF1	CF0	RESET	SL	LVDE	CLKE	$00
Reset Value	1	0	0	1	0	0	0	1	

Figure 19. CONFIG1 Register

Table 9. LOF[1:0] and CF[1:0] Setting Versus Carrier Frequency

Carrier Frequency	LOF1	LOF0	CF1	CF0
304 MHz	0	0	0	0
315 MHz	1	0	0	0
426 MHz	0	1	0	1
434 MHz	0	1	0	1
868 MHz	0	1	1	1
915 MHz	1	1	1	1

RESET is a global reset. The bit is cleared internally, after use.

0 = no action

1 = reset all registers and counters

SL (Switch Level) selects the active level of the SWITCH output pin.

Table 10. Active Level of SWITCH Output Pin

SL	Transceiver Function	Level on SWITCH
0	Receiving	Low
	Transmitting	High
1	Transmitting	Low
	Receiving	High

LVDE (Low Voltage Detection Enable) enables the low voltage detection function.

0 = disabled

1 = enabled

NOTE

This bit is cleared by POR. In the event of a complete loss of the supply voltage, LVD is disabled at power-up, but the information is not lost as the status bit LVDS is set by POR.

CLKE (Clock Enable) controls the DATACLK output buffer.

0 = DATACLK remains low

1 = DATACLK outputs $F_{dataclk}$

Figure 20 describes configuration register 2, CONFIG2.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
Bit Name	DSREF	FRM	MODU	DR1	DR0	TRXE	DME	SOE	$01
Reset Value	0	0	0	1	0	0	0	0	

Figure 20. CONFIG2 Register

DSREF (Data Slicer Reference) selects the data slicer reference.

0 = Fixed reference (cannot be used in FSK)

1 = Adaptive reference (recommended for maximum sensitivity in OOK and FSK)

In the case of FSK modulation (MODU = 1), DSREF must be set.

FRM (Frequency Register Manager) enables either a user friendly access to one frequency register or a direct access to the two frequency registers.

0 = The carrier frequency and the FSK deviation are defined by the F register

1 = The local oscillator frequency and the two carrier frequencies are defined by two frequency registers, F and FT.

MODU (Modulation) sets the data modulation type.

0 = On/Off Keying (OOK) modulation

1 = Frequency Shift Keying (FSK) modulation

DR[1:0] (Data Rate) configure the receiver blocks operating in base band.

- Low-pass data filter
- Low-pass average filter generating the data slicer reference, if DSREF is set
- Data manager

Table 11. Base Band Parameter Configuration

DR1	DR0	Data Filter Cut-off Frequency	Average Filter Cut-off Frequency	Data Manager Data Rate Range
0	0	6 kHz	0.5 kHz	2–2.8 kBd
0	1	12 kHz	1 kHz	4–5.6 kBd
1	0	24 kHz	2 kHz	8–10.6 kBd
1	1	48 kHz	4 kHz	16–22.4 kBd

If the data manager is disabled, the incoming signal data rate must be lower than or equal to the data manager maximum data rate.

TRXE (Transceiver Enable) enables the whole transceiver.

0 = standby mode

1 = other modes can be activated

DME (Data Manager Enable) enables the data manager.

0 = disabled

1 = enabled

SOE (Strobe Oscillator Enable) enables the strobe oscillator.

0 = disabled

1 = enabled

Figure 21 describes configuration register 3, CONFIG3.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
Bit Name	AFF1	AFF0	OLS	LVDS	ILA1	ILA0	OLA1	OLA0	$02
Reset Value	0	0	1	1	0	0	0	0	

Figure 21. CONFIG3 Register

OLS (Out of Lock Status) indicates the current status of the PLL.

0 = The PLL is in lock-in range

1 = The PLL is out of lock-in range

LVDS (Low Voltage Detection Status) indicates that a low voltage event has occurred when LVDE = 1. This bit is read-only and is cleared after a read access.

0 = No low voltage detected

1 = Low voltage detected

ILA[1:0] (Input Level Attenuation) define the RF input level attenuation.

Table 12. RF Input Level Attenuation

ILA1	ILA0	RF Input Level Attenuation	See Parameter Number
0	0	0 dB	2.5
0	1	8 dB	2.6
1	0	16 dB	2.7
1	1	30 dB	2.8

Values in Table 12 assume the LNA gain is not reduced by the AGC.

OLA[1:0] (Output Level Attenuation) define the RF output level attenuation.

Table 13. RF Output Level Attenuation

OLA1	OLA0	RF Output Level Attenuation	See Parameter Number
0	0	0 dB	4.20
0	1	6 dB	4.3
1	0	12 dB	4.4
1	1	25 dB	4.5

AFF[1:0] (Average Filter Frequency) define the average filter cut-off frequency if the AFFC bit is set.

Table 14. Average Filter Cut-off Frequency

AFF1	AFF0	Average Filter Cut-off Frequency
0	0	0.5 kHz
0	1	1 kHz
1	0	2 kHz
1	1	4 kHz

If AFFC is reset, the average filter frequency is directly defined by bits DR[1:0], as shown in Table 11.

If AFFC is set, AFF[1:0] allow the overall receiver sensitivity to be improved by reducing the average filter cut-off frequency. The typical preamble duration of three Manchester zeroes or ones at the data rate must then be increased, as shown in Table 15.

Table 15. Minimum Number of Manchester Symbols in Preamble versus DR[1:0] and AFF[1:0]

		DR[1:0]			
		00	01	10	11
AFF[1:0]	00	3	6	12	24
	01	—	3	6	12
	10	—	—	3	6
	11	—	—	—	3

17.2 Command Register

Figure 22 describes the Command register, COMMAND.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
Bit Name	AFFC	IFLA	MODE	RSSIE	EDD	RAGC	FAGC	—	$03
Reset Value	0	0	0	0	1	0	0	1	

Figure 22. COMMAND Register

AFFC (Average Filter Frequency Control) enables direct control of the average filter cut-off frequency.

0 = Average filter cut-off frequency is defined by DR[1:0]

1 = Average filter cut-off frequency is defined by AFF[1:0]

IFLA (IF Level Attenuation) controls the maximum gain of the IF amplifier in OOK modulation.

0 = No effect

1 = Decreases by 20 dB (typical) the maximum gain of the IF amplifier, in OOK modulation only

The reduction in gain can be observed if the IF amplifier AGC system is disabled (by setting RAGC = 1).

MODE selects the mode.

0 = Receive mode
1 = Transmit mode

RSSIE (RSSI Enable) enables the RSSI function.

0 = Disabled
1 = Enabled

EDD (Envelop Detector Decay) controls the envelop detector decay.

0 = Slow decay for minimum ripple
1 = Fast decay

RAGC (Reset Automatic Gain Control) resets both receiver internal AGCs.

0 = No action
1 = Sets the gain to its maximum value

A first SPI access allows RAGC to be set; a second SPI access is required to reset it.

FAGC (Freeze Automatic Gain Control) freezes both receiver AGC levels.

0 = No action
1 = Holds the gain at its current value

17.3 Frequency Registers

Figure 23 and Figure 24 define the Frequency registers, F and FT.

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Addr
Bit Name	FSK3	FSK2	FSK1	FSK0	F11	F10	F9	F8	$04
Reset Value	0	1	0	0	1	0	0	0	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Bit Name	F7	F6	F5	F4	F3	F2	F1	F0	$05
Reset Value	0	0	0	0	0	0	0	0	

Figure 23. F Register

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Addr
Bit Name	FTA11	FTA10	FTA9	FTA8	FTA7	FTA6	FTA5	FTA4	$06
Reset Value	0	1	1	1	0	0	0	0	
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
Bit Name	FTA3	FTA2	FTA1	FTA0	FTB11	FTB10	FTB9	FTB8	$07
Reset Value	0	0	0	0	0	1	1	1	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Bit Name	FTB7	FTB6	FTB5	FTB4	FTB3	FTB2	FTB1	FTB0	$08
Reset Value	0	0	0	0	0	0	0	1	

Figure 24. FT Register

How these registers are used is determined by the FRM bit, which is described below.

FRM = 0 (User Friendly Access)

Whatever type of modulation is used (OOK or FSK), bits F[11:0] define the carrier frequency $F_{carrier}$. The local oscillator frequency F_{LO} is then set automatically to $F_{carrier} + F_{IF}$ (with F_{IF} = intermediate frequency). In addition,

- in the case of OOK modulation (MODU = 0):
  - FSK[3:0], FTA[11:0], and FTB[11:0] are not used.
- in the case of FSK modulation (MODU = 1):
  - FSK[3:0] sets the frequency deviation Df as defined in Table 16.

Table 16. Frequency Deviation Definition

CF[1:0]	Frequency Deviation Δf
00, 01	F_{ref} x(FSK[3:0]+1)/ 2048
11	F_{ref}x(FSK[3:0]+1)/ 1024

Table 17 gives a numerical example in the 434 MHz band (CF[1:0] = 01).

Table 17. Frequency Numerical Example (434 MHz Band)

FSK[3:0]	Frequency Deviation Δf
0000	± 12 kHz
0001	± 24 kHz
0010	± 36 kHz
...	...
1111	± 192 kHz

Then, two frequencies are calculated internally, as follows.

— $F_{carrier0}$ = F[11:0] - Δf to transmit a logical 0

— $F_{carrier1}$ = F[11:0] + Δf to transmit a logical 1

FTA[11:0] and FTB[11:0] are not used

FRM = 1 (Direct Access)

Whatever type of modulation is used (OOK or FSK), F[11:0] defines the receiver local oscillator frequency F_{LO}, and,

- if OOK modulation is used (MODU = 0):
  - FTA[11:0] define the carrier frequency $F_{carrier}$
  - FTB[11:0] are not used
- if FSK modulation is used (MODU = 1):
  - FTA[11:0] define the carrier frequency $F_{carrier0}$ to transmit a logical 0
  - FTB[11:0] define the carrier frequency $F_{carrier1}$ to transmit a logical 1

Table 18 defines the value to be binary coded in the frequency registers F[11;0], FTA/B[11:0], versus the desired frequency value F (in Hz).

Table 18. Frequency Register Value versus Frequency Value F

CF[1:0]	Frequency Register Value
00, 01	(2 x F/F_{ref}-35) x 2048
11	(F/F_{ref}-35) x 2048

Conversely, Table 19 gives the desired frequency F and the frequency resolution versus the value of the frequency registers F[11;0].

Table 19. Frequency Value F versus Frequency Register Value

CF[1:0]	Frequency (Hz)	Frequency Resolution (Hz)
00, 01	(35 + F[11;0]/2048)xF_{ref}/2	F_{ref}/4096
11	(35 + F[11;0]/2048)xF_{ref}	F_{ref}/2048

17.4 Receiver On/Off Duration Register

Figure 25 describes the receiver on/off duration register, RXONOFF.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
Bit Name	—	RON3	RON2	RON1	RON0	ROFF2	ROFF1	ROFF0	$09
Reset Value	0	1	1	1	1	1	1	1	

Figure 25. RXONOFF Register

RON[3:0] (Receiver On) define the receiver on time (after crystal oscillator startup) as described in Section 14, “Receiver On/Off Control.”

Table 20. Receiver On Time Definition

RON[3:0]	Receiver On Time: N x 512 x T_{digclk}
0000	Forbidden value
0001	1
0010	2
...	...

Table 20. Receiver On Time Definition

RON[3:0]	Receiver On Time: N x 512 x T_{digclk}
1111	15

ROFF[2:0] (Receiver Off) define the receiver off time as described in Section 14, “Receiver On/Off Control.”

Table 21. Receiver Off Time Definition

ROFF[2:0]	Receiver Off Time: N x T_{Strobe}
000	1
001	2
010	4
011	8
100	12
101	16
110	32
111	63

17.5 ID and Header Registers

Figure 26 defines the ID register, ID.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
Bit Name	IDL1	IDL0	ID5	ID4	ID3	ID2	ID1	ID0	$0A
Reset Value	1	1	0	0	0	0	0	0	

Figure 26. ID Register

IDL[1:0] (Identifier Length) sets the length of the identifier, as shown on Table 22.

Table 22. ID Length Selection

IDL1	IDL0	ID Length
0	0	2 bits
0	1	4 bits
1	0	5 bits
1	1	6 bits

ID[5:0] (Identifier) sets the identifier. The ID is Manchester coded. Its LSB corresponds to the register’s LSB, whatever the specified length.

Figure 27 defines the Header register, HEADER.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
Bit Name	HDL1	HDL0	HD5	HD4	HD3	HD2	HD1	HD0	$0B
Reset Value	1	0	0	0	0	0	0	0	

Figure 27. HEADER Register

HDL[1:0] (Header Length) sets the length of the header, as shown on Table 23.

Table 23. Header Length Selection

HDL1	HDL0	HD Length
0	0	1 bits
0	1	2 bits
1	0	4 bits
1	1	6 bits

HD[5:0] (Header) sets the header. The header is Manchester coded. Its LSB corresponds to the register's LSB, whatever the specified length.

17.6 RSSI Register

Figure 28 describes the RSSI Result register, RSSI.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
Bit Name	RSSI7	RSSI6	RSSI5	RSSI4	RSSI3	RSSI2	RSSI1	RSSI0	$0C
Reset Value	0	0	0	0	0	0	0	0	

Figure 28. RSSI Register

Bits RSSI[7:4] contain the result of the analog-to-digital conversion of the signal measured at the LNA output.

Bits RSSI[3:0] contain the result of the analog-to-digital conversion of the signal measured at the IF filter output.

18 Controller

This section describes how the MC33696 controller executes sequences of operations, relative to the selected mode. The controller is a finite state machine, clocked at T_{digclk}. An overview is presented in Figure 29 (note that some branches refer to other diagrams that provide more detailed information).

There are four different modes: configuration, transmit, receive, and standby/LVD. Each mode is exclusive and can be entered in different ways, as follows.

- External signal: CONFB for configuration mode,
- External signal and configuration bits: CONFB, TRXE, and/or MODE for all other modes,

- External signal and internal conditions: see Figure 33 and Figure 35 for information on how to enter standby/LVD mode.

After a POR, the circuit is in state 60 (see Figure 29) and configuration registers' content is set to the reset value.

At any time, a low level applied to CONFB forces the finite state machine into state 1, whatever the current state. This is not always shown in state diagrams, but must always be considered.

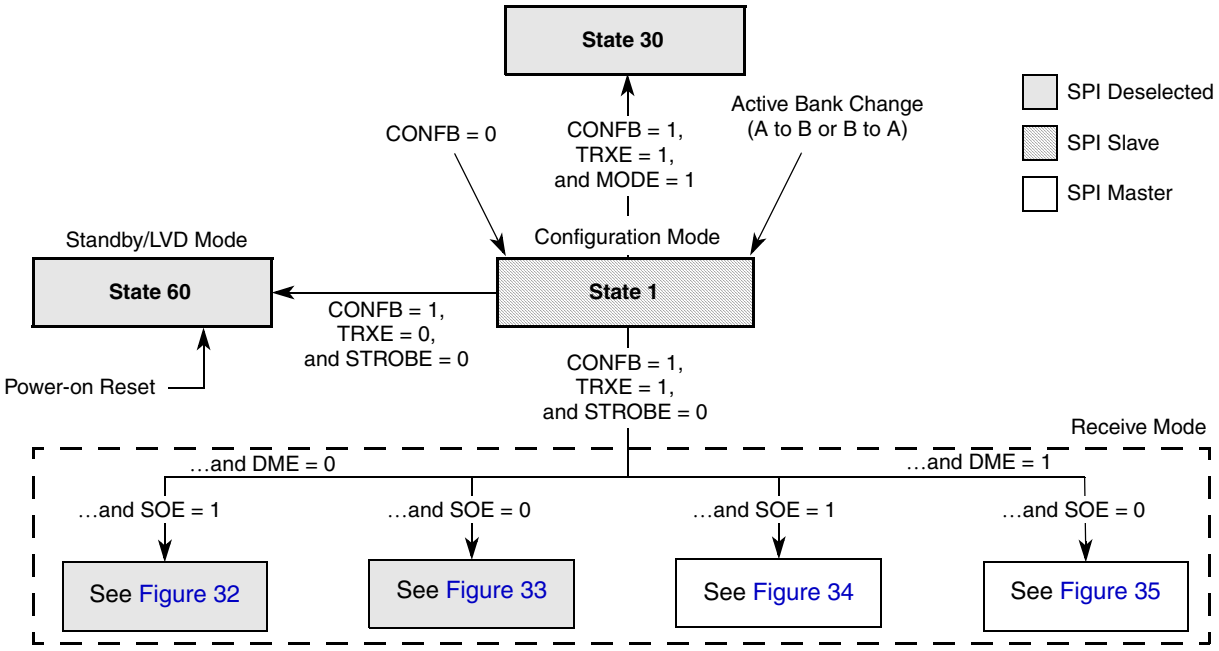


Figure 29. State Machine Overview

18.1 Configuration Mode

The configuration mode is selected by the microcontroller unit (MCU) to write to the internal registers (to configure the system) or to read them. In this mode, the SPI is a slave. The analog parts (receiver and transmitter) remain in the state (on, off) they were in prior to entering configuration mode, until a new configuration changes them. In configuration mode, data can be neither sent nor received. As long as a low level is applied to CONFB, the circuit stays in State 1, the only state in this mode.

Figure 30 and Figure 31 describe the two valid sequences for enabling a correct transition from Standby/LVD mode to configuration mode.

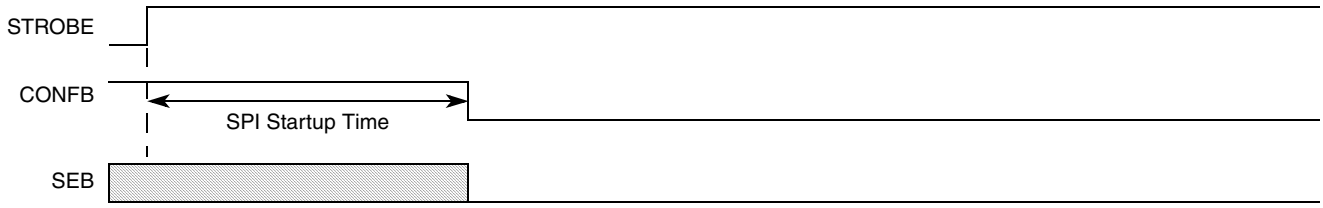


Figure 30. First Valid Sequence from Standby/LVD Mode to Configuration Mode

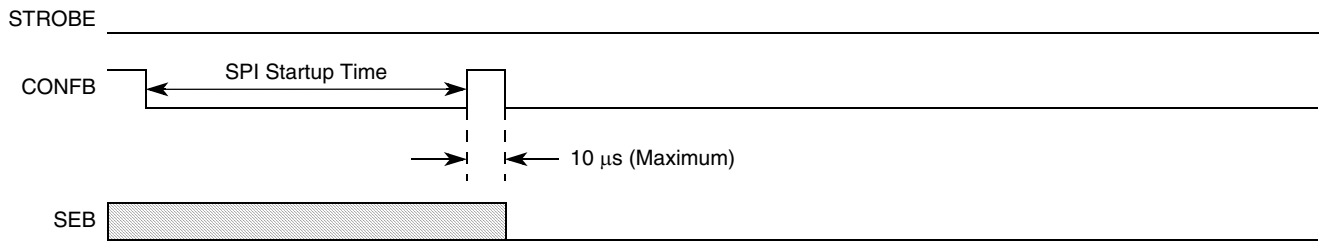


Figure 31. Second Valid Sequence from Standby/LVD Mode to Configuration Mode

18.2 Transmit Mode

In transmit mode, the state diagram is reduced to only one state: state 30. The circuit is either waiting for a digital telegram to send, or is sending one. In this mode, the circuit can be considered as a simple RF physical interface. The information presented on MOSI is sent directly in RF (according to the selected modulation), with no internal processing.

Data transmission is possible only if the PLL is within the lock-in range. Therefore, during transmission, if the PLL switches out of lock-in range, the RF output stage is switched off internally, thereby preventing data from being transmitted in an unwanted band.

18.3 Receive Mode

The receiver is either waiting for an RF telegram, or is receiving one. Four different processes are possible, as determined by the values of the DME and SOE bits. The transmitter part is maintained off. A state diagram describes the sequence of operations in each case.

NOTE

If the STROBE pin is tied to a high level before switching to receive mode, the receiver does not go through an off or standby state.

18.3.1 Data Manager Disabled and Strobe Oscillator Enabled

Raw received data are sent directly on the MOSI line. Figure 32 shows the state diagram.

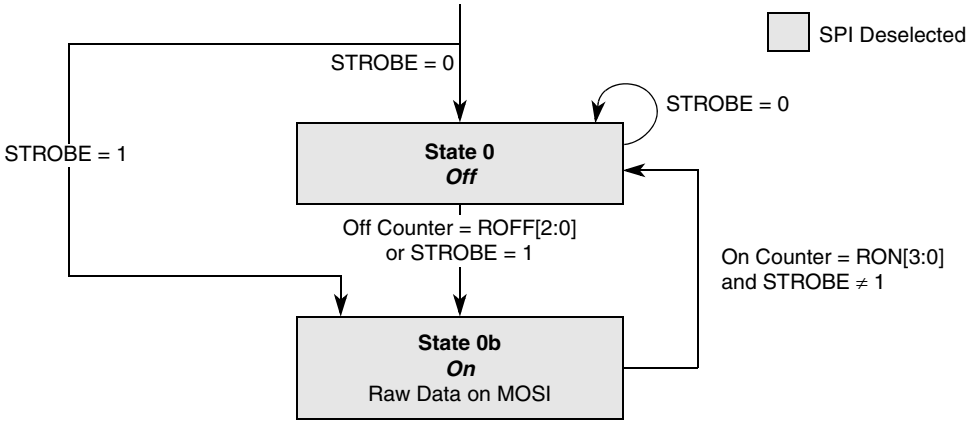


Figure 32. Receive Mode, DME = 0, SOIE = 1

State 0: The receiver is off, but the strobe oscillator and the off counter are running. Forcing the STROBE pin low maintains the system in this state.

State 0b: The receiver is kept on by the STROBE pin or the on counter. Raw data are output on the MOSI line.

For all states: At any time, a low level applied to CONFB forces the state machine to state 1.

18.3.2 Data Manager Disabled and Strobe Pin Control

Raw received data are sent directly on the MOSI line. Figure 33 shows the state diagram.

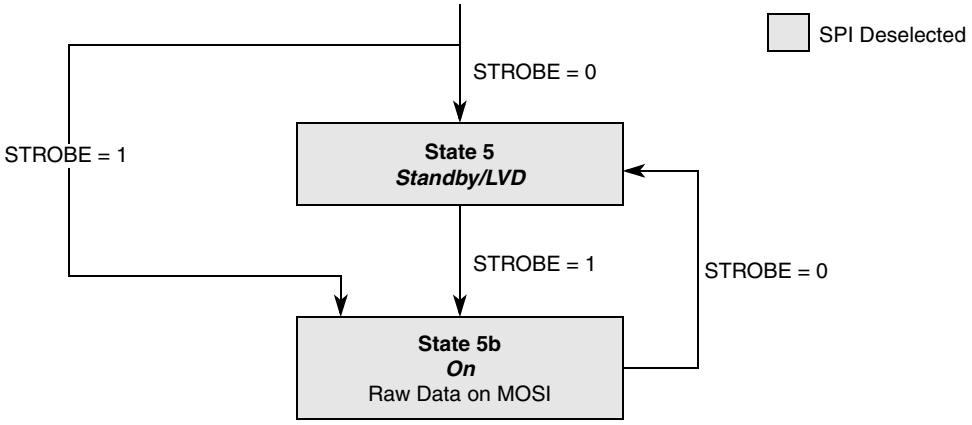


Figure 33. Receive Mode, DME = 0, SOE = 0

State 5: The receiver is in standby/LVD mode. For further information, see Section 18.4, “Standby/LVD Mode.” A high level applied to STROBE forces the circuit to state 5b.

State 5b: The receiver is kept on by the STROBE pin. Raw data are output on the MOSI line.

For all states: At any time, a low level applied to CONFB forces the state machine to state 1.

18.3.3 Data Manager Enabled and Strobe Oscillator Enabled

Figure 34 shows the state diagram when the data manager and the strobe oscillator are enabled. in this configuration, the receiver is controlled internally by the strobe oscillator. However, external control via the STROBE pin is still possible, and overrides the strobe oscillator command.

State 10: The receiver is off, but the strobe oscillator and the off counter are running. Forcing STROBE pin to the low level maintains the system in this state.

State 11: The receiver is waiting for a valid ID. If an ID, or its complement, is detected, the state machine advances to state 12; otherwise, the circuit goes back to state 10 at the end of the RON time, if STROBE≠1.

State 12: An ID or its complement has been detected. The data manager is now waiting for a header or its complement. If neither a header, nor its complement, has been received before a time-out of 256 bits at data rate, the system returns to state 10.

State 13: A header, or its complement, has been received. Data and clock signals are output on the SPI port until EOM indicates the end of the data sequence. If the complement of the header has been received, output data are complemented also.

When an EOM occurs before the current byte is fully shifted out, dummy bits are inserted until the number of shifted bits is a multiple of 8.

For all states: At any time, a low level applied to STROBE forces the circuit to state 10, and a low level applied on CONFB forces the state machine to state 1.

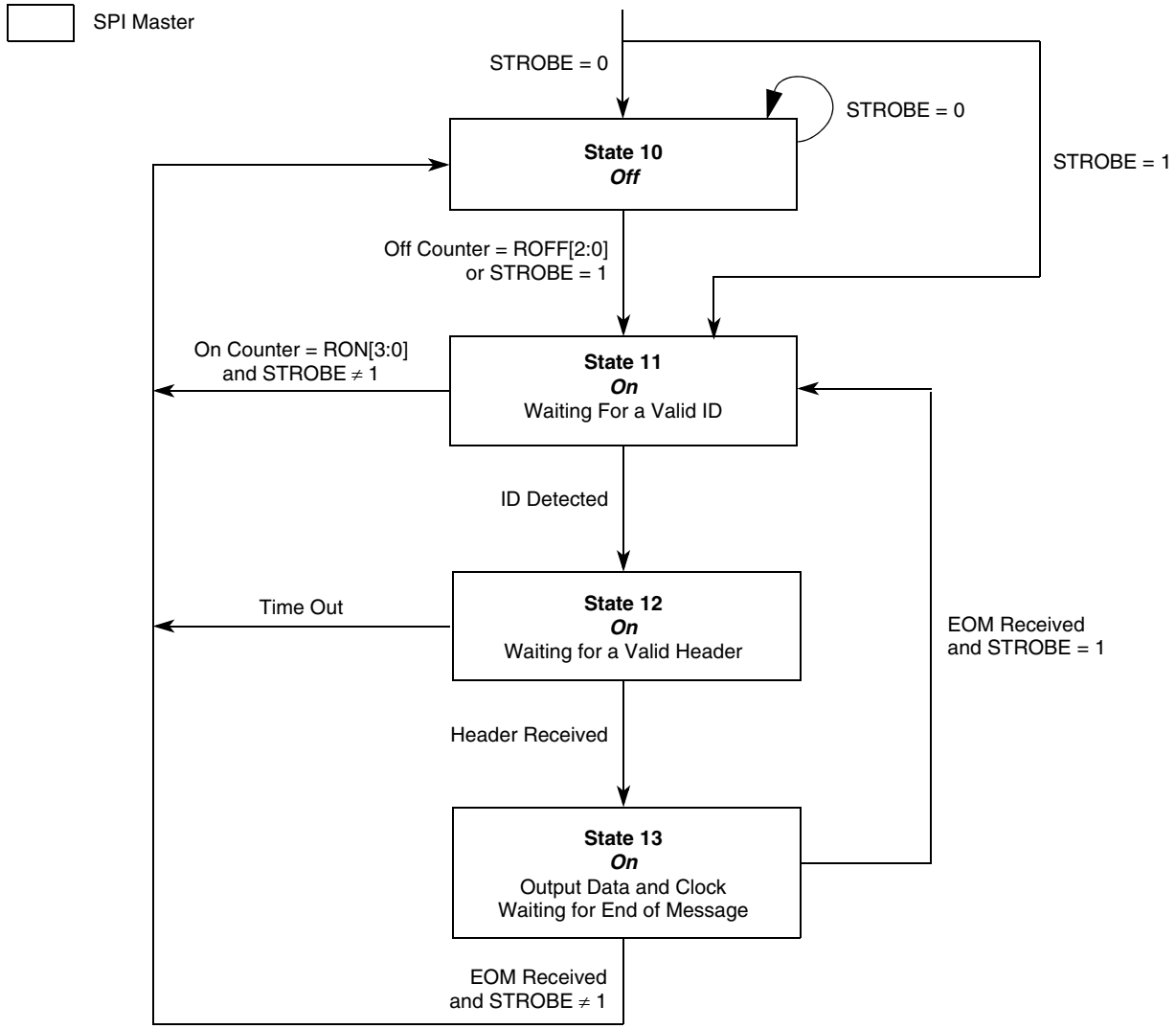


Figure 34. Receive Mode, DME = 1, SOE = 1

18.3.4 Data Manager Enabled and Strobe Pin Control

Figure 35 shows the state diagram when the data manager is enabled and the strobe oscillator is disabled. In this configuration, the receiver is controlled only externally by the MCU.

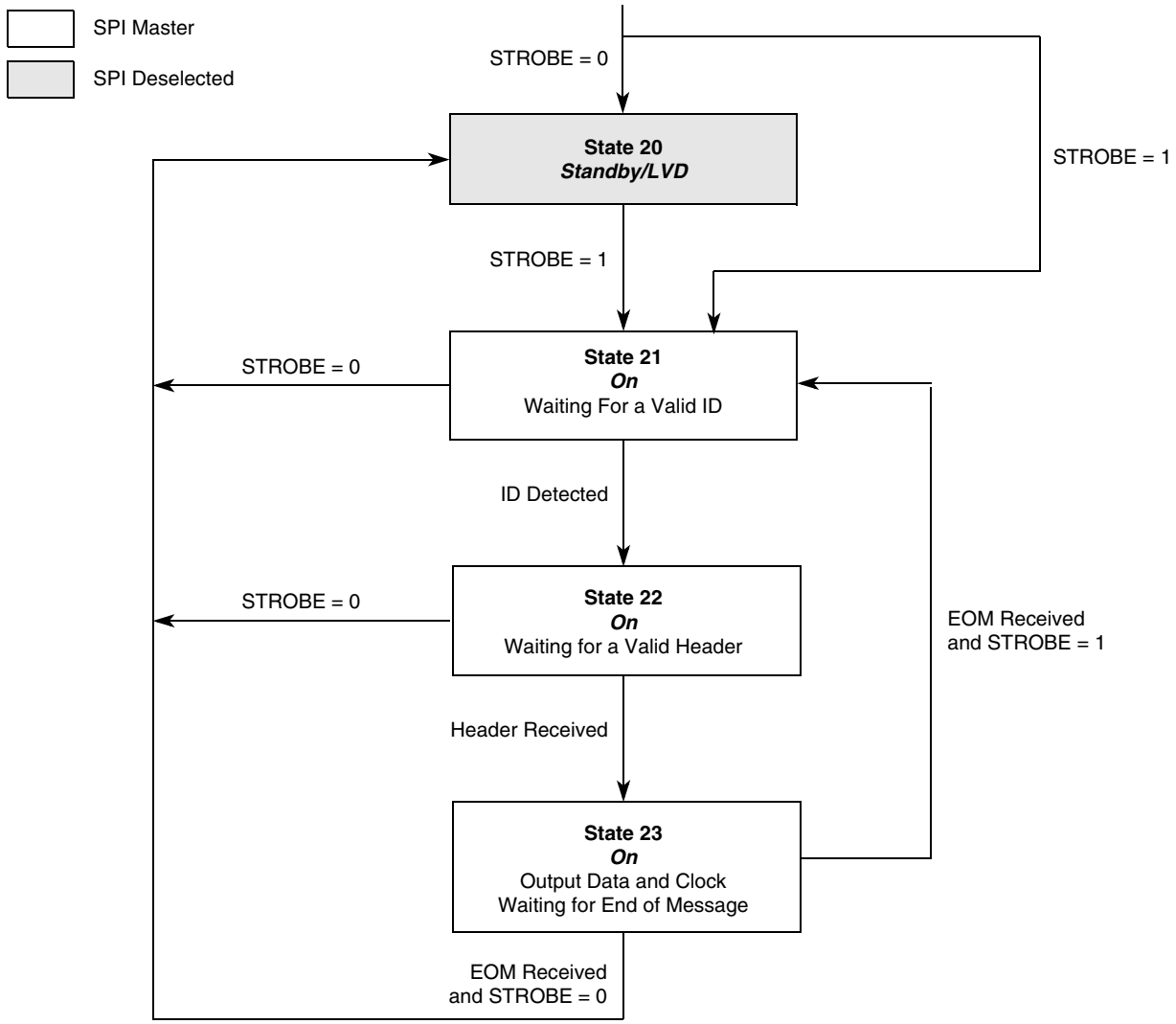


Figure 35. Receive Mode, DME = 1, SOE = 0

State 20: The receiver is in standby/LVD mode. For further information, see Section 18.4, “Standby/LVD Mode.” A high level applied to STROBE forces the circuit to state 21.

State 21: The circuit is waiting for a valid ID. If an ID, or its complement, is detected, the state machine advances to state 22; if not, the state machine will remain in state 21, as long as STROBE is high.

State 22: If a header, or its complement, is detected, the state machine advances to state 23. If not, the state machine will remain in state 22, as long as STROBE is high.

State 23: A header or its complement has been received; data and clock signals are output on the SPI port until an EOM indicates the end of the data sequence. If the complement of the header has been received,

output data are complemented also. When an EOM occurs before the current byte is fully shifted out, dummy bits are inserted until the number of shifted bits is a multiple of 8.

For all states: At any time, a low level applied to STROBE puts the circuit into state 20, and a low level applied to CONFB forces the state machine to state 1.

18.4 Standby/LVD Mode

Standby/LVD mode allows minimum current consumption to be achieved. Depending upon the value of the LVDE bit, the circuit is in standby mode (state 60) or LVD mode (state 5 and 20).

LVDE = 0: The transceiver is in standby; consumption is reduced to leakage current (current state after POR).

LVDE = 1: The LVD function is enabled; consumption is in the range of tens of microamperes.

The only way to exit this mode is to go back to configuration mode by applying a low level to CONFB.

18.5 Transition Time

Table 24 details the different times that must be considered for a given transition in the state machine, once the logic conditions for that transition are met.

Table 24. Transition Time Definition

Transition State x -> y	Crystal Oscillator Startup Time, Parameter 5.10	PLL Timing	Receiver Preamble Time[1]	Receiver On-to-Off Time, Parameter 1.12
Standby to SPI running, state 60 -> 1	√			
Standby to receiver running, states 5 -> 5b, 20 -> 21	√	Lock time parameter 5.9	√	
Off to receiver running, states 0 -> 0b, 10 -> 11	√	Lock time parameter 5.9	√	
Configuration to receiver running, states 1 -> (0b, 5b, 11, 21)		0 or lock time parameter 5.1 or lock time parameter 5.9 [2]	√	
Configuration to transmitter mode, state 1 -> 30		0 or lock time parameter 5.1 or lock time parameter 5.9 [2]		
Receiver running to configuration mode, state (0b, 5b, 11, 12, 13, 21, 22, 23) -> 1,				
Transmitter mode to configuration mode, state 30 -> 1				
Receiver running to standby mode, state 5b -> 5, (21, 22, 23) -> 20				√
Receiver running to off mode, state 0b -> 0, (11, 12, 13) -> 10				√

NOTES:
1 See Section 12.2, “Preamble, Identifier, Header, and Message.”
2 Depending on the PLL status before entering configuration mode. For example, the transition time from standby to receiver running (FSK modulation, 19.2 kBd, AFFC = 0, data manager enabled) is: 0.6 ms + 50 µs + (3 + 1)/19.2k = 970 µs.

19 Electrical Characteristics

19.1 General Parameters

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions Comments	Limits			Unit
			Min	Typ	Max	
1.2	Supply current in receive mode	Receiver on	—	10.3	13	mA
1.3		Strobe oscillator only	—	24	50	µA
1.4	Supply current in transmit mode	Continuous wave (CW) OLA[1:0}=00	—	13.5	17.5	mA
1.5		No power output	—	6.1	8	mA
1.6	Supply current in standby mode	–40°C ≤ T_A ≤ 25°C	—	260	700	nA
1.8		T_A = 85°C	—	800	1200	nA
1.9	Supply current in LVD mode	LVDE = 1	—	35	50	µA
1.12	Receiver on-to-off time	Supply current reduced to 10%	—	100	—	µs
1.13	VCC2 voltage regulator output	2.7 V < V_{CC}	2.4	2.6	2.8	V
1.14		2.1 V ≤ V_{CC} ≤ 2.7 V	—	V_{CC}–0.1	—	V
1.15	VCCDIG2 voltage regulator output	Circuit in standby mode (V_{CCDIG} = 3 V)	—	0.7 x V_{CCDIG}	—	V
1.16		Circuit in all other modes	1.4	1.6	1.8	V
1.19	Voltage on VCC (Preregulator output)	Receive mode with VCCIN=5V	2.4	—	—	V

19.2 Receiver: RF Parameters

RF parameters assume a matching network between test equipment and the D.U.T, and apply to all bands unless otherwise specified.

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions, Comments	Limits				Unit
			Min	Typ	Max (FCE, FJE)	Max (FCAE, FJAE)	
2.2	OOK sensitivity at 315 MHz	DME = 1, DSREF = 1, DR = 4.8 kbps, PER = 0.1	—	–104	–99	–97	dBm
2.40	OOK sensitivity at 434 MHz	DME = 1, DSREF = 1, DR = 4.8 kbps, PER = 0.1	—	–103.5	–98	–96	dBm

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions, Comments	Limits				Unit
			Min	Typ	Max (FCE, FJE)	Max (FCAE, FJAE)	
2.41	OOK sensitivity at 868 MHz	DME = 1, DSREF = 1, DR = 4.8 kbps, PER = 0.1	—	–103	–98	–96	dBm
2.42	OOK sensitivity at 916 MHz	DME = 1, DSREF = 1, DR = 4.8 kbps, PER = 0.1	—	–103	–98	–96	dBm
2.24	FSK sensitivity at 315 MHz	DME = 1, DSREF = 1, DR = 4.8 kbps, $DF_{carrier}$ = ±64 kHz, PER = 0.1	—	–106.5	–102	–100	dBm
2.50	FSK sensitivity at 434 MHz	DME = 1, DSREF = 1, DR = 4.8 kbps, $DF_{carrier}$ = ±64 kHz, PER = 0.1	—	–105.5	–101	–99	dBm
2.51	FSK sensitivity at 868 MHz	DME = 1, DSREF = 1, DR = 4.8 kbps, $DF_{carrier}$ = ±64 kHz, PER = 0.1	—	–104.5	–100	–98	dBm
2.52	FSK sensitivity at 916 MHz	DME = 1, DSREF = 1, DR = 4.8 kbps, $DF_{carrier}$ = ±64 kHz, PER = 0.1	—	–105.4	–102	–100	dBm
2.35	Sensitivity improvement in RAW mode	DME = 0	—	0.6	—	—	dB
2.5	Sensitivity reduction	ILA[1:0] = 00	—	0	—	—	dB
2.6		ILA[1:0] = 01	—	8	—	—	dB
2.7		ILA[1:0] = 10	—	16	—	—	dB
2.8		ILA[1:0] = 11	—	30	—	—	dB
2.9	In-band jammer desensitization	Sensitivity reduced by 3 dB CW jammer at $F_{carrier}$ ± 50 kHz/OOK	—	–4	—	—	dBc
2.60		Sensitivity reduced by 3 dB CW jammer at $F_{carrier}$ ± 50 kHz/FSK	—	–6	—	—	dBc
2.11	Out-of-band jammer desensitization	Sensitivity reduced by 3dB CW jammer at $F_{carrier}$ ±1 MHz	—	37	—	—	dBc
2.12		Sensitivity reduced by 3dB CW jammer at $F_{carrier}$ ± 2 MHz	—	40	—	—	dBc
2.13	RFIN parallel resistance	Receive mode	—	300	—	—	Ω
2.14	RFIN parallel resistance	Transmit mode	1300	—	—	—	Ω
2.15	RFIN parallel capacitance	Receive and transmit modes	—	1.2	—	—	pF
2.17	Maximum detectable signal, OOK	Modulation depth: 99%, level measured on a NRZ ‘1’	–25	—	—	—	dBm
2.25	Maximum detectable signal, FSK	$\Delta F_{carrier}$ = ±64kHz	-10	—	—	—	dBm

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions, Comments	Limits				Unit
			Min	Typ	Max (FCE, FJE)	Max (FCAE, FJAE)	
2.18	Image frequency rejection	304–434 MHz	20	36	—	—	dB
2.19		868–915 MHz	15	20	—	—	dB

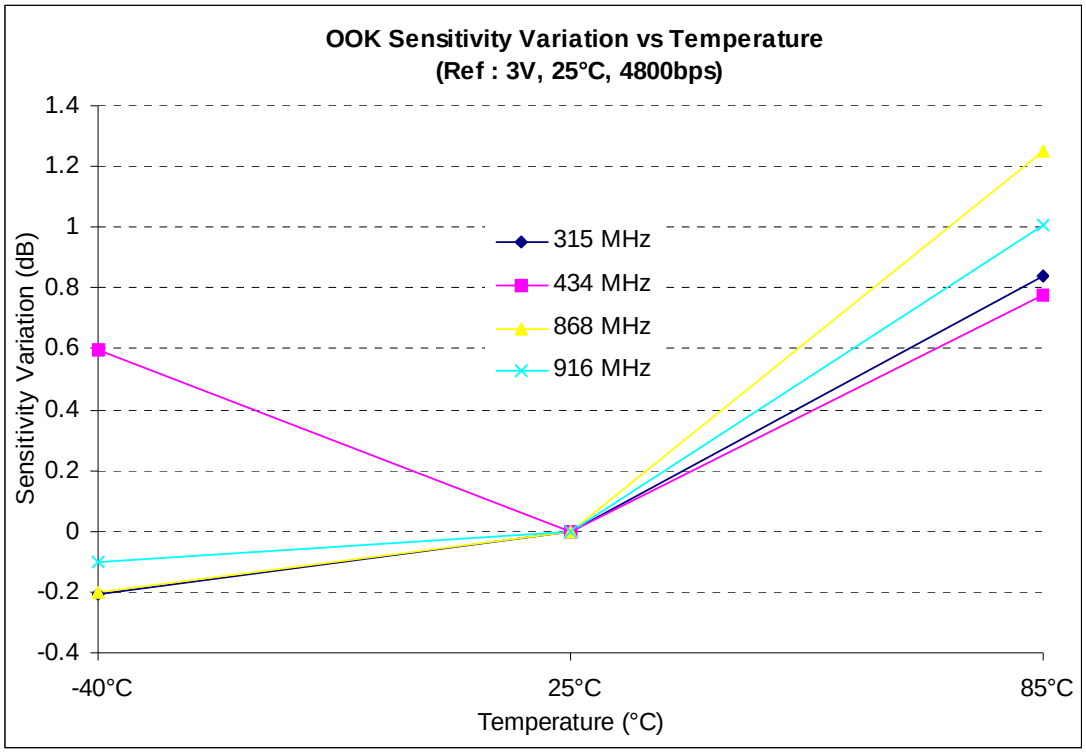


Figure 36. OOK Sensitivity Variation Versus Temperature

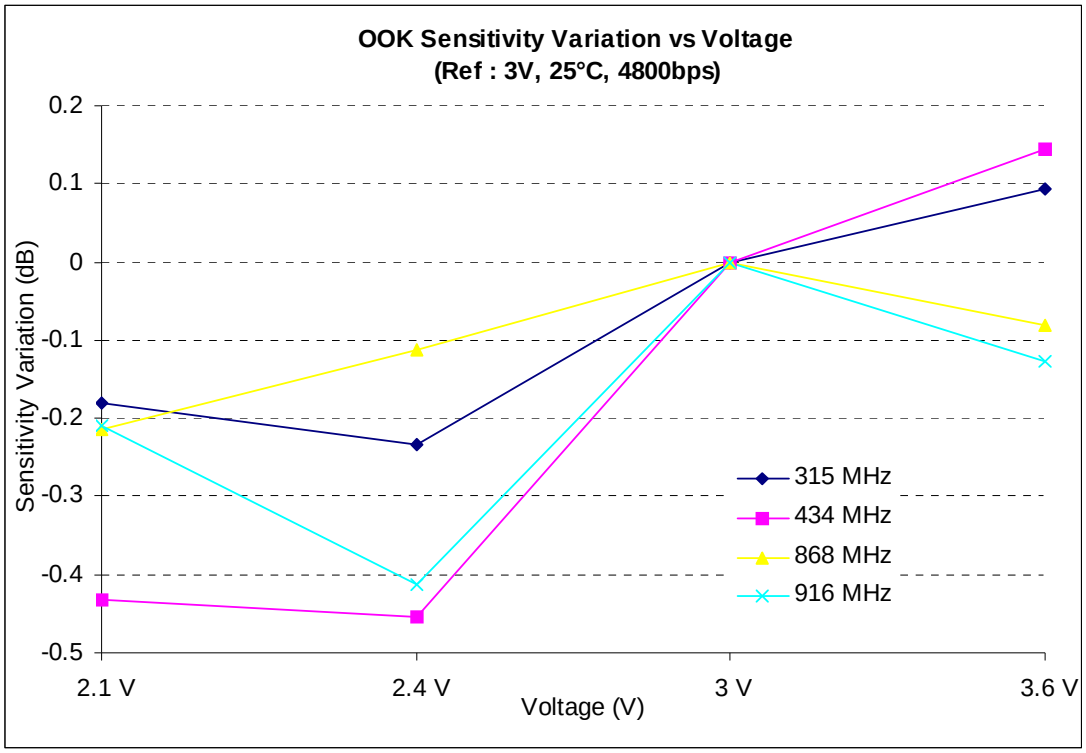


Figure 37. OOK Sensitivity Variation Versus Voltage

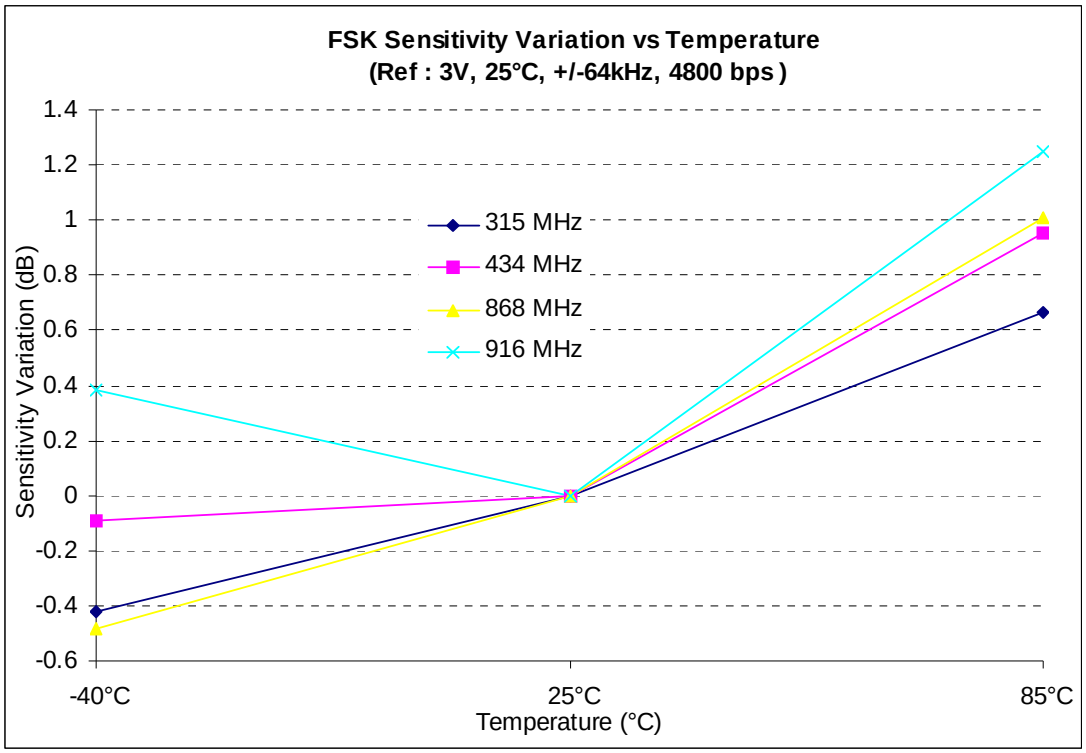


Figure 38. FSK Sensitivity Variation Versus Temperature

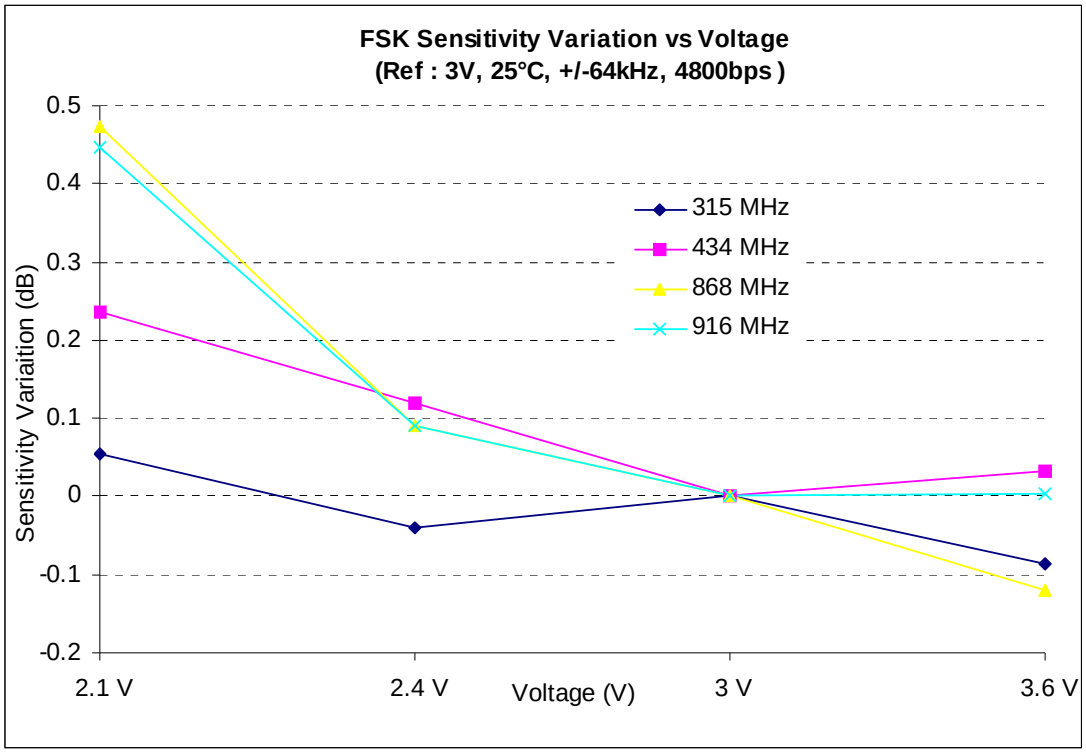


Figure 39. FSK Sensitivity Variation Versus Voltage

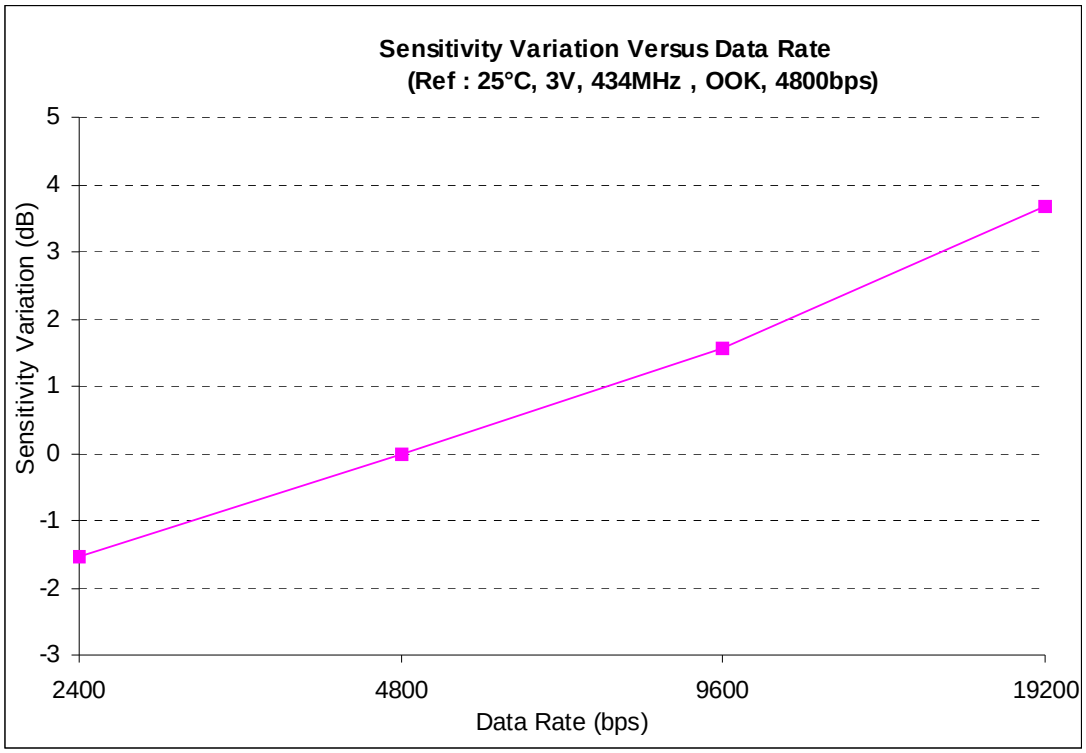


Figure 40. OOK Sensitivity Variation Versus Data Rate

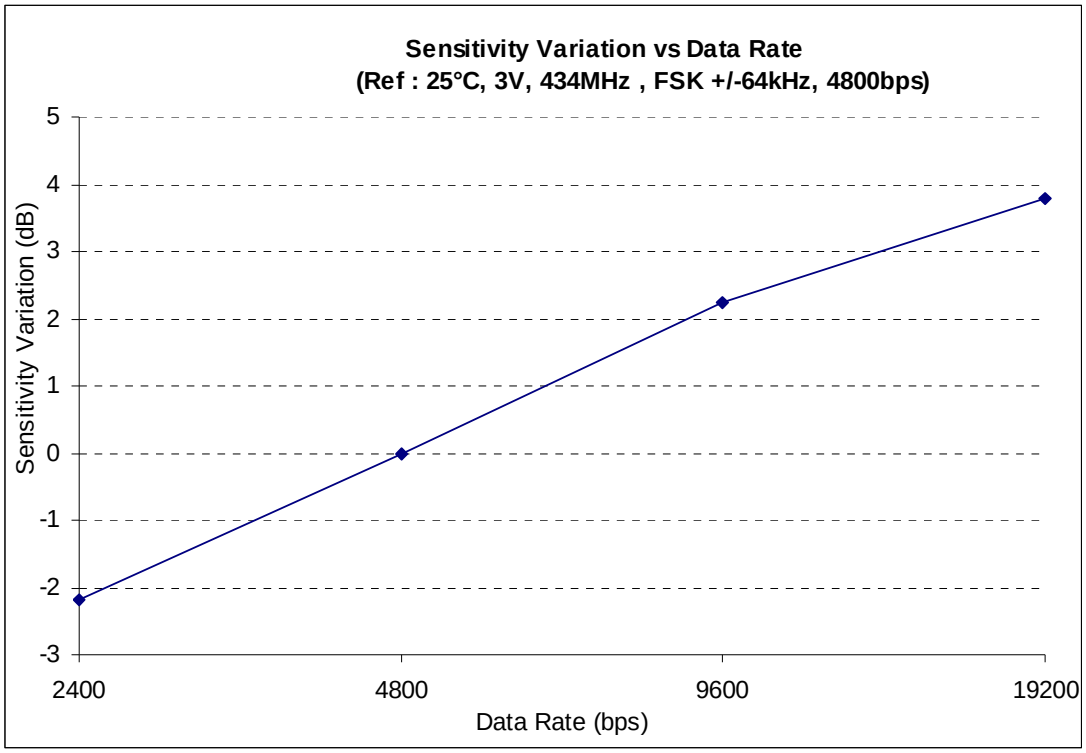


Figure 41. FSK Sensitivity Variation Versus Data Rate

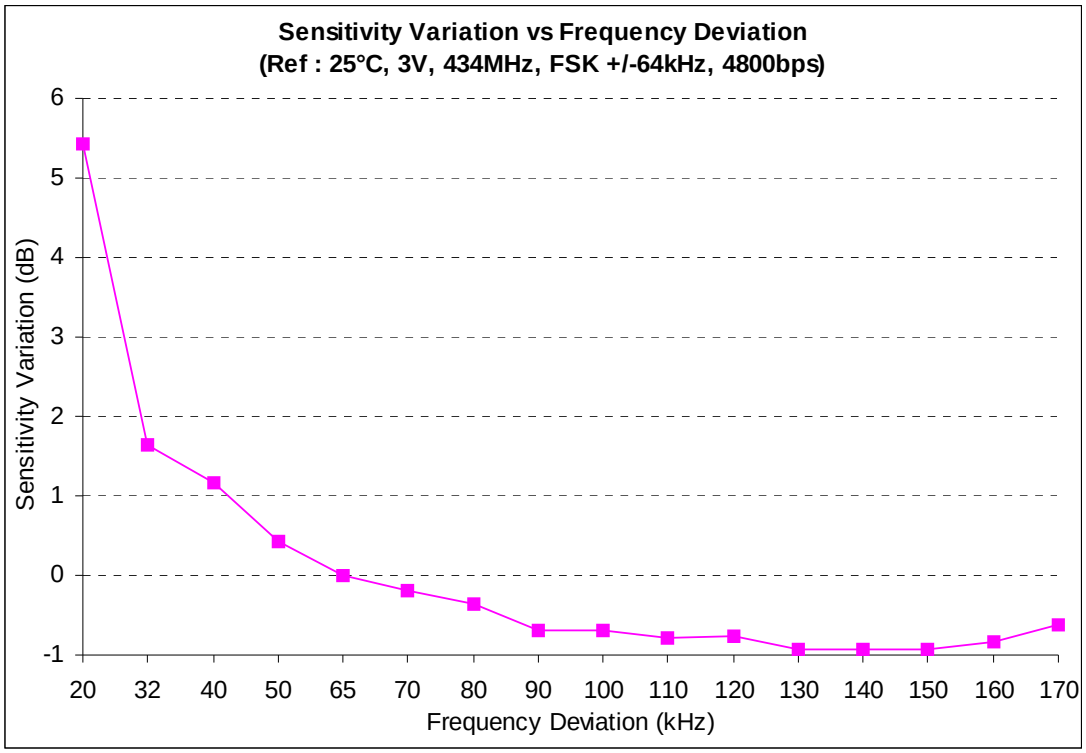


Figure 42. FSK Sensitivity Variation Versus Frequency Deviation

19.3 Receiver Parameters

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions Comments	Limits			Unit
			Min	Typ	Max	
	Receiver: IF filter, IF Amplifier, FM-to-AM Converter and Envelope Detector					
3.1	IF center frequency	Refer to Section 10, “Frequency Planning”.	—	1.5	—	MHz
3.2	IF bandwidth at –3dB		—	380	—	kHz
3.3	IF cut-off low frequency at –3 dB		—	—	1.387	MHz
3.4	IF cut-off high frequency at –3 dB		1.635	—	—	MHz
3.12	Recovery time from strong signal	OOK modulation, 2.4 kbps, FAGC = 0, input signal from –50 dBm to –100 dBm	—	15	—	ms
	Receiver: Analog and Digital RSSI					
3.51	Analog RSSI output signal for Input signal @–108 dBm	Measured on RSSIOUT	380	—	650	mV
3.52	Analog RSSI output signal for Input signal @–100 dBm		420	—	700	mV
3.53	Analog RSSI output signal for Input signal @–70 dBm		850	—	1200	mV
3.54	Analog RSSI output signal for Input signal @–28 dBm		1000	—	1300	mV
3.55	Digital RSSI Registers for Input signal @–108 dBm	RSSI [0:3]	0	—	2	
3.56	Digital RSSI Registers for Input signal @–100 dBm		0	—	3	
3.57	Digital RSSI Registers for Input signal @–70 dBm		9	—	13	
3.58	Digital RSSI Registers for Input signal @–28 dBm		13	—	16	
3.59	Digital RSSI Registers for Input signal @–70 dBm	RSSI [4:7]	0	—	2	
3.6	Digital RSSI Registers for Input signal @–50 dBm		4	—	8	
3.61	Digital RSSI Registers for Input signal @–24 dBm		13	—	15	

19.4 Transmitter: RF Parameters

RF parameters assume a matching network between test equipment and the D.U.T, and apply to all bands unless otherwise specified.

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions Comments	Limits				Unit
			Min (FCE, FJE)	Min (FCAE, FJAE)	Typ	Max	
4.1	Output power at 315 MHz	OLA[1:0] = 00, V_{CC} = 3.0 V, T_A = 25°C	4	2	7.25	11	dBm
4.16	Output power at 434 MHz	OLA[1:0] = 00, V_{CC} = 3.0 V, T_A = 25°C	3.5	1.5	6.8	10	dBm
4.2	Output power at 868 MHz	OLA[1:0] = 00, V_{CC} = 3.0 V, T_A = 25°C	2.3	0.3	5.7	10	dBm
4.25	Output power at 916 MHz	OLA[1:0] = 00, V_{CC} = 3.0 V, T_A = 25°C	—	—	5.8	—	dBm
4.20	Output power attenuation	OLA[1:0] = 00	—	—	0	—	dB
4.3		OLA[1:0] = 01	—	—	6	—	dB
4.4		OLA[1:0] = 10	—	—	12	—	dB
4.5		OLA[1:0] = 11	—	—	25	—	dB
4.10	Harmonic 2 level at 315 MHz	OLA[1:0] = 00	—	—	–33	—	dBc
4.17	Harmonic 2 level at 434 MHz	OLA[1:0] = 00	—	—	–32	—	dBc
4.11	Harmonic 2 level at 868 MHz	OLA[1:0] = 00	—	—	–50	—	dBc
4.20	Harmonic 2 level at 916 MHz	OLA[1:0] = 00	—	—	–54	—	dBc
4.12	Harmonic 3 level at 315 MHz	OLA[1:0] = 00	—	—	–41	—	dBc
4.18	Harmonic 3 level at 434 MHz	OLA[1:0] = 00	—	—	–49	—	dBc
4.13	Harmonic 3 level at 868 MHz	OLA[1:0] = 00	—	—	–53	—	dBc
4.21	Harmonic 3 level at 916 MHz	OLA[1:0] = 00	—	—	–58	—	dBc
4.30	Spurious level at 315 MHz ± F_{ref}	OLA[1:0] = 00	—	—	–54	—	dBm
4.14	Spurious level at 434 MHz ± F_{ref}	OLA[1:0] = 00	—	—	–57	—	dBm
4.15	Spurious level at 868 MHz ± F_{ref}	OLA[1:0] = 00	—	—	–56	—	dBm
4.31	Spurious level at 916 MHz ± F_{ref}	OLA[1:0] = 00	—	—	–57	—	dBm
4.6	Output rise/fall time		—	—	3	—	µs
4.7	RFOUT parallel resistance at 315 MHz	OLA[1:0] = 00, RX mode	—	—	2500	—	Ω
4.71	RFOUT parallel resistance at 434 MHz	OLA[1:0] = 00, RX mode	—	—	2100	—	Ω
4.72	RFOUT parallel resistance at 868 MHz	OLA[1:0] = 00, RX mode	—	—	1300	—	Ω
4.73	RFOUT parallel resistance at 916 MHz	OLA[1:0] = 00, RX mode	—	—	1200	—	Ω
4.8	RFOUT optimum load resistance at 315 MHz	OLA[1:0] = 00, TX mode	—	—	310	—	Ω

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions Comments	Limits				Unit
			Min (FCE, FJE)	Min (FCAE, FJAE)	Typ	Max	
4.81	RFOUT optimum load resistance at 434 MHz	OLA[1:0] = 00, TX mode	—	—	310	—	Ω
4.82	RFOUT optimum load resistance at 868 MHz	OLA[1:0] = 00, TX mode	—	—	310	—	Ω
4.83	RFOUT optimum load resistance at 916 MHz	OLA[1:0] = 00, TX mode	—	—	310	—	Ω
4.9	RFOUT parallel capacitance	Receive and transmit modes	—	—	1	—	pF

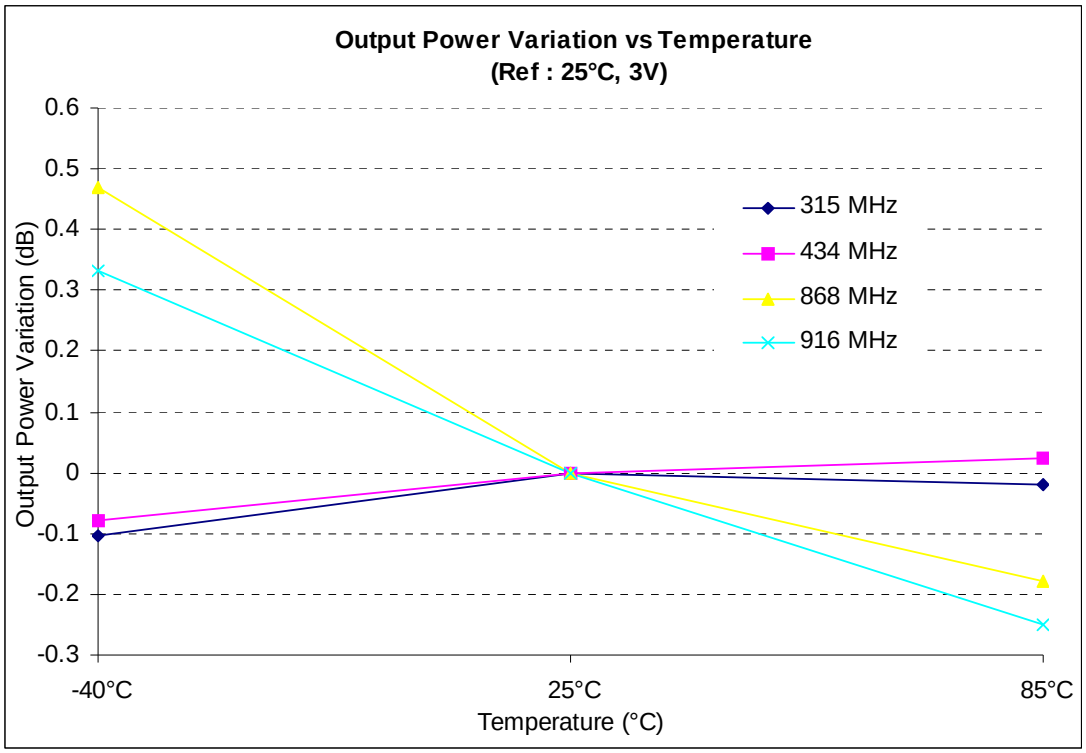


Figure 43. Output Power Versus Temperature

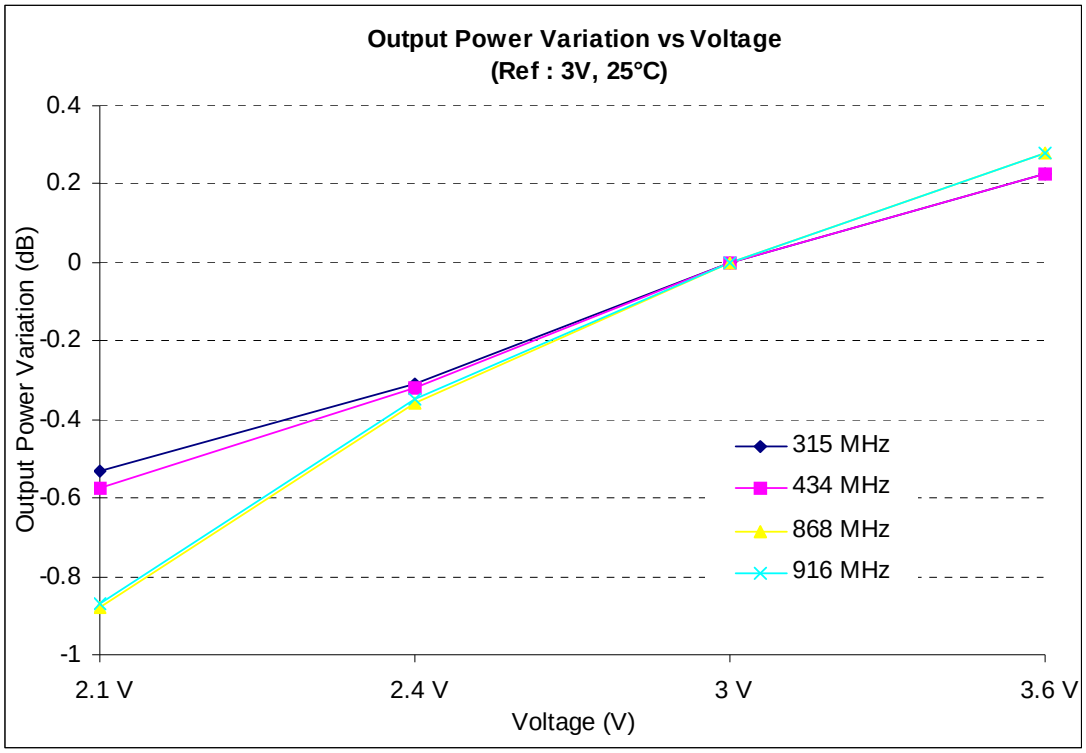


Figure 44. Output Power Versus Supply Voltage

19.5 PLL & Crystal Oscillator

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions Comments	Limits			Unit
			Min	Typ	Max	
5.9	PLL lock time	RF frequency ±25kHz	—	50	100	µs
5.1	Toggle time between 2 frequencies	RF frequency step <1.5MHz, RF frequency ±25kHz	—	30	—	µs
5.21	Occupied bandwidth @ 99%	OOK 1.2 kbps	—	58	—	kHz
5.22		OOK 19.2 kbps	—	248	—	kHz
5.23		FSK 128 kHz, 1.2 kbps	—	160	—	kHz
5.24		FSK 128 kHz, 19.2 kbps	—	278	—	kHz
5.10	Crystal oscillator startup time		—	0.6	1.2	ms
5.8	Crystal series resistance		—	—	120	Ω

19.6 Strobe Oscillator (SOE = 1)

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions Comments	Limits			Unit
			Min	Typ	Max	
6.1	Period range	$T_{Strobe} = 10^6.C3$	0.1	—	—	ms
6.2	External capacitor C3		0.1	—	10	nF
6.3	Sourced/sink current	With 1% resistor R13	—	1	—	µA
6.4	High threshold voltage		—	1	—	V
6.5	Low threshold voltage		—	0.5	—	V
6.6	Overall timing accuracy	With 1% resistor R13 & 5% capacitor C3, ±3 sigma variations	–14.2	—	15.8	%

19.7 Digital Input: CONFB, MOSI, SCLK, SEB, STROBE, RSSIC

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions Comments	Limits			Unit
			Min	Typ	Max	
7.7	Input low voltage	MOSI, SCLK, SEB, RSSIC(1)	—	—	0.4 x V_{CC2}	V
7.8	Input high voltage		0.8 x V_{CC2}	—	—	V
7.9	Input hysteresis		0.1 x V_{CC2}	—	—	V
7.10	Input low voltage	CONFB, STROBE[2]	—	—	0.4 x V_{CCDIG2}	V
7.11	Input high voltage		0.8 x V_{CCDIG2}	—	—	V
7.12	Input hysteresis		0.1 x V_{CCDIG2}	—	—	V
7.5	Sink current	Configuration, receive, transmit modes	1	—	100	nA
7.6		standby or LVD modes	0.5	—	10	nA

NOTES:
1 Input levels of those pins are referenced to V_{CC2} which depends upon V_{CC} (see Section 6, “Power Supply”).
2 Input levels of those pins are referenced to V_{CCDIG2} which depends upon the circuit state (see Section 6, “Power Supply”).

19.8 Digital Output

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions Comments	Limits			Unit
			Min	Typ	Max	
	Digital Output: DATACLK, LVD, MISO, MOSI, SCLK					
8.1	Output low voltage	$\|I_{ILOAD}\|$ = 50 µA	—	—	0.2 x V_{CCIO}	V
8.2	Output high voltage		0.8 x V_{CCIO}	—	—	V
8.3	Fall and rise time	From 10% to 90% of the output swing, C_{LOAD} = 10pF	—	80	150	ns
	Digital Output: SWITCH (V_{CC} = 3V)					
8.4	Output low voltage	$\|I_{ILOAD}\|$ = 50 µA	—	—	0.2 x V_{CC}	V
8.5	Output high voltage		0.8 x V_{CC}	—	—	V

19.9 Digital Interface Timing

Operating supply voltage and temperature range see Table 3. Values refer to the circuit recommended in the application schematic (see Figure 47), unless otherwise specified. Typical values reflect average measurement at V_{CC} = 3.0 V, T_A = 25°C.

	Parameter	Test Conditions Comments	Limits			Unit
			Min	Typ	Max	
9.2	SCLK period		1	—	—	µs
9.8	Configuration enable time		20	—	—	s
9.3	Enable lead time	If crystal oscillator is running, if not see page 15 for entering into configuration	3 x T_{digclk}	—	—	ns
9.4	Enable lag time		100	—	—	ns
9.5	Sequential transfer delay		100	—	—[1]	ns
9.6	Data hold time	Receive mode, DME = 1, from SCLK to MOSI	3 x T_{digclk}	—	—	s
9.7	Data setup time	Configuration mode, from SCLK to MISO	—	—	100	ns
9.9		Configuration mode, from SCLK to MOSI	120	—	—	ns
9.10	Data setup time	Configuration mode, from SCLK to MOSI	100	—	—	ns

NOTES:
1 The digital interface can be used in SPI burst protocol, i.e., with a continuous clock on SCLK port. For example, one (or more) read access followed by one (or more) write access and so on. In this case and for a practical use, the pulse required on CONFB between accesses must be less than one digital clock period T_{digclk}.

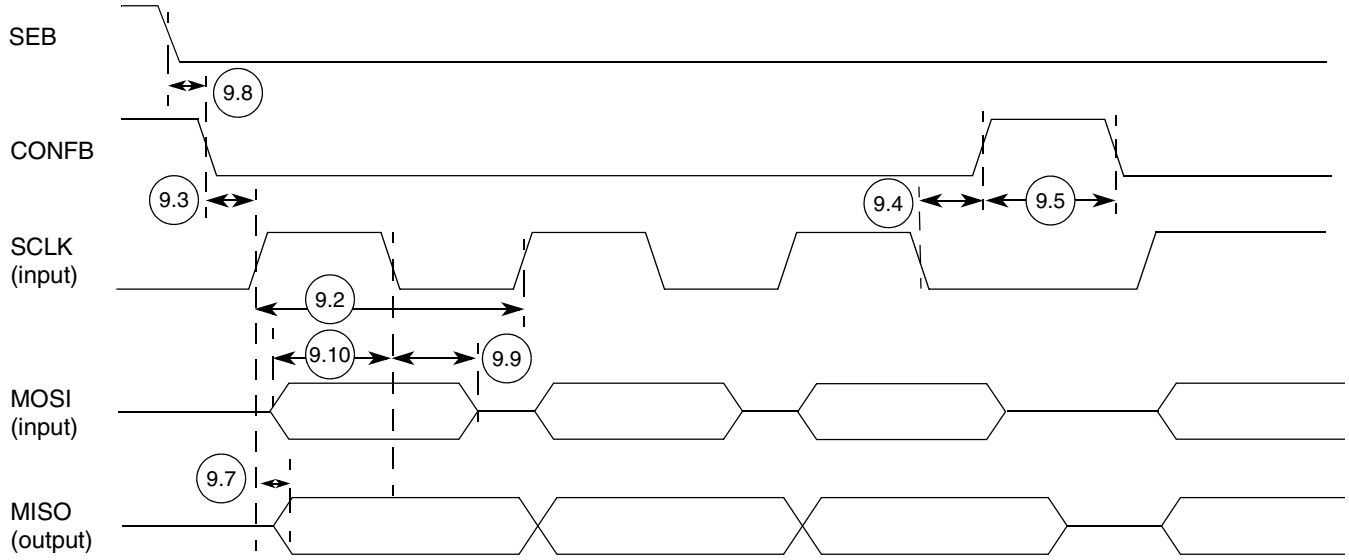


Figure 45. Digital Interface Timing Diagram in Configuration Mode

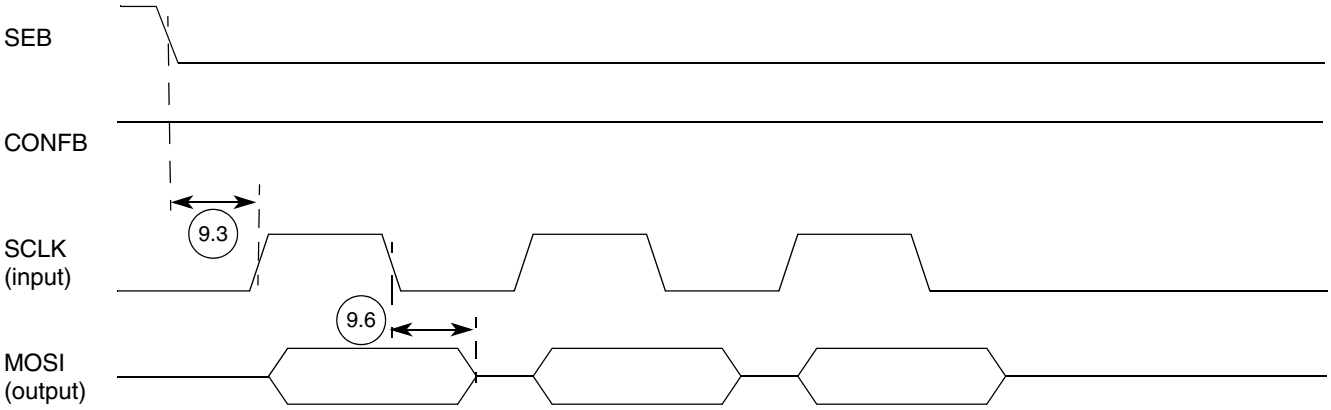


Figure 46. Digital Interface Timing Diagram in Receive Mode (DME = 1)

Examples of crystal characteristics are given in Table 25.

Table 25. Typical Crystal Reference and Characteristics

Parameter	Reference & Type			Unit
	315 MHz	434 MHz	868 MHz	
	LN-G102-1183 NX5032GA	LN-G102-1182 NX5032GA	EXS00A-01654 NX5032GA	
Frequency	17.5814	24.19066	24.16139	MHz
Load capacitance	8	8	8	pF
ESR	25	15	<70	Ω

20 Application Schematics

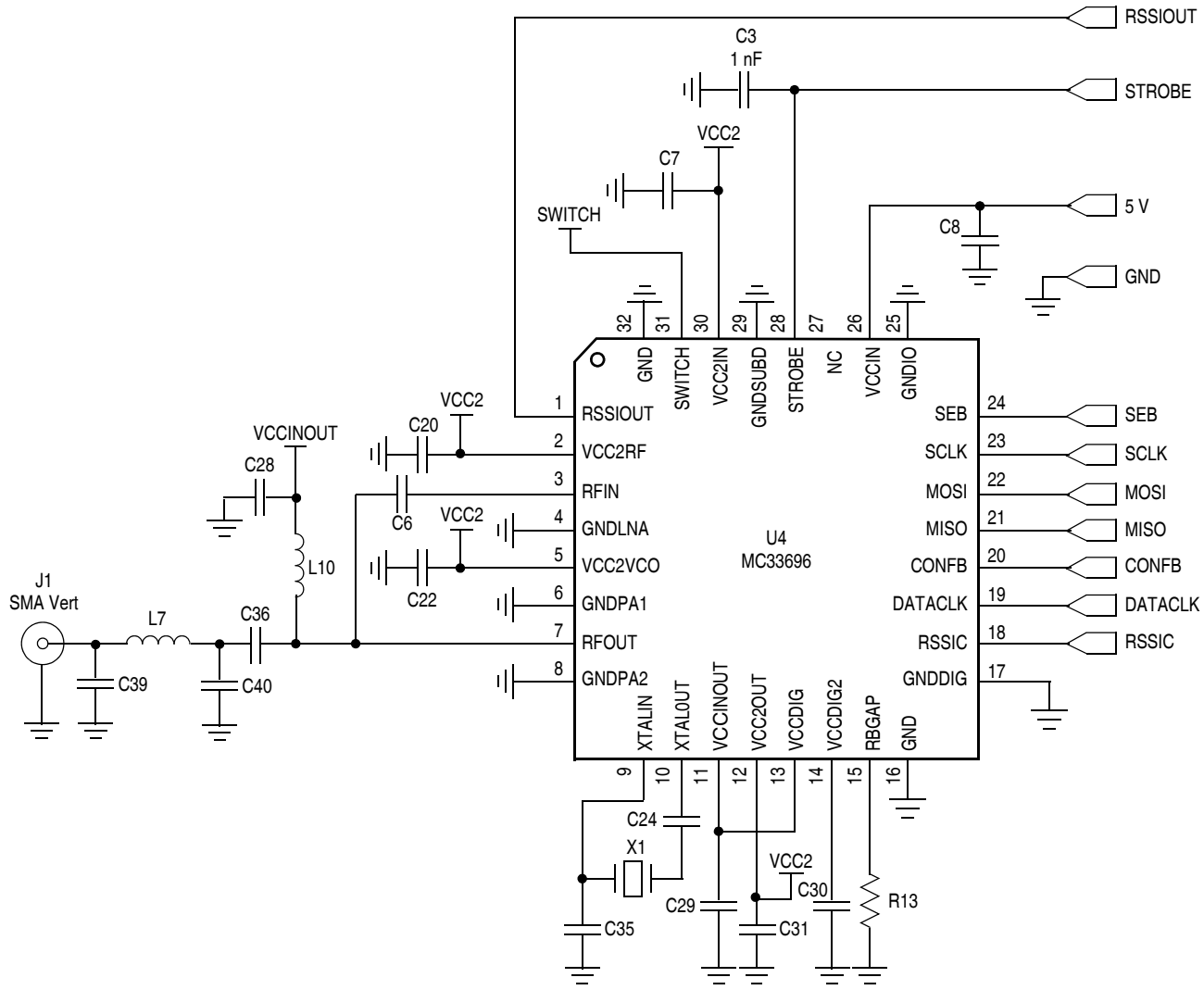


Figure 47. MC33696 Application Schematic (5 V)

20.1 PCB Design Recommendations

Pay attention to the following points and recommendations when designing the layout of the PCB.

- **Ground Plane**
  - — If you can afford a multilayer PCB, use an internal layer for the ground plane, route power supply and digital signals on the last layer, RF components being located on the first layer.
  - — Use at least a double-sided PCB.
  - — Use a large ground plane on the opposite layer.
  - — If the ground plane must be cut on the opposite layer for routing some signals, maintain continuity with another ground plane on the opposite layer and a lot of via to minimize

parasitic inductance.

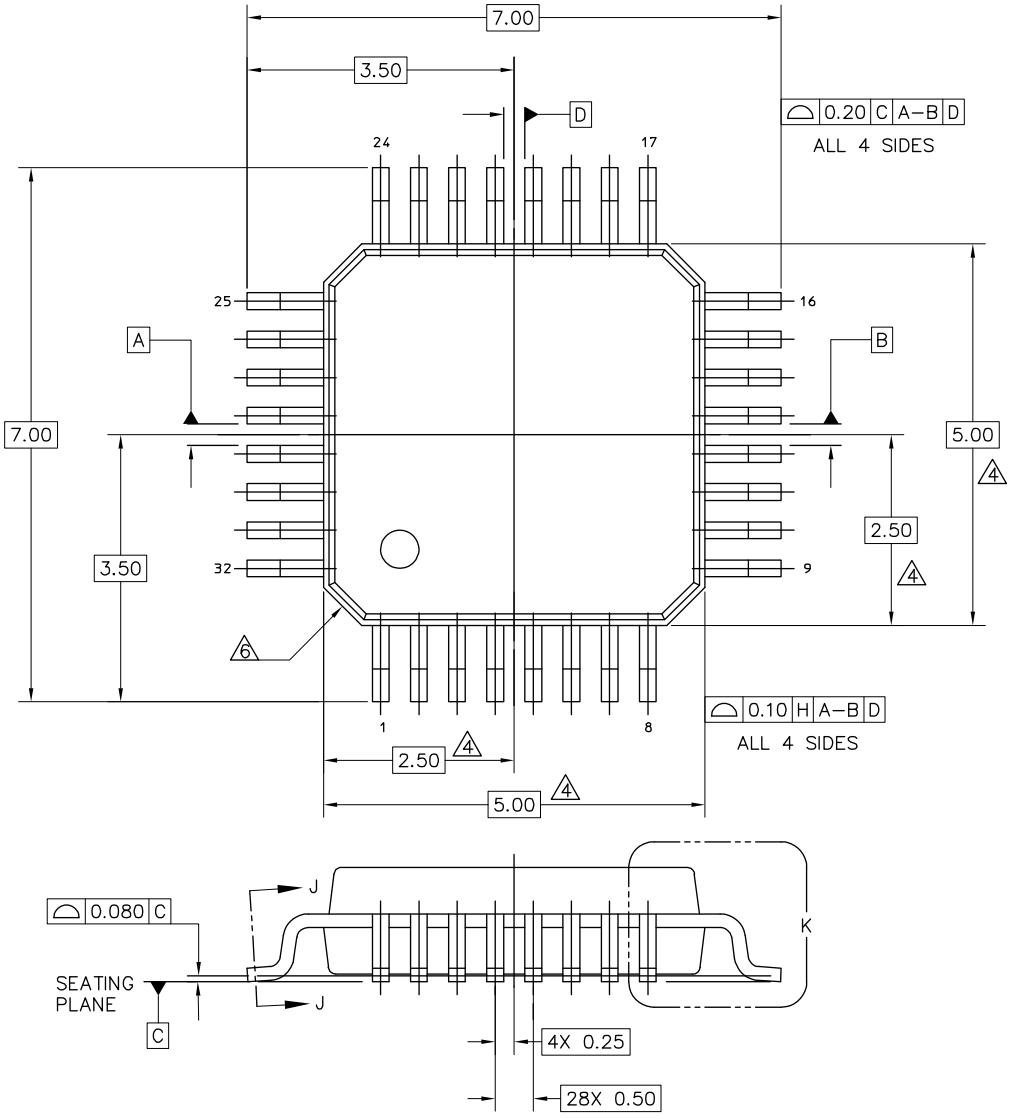
- **Power Supply, Ground Connection and Decoupling**
  - — Connect each ground pin to the ground plane using a separate via for each signal; do not use common vias.
  - — Place each decoupling capacitor as close to the corresponding VCC pin as possible (no more than 2–3 mm away).
  - — Locate the VCCDIG2 decoupling capacitor (C13) directly between VCCDIG2 (pin 14) and GND (pin 16).
  - — GNDPA1 and GNDPA2 inductance to ground should be minimum. If possible, use two via for each pin.
- **RF Tracks, Matching Network and Other Components**
  - — Minimize any tracks used for routing RF signals.
  - — Locate crystal X1 and associated capacitors C15 and C11 close to the MC33696. Avoid loops occurring due to component size and tracks. Avoid routing digital signals in this area.
  - — Use high frequency coils with high Q values for the frequency of operation (minimum of 15). Validate any change of coil source.
  - — Track between RFOUT and RFIN should be as short as possible to minimize lost in TX mode.

NOTE

The values indicated for the matching network have been computed and tuned for the the MC33696 RF Modules available for MC33696 evaluation. Matching networks should be retuned if any change is made to the PCB (track width, length or place, or PCB thickness, or component value). Never use, as is, a matching network designed for another PCB.

21 Case Outline Dimensions

21.1 LQFP32 Case



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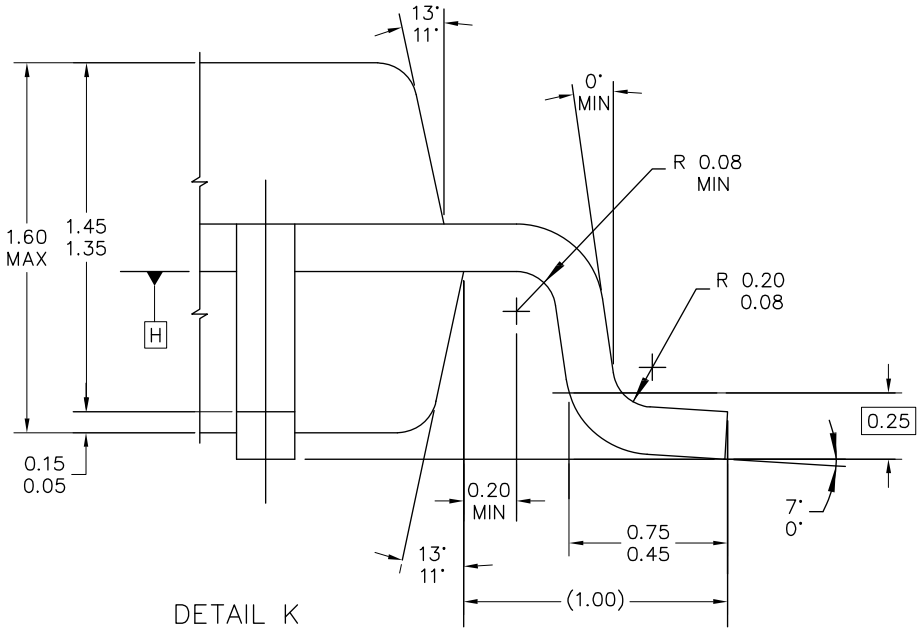
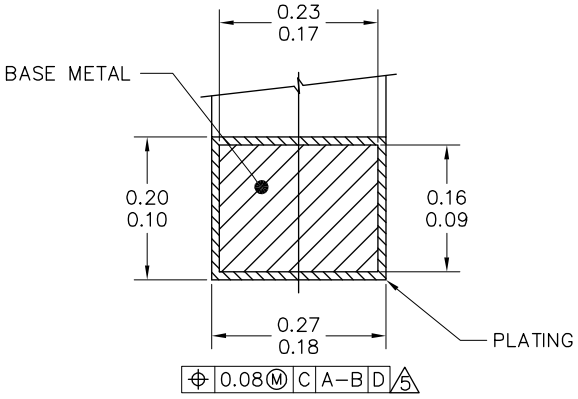
TITLE: LQFP, 32–LEAD, 5 X 5 X 1.4 PKG	DOCUMENT NO: 98ASH70471A	REV: C
	CASE NUMBER: 873C–01	02 JUN 2005
	STANDARD: JEDEC MS–026–BAA EIAJ ED–7404A	



DETAIL K



SECTION J–J

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TITLE: LQFP, 32–LEAD, 5 X 5 X 1.4 PKG	DOCUMENT NO: 98ASH70471A	REV: C
	CASE NUMBER: 873C–01	02 JUN 2005
	STANDARD: JEDEC MS–026–BAA EIAJ ED–7404A	

NOTES:

1. DIMENSION ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS A, B AND D TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.

4. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

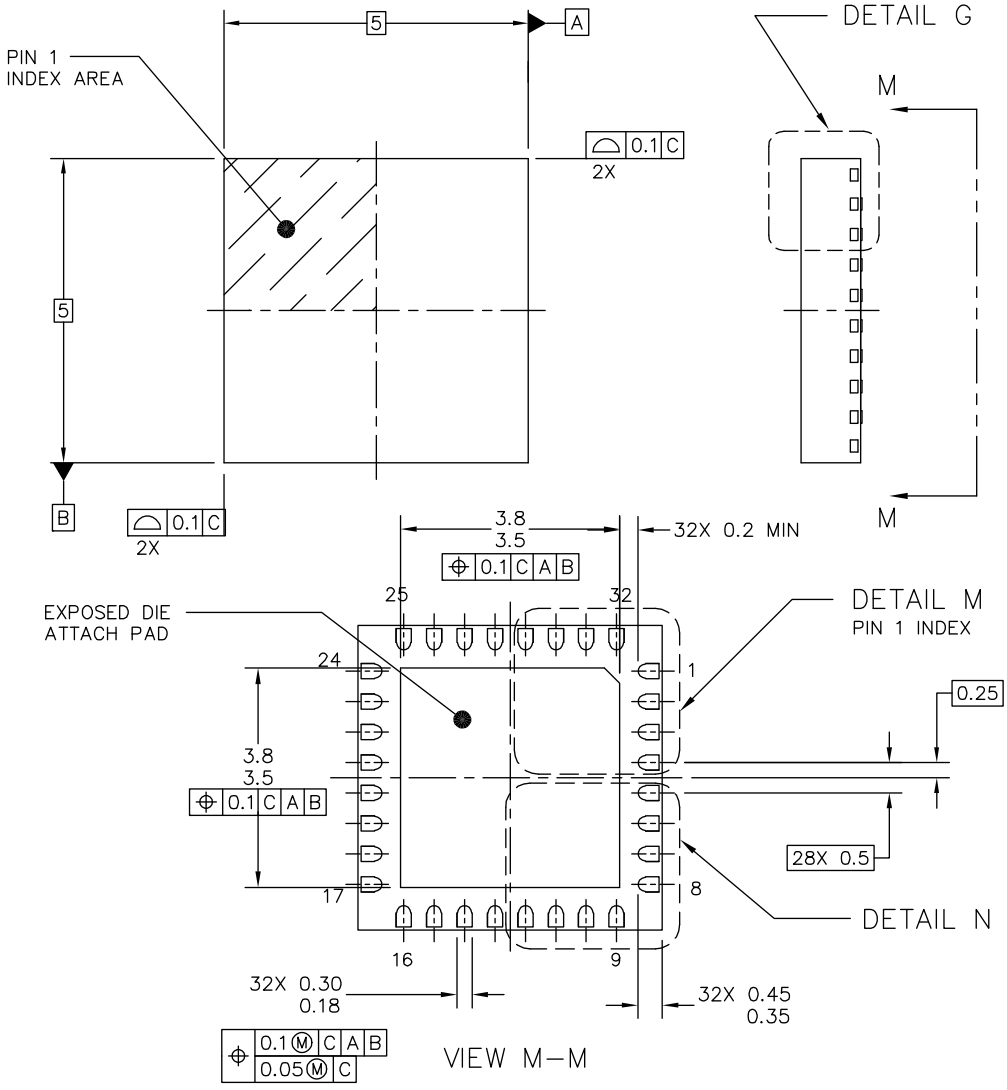
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07 MM.

6. EXACT SHAPE OF CORNERS MAY VARY.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70471A	REV: C
LQFP, 32–LEAD, 5 X 5 X 1.4 PKG	CASE NUMBER: 873C–01	02 JUN 2005
	STANDARD: JEDEC MS–026–BAA EIAJ ED–7404A	

21.2 QFN32 Case



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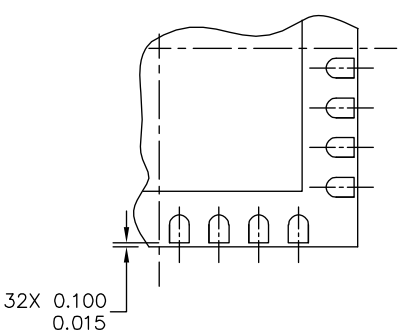
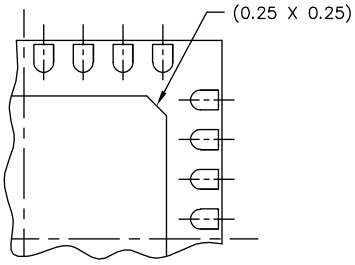
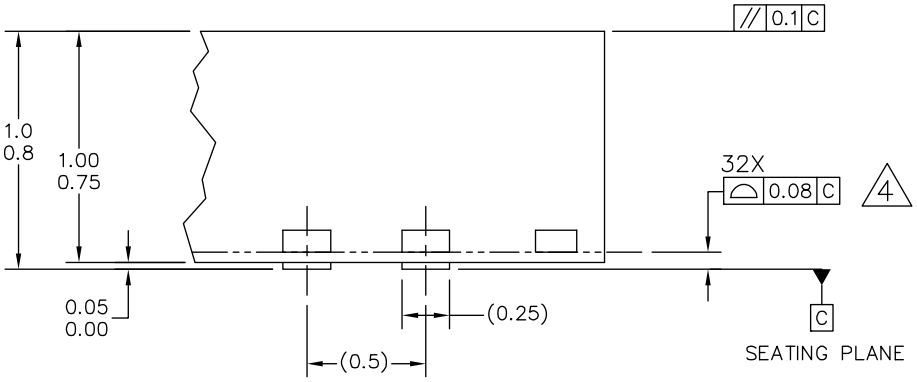
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 32 TERMINAL, 0.5 PITCH (5 X 5 X 1) 3.6 X 3.6 EP, CASE OUTLINE	DOCUMENT NO: 98ARE10566D	REV: C
	CASE NUMBER: 1582–02	26 FEB 2007
	STANDARD: JEDEC MO–220 VHHD–4	



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL M
PREFERRED BACKSIDE PIN 1 INDEX



DETAIL G
VIEW ROTATED 90° CW

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TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 32 TERMINAL, 0.5 PITCH (5 X 5 X 1) 3.6 X 3.6 EP, CASE OUTLINE	DOCUMENT NO: 98ARE10566D	REV: C
	CASE NUMBER: 1582-02	26 FEB 2007
	STANDARD: JEDEC MO-220 VHHD-4	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, AND DIE ATTACH PAD.
5. MINIMUM METAL GAP SHOULD BE 0.2 MM.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 32 TERMINAL, 0.5 PITCH (5 X 5 X 1) 3.6 X 3.6 EP, CASE OUTLINE	DOCUMENT NO: 98ARE10566D	REV: C
	CASE NUMBER: 1582–02	26 FEB 2007
	STANDARD: JEDEC MO–220 VHHD–4	

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