Si53xx Any-Rate Precision Clocks

March 2007

Introducing Si53xx Any-Rate Precision Clocks

- **New family of 9 highly integrated, ultra low jitter clock multiplier ICs**
- **DSPLL based architecture enables any-rate frequency synthesis**
- **Improves performance and simplifies design**

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Precision Timing Market

Market Segment	Application	Example Frequencies (MHz)
Telecom	SONET/SDH	155.52, 622.08
Datacom	Ethernet	156.25, 644.53
Storage Area Networks	Fibre Channel	106.25, 212.50
Wireless Basestations	CDMA, GSM, WiMAX	78.64, 491.52
Data Acquisition	Data converter sampling clock	80, 124.41
Video	HDTV broadcast video	74.17, 74.25
Test & Measurement	Bench equipment	125, 533
Military	Communications Displays	27, 129.29

- **Diverse market requiring a broad range of frequencies and excellent jitter performance**

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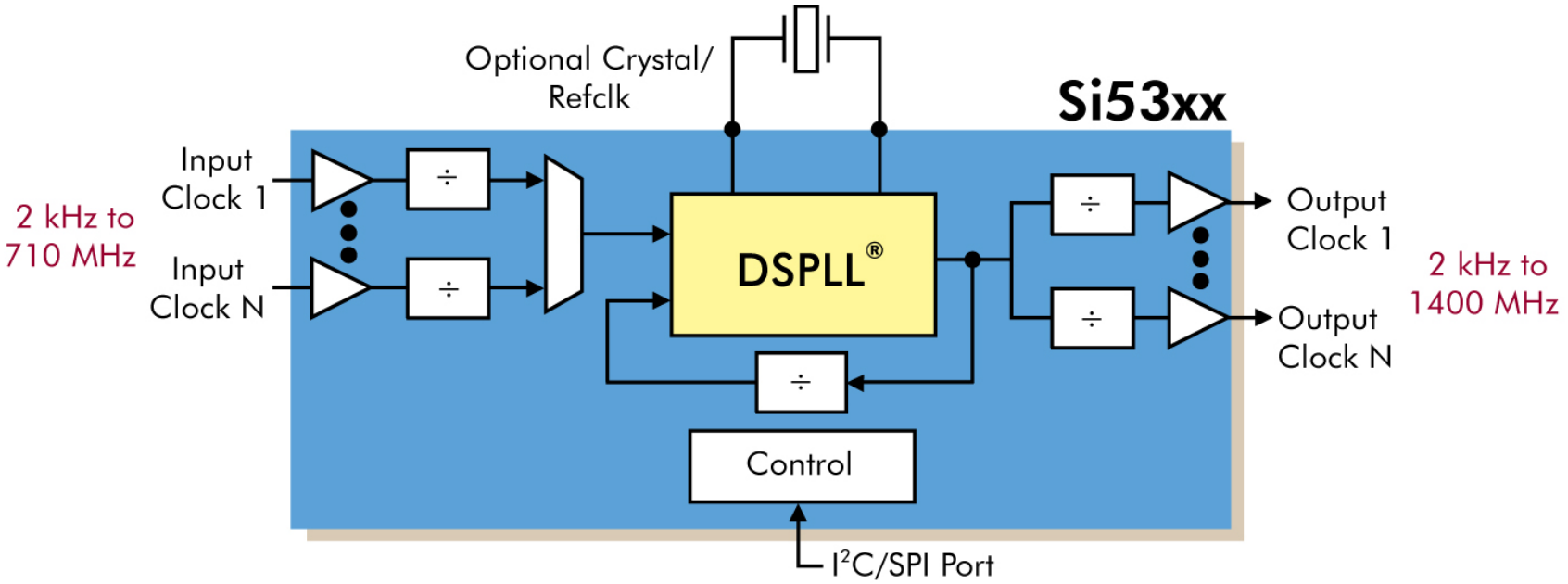
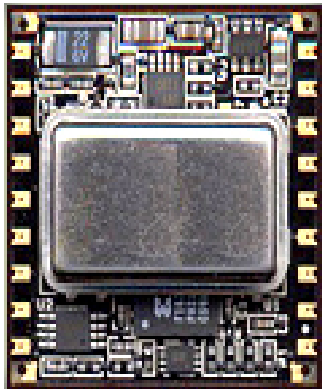
Key Feature—Any-Rate Frequency Synthesis



- **DSPLL enables any-rate operation over a wide frequency range**
- **No external component changes required**
- **Frequency flexibility reduces BOM and enables design reuse**

Silicon Labs Si53xx versus Discrete Solutions



Si53xx Any-Rate Precision Clocks | **Traditional VCXO/VCSO-Based PLLs**

Fully integrated IC replaces VCXO/VCSO PLLs	PLL implemented with discrete VCXO or VCSOs
Same device can be re-used for all frequencies of operation	New PLL design and components required for each frequency of operation
Reconfigurable for multi-rate applications	Multi-rate applications require multiple VCXOs
PLL designed and integrated in IC	Requires analog PLL design expertise
Short, consistent lead times: 4-6 weeks	Long, unpredictable lead times: 8-14 weeks

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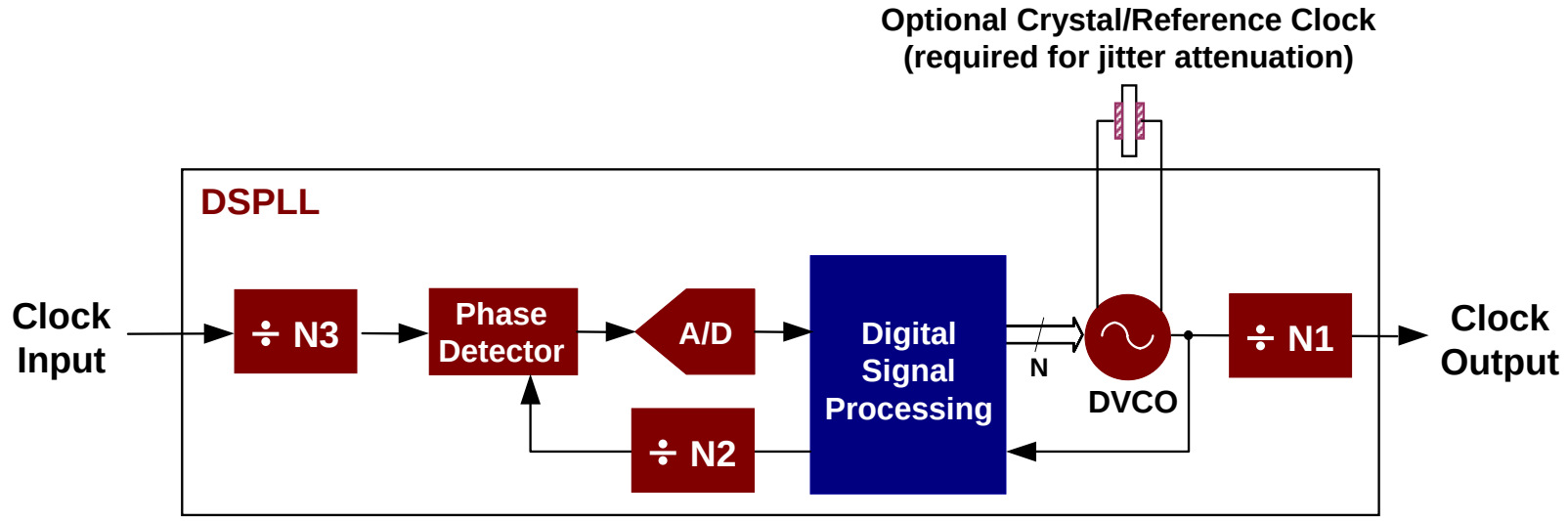
The DSPLL Advantage



- **Patented DSPLL architecture provides frequency agility**
  - Eliminates need for discrete VCXO/VCSOs
- **Ultra-low jitter generation (0.3 ps rms: 12 kHz to 20 MHz)**
- **Integrated loop filter minimizes PLL sensitivity to board-level noise**
- **High integration simplifies PLL design and layout**
- **User-selectable loop bandwidth enables jitter performance optimization**

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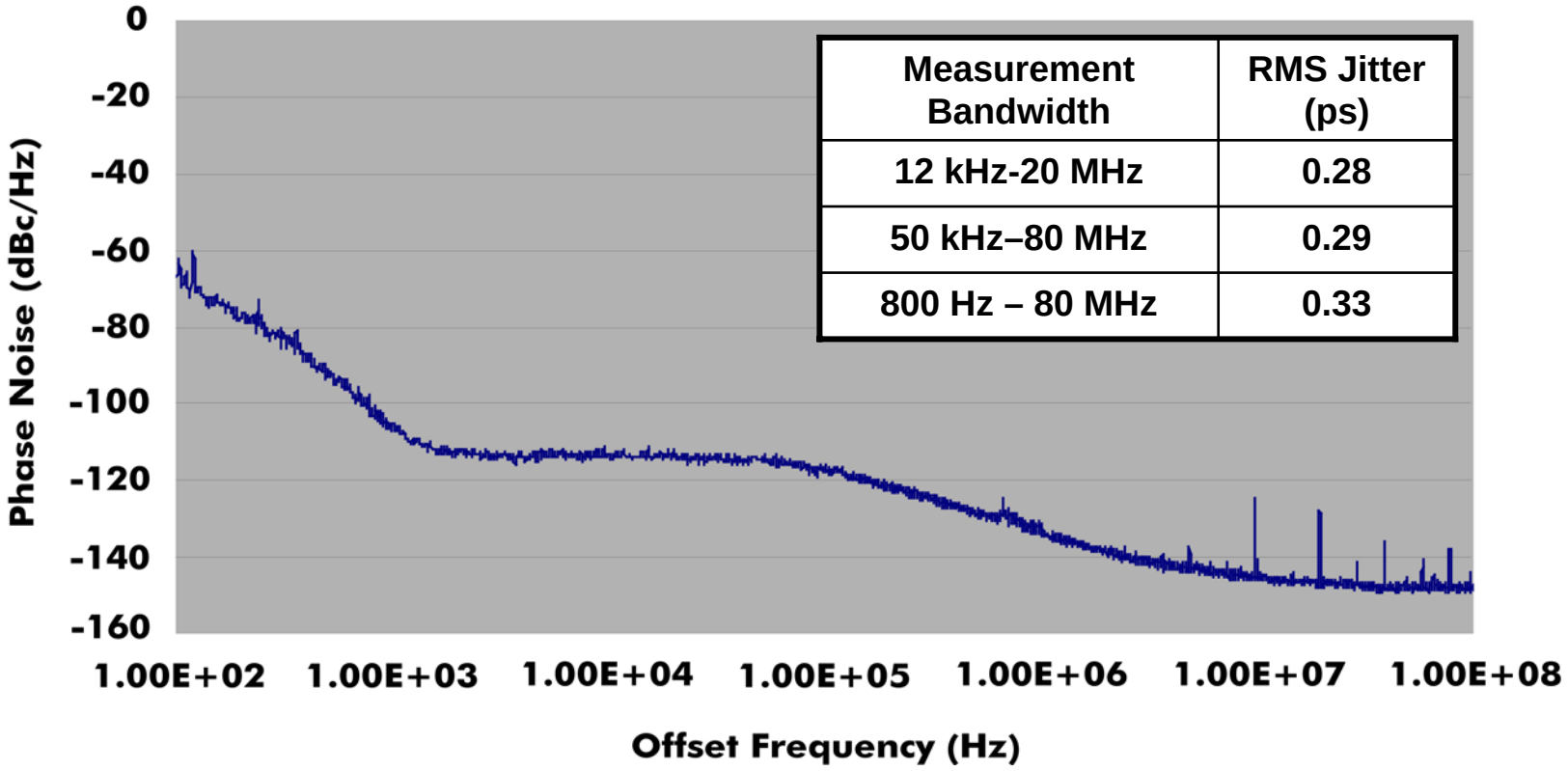
Si53xx—Ultra Low Jitter/Phase Noise



Measurement Bandwidth	RMS Jitter (ps)
12 kHz-20 MHz	0.28
50 kHz–80 MHz	0.29
800 Hz – 80 MHz	0.33

- **Si53xx performance comparable to best-in-class VCXO/VCSO PLLs**

Configuration: CLKIN = 155.52 MHz, CLKOUT = 622.08 MHz, 800 Hz Loop Bandwidth

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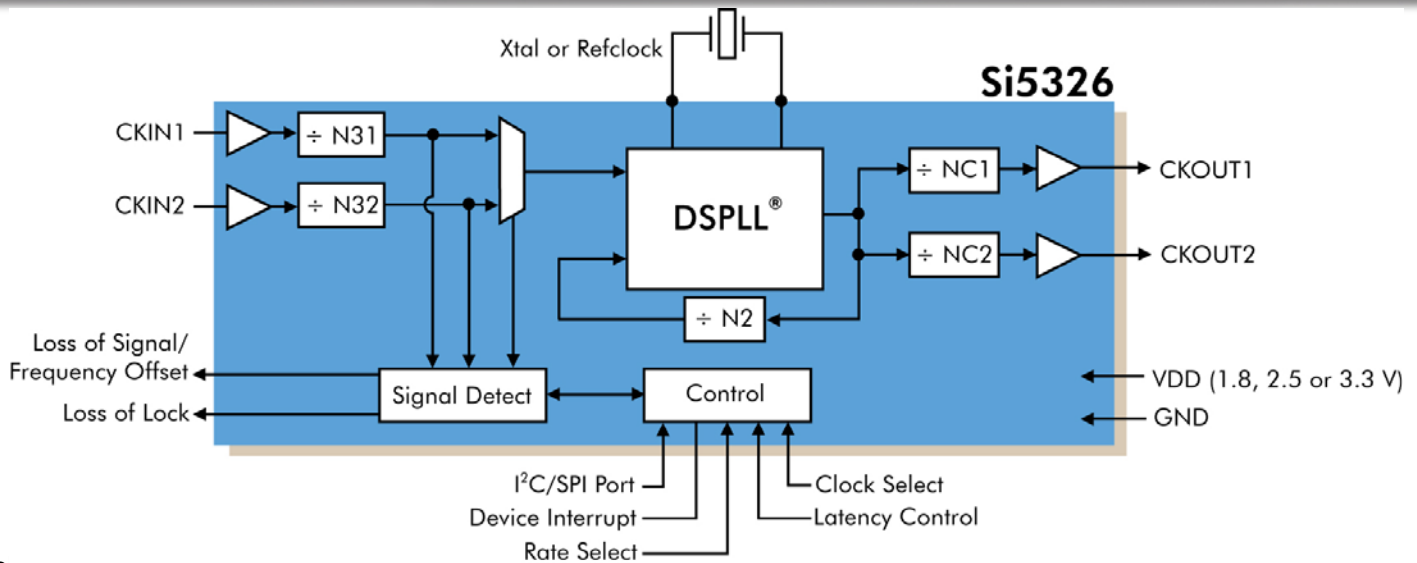
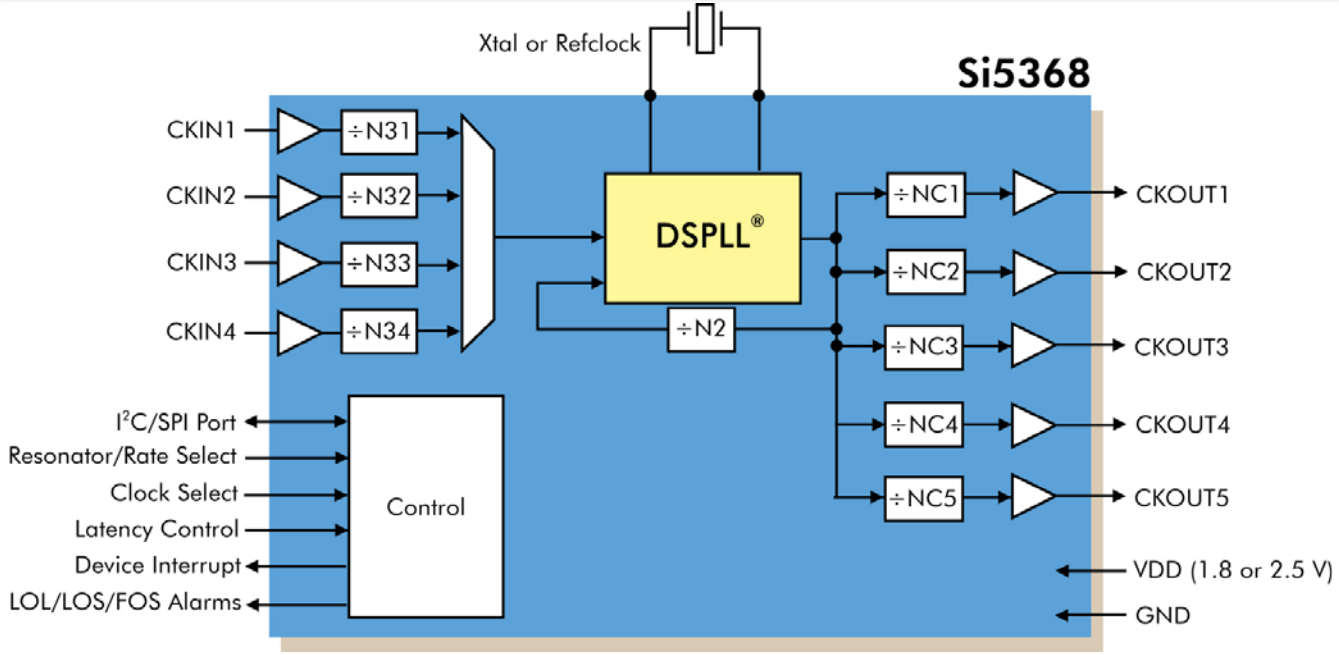
Si532x Any-Rate Precision Clocks



- Two clock inputs/two clock outputs
- Input frequency range: 2 kHz to 710 MHz
- Output frequency range: 2 kHz to 945 MHz, select frequencies to 1.4 GHz
- Output clocks related by ratio of output divider settings (CKOUT2 = (NC1/NC2) * CKOUT1)
- Ultra low jitter: 0.3 ps_{rms} (12 kHz to 20 MHz)
- Automatic (revertive, non-revertive) or manual clock selection with hitless switching
- Programmable output clock signal format: LVPECL, LVDS, CML or CMOS
- Programmable loop bandwidth for jitter attenuation: 60 Hz to 8.4 kHz
- Supply: 1.8 V, 2.5 V, or 3.3 V
- 6x6 mm 36-QFN, Pb-free

	Function		Control	
Part #	**Jitter Attenuation**	**Clock Multiplication**	**µP I²C/SPI**	**Pin**
Si5326	✓	✓	✓	
Si5323	✓	✓		✓
Si5316	✓			✓
Si5325		✓	✓	
Si5322		✓		✓

Si536x Any-Rate Precision Clocks



- Same base features as Si532x PLUS:
  - Four clock inputs
  - Five clock outputs
- Supply: 1.8 or 2.5 V
- 14x14 mm 100-TQFP, Pb-free

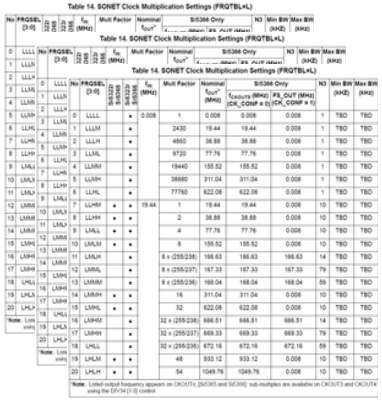
	Function		Control	
Part #	**Jitter Attenuation**	**Clock Multiplication**	**µP I²C/SPI**	**Pin**
Si5368	✓	✓	✓	
Si5366	✓	✓		✓
Si5367		✓	✓	
Si5365		✓		✓

Key Feature—Frequency Flexibility

- **Si5325/26/65/68 µP-controlled precision clocks provide any-rate frequency synthesis**
  - Easily supports custom frequencies
  - Reconfigurable to support multi-rate applications
  - Three speed grades available

Speed Grade	Max Output Frequency
A	1417 MHz
B	808 MHz
C	346 MHz

- **Si5322/23/66/68 pin-controlled precision clocks provide ease of use**
  - 275 popular SONET, Ethernet, Fibre Channel and HDTV frequency translations available via lookup tables
  - Includes support for SONET-to-datacomm frequency translations
  - Provides upgrade path for existing Si5320/21/64 customers



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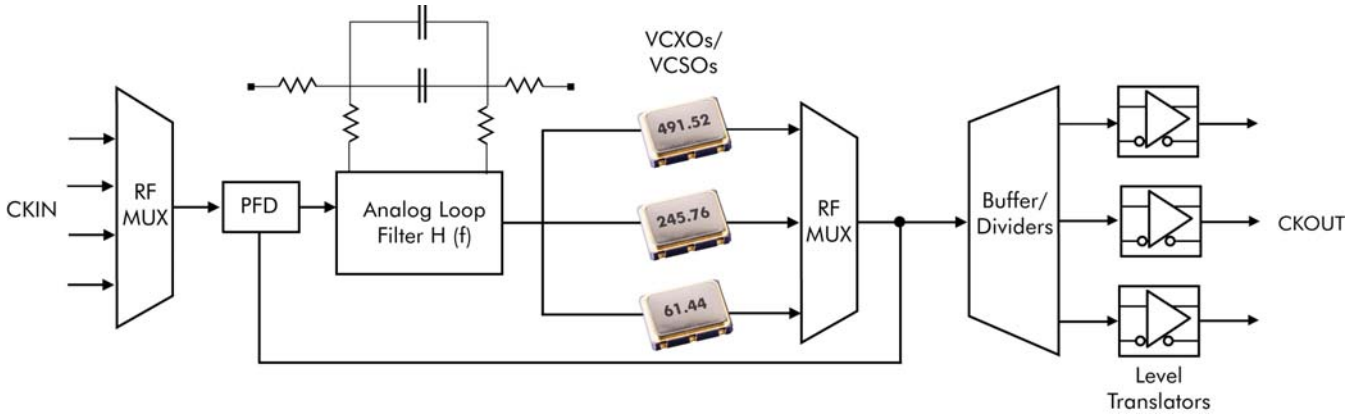
Key Feature—Integration

Single IC

Replaces

Complex Discrete PLL



- **Traditional PLL designs require many discrete components**
  - Multiple VCXO/VCSOs required for multi-frequency applications
  - RF muxes, phase frequency detector, analog loop filter, low jitter buffers, etc.
- **Si53xx provides highly integrated solution**
  - Simplifies PLL design and layout
  - Improves noise immunity since all loop components are integrated

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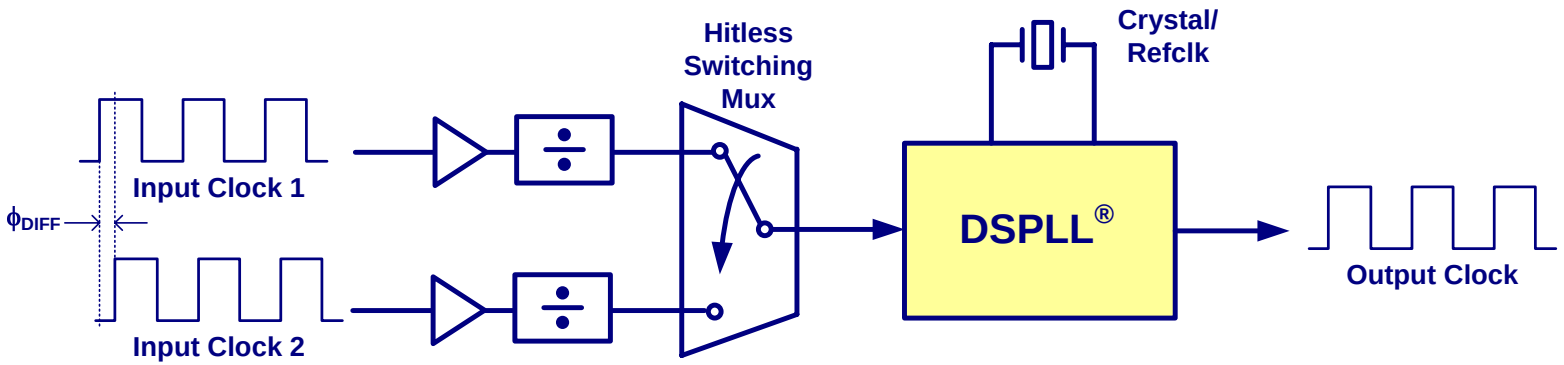
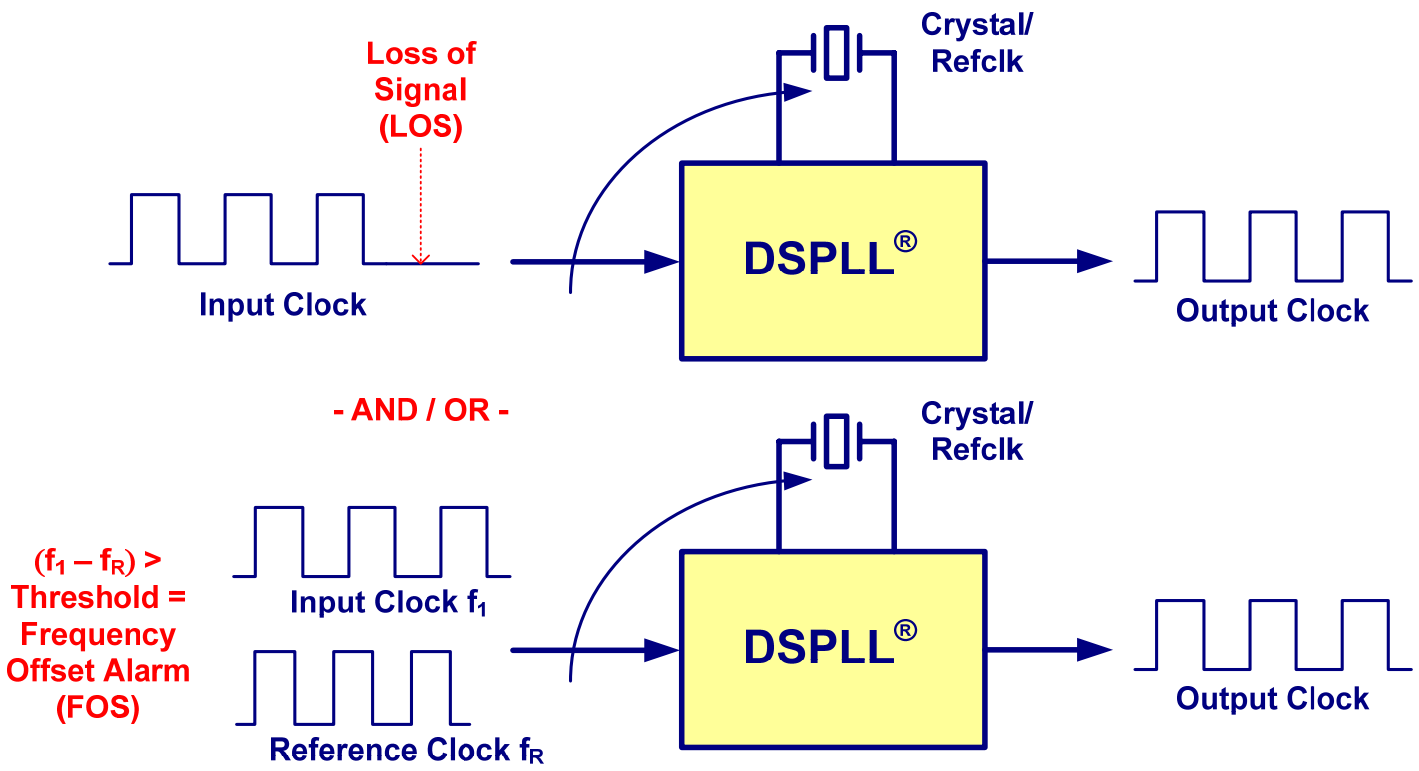
Key Feature—Hitless Switching



- **Absorbs phase difference between input clocks during switchover**
  - Guarantees system BER in mission-critical telecom applications
  - Meets SONET Stratum 3/3E phase transient requirements (MTIE)
- **Simplifies clock switching in applications requiring multiple input clocks**
  - Automatic (revertive, non-revertive) and manual control options available
- **Supports switching between clocks at different frequencies**

Key Feature—Digital Hold



- **Provides stable output clock in the absence of a valid input clock**
  - Entry to digital hold triggered by input clock alarm (LOS, FOS)
- **Meets stringent telecom specifications for initial frequency accuracy**
  - Stratum 3E: 1 ppb
- **Tracks crystal/reference clock's drift and temperature stability**

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Si53xx Features and Benefits Summary

Key Feature	Customer Benefits
Any-rate frequency synthesis	Replaces VCXO/VCSO-based PLL with IC solution Reconfigurable to support multi-frequency operation Simplifies design reuse
Low jitter (0.3 ps rms typ)	Great fit for high-performance applications Additional design margin for less jitter-sensitive apps
Integrated VCO and loop filter	Simplifies design/layout Adjustable jitter attenuation Superior PSRR to discrete PLLs Low phase noise in real-world applications
Multiple inputs with hitless switching	Simplifies design/layout Comprehensive alarm monitoring Meets telecom phase transient (MTIE) requirements
Multiple frequency flexible outputs	Simplifies design/layout Eliminates buffers, level translators
IC-based solution	Short lead times: 4-6 weeks

Silicon Labs Any-Rate Precision Clocks

Device	No. Clock Inputs	No. Clock Outputs	Control	Input Freq. (MHz)	Output Freq. (MHz)	Jitter Gen (50 kHz-80 MHz)	Loop BW	Clock Mult.	Hitless Switching	Alarms			Pkg.
										LOL	LOS	FOS	
Any-Rate Precision Clock Multipliers													
Si5322[1]	2	2	Pin	15 to 707	19 to 1050	0.6 ps rms typ	30 kHz to 1.3 MHz	Y	N		●		6x6 mm 36-QFN
Si5325			I^2C or SPI	10 to 710	10 to 1400						●	●	
Si5365[1]	4	5	Pin	15 to 707	19 to 1050						●	●	14x14 mm 100-TQFP
Si5367			I^2C or SPI	10 to 710	10 to 1400						●	●	
Any-Rate Precision Clock Multipliers with Jitter Attenuation													
Si5316[1,2]	2	1	Pin	19 to 710	19 to 710	0.3 ps rms typ	60 Hz to 8.4 kHz	N	N	●	●		6x6 mm 36-QFN
Si5323[1,2]		2		0.008 to 707	0.008 to 1050			Y	Y	●	●		
Si5326[2]			I^2C or SPI	0.002 to 710	0.002 to 1400					●	●	●	
Si5366[1,2]	4	5	Pin	0.008 to 707	0.008 to 1050					●	●	●	14x14 mm 100-TQFP
Si5368[2]			I^2C or SPI	0.002 to 710	0.002 to 1400					●	●	●	

Note 1: Frequency plan pin-selectable from lookup table

Note 2: Requires external low-cost, fixed frequency crystal or 38.88 MHz reference clock

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Silicon Labs Precision Timing Products

- **Industry's broadest portfolio of frequency flexible, low jitter timing solutions**

Any-Rate Precision Clocks

Si5368
Si5367
Si5366
Si5365

Si5326
Si5325
Si5323
Si5322
Si5316

Dual/Quad Frequency XO/VCXOs

Quad VCXO

Dual VCXO

Quad XO

Dual XO

Single Frequency XO/VCXOs

VCXO

XO, OE pin 1

XO

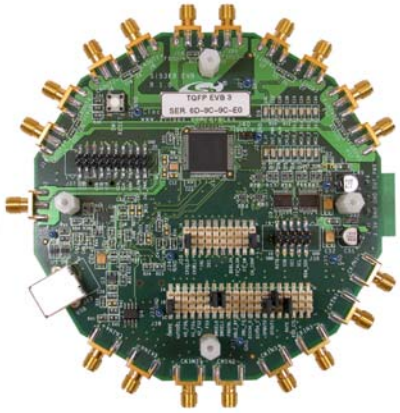
Features/Integration

Sales Tools

- **Documentation available from www.silabs.com/Timing**
  - **Data sheets**
  - **EVB data sheets**

- **Evaluation boards**
  - **Si5316-EVB**
  - **Si5322/23-EVB**
  - **Si5325/26-EVB**
  - **Si5365/66-EVB**
  - **Si5367/68-EVB**

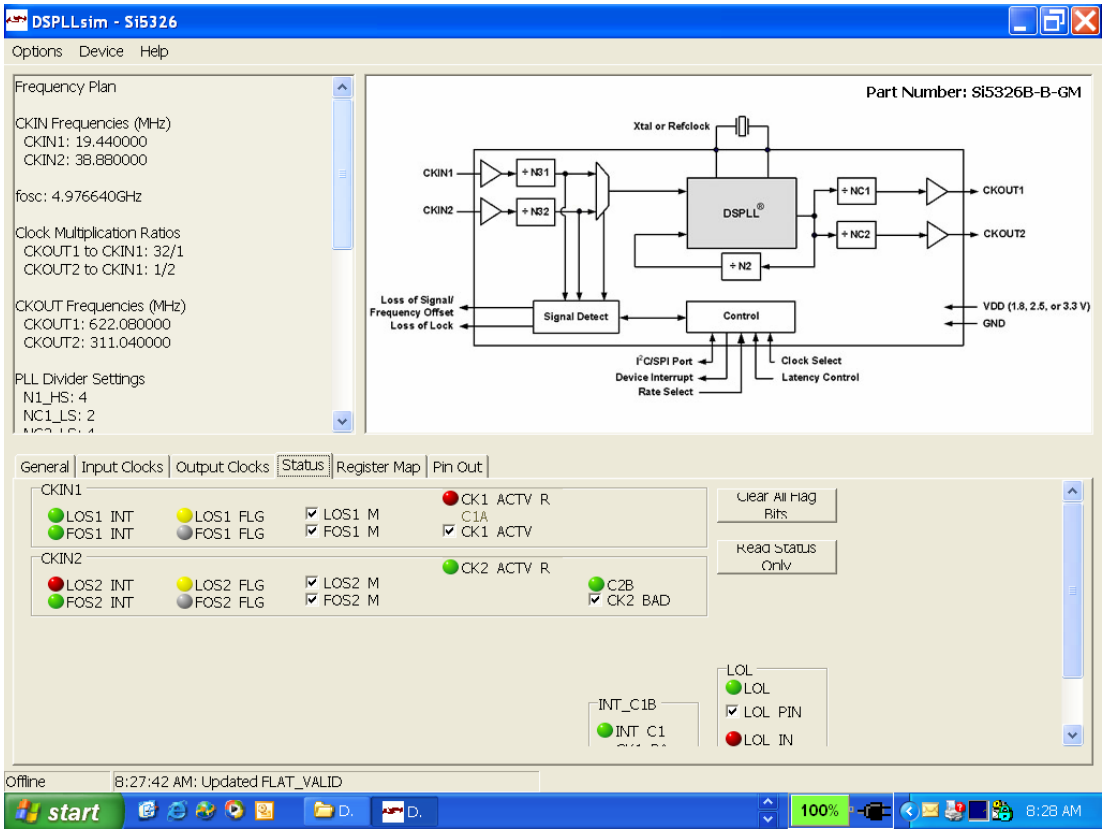
Si5325/26-EVB



Si5367/68-EVB

- **Documentation available from www.mysilabs.com/SalesGuide/Timing/PrecisionClockICs**
  - **DSPLL*sim* evaluation software**
  - **Any-Rate Precision Clock Family Reference Manual**
  - **Device errata**

DSPLL*sim*—Si53xx Customer Software



- **Simplifies frequency planning, loop bandwidth selection, device configuration**
- **Provides listing of pin/register settings for desired configuration**
- **Also used to control EVBs**

Product Availability & Contact Info

- **Product status**
  - **Samples: *Available today!***
  - **Evaluation Boards: *Available today!***
  - **Production: *2Q'07***

- **Contact**

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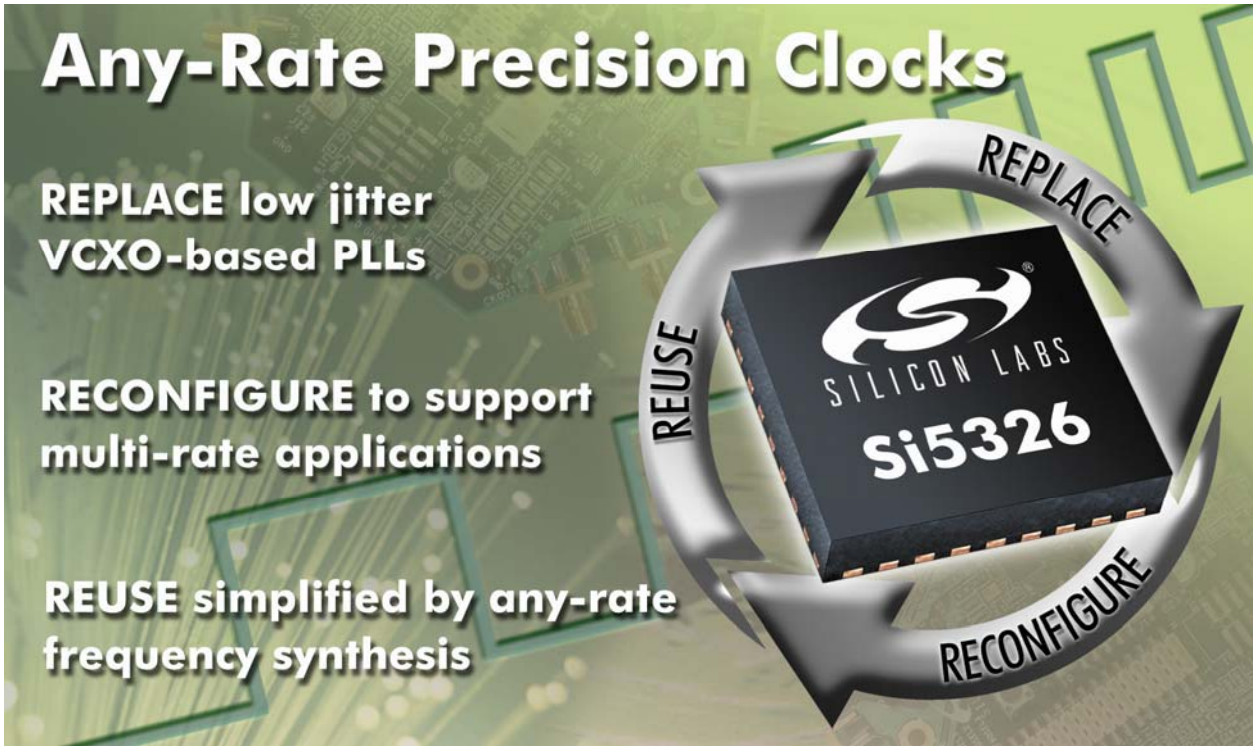
Si53xx Summary



- **Industry's first low jitter, any-rate clock multiplier/jitter attenuator family**
- **Industry-leading jitter performance**
- **Highly integrated and easy-to-use**

www.silabs.com/Timing