Features

Atmel's System Designer Contains the Following Items:

- **CD-ROM Containing all Necessary Software and Online Documents**
  - **Atmel's AVR Studio®**
  - **Atmel's Configurator Programming System (CPS)**
  - **Co-verification, Powered by Mentor Graphics**
  - **Exemplar's LeonardoSpectrum™**
  - **Model Technology™'s ModelSim®**
  - **Several C Compiler Evaluation Copies**
  - **Atmel's Integrated Development System (IDS) – FPGA Place & Route Tool**
- **Security Dongle (If Purchased ATDH94DNG)**

The materials delivered may vary based on the products ordered.

Description

Atmel's System Designer lets designers create fast and predictable designs with AT94K Field Programmable System Level Integrated Circuit (FPSLIC) and AT94S Secure FPSLIC devices.

Available for use with Windows® 95/98/2000/Me/XP and WindowsNT®-based computers. System Designer combines industry-standard software for design entry, synthesis and simulation with Atmel's proprietary software for component generation, automatic and interactive placement and routing, timing analysis and bit stream generation.

System Designer™

FPSLIC™

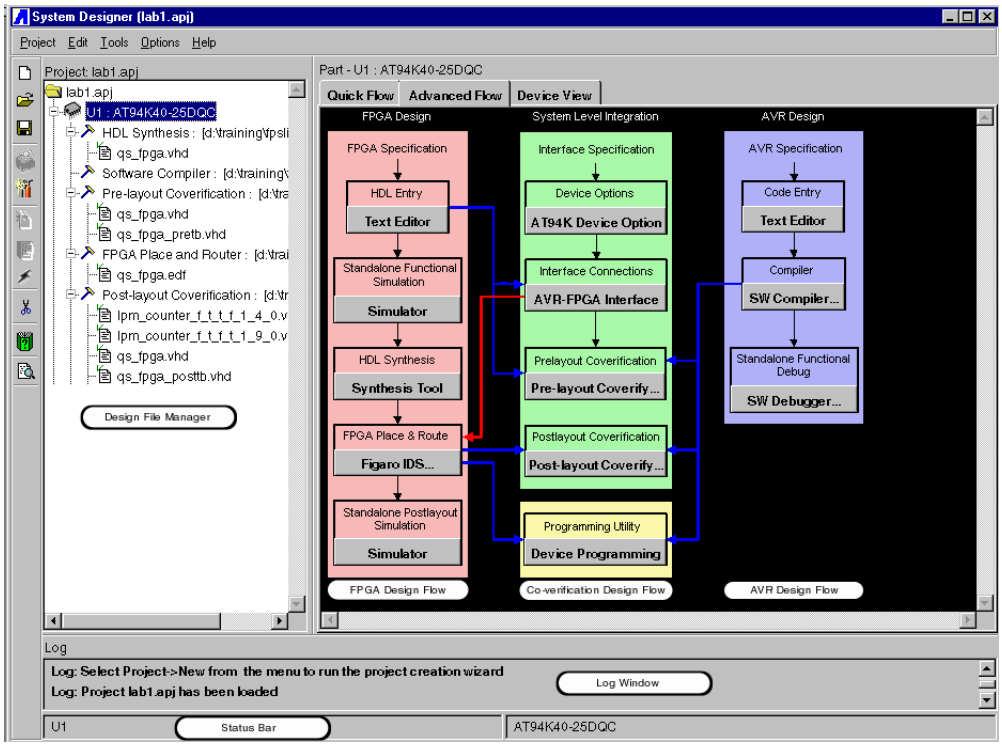
Programmable SLI AT94K/AT94S Series

Rev. 2307D–FPSLI–03/03

System Designer Desktop

The System Designer desktop is shown in Figure 1. The Design Flow chart on the right provides push-button access to all the stages in a typical design flow. This includes code entry, software debugging (Figure 2), simulation (Figure 3), synthesis (Figure 4) and generating files for simulations automatically. The FPGA Place and Route is described in Figure 5, Figure 6 and Figure 7 and the AVR®-FPGA Interface is described in Figure 8.

Figure 1. System Designer Desktop



Design Flow View

The Design Flow view shows the steps required to create a design for FPSLIC devices using System Designer and Co-verification. The arrows on the diagram show dependencies between the steps. The Flow view consists of two flows: FPGA flow and AVR flow. The System Level Integration flow is used for co-verification, see “Co-verification” on page 4. Designers can use the Coverification flow or may prefer to run the FPGA flow and the AVR flow stand-alone, and then merge the design at the end. In this case, the AVR designer and the FPGA designer have to agree on which parts of the design will be done in the AVR and which will be done in the FPGA. Then define the signals between the 2 devices.

FPGA Flow

To run the FPGA flow a test bench has to emulate the AVR side of the design to progress with the FPGA part of the design independently from the AVR progress. The only dependency into the FPGA flow is that the AVR FPGA interface section has to be run. This defines the connections from the FPGA to the AVR and provides the correct layout to optimize timing in design. If this dependency is not completed, the design will run as if it was a stand-alone FPGA with all the inputs being provided externally.

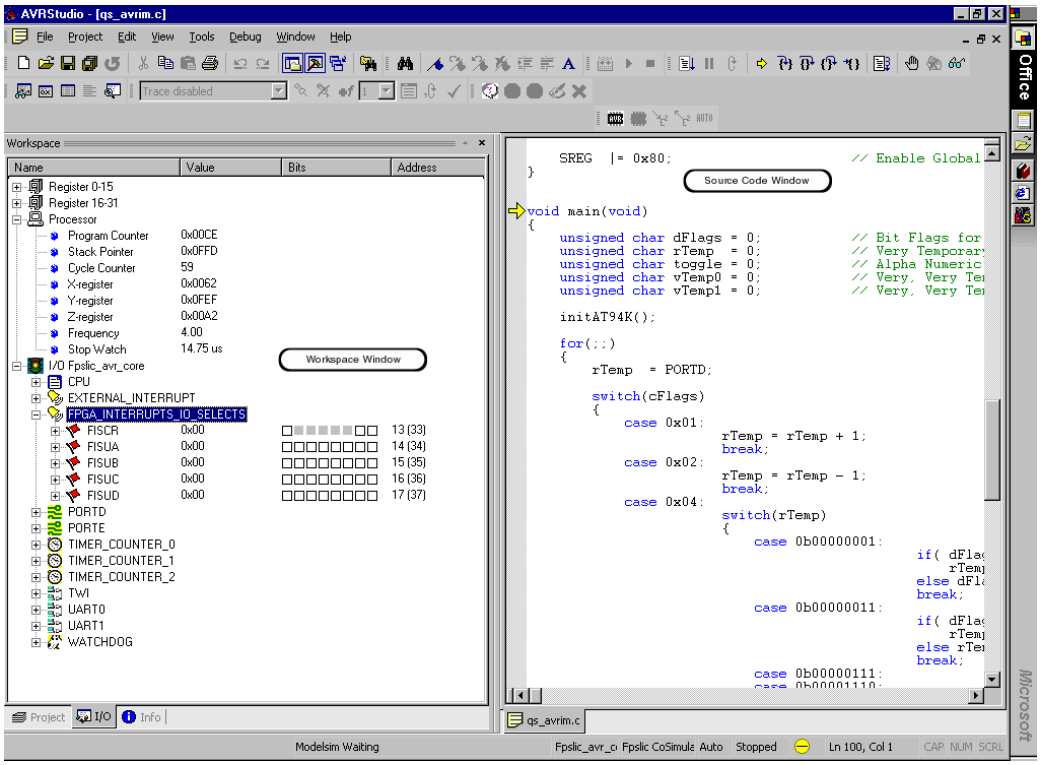
AVR Flow

The designer will develop the AVR function and use the normal AVR design flow with a compiler and debugger. This can either be done within System Designer or externally using IAR Workbench or Standalone AVR Studio.

AVR Studio

Figure 2 shows the AVR Studio software debugger tool, which provides a stand-alone debugging environment for the software-based design.

Figure 2. AVR Studio Debugger



JTAG ICE

The FPSLIC JTAG protocol gives the user the capability to view and control the internal resources of the FPSLIC device and perform real time emulation while the FPSLIC device is running on the target system. The FPSLIC JTAG ICE is supported only by AVR Studio 4.04 and not by any previous versions, System Designer populates AVR Studio with the FPSLIC specific files and makes it capable to emulate or simulate the FPSLIC devices.

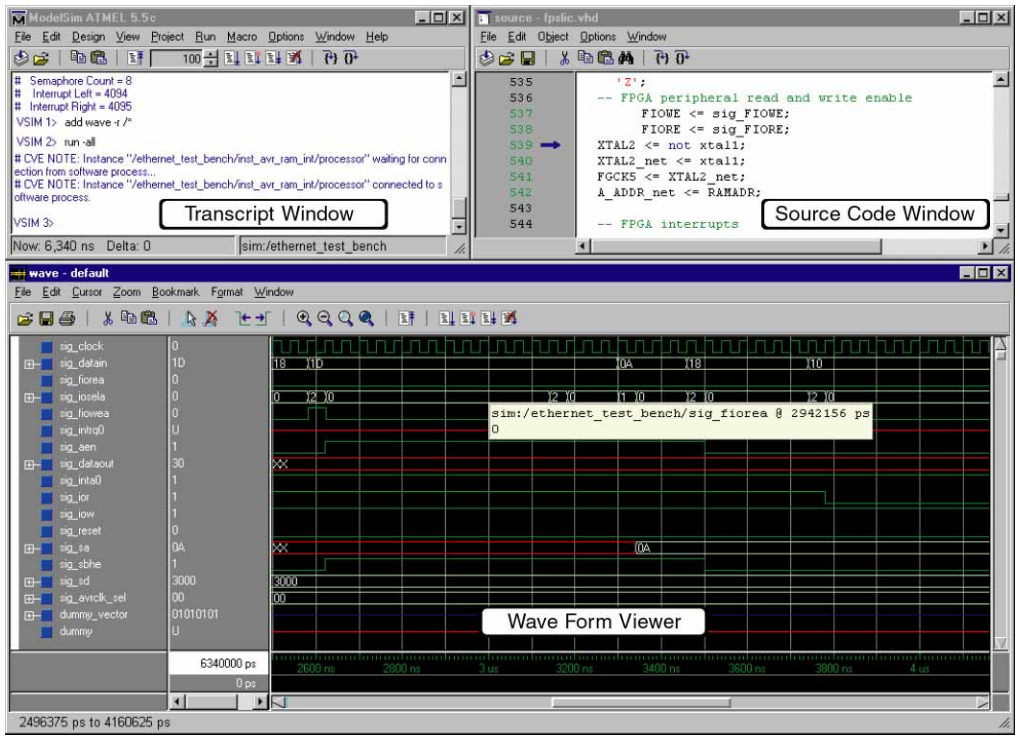
All FPSLIC devices with a JTAG compliant interface are provided with an OCD logic that interfaces with the JTAG emulator. This logic is capable of controlling the code execution in the FPSLIC device. So while a traditional emulator emulates device behavior, the JTAG ICE takes control of the device and executes the code in a physical device.

The OCD system provides exact electrical and timing characteristics, but a traditional emulator will normally have better visibility and control of the internal resources of the device. Features like trace buffer are not possible using the FPSLIC OCD system.

ModelSim

Model Technology's ModelSim is shown in Figure 3. ModelSim is the hardware simulator included with System Designer and is used for stand-alone and co-verification debugging of the HDL portion of the design.

Figure 3. Model Technology's ModelSim



Co-verification

Co-verification provides a simulation of the FPGA design with the AVR code, including the timing information from the FPGA. Co-verification allows 2 simulators to run through a shared interface, but only one of the simulators can accept input at any one time. If the AVR window is active, the ModelSim windows will be inactive. If ModelSim is active, the AVR Studio window will be inactive.

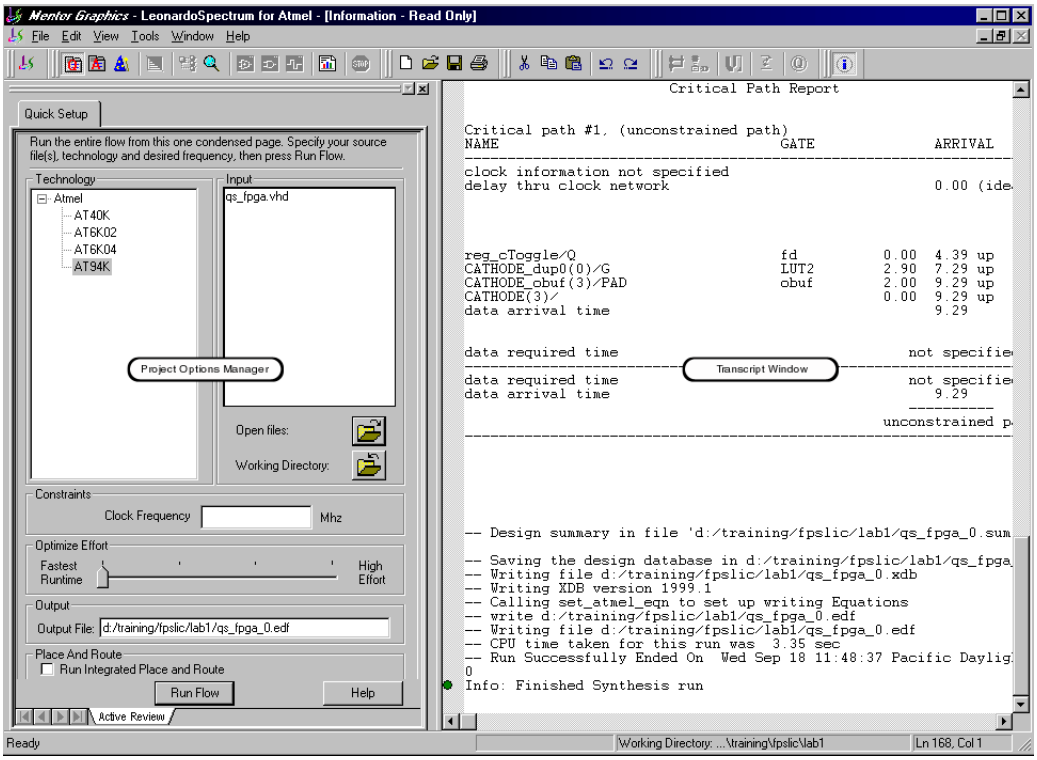
- Eliminates Prototype Boards by allowing the microcode and the hardware design to be developed simultaneously without a prototype board
- Allows Hardware/software Trade-off to quickly explore and test various hardware/software implementations to arrive at a highly optimized design.
- Faster Design Cycles by allowing the concurrent design of hardware and software.
- Parallel Hardware/Software Development by removing the software from the critical path and reducing the risk of hardware prototype iterations resulting from integration errors.

LeonardoSpectrum

LeonardoSpectrum is the synthesis tool included with System Designer and is shown in Figure 4. The synthesis tool is responsible for taking the HDL design and mapping it to the FPSLIC device.

System Designer also supports synthesis tools from vendors other than Mentor Graphics, such as Synplicity's Synplify® and Synopsys' FPGA Express™.

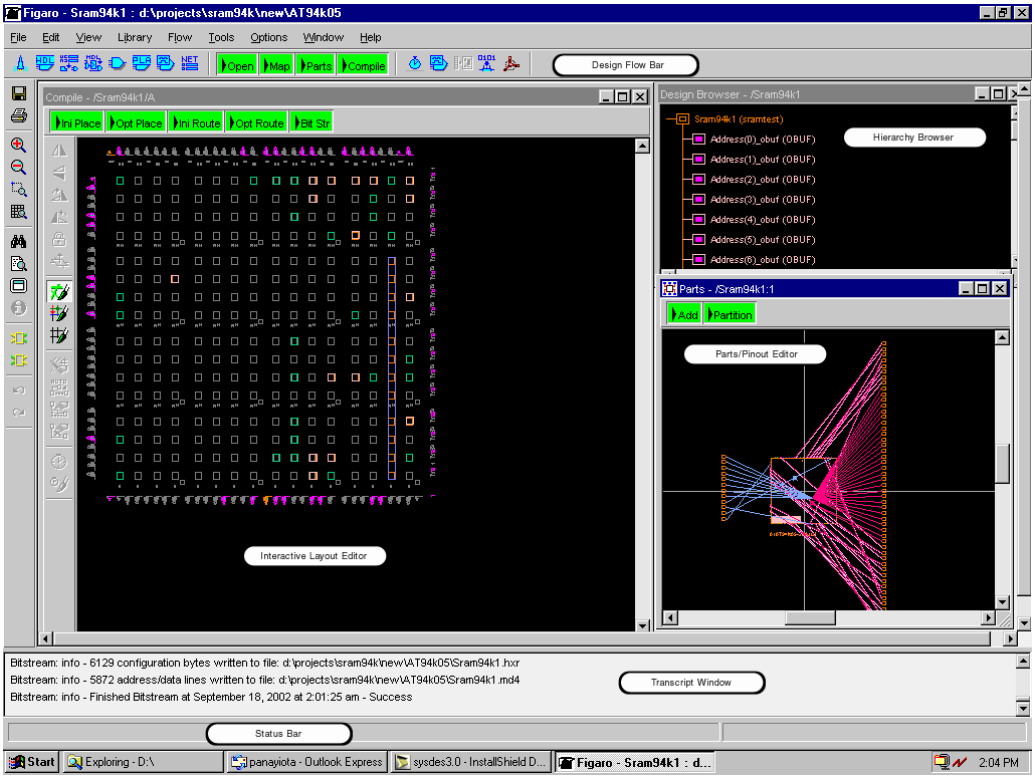
Figure 4. LeonardoSpectrum



Integrated Development System (IDS)

The FPSLIC/FPGA Integrated Development System (IDS) desktop is shown in Figure 5. The Design Flow Bar provides push-button access to all the steps in the design flow. This includes opening schematic entry and synthesis tools, and generating files for simulations automatically. The main responsibility of IDS in System Designer is for Placing and Routing the FPGA Logic.

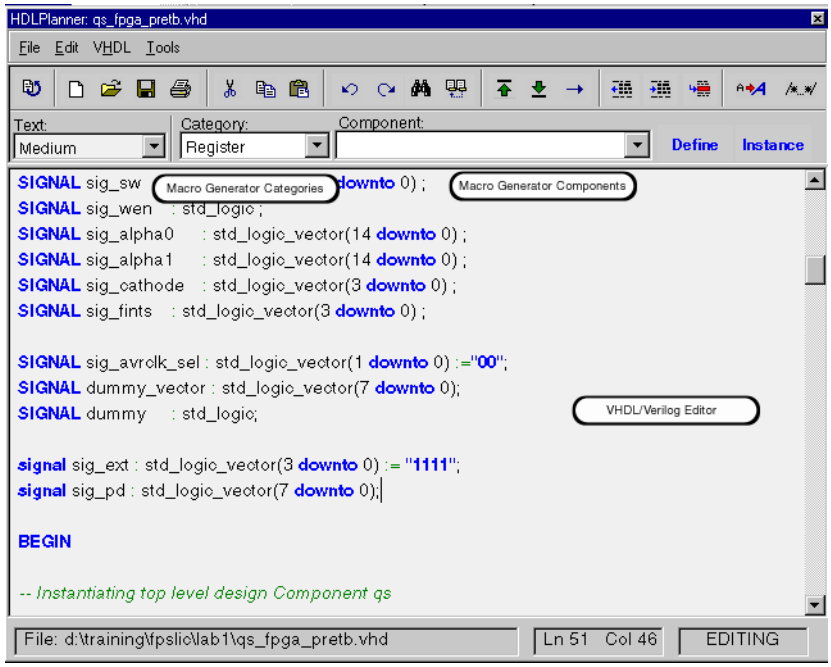
Figure 5. Integrated Development System (IDS) Desktop



HDLPlanner

Figure 6 shows the HDL Planner tool, which is used for VHDL and Verilog design entry.

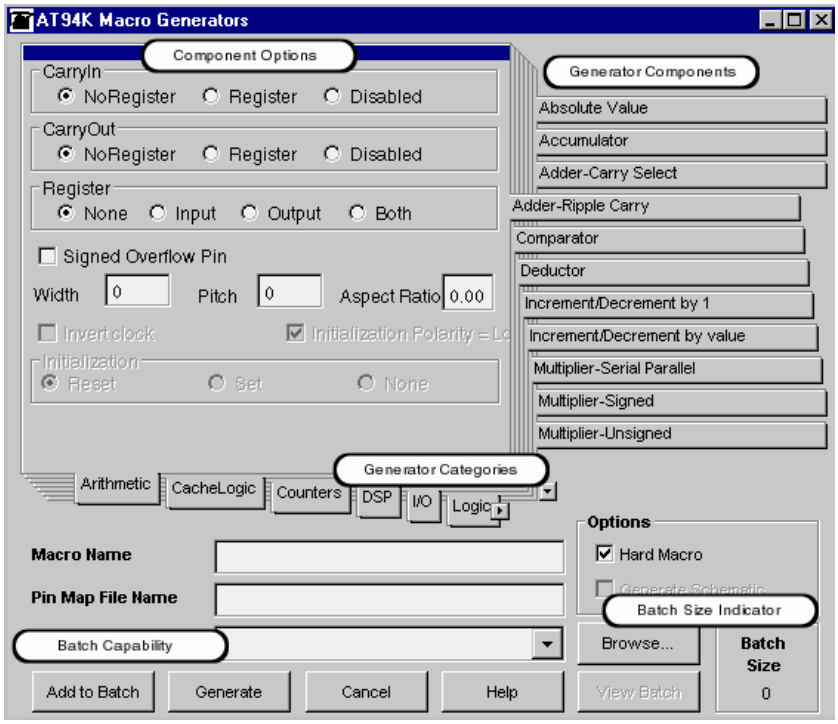
Figure 6. HDL Planner Tool



Macro Generator

Figure 7 shows the Macro Generator used to generate standard components with optimal layout and performance.

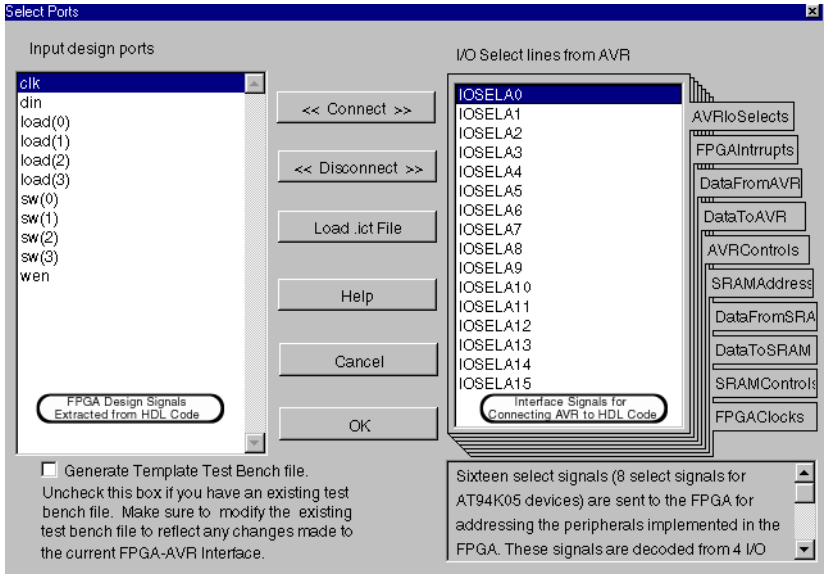
Figure 7. Macro Generator Window



AVR - FPGA Interface

The **AVR ⇔ FPGA Interface** dialog is shown in Figure 8. This is where the internal connections between the AVR Core and the FPGA Core are specified.

Figure 8. AVR ⇔ FPGA Interface



System Requirements

PC-based Systems

For a single-user system, System Designer requires a personal computer with a 80,486 or greater microprocessor equipped as follows:

- 3.5" 1.44-Mbyte capacity high-density disk drive (recommended)
- CD-ROM drive
- 250-Mbyte minimum hard drive (System Designer, ModelSim, LeonardoSpectrum, and IDS)
- 128 MB extended memory minimum
- Serial interface port
- Parallel interface port
- Windows 95/98/2000/Me/XP, or WindowsNT 4.0
- VGA graphics card and display monitor
- Windows compatible mouse
- A permanent swap space of 64 Mbytes – Refer to the Windows documentation for details on its setup
- Sufficient disk space for file archival and management
- Network Interface card or security dongle

Security Dongle

The software security dongle is used to generate a unique HOSTID for systems without a network interface card. The security dongle is connected to the PC through the parallel port interface. It is possible to configure a floating network license through the security dongle. The security dongle allows users to use the software dongle on different machines by removing and placing the dongle on other machines.

Ordering Information

Table 1. Software Ordering Codes

Code	Description
ATDS94KSW1	1 Year License
ATDS94KSW2	Perpetual License
ATDM94KSW2	Maintenance for Perpetual License

Table 2. Hardware Ordering Codes

Code	Description
ATDH40M	AT94K Series FPSLIC Prototyping Kit One Daughter Board Included – Specify: ATDH40D84 ATDH40D100 ATDH40D144 ATDH40D208
ATDH40D84	Daughter Board Attachment – 84PLCC
ATDH40D100	Daughter Board Attachment – 100VQFP
ATDH40D144	Daughter Board Attachment – 144PQFP
ATDH40D208	Daughter Board Attachment – 208PQFP
ATDH2200E	AT17 Series Configurator Programming Kit (Enhanced)
ATDH2221	20-pin SOIC Adapter for ATDH2200
ATDH2222	20-pin PLCC Adapter for ATDH2200
ATDH2223	8-pin SOIC Adapter for ATDH2200
ATDH2224	44-pin TQFP Adapter for ATDH2200
ATDH2225	In-System Programming (ISP) Cable
ATDH2226	32-pin TQFP Adapter for ATDH2200
ATDH2227	44-pin PLCC Adapter for ATDH2200
ATDH2228	8-pin LAP Adapter for ATDH2200
ATSTK94	AT94K FPSLIC Starter Kit with System Designer
ATDH94DNG	System Designer Software Security Dongle

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