# Features

Atmel's System Designer Contains the Following Items:

- CD-ROM Containing all Necessary Software and Online Documents
  - Atmel's AVR Studio<sup>®</sup>
  - Atmel's Configurator Programming System (CPS)
  - Co-verification, Powered by Mentor Graphics
  - Exemplar's LeonardoSpectrum™
  - Model Technology<sup>™</sup>'s ModelSim<sup>®</sup>
  - Several C Compiler Evaluation Copies
  - Atmel's Integrated Development System (IDS) FPGA Place & Route Tool
- Security Dongle (If Purchased ATDH94DNG)

The materials delivered may vary based on the products ordered.

# Description

Atmel's System Designer lets designers create fast and predictable designs with AT94K Field Programmable System Level Integrated Circuit (FPSLIC) and AT94S Secure FPSLIC devices.

Available for use with Windows<sup>®</sup> 95/98/2000/Me/XP and WindowsNT<sup>®</sup>-based computers. System Designer combines industry-standard software for design entry, synthesis and simulation with Atmel's proprietary software for component generation, automatic and interactive placement and routing, timing analysis and bit stream generation.



System Designer<sup>™</sup>



Programmable SLI AT94K/AT94S Series

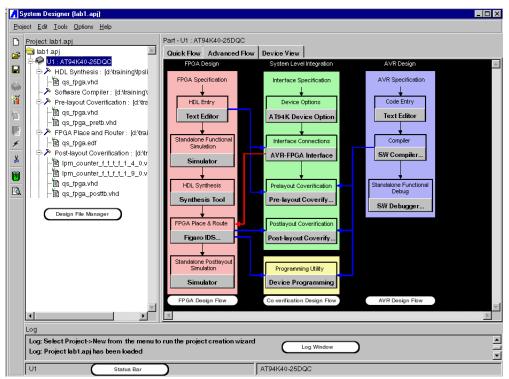
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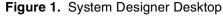




# System Designer Desktop

The System Designer desktop is shown in Figure 1. The Design Flow chart on the right provides push-button access to all the stages in a typical design flow. This includes code entry, software debugging (Figure 2), simulation (Figure 3), synthesis (Figure 4) and generating files for simulations automatically. The FPGA Place and Route is described in Figure 5, Figure 6 and Figure 7 and the AVR<sup>®</sup>-FPGA Interface is described in Figure 8.



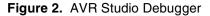


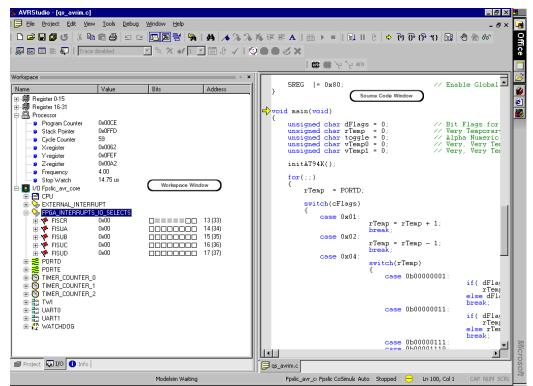
Design Flow View	The Design Flow view shows the steps required to create a design for FPSLIC devices using System Designer and Co-verification. The arrows on the diagram show dependencies between the steps. The Flow view consists of two flows: FPGA flow and AVR flow. The System Level Integration flow is used for co-verification, see "Co-verification" on page 4. Designers can use the Coverification flow or may prefer to run the FPGA flow and the AVR flow stand-alone, and then merge the design at the end. In this case, the AVR designer and the FPGA designer have to agree on which parts of the design will be done in the AVR and which will be done in the FPGA. Then define the signals between the 2 devices.
FPGA Flow	To run the FPGA flow a test bench has to emulate the AVR side of the design to progress with the FPGA part of the design independently from the AVR progress. The only dependency into the FPGA flow is that the AVR FPGA interface section has to be run. This defines the connections from the FPGA to the AVR and provides the correct layout to optimize timing in design. If this dependency is not completed, the design will run as if it was a stand-alone FPGA with all the inputs being provided externally.
AVR Flow	The designer will develop the AVR function and use the normal AVR design flow with a compiler and debugger. This can either be done within System Designer or externally using IAR Workbench or Standalone AVR Studio.

# **System Designer**

## **AVR Studio**

Figure 2 shows the AVR Studio software debugger tool, which provides a stand-alone debugging environment for the software-based design.





## JTAG ICE

The FPSLIC JTAG protocol gives the user the capability to view and control the internal resources of the FPSLIC device and perform real time emulation while the FPSLIC device is running on the target system. The FPSLIC JTAG ICE is supported only by AVR Studio 4.04 and not by any previous versions, System Designer populates AVR Studio with the FPSLIC specific files and makes it capable to emulate or simulate the FPSLIC devices.

All FPSLIC devices with a JTAG compliant interface are provided with an OCD logic that interfaces with the JTAG emulator. This logic is capable of controlling the code execution in the FPSLIC device. So while a traditional emulator emulates device behavior, the JTAG ICE takes control of the device and executes the code in a physical device.

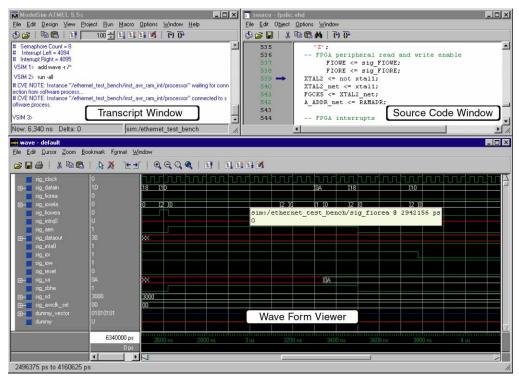
The OCD system provides exact electrical and timing characteristics, but a traditional emulator will normally have better visibility and control of the internal resources of the device. Features like trace buffer are not possible using the FPSLIC OCD system.





## ModelSim

Model Technology's ModelSim is shown in Figure 3. ModelSim is the hardware simulator included with System Designer and is used for stand-alone and co-verification debugging of the HDL portion of the design.



## **Co-verification**

Co-verification provides a simulation of the FPGA design with the AVR code, including the timing information from the FPGA. Co-verification allows 2 simulators to run through a shared interface, but only one of the simulators can accept input at any one time. If the AVR window is active, the ModelSim windows will be inactive. If ModelSim is active, the AVR Studio window will be inactive.

- Eliminates Prototype Boards by allowing the microcode and the hardware design to be developed simultaneously without a prototype board
- Allows Hardware/software Trade-off to quickly explore and test various hardware/software implementations to arrive at a highly optimized design.
- Faster Design Cycles by allowing the concurrent design of hardware and software.
- Parallel Hardware/Software Development by removing the software from the critical path and reducing the risk of hardware prototype iterations resulting from integration errors.

**System Designer** 

## LeonardoSpectrum

LeonardoSpectrum is the synthesis tool included with System Designer and is shown in Figure 4. The synthesis tool is responsible for taking the HDL design and mapping it to the FPSLIC device.

System Designer also supports synthesis tools from vendors other than Mentor Graphics, such as Synplicity's Synplify<sup>®</sup> and Synopsys' FPGA Express<sup>™</sup>.

J Menter Graphics - LeonardoSpectrum for Atmel - [Information - Re	ad Onlu	1	
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	1	Critical Path Report	<b></b>
Quick Setup Run the entire flow from this one condensed page. Specify your source		Critical path #1, (unconstrained path) NAME GATE	ARRIVAL
file(s), technology and desired frequency, then press Run Flow.			ARRIVAL
Technology Input		clock information not specified Helay thru clock network	0.00 (ide
AT40K AT6K02 AT6K04 AT94K		CATHODE_dup0(0)/G LUT2 2.90 CATHODE_obuf(3)/PAD obuf 2.00	4.39 up 7.29 up 9.29 up 9.29 up 9.29 up 9.29
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Open files:	- 11	uncor	nstrained p
Working Directory:			
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Clock Frequency Mhz		Design summary in file 'd:/training/fpslic/lab1/gs	foga 0.sum
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Ready		Working Directory:\training\fpslic\lab1	.n 168, Col 1 🦷 🎢

Figure 4. LeonardoSpectrum

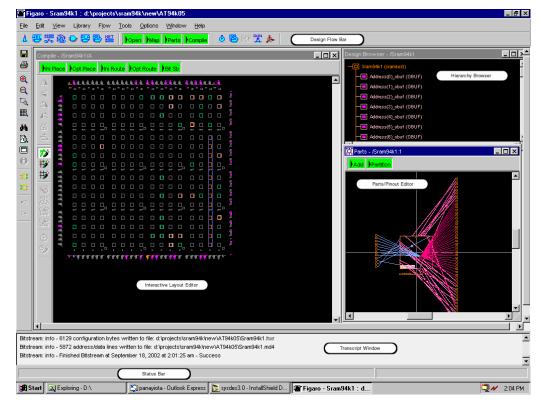




# Integrated Development System (IDS)

The FPSLIC/FPGA Integrated Development System (IDS) desktop is shown in Figure 5. The Design Flow Bar provides push-button access to all the steps in the design flow. This includes opening schematic entry and synthesis tools, and generating files for simulations automatically. The main responsibility of IDS in System Designer is for Placing and Routing the FPGA Logic.





# 6 System Designer

## **HDLPlanner**

Figure 6 shows the HDL Planner tool, which is used for VHDL and Verilog design entry.

Figure 6	. HDL	Planner	Tool
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HDLPlanner: qs_fpga_pretb.vhd
<u>File Edit VH</u> DL <u>I</u> ools
Text: Component. Medium  Category: Component. Define Instance
SIGNAL sig_sw (Macro Generator Categories plownto 0); (Macro Generator Components)
SIGNAL sig_wen : std_logic;
SIGNAL sig_alpha0 : std_logio_vector(14 downto 0);
SIGNAL sig_alpha1 : std_logio_vector(14 downto 0);
SIGNAL sig_cathode : std_logic_vector(3 downto 0);
SIGNAL sig_fints : std_logio_vector(3 downto 0);
SIGNAL sig_avrolk_sel: std_logic_vector(1 downto 0) :="00";
SIGNAL dummy_vector : std_logic_vector(7 downto 0);
SIGNAL dummy : std_logic; VHDL/Verilog Editor
signal sig_ext : std_logic_vector(3 downto 0) := "1111";
signal sig_pd : std_logio_vector(7 downto 0);
BEGIN
Instantiating top level design Component gs
L
File: d:\training\fpslic\lab1\qs_fpga_pretb.vhd Ln 51 Col 46 EDITING

## **Macro Generator** Figure 7 shows the Macro Generator used to generate standard components with optimal layout and performance.

#### Figure 7. Macro Generator Window

AT94K Macro Generators	
CarryIn Component Options	Generator Components
NoRegister O Register O Disabled	Absolute Value
CarryOut © NoRegister O Register O Disabled	Accumulator
Register	Adder-Carry Select
None O Input O Output O Both	Adder-Ripple Carry
Signed Overflow Pin	Comparator Deductor
Width 0 Pitch 0 Aspect Ratio 0.00	Increment/Decrement by 1
Invertolook 🗹 Initialization Polarity = Lo	Increment/Decrement by value
Initialization     O Set     O None	Multiplier-Serial Parallel
	Multiplier-Signed Multiplier-Unsigned
Arithmetic CacheLogic Counters DSP 1/0 Logic	
Macro Name	Hard Macro
Pin Map File Name	Batch Size Indicator
Batch Capability	▼ Browse Batch
Add to Batch Generate Cancel He	lp View Batch 0

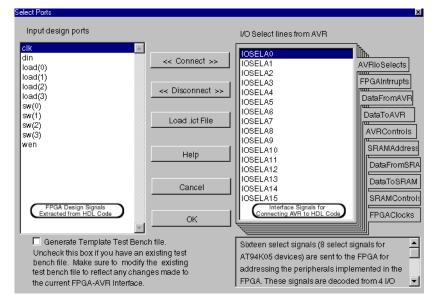




## AVR - FPGA Interface

The **AVR**  $\Leftrightarrow$  **FPGA Interface** dialog is shown in Figure 8. This is where the internal connections between the AVR Core and the FPGA Core are specified.





## System Requirements

PC-based Systems

For a single-user system, System Designer requires a personal computer with a 80,486 or greater microprocessor equipped as follows:

- 3.5" 1.44-Mbyte capacity high-density disk drive (recommended)
- CD-ROM drive
- 250-Mbyte minimum hard drive (System Designer, ModelSim, LeonardoSpectrum, and IDS)
- 128 MB extended memory minimum
- Serial interface port
- Parallel interface port
- Windows 95/98/2000/Me/XP, or WindowsNT 4.0
- VGA graphics card and display monitor
- Windows compatible mouse
- A permanent swap space of 64 Mbytes Refer to the Windows documentation for details on its setup
- Sufficient disk space for file archival and management
- Network Interface card or security dongle

## Security Dongle

The software security dongle is used to generate a unique HOSTID for systems without a network interface card. The security dongle is connected to the PC through the parallel port interface. It is possible to configure a floating network license through the security dongle. The security dongle allows users to use the software dongle on different machines by removing and placing the dongle on other machines.

# **Ordering Information**

Table 1. Software Ordering Codes

Code	Description
ATDS94KSW1	1 Year License
ATDS94KSW2	Perpetual License
ATDM94KSW2	Maintenance for Perpetual License

### Table 2. Hardware Ordering Codes

Code	Description
ATDH40M	AT94K Series FPSLIC Prototyping Kit
	One Daughter Board Included – Specify:
	ATDH40D84
	ATDH40D100
	ATDH40D144
	ATDH40D208
ATDH40D84	Daughter Board Attachment – 84PLCC
ATDH40D100	Daughter Board Attachment – 100VQFP
ATDH40D144	Daughter Board Attachment – 144PQFP
ATDH40D208	Daughter Board Attachment – 208PQFP
ATDH2200E	AT17 Series Configurator Programming Kit (Enhanced)
ATDH2221	20-pin SOIC Adapter for ATDH2200
ATDH2222	20-pin PLCC Adapter for ATDH2200
ATDH2223	8-pin SOIC Adapter for ATDH2200
ATDH2224	44-pin TQFP Adapter for ATDH2200
ATDH2225	In-System Programming (ISP) Cable
ATDH2226	32-pin TQFP Adapter for ATDH2200
ATDH2227	44-pin PLCC Adapter for ATDH2200
ATDH2228	8-pin LAP Adapter for ATDH2200
ATSTK94	AT94K FPSLIC Starter Kit with System Designer
ATDH94DNG	System Designer Software Security Dongle





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La Chantrerie BP 70602 44306 Nantes Cedex 3, France Tel: (33) 2-40-18-18-18 Fax: (33) 2-40-18-19-60

#### ASIC/ASSP/Smart Cards

Zone Industrielle 13106 Rousset Cedex, France Tel: (33) 4-42-53-60-00 Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd. Colorado Springs, CO 80906 Tel: 1(719) 576-3300 Fax: 1(719) 540-1759

Scottish Enterprise Technology Park Maxwell Building East Kilbride G75 0QR, Scotland Tel: (44) 1355-803-000 Fax: (44) 1355-242-743 **RF**/Automotive

Theresienstrasse 2 Postfach 3535 74025 Heilbronn, Germany Tel: (49) 71-31-67-0 Fax: (49) 71-31-67-2340

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