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Comparison of MC9S08QE128 and MCF51QE128 Microcontrollers

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The MC9S08QE128 and MCF51QE128 are the first pair of 8-bit and 32-bit MCUs to be designed specifically for Freescale's controller continuum. These devices maximize reuse of peripherals, packages, pinouts, and development tools to make the conversion from an 8-bit to a 32-bit MCU (or vice versa) as seamless and effortless as possible.

This document highlights the similarities of the two devices and also points out the few differences developers need to consider to design systems that are compatible with both devices. It will also make developers aware of the additional features available when migrating up to the MCF51QE128. The features and operation will not be discussed in detail in this document. Instead, the data sheets and reference manuals for each device should be consulted for detailed descriptions.

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Table 1. Comparison of MC9S08QE128 and MCF51QE128

MC9S08QE128	MCF51QE128
Central Processor Unit (CPU) Core	
Up to 50-MHz CPU[2] from 3.6 V to 2.1 V, and 20-MHz CPU from 2.1 V to 1.8 V across temperature range of –40°C to 85°C	
8-bit HCS08 core	*32-bit ColdFire® V1 core[1]*
8-bit data bus, 16-bit address bus	*32-bit core data bus, 8-bit peripheral data bus, 24-bit address bus*
64K memory map, 16K paging window for addressing memory beyond 64K[2]; linear address pointer for accessing data across entire memory range[2]	*16M memory map, entire memory map addressed directly*
HC08 instruction set with added BGND, CALL[2], and RTC[2] instructions	*ColdFire Instruction Set Revision C (ISA_C)*, additional instructions for efficient handling of 8-bit and 16-bit data
Support for up to 32 interrupt/reset exceptions; exception priorities are fixed; one level of interrupt grouping; no hardware support for nesting	*Support for up to 256 interrupt/reset exceptions (39 used on MCF51QE128); exception priorities are fixed, except two interrupts can be remapped; seven levels of interrupt grouping; hardware support for nesting*
Resets: one vector for all reset sources; vector must point to address within pages 0–3; no illegal address reset, entire memory map is legal	*Resets: vectors for up to 64 reset sources; vector can point to any valid address; illegal address reset is supported*
System reset status (SRS) register sets flag for most recent reset source[1]	
On-Chip Memory	
Peripheral register maps maintain relative addresses	
Up to 8K of random-access memory (RAM)	
Flash read/program/erase over full operating voltage and temperature	
Up to 128K byte of flash[2], two flash arrays of 64K x 8-bits arranged in series; two flash arrays allow for "read while write" programming	*Up to 128K byte of flash, two flash arrays of 32K x 16-bits arranged in parallel; flash "read while write" not supported*
Security circuitry to prevent unauthorized access to RAM and flash contents; default is secured when blank	*Security circuitry to prevent unauthorized access to RAM and flash contents; default is unsecured when blank*
Power-Saving Modes	
Two very low power stop modes	
Low power run (LPRun) and wait (LPWait) modes allow for use of peripherals in reduced-current and reduced-speed mode[1,2]	
Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents[1,2]	
Very low power external oscillator that can be used in stop modes to provide accurate clock source to RTC module[1,2]	
Very low power real time counter for use in run, wait, and stop modes with internal and external clock sources[1]	
6 μs typical wake up time from stop3 mode[1,2]	
Reduced power wait mode *(enabled by WAIT instruction)*	Reduced power wait mode *(enabled by setting WAITE bit in the SOPT1 register then executing STOP instruction)*[1]

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Clock Source Options	
Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz	
Internal Clock Source (ICS)[1] — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports CPU frequencies from 2 MHz to 50 MHz[2]	
System Protection	
Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock	
Low-voltage detection with reset or interrupt; selectable trip points	
Illegal opcode detection with reset	
No illegal address reset, all addresses in map are legal	*Illegal address detection with reset*
Flash block protection: protects in 1K increments; protects array 0 first (from 0x0FFFF–0x00000), then array 1 (from 0x1FFFF–0x10000)[2]	*Flash block protection: protects in 2K increments; protects array from 0x(00)00_0000 to 0x(00)01_FFFF*
Development Support	
Single-wire background debug interface; same hardware BDM cable supports both devices[1]	
One version of CodeWarrior™ IDE and debugger supports both devices[1]	
CodeWarrior stationary, project wizard, initialization wizard and Processor Expert make C-code conversion between devices easy	
Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus three more breakpoints in on-chip debug module)	*Integrated ColdFire DEBUG_Rev_B+ interface with single-wire BDM connection supports same electrical interface used by the S08 family debug modules.[1]*
On-chip in-circuit emulator (ICE) debug module containing three comparators[2] and nine trigger modes. Eight deep FIFO for tracing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.	*Classic ColdFire Debug B+ functionality mapped into the single-pin BDM interface; 64 deep FIFO for tracing processor status (PST) and debug data (DDATA)[1]; real time debug support, with 6 hardware breakpoints (four PC, one address, and one data) that can be configured into a 1- or 2-level trigger with a programmable response*
Peripherals[3]	
ADC — 24-channel, 12-bit resolution; 2.5 μs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V	
ACMPx — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; operation in stop3	
SCIx — Two serial communications interface modules with optional 13-bit break	
SPIx— Two serial peripheral interfaces with full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting	

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IICx — Two IICs with up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing	
TPMx — One 6-channel (TMP3) and two 3-channel (TPM1 and TPM2) 16-bit timer modules; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel;	
RTC — (real-time counter) 8-bit modulus counter with binary or decimal based prescaler; external clock source for precise time base, time-of-day, calendar, or task scheduling functions; free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components; runs in all MCU modes	
Input/Output	
70 GPIOs and 1 input-only and 1 output-only pin	
16 KBI interrupt pins with selectable polarity	
Hysteresis and configurable pull up device on all input pins; configurable slew rate and drive strength on all output pins.	
SET/CLR registers on 16 pins (PTC and PTE)[2]	
No support for Rapid I/O	*Selectable Rapid I/O supported on PTC and PTE*
Package Options	
Pin-to-pin compatible in 80-LQFP and 64-LQFP packages	
Additional 48-QFN, 44-QFP and 32-LQFP packages[4]	*no additional packages*

1 New feature for ColdFire MCUs

2 New feature for S08 MCUs

3 All peripherals new to ColdFire MCUs

4 32-LQFP package is available only on the MC9S08QE64 derivative

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