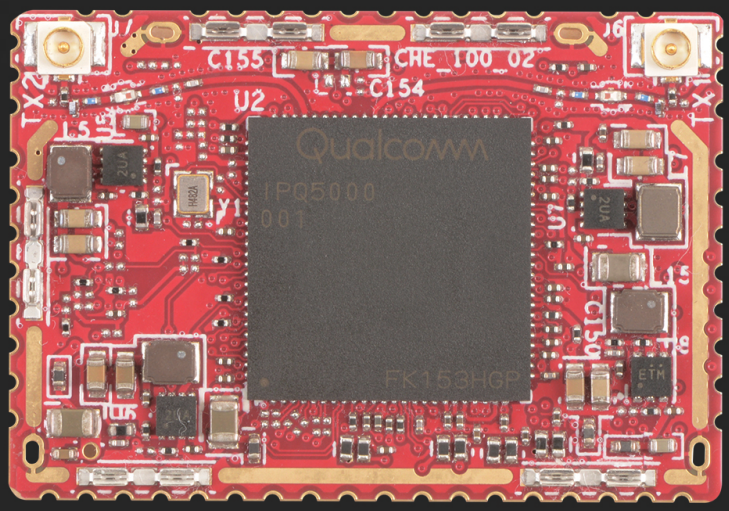


Cherry is an IPQ 5000 SoC based Wi-Fi 6 System-on-Module (SoM). It is a compact, integrated module that combines all the components required for building a complete system into a single form factor. Cherry is designed to simplify the process of designing and manufacturing embedded devices and wireless communication systems. With its high-performance processor, memory, storage, and networking capabilities, the Cherry SoM is well-suited for a wide range of applications, including IoT, networking, and wireless communications. By incorporating all the necessary components into a single module, the Cherry SoM reduces the time-to-market and overall cost of the end product, making it an attractive solution for many different types of embedded systems.

The module supports 2 spatial streams (2x2 MiMo) and is powered by a 64-bit dual-core ARM Cortex A53 processor with a 1 GHz clock speed. It is a surface mountable SoM and has a very small form factor (same as Lima). Cherry has external castellated pins that are pin to pin compatible with Lima castellated pins. For additional functions, Cherry has an additional line of inner LGA pins.

Quick specs

- Wi-Fi 6 (802.11b/g/n/ac/ax) 2.4 GHz with 2x2 MU-MIMO 1024 QAM (2SS), 20/40 MHz, 573.5 Mbps data-rate
- Based on IPQ-5000 SoC
- 22 dBm per chain RF output power
- Size – 30.5 by 19.4 mm
- Calculated maximum power consumption is 7 W
- Available interfaces – UART, 1 GbE PHY and SGMII+ or SGMII mode for 2.5/1 GbE PHY, 2x free SPI chip select pins, PCIe 2.0, 25xGPIO.

Table of Contents

1. Features

TABLE 1-1. CHERRY FEATURES

Feature list			CHE_100 Cherry
Integrated core	Core type		IPQ-5000 64-bit dual core ARM Cortex-A53
	Core clock frequency		1GHz
	Cache		256kB L2
Memory	DRAM		Integrated DDR3L 256MB
	NOR FLASH		32MB
WIFI	IEEE 802.11 b/g/n/ax 2x2 MU-MIMO 2.4GHz 20/40 MHz 1024 QAM		2412-2472MHz 22dBm per chain
RF connector	Two U.FI connectors		2
Peripherals	PWM	Pulse Width Modulation interface	4
	QSPI	Qualcomm Parallel Interface Controller	1
	BLSP	UART/SPI/I2C	3
	I2C	Audio Pulse Width Modulation interface	4
	PCIe	2.0 single lane PCIe interface	1
	Ethernet	One integrated 1Gbps and one SerDes supporting 3.125/1.25Gbps Ethernet port for external 2.5/1 GbE PHYs.	2
	Reset	Internal reset input	1

2. Module pinout and Pin description

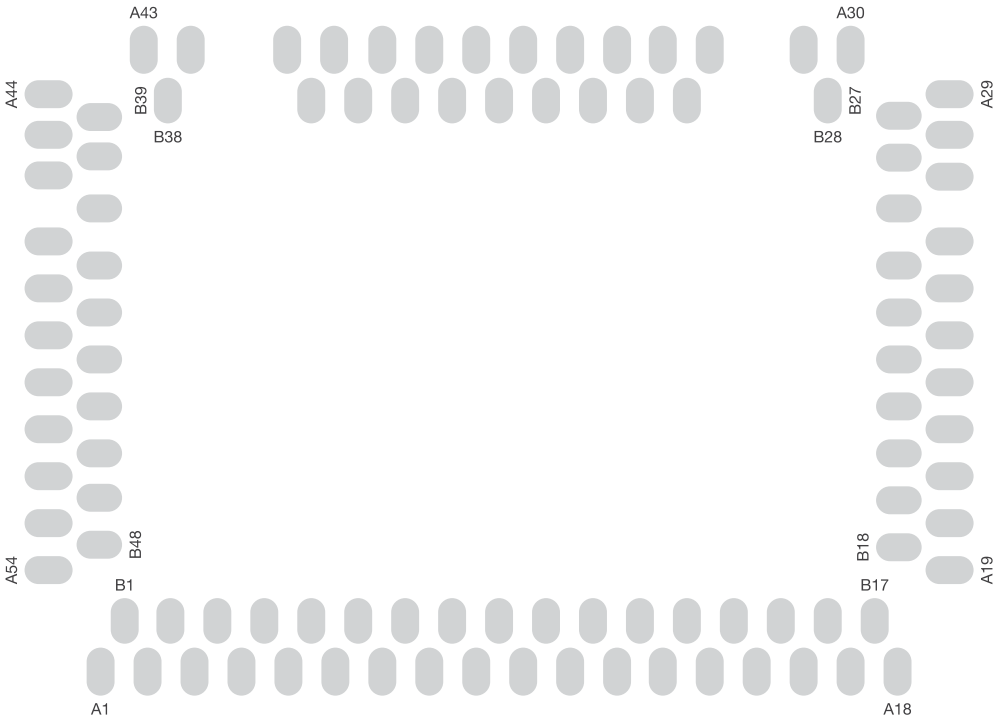


TABLE 2-1. I/O DESCRIPTION (PIN TYPE) PARAMETERS

Symbol	Description
AI	Analog input
AO	Analog output
GND	Ground
RF In/Out	RF input/output
I	Digital input signal
O	Digital output signal
IO	Digital bidirectional signal
Z	High-impedance

TABLE 2-2. POWER AND GROUND

Pin ID	Pin name	Type	Description
A1, B1, A2, B2	3.3VD	I	3.3V digital power
A18	VDD1P95	O	1.95V output power for ethernet
B3, A8, B11, B12, A13, B13, A23, A26, A27, B26, B27, A29, A30, B37, A42, A43, A44, B39, B40, A46, A50, B47, A53, B48, A54	GND	GND	Ground
A25, A24, A32, A33, A34, A35, A36, A37, B32, B33, B35, B36, B38, A28, A45	NC	NC	Not connected

TABLE 2-4. PCIE

Pin ID	Pin name	Type	Description
B8	UPHY_REFCLK_OP	AO	Differential reference clock
B7	UPHY_REFCLK_ON	AO	
B10	UPHY_TXP	AO	Differential output of transmitter
B9	UPHY_TXN	AO	
B5	UPHY_RXP	AI	Differential output of receiver
B6	UPHY_RXN	AI	

TABLE 2-5. SPI

Pin ID	Pin name	Type	Description
A24	SPI_MISO	IO	Data transmission from an external device to the Lima. On reset, SPI_MISO is input, which should be interfaced with an SPI device via a resistor divider for reliability.
A25	SPI_MOSI	IO	Data transmission from the Lima to an external device. On reset, SPI_MOSI is output and can directly interface with a SPI device such as a serial flash.
A21	SPI_CLK	AO	SPI serial interface clock
A19	SPI_CS1	AO	SPI chip select

TABLE 2-6. ETHERNET

Pin ID	Pin name	Type	Description
A15	P4_TRX0-	IO	GEPHY signal channel0 signal
A14	P4_TRX0+	IO	
A17	P4_TRX1-	IO	GEPHY signal channel1 signal
A16	P4_TRX1+	IO	
A10	P4_TRX2-	IO	GEPHY signal channel2 signal
A9	P4_TRX2+	IO	
A12	P4_TRX3-	IO	GEPHY signal channel3 signal
A11	P4_TRX3+	IO	
B25	SGMII_RXN	AI	Differential output of transmitter. Max data rate = 3.125Gbps
B24	SGMII_RXP	AI	
B23	SGMII_REFCLK_OP	AO	Reference clock
B22	SGMII_TXN	AO	Differential output of receiver. Max data rate = 3.125Gbps
B21	SGMII_TXP	AO	

TABLE 2-7. GPIO

Pin ID	Pin name	Type	Description
A3	GPIO_4	IO	General-purpose digital I/O pin
A4	GPIO_5	IO	General-purpose digital I/O pin
A5	GPIO_6	IO	General-purpose digital I/O pin
A6	GPIO_7	IO	General-purpose digital I/O pin
A7	GPIO_8	IO	General-purpose digital I/O pin
B45	GPIO_9	IO	General-purpose digital I/O pin
A47	GPIO_14	IO	General-purpose digital I/O pin
A48	GPIO_15	IO	General-purpose digital I/O pin
A49	GPIO_16	IO	General-purpose digital I/O pin
B46	GPIO_17	IO	General-purpose digital I/O pin
B43	GPIO_18	IO	General-purpose digital I/O pin
B4	GPIO_20	IO	General-purpose digital I/O pin
B44	GPIO_21	IO	General-purpose digital I/O pin
B28	GPIO_22	IO	General-purpose digital I/O pin
A39	GPIO_23	IO	General-purpose digital I/O pin
A40	GPIO_24	IO	General-purpose digital I/O pin
A41	GPIO_27	IO	General-purpose digital I/O pin
B31	GPIO_30	IO	General-purpose digital I/O pin
B30	GPIO_31	IO	General-purpose digital I/O pin
B16	GPIO_32	IO	General-purpose digital I/O pin
B29	GPIO_33	IO	General-purpose digital I/O pin
B15	GPIO_34	IO	General-purpose digital I/O pin
B14	GPIO_35	IO	General-purpose digital I/O pin
B41	GPIO_38	IO	General-purpose digital I/O pin
B42	GPIO_39	IO	General-purpose digital I/O pin
B34	GPIO_46	IO	General-purpose digital I/O pin
B18	GPHY_RST	IO	General-purpose digital I/O pin (1Gbit external PHY reset)
B17	GPHY_INTn	IO	General-purpose digital I/O pin (Wake-on-LAN interrupt)
A31	RESIN_N	I	General-purpose digital I/O pin (Hardware reset)
A52	GPIO28_UART_RX	IO	General-purpose digital I/O pin (UART receiver line)
A51	GPIO29_UART_TX	IO	General-purpose digital I/O pin (UART transmitter line)
B19	GPIO36_MDC	IO	General-purpose digital I/O pin (Management data clock)
B20	GPIO37_MDIO	IO	General-purpose digital I/O pin (Management data I/O)
A38	PCIE_RST_L_OUT	IO	General-purpose digital I/O pin (PCIE reset connection)

TABLE 2-9. PIN STATUS ON BOOT

Pin #	Pin name and/ or function	Pin name or alt function	Voltage	Internal Pull-down(PD)/ Pull-up(PU)	Description
B45	GPIO_9	-	1.8V	PD	0: Reserved 1: Reserved
A20	GPIO_10	SPI_CLK	1.8V	PD	Auth enable: 0: No auth. (default) 1: Auth is required
A22 B44	GPIO_11 GPIO_21	SPI_MOSI	1.8V	PD	Boot up interface select: 00: SPI NOR (default) 01: Reserved 10: QSPI (4bit) 11: Reserved
A48	GPIO_15	-	1.8V	PD	Use serial Num: 0: Use serial Num 1: Use OEM ID
B43	GPIO_18	-	1.8V	PD	JTAG_boot_en: 0: Used as normal function GPIO 1: Used as JTAG
B31	GPIO_30	-	1.8V	PD	Watchdog enable: 0: Watchdog enable 1: Watchdog disable
B14	GPIO_35	-	1.8V	PD	Hash in fuse (SW use only): 0: PK hash is stored in boot ROM 1: PK hash is stored in OTP
B42	GPIO_39	-	1.8V	PD	Boot ROM boot speed: 0: 24MHz (default) 1: 400MHz
A38	GPIO_40	PCIE reset connection	1.8V	PD	TCXO_mode: 0: XO-mode 1: TXCO-mode
B34	GPIO_46	-	1.8V	PD	RFA REFCLK frequency selection: 0: 45MHz 1: 96MHz

NOTE: These pins are for booting the device, use them cautiously.

3. Electrical characteristics

TABLE 3-1. POWER SUPPLY DC CHARACTERISTICS

Symbol	Parameter	Minimum	Typical	Maximum	Units
+3V3	3.3 V Supply voltage	3	3.3	3.6	V
+1V95	1.95 V Output voltage for the ethernet transformer	1.9	1.95	2.05	V

TABLE 3-2. TEMPERATURE LIMIT RATINGS

Parameter	Minimum	Maximum	Units
Storage Temperature	-65	+150	°C
Commercial Operating Temperature	0	+65	°C
Humidity	10	90	%RH
Storage humidity	5	90	%RH

4. Power management

TABLE 4-1. POWER CONSUMPTION

DBS			Voltage V	Current A	Total power W
TX	2x2	MCS0	5	1.31	6.55
		MCS11	5	1.11	5.55
		Throughput at 440Mbps	5	1.2	6

5. Radio characteristics

TABLE 5-1. 2.4 GHZ 802.11AX 20 MHZ RADIO CHARACTERISTICS PER CHAIN

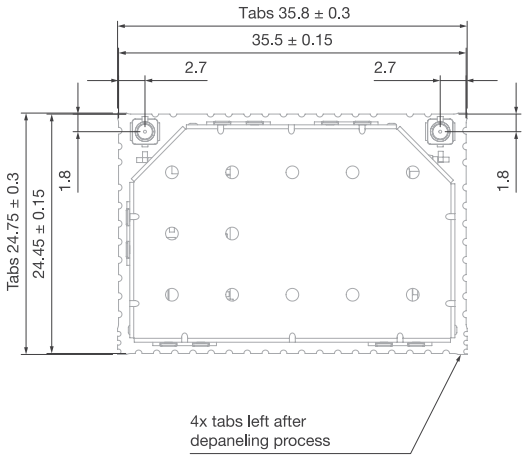
	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9	MCS10	MCS11
Data rate (Mbps)	17.2	34.4	51.6	68.8	103.2	137.6	154.9	172.1	206.5	229.4	258.1	286.8
TX power (dBm)	22	20	18	18	17	17	16	16	16	16	16	15
RX sensitivity (dB)	-94	-90	-88	-85	-82	-77	-76	-74	-70	-68	-65	-63

TABLE 5-2. 2.4GHZ 802.11AX 40MHZ RADIO CHARACTERISTICS PER CHAIN

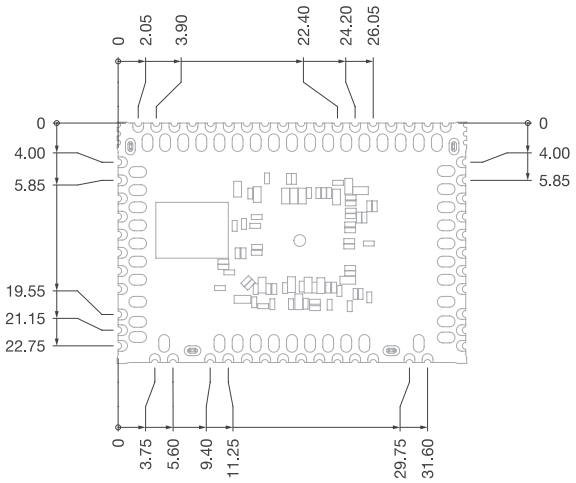
	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9	MCS10	MCS11
Data rate (Mbps)	17.2	34.4	51.6	68.8	103.2	137.6	154.9	172.1	206.5	229.4	258.1	286.8
TX power (dBm)	22	20	18	18	16	16	16	16	16	15	15	15
RX sensitivity (dB)	-92	-88	-85	-82	-79	-74	-73	-71	-67	-65	-62	-59

6. Mechanical characteristics

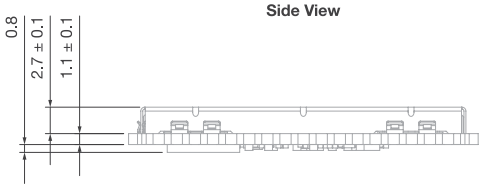
Top View



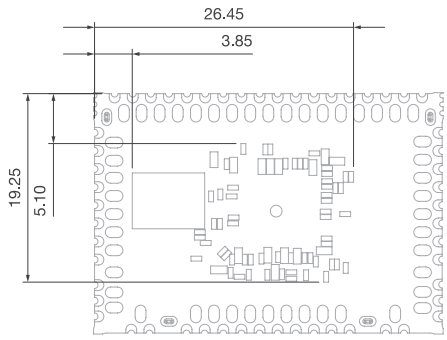
Bottom View



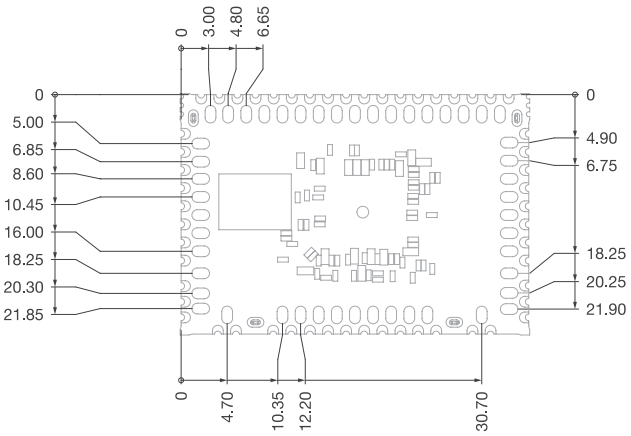
Side View



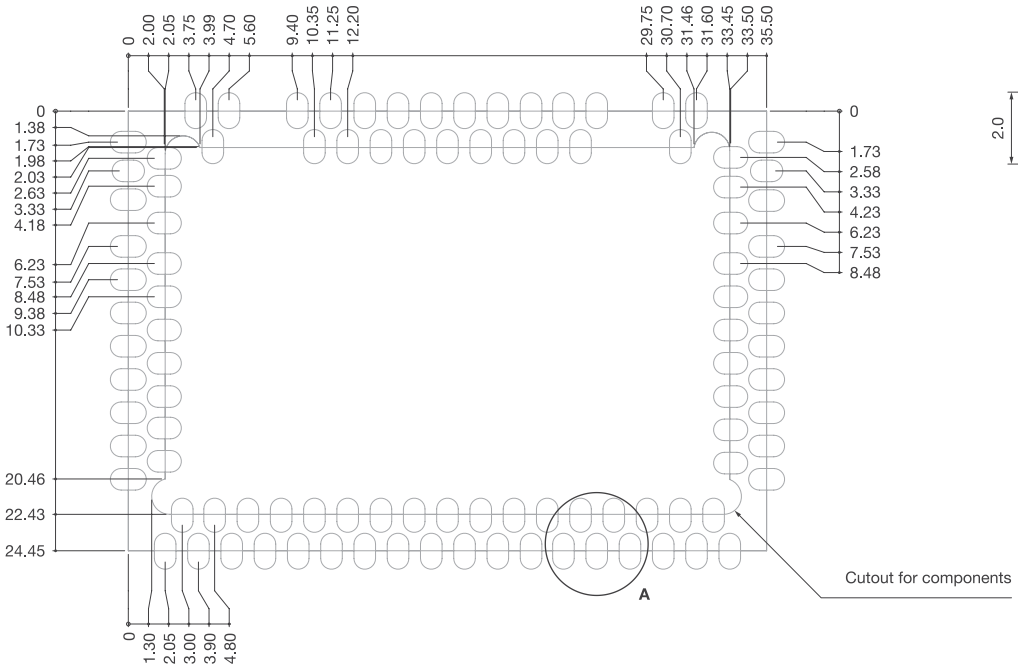
Bottom View

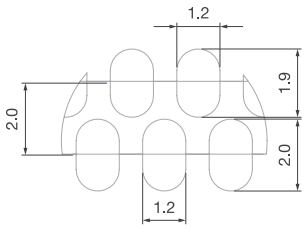


Bottom View



7. PCB footprint





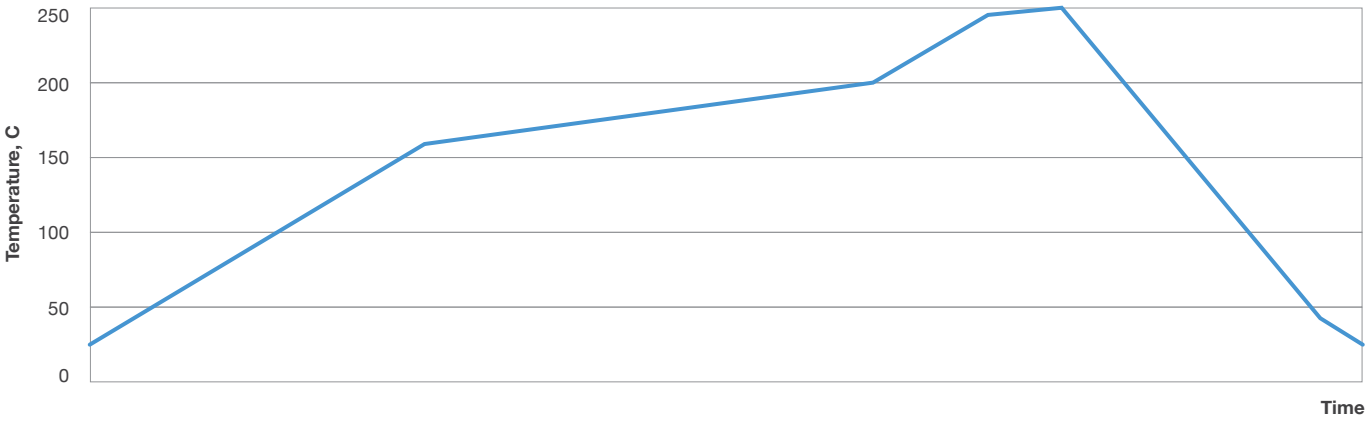
DETAIL A
SCALE 10 : 1

8. Reflow profile recommendations

8.1. REFLOW PROFILE PARAMETERS

Reflow profile recommendation	
Ramp up rate	3°C/second max
Maximum time maintained above 217°C	120 seconds
Peak temperature	250°C
Maximum time within 5°C of peak temperature	20 seconds
Ramp down rate	6°C/second max

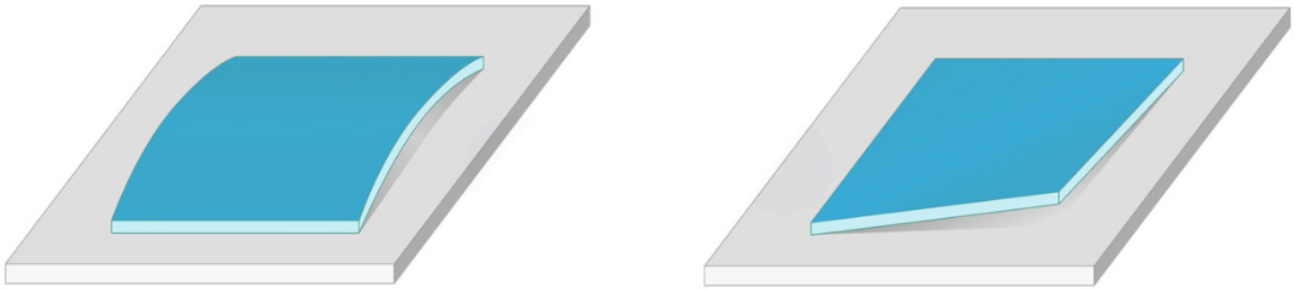
8.2. REFLOW PROFILE



9. Laminate Conditions

8devices modules are manufactured according to the standard IPC-A-610 Norm Class 2. Standard states: “Bow/twist after solder should not exceed 1.5% for through-hole and 0.75% for surface mount printed board applications”. According to this statement, Cherry module can be bowed and twisted up to 0.269mm. To avoid negative effects of bow and twist we recommend to increase the paste thickness for the module pads to achieve better co-planarity.

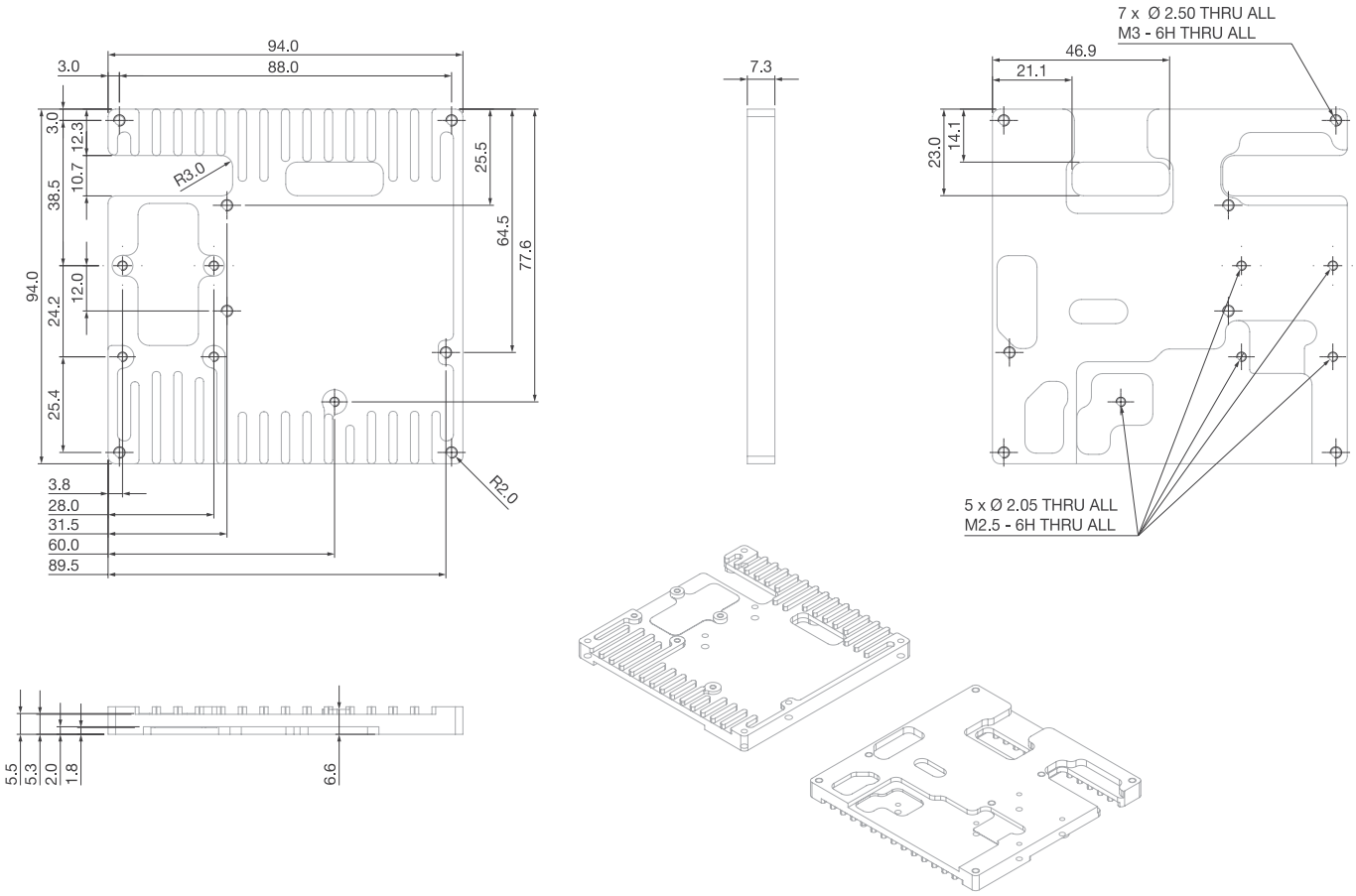
FIGURE 9-1. EXAMPLE OF BOW AND TWIST



Bow **Twist**

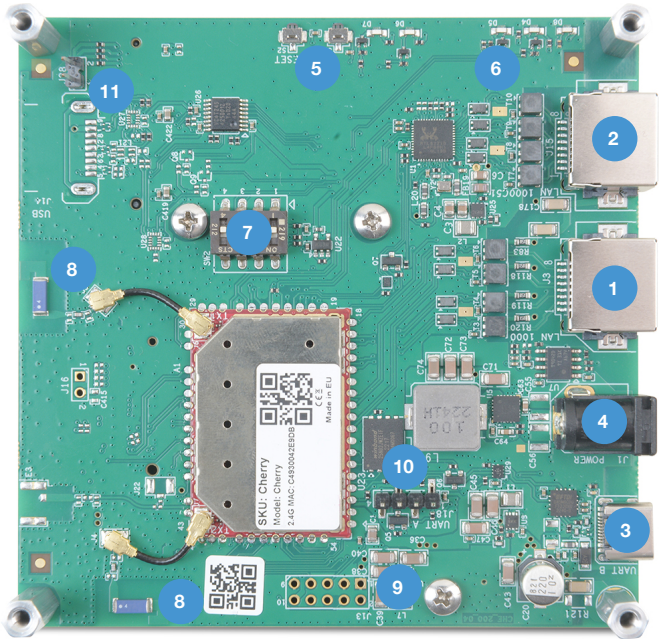
10. Thermal considerations

Because of a higher power consumption, it is mandatory to use heatsink together with the Cherry module to avoid overheating issue or permanent module damage.
It is recommended to use a heatsink with at least of 90cm^2 of the effective surface area (fins area).

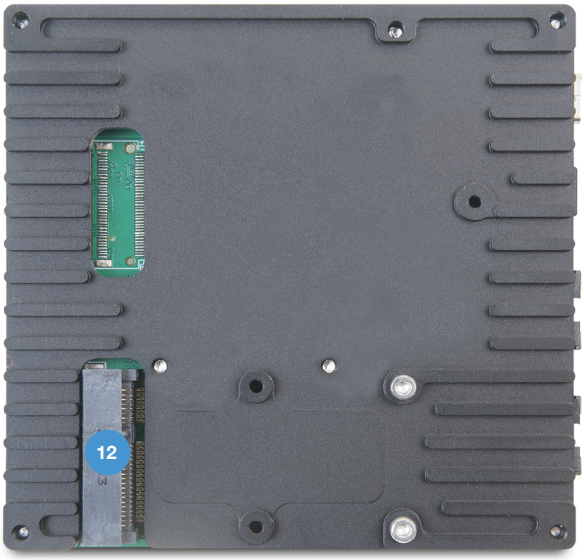


11. Development Board

11.1. DEVELOPMENT KIT INTERFACES

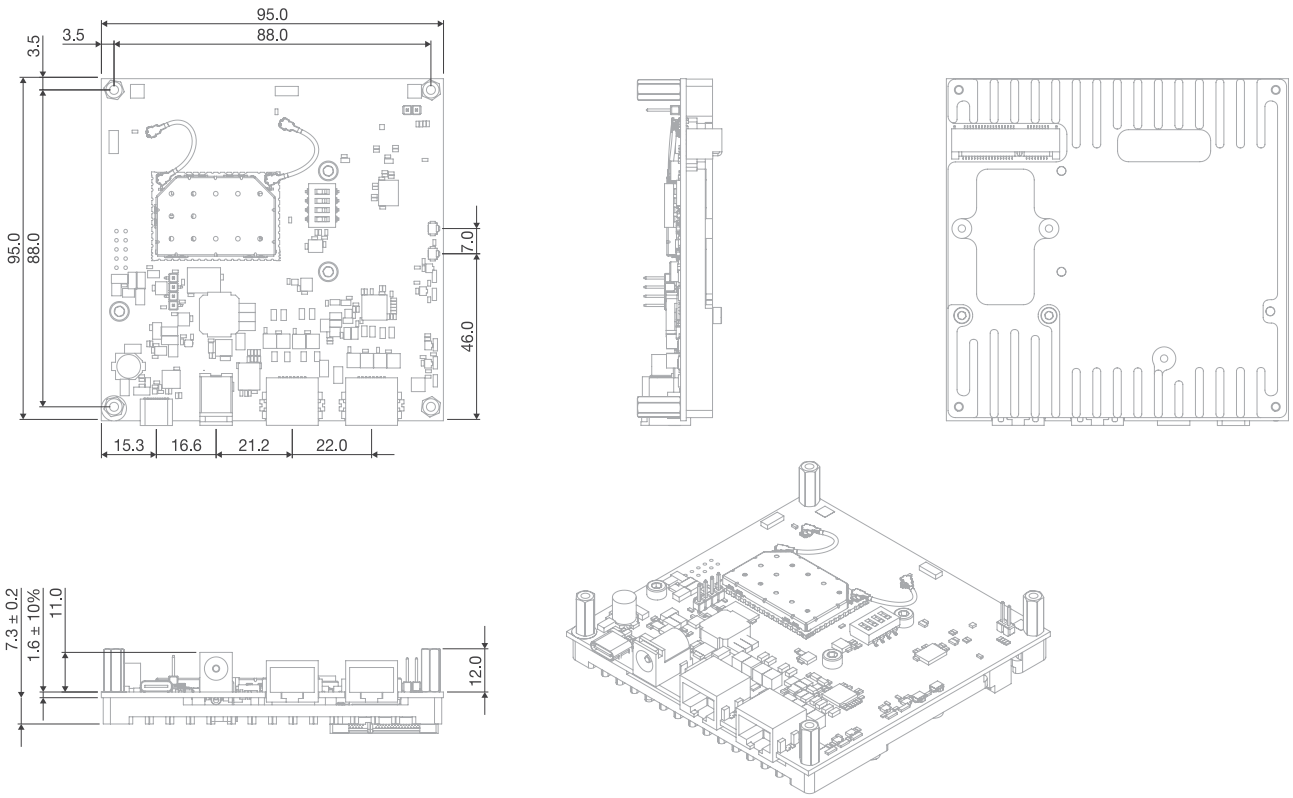


1. 1Gbps Ethernet port
2. 2.5Gbps Ethernet port
3. USB Type C socket (console + power)
4. DC power jack (12V-24V)
5. Switches (Refer to datasheet 11.3)
6. LEDs (Refer to datasheet 11.4)
7. Bootstrap switch (Refer to datasheet 11.5)
8. Antennas (Wi-Fi 2.4GHz)
9. GPIOs (Refer to datasheet 11.6)
10. UART connector (Refer to datasheet 11.5 Note)
11. PCIe +5V connector (Refer to datasshet 11.7)

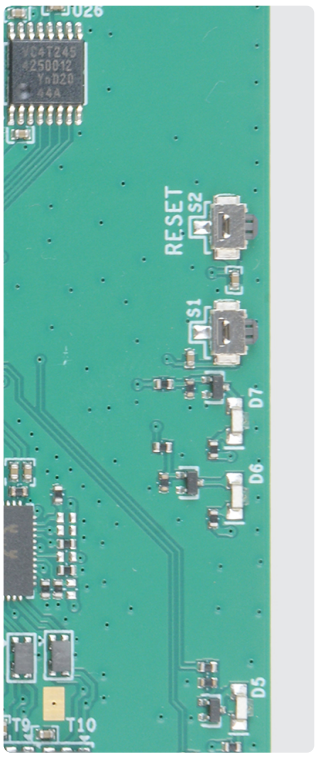


12. Mini-PCIe connector (single lane, PCIe 2.0)

11.2. DEVELOPMENT KIT DIMENSIONS



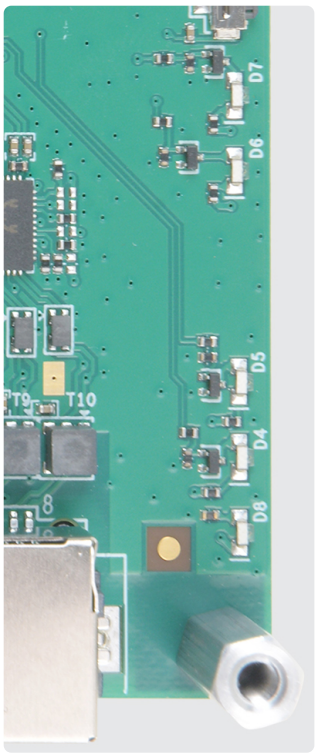
11.3. SWITCHES



S2 – Reset;

S1 – GPIO22.

11.4. LEDS



D7 – GPIO38

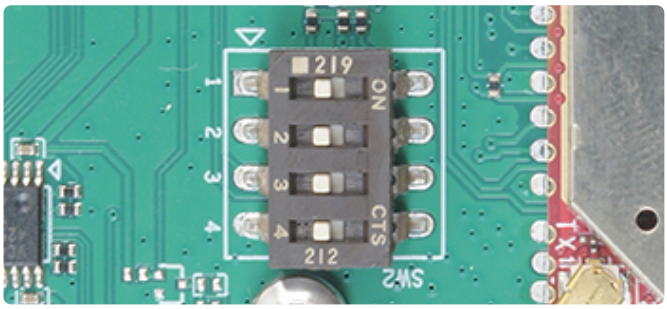
D6 – GPIO33

D5 – GPIO24

D4 – GPIO23

D8 – Power

11.5. BOOTSTRAP SWITCH

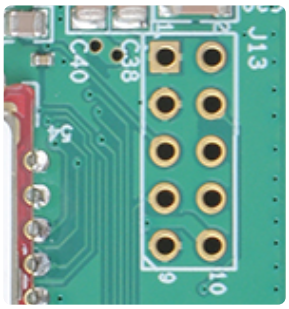


Config	1	2	3
Boot from SPI NOR	0	0	0
Boot from QSPI	0	1	0
Reserved	0	0	1
Reserved	1	1	1

Note. Pin 4 UART selector. OFF - UART through USB C. ON - UART through header.

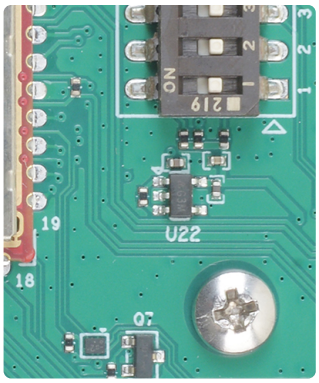
11.6. GPIOS

1 – GND
2 – 1.8V
3 – GND
4 – GPIO31
5 – GPIO20



6 – GPIO39
7 – GPIO27
8 – GPIO46
9 – GND
10 – 3.3V

11.7. PCIE +5V CONNECTOR



To allow +5V to go into PCIe pins: 45, 47, 49, 51, this header must be shorted out.

12. Cherry packaging and ordering info

Cherry modules are packing into trays. Each tray fits 25 modules. Every 5 trays are vacuum sealed and one standard packaging box contains 625 modules.

FIGURE 12-1. CHERRY TRAY DIMENSIONS

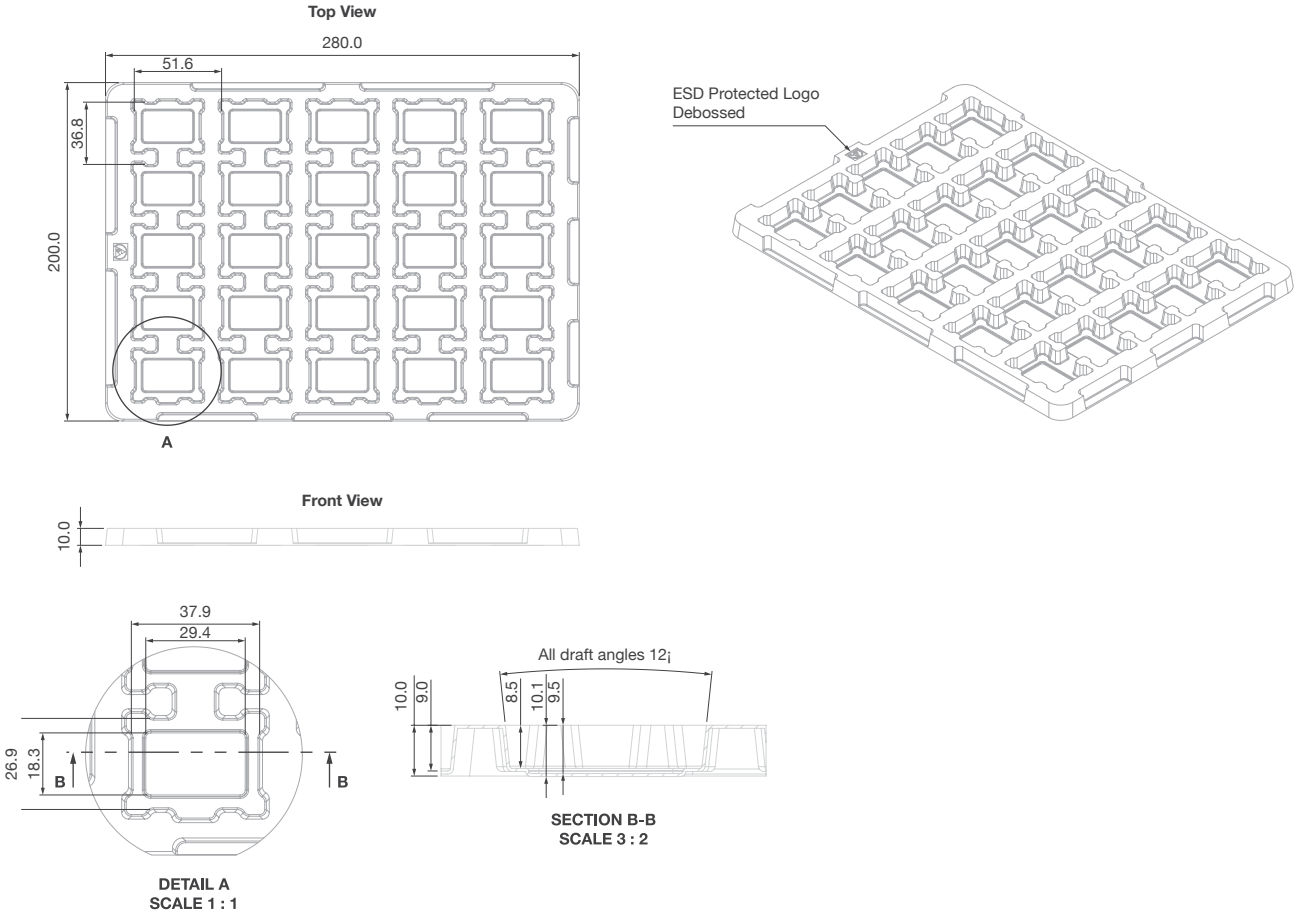
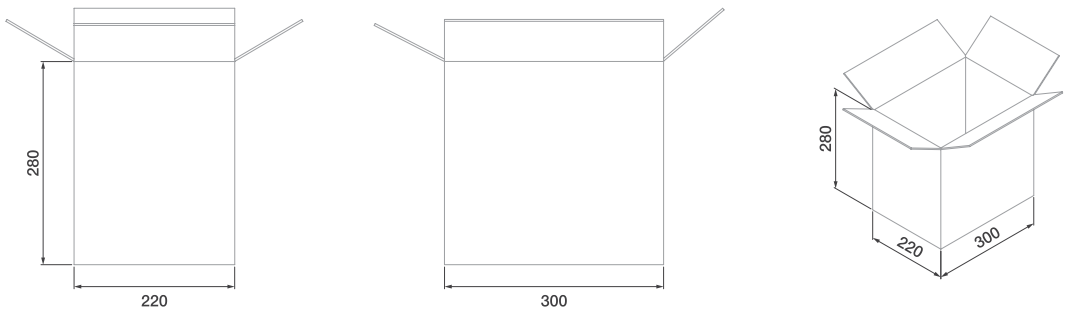


FIGURE 12-2. STANDARD PACKAGING BOX DIMENSIONS



13. Document Revision History

Revision	Revision Date	Description
v1.0	2023-02-15	Initial release
v1.1	2023-06-06	Updated information about development board
v1.2	2023-10-18	Updated DVK photos and drawings
v1.3	2024-01-02	SPI_CLK and SPI_CS1 Pin ID correct