

# Guidelines for CoolSiC™ MOSFET gate drive voltage window

## About this document

Infineon strives to enhance electrical systems with comprehensive semiconductor competence. This expertise is revealed in the products themselves and their behavior under relevant use conditions, and also in the sharing of knowledge on the latest semiconductor technologies. For new technologies such as the silicon carbide (SiC) MOSFET, this is of particular importance, since a SiC MOSFET under certain operating conditions shows different characteristics compared to silicon (Si) switches. Moreover, experience with this new technology and accompanying literature is not available to the public to the same extent as for other technologies that have been on the market for a long time.

One important aspect to be considered for the SiC MOSFET is the drift of gate threshold voltage ( $V_{GS(th)}$ ) under long-term operation.

The bias-temperature-instability (BTI) effects caused by continuous bias at the gate have been well studied. In addition, a second, dynamic component has been revealed. This is related to a drift of  $V_{GS(th)}$  which mainly depends on the switching frequency and the selected gate-source voltage for turn-off ( $V_{GS(off)}$ ). It is necessary to adjust the operating parameters with respect to the  $V_{GS}$  operating window according to potential drift effects.

## Scope and purpose

- To explain the long-term behavior of  $V_{GS(th)}$  under switching operation
- To discuss its impact on the application
- To provide design guidelines to limit the related increase of on-state resistance  $R_{DS(on)}$  as the major implication for the user in the application

## Intended audience

Development, design and qualification engineers working with CoolSiC™ MOSFETs.

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## V<sub>GS(th)</sub> drift phenomenon

### 1 V<sub>GS(th)</sub> drift phenomenon

The nature of the wide-bandgap material SiC and the different properties of the semiconductor-dielectric interface compared to silicon material cause some natural peculiarities in threshold voltage variation and bias-temperature instability (BTI), which need to be understood and assessed. Extensive investigations have been conducted with the target to understand such differences, to explain their relation to the semiconductor material, to clarify their relevance for the application, and to define their consequences with respect to specification and system design.

As far as static gate-bias stress is concerned, the standard test procedures typically used to characterize threshold voltage and threshold voltage drifts for Si devices need to be adapted for SiC MOSFETs. Based on these findings, a new measure-stress-measure procedure has been developed for the BTI evaluation of SiC MOSFETs, which allows one to distinguish between reversible threshold voltage hysteresis and more permanent threshold voltage drift (BTI). This measurement technique has been used for an in-depth study assessing the V<sub>GS(th)</sub> stability of recently launched SiC MOSFET parts. It has been demonstrated that the Infineon CoolSiC™ MOSFET excels in overall V<sub>GS(th)</sub> stability, in particular due to a very low negative BTI and a very narrow drift variation among different devices[1].

Besides the drift driven by static stress, the threshold voltage of SiC MOSFET devices may undergo an additional drift triggered by switching events (turn-on and turn-off of the device). This additional component can only be identified in long-term switching tests. Based on the current knowledge, the effect is related to gate-oxide trap dynamics. More details will be discussed in upcoming scientific papers. This effect is a general characteristic of the current SiC MOSFET technologies as related internal studies have shown. It is not limited to Infineon CoolSiC™ MOSFET devices.

The characteristics of this phenomenon for Infineon CoolSiC™ MOSFET have been studied by performing long-term tests under various switching conditions. The data shows that switching stress leads to a slow V<sub>GS(th)</sub> increase over time. However, irrespective of the parameters chosen, a negative switching-induced V<sub>GS(th)</sub> drift has never been observed. The V<sub>GS(th)</sub> drift value is similar among different devices, which have been stressed at the same operation conditions. The increase of V<sub>GS(th)</sub> causes a slight increase in R<sub>DS(on)</sub>, which translates into increased on-state losses over time.

Please note that the basic function of the device is not affected, in particular:

- the blocking capability is not affected
- the reliability level of the devices is not affected, e.g. cosmic radiation robustness, humidity ruggedness, etc.
- the V<sub>GS(th)</sub> drift has a negligible effect on the total switching losses

Key parameters that influence the switching-induced V<sub>GS(th)</sub> drift include:

- the number of switching events, which translates into switching frequency and total operation time
- gate drive voltage, mainly V<sub>GS(off)</sub>
- the overshoot and undershoot of the gate-source terminal directly at the chip

The following operation parameters were found to have minor or negligible impact on the switching-induced V<sub>GS(th)</sub> drift:

- junction temperature
- switching slopes (dV/dt and dI/dt)
- drain-source voltage
- drain current

Impact on the application

## 2 Impact on the application

The major impact of the  $V_{GS(th)}$  drift is a long-term increase of the  $R_{DS(on)}$  for the chosen  $V_{GS}$  in the application. Generally, the increase of  $R_{DS(on)}$  increases the conduction losses leading to an increase in junction temperature  $T_j$  over time. This increase of  $T_j$  over time should also be considered during the assessment of power cycling.

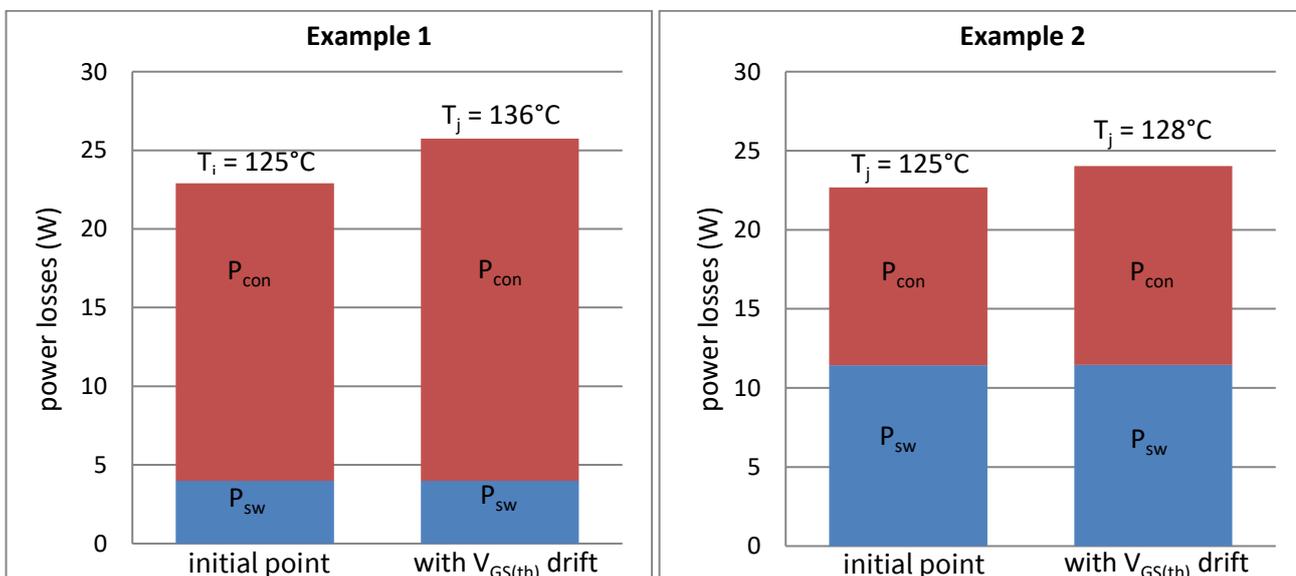
Whether the  $T_j$  increase is critical or not depends on the individual applications and the used operating conditions. In many cases the impact is minor and leads to a negligible increase in  $T_j$  even after 20 years' lifetime. Other applications might be more critical. Therefore, the design guideline shown in Chapter 3 must be considered.

Below, two examples (half-bridge configuration in a DC-AC-inverter) illustrate the varying impact of a given, fixed-amplitude  $V_{GS(th)}$  drift on different applications. The first example represents applications where the conduction losses ( $P_{con}$ ) dominate the losses distribution. The second example considers an application in which switching losses ( $P_{sw}$ ) and conduction losses contribute equally. The parameters of the two examples are listed in Table 1.

**Table 1 Parameters of two examples**

	Example 1: conduction losses dominating	Example 2: conduction losses and switching losses equally distributed
Switching frequency (kHz)	8	30
Nominal current (A)	50	38.5
Output voltage (V)	400	400
Output frequency (Hz)	50	50
DC link voltage (V)	600	600
Power factor	1	1
Thermal resistance (K/W)	3.6	3.6
Ambient temperature( °C )	40	40

For each example, the effects of a  $V_{GS(th)}$  drift on the losses distribution and the junction temperature are shown in Figure 1. Both examples have the same  $V_{GS(th)}$  drift of 1 V, which could be expected at the end of the lifetime.



**Figure 1 Examples of  $V_{GS(th)}$  drift impacts on applications**

### Impact on the application

As seen from example 1, in which conduction losses dominate, a  $V_{GS(th)}$  drift leads to notably higher total losses and thus to higher junction temperatures. For those applications, the design guidelines detailed in Chapter 3 must be considered. For the application with balanced switching and conduction losses, a  $V_{GS(th)}$  drift will only have a minor effect on the total losses and the junction temperature. In other applications in which the overall losses are dominated by the dynamic losses, the impact of the  $V_{GS(th)}$  drift is nearly negligible.

Gate drive voltage guidelines

### 3 Gate drive voltage guidelines

By limiting the gate voltage for turn-off ( $V_{GS(off)}$ ), the  $V_{GS(th)}$  drift can be constrained to a range that is acceptable for applications. The upper limit of the turn-off gate voltage is 0 V for all conditions, while the lower limit should be chosen depending on the turn-on voltage, the switching frequency and the total operation time, to limit the  $R_{DS(on)}$  increase to an acceptable range.

#### 3.1 Guidelines

The dynamic drift of the  $V_{GS(th)}$  increases with the number of switching events. For an easy understanding, the total number of switching events is translated into a normalized switching frequency considering 10 years of full operation (24h/7d). With the known actual switching frequency  $f_{sw}$  in kHz, the target lifetime in years, and the operation time in percentage of the total system lifetime, a normalized switching frequency is defined by the following formula:

$$\text{Normalized } f_{sw} = \text{actual } f_{sw} \text{ [kHz]} \times \text{lifetime [yrs.]} \times \text{operation time in percentage [\%]} \div 10 \text{ [yrs.]}$$

The recommended operating area provided by Infineon is separately given for CoolSiC™ MOSFETs in module and in discrete packages despite the fact that the basic chip technology is the same. It is because over- and undershoots in the gate signal are strongly dependent on operation conditions, circuit design and parasitics. In particular, the recommended operating area (ROA) for discrete devices is more conservative due to much more flexibility in circuit design, application conditions, inverter topology, gate-drive design, PCB layout and thermal design. For these reasons, the ROA of discrete devices also includes a potential overshoot of 2 V to account for variabilities in gate-driver design. For modules, no extra overshoot needs to be considered, since 0 V overshoot can be achieved in any case by proper gate-driver design.

With the estimated normalized switching frequency based on the actual application, the minimum turn-off gate voltage including a potential undershoot can be extracted from Figure 2 and Figure 3, respectively for discrete and module products.

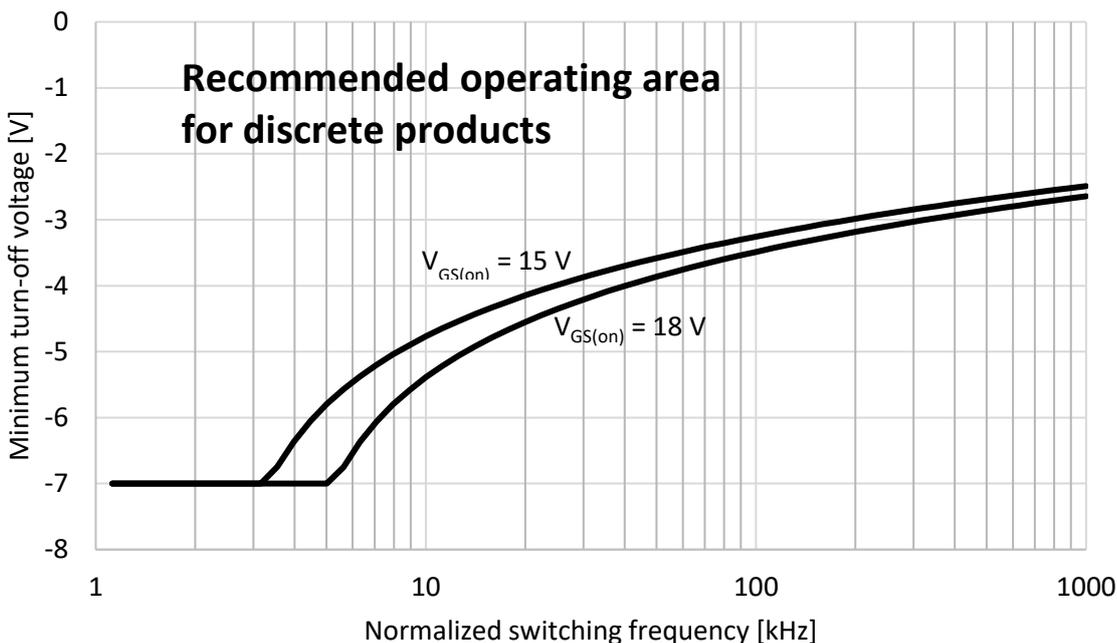
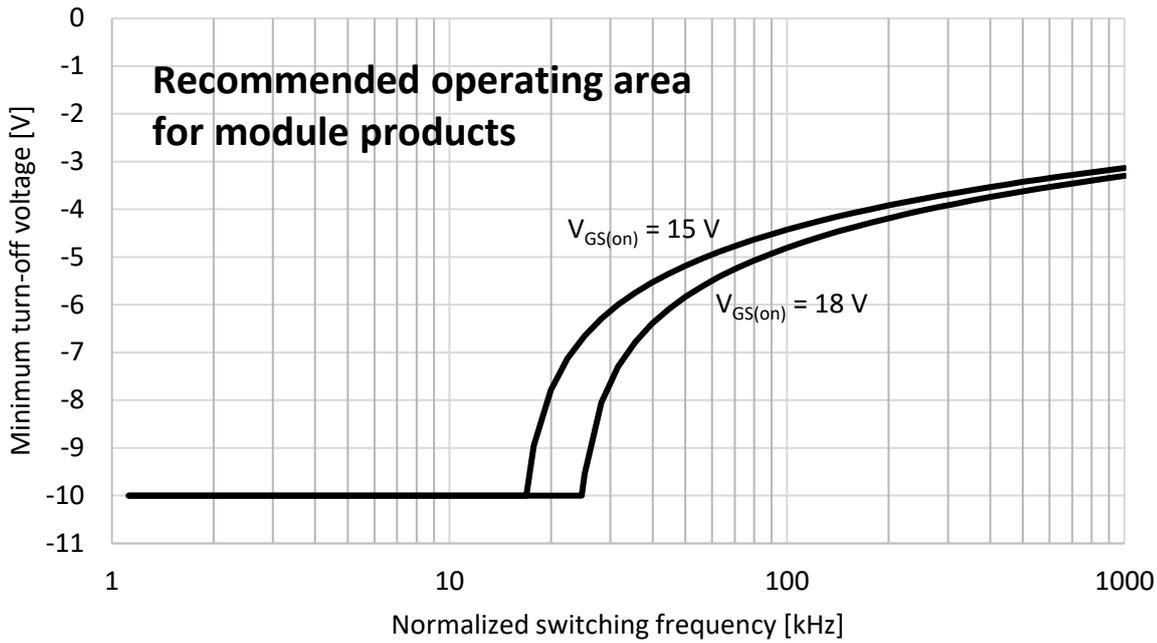


Figure 2 Minimum turn-off gate voltage for discrete package products

## Gate drive voltage guidelines



**Figure 3 Minimum turn-off gate voltage for module products**

How to use this information is explained in the following example. A solar inverter has:

- an actual switching frequency of 20 kHz
- a targeted lifetime of 20 years
- operation time of 50%
- a normalized switching frequency of  $20 \text{ kHz} * 20 \text{ yrs.} * 50\% / 10 \text{ yrs.} = 20 \text{ kHz}$

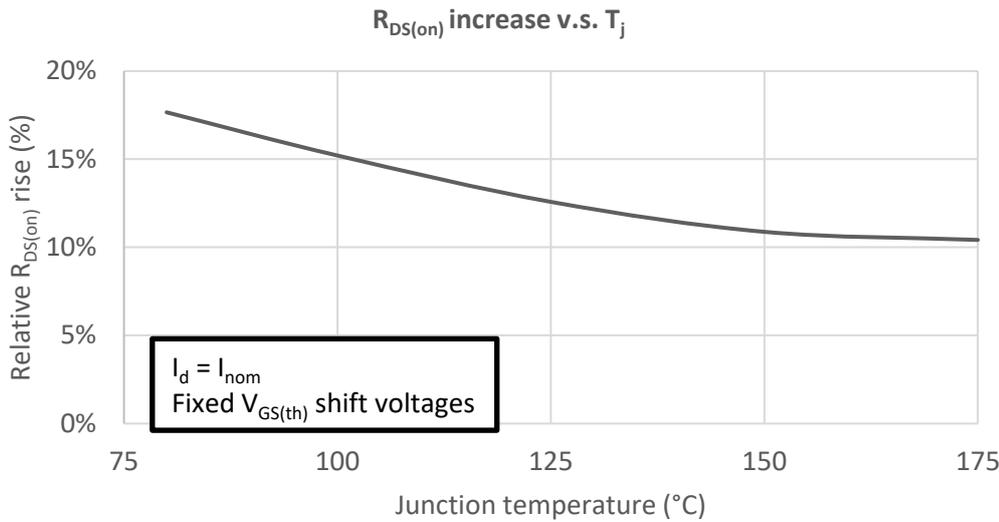
For a turn-on voltage of 18 V, using CoolSiC™ MOSFETs in discrete packages, the turn-off gate voltage including undershoot has to be between -4.6 V and 0 V, as can be seen in Figure 2. For a turn-on voltage of 15 V, using CoolSiC™ MOSFET modules, the turn-off gate voltage including undershoot has to be designed between -7.7 V and 0 V (see Figure 3).

### 3.2 Definition of the recommended operating area

The minimum turn-off voltage which defines the recommended operating area is set to ensure that the  $R_{DS(on)}$  increase at  $I_{nom}$  and  $T_j=125^\circ\text{C}$  will not exceed 15% of the initial value during the entire product lifetime.

The relative increase of  $R_{DS(on)}$  depends on the operating current  $I_d$  and junction temperature  $T_j$  (see Figure 4).

## Gate drive voltage guidelines



**Figure 4** Relative  $R_{DS(on)}$  increase at different junction temperatures

As a final remark, please note that independent of the ROA, the lowest peak gate voltage must never exceed the maximum ratings in the data sheet.

### 3.3 Definition of the gate-voltage overshoot and undershoot

The  $V_{GS(th)}$  drift is a long-term effect, therefore only the repetitive overshoot and undershoot should be considered. An overshoot and undershoot of the gate voltage caused by non-standard operating conditions, e.g. power-grid instability, short-circuit conditions, etc. should not be considered.

The overshoot and undershoot is only critical for  $V_{GS(th)}$  drift if the spikes reach the gate- source terminals directly at the chip. To quantify them experimentally, over- and undershoots would ideally be measured directly at the chip terminals. However, since this is not always possible, the following guidelines provide a good estimation:

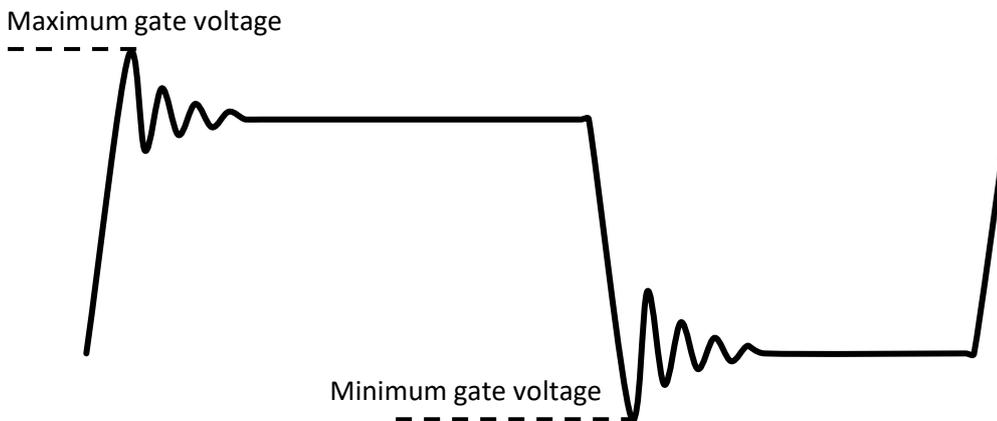
- Use a direct probe with high bandwidth (100 MHz) if isolation is not required
- Alternatively use a differential probe with high bandwidth and high common-mode rejection capability if isolation is required
- Always try to measure as close to the chip as possible, as shown in Figure 5



**Figure 5** Example of gate voltage measurement points

## Gate drive voltage guidelines

The shape of the gate voltage overshoot and undershoot may vary between individual inverter designs. The peak voltage should be considered, as shown in Figure 6.



**Figure 6** Gate voltage overshoot and undershoot

### 3.4 Notes for 18 V turn-on voltage

CoolSiC™ MOSFET could be used with 18 V gate voltage, for better current handling capability.

Please note, a turn-on gate voltage higher than 15 V has two opposing effects:

- it reduces the typical  $R_{DS(on)}$  and also the sensitivity of  $R_{DS(on)}$  to  $V_{GS(th)}$  drift
- the  $V_{GS(th)}$  drift may be higher than 15 V at the end of life, however, the  $R_{DS(on)}$  increase will be lower due to the larger overdrive.

It should also be considered that the short-circuit peak current is much higher compared to the 15 V turn-on voltage. Therefore the short-circuit capability of the device, as stated in the data sheet for a turn-on voltage of 15 V, will be lost at 18 V turn-on voltage.

### 3.5 Notes for less negative turn-off voltage

When operating at a less negative turn-off gate voltage (e.g. -2 V instead of -5 V), the impact on the application is minor. Several application-relevant parameters should be considered however:

- $E_{on}$  and  $E_{off}$  will change slightly
- The forward voltage of the SiC MOSFET body diode will be reduced
- Increased risk of parasitic turn-on, which could increase the turn-on losses. This is especially relevant with the combination of 0 V turn-off voltage, large turn-off gate resistance and large gate-source loop inductance.

It should be emphasized that the discrete CoolSiC™ MOSFET products can be safely operated with a designed turn-off voltage of 0 V. Thus, the values in the guidelines do not have a negative impact on the performance. Furthermore, it even enables a less complex, unipolar gate-driver circuit design. For CoolSiC™ MOSFET modules with single-switch topologies like booster circuits, a turn-off with 0 V at the gate is also generally possible.

[1] T. Aichinger, G. Rescher, G. Pobegen: Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs; Microelectronics Reliability 80 (2018) 68–78.

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## Revision history

### Revision history

Document version	Date of release	Description of changes
1.0	2018-05-28	Initial version
1.1	2019-05-06	Including the undershoot/overshoot in the ROA, and modify corresponding wording

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