Nisshinbo Micro Devices Inc.

NB7140ZA Series

1-cell Li-ion Battery Protection IC with Forced Standby and Built-In System Reset Function

FEATURES

- Supply Current
  Normal mode: Typ. 1.50 μA / Max. 3.00 μA
  Forced standby mode: Max. 0.04 μA
  Standby mode: Max. 0.20 μA
  (V_{DET2}: Auto release type)
  Max. 0.04 μA
  (V_{DET2}: Latch 1/2 type)
- Detector Selectable Range and Accuracy
  Overcharge detection voltage (V_{DET1}):
  4.2 V to 4.7 V, ±15 mV
  Overdischarge detection voltage (V_{DET2}):
  2.1 V to 3.2 V, ±35 mV
  Discharge overcurrent detection voltage 1 (V_{DET31}):
  0.0050 V to 0.0300 V, ±1.0 mV
  0.0305 V to 0.0500 V, ±1.5 mV
  Discharge overcurrent detection voltage 2 (V_{DET32}):
  0.0110 V to 0.0600 V, ±2 mV
  0.0605 V to 0.1000 V), ±4.0 %
  Charge overcurrent detection voltage (V_{DET4}):
  –0.0050 V to –0.0300 V, ±1.0 mV
  –0.0305 V to –0.0500 V, ±1.5 mV
  Short-circuit detection voltage 1 (V_{SHORT1}):
  0.030 V to 0.120 V, ±4.0 mV
  0.121 V to 0.200 V, ±5.0 mV
- 0 V Battery Charging selectable: Permission / Inhibition
- 0 V Battery Charging Inhibition Voltage (V_{NOCHG}):
  1.000 V to 2.500 V, ±4.0 %
- Overcharge Release Type selectable:
  Auto Release / Latch
- Overdischarge Release Type selectable:
  Auto Release / Latch 1 / Latch 2
- Discharge Overcurrent Release Type selectable:
  Auto Release1 (V- = V_{DD} × 0.8 V) /
  Auto Release2 (V- = 0.070 V) /
  Latch (At charger connection)
- Discharge Overcurrent Detection Voltage 2 (V_{DET32})
  selectable: Available / Unavailable
- Reset Detection Timing selectable:
  1st Step / 2nd Step
- Reset Release Type selectable:
  Auto Release / V- rising

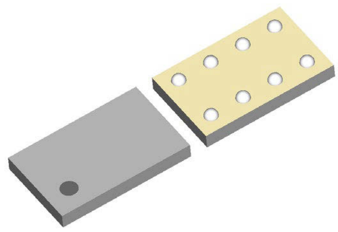
APPLICATIONS

Hearable / Wearable devices,
Smart Phone,
Handheld Data Terminals

GENERAL DESCRIPTION

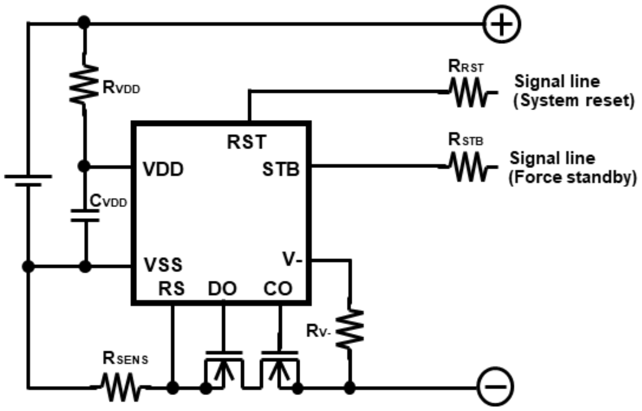
The NB7140ZA is a 1-cell Li-ion / polymer battery protection IC which provides over-charge, over-discharge, charge / discharge overcurrent and short circuit protection, with built-in system reset function.
The NB7140ZA can shift to the Forced Standby Mode by an external signal to STB pin to reduce own current consumption.

Low voltage and high accuracy overcurrent detection achieves a heat reduction on board by using low sense resistor. Low operating current and standby current can prolong the battery life even when its capacity is small, and the forced standby mode with STB pin too can prolong the small battery life.
System reset is possible by turning off the charge FET / discharge FET during MCU runaway with the RST pin.



WLCSP-8-P10
1.6 × 1.0 × 0.3 [mm]

TYPICAL APPLICATION CIRCUIT



NB7140ZA Application Circuit for 1st Step Reset Detection

PRODUCT NAME INFORMATION

NB7140 ZA * * * E2 S**

aa bbb c d ee f

Description of configuration

Suffix	Item	Description
aa	Package code	Indicates the package code.
bbb	Specific option code	Indicates a three-digit number code that combined set voltages. Refer to the table of set voltages for details.
c		Indicates a delay time code. Refer to the table of delay times for details.
d		Indicates a function code. Refer to the table of functions for details.
ee	Packing	Indicates the taping code of the package. Refer to *Packing Specification* in the appendix *Package Information* for details.
f	Grade	Indicates the quality grade. Refer to the table of grade for details.

Table of set voltages (bbb)

Symbol	V_{DET1}	V_{REL1} [*1]	V_{DET2}	V_{REL2} [*1]	V_{DET31} [*2]	V_{DET32} [*2]	V_{DET4}	V_{SHORT1} [*2]	V_{NOCHG}
Voltage Range (Step) [V]	4.2 to 4.7 (0.005)	4.0 to 4.7 (0.005)	2.1 to 3.2 (0.005)	2.3 to 3.6 (0.005)	0.0050 to 0.0500 (0.0005)	0.0110 to 0.1000 (0.0005)	−0.0050 to −0.0500 (0.0005)	0.030 to 0.200 (0.001)	1.000 to 2.500 (0.05)

[*1] Under the following conditions,
V_{REL1}: $V_{DET1} - V_{REL1} = 0.400$ V (Max.)
V_{REL2}: $V_{REL2} - V_{DET2} = 0.700$ V (Max.)

[*2] When selecting each set voltage of V_{DET31}, V_{DET32} and V_{SHORT1}, keep from overlapping among them in consideration of their output voltage accuracy. Especially, V_{SHORT1} should be higher than 10 mV from V_{DET31} and V_{DET32}.

Table of delay times (c)

Symbol	t_{VDET1}	t_{VREL1}	t_{VDET2}	t_{VREL2}	t_{VDET31} [*1]		t_{VDET32}	t_{VREL3}	t_{VDET4}	t_{VREL4}	t_{SHORT}	t_{STBD}	t_{STBR}	t_{RST1}	t_{RST2}	t_{RSTR}
					type A	type B										
Time [ms]	1024	16	32 64 128	1.05	1024.0 2048.0 3072.0 4096.0	12.5 16.5 1024.0 4096.0	7.5 12.5 16.5	9.0	10 17	4	0.28	50 300	4.5 8.5 33.0	48 100	4.5	200 512
A	1024	16	64	1.05	1024.0		16.5	9.0	17	4	0.28	300	33.0	48	4.5	512
D	1024	16	128	1.05	1024.0		-	9.0	10	4	0.28	50	4.5	48	-	200
F	1024	16	32	1.05	12.5		-	9.0	10	4	0.28	50	8.5	100	-	200
G	1024	16	128	1.05	16.5		-	9.0	17	4	0.28	300	33.0	100	-	512

[*1] t_{VDET31} can be selected from two types, A and B, with mask options, and each type has four patterns with trimming options.

Table of functions (d)

Function	Overcharge Release	Overdischarge Release [*1]	Discharge Overcurrent Release	Type of t_{VDET31}	Discharge Overcurrent Detection 2 (V_{DET32})	0 V Battery Charging	Forced Reset		V_{STBD} [V]	V_{RSTD} [V]
							Detection	Release		
Type/ Condition	Auto Release Latch	Auto Release Latch1 Latch2	Auto Release1 Auto Release2 Latch	A B	Available Unavailable	Permission Inhibition	1st Step 2nd Step	V- Rising Auto Release	0.65 0.80 1.20 1.80	0.65 0.80 1.20 1.80
E	Latch	Latch1	Latch	B	Unavailable	Inhibition	1st Step	V- Rising	0.65	0.65
F	Latch	Latch2	Latch	A	Available	Inhibition	2nd Step	Auto Release	0.80	0.80
J	Latch	Latch1	Auto Release1	B	Unavailable	Inhibition	1st Step	V- Rising	0.65	0.65
K	Latch	Latch1	Auto Release1	B	Unavailable	Permission	1st Step	V- Rising	0.65	0.65
Q	Auto Release	Auto Release	Auto Release1	B	Unavailable	Inhibition	1st Step	V- Rising	0.65	0.65

[*1] Overdischarge Release Conditions,
Auto Release: Cell voltage > V_{REL2}
Latch 1: Cell voltage > V_{DET2} under charger connection
Latch 2: Charger connection

Grade

Grade	Application	Operating Temperature Range	Test Temperature
S	General-purpose and Consumer	−40°C to 85°C	25°C

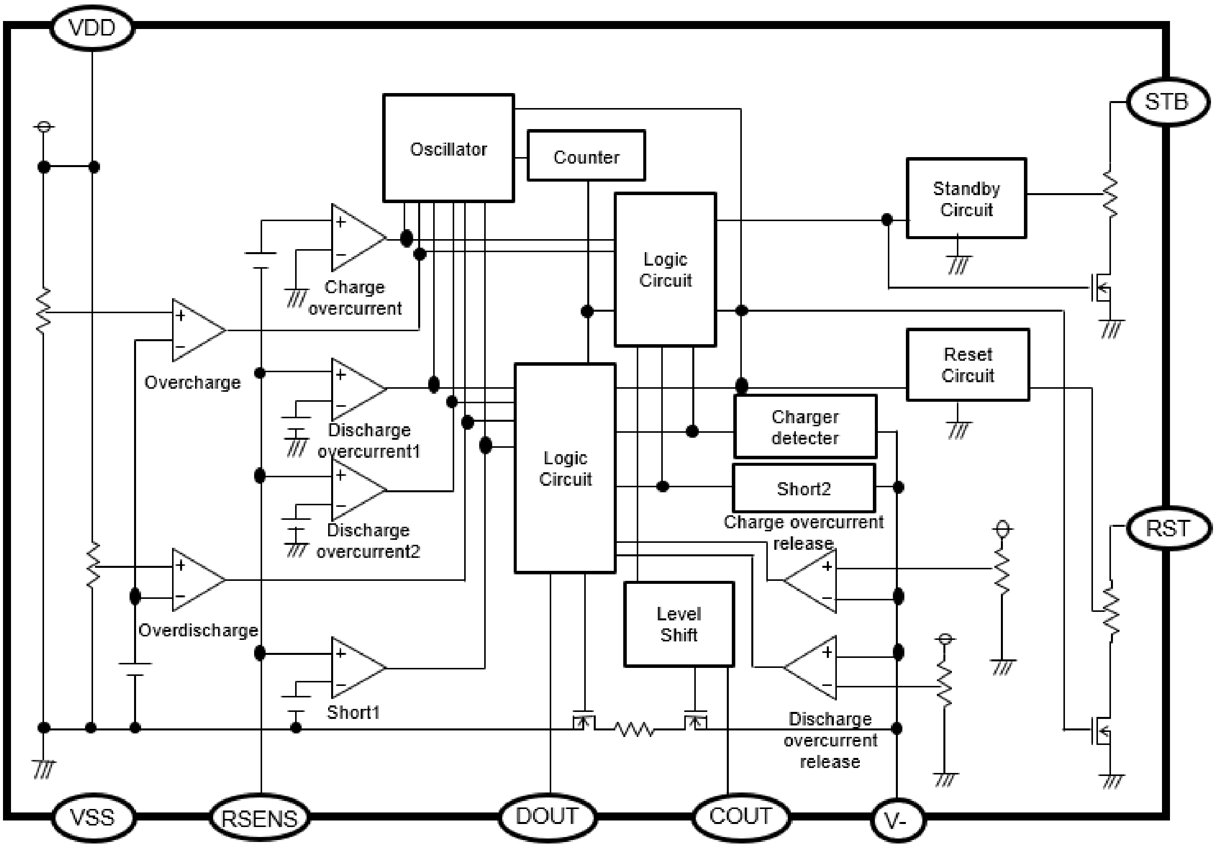
ORDER INFORMATION

For details of the orderable products, please refer to the Appendix *"Product Code List"*.

Product Name	Package	RoHS	Halogen-Free	Plating Composition	Weight [mg]	Quantity Per Reel [pcs]
NB7140ZA*****E2S	WLCSP-8-P10	Yes	Yes	Sn3.0Ag0.5Cu	0.73	5,000

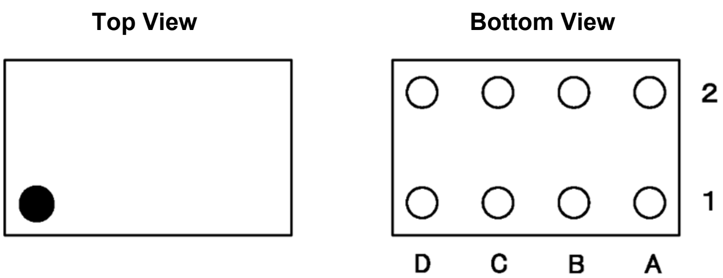
Note: Contact our sales representatives for other specific option code (indicated with five asterisks).

BLOCK DIAGRAM



NB7140ZA Block Diagram

PIN DESCRIPTION



NB7140ZA (WLCSP-8-P10) Pin Configuration

Pin No.	Pin Name	I/O	Description
A1	STB	I	Forced standby instruction signal input pin
B1	V-	I	Charger negative input pin
C1	COUT	O	Charge control pin, CMOS output
D1	DOUT	O	Discharge control pin, CMOS output
A2	RST	I	Forced-off state input pin
B2	RSENS	I	Overcurrent detection input pin
C2	VDD	-	Power supply pin, the substrate level of the IC
D2	VSS	-	Ground pin for the IC

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.3 to 12	V
V- pin input voltage	V-	V_{DD} – 30 to V_{DD} + 0.3	V
RSENS pin input voltage	V_{RSENS}	V_{SS} – 0.3 to V_{DD} + 0.3	V
RST pin input voltage	V_{RST}	V_{DD} – 30 to V_{DD} + 0.3	V
STB pin input voltage	V_{STB}	V_{DD} – 30 to V_{DD} + 0.3	V
COUT pin output voltage	V_{COUT}	V_{DD} – 30 to V_{DD} + 0.3	V
DOUT pin output voltage	V_{DOUT}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D	150	mW
Junction temperature range	Tj	–40 to 125	°C
Storage temperature range	Tstg	–55 to 125	°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

ELECTROSTATIC DISCHARGE RATINGS

Parameter	Conditions	Rating	Unit
HBM (Human Body Model)	C = 100 pF, R = 1.5 kΩ	±2000	V
CDM (Charged Device Model)	Field Included CDM (FI-CDM)	±1000	V

ELECTROSTATIC DISCHARGE RATINGS
The electrostatic discharge test is done based on JESD47. In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating	Unit
Operating input voltage	V_{DD}	1.5 to 5.0	V
Operating temperature range	Ta	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

Ta = 25°C, unless otherwise noted

NB7140ZA***E2S Electrical Characteristics**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark *1
Minimum charging voltage for 0 V battery charger *2	V_{STCHG}	$V_{DD} – V_{SS}$ = 0 V, defined as V_{DD} – V- difference voltage			1.8	V	B
0 V battery charging inhibition voltage *3	V_{NOCHG}	V_{DD} – V- = 4 V, defined as $V_{DD} – V_{SS}$ difference voltage	V_{NOCHG} × 0.96	V_{NOCHG}	V_{NOCHG} × 1.04	V	A
Overcharge detection voltage	V_{DET1}	R_{VDD} = 330Ω, C_{VDD} = 0.1µF	V_{DET1} – 0.015	V_{DET1}	V_{DET1} + 0.015	V	A
Overcharge release voltage	V_{REL1}	R_{VDD} = 330Ω, C_{VDD} = 0.1µF	V_{REL1} – 0.045	V_{REL1}	V_{REL1} + 0.045	V	A
Overcharge detection delay time	t_{VDET1}	V_{DD} = 3.6 V → V_{DET1} + 0.1 V	t_{VDET1} × 0.80	t_{VDET1}	t_{VDET1} × 1.20	ms	A
Overcharge release delay time	t_{VREL1}	Overcharge: Auto Release: V_{DD} = 4.8 V → V_{REL1} – 0.1 V Overcharge: Latch: V_{DD} = 4.8 V → V_{DET1} – 0.1 V, V- = 0.2 V	12.8	16.0	19.2	ms	A
Overdischarge detection voltage	V_{DET2}	Detect falling edge of supply voltage	V_{DET2} – 0.035	V_{DET2}	V_{DET2} + 0.035	V	C
Overdischarge release voltage	V_{REL2}	Detect rising edge of supply voltage	V_{REL2} – 0.070	V_{REL2}	V_{REL2} + 0.070	V	C
Overdischarge detection delay time	t_{VDET2}	V_{DD} = V_{DET2} + 0.15 V → V_{DET2} – 0.10 V	t_{VDET2} × 0.80	t_{VDET2}	t_{VDET2} × 1.20	ms	C
Overdischarge release delay time	t_{VREL2}	Overcharge: Auto Release: V_{DD} = V_{DET2} – 0.04 V → V_{REL2} + 0.1 V Overcharge: Latch: V_{DD} = V_{DET2} – 0.04 V → V_{DET2} + 0.04 V, V- = 0.0 V	0.75	1.05	1.53	ms	C
V- pin pullup resistance for V_{DET2}	R_{V-1}	V_{DD} = 1.8 V	0.1	0.6	1.0	MΩ	E
Discharge overcurrent detection voltage 1	V_{DET31}	V_{DD} = 3.6 V, Detect rising edge of V_{RSENS}; V_{DET31} ≤ 0.030 V	V_{DET31} – 0.0010	V_{DET31}	V_{DET31} + 0.0010	V	F
		V_{DD} = 3.6 V, Detect rising edge of V_{RSENS}; V_{DET31} > 0.030 V	V_{DET31} – 0.0015		V_{DET31} + 0.0015		
Discharge overcurrent detection delay time 1	t_{VDET31}	V_{DD} = 3.6 V, V_{RSENS} = 0.0 V → V_{DET31} + 0.005 V	t_{VDET31} × 0.80	t_{VDET31}	t_{VDET31} × 1.20	ms	F
Discharge overcurrent detection voltage 2	V_{DET32}	V_{DD} = 3.6V, Detect rising edge of V_{RSENS}; V_{DET32} ≤ 0.060 V	V_{DET32} – 0.002	V_{DET32}	V_{DET32} + 0.002	V	F
		V_{DD} = 3.6V, Detect rising edge of V_{RSENS}; V_{DET32} > 0.060 V	V_{DET32} × 0.96		V_{DET32} × 1.04		
Discharge overcurrent detection delay time 2	t_{VDET32}	V_{DD} = 3.6 V, V_{RSENS} = 0.0 V → V_{DET32} + 0.005 V	t_{VDET32} × 0.80	t_{VDET32}	t_{VDET32} × 1.20	ms	F
Short circuit detection voltage 1	V_{SHORT1}	V_{DD} = 3.6 V, Detect rising edge of V_{RSENS}; V_{SHORT1} ≤ 0.120 V	V_{SHORT1} – 0.004	V_{SHORT1}	V_{SHORT1} + 0.004	V	F
		V_{DD} = 3.6 V, Detect rising edge of V_{RSENS}; V_{SHORT1} > 0.120 V	V_{SHORT1} – 0.005		V_{SHORT1} + 0.005		
Short circuit detection delay time *4	t_{SHORT}	V_{DD} = 3.6 V, V_{RSENS} = 0.0 V → 1.0 V	210	280	380	µs	F
Short circuit detection voltage 2	V_{SHORT2}	Detect rising edge of V-, V_{DD} = 3.6 V, V_{RSENS} = 0.0 V	V_{DD} – 2.00	V_{DD} – 1.50	V_{DD} – 0.80	V	G

*1 The test circuits for device evaluation. Refer to the section of *TEST CIRCUITS* for detail information.
*2 Only 0 V battery charging permission type
*3 Only 0 V battery charging inhibition type
*4 Short circuit release delay time is same as t_{VREL3}.

Ta = 25°C, unless otherwise noted

NB7140ZA***E2S Electrical Characteristics (Continued)**

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Remark *1
Charger detection voltage 1	$V_{CHGDET1}$	Detect falling edge of V-, R_{V-} = 1.0kΩ, V_{DD} = V_{DET2} + 0.05 V		0.500	0.800	1.100	V	G
Charger detection voltage 2	$V_{CHGDET2}$	Detect falling edge of V-, R_{V-} = 1.0kΩ V_{DD} = V_{DET2} - 0.03 V		–0.310	–0.100	-	V	G
Discharge overcurrent release voltage	V_{REL3}	Detect falling edge of V-, V_{DD} = 3.6 V, V_{RSENS} = 0.0 V	Auto Release1	V_{DD} × 0.800 – 0.050	V_{DD} × 0.800	V_{DD} × 0.800 + 0.050	V	G
			Auto Release2	0.040	0.070	0.100		
			Latch	0.040	0.070	0.100		
Discharge overcurrent release resistance	R_{SHORT}	Auto Release 1: V_{DD} = 3.6 V, V- = V_{REL3} + 0.050 V		6.5	10.0	13.5	kΩ	H
		Auto Release 2: V_{DD} = 3.6 V, V- = 0.200 V		20	45	70		
Discharge overcurrent release delay time	t_{VREL3}	V_{DD} = 3.6 V, V- = 3.6 V → 0.0 V V_{RSENS} = 0.0 V		7.3	9.0	10.8	ms	G
Charge overcurrent detection voltage	V_{DET4}	V_{DD} = 3.6 V, Detect falling edge of V_{RSENS}	V_{DET4} ≥ –0.030 V	V_{DET4} – 0.0010	V_{DET4}	V_{DET4} + 0.0010	V	I
			V_{DET4} < –0.030 V	V_{DET4} – 0.0015		V_{DET4} + 0.0015		
Charge overcurrent detection delay time	t_{VDET4}	V_{DD} = 3.6 V, V_{RSENS} = 0.0 V → –0.5 V		t_{VDET4} × 0.80	t_{VDET4}	t_{VDET4} × 1.20	ms	I
Charge overcurrent release voltage	V_{REL4}	Detect rising edge of V-, V_{DD} = 3.6V, V_{RSENS} = 0.0V		0.040	0.070	0.100	V	J
Charge overcurrent release delay time	t_{VREL4}	V_{DD} = 3.6 V, V- = −0.5 V → 1.0 V V_{RSENS} = 0.0 V		3.2	4.0	4.8	ms	J
Forced standby detection voltage	V_{STBD}	Detect rising edge of STB, V_{DD} = 3.6 V, V- = V_{RSENS} = 0.0 V		V_{STBD} × 0.80	V_{STBD}	V_{STBD} × 1.20	V	K
Forced standby detection delay time	t_{STBD}	V_{DD} = 3.6 V, V_{STB} = 0.0 V → 3.6 V, V- = V_{RSENS} = 0.0 V		t_{STBD} × 0.80	t_{STBD}	t_{STBD} × 1.20	ms	K
Forced standby release delay time	t_{STBR}	V_{DD} = 3.6 V, V- =3.6 V → 0.0 V, V_{STB} = V_{RSENS} = 0.0 V		t_{STBR} × 0.80	t_{STBR}	t_{STBR} × 1.20	ms	L
STB pin pulldown resistance	R_{STBPD}	V_{DD} = 3.6 V, V_{STB} = 3.6 V, V- = V_{RSENS} = 0 V		5.5	11.0	22.0	MΩ	M
V- pin pullup resistance in forced standby mode	R_{V-2}	V_{DD} = 3.6 V, V_{STB} = 3.6 V, V- = V_{RSENS} = 0.0 V		40	70	120	kΩ	N
System reset detection voltage	V_{RSTD}	Detect rising edge of RST, V_{DD} = 3.6 V, V- = V_{RSENS} = 0.0 V		V_{RSTD} × 0.80	V_{RSTD}	V_{RSTD} × 1.20	V	O
System reset 1st step detection delay time	t_{RST1}	V_{DD} = 3.6 V, V_{RST} = 0.0 V → 3.6V, V- = V_{RSENS} = 0.0 V		t_{RST1} × 0.80	t_{RST1}	t_{RST1} × 1.20	ms	O
System reset 2nd step detection delay time *2	t_{RST2}	V_{DD} = 3.6 V, V_{RST} = 3.6 V → 0.0 V, V- = V_{RSENS} = 0.0 V		t_{RST2} × 0.80	t_{RST2}	t_{RST2} × 1.20	ms	O
System reset release delay time	t_{RSTR}	Auto Release Type: V_{DD} = 3.6 V		t_{RSTR} × 0.80	t_{RSTR}	t_{RSTR} × 1.20	ms	O, P
		V- Rising Type: V_{DD} = 3.6 V, V- = 0.0 V → 3.6 V						
RST pin pulldown resistance	R_{RSTPD}	V_{DD} = 3.6 V, V_{RST} = 3.6 V, V- = V_{RSENS} = 0.0 V		5.5	11.0	22.0	MΩ	Q

*1 The test circuits for device evaluation. Refer to the section of *TEST CIRCUITS* for detail information.
*2 Only Reset pulse detection type

Ta = 25°C, unless otherwise noted

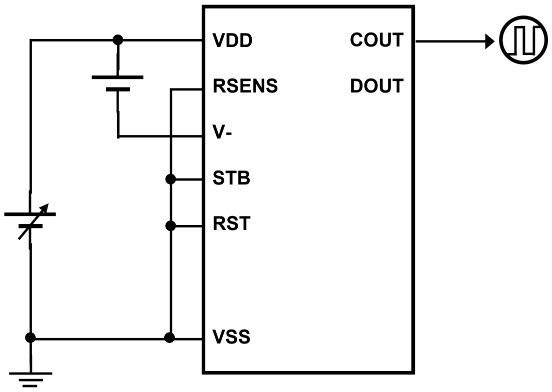
NB7140ZA∗∗∗∗∗E2S Electrical Characteristics (Continued)

<table>
<tr><th>Parameter</th><th>Symbol</th><th colspan="2">Conditions</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th>Remark *1</th></tr>
<tr><td>COUT pin NMOS ON voltage</td><td>V_{OL1}</td><td colspan="2">I_{OL} = 50μA, V_{DD} = 4.80 V</td><td></td><td>0.4</td><td>0.5</td><td>V</td><td>R</td></tr>
<tr><td>COUT pin PMOS ON voltage</td><td>V_{OH1}</td><td colspan="2">I_{OH} = –50μA, V_{DD} = 3.90 V</td><td>3.4</td><td>3.7</td><td></td><td>V</td><td>S</td></tr>
<tr><td>DOUT pin NMOS ON voltage</td><td>V_{OL2}</td><td colspan="2">I_{OL} = 50μA, V_{DD} = 1.90 V</td><td></td><td>0.2</td><td>0.5</td><td>V</td><td>T</td></tr>
<tr><td>DOUT pin PMOS ON voltage</td><td>V_{OH2}</td><td colspan="2">I_{OH} = –50μA, V_{DD} = 3.90 V</td><td>3.4</td><td>3.7</td><td></td><td>V</td><td>U</td></tr>
<tr><td rowspan="2">Supply current</td><td rowspan="2">I_{DD}</td><td rowspan="2">V_{DD} = 3.9 V,
V- = 0.0 V</td><td>0 V battery charging: Permission</td><td></td><td>1.4</td><td>2.8</td><td rowspan="2">μA</td><td rowspan="2">V</td></tr>
<tr><td>0 V battery charging: Inhibition</td><td></td><td>1.5</td><td>3.0</td></tr>
<tr><td>Supply current in forced standby mode</td><td>I_{FSTB}</td><td colspan="2">V_{DD} = V- = 3.9 V</td><td></td><td></td><td>0.04</td><td>μA</td><td>W</td></tr>
<tr><td rowspan="2">Standby current</td><td rowspan="2">$I_{STANDBY}$</td><td rowspan="2">V_{DD} = 1.9 V</td><td>Overdischarge: Auto release</td><td></td><td></td><td>0.20</td><td rowspan="2">μA</td><td rowspan="2">W</td></tr>
<tr><td>Overdischarge: Latch 1 / 2</td><td></td><td></td><td>0.04</td></tr>
</table>

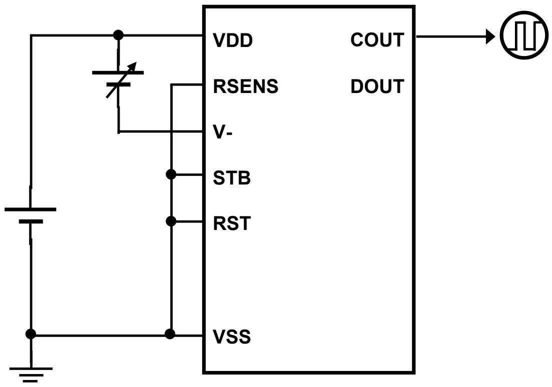
*1 The test circuits for device evaluation. Refer to the section of *TEST CIRCUITS* for detail information.
All test parameters listed in Electrical Characteristics are done under Ta = 25°C only.

Test Circuits

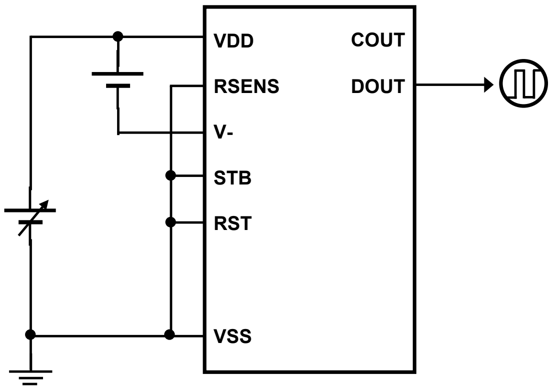
A



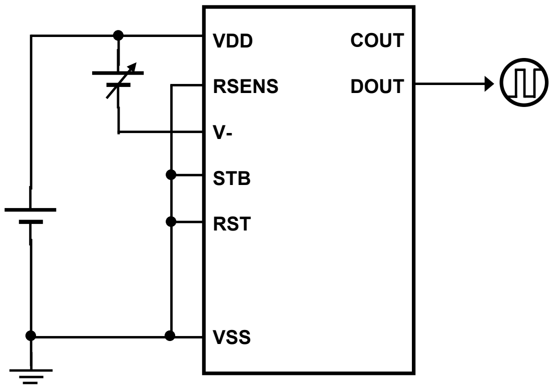
B



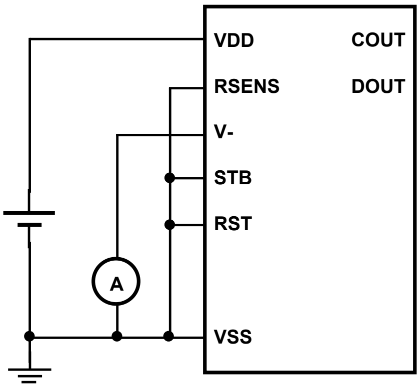
C



D



E



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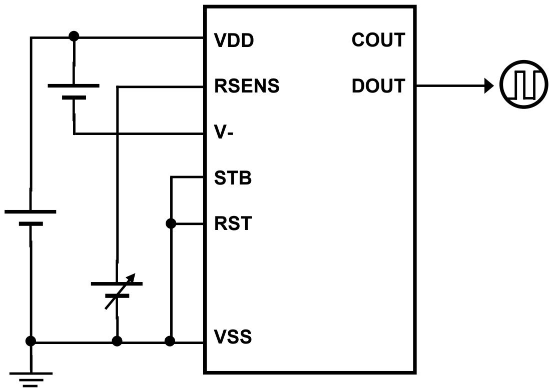

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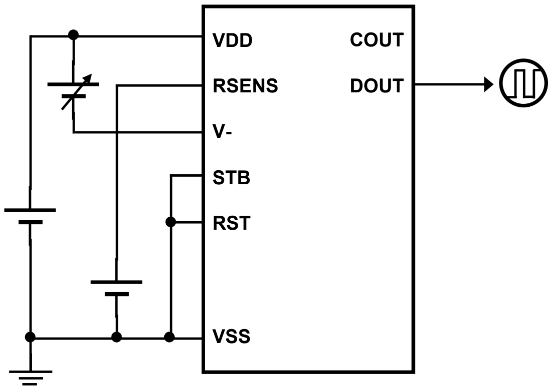

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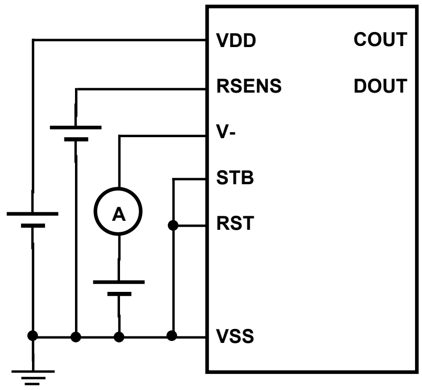

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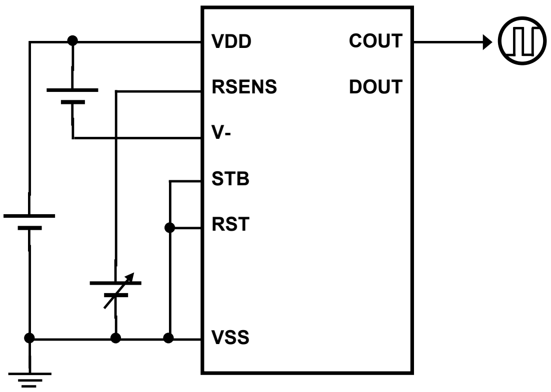
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RSENS
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VSS

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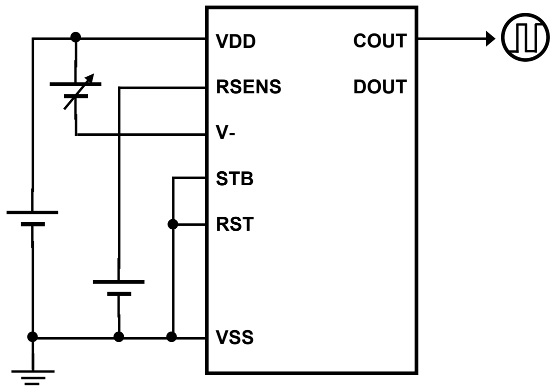
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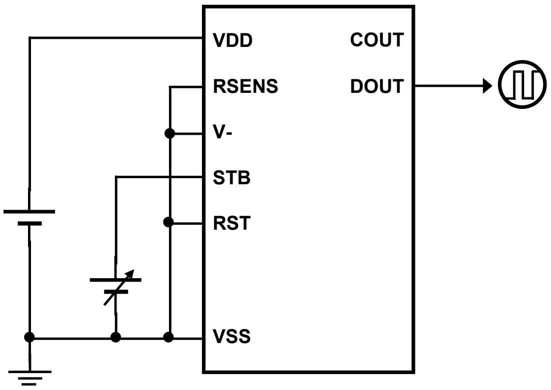
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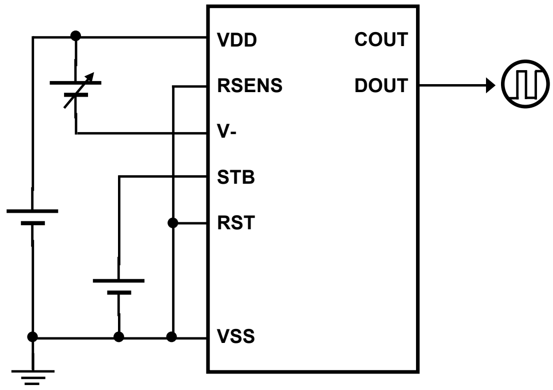
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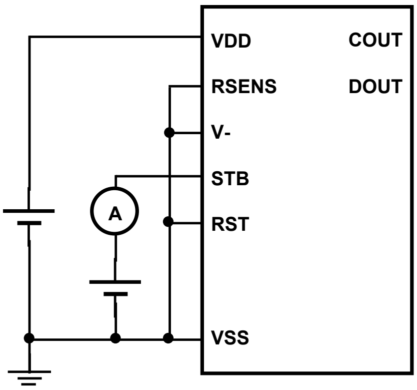
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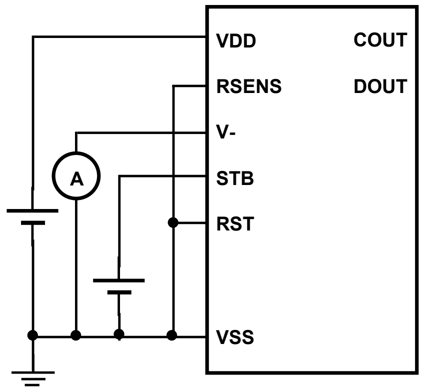
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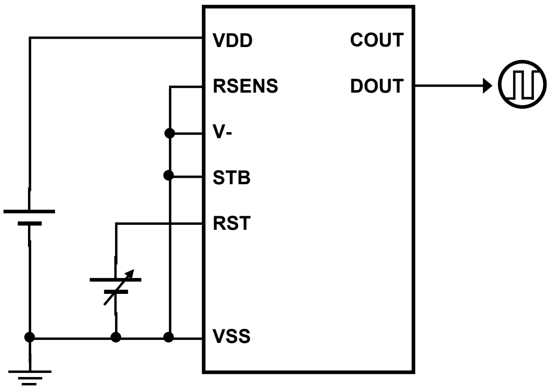
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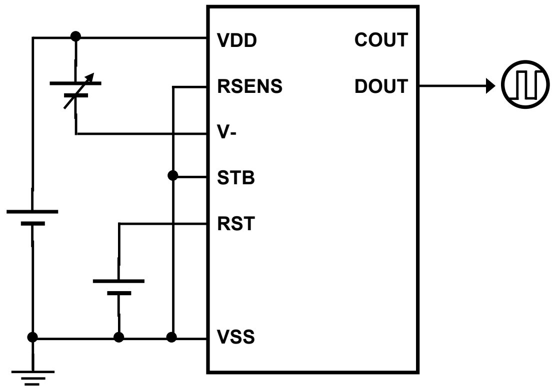
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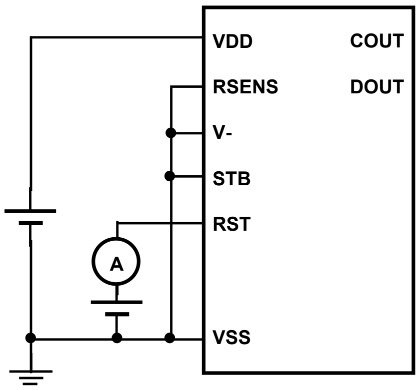
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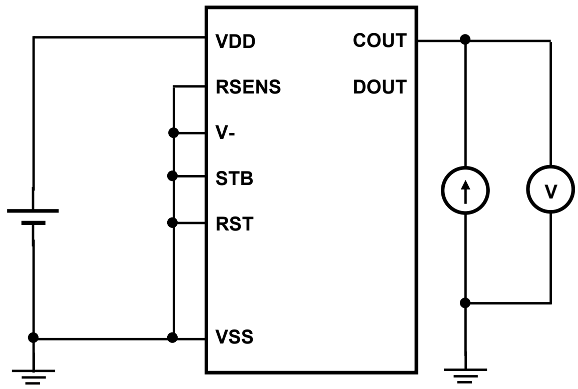
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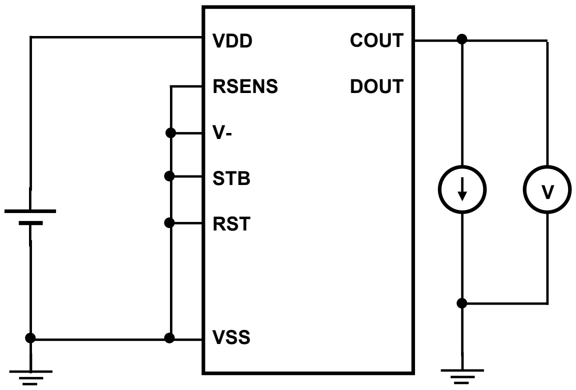
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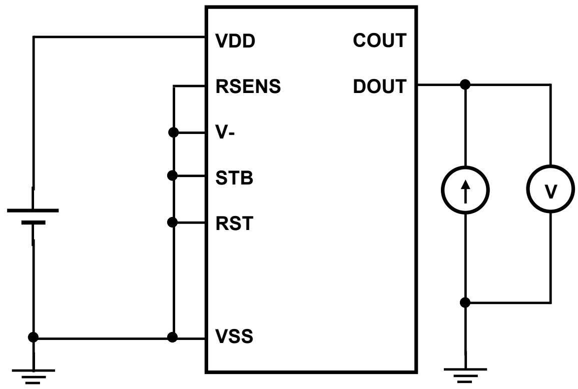
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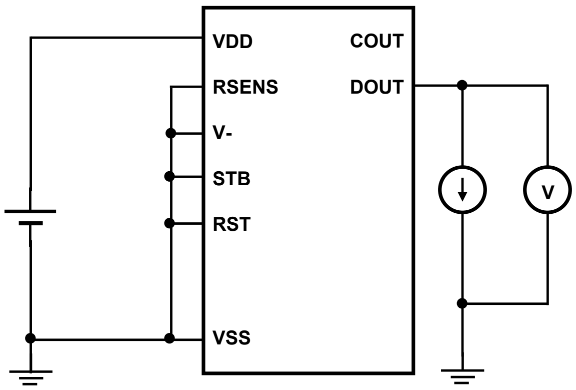
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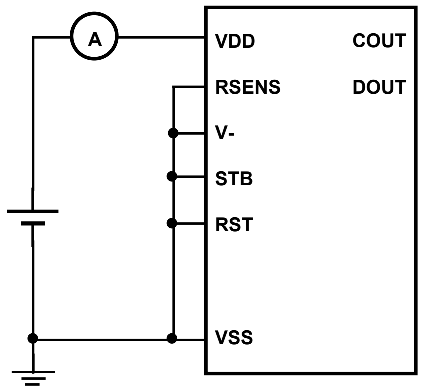
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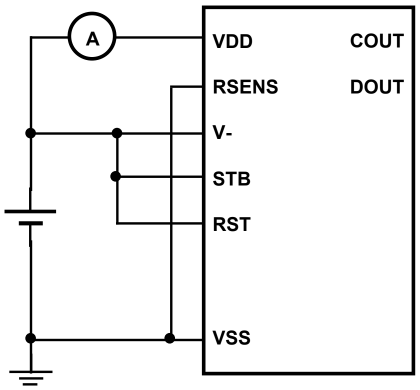
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V-
STB
RST
VSS
COUT
DOUT

THEORY OF OPERATION

Overcharge Protection

When the overcharge detection delay time (t_{VDET1}) passes under the condition that the VDD pin voltage (V_{DD}) exceeds the overcharge detection voltage (V_{DET1}), this IC enters the over-charge state.
In this state, the COUT pin becomes Low, and the charge control FET is turned off to stop charging. The V- pin voltage (V-) increases by the Vf voltage (Vf) of the internal parasitic diode than the VSS pin voltage (V_{SS}) because the discharge current flows via the parasitic diode even when the charge control FET is off.
A release from the overcharge state must meet the following pin conditions and delay time according to the selected release type.

Type	Pin Conditions	Delay Time
Auto Release	V- < V_{REL4} and V_{DD} < V_{REL1} or V- > V_{REL4} and V_{DD} < V_{DET1}	t_{VREL1}
Latch	V- > V_{REL4} and V_{DD} < V_{DET1}	t_{VREL1}

Overdischarge Protection

When the overdischarge detection delay time (t_{VDET2}) passes under the condition that the VDD pin voltage (V_{DD}) falls below the over-discharge detection voltage (V_{DET2}), this IC enters the over-discharge state.
In this state, the DOUT pin becomes Low, and the discharge control FET is turned off to stop discharging. The V- pin voltage (V-) decreases by the Vf voltage (Vf) of the internal parasitic diode than the VSS pin voltage (V_{SS}) because the charge current flows via the parasitic diode even when the discharge control FET is off.
In addition, when V- is pulled up to V_{DD} level and exceeds the charger detection voltage 1 ($V_{CHGDET1}$), the IC enters the standby state. It results in reducing the standby current ($I_{STANDBY}$) to a minimum.
A release from the overdischarge state must meet the following pin conditions and delay time according to the selected release type.

Type	Pin Conditions	Delay Time
Auto Release	V- > $V_{CHGDET1}$ and V_{DD} > V_{REL2} or V- < $V_{CHGDET1}$ and V_{DD} > V_{DET2}	t_{VREL2}
Latch 1	V- < $V_{CHGDET1}$ and V_{DD} > V_{DET2}	t_{VREL2}
Latch 2	V- < $V_{CHGDET2}$	t_{VREL2}

Discharge Overcurrent Protection

To monitor a discharge current, this IC measures a voltage difference of the sense resistor (R_{SENS}) connected between the RSENS and the VSS pins to detect the current value.
This IC has two levels of the discharge overcurrent detection voltage 1/2 (V_{DET31} / V_{DET32}). When the discharge overcurrent detection delay time (t_{VDET31}) passes under the condition that the discharge current, which is converted through R_{SENS} for current-to-voltage conversion, exceeds V_{DET31}, this IC enters the discharge overcurrent state. In a case where V_{DET32} is enabled, this IC enters the discharge overcurrent state when the discharge overcurrent detection delay time (t_{VDET32}) passes under the condition exceeding V_{DET32}.
In this state, the DOUT pin becomes Low, and the discharge control FET is turned off to shut off the discharge current.
A release from the discharge overcurrent state must meet the following pin condition and delay time according to the selected release type.

Type	Pin Condition	Delay Time	Remarks
Auto Release 1	V- < V_{REL3} (Typ. V_{DD} × 0.800)	t_{VREL3}	V- is pulled down to the V_{SS} level inside the IC. Note1 (R_{SHORT} = Typ.10kΩ)
Auto Release 2	V- < V_{REL3} (Typ. 0.700 V)	t_{VREL3}	V- is pulled down to the V_{SS} level inside the IC. Note1 (R_{SHORT} = Typ.45kΩ)
Latch	V- < V_{REL3} (Typ. 0.700 V)	t_{VREL3}	V- is pulled up to the V_{DD} level inside the IC. Note2

Note1: It is possible to release the abnormal condition of the load connected to the battery pack. When the discharge overcurrent release delay time (t_{VREL3}) passes under the condition V- falls below V_{REL3}, this IC releases from the discharge overcurrent state. V- can be expressed by the following equation.

$$V- = V_{CELL} \times R_{SHORT} / (R_{SHORT} + R_{V-} + R_{LOAD})$$

V_{CELL} : Battery voltage
R_{SHORT} : Discharge overcurrent release resistance
R_{V-} : External resistor for V- pin
R_{LOAD} : Load resistance to a battery pack

Note2: When connecting a charger to pull V- down, this IC releases from the discharge overcurrent state.

Short-circuit Current Protection

To monitor a short-circuit current, this IC measures a voltage difference of the sense resistor (R_{SENS}) connected between the RSENS and the VSS pins to detect the current value. When the short-circuit current, which is converted through RSENS for current-to-voltage conversion, exceeds the short-circuit detection voltage 1 (V_{SHORT1}), this IC enters the short-circuit state. But it is possible for this IC to avoid its state when the short-circuit current falls below V_{SHORT1} within the short-circuit detection delay time (t_{SHORT}).
In this state, the DOUT pin becomes Low, and the discharge control FET is turned off to shut off the short-circuit current.
A release from the short-circuit state must meet the same condition and delay time as the discharge overcurrent protection.

Charge Overcurrent Protection

To monitor a charge current, this IC measures a voltage difference of the sense resistor (R_{SENS}) connected between the RSENS and the VSS pins to detect the current value. When the charge overcurrent detection delay time (t_{VDET4}) passes under the condition that the charge current, which is converted through RSENS for current-to-voltage conversion, falls below the charge overcurrent detection voltage (V_{DET4}), this IC enters the charge overcurrent state.
In this state, the COUT pin becomes Low, and the charge control FET is turned off to shut off the charge current.
A release from the charge overcurrent state must meet the following pin condition and delay time according to the selected release type.

Type	Pin Condition	Delay Time	Remarks
Auto Release	V- > V_{REL4}	t_{VREL4}	V- is pulled up to the V_{DD} level inside the IC. Note

Note: By disconnecting the charger, this IC releases from the charge overcurrent state.

0 V Battery Charging

This IC has the selectable charging function for the battery discharged to 0 V.

0 V Battery Charge Function “Permission”
This function allows to charge to the 0 V battery by connecting the charger with the minimum charging voltage (V_{STCHG}) and more.

0 V Battery Charge Function “Inhibition”
This function inhibits to charge to the battery with the 0 V-battery charging inhibition voltage (V_{NOCHG}) or less even when connecting the charger.

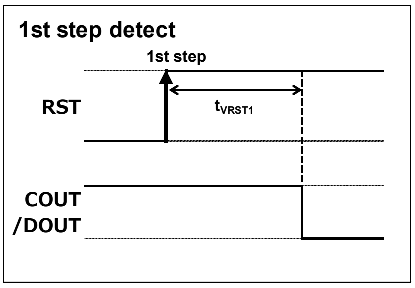
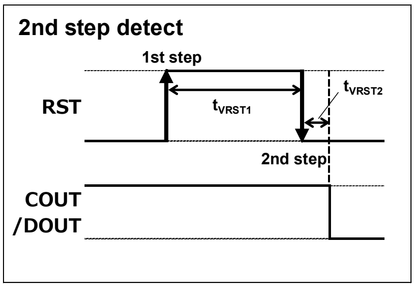
Forced-standby Function

When the forced standby detection delay time (t_{STBD}) passes under the condition that the STB pin voltage (V_{STB}) exceeds the forced standby detection voltage (V_{STBD}), this IC enters the forced standby detected state.
In this state, the IC turns off the charge and the discharge control FETs and the V- pin is pulled up to the VDD level by an internal resistor, here the V- pin pullup resistance is R_{V-2}.
After that, the IC enters the forced standby state when V- exceeds the charger detection voltage ($V_{CHGDET1}$). It results in reducing the supply current (I_{FSTB}) to a minimum.
A release from the forced standby state must meet the following pin condition and delay time according to the selected release type.

Type	Pin Condition	Delay Time	Remarks
Latch	V- < $V_{CHGDET1}$	t_{STBR}	V- is required to exceed V_{SHORT2} once for the release. The IC should not enter the forced standby state under connecting the charger.

Forced-reset Function

Forced reset detection must meet the following pin condition and delay time according to the selected detection type.
In this state, the IC turns off the charge and the discharge control FETs.

Type	Pin Condition	Delay Time	Remarks
1st step detection	$V_{RST} > V_{RSTD}$	t_{RST1}	
2nd step detection	$V_{RST} > V_{RSTD}$	t_{RST1}	
	$V_{RST} < V_{RSTD}$	t_{RST2}	

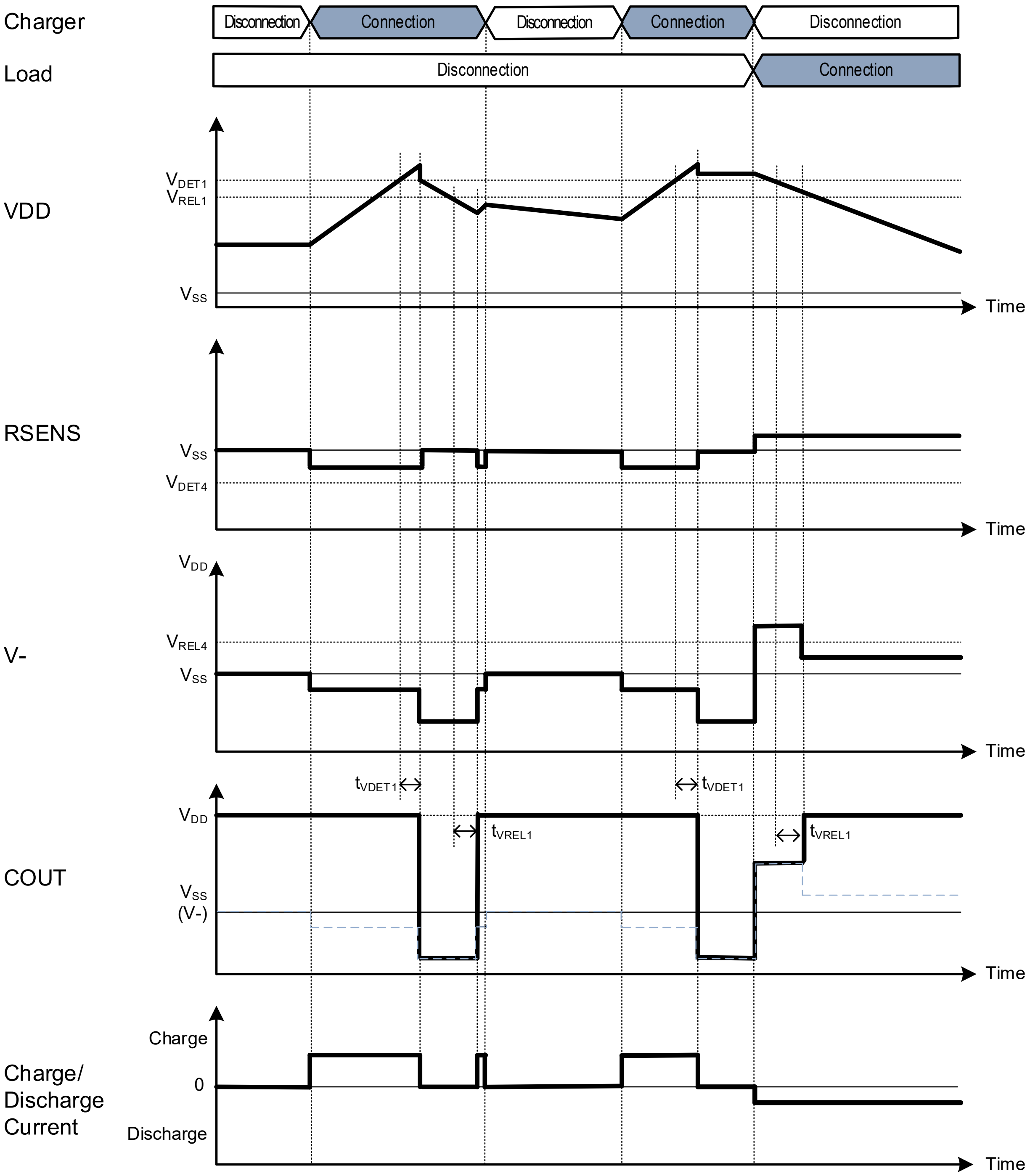
A release from the forced reset state must meet the following pin condition and delay time according to the selected release type.

Type	Pin Condition	Delay Time	Remarks
Auto release	-	t_{RSTR}	Immediately after forced reset is detected, forced reset release delay time (t_{RSTR}) counting starts.
V- rising	$V- > V_{SHORT2}$	t_{RSTR}	After the system power is depleted, forced reset release delay time (t_{RSTR}) counting starts.
	$V_{RST} < V_{RSTD}$ NOTE		When the charger is connected, and the RST pin voltage (V_{RST}) falls below V_{RSTD}, forced reset release delay time (t_{RST}) counting starts.

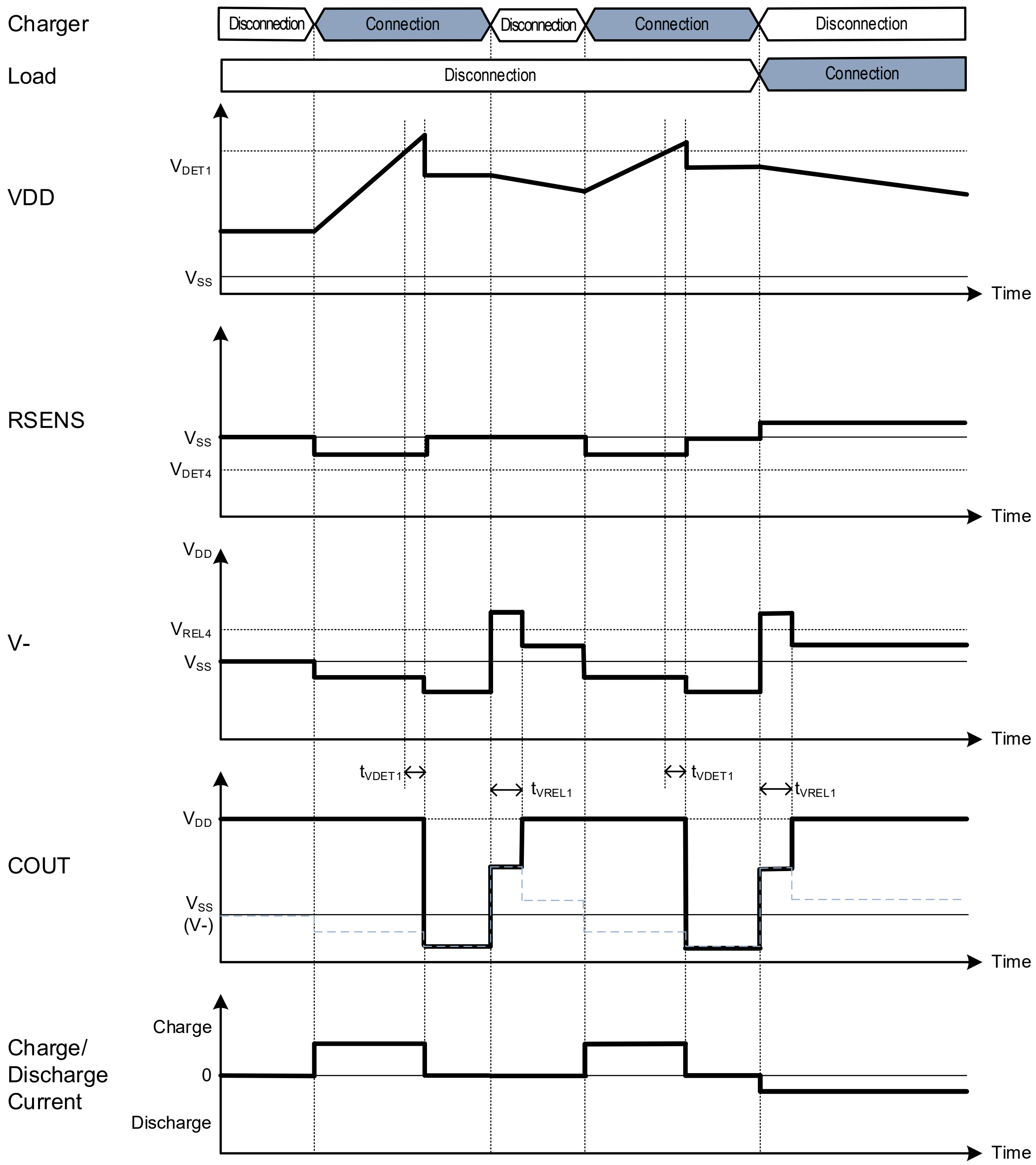
Note: The release operation by the RST pin is only for 1st step detection type.

Timing Chart

Overcharge

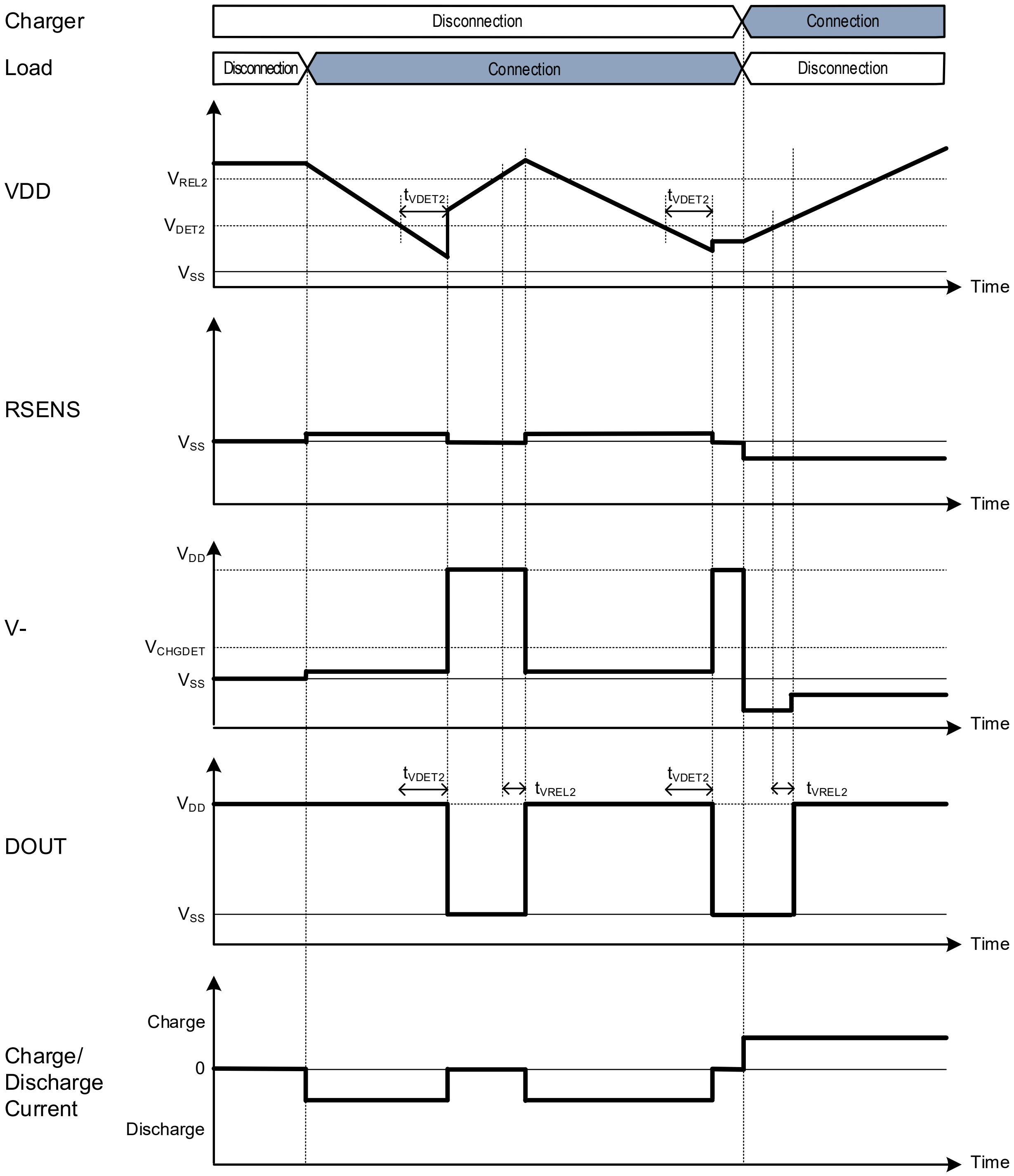


Overcharge (Auto Release) Timing Chart

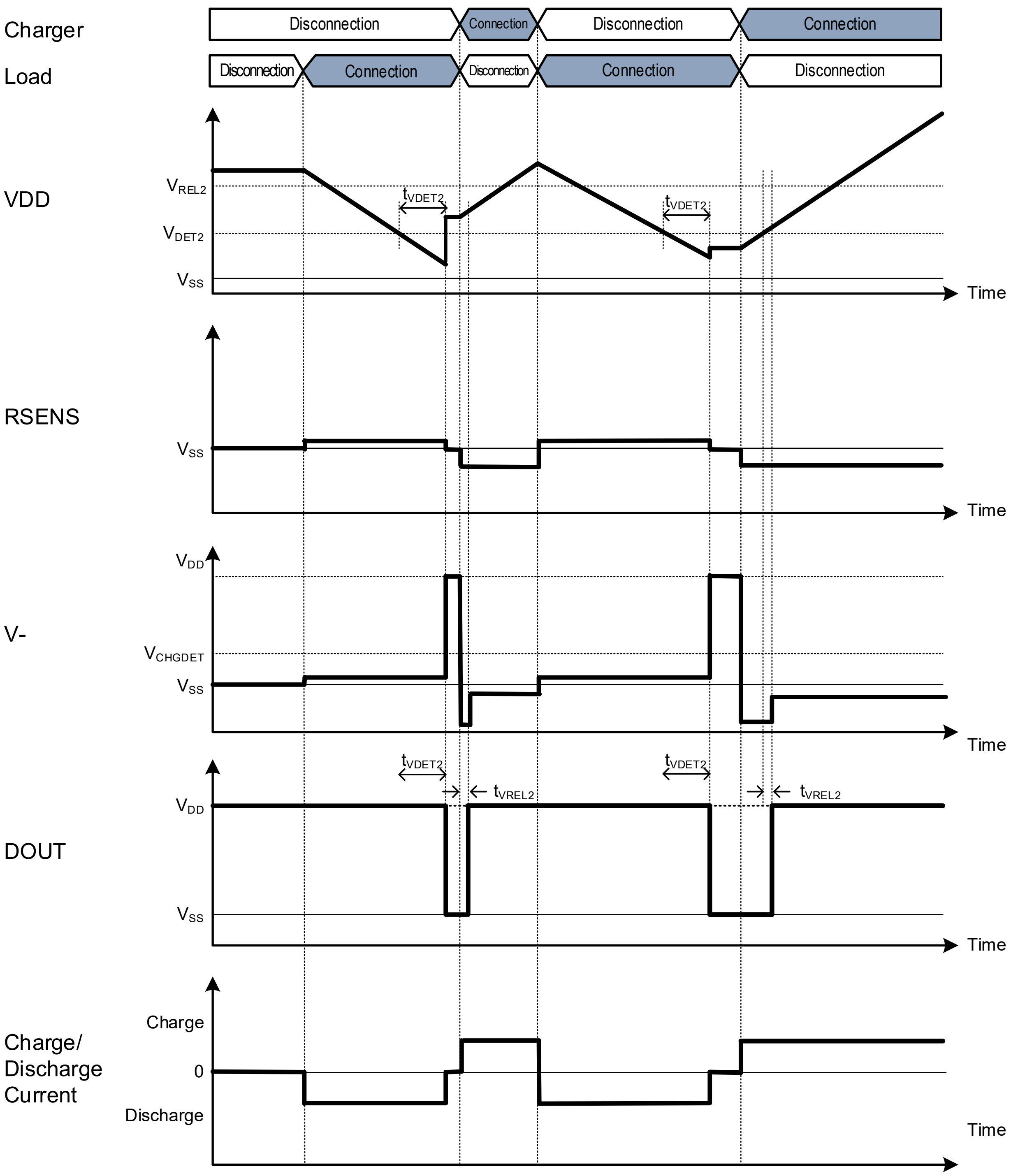


Overcharge (Latch) Timing Chart

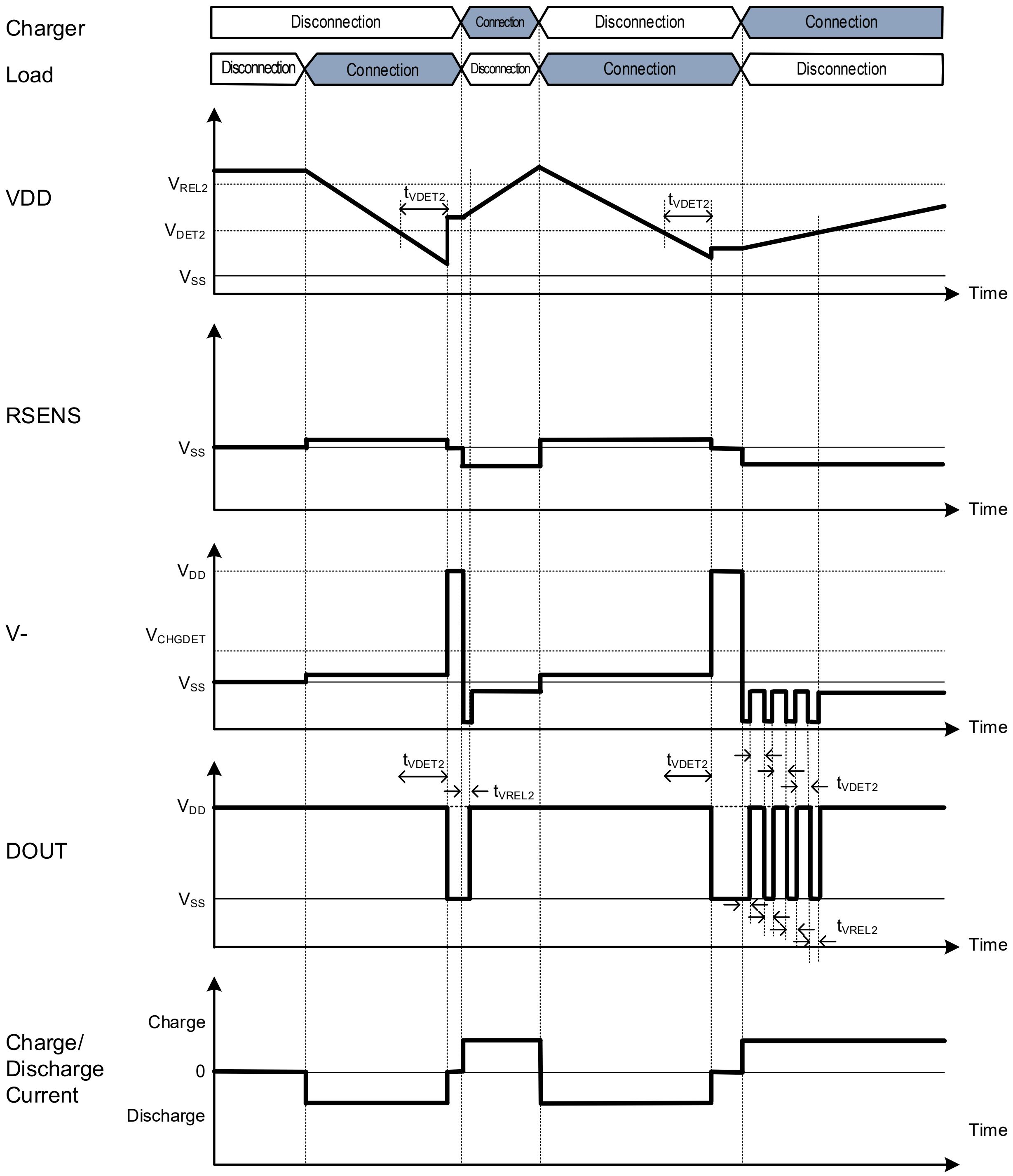
Overdischarge



Overdischarge (Auto Release) Timing Chart

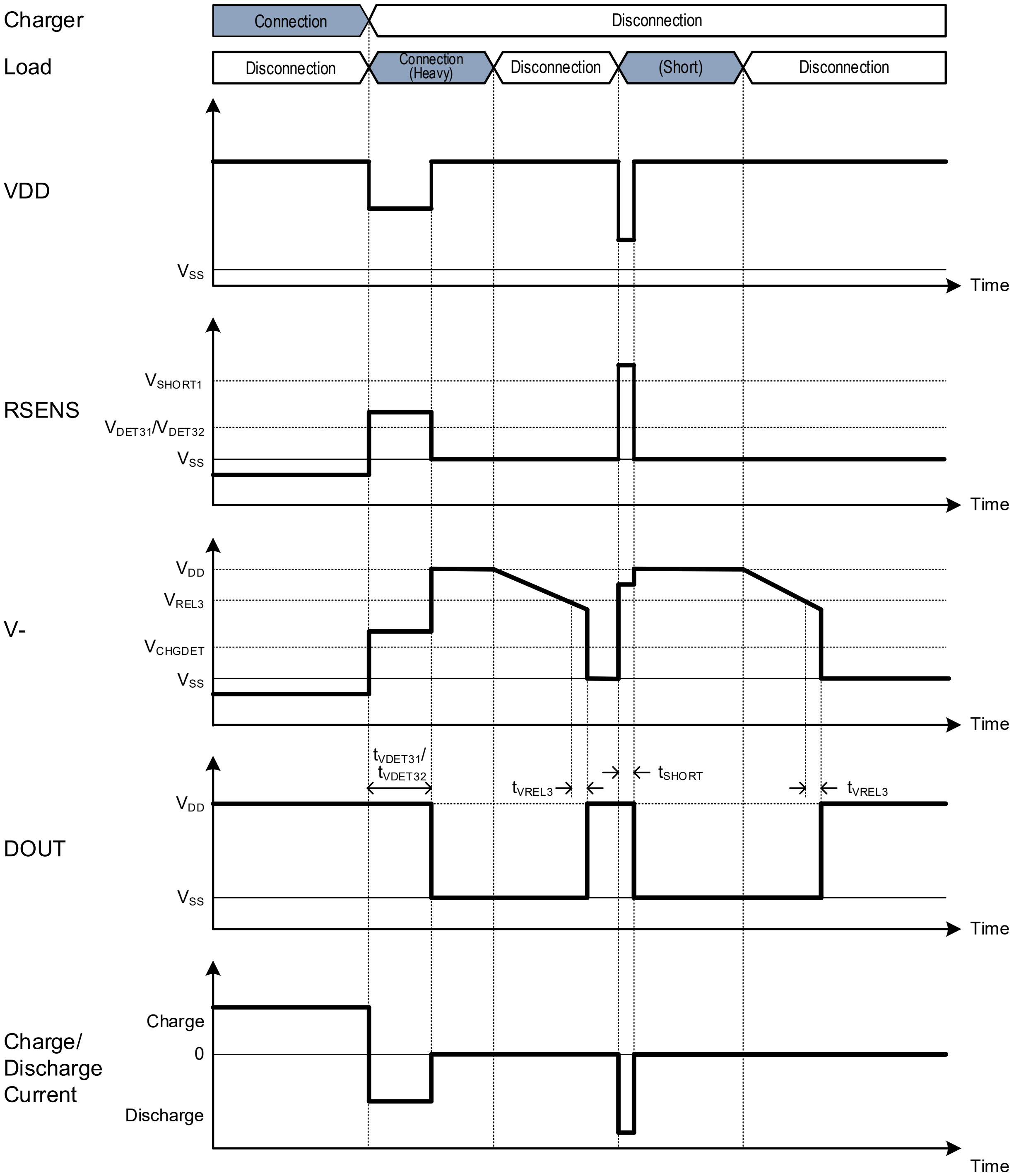


Overdischarge (Latch 1) Timing Chart

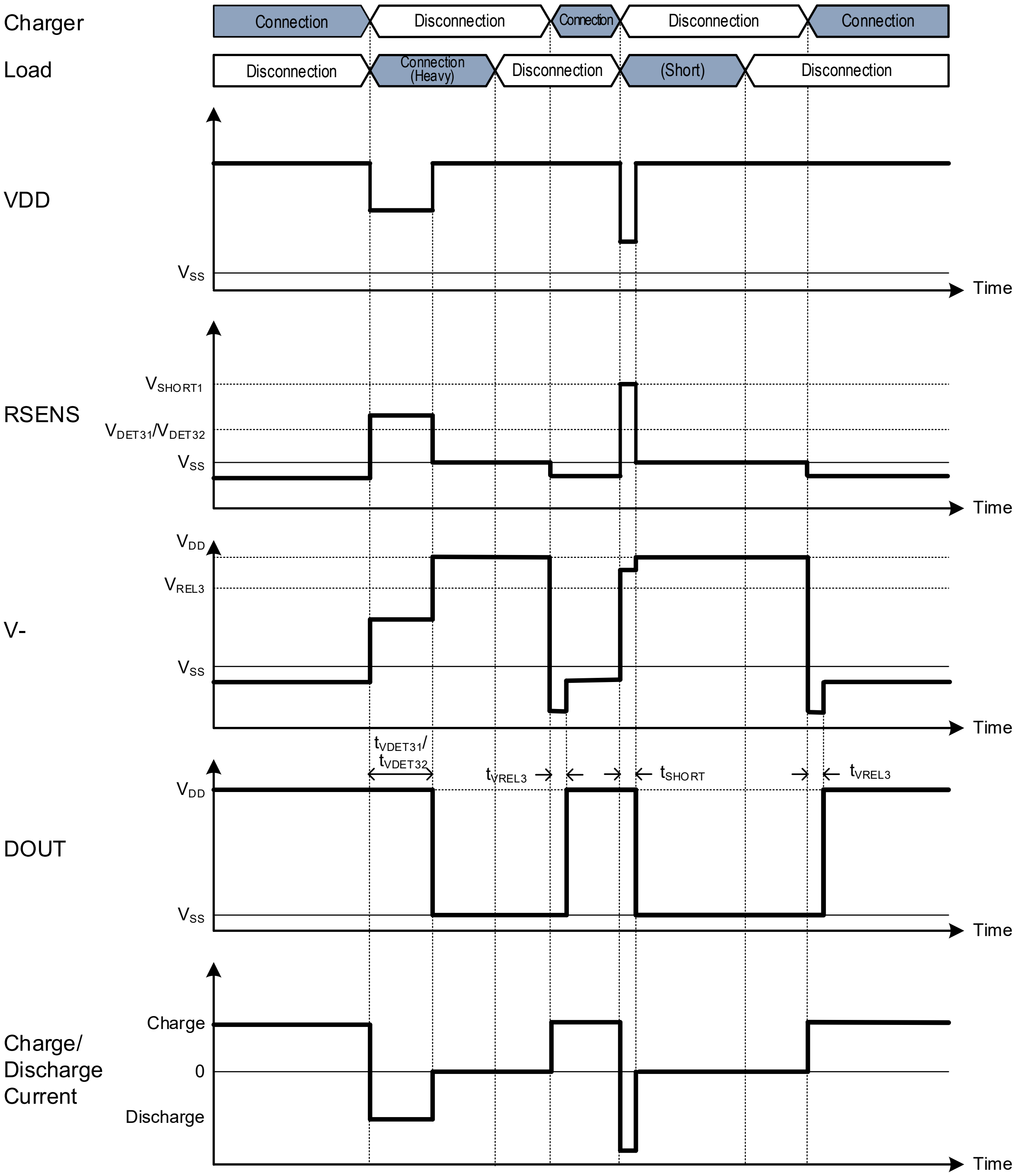


Overdischarge (Latch 2) Timing Chart

Discharge Overcurrent

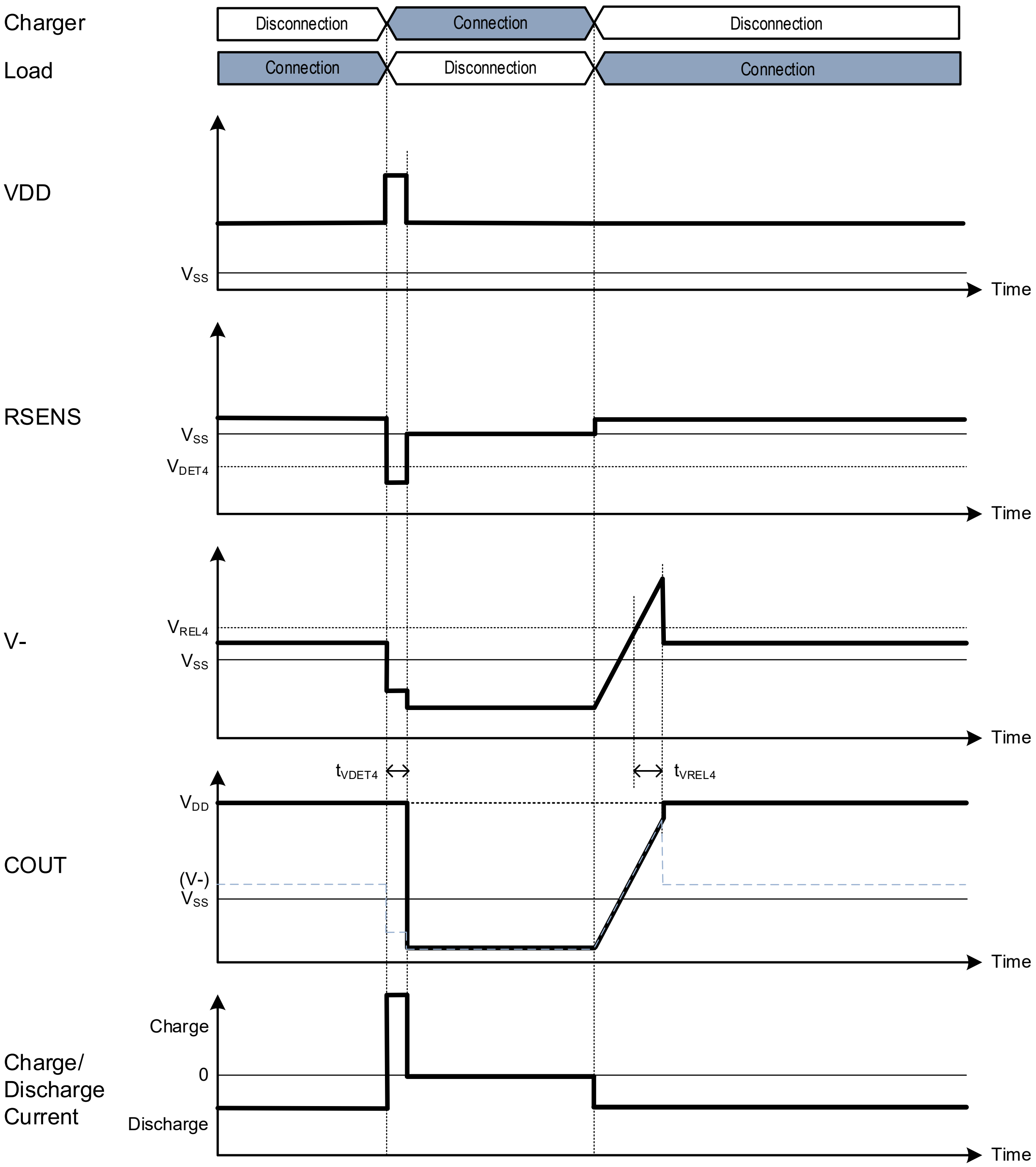


Discharge Overcurrent (Auto Release) Timing Chart



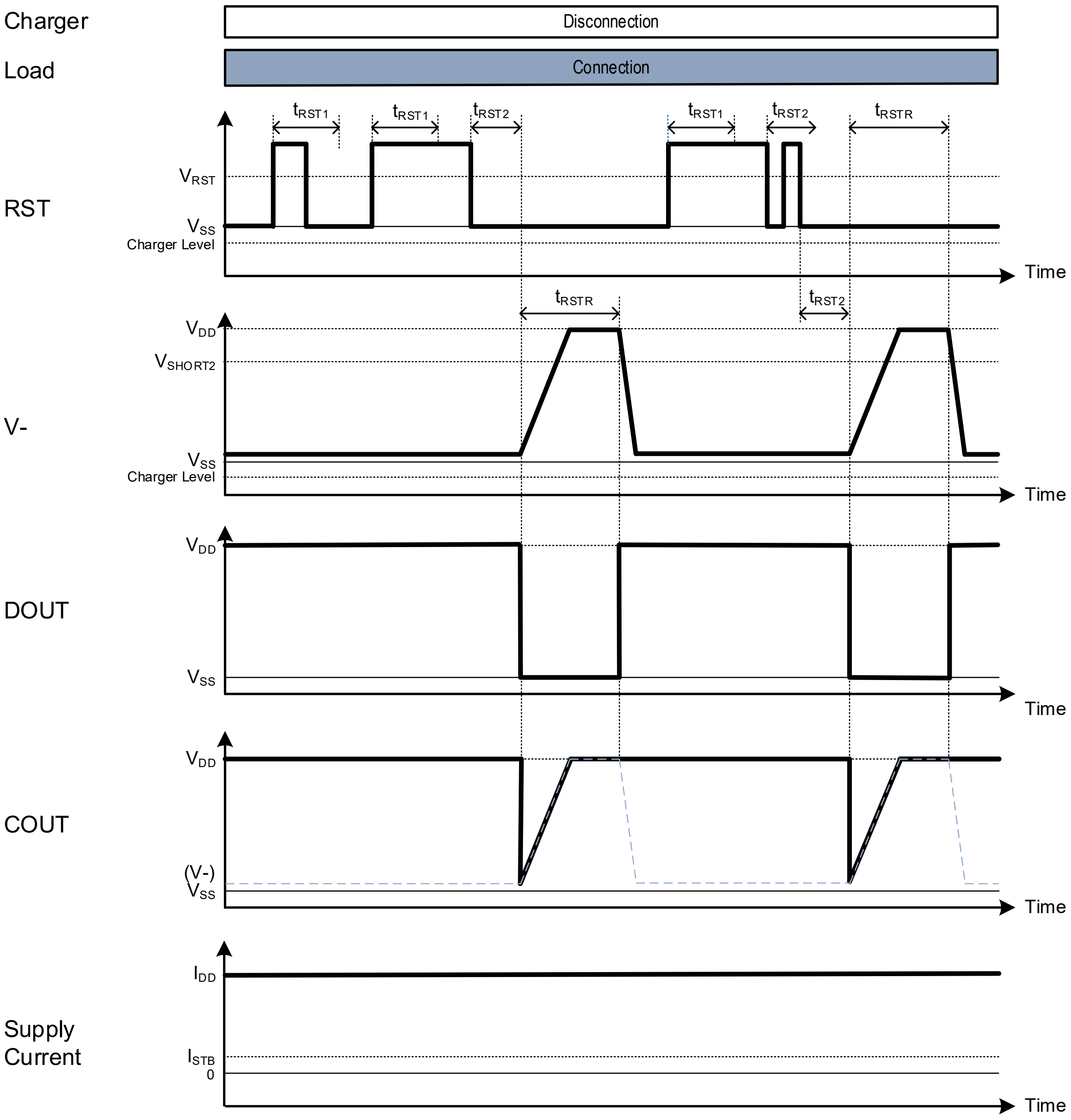
Discharge Overcurrent (Latch) Timing Chart

Charge Overcurrent

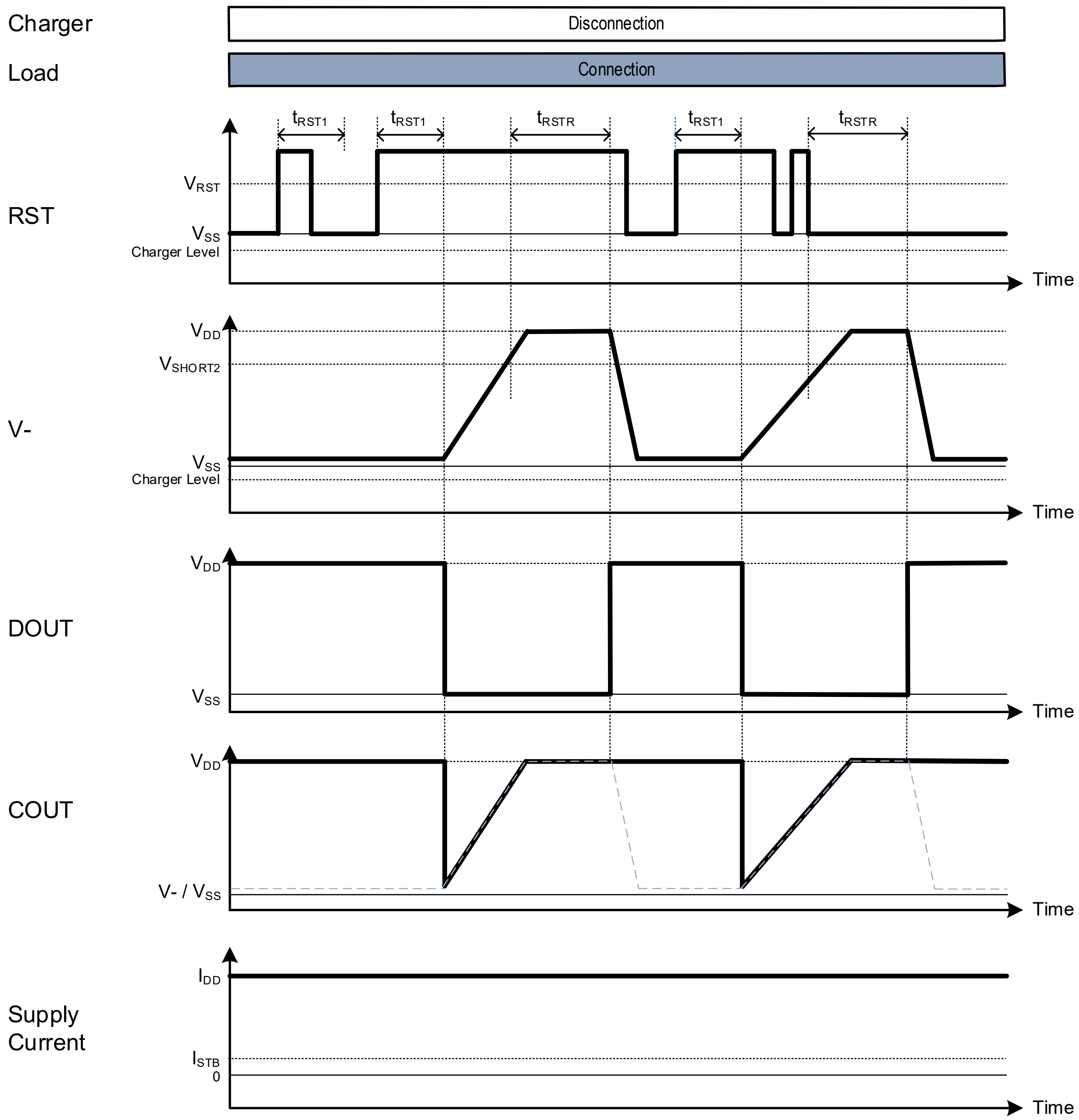


Charge Overcurrent Timing Chart

System Reset

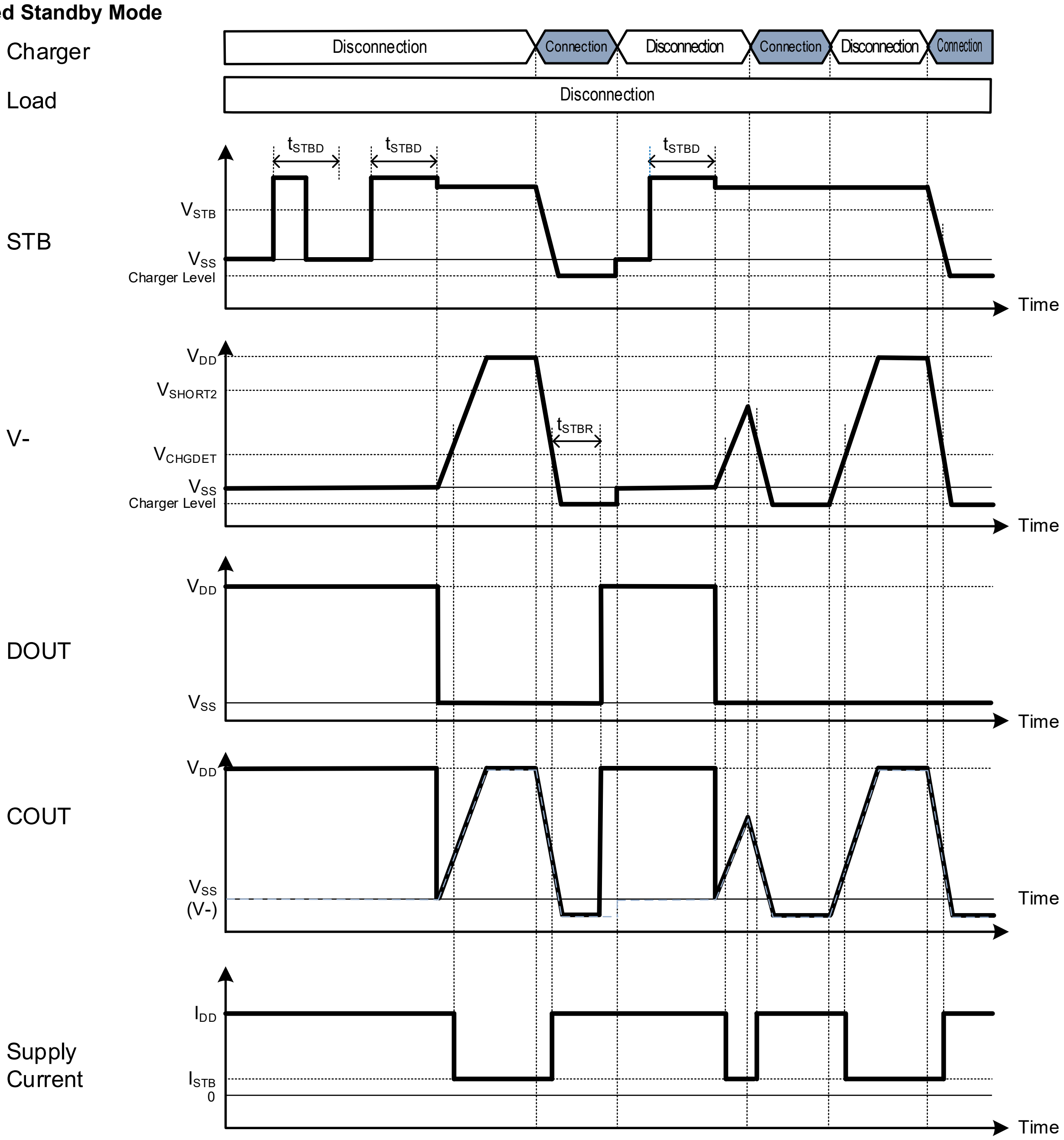


System Reset (Reset Detection: 2nd step detection, Reset Release: Auto release) Timing Chart



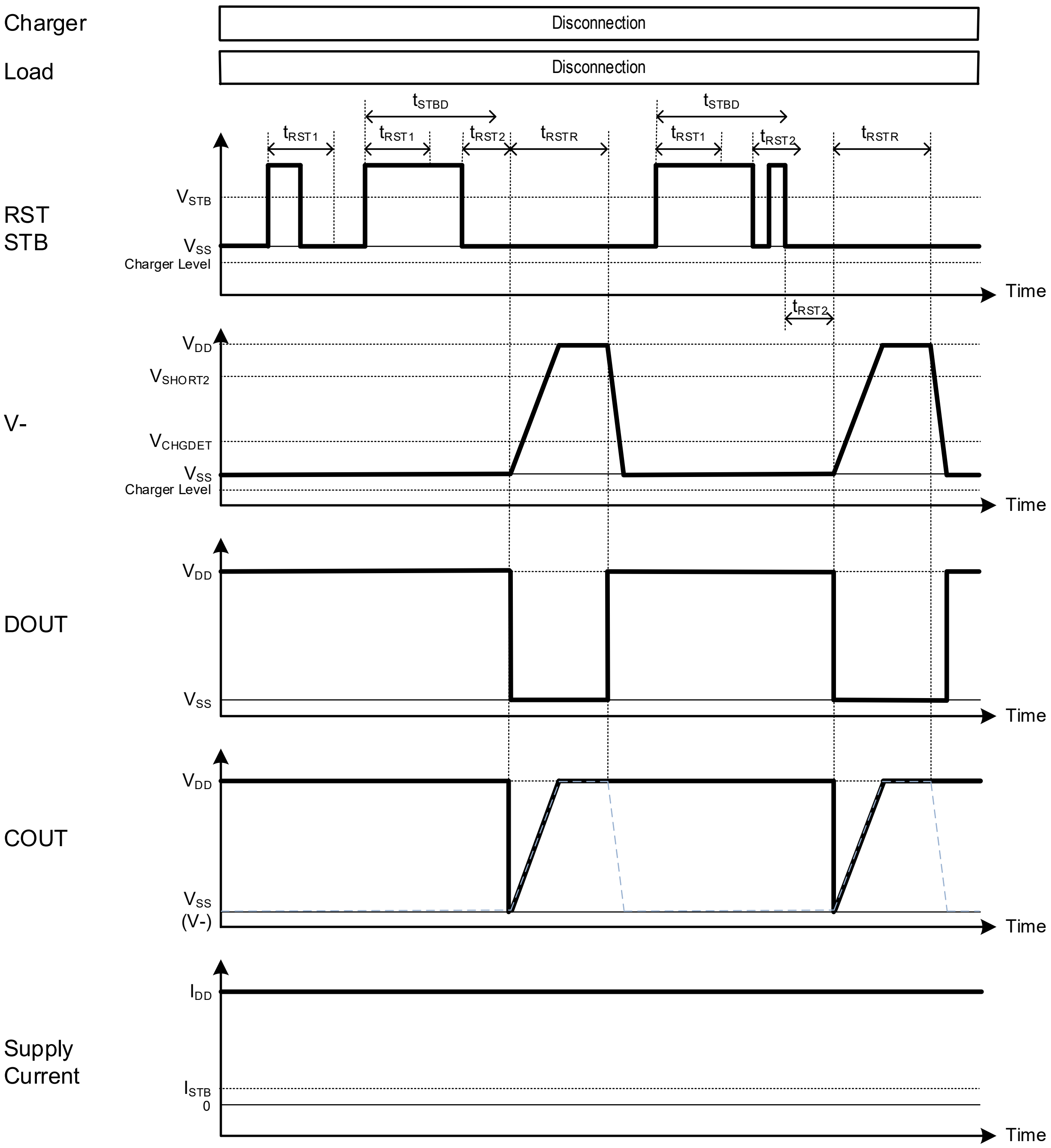
System Reset (Reset Detection: 1st step detection, Reset Release: V- rising) Timing Chart

Forced Standby Mode



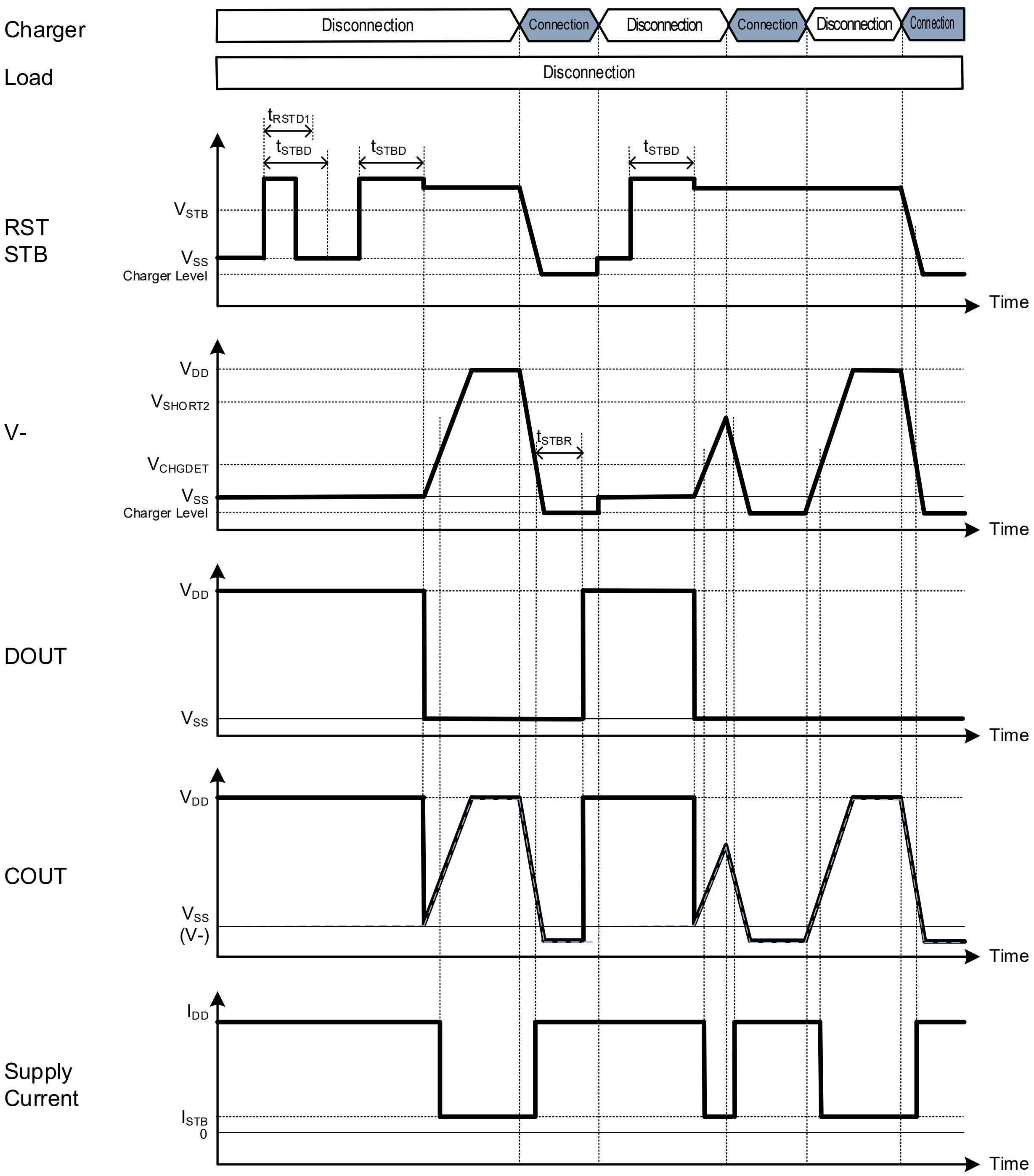
Forced Standby Mode Timing Chart

System Reset (In the case of connecting between the RST and the STB pins)



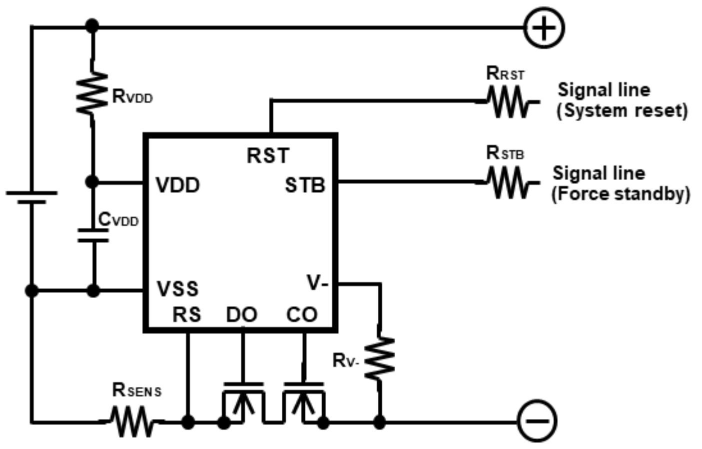
System Reset (Reset Detection: 2nd step detection, Reset Release: Auto release) Timing Chart

Forced Standby Mode (In the case of connecting between the RST and the STB pins)

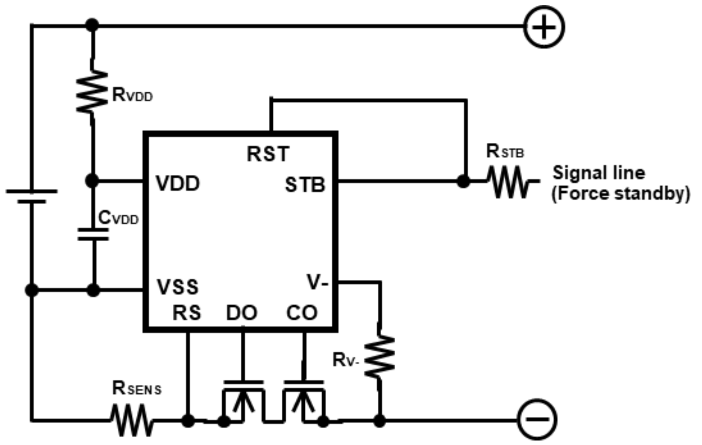


Forced Standby Mode (Reset Detection: 2nd step detection, Reset Release: Auto release) Timing Chart

TYPICAL APPLICATION CIRCUITS



NB7140ZA (Reset Detection at 1st Step) Typical Application Circuit



NB7140ZA (Reset Detection at 2nd Step) Typical Application Circuit

External Components

Symbol	Min.	Typ.	Max.
Resistor			
R_{VDD} *1	-	330Ω	1kΩ
R_{V-} *1	-	1.0kΩ	1.3kΩ
R_{SENS}	-	1.5mΩ	-
R_{STB}, R_{RST}	-	1.0kΩ	10kΩ
Capacitor			
C_{VDD}	0.01µF	0.10µF	1.00µF

*1 The total resistance of R_{VDD} and R_{V-} must be 1kΩ or more.

Technical Notes Related to External Components

- The voltage fluctuation is stabilized with R_{VDD} and C_{VDD}. If a R_{VDD} is too large, the detection voltage rises by the conduction current at detection. To stabilize the operation, it is recommended to use a resistor of 1kΩ or less for R_{VDD} and a capacitor of 0.01 μF to 1.00 μF for C_{VDD}.

- R_{VDD} and R_{V-} serve as a current limit resistor when the battery pack is charged with reversed polarity, or a voltage of the connected charger is more than the absolute maximum rating. When using a small resistor for R_{VDD} and R_{V-}, the device's power dissipation might be exceeded. Therefore, a total of R_{VDD} and R_{V-} must be 1kΩ or more. When using a large resistor for R_{V-}, the charger might not be released by re-connecting to the battery pack after the over-discharge detection. Therefore, R_{V-} must be 1.3kΩ or less. Production variation and temperature properties are included in the value. R_{SENS} is a resistor for sensing an overcurrent. If the resistance value is too large, power loss becomes also large. By the overcurrent, if the R_{SENS} is not appropriate, the power loss may be beyond the power dissipation of R_{SENS}. Choose an appropriate R_{SENS} according to the cell specification.

- The typical application circuit diagrams are just examples. This circuit performance largely depends on the PCB layout and external components. In the actual application, fully evaluation is necessary.

- If the positive terminal and the negative terminal of the battery pack are short even though the device has the short protection circuit, a large current may flow through the FET during the delay time until detecting the short circuit. Therefore, select an appropriate FET with large enough current capacitance to endure the large current during the delay time.

Selection of External Sense Resistor and MOSFET

The short mode is detected by the current base or the relation between V_{DD} at short and total on resistance of external MOSFETs for C_{OUT} and D_{OUT}. When a short circuit detection is required with the current determined by V_{SHORT1}, V_{SHORT2}, and R_{SENS}, the next formula must be true, otherwise, the short current limit becomes (V_{SHORT2}) / (R_{SENS} + R_{SS} (on)).

$$\frac{V_{SHORT2}}{R_{SENS} + R_{SS}(on)} \geq \frac{V_{SHORT1}}{R_{SENS}}$$

V_{SHORT1} = Threshold value of detecting short circuit using R_{SENS} terminal [V]
V_{SHORT2} =Threshold value of detecting short circuit using V- terminal [V]
R_{SENS} = External current sense resistance [Ω]
R_{SS} (on) = external MOSFETs' total ON resistance [Ω]

In the short mode, a short current is determined by the relation between R_{SENS} and V_{SHORT1} value.

TECHNICAL NOTES

A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

- Please evaluate the product at the PCB level before use, as some symptoms may remain that cannot be confirmed by the evaluation at the IC level.
- When using any coating or underfill to improve moisture resistance or joining strength, evaluate them adequately before using. In certain materials or coating conditions, corrosion by contained constituents, current leakage by moisture absorption, crack and delamination by physical stress can happen. If the curing temperature of the coating material or underfill material exceeds the absolute maximum rating, the electrical characteristics of this product may change.
- When performing X-ray inspection in mass production process and evaluation build stage such as the product functions and characteristics confirmation, please confirm X-ray irradiation does not exceed 1.5Gy (absorbed dose for air).

REVISION HISTORY

Date	Version	Changes
June 20, 2022	1.00	First public release
July 12, 2022	1.10	Corrected mistakes in writing.
August 1, 2022	1.20	Added Electrostatic Discharge (ESD) ratings. Corrected mistakes in writing.
September 22, 2022	1.30	Updated timing diagrams in the timing chart section.
November 7, 2022	1.40	Deleted marking information from ORDER INFORMATION and PKG INFORMATION and merge them as Marking Specification. Updated timing diagrams in the timing chart section.

	Set Voltage [V] / Delay Time [ms]																	Optional Function					
	V_{DET1} / t_{VDET1}	V_{REL1} / t_{VREL1}	V_{DET2} / t_{VDET2}	V_{REL2} / t_{VREL2}	V_{DET31} / t_{VDET31}	V_{DET32} / t_{VDET32}	t_{VREL3}	V_{DET4} / t_{VDET4}	t_{VREL4}	V_{SHORT} / t_{SHORT}	V_{NOCHG}	V_{STBD} / t_{STBD}	t_{STBR}	V_{RSTD} / t_{RST1}	t_{RST2}	t_{RSTR}	Unit	Overcharge Release	Overdischarge Release [*1]	Discharge Overcurrent Release	Discharge Overcurrent Detection2 [*2]	0 V Battery Charging [*3]	
NB7140ZA**102DE**E2S	4.450	-	3.100	-	0.0120	-	-	-0.0120	-	0.040	1.10	0.65	-	0.65	-	-	V	Latch	Latch1	Latch	No	No	
	1024	16.0	128	1.05	1024	-	9.0	10.0	4.0	0.28	-	50	4.5	48	-	200	ms						
NB7140ZA**103DE**E2S	4.450	-	3.100	-	0.0120	-	-	-0.0120	-	0.040	2.20	0.65	-	0.65	-	-	V	Latch	Latch1	Latch	No	No	
	1024	16.0	128	1.05	1024	-	9.0	10.0	4.0	0.28	-	50	4.5	48	-	200	ms						
NB7140ZA**102DJ**E2S	4.450	-	3.100	-	0.0120	-	-	-0.0120	-	0.040	1.10	0.65	-	0.65	-	-	V	Latch	Latch1	Auto1	No	No	
	1024	16.0	128	1.05	1024	-	9.0	10.0	4.0	0.28	-	50	4.5	48	-	200	ms						
NB7140ZA**105FK**E2S	4.200	-	3.200	-	0.0200	-	-	-0.0500	-	0.030	-	0.65	-	0.65	-	-	V	Latch	Latch1	Auto1	No	Yes	
	1024	16.0	32	1.05	12.5	-	9.0	10.0	4.0	0.28	-	50	8.5	100	-	200	ms						
NB7140ZA**106GQ**E2S	4.700	4.300	2.100	2.800	0.0050	-	-	-0.0050	-	0.200	2.00	0.65	-	0.65	-	-	V	Auto	Auto	Auto1	No	No	
	1024	16.0	128	1.05	16.5	-	9.0	17.0	4.0	0.28	-	300	33	100	-	512	ms						
NB7140ZA**101AF**E2S	4.250	-	2.900	-	0.0300	0.0450	-	-0.0150	-	0.055	2.50	0.80	-	0.80	-	-	V	Latch	Latch2	Latch	Yes	No	
	1024	16.0	64	1.05	1024	16.5	9.0	17.0	4.0	0.28	-	300	33	48	4.5	512	ms						
NB7140ZA**104AF**E2S	4.250	-	2.900	-	0.0450	0.0600	-	-0.0220	-	0.070	2.50	0.80	-	0.80	-	-	V	Latch	Latch2	Latch	Yes	No	
	1024	16.0	64	1.05	1024	16.5	9.0	17.0	4.0	0.28	-	300	33	48	4.5	512	ms						

[*1] Overdischarge Release Conditions,

Auto (Auto Release): Cell voltage > V_{REL2}

Latch 1: Cell voltage > V_{DET2} under charger connection

Latch 2: Charger connection

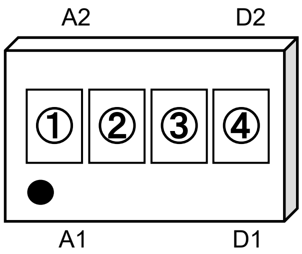
[*2] Yes : Available No: Unavailable

[*3] Yes : Permission No: Inhibition

N B 7 1 4 0 Z A x x x x x E 2 S

- S — Grade (Consumer)
- E 2 — Orientation in taping pocket (E2)
- x x x x x — Series Name
- Z A — Package Type (ZA:WLCSP)

PKG : WLCSP-8-P10



①② : Product code (See below)

③④ : Lot No.(series)

NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

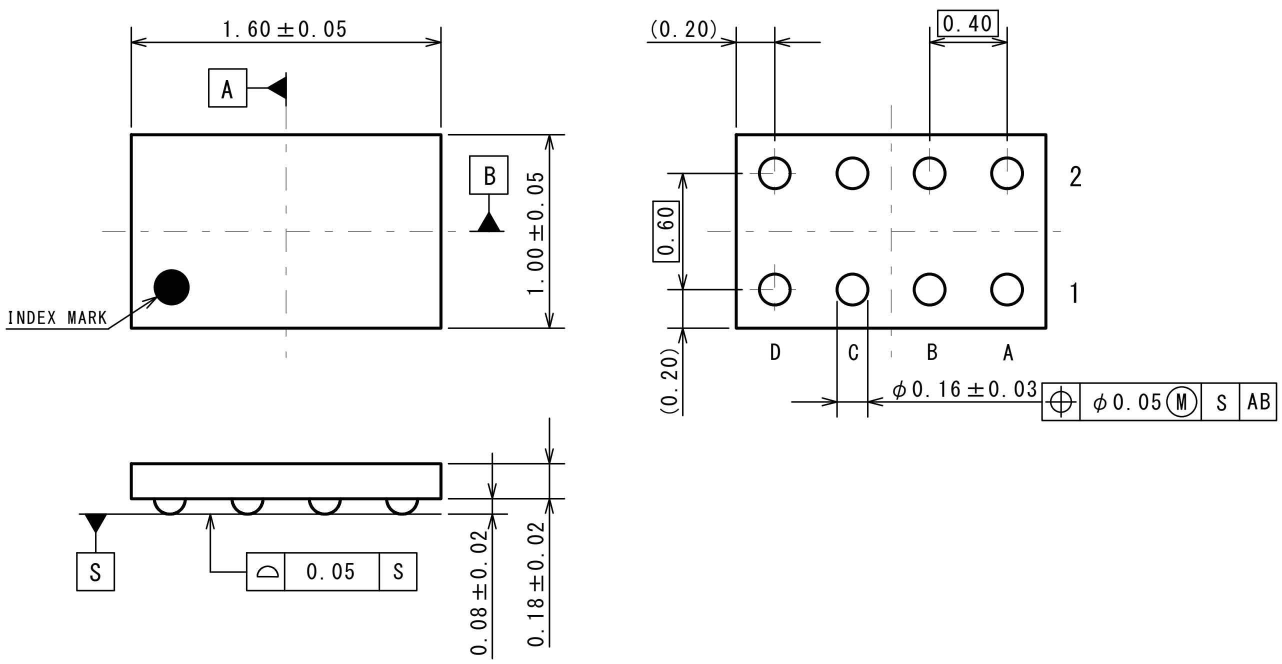
Product Name	① ②
NB7140ZA102DE	T 0
NB7140ZA103DE	T 1
NB7140ZA102DJ	T 2
NB7140ZA105FK	T 3
NB7140ZA106GQ	T 4
NB7140ZA101AF	T 5
NB7140ZA104AF	T 6

Nisshinbo Micro Devices Inc.

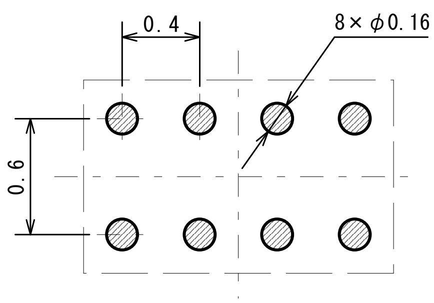
WLCSP-8-P10

■ PACKAGE DIMENSIONS

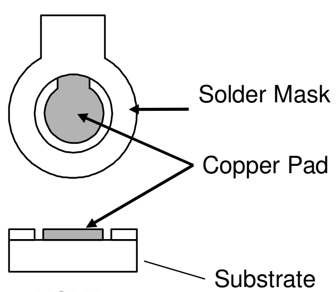
UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS



Recommended Land Pattern



NSMD

NSMD Pad Definition		
Pad definition	Copper Pad	Solder Mask Opening
NSMD (Non-Solder Mask defined)	0.16mm	MIN. 0.26mm

*) Pad Layout and size can modify by customers material, equipment and method.
*) Please adjust pad layout according to your conditions.
*) Recommended Stencil Aperture Size: ϕ0.26mm

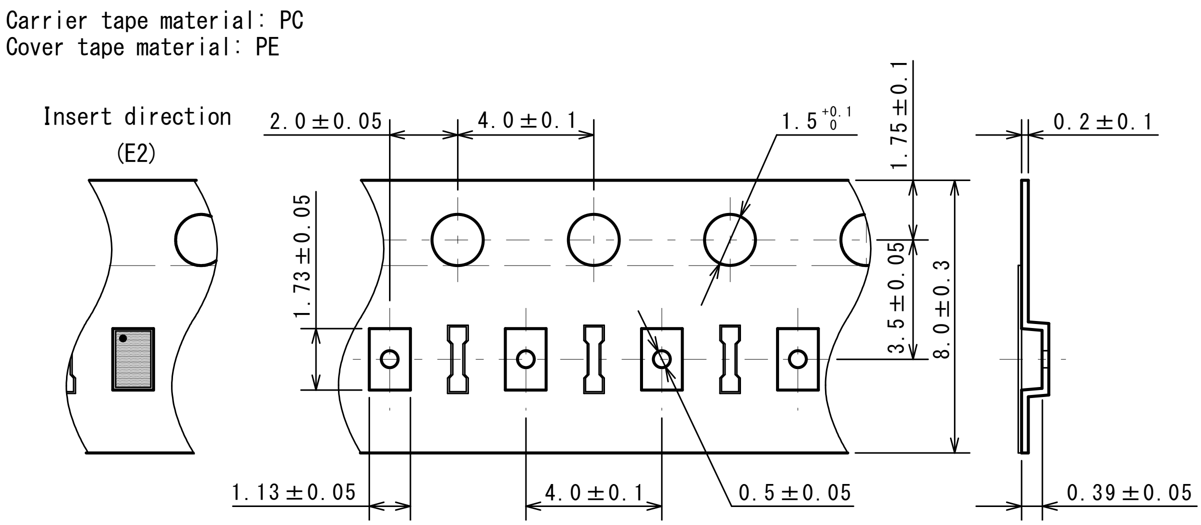
Nisshinbo Micro Devices Inc.

WLCSP-8-P10 PI-WLCSP-8-P10-E-B

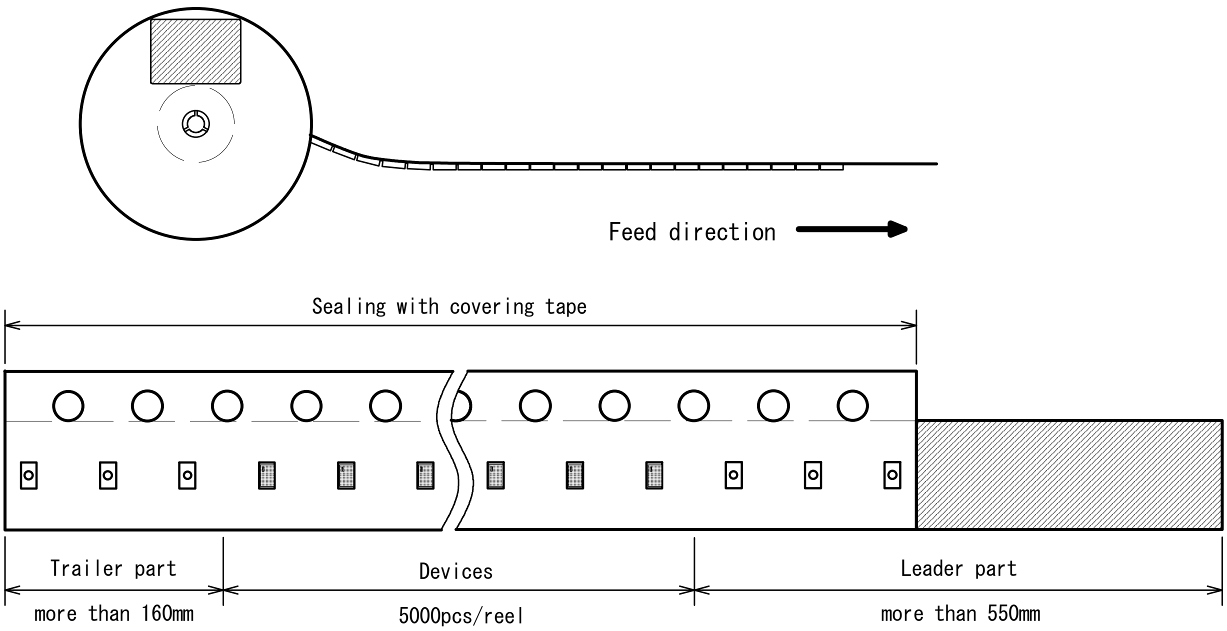
■ PACKING SPEC

UNIT: mm

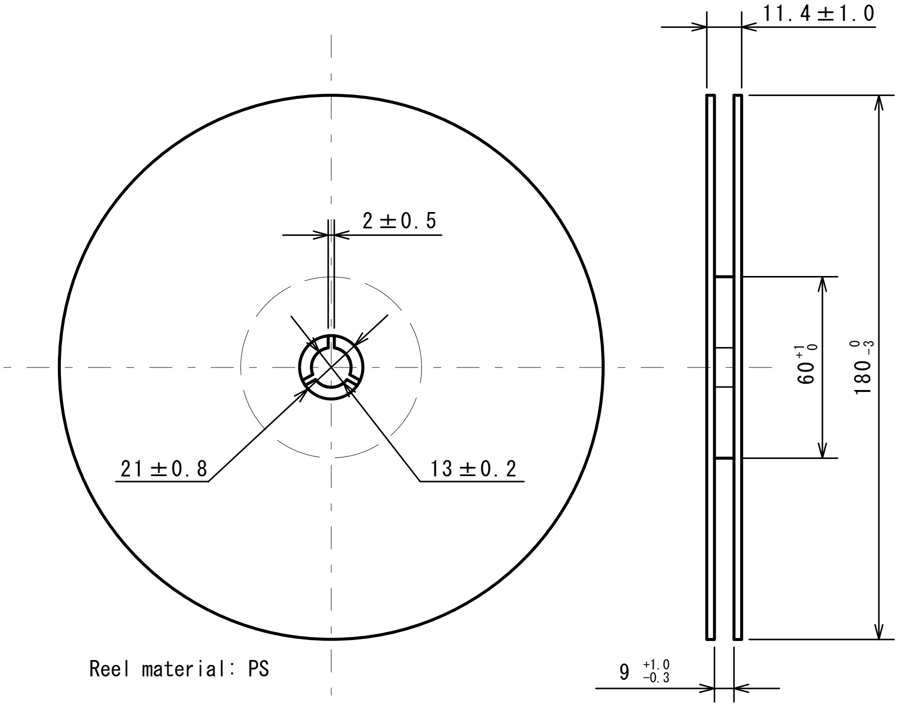
(1) Taping dimensions / Insert direction



(2) Taping state



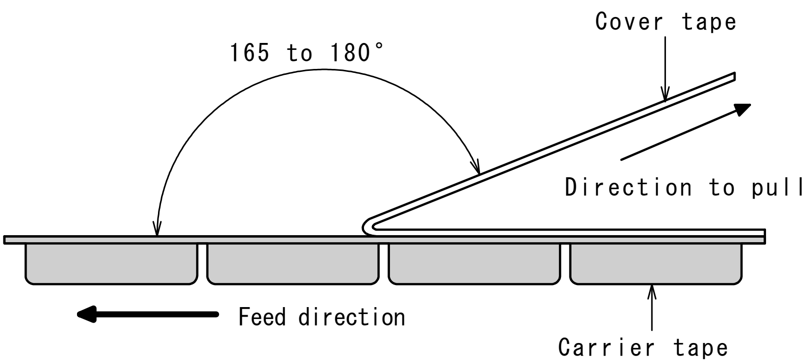
(3) Reel dimensions



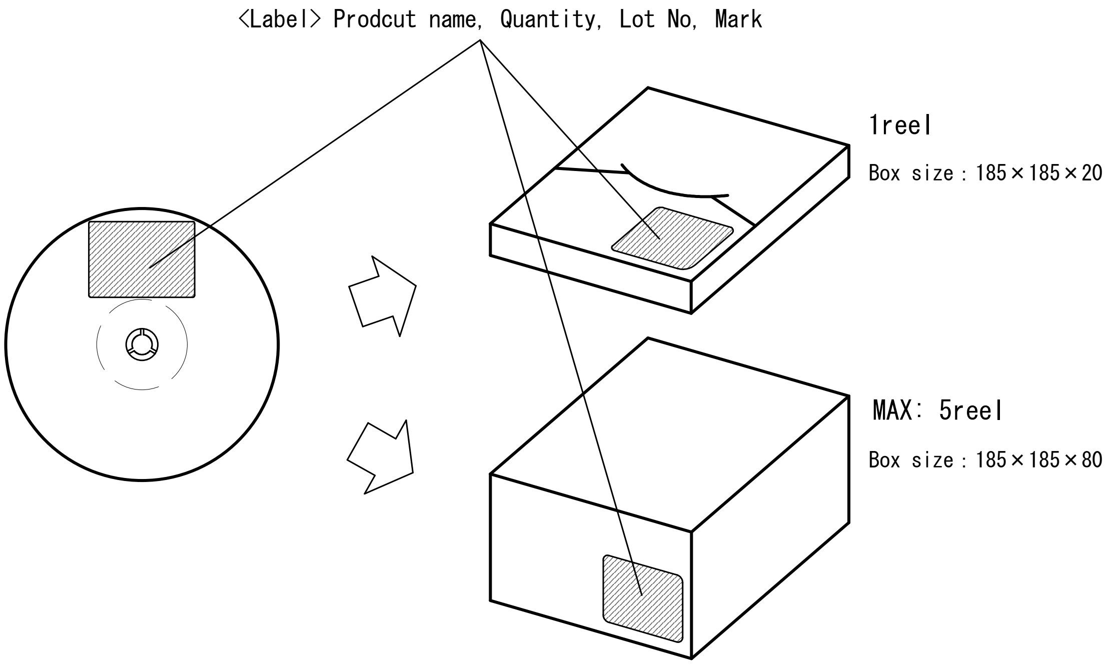
(4) Peeling strength

Peeling strength of cover tape

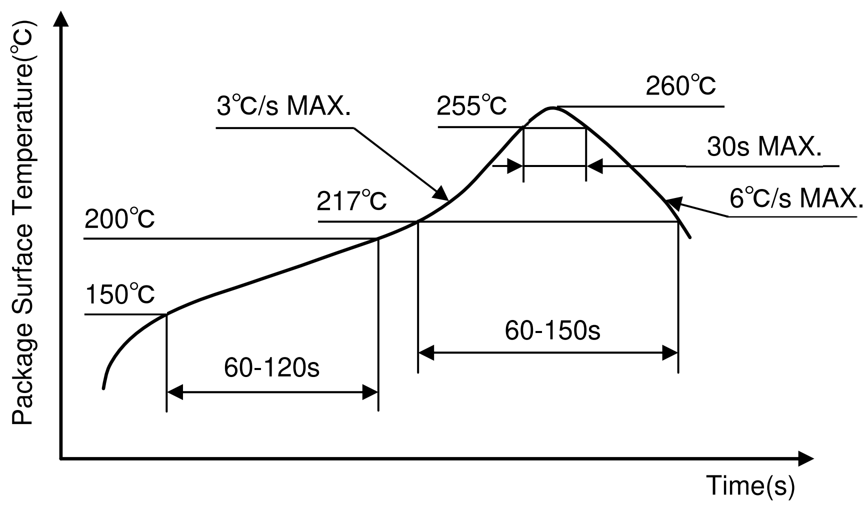
・Peeling angle	165 to 180° degrees to the taped surface.
・Peeling speed	300mm/min
・Peeling strength	0.1 to 1.0N



(5) Packing state

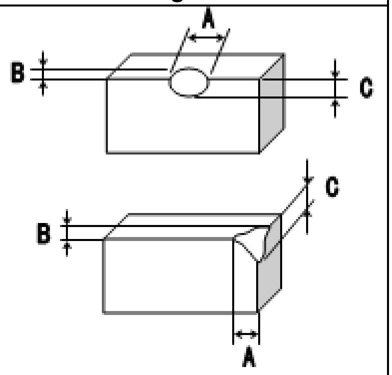


■ **HEAT-RESISTANCE PROFILES**



Reflow profile

Visual Inspection Criteria

No.	Inspection Items	Inspection Criteria	Figures
1	Package chipping	A ≥ 0.2mm is rejected B ≥ 0.2mm is rejected C ≥ 0.2mm is rejected And, Package chipping to Si surface and to bump is rejected.	
2	Si surface chipping	A≥0.2mm is rejected B≥0.2mm is rejected C≥0.2mm is rejected But, even if A ≥ 0.2mm, B ≤ 0.1mm is acceptable.	
3	No bump	No bump is rejected.	
4	Marking miss	To reject incorrect marking, such as another product name marking or another lot No. marking.	
5	No marking	To reject no marking on the package.	
6	Reverse direction of marking	To reject reverse direction of marking character.	
7	Defective marking	To reject unreadable marking. (Microscope: X15/ White LED/ Viewed from vertical direction)	
8	Scratch	To reject unreadable marking character by scratch. (Microscope: X15/ White LED/ Viewed from vertical direction)	
9	Stain and Foreign material	To reject unreadable marking character by stain and foreign material. (Microscope: X15/ White LED/ Viewed from vertical direction)	

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to our sales representatives for the latest information thereon.
2. The materials in this document may not be copied or otherwise reproduced in whole or in part without the prior written consent of us.
3. This product and any technical information relating thereto are subject to complementary export controls (so-called KNOW controls) under the Foreign Exchange and Foreign Trade Law, and related politics ministerial ordinance of the law. (Note that the complementary export controls are inapplicable to any application-specific products, except rockets and pilotless aircraft, that are insusceptible to design or program changes.) Accordingly, when exporting or carrying abroad this product, follow the Foreign Exchange and Foreign Trade Control Law and its related regulations with respect to the complementary export controls.
4. The technical information described in this document shows typical characteristics and example application circuits for the products. The release of such information is not to be construed as a warranty of or a grant of license under our or any third party's intellectual property rights or any other rights.
5. The products listed in this document are intended and designed for use as general electronic components in standard applications (office equipment, telecommunication equipment, measuring instruments, consumer electronic products, amusement equipment etc.). Those customers intending to use a product in an application requiring extreme quality and reliability, for example, in a highly specific application where the failure or misoperation of the product could result in human injury or death should first contact us.
    - Aerospace Equipment
    - Equipment Used in the Deep Sea
    - Power Generator Control Equipment (nuclear, steam, hydraulic, etc.)
    - Life Maintenance Medical Equipment
    - Fire Alarms / Intruder Detectors
    - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
    - Various Safety Devices
    - Traffic control system
    - Combustion equipment

    In case your company desires to use this product for any applications other than general electronic equipment mentioned above, make sure to contact our company in advance. Note that the important requirements mentioned in this section are not applicable to cases where operation requirements such as application conditions are confirmed by our company in writing after consultation with your company.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. The products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. We shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products.
8. Quality Warranty

    8-1. Quality Warranty Period

    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.

    8-2. Quality Warranty Remedies

    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.

    8-3. Remedies after Quality Warranty Period

    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

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