# NPS3102A; NPS3102B

## 12 V, 2 A to 13.5 A, 17 mΩ eFuse

Rev. 1 — 18 July 2024 Product data sheet

## 1. General description

NPS3102A and NPS3102B are low-ohmic (17 mΩ), high current (13.5 A), resettable electronic fuses that are targeted for 12 V applications. They are designed to protect downstream loads from exposure to excessive voltage and protect the power supply from load faults and large inrush currents.

Output slew rate is controlled by a capacitor at dVdt pin. Current limit can be adjusted in the 2 A to 13.5 A range using a resistor at ILIM pin. The voltage at ILIM pin can also be used as a measure of the load current in real-time. The devices include a built-in over voltage clamp that will limit the output voltage during input over voltage conditions.

The devices also include a multi-function EN/FLT pin. When the pin is left floating and the voltage at IN is greater than the under voltage lock-out, the devices turn on. During operation, the voltage at the pin can be used as a fault indicator to determine if the devices are operating normally. Pulling the EN/FLT pin low will turn off the devices.

During thermal shutdown, both devices disable the integrated pass-FET if the die temperature crosses the over temperature threshold. The NPS3102A latches off under a thermal shutdown event and requires user reset by toggling the EN/FLT pin or cycling the voltage at the IN pin. The NPS3102B integrates auto-retry, which safely attempts to re-enable the pass-FET without the need for user intervention.

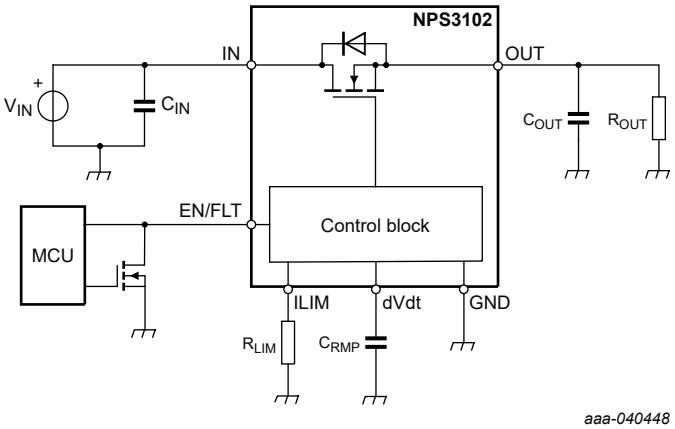


**Fig. 1. Typical Application**

## 2. Features and benefits

- Up to 18 V operating range, 21 V absolute maximum
- Integrated 17 mΩ pass MOSFET
- 15 V output voltage clamp
- 2 A to 13.5 A adjustable output current clamp
- 2 µs short circuit protection response time
- Programmable output rise time control
- Built-In thermal shutdown with fault alert pin
- Fault response options: latch-off, auto-retry
- Leadless plastic package; 10 terminals, body 3.0 x 3.0 x 0.75 mm (DFN3030-10/SOT8037-1)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from $T_j$ = -40 °C to +125 °C

## 3. Applications

- Server
- Solid State Drive (SSD) and Hard Disk Drive (HDD)
- Mobile infrastructure
- Fan control
- Hot-Swap/Plug

# 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| NPS3102AGB<br>NPS3102BGB | -40 °C to +125 °C | DFN3030-10 | leadless plastic package; 10 terminals; body 3.0 × 3.0 × 0.75 mm | SOT8037-1 |

# 5. Marking

**Table 2. Marking codes**

| Type number | Marking code |
|---|---|
| NPS3102AGB | s2A |
| NPS3102BGB | s2B |

# 6. Block diagram

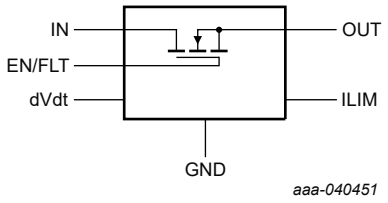


**Fig. 2. Functional diagram**

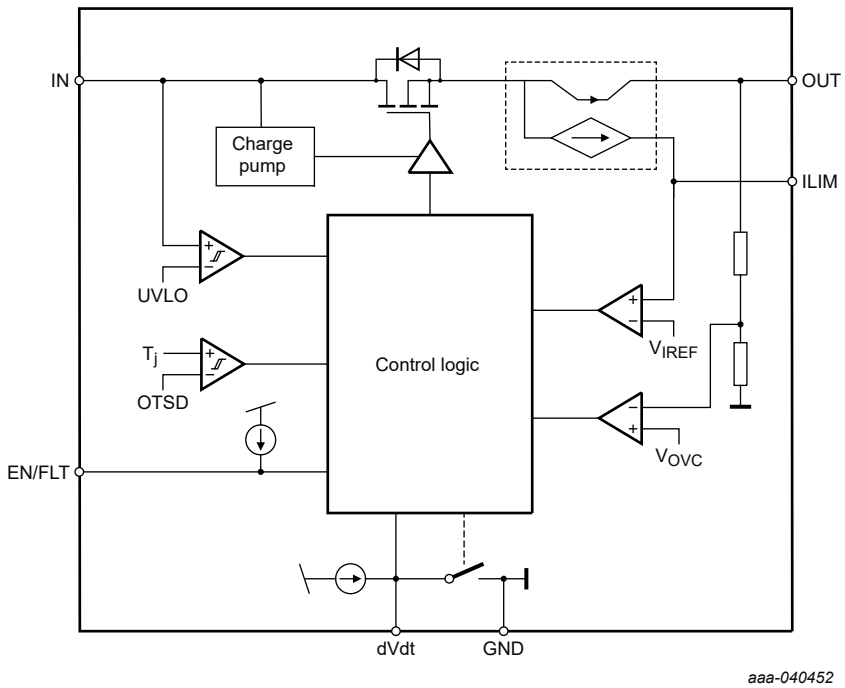


**Fig. 3. Block diagram**

# 7. Pinning information

## 7.1. Pinning

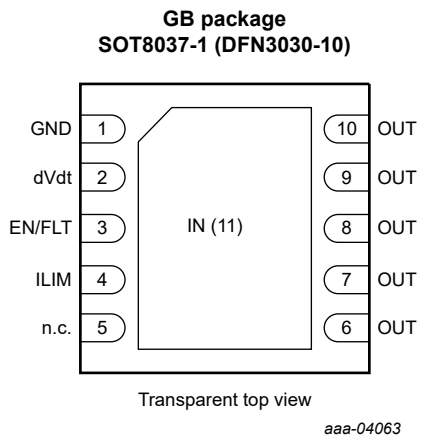


**Fig. 4. Pin configuration SOT8037-1 (DFN3030-10)**

## 7.2. Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| GND | 1 | Ground (0 V) |
| dVdt | 2 | Controls the output voltage rise time once the device has been enabled. Rise times are proportional to the value of the capacitor at this pin. A minimum of 4.7 nF is recommended at this pin. Do not actively drive this pin. |
| EN/FLT | 3 | A 3-state, bidirectional interface that serves to enable/disable the output, and alert monitoring circuits when the eFuse enters or exits thermal shutdown. Do not actively drive this pin to any voltage except for GND. Use an open-drain or open-collector pull-down component to set the EN/FLT logic. See Section 13 for more details. |
| ILIM | 4 | Current limit configuration. Connect a resistor between this pin and GND to set the current limit. The voltage at this pin can be monitored for real-time load current information. |
| n.c. | 5 | Not connected. Do not connect this pin to a trace on the PCB. |
| OUT | 6, 7, 8, 9, 10 | Output voltage of the device, connected to the downstream loads. |
| IN | 11 | Positive input supply voltage to the device. |

# 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | input voltage pin IN | | -0.3 | - | 21 | V |
| $V_{OUT}$ | output voltage pin OUT | | -0.3 | - | $V_{IN}$ + 0.3 | V |
| $V_{EN/FLT}$ | EN/FLT pin voltage | | -0.3 | - | 3 | V |
| $V_{dVdt}$ | dVdt pin voltage | | -0.3 | - | 3 | V |
| $V_{ILIM}$ | ILIM pin voltage | | -0.3 | - | $V_{IN}$ | V |
| $I_{OUT}$ | continuous load current | | internally limited | | | A |
| $T_j$ | junction temperature | | -40 | | Internally Limited | °C |
| $T_{stg}$ | storage temperature | | -65 | | 150 | °C |

# 9. ESD ratings

**Table 5. ESD ratings**

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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD}$ | electrostatic discharge voltage | HBM ANSI/ESDA/JEDEC JS-001 class 2 | -2000 | - | 2000 | V |
| | | CDM ANSI/ESDA/JEDEC JS-002 class C3 | -1000 | - | 1000 | V |

# 10. Recommended operating conditions

**Table 6. Operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | input voltage pin IN | | 9 | - | 18 | V |
| $R_{LIM}$ | external resistor at pin ILIM | | 226 | - | 1870 | Ω |
| $V_{dvdt}$ | voltage rating of external capacitor at dVdt pin | | 6.3 | - | - | V |
| $C_{dvdt}$ | capacitance at dVdt pin | | 4.7 | - | - | nF |
| $T_j$ | junction temperature | | -40 | - | 125 | °C |

# 11. Thermal characteristics

**Table 7. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{\theta ja}$ | junction to ambient thermal resistance | As per JEDEC JESD51-7 | - | 62 | - | °C/W |
| | | 4 layers, 1oz copper, 4 thermal vias | - | 38 | - | °C/W |
| $\Psi_{JT}$ | junction to top characterization parameter | | - | 3.7 | - | °C/W |

# 12. Electrical characteristics

**Table 8. Electrical characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V)*
*$V_{IN}$ = 12 V, EN/FLT = open, $C_{dV/dt}$ = open, $R_{LIM}$ = 604 Ω, $R_L$ = open, $C_{IN}$ = 0.1 µF,*
*$C_L$ = 0.1 µF, unless otherwise stated.*

| Symbol | Parameter | Conditions | $T_j$ = -40 °C to 125 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | |
| **Power consumption** | | | | | | |
| $I_{IN}$ | quiescent current | | - | 320 | 500 | µA |
| $I_{OFF}$ | OFF-state (disabled) current | EN/FLT = GND | - | 100 | 200 | µA |
| $I_{TSD}$ [2] | thermal shutdown current | $T_j = T_{SD}$; EN/FLT is driven to $V_{FAULT}$ by eFuse | - | - | 1000 | µA |
| **Undervoltage lockout** | | | | | | |
| $V_{UVLO\_R}$ | undervoltage lockout rising threshold | EN/FLT changes from $V_{EN\_UVLO}$ to $V_{IPU}$ | 7.8 | 8.4 | 8.9 | V |
| $V_{UVLO\_F}$ | undervoltage lockout falling threshold | EN/FLT changes from $V_{IPU}$ to $V_{EN\_UVLO}$ | 7.0 | 7.6 | 8.1 | V |
| $V_{UVLO\_HYS}$ | undervoltage lockout hysteresis | | - | 0.8 | - | V |
| **Overvoltage and overcurrent protection** | | | | | | |
| $V_{OVC}$ | output voltage clamp | $V_{CC}$ = 18 V; $R_L$ = 100 Ω; | 13.5 | 15 | 16 | V |
| $I_{ILIM}$ [2] | output hold/limit current | $R_{LIM}$ = 226 Ω; $V_{IN}$ - $V_{OUT}$ = 0.5 V | 12.4 | 13.8 | 15.1 | A |
| | | $R_{LIM}$ = 604 Ω; $V_{IN}$ - $V_{OUT}$ = 0.5 V | 5 | 5.55 | 6.1 | A |
| $I_{ILIM\_R\_OPEN}$ | output hold/limit current - open ILIM | $R_{LIM}$ = Open | - | 0 | - | A |
| $I_{ILIM\_R\_SHORT}$ [2] | output hold/limit current - short ILIM | $R_{LIM}$ = 0 Ω | - | 20 | 24 | A |
| $G_{IMON}$ | current monitor gain | $I_{ILIM}$ / $I_{OUT}$ | 184 | 203 | 216 | µA/A |
| **Power MOSFET** | | | | | | |
| $R_{ON}$ | ON-state resistance | | - | 17 | 30 | mΩ |
| $I_{LKG}$ | leakage current (from IN to OUT) | EN/FLT = GND; $R_L$ = 10 kΩ; $T_j$ = 25 °C | - | 0.1 | 6 | µA |
| | | EN/FLT = GND; $R_L$ = 10 kΩ; $T_j$= -40 °C to +85 °C | - | - | 30 | |
| | | EN/FLT = GND; $R_L$ = 10 kΩ; $T_j$ = -40 °C to +125 °C | - | - | 100 | |
| **Bi-directional enable and fault functionality** | | | | | | |
| $V_{IL}$ | input voltage to reset eFuse | EN/FLT pin pulled low externally | - | - | 0.4 | V |
| $V_{IPU}$ | EN/FLT voltage in normal operation | EN/FLT pin voltage set by NPS3102 | 2.2 | 2.35 | 2.5 | V |
| $V_{FAULT}$ | EN/FLT voltage due to thermal shutdown | EN/FLT pin voltage set by NPS3102 | 0.7 | 0.9 | 1.1 | V |
| $V_{EN\_UVLO}$ | EN/FLT voltage when $V_{IN}$ < $V_{UVLO\_F}$ | EN/FLT pin voltage set by NPS3102 | - | - | 0.3 | V |
| $I_{IL}$ | current sourced out of EN/FLT pin when in thermal shutdown | | - | 17 | 25 | µA |
| N [2] | fault signal fanout | number of devices that can be paralleled | - | - | 3 | - |

| Symbol | | Parameter | Conditions | $T_j$ = -40 °C to 125 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| **Thermal shutdown** | | | | | | | |
| $T_{SD}$ | [2] | termal shutdown temperature | rising $T_j$ | 150 | 185 | 200 | °C |
| $T_{HYST}$ | [2] | temperature hysteresis | falling $T_j$ | - | 30 | - | °C |

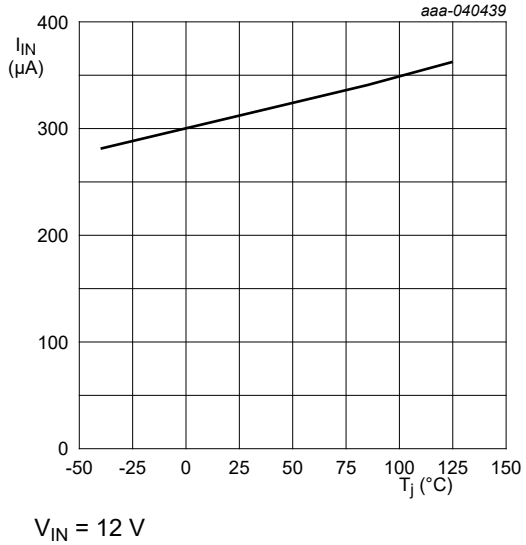
[1] Typical values are measured at $T_j$ = 25 °C.
[2] Not production tested. Guaranteed by Design and/or Characterization.

**Table 9. Dynamic characteristics**

*$V_{CC}$ = 12 V, EN/FLT = open, $C_{dV/dt}$ = open, $R_{LIM}$ = 604 Ω , $R_L$ = open, $C_{IN}$ = 0.1 µF, $C_L$ = 0.1 µF, unless otherwise stated.*

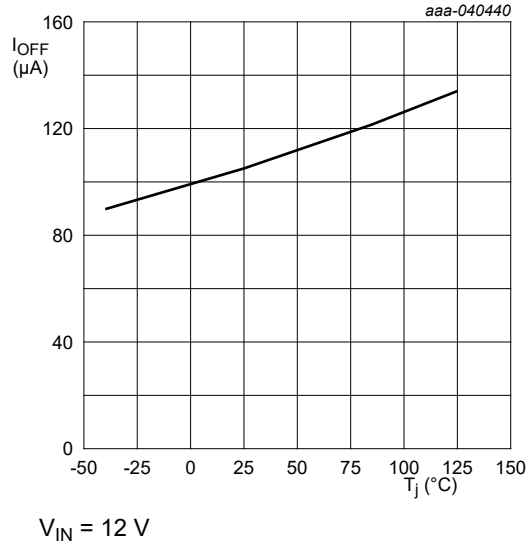
| Symbol | Parameter | Conditions | $T_j$ = -40 °C to 125 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{ONDLY}$ | EN on delay time | $V_{ENFLT}$ = $V_{IPU}$ to $V_{OUT}$ = 10% of $V_{IN}$; $C_{OUT}$ = 10 µF | - | 170 | - | µs |
| $t_{OFFDLY}$ | EN off delay time | $V_{ENFLT}$ < $V_{IL}$ to $V_{OUT}$=90% of $V_{IN}$; $C_{OUT}$ = 10 µF | - | 18 | - | µs |
| SR | output slew rate | $C_{dvdt}$=10 nF; $C_{OUT}$ = 10 µF | - | 3.3 | - | V/ms |
| | | $C_{dvdt}$=33 nF; $C_{OUT}$ = 10 µF | - | 1 | - | V/ms |
| $t_{OVC}$ | output voltage clamp response time | $V_{IN}$ rises above $V_{OVC}$ to peak $V_{OUT}$; $R_L$ = 100 Ω | - | 5 | - | µs |
| $t_{ILIM}$ | output current clamp response time | $I_{OUT}$ > $I_{LIM}$ + 20% to $I_{OUT}$ within 5% of $I_{ILIM}$; $R_L$ = 1.5 Ω | - | 20 | - | µs |
| $t_{SC}$ | output short circuit response time | $I_{OUT}$ > $I_{LIM}$ + 20% to $I_{OUT}$ peak; $R_L$ = 0.1 Ω | - | 2 | - | µs |
| $t_{TSD\_ARI}$ | thermal shutdown auto-retry interval | NPS3102B $T_j$ = $T_{SD}$ - $T_{HYST}$ | - | 1 | 2 | ms |

## 12.1. Typical characteristics graphs




$V_{IN}$ = 12 V

**Fig. 5. Input quiescent current ($I_{IN}$) vs junction temperature**




$V_{IN}$ = 12 V

**Fig. 6. Input disabled current ($I_{IN,OFF}$) vs junction temperature**

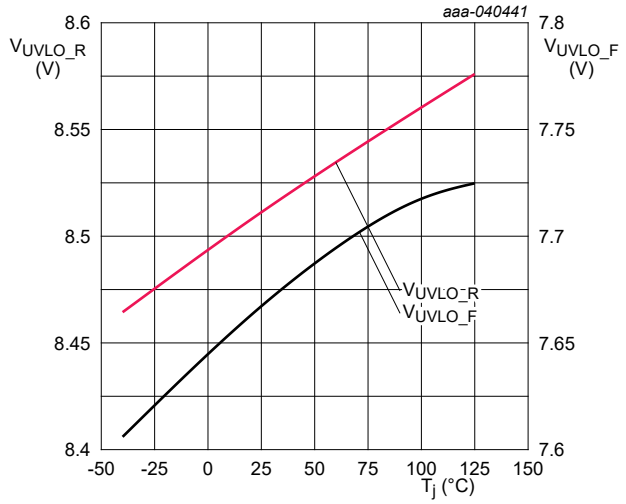
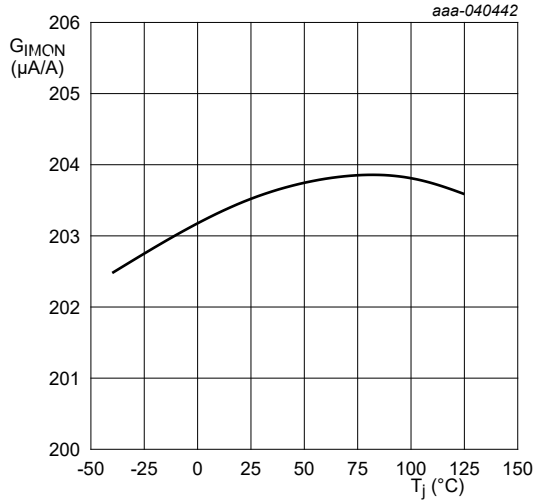
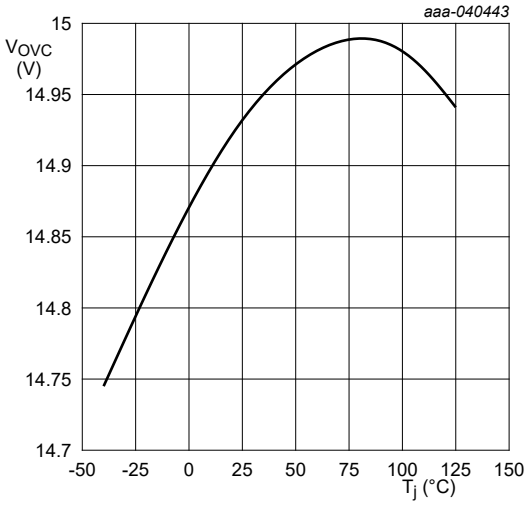



**Fig. 7. UVLO rise and fall thresholds ($V_{UVLO\_R}$) and $V_{UVLO\_F}$) vs junction temperature**



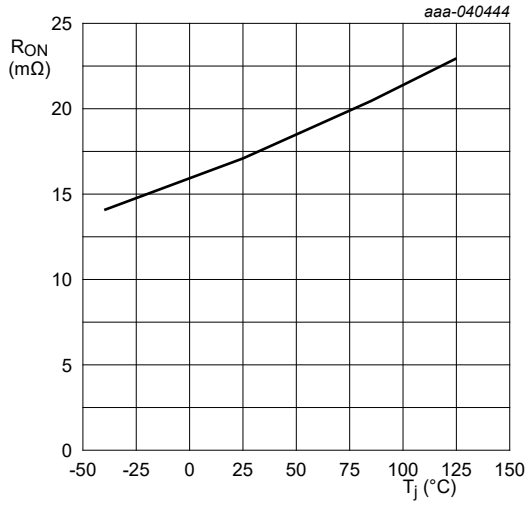

$V_{IN}$ = 12 V

**Fig. 8. Current gain ($G_{IMON}$) vs junction temperature**



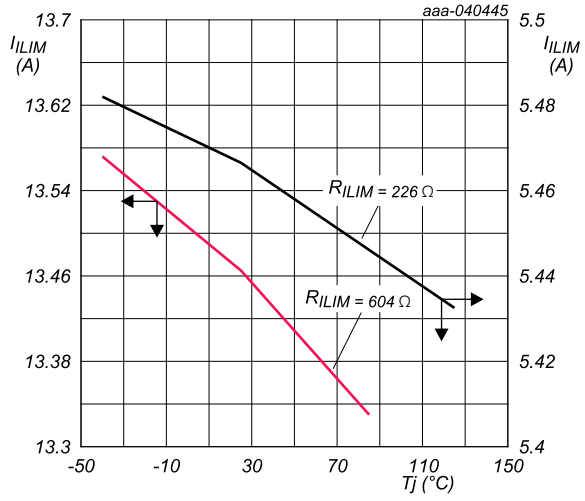

$V_{IN}$ = 18 V

**Fig. 9. Output clamp voltage ($V_{OVC}$) vs junction temperature**



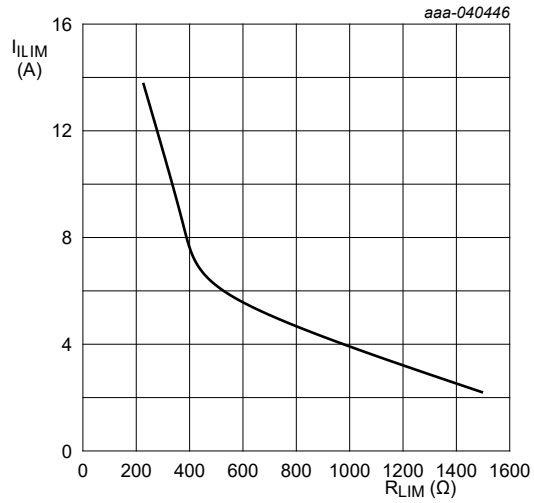

$V_{IN}$ = 12 V

**Fig. 10. On-state resistance ($R_{ON}$) vs junction temperature**



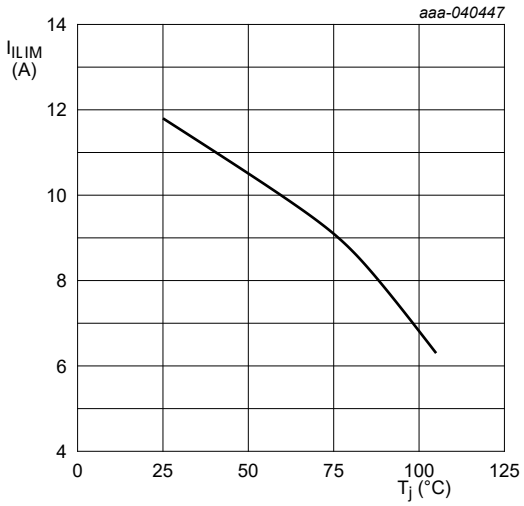

$V_{IN}$ = 12 V

**Fig. 11. Current limit ($I_{ILIM}$) vs junction temperature**




$V_{IN}$ = 12 V; $T_j$ = 25 °C

**Fig. 12. Current limit ($I_{ILIM}$) vs resistance ($R_{LIM}$)**




$V_{IN}$ = 12 V

Load current is current required for junction temperature to reach 125 °C

**Fig. 13. Thermal derating curve**

## 12.2. Typical waveforms

*$V_{IN}$ = 12 V, EN/FLT = open, $C_{dV/dt}$ = 10 nF, $R_{LIM}$ = 1.5 kΩ, $R_L$ = open, $C_{IN}$ = 10 µF, $C_L$ = 10 µF, $T_j$ = 25 °C unless otherwise stated.*

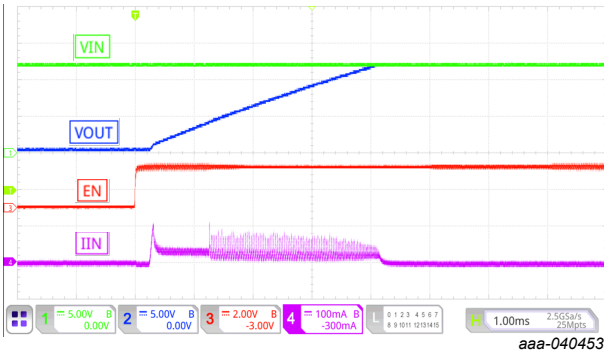
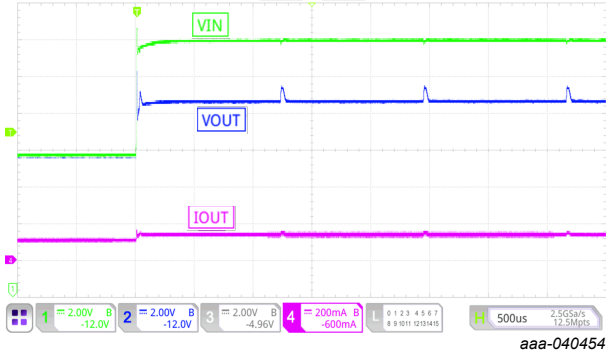
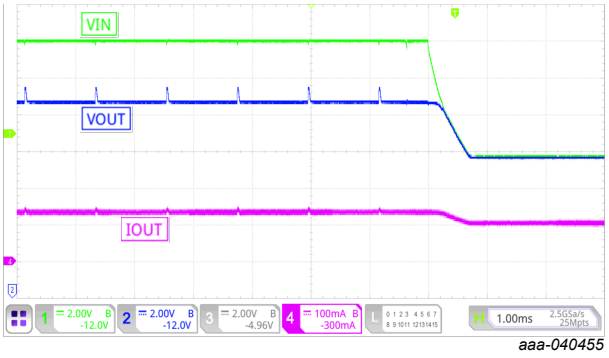



**Fig. 14. Soft start with 10 nF at dVdt pin**



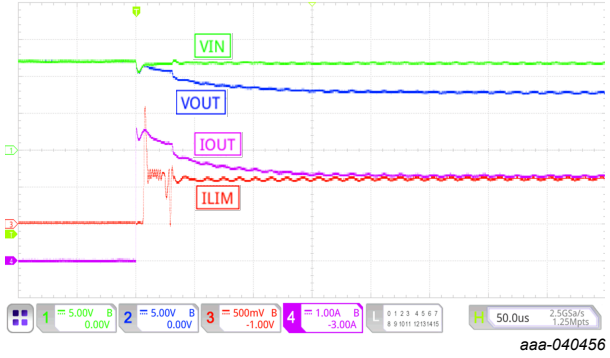

$V_{IN}$ step up from 12 V to 18 V, $R_L$=100 Ω

**Fig. 15. Over voltage clamp operation**



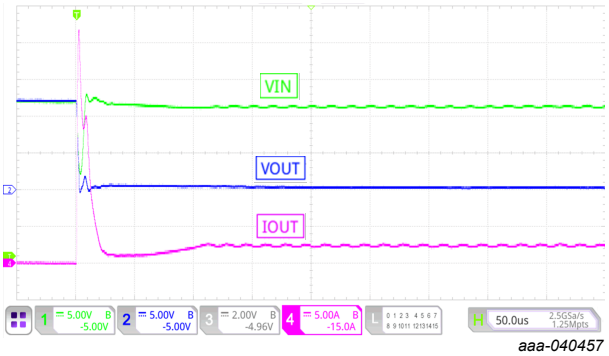

$V_{IN}$ drops from 18 V to 12 V, $R_L$=100 Ω

**Fig. 16. Recovery from an over voltage clamp**



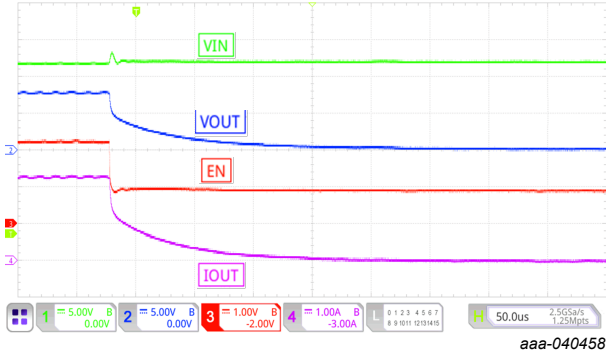

$R_L$ step from open to 3.3 Ω

**Fig. 17. Current limit operation in an overload condition**



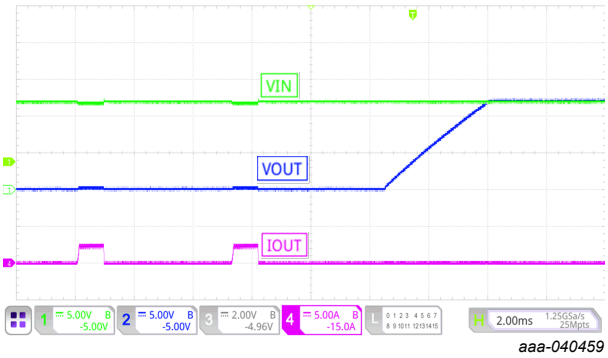

OUT shorted with 0.1 Ω resistor

**Fig. 18. Short circuit response**




$V_{IN}$ = 18 V, $R_L$=100 Ω

**Fig. 19. Over temperature shutdown due to persistent input over voltage**




$R_L$ = 3.33 Ω to open

**Fig. 20. Recovery from over temperature condition for NPS3102B**

# 13. Feature description

## Basic operation

NPS3102 is an electronic fuse device, integrating a low ohmic pass FET along with several system protection features to ensure safe power delivery to a downstream load.

NPS3102 starts its operation by monitoring the voltage on its IN pin and its EN/FLT pin. Once the pin voltages cross their respective thresholds ($V_{UVLO\_R}$ and $V_{IPU}$), NPS3102 will enable the pass FET, delivering power to the load that is connected to the OUT pins. The power ramp is regulated by the configuration of the dVdt pin.

In normal operation, NPS3102 monitors the load current and input voltage, using both characteristics to regulate the pass FET configuration. If the load current crosses the programmed over-current limit threshold ($I_{ILIM}$) or if the load voltage crosses the over-voltage limit threshold ($V_{OVC}$), the device will reduce the conductivity of the pass FET to restrict load current and voltage to the respective threshold values. NPS3102 has a built-in mechanism to provide a rapid protection response to rapid over-current events (i.e., short-circuit).

NPS3102 also integrates a junction temperature monitoring block that will disconnect power delivery before the junction temperature rises to a point where it would be permanently damage the device.

## Start-up

NPS3102 starts up when the input voltage $V_{IN}$ exceeds the rising under-voltage lockout threshold ($V_{UVLO\_R}$) and the voltage at the EN/FLT pin reaches $V_{IPU}$. Both $V_{IN}$ and $V_{EN/FLT}$ are continuously monitored. If the input voltage falls below $V_{UVLO\_F}$ or if the EN/FLT pin voltage drops below $V_{IL}$, the device turns off.

## Soft start

Once the device starts up, the device starts charging the output capacitor at a slew rate determined by the capacitor connected at the dVdt pin. There are a few modes of operation during the soft start period.

- While the EN/FLT pin is held low, the internal charge pump is turned off.
- When the EN/FLT pin exceeds $V_{IPU}$, the internal charge pump is turned on in a low power mode. This mode lasts for approximately 1 ms. This mode is intended to act as a fail-safe to limit the output slew rate in case there is insufficient capacitance at the dVdt pin.
- After the 1 ms time, the charge pump is switched to a high power mode.

Once the charge pump shifts to the high power mode, the device uses an internal resistor divider to step down the output voltage and compares this voltage to the voltage at the dVdt pin.

- If the slew rate of the output voltage is less than the slew rate of the dVdt pin voltage, the charge pump is turned on in the strong mode.
- If the slew rate of the output voltage is more than the slew rate of the dVdt pin voltage, the charge pump is turned off.

Thus, by turning the charge pump off and off, the device regulates the output slew rate to match the slew rate of the dVdt pin.

The capacitor that is required at the dVdt pin can be computed based on the rise time desired for the output voltage.

$$C_{dVdt} = \left(3.4 \times 10^{-6}\right) \times t_R$$

where $C_{dVdt}$ is the capacitor at the dVdt pin and $t_R$ is the desired 10% - 90% rise time of the output voltage.

Fig. 14 shows the start-up waveform with a 10 µF load capacitor and a 10 nF capacitor at the dVdt pin.

Note that the maximum capacitor at dVdt pin is determined by the load capacitance.

$$C_{dVdt,max} = \frac{C_{OUT}}{60}$$

where $C_{OUT}$ is the total output capacitance including those of any downstream loads. For example, a 10 µF load capacitance leads to a maximum capacitance of 167 nF at the dVdt pin.

## Normal operation

Once the device completes inrush, the pass FET is completely turned on to achieve a low on-state resistance. The device constantly monitors the output voltage and the current through the device.

## Output over-voltage clamp

The over-voltage protection in the NPS3102 is designed to be fast acting and consume low power in normal operation. When the NPS3102 is enabled, the over-voltage comparator continuously monitors the OUT pin voltage. Once the OUT pin voltage rises above the threshold value $V_{OVC}$, the internal over-voltage comparator quickly turns off the pass-FET and clamps its gate voltage.

As the output voltage droops due to the load, the IC detects that the output is lower than the clamp voltage. At this point, the device releases the over-voltage circuitry and turns on the pass-FET. This causes the output to rise and detect over voltage (if the input is still above the over voltage limit) and restarts the clamp circuit.

Activation of the over-voltage clamp elevates the power dissipation of the pass FET due to the increased voltage difference between the IN and OUT pins. This increased power dissipation will also elevate the NPS3102 junction temperature, depending on the load current. A prolonged over-voltage condition can increase the junction temperature high enough to trigger a thermal shutdown (see Thermal shutdown protection).

Fig. 15 shows the device entering over voltage protection with a 100 mA load. When the input voltage jumps from 12 V to 18V, the output voltage clamps to 15 V. The short spikes seen in the output voltage are due to the periodic release of the over voltage circuitry as described. Fig. 16 shows the recovery of the part when the input over voltage condition disappears. In both cases, there is no disruption to the load.

## Current monitoring and over current protection

During normal operation, the device constantly monitors the output current ($I_{OUT}$). The current is mirrored and sourced out of the ILIM pin. The ratio of the current sourced out of the ILIM pin and the current through the pass FET is $G_{IMON}$. A resistor to ground at ILIM pin ($R_{LIM}$) converts this current into a voltage ($V_{ILIM}$), which can be used a real time measurement of the load current.

$$I_{OUT} = \frac{V_{ILIM}}{G_{IMON} \times R_{LIM}}$$

$R_{LIM}$ is chosen to program the over current limit ($I_{ILIM}$).

$$R_{LIM} = \frac{0.63V}{G_{IMON} \times I_{LIM}}$$

When the load current exceeds the programmed $I_{ILIM}$ value, the device limits the current to $I_{ILIM}$. This is done in a hysteretic manner by turning the pass FET on and off. The FET turn off is done quickly to ensure no large over current conditions occur, whereas the FET turn-on is controlled so that the hysteresis frequency does not become too large. The device remains in this mode until the overload condition resolves or the device hits its over temperature shut down limit (see Thermal shutdown protection).

Fig. 17 shows the behavior of the device to an over current event. In this case, $R_{LIM}$ is set to 1.5 kΩ, which is about a 2 A current limit. When a 3 A over current event occurs, the device limits the output current to the programmed value. This also causes the output voltage drop and increases the power dissipation in the device (in this case, to approximately 8 W).

The NPS3102 is protected against ILIM pin open or short to ground conditions. If the ILIM pin is left open, the device will not allow any current to pass. If ILIM pin is shorted to ground, then the over current limit is set to 22 A internally. In either case, the device will not get damaged.

## Short circuit protection

When the output of the NPS3102 is shorted to ground, the current through the device increases rapidly. Short circuit protection comparator is activated when the voltage at ILIM pin exceeds 1.2 V. At this point, the device pulls down the gate of the NFET rapidly to prevent high peak currents and limit the output current to the programmed value.

Fig. 18 shows the behavior of the device to a short circuit condition which is initiated by shorting the output with a 0.1 Ω load. The device reduces the gate voltage to the FET within 2 µs, which causes the load current to drop. Once the load current drops to a safe value, the output current limit circuit is engaged.

## Bi-directional enable/fault functionality

The EN/FLT pin is a bi-directional I/O. The pin has a weak pull-up internal to the device. This pin can be used to control the device, monitor the status of the device, and connect multiple devices in parallel.

To use this pin as a control input, connect it to an open-drain FET or a GPIO pin of a micro-controller configured as an open-drain output. Pulling the pin down to GND (less than $V_{IL}$) turns off the NPS3102. Turning off the pull-down FET turns on the NPS3102.

The pin can be used as a status pin by monitoring the voltage at the pin.

Low level ($V_{IL}$) – A voltage below this level indicates NPS3102 has been turned off.

Mid level ($V_{FAULT}$) – A voltage within this range indicates NPS3102 is in Thermal Shutdown.

High level ($V_{IPU}$) – A voltage above this level indicates NPS3102 has been turned ON.

In cases where multiple NPS3102s are used in parallel, the EN/FLT pins of all the ICs need to be connected together to ensure proper operation. NPS3102 is designed to allow up to 3 devices to be connected in parallel (see Paralleling eFuses).

## Thermal shutdown protection

The NPS3102 has internal SOA management to prevent an elevated junction temperature ($T_j$) from permanently damaging the pass FET. In normal operation, the NPS3102 continuously monitors its internal junction temperature. If it crosses the over temperature threshold ($T_{SD}$), the pass FET is disabled and the load is disconnected. The EN/FLT pin will be driven internally to $V_{FAULT}$ while the NPS3102 remains in thermal shutdown (see Bi-directional enable/fault functionality).

In NPS3102A, there are two options to exit thermal shutdown and attempt to resume normal operation

- power cycle the IN pin, or
- toggle the EN/FLT pin.

Note that if $T_j$ has not fallen below ($T_{SD}$ – $T_{HYST}$), NPS3102 will re-enter thermal shutdown.

If user-trigger to resume normal operation is not a viable option, then NPS3102B is recommended due to its auto-retry feature. This feature enables the NPS3102B to automatically resume normal operation once $T_j$ has dropped to ($T_{SD}$ – $T_{HYST}$). Once $T_j$ has sufficiently dropped, the device will wait for an additional delay of $t_{TSD\_ARI}$, and then attempt to re-enable the pass FET. The pin voltage will return to $V_{IPU}$.

- The junction temperature of the NPS3102 can exceed its internal limit TSD in a few scenarios.
- The rms current through the device exceeds the maximum current in the temperature de-rating curve (see Fig. 13)
- The device is in over current protection mode causing excessive power dissipation
- The device is in the over voltage clamp mode with a load current causing excess power dissipation
- Start-up with a large load capacitor which causes excessive power dissipation.

Behavior of the NPS3102 to an over temperature condition is shown in Fig. 19. In this case, a persistent over current condition causes the device to heat up and shut down. When the device shuts down, the EN/FLT pin is pulled to $V_{FAULT}$ to indicate that the device is in thermal shutdown.

Fig. 20 shows the recovery of the NPS3102B device from a persistent overload condition. The device keeps trying to restart until both the over temperature condition and overload conditions disappear. At this point, the device enters soft start and ramps up the load capacitor.

# 14. Application information

## Basic operation

The NPS3102 is an electronic fuse intended to overcome the disadvantages of one shot fuses, PTC fuses or discrete protection circuits. It protects the downstream components against overvoltage and limits the maximum current flow during a fault ensuring maximal safety. With an input voltage range of 9 V to 18 V and a programmable current limit between 2 A and 13.5 A, it can be used in a broad range of applications where protection is needed.

## Typical standalone application

Fig. 21 depicts a standard standalone application. This application is designed to limit the current to 13.5 A and an output voltage rise time of 3 ms.

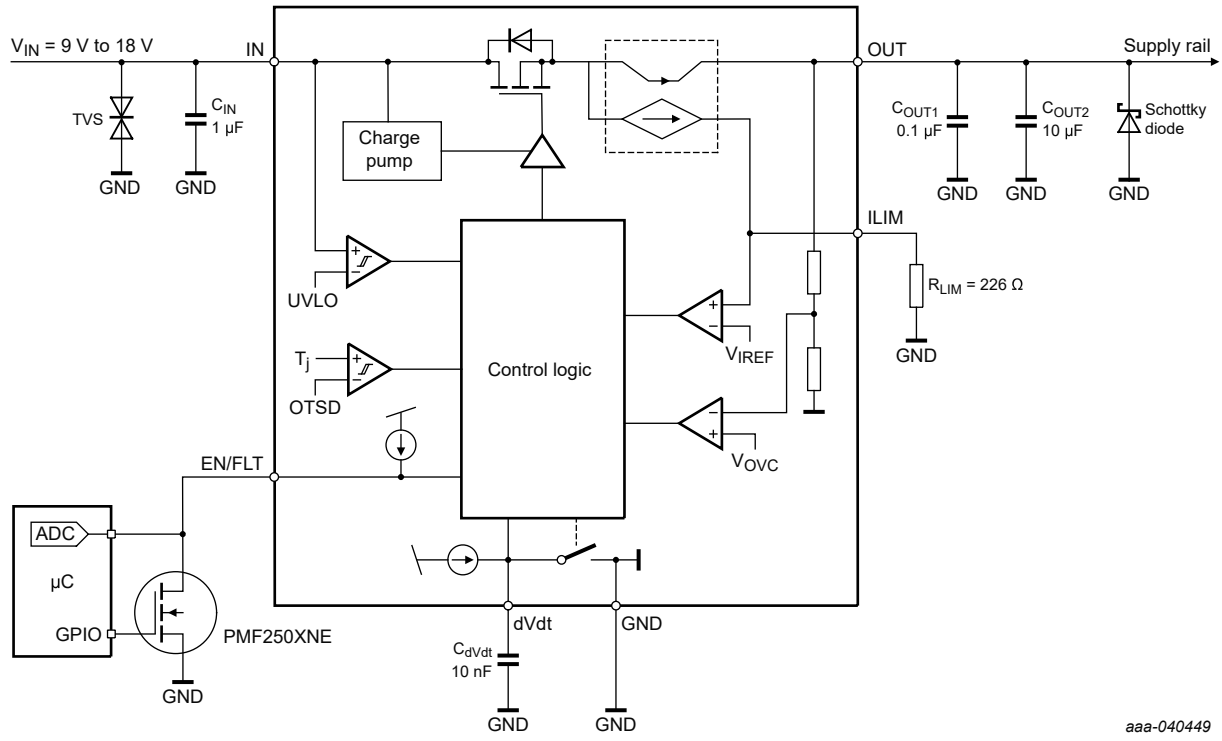



**Fig. 21. Typical standalone application schematic**

The current limit threshold is controlled by the value of $R_{LIM}$ and can be calculated by:

$$R_{LIM} = \frac{0.63V}{G_{IMON} \times I_{LIM}} = \frac{0.63V}{203\frac{\mu A}{A} \times 13.5A} = 229\Omega$$

Rounded to an E96 resistor value this result in 226 Ω.

Both $C_{IN}$ and $C_{OUT}$ are needed for decoupling and transient suppression. The input transient voltage suppressor protects the eFuse against large voltage transients that might exceed the recommended voltage operating range during switching of load circuitry. These transients might occur due to parasitic inductance from the supply connection to the input of the eFuse. The Schottky diode on the output protects the eFuse from negative voltage transients. Both the TVS and the Schottky diode can be omitted, but for robustness, these are recommended. $C_{dVdt}$ sets the output slew rate to 3 ms as per the equation below.

$$C_{dVdt} = \left(3.4 \times 10^{-6}\right) \times t_R = \left(3.4 \times 10^{-6}\right) \times 3ms = 10.2nF$$

Rounding the value to a standard value results in a 10 nF capacitor at dVdt pin. It is recommended to choose either a ≥6.3 V rated NP0/C0G or a ≥10 V rated X7R capacitor to minimize capacitance change due to DC bias. The minimum slew rate achievable is 1 ms, which occurs when the dVdt pin is left floating.

The bi-directional EN/FLT pin is used to disable the device using an open drain NMOS which in turn is controlled by a micro controller. During normal operation, the voltage of the EN/FLT pin can be monitored using an ADC to monitor fo fault situations. The voltage across $R_{LIM}$ can be used as a real time current monitor and can also be connected to an ADC. When using an analog switch both signals can be monitored sequentially.

If the input range of the ADC is lower than the maximum voltages at either EN/FLT or ILIM pins, the voltages need to be stepped down using external buffers. The pins are not capable of sourcing more than 1 µA to external circuitry.

## Paralleling eFuses

If the current rating of a single eFuse is insufficient, or if there is a need to distribute power dissipation across the PCB, it is possible to parallel a maximum of three eFuses. Fig. 22 illustrates the appropriate connection of these devices.

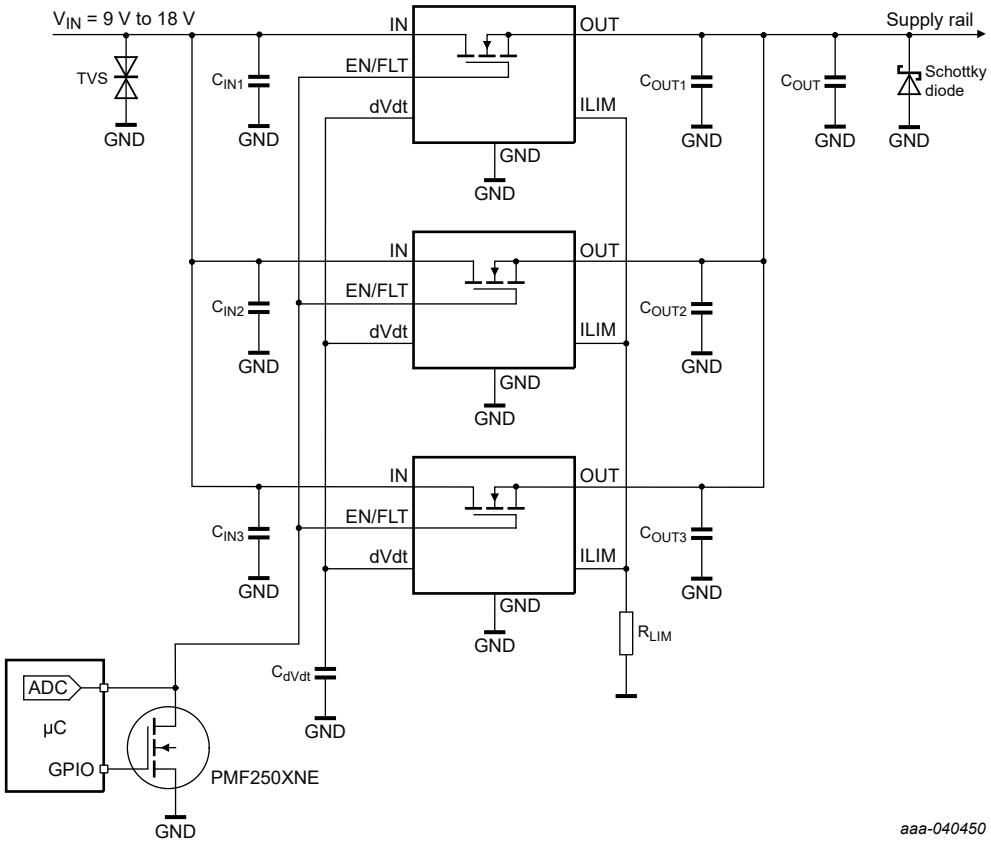



**Fig. 22. Parallel operation of eFuses**

Several considerations must be taken into account:

- The current charging the dVdt capacitor will be three times the value of a single device, resulting in a ramp rate that is three times faster, if the capacitor is not adjusted accordingly.
- The current through the current-limiting resistor will be three times the value of a single device. Since the voltage across this resistor triggers the current-limiting circuit, it should be one-third of the value of a single device.
- EN/FLT pins should be tied together. In the event that one device enters thermal shutdown, the voltage on this pin will trigger the other eFuses to enter thermal shutdown as well.
- Each device should have its own decoupling capacitors at input and output pins.
- Careful attention must be paid to the layout. The distribution of current will significantly depend on the added series resistance, which should be equal for every eFuse. Failure to comply may result in variations in power dissipation per product, potentially leading to thermal shutdown of the system.

## PCB Layout

Fig. 23 depicts a proven layout example. Both $C_{IN}$ and $C_{OUT}$ should be as close as possible to the device to keep the inductivity of the current loop as low as possible. Transient protection devices can be placed next to these capacitors.

To prevent unwanted activation of the thermal protection, it is advised to connect as much as possible copper area to the exposed pad of the device using thermal via's in the pad distributing the dissipated power to the $V_{CC}$ plane.

To optimize the thermal performance of the device, it is important to design the board stack-up and copper areas on each layer correctly. A stack-up example based on the NPS3102 evaluation module is shown in Fig. 24. The minimum copper areas connected to the thermal pad of the IC for each layer is listed in Table 10. Using this PCB stack-up and a similar layout, it is possible to achieve a junction to ambient thermal impedance of 33 °C/W.

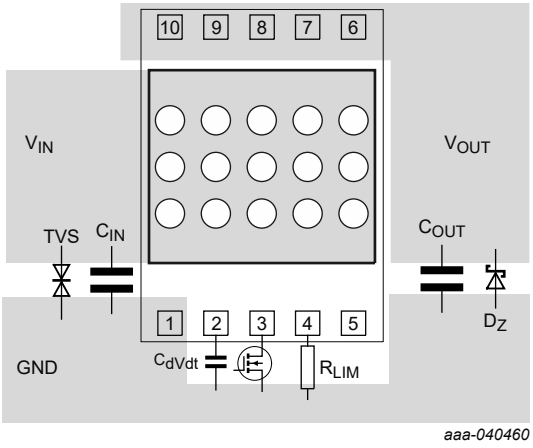



**Fig. 23. Recommended Layout**

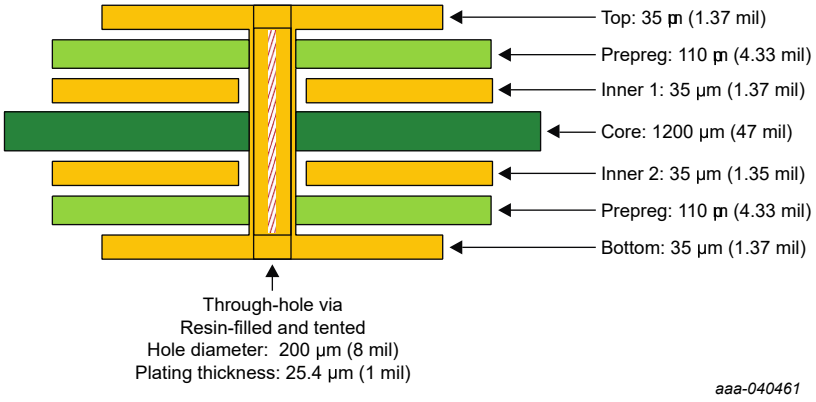


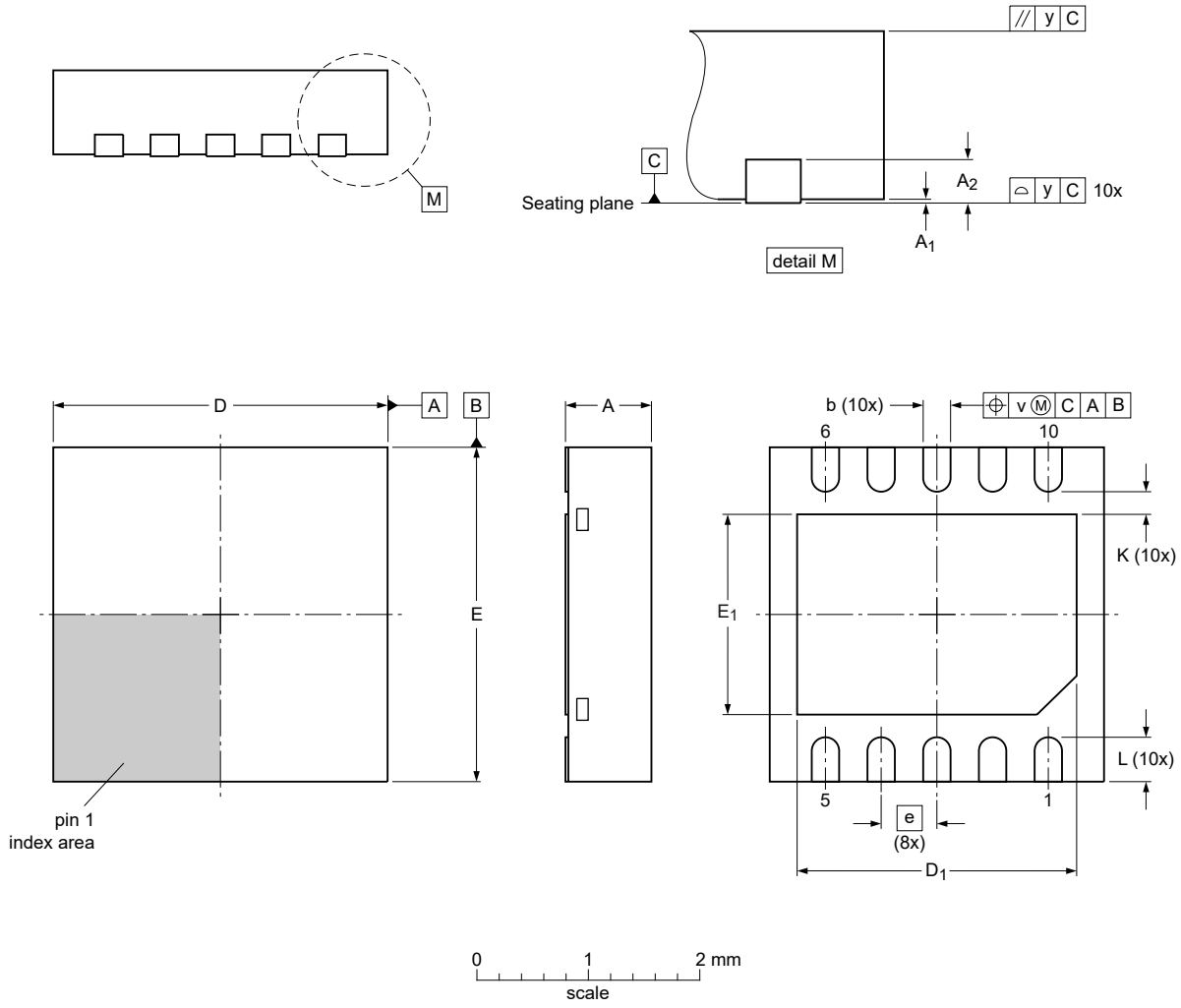

**Fig. 24. Recommend PCB Stackup**

**Table 10. Recommended copper area in each layer**

| Layer | Minimum Copper area connected to thermal pad | Number of vias in thermal pad |
|---|---|---|
| Top | 30 $mm^2$ | 15 vias arranged in a 5 x 3 pattern |
| Inner 1 | 100 $mm^2$ | |
| Inner 2 | 20 $mm^2$ | |
| Bottom | 50 $mm^2$ | |

## 15. Package outline

**DFN3030-10: Leadless plastic package; 10 terminals, body 3.0 x 3.0 x 0.75 mm** **SOT8037-1**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | $A_2$ | b | D | $D_1$ | E | $E_1$ | e | L | K | v | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.80 | 0.05 | | 0.30 | 3.05 | 2.55 | 3.05 | 1.85 | | 0.45 | | | |
| | nom | 0.75 | 0.03 | (0.20) | 0.25 | 3.00 | 2.50 | 3.00 | 1.80 | 0.50 | 0.40 | (0.2) | 0.10 | 0.05 |
| | min | 0.70 | 0.00 | | 0.20 | 2.95 | 2.45 | 2.95 | 1.75 | | 0.35 | | | |

*sot8037-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT8037-1 | | | | | | ~~21-10-13~~ 24-06-27 |

**Fig. 25. Package outline SOT8037-1 (DFN3030-10)**

# 16. Abbreviations

**Table 11. Abbreviations**

| Acronym | Description |
|---|---|
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| PCB | Printed-Circuit Board |
| TDB | To Be Determined |

# 17. Revision history

**Table 12. Revision history**

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| NPS3102 v.1 | 20240718 | Product data sheet | - | - |

# 18. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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**Date of release: 18 July 2024**