

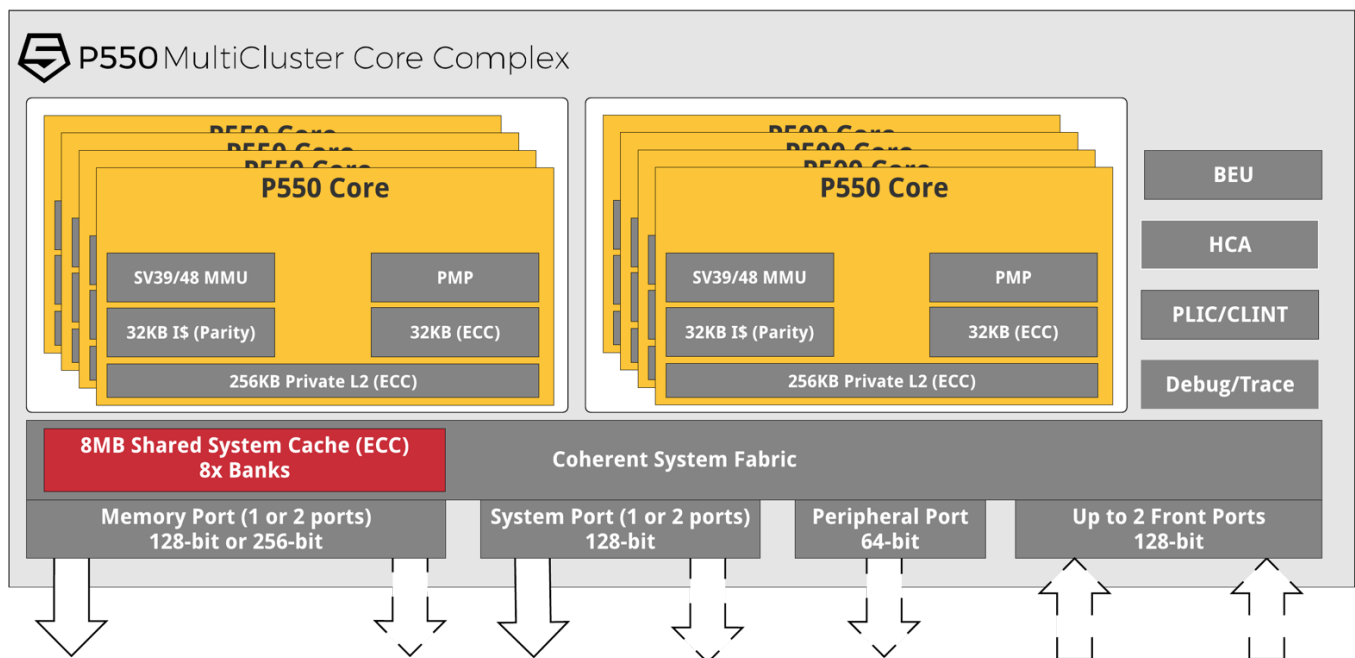
SiFive Performance P550

The **SiFive® Performance™** P550 is a 64-bit RISC-V ISA, triple-issue, out-of-order, thirteen-stage pipeline processor offering the highest performance within a tightly constrained power and area footprint.

The **SiFive Performance** family of processors is designed for maximum throughput, while preserving power and area efficiency for workloads as varied as branch-intensive operating systems and multimedia processing.

Building on the robust foundations of the comprehensive **SiFive® Essential™** product portfolio, the P550 enhances the high-end capability with a feature set designed to offer the utmost flexibility to a designer, targeting applications requiring the most demanding computational capabilities.

The finely tuned combination of out-of-the-box features, high level of configurability, and design scalability ensures designers can achieve the optimal balance of power, performance, and area requirements while achieving the fastest time to market.



SiFive Performance P550 Key Features

- 64-bit RISC-V ISA
- Thirteen-stage, three issue, out-of-order pipeline tuned for scalable performance
- Multi-core, multi-cluster processor configuration options, with up to 8 cores
- Multiple data-types supported for integer, floating point, and DSP compute requirements
- SECCED ECC with Error Reporting
- Multi-layer caching support for optimum data movement
- Private L2 Caches and streaming prefetcher for improved memory performance
- Cache stashing to Level 3 cache for tightly coupled accelerators
- High performance memory subsystem
- Memory parallelism provides cache miss tolerance
- Virtual memory support, with up to 48-bit addressing, with precise exceptions
- High performance, flexible connectivity to SoC peripherals

Memory System And Caches

The P550 memory system has been tuned for high performance workloads. The instruction memory system consists of a dedicated 32KB 4-way set-associative L1 instruction cache with a line size of 64 bytes. The data memory subsystem has a 4-way set-associative 32KB write-back L1 data cache that supports 64-byte cache lines.

The private L2 cache is a 256KB 8-way set-associative cache with a line size of 64 bytes.

A flexible Level 3 cache can be configured to be either 1MB, 2MB or 4MB, with a multi-cluster option of 8MB.

P550 Ports

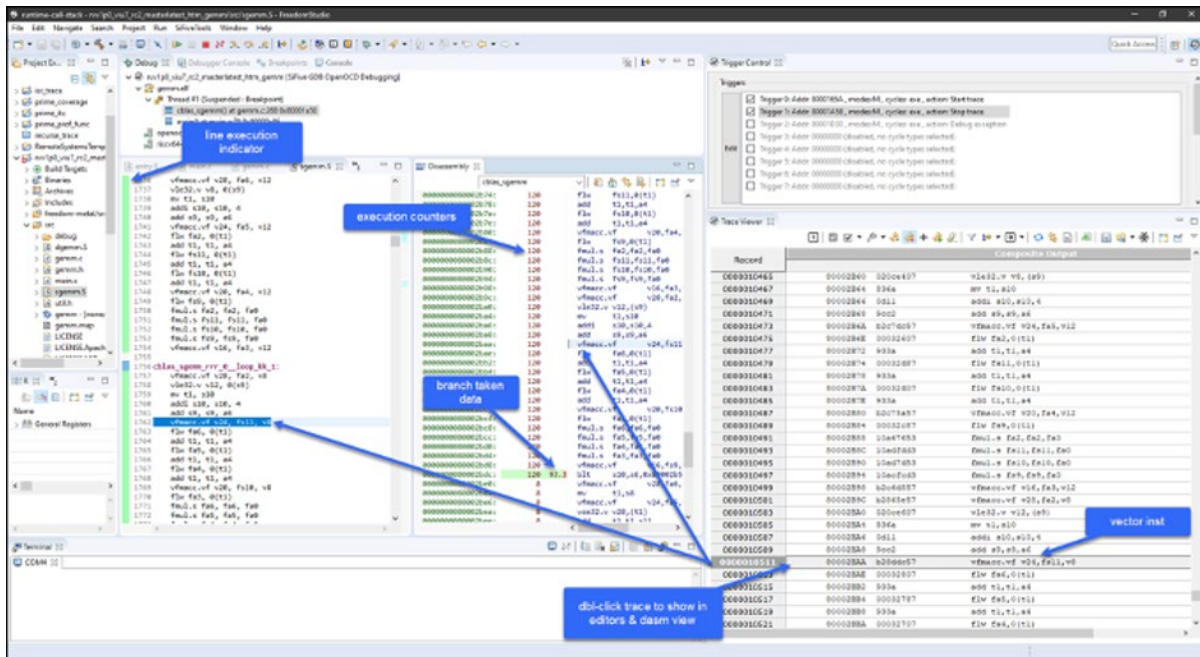
For maximum flexibility in moving data in and out of the processor for general purpose I/O or other more demanding system components like DMA, there are several ports within the bus matrix that are available. These ports provide connection interfaces to external system memories and peripherals and are shared across all processors in a multi-core, multi-cluster configuration.

Memory Port 1 or 2 ports	Arm® AMBA® AXI4™ 256-bit	<ul style="list-style-type: none"> • Interface with memory that offers the highest performance • The only cacheable region of memory support accesses for data and instructions • Supports up to 128 outstanding transfers per memory port
System Port 1 or 2 ports	AXI4 64-bit	<ul style="list-style-type: none"> • Used typically for high-bandwidth, uncached memory or devices
Peripheral Port 1 port	AXI4 64-bit	<ul style="list-style-type: none"> • Interface with lower speed peripherals • Supports code execution • supports the RISC-V standard Atomic (A) extension
Front Port 1 or 2 ports	AXI4 256-bit	<ul style="list-style-type: none"> • External Initiators for accessing on Core Complex devices and ports • Transactions through the Front Port are coherent with L1 Data Caches

Advanced Software Development Capabilities

SiFive Freedom Studio, built on top of the popular Eclipse IDE, is the fastest way to get started programming with your SiFive hardware. Freedom Studio is packaged with a pre-built tool suite, example projects, and includes comprehensive support for SiFive Insight Advanced Trace and Debug capabilities.

Multiple execution targets are supported by Freedom Studio, including simulation models and a variety of FPGA platforms, in addition to fully featured silicon-based development boards. Freedom Studio is supported on Windows, macOS, and Linux host computers.



Comprehensive Linux Support

SiFive includes and supports Linux FPGA bitstreams for all the **SiFive Intelligence™**, **SiFive® Performance™**, and **SiFive Essential Application** processors. The Linux FPGA platform, based on the Xilinx VCU118, provides a fast, hassle-free way to experience a complete Linux environment.

It takes just three simple steps to get started:

1. Download and flash the Xilinx VCU118 FPGA with the supplied bitstream for your chosen SiFive processor
2. Download and flash the SiFive Linux BSP onto an SD card
3. Boot Linux

Broad Application Coverage

The P550 enables greater innovation and flexibility in the broadest range of high-performance applications for endpoints, edge, and cloud:

Endpoints

- DTV / Smart Home
- AR, VR, MR
- Set Top Box
- Game Consoles
- Digital Imaging

Enterprise

- 5G Wireless
- Core/Edge Routers
- Base Stations
- Access Points

Edge/Autonomous

- AV / ADAS
- IVI / Cluster
- HUD / Telematics
- Military / Aerospace
- Robots / Drones