PN7642

Single chip solution with high performance NFC reader, customizable MCU and security toolbox

Rev. 3.0 — 14 March 2023 Product data sheet

1 General description

This document describes the functionality and electrical specification of the NFC open controller PN7642.

Additional documents supporting a design-in of the PN7642 are available from NXP, this additional design-in information is not part of this document.

The PN7642 is a Cortex M33 microcontroller with integrated NFC interface and security subsystem.

In this document, the term „MIFARE card“ refers to a contactless card using an IC out of the MIFARE Classic, MIFARE Plus, MIFARE Ultralight or MIFARE DESFire product family.

2 Features and benefits

Arm Cortex-M33 microcontroller

- Running at a frequency of up to 90 MHz
- Arm Cortex M33 built-in nested vectored interrupt controller (NVIC)
- Non-maskable interrupt (NMI) input with a selection of sources
- Serial wire debug with breakpoints and watch points. Includes serial wire output for enhanced debug capabilities.
- System tick timer
- up to 21 GPIOs (6 dedicated GPIOs)
- On-chip memory
  - 256 kB flash memory (188 kB available to the user)
  - 32 kB RAM (20 kB available to the user)
- Security
  - Symmetric crypto accelerator
  - Asymmetric crypto accelerator
  - Secure key storage for symmetric keys
    - Refer to Section 9.12.3 for information about how to replace the factory default keys with custom keys
  - Secure boot support
  - Key transfer unit to transfer symmetric keys between key store and crypto engine, without involvement of the CPU
- Serial interfaces
  - I^2C controller[1]
  - SPI controller
  - USB 2.0 Full-speed device controller
  - I^2C target up to 3.4 Mbit/s (High-speed mode)
  - I^3C target
  - SPI target up to 15 MBit/s
  - UART
  - CT auxiliary interface
  - Host interface supply voltage of 1.8 V and 3.3 V is supported for maximum interoperability with existing micro-controllers

NFC functionality

- The following 13.56 MHz reader/writer modes (PCD) are supported
  - ISO14443-3/4 A/B
  - ISO15693 / ISO18000-3 mode 1
  - FeliCa
  - ISO18000-3 mode 3
- The following 13.56 MHz card modes (PICC) are supported
  - ISO14443-3/4A
- Supports ECP 2.0 (ref. [1])
- All relevant 13.56 MHz reader/writer modes (PCD) are supported
- High data rates for communication with NTAG 5 (based on ISO/IEC15693) up to 212 kBit/s
- Fast hardware and firmware-based EMD error handling without host controller interaction

1 Updated the terms "master/slave" to "controller/target" to align with the recommendation of the NXP - I^2C and JEDEC SPI standards organizations.

Transmitter

- 2.0 W transmitter output power
- Dynamic power control (DPC 2.0) works with true current measurement
- DPC 2.0 regulates the transmitter current with lowest latency and without any host controller interaction
- Fine granularity of DPC 2.0 transmitter output voltage settings, step-width is 100 mV
- Adaptive waveform control (AWC) reduces the effort to achieve the standard compliance for various data rates and protocols

Receiver

- Innovative receiver signal processing implemented for advanced robustness against external noise sources (e.g. TFT display and external DC-DC noise)
- True automatic gain control (AGC) and internal voltage divider adjust signal levels automatically for optimized signal to noise ratio
- 10-bit ADC - together with the innovative signal processing delivers high receiver sensitivity and wide communication range
- Receiver signal strength indicator (RSSI) allows configuring receiver settings automatically dependent on the actual antenna signal reception condition.

Power-saving support

- Comprehensive power-saving configurations allow minimizing the power consumption including standby, OFF mode and hard power down (HPD) mode.
- Software-based low-power card detection (LPCD) for highest detection sensitivity
- Hardware-based ultra low-power card detection (ULPCD) for lowest current consumption

Special features

- Integrated low noise DC-DC allows supplying the transmitter with up to 6.0 V while the system supply is 3.3 V (e.g. battery supply).
- Internal temperature sensor protects against overheating, warning levels are configurable, emergency shutdown at temperature level which might impact product lifetime.
- Overcurrent protection (configurable) protects the chip in case of short on the transmitter outputs
- Two DAC outputs allow the connection of variable capacitors for automatic antenna tuning
- Firmware upgrade is possible "in the field"
- Operating ambient temperature range -40 °C to +85 °C with full RF output power
- Operating ambient temperature from +85 °C to +105 °C is possible with reduced RF output power

2.1 RF functionality

- As a highly integrated high performance full NFC Forum-compliant frontend IC for contactless communication at 13.56 MHz, this NFC frontend IC utilizes an outstanding modulation and demodulation concept completely integrated for relevant 13.56 MHz based contactless communication methods and protocols.
  PN7642 supports communication with all products of the MIFARE product-based card family including MIFARE Ultralight, MIFARE Classic 1K/4K, MIFARE DESFire EV1/EV2 and MIFARE Plus cards CRYPTO implemented in hardware for R/W of all NXP MIFARE product-based cards (includes intellectual-property licensing rights for NXP ISO/IEC 14443-A, Innovatron ISO/IEC 14443-B, and NXP MIFARE products).
  The PN7642 frontend IC supports the following RF operating modes:

2.1.1 ISO/IEC14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

2.1.2 ISO/IEC14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kBit/s

2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kBit/s and 424 kBit/s (without crypto)

2.1.4 Tag type reading

- Supports reading of all NFC tag types (type 1, type 2, type 3, type 4A and type 4B, type 5)

2.1.5 MIFARE card reading

- Reader/writer communication mode for the MIFARE card family including MIFARE Classic

2.1.6 ISO/IEC 15693

- Reader/writer mode supporting ISO/IEC 15693 (ICODE)
- Proprietary data rates based on ISO/IEC15693 with 106 kbit and 212 kbit/s (for NXP NTAG 5 communication)

2.1.7 ISO/IEC 18000-3 Mode 3

- Reader/writer mode supporting ISO/IEC 18000-3 Mode 3

2.1.8 Card emulation

- ISO/IEC4443-A card mode from 106 Kbit/s up to 848 Kbit/s (PICC) with active load modulation for increased communication range.

2.2 Product comparison

The PN76 family consists of two derivatives. Find a comparison in the following table.

Table 1. Comparison of the PN76 family members

	PN7640EV	PN7642EV
Contactless interface features PCD (reader/writer)	• ISO14443-3/4 A/B • ISO15693 / ISO18000-3 mode 1 • MIFARE	• ISO14443-3/4 A/B • ISO15693 / ISO18000-3 mode 1 • FeliCa • ISO18000-3 mode 3 • MIFARE
Contactless interface features PICC (card mode)	• ISO14443-4A	• ISO14443-4A
Available flash memory	120 kB	180 kB
General-purpose I/O	6	Up to 21
Host interfaces	SPI, I^2C, UART, USB device	SPI, I^2C (with SMBUS support), I^2C, HSUART, USB device
Controller interfaces	-	SPI, I^2C (with SMBUS support), ISO7816 UART
Firmware update in the field	I^2C and SPI	USB, SPI, I^2C, I^3C, UART, NFC, from user app

Table 1. Comparison of the PN76 family members*...continued*

	PN7640EV	PN7642EV
High data rates for NTAG 5 support	-	Yes, up to 212 kbit/s
PWM / ADC interface	-	3 PWM outputs / 1 ADC input
Certification	-	SESIP L2, NFC Forum (reader device and card emulation)
Compliance	-	USB, CT ISO
Cryptographic features	• Hardware Key store for symmetric AES keys (128 or 256 bit) • Key store software extension for symmetric keys • mbedTLS library	• Hardware Key store for symmetric AES keys (128 bit or 256 bit) • Key store software extension for symmetric and asymmetric keys • mbedTLS library
Cryptographic features symmetric	• Fast AES-128 or AES-256 en/decryption • Support for chaining modes: CBC, CTR • SHA256 coprocessor • AES en/decryption via DMA • SHA256 hashing via DMA • Random number generator (RNG) • Countermeasures against side channel information leakage • Supported algorithms – AES-CCM – AES-CBC – AES-ECB – AES-CTR – AES-GCM (in software) – AES-GMAC – SHA-256	• Fast AES-128 or AES-256 en/decryption • Support for chaining modes: CBC, CTR • SHA256 coprocessor • AES en/decryption via DMA • SHA256 hashing via DMA • Random number generator (RNG) • Countermeasures against side channel information leakage • Supported algorithms – AES-CCM – AES-CBC – AES-ECB – AES-CTR – AES-GCM (in software) – AES-GMAC – AES-EAX – SHA-256 – SHA-384 / 512 (in software) – 3DES
Cryptographic features asymmetric	• HKDF • HMAC • Elliptic Curve algorithms – ECKA – ECC key generation – ECDSA signing and verification – EdDSA signature verification for Edward curve – Curves – Brainpool P256r1 – Brainpool P384r1 – SECP256 – SECP384 – Ed25519 signature verification – Additional curves on Weierstrass and Prime are	• HKDF • HMAC • RSA • Elliptic Curve algorithms – ECKA – ECC key generation – ECDSA signing and verification – EdDSA signing and verification for Edward curve – Curves – Brainpool P256r1 – Brainpool P384r1 – SECP256 – SECP384 – Ed25519 (signature generation and verification)

Table 1. Comparison of the PN76 family members*...continued*

	PN7640EV	PN7642EV
	supported by feeding the specific domain parameters	– Additional curves on Weierstrass and Prime are supported by feeding the specific domain parameters

3 Applications

- Physical access
- eGov
- Closed loop payment
- Secure authentication
- Enhanced Contactless Polling (ECP)

4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$VDD_{(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT ≥ VDDIO	2.4	-	5.5	V
$VDD_{(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	1.8 V supply	1.62	-	1.98	V
		3.3 V supply	2.4	-	3.6	V
$VDD_{(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	supply with VDDPA from internal VDDPALDO with DC-DC	1.5	-	5.7	V
I_{pd}	power down current	$VDD_{(VDDPA)}$ = $VDD_{(VDDIO)}$ =$VDD_{(VDD)}$ 3.0 V; hard power down state; pin VEN set LOW, T_{amb} = 25 °C, External supply by VDDIO	-	40	105	µA
I_{stb}	standby current	T_{amb} = 25 °C	-	45	110	µA
I_{ULPCD}	average ultra-low-power card detection current	T_{amb} = 25 °C, VDD(VDDPA) = VDD(VDDIO) =VDD(VDD) 3.0 V, 330 ms Polling interval, 50 R antenna matching	-	22	-	µA
$IDD_{(VDDPA)}$	supply current on pin VDDPA	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
		supplied without DC-DC and TXLDO active	-	-	400	mA
$P_{(PA)}$	Transmitter output power	supplied via VUP_TX (TX_LDO active)	-	-	2.0	W
		supplied without DC-DC and TXLDO active	-	-	2.3	W
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB,	-40	-	+85	°C
T_{stg}	storage temperature	no supply voltage applied	-55	-	+150	°C
T_{j_max}	maximum junction temperature	-	-	-	+125	°C

5 Ordering information

Table 3. Ordering information

Type number	Package			Packing	12NC
	Name	Description	Version		
PN7642EV/C100	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm. MSL = 3.	SOT1307-2	Tape and Reel packing. Minimum order quantity = 4000 pcs	9354 378 87518
PN7642EV/C100	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm. MSL = 3.	SOT1307-2	Tray packing. Minimum order quantity = 2450 pcs	9354 378 87557

Table 4. Factory default transport key

Type number	12NC	Factory default transport key
PN7642EV/C100	9354 378 87518 9354 378 87557	**128-bit:** 4B3CEAED37CB6C03DB322BB483888474 **256-bit:** 7B986646E11B4DC55BBF1D35F2B00CAC BA0AE0E822D70E89EAB95825BA843B82

6 Firmware versions

Firmware versions covered by this data sheet:

PN7642EV/C100

Initialized with firmware 01.00

7 Block diagram

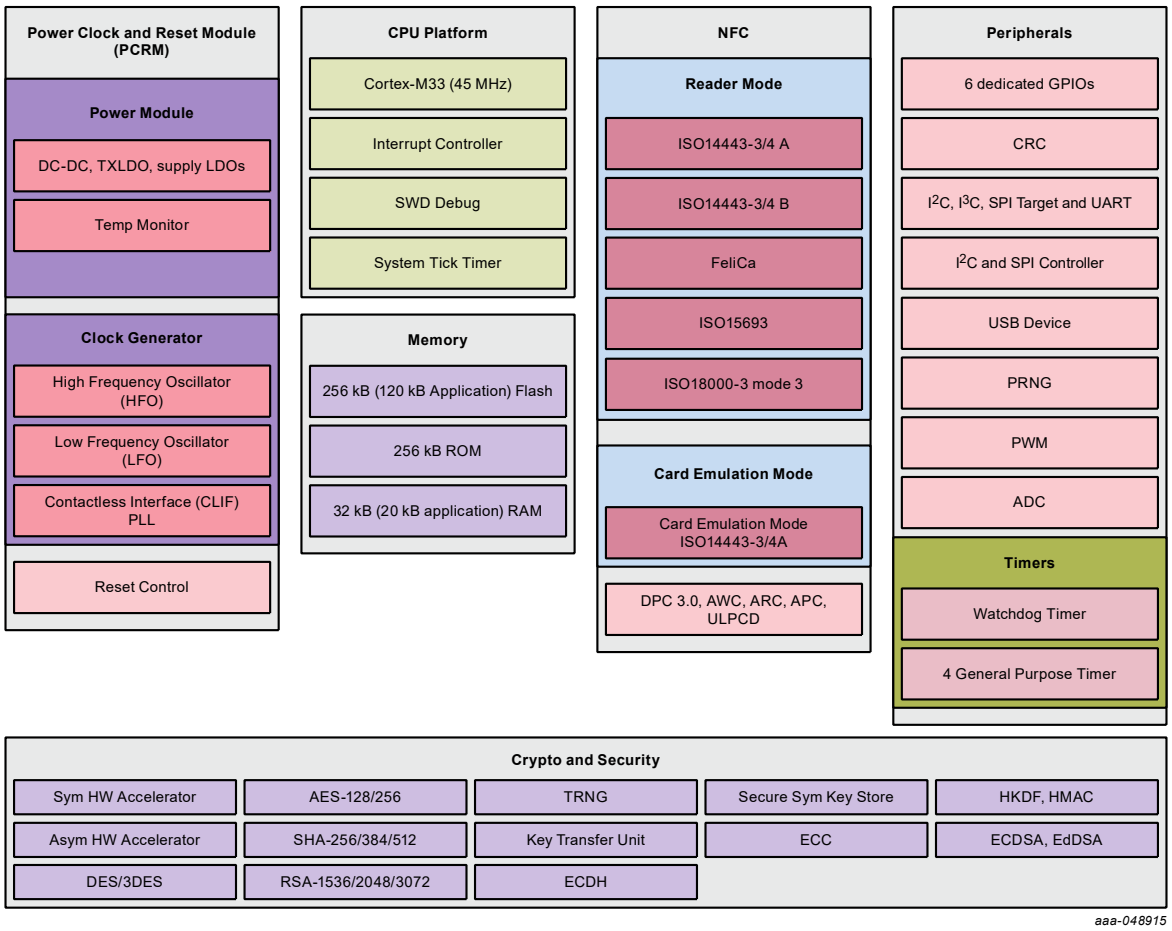


Figure 1. Block diagram PN7642

8 Pinning information

8.1 Pin description VFBGA64

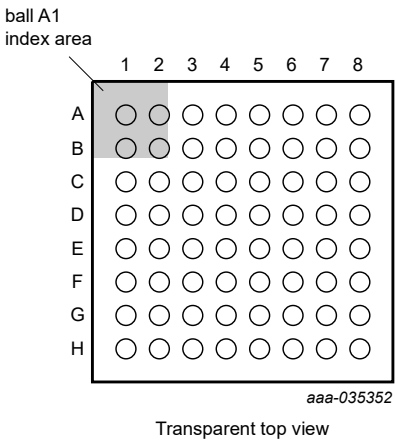


Figure 2. Pin configuration for VFBGA64

Table 5. Pin description VFBGA64

Pin Number	Symbol	Type	Description PN5190	Description PN7642
Host Interface				
E6	ATX_A	Output	SPI target[1] data output	UART RX / I^3C SDA / SPI MISO / I^2C SDA
E5	ATX_B	Input	SPI clock input	UART CTS / I^3C SCL / SPI SCK / I^2C SCL
D6	ATX_C	Input	SPI target select input	UART RTS / I^3C Adr Bit 0 / SPI NSS / I^2C Adr Bit 0 / USB D+
D5	ATX_D	Input	SPI target data input	UART TX / I^3C Adr Bit 1 / SPI MOSI / I^2C Adr Bit 1 / USB D-
B7	IRQ	Output	Host communication/ event interrupt signal	Host communication / event interrupt signal
F8	XTAL1	Input	Crystal / system clock input	Crystal / system clock input
G8	XTAL2	Output	Clock output (amplifier-inverted signal output) for crystal	Clock output (amplifier-inverted signal output) for crystal
B3	VEN	Input	Hardware reset, low active (independent from V_{VDDIO}) Avoid a floating or unexpected toggling of the pin.	Hardware reset, low active (independent from V_{VDDIO}) Avoid a floating or unexpected toggling of the pin.
Supply pins				
H2	VSS_PA	Supply GND	Transmitter ground	Transmitter ground
G3	VSS_PLL	Supply GND	PLL ground (low noise)	PLL ground (low noise)

Table 5. Pin description VFBGA64*...continued*

Pin Number	Symbol	Type	Description PN5190	Description PN7642
A2	VSS_PWR	Supply GND	DC-DC boost ground	DC-DC boost ground
D3	VSS_REF	Supply GND	PMU ground	PMU ground
B2, E3	VSS_SUB	Supply GND	Substrate ground	Substrate ground
C3	VSS_PMU	Supply GND	PMU ground	PMU ground
F4	VSS_DIG	Supply GND	Digital ground	Digital ground
F3	VSS_NFC	Supply GND	NFC ground	NFC ground
E1	VBAT	Supply	System supply, used to supply the analog and digital blocks, memory and internal voltage references	System supply, used to supply the analog and digital blocks, memory and internal voltage references
A8	VDDIO	Supply	IO pads power supply	IO pads power supply
G1	VDDPA	Supply	Transmitter supply	Transmitter supply
F1	VUP_TX	Supply	Input supply voltage for transmitter LDO	Input supply voltage for transmitter LDO
B1	VDD BOOST	Supply	DC-DC boost supply	DC-DC boost supply
A1	BOOST_ LX	Output	Boost inductance loopback, to be connected to boost inductor	Boost inductance loopback, to be connected to boost inductor
A3	VBATPWR	Supply	To be connected to boost inductor and transmitter power supply	To be connected to boost inductor and transmitter power supply
Outputs for stabilizing cap				
A4	VDDNV	Output	Non-volatile memory power supply, to be connected to ground via 220 nF blocking cap	Non-volatile memory power supply, to be connected to ground via 220 nF blocking cap
D2	VREF	Output	High quiescent reference voltage, to be connected to ground via 100 nF blocking cap	High quiescent reference voltage, to be connected to ground via 100 nF blocking cap
C1	VDDC	Output	Power supply for Digital Core, to be connected to ground via 220 nF blocking cap	Power supply for Digital Core, to be connected to ground via 220 nF blocking cap
G2	TXVCM	Output	Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap	Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap
F2	TXVCASC	Output	TX decoupling cap, to be connected to VDDPA	TX decoupling cap, to be connected to VDDPA
H6	VMID	Output	Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap	Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap
RF Debug signals				

Table 5. Pin description VFBGA64*...continued*

Pin Number	Symbol	Type	Description PN5190	Description PN7642
G7	AUX_1	Output	Test bus 1	Test bus 1
F7	AUX_2	Output	Test bus 2	Test bus 2
H8	AUX_3 / VTUNE0	Output	Test bus 3 / VTUNE0 (digital-to-analog output 0)	Test bus 3
Antenna connections				
H5	RXP	Input	Receiver input "Positive"	Receiver input "Positive"
H4	RXN	Input	Receiver input "Negative"	Receiver input "Negative"
H1	TX1	Output	Antenna driver output 1	Antenna driver output 1
H3	TX2	Output	Antenna driver output 2	Antenna driver output 2
Analog/Digital inputs and outputs				
H7	VTUNE1	Output	Digital-to-analog output 1	Do not connect
E8	GPIO0	Input/ Output	General Purpose Output 0	General Purpose I/O 0 / PWM 0
D8	GPIO1	Input/ Output	General Purpose Output 1	General Purpose I/O 1 / PWM 1
E7	GPIO2	Input/ Output	General Purpose Output 2	General Purpose I/O 2 / PWM 2
D7	GPIO3	Input/ Output	General Purpose Input/Output 3 If ULPCD is used, GPIO3 cannot be used for any other purpose than aborting the ULPCD.	General Purpose I/O 3 / PWM 3 If ULPCD is used, GPIO3 cannot be used for any other purpose than aborting the ULPCD.
Security feature				
B4	PRD1	Input/ Output	Package removal detection, internally connected to PRD2	Package removal detection, internally connected to PRD2
G4	PRD2	Input/ Output	Package removal detection, internally connected to PRD1	Package removal detection, internally connected to PRD1
Pins connected on PN76 family only				
A5	PVDD_ OUT	Output	Do not connect	PVDD LDO output
A6	I2CM_ SDA	Input/ Output	Do not connect	I^2C controller SDA
A7	DWL_REQ	Input	Do not connect	Download request (optional)
B5	GPIO5	Input/ Output	Do not connect	General Purpose I/O 5
B6	I2CM_SCL	Input	Do not connect	I^2C controller SCL
B8	SWDIO	Input/ Output	Do not connect	Single Wire Debug Interface Data
C2	TEST	Input/ Output	Internal test pin. Do not connect	Internal test pin. Do not connect.

Table 5. Pin description VFBGA64*...continued*

Pin Number	Symbol	Type	Description PN5190	Description PN7642
C4	ISO_INT_ AUX	Input/ Output	Do not connect	Auxiliary Card Interrupt
C5	GPIO4	Input/ Output	Do not connect	General Purpose I/O 5
C6	HOST_IF_ SEL1	Input	Do not connect	Host interface select 1
C7	HOST_IF_ SEL0	Input	Do not connect	Host interface select 0
C8	SWD_CLK	Input	Do not connect	Single Wire Debug Interface Clock
D1	USB_ VBUS	Input	Do not connect	Used for USB VBUS detection
D4	ISO_IO_ AUX	Input/ Output	Do not connect	Auxiliary Card I/O
E2	AD1	Input	Do not connect	Analog/Digital converter Input 1
E4	ISO_CLK_ AUX	Input	Do not connect	Auxiliary Card Clock
F5	SPIM_ MOSI	Input	Do not connect	SPI controller MOSI
F6	SPIM_ MISO	Output	Do not connect	SPI controller MISO
G5	SPIM_ SCLK	Input	Do not connect	SPI controller clock
G6	SPIM_ NSS	Input	Do not connect	SPI controller NSS

[1] Updated the terms "master/slave" to "controller/target" to align with the recommendation of the NXP - I^2C and JEDEC SPI standards organization

For good RF performance, all blocking capacitors shall be placed on the same side of the PCB, traces from pin to capacitor shall be as short as possible.

All Supply GND connections shall be connected by low-ohmic connections on the PCB.

9 Functional description

9.1 Functional overview

The PN7642 is a Cortex M33 microcontroller that integrates an NFC frontend with high transmitter output power. It implements the RF functionality like an antenna driving and receiver circuit and all the low-level functionality to realize an NFC Forum-compliant reader.

The PN7642 contains a secure cryptographic subsystem that consists of secure DMA, one accelerator for symmetric cryptography, one accelerator for asymmetric cryptography, one key obfuscation and transfer unit, one True Random Number Generator and a secure symmetric key store.

Arm Cortex M33 processor

The Arm Cortex-M33 is based on the ARMv8-M architecture that offers systems enhancements, such as low power consumption, enhanced debug features, and a high level of support block integration. The Arm Cortex-M33 CPU employs a 7-stage instruction pipe and includes an internal prefetch unit that supports speculative branching. A hardware floating-point processor is integrated into the core. On the PN7642, the Cortex-M33 is augmented with one hardware co-processors providing accelerated support for cryptography.

Nested vectored interrupt controller (NVIC) for Cortex-M33

The NVIC is an integral part of the Cortex-M33. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

NVIC features

- Controls system exceptions and peripheral interrupts.
- 48 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Configurable levels of interrupt priority from 8 to 256. This is configured at implementation to support 8 priority levels.
- Non-maskable Interrupt (NMI).
- Software interrupt generation.

Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

System tick timer (SysTick)

The Arm Cortex-M33 core includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

On-chip static RAM

The PN7642 supports up to 32 kB SRAM with separate bus controller access for higher throughput and individual power control for low-power operation. 20 kB RAM are available to the user.

On-chip flash

The PN7642 supports up to 256 kB of on-chip flash memory, where 188 kB is accessible by the user. 68 kB are reserved by the system.

Clock supply

The PN7642 uses an external 27.12 MHz crystal as clock source for generating the RF field and its internal digital logic. Alternatively, an internal PLL allows using an accurate external clock source of either 24 MHz, 32 MHz, and 48 MHz (configured in EEPROM register CLK_INPUT_FREQ, 0012h)). This allows saving the 27.12 MHz crystal in systems which implement one of the mentioned clock frequencies.

Integrated DC-DC

The integrated DC-DC allows a single supply voltage while delivering maximum RF output power. Dependent on the application target either a direct transmitter supply or a transmitter supply by the integrated DC-DC can be chosen. The usage of the integrated DC-DC is the preferred choice for stable RF performance, even in case of a de-charged battery. Optimized usage of a battery charge can be achieved by directly connecting the transmitters to the supply. The DC-DC is controlled by the Dynamic Power Control 2.0 to keep the power dissipation of the chip minimized in antenna loading cases which require a reduction of the RF output power.

The DC-DC is a step-up converter and is able to deliver an output voltage from approx. 2.8 V up to 6.0 V. The targeted output voltage can be configured by software.

The DC-DC clock is synchronized with the clock of the receiver - this avoids the typical performance reduction by DC-DC noise which can be seen in systems using external DC-DCs.

Transmitter LDO (VDDPALDO)

The transmitter output drivers are supplied by a transmitter LDO which reduces external noise and is used for the DPC functionality to lower the supply voltage of the transmitters. The high granularity of 100 mV for setting the VDDPALDO output voltage together with a sophisticated control loop and true current measurement ensures that a DPC regulation is not accidentally treated as received data.

Ultra Low-power card detection

The ultra low-power card detection (ULPCD) allows saving battery charge during polling for NFC counterparts like cards and mobile phones. In general, the ultra low-power card detection provides a functionality, which allows to power down the NFC controller for a certain amount of time to safe energy. After some time, the NFC controller becomes active again to poll for cards. If no card is detected, the device can go back to the power down state.

Dynamic power control 2.0

The next generation dynamic power control (DPC2.0) with true transmitter current measurement works autonomously without host interaction. Avoiding additional host controller processing load is important for time critical applications like payment. A fast control response time of less than 1 ms allows using optimized antenna matching.

Adaptive waveshape control

The adaptive waveshape control (AWC) helps to keep the wave shapes within specification limits, even in case of antenna detuning. This simplifies the time-consuming antenna-matching procedure and does not require any matching compromises to be taken.

Receiver signal level control

The receiver signal chain consists of an automatic controller RF input attenuator and a true baseband amplifier (BBA). This feature delivers an outstanding communication range with tags, labels, cards, and mobile phones.

RF Debugging

Comprehensive and innovative debug features are implemented to support the NFC reader development even for difficult and non-standard compliant cards and mobile phones. An Integrated Chip scope allows performing a non-intrusive debugging of receiver signals without the need of connecting additional wires to the chip. Capturing of chip-internal signals is done by configuring flexible trigger conditions, sampled internal data is stored in RAM memory, transferred by SPI to a host microcontroller and visualized on a PC by the NFC Cockpit development tool. A virtual COM interface (VCOM) is supported by the NFC cockpit tool, which allows to use the NFC cockpit together with any host microcontroller. Analog debug signals (AUX1, AUX2) are available as well and allow the connection of an Oscilloscope for analog and digital signal debugging.

The receiver signal processing is optimized to cope with noisy environments. This is beneficial, especially in case a TFT display or DC-DCs are part of the NFC system.

Automatic EMD error handling

An automatic EMD handling performed without host interaction relaxes the timing requirements on the Host Controller. Automatic EMD error handling according to ISO/IEC14443 and EMVCo 3.0 is supported. In addition, the EMD error handling is widely configurable, which allows adaptions in case of future possible specification changes.

Firmware update

The PN7642 supports a secure update of the implemented firmware. The secure firmware download mode is using a dedicated command set. The firmware download does not require any additional hardware pin to be handled, instead the download mode is activated by a command, followed by a hardware reset. After booting from reset, the PN7642 will be in download mode.

For the secure firmware update, the following interfaces can be used: I^2C, I^3C, SPI, and UART.

Register configuration

Internal registers of the PN7642 store volatile configuration data. The internal registers are reset to configurable initial values in case of power on, hardware-reset and standby.

The configuration for dedicated RF protocols and antenna-dependent configuration is defined in non-volatile memory. This configuration is typically done only once during production, and is performed by a command issued from the PN7642 user application.

EEPROM configuration

Non-volatile EEPROM memory of the PN7642 is used to store configuration data that needs to be preserved in case the PN7642 is not connected to any supply voltage. The configuration for dedicated RF protocols and antenna-dependent configuration is defined in this non-volatile memory and copied to volatile registers by the PN7642 user application. In addition, other configuration data which needs to be preserved during power supply disconnect is stored in this EEPROM memory as well. Examples for this are configurations for DPC and ULPCD configurations.

RF configuration

The PN7642 allows a fast RF protocol selection based on the command Load_RF_configuraton and pre-defined user configuration data in non-volatile memory (EEPROM).

On the one hand, the configuration of modulation-related parameters can be done (e.f. selection of ISO/IEC14443-A), on the other hand antenna-specific parameters can be configured

Cryptographic subsystem

The PN7642 includes a cryptographic subsystem that accelerates symmetric and asymmetric operations. Furthermore it contains a symmetric key store that helps to securely store customer keys. With the help of the key transfer unit, keys can be loaded directly into the crypto subsystem without passing the CPU, which significantly enhances the confidentiality of the keys.

9.2 Endianness

The endianness describes the order of bytes or bits within a binary representation of a value in the memory, which can be a register or EEPROM.

"Array size" defines the number of elements of "type size". Type size can be uint8 (8 bit), uint16 (16 bit) or uint32 (32 bit).

The location of byte sized data (8 bit) with an array size of 2 is as follows:

Value hex: 0x1234

address x: 12

address x+1: 34

The location of word sized data (16 bit) is as follows:

Value hex: 0x1234

address x: 34

address x+1: 12

The location of word sized data (16 bit) in an array size of 2 is as follows:

The placement of the array is large endian, the placement of nibbles of the variable is small endian.

Value hex: 0xAABBCCDD

address x: BB

address x+1: AA

address x+2: DD

address x+3: CC

The location of double word sized data (32 bit) is as follows:

Value hex: 0xAABBCCDD

address x: DD

address x+1: CC

address x+2: BB

address x+3: AA

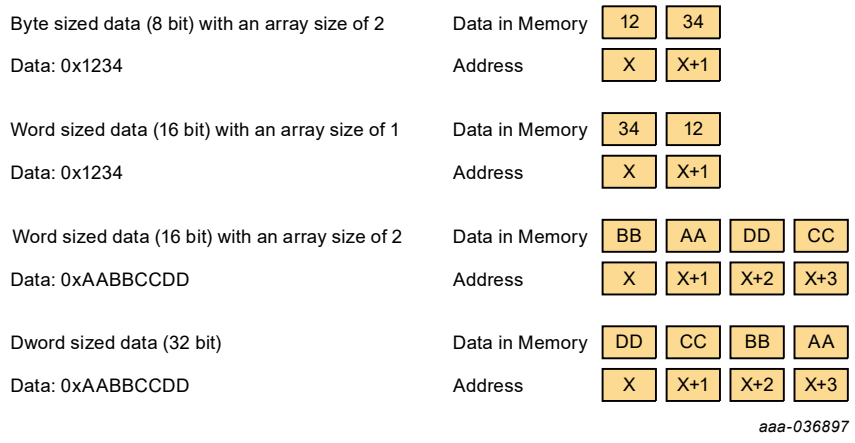


Figure 3. Endianness examples

The PN7642 is a little-endian system. This means that the byte at the lower address is read first.

9.3 CPU Sub System

9.3.1 Overview

The PN7642 device is controlled using a CPU (Arm) subsystem described in the following section. The CPU Sub-System is controlled by an Arm Cortex M33 Processor that runs the application firmware. It incorporates two DMA controllers of type PL080 which aim to transfer data between peripherals and the system RAM but also between memories only. These DMA controllers are connected to an AHB Lite multi controller matrix and an AHB-to-APB bridge that gives access to the various target peripheral IPs (e.g. HostIF)

The CPU Sub-System includes two external Implementation Defined Attribution Units (IDAUs), one for each of its two AHB controller ports, and a special firewall IP for memory segmentation and access right management. Together with Arm's Trust Zone concept, this is the core concept to enable an open platform architecture by configuring memory apertures to protect/restrict specific memory regions and IP accesses from user application code or debug accesses.

9.3.2 Features

The PN7642 CPU subsystem provides the following set of features:

- Arm Cortex M33 Processor with Security Add-ons (Trust Zone)
  Note: The Trust Zone is not available to the user. It is used for internal purposes.
- Single Cycle Multiplier, Vector Table Offset Register (allowing relocation of Vector Table), SysTick, NVIC with 48 user interrupts, SWD DAP, and debug options
- Code Patch Module with 48 entries
- AHB-Lite multilayer (6 AHB Controllers, 11 AHB Targets)
- AHB to APB bridge (19 APB Targets)
- SRAM/ROM controllers and FLASH controller
- Standard Arm CoreSight Debug Architecture
  - Single Wire Debug Access Port (SW-DP)
  - Embedded Trace Macro cell (ETM)
  - Cross Trigger Interface (CTI)
  - 4 kB Embedded Trace Buffer (ETB)
- Internal Trace RAM configurable for normal usage if debug is not needed
- Secure and Application accessible high performance DMACs (PL080)
- One IDAU per CPU AHB controller port, and firewall IP monitoring any AHB-Lite Interconnect for CPU mode aware access control to AHB targets
- AHB split, retry and locked transfers are not supported

9.3.3 Block diagram

The block diagram is showing the high-level CPU subsystem integration and its surrounding IPs.

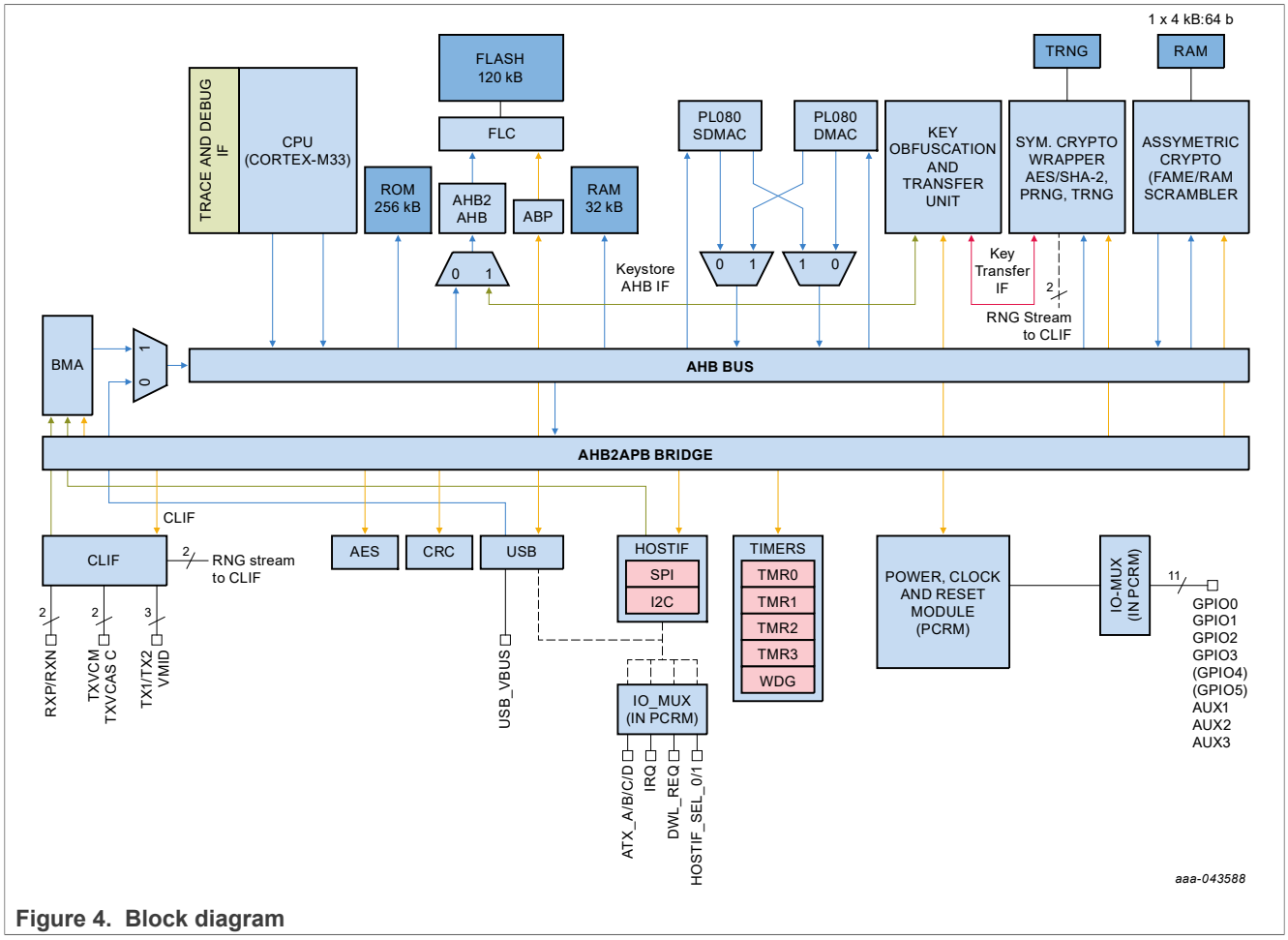


Figure 4. Block diagram

The AHB multilayer brings high-bandwidth connections between the processor and the memories, and access to the APB bridge. It also provides a direct connection from the host interface IP to the SRAM memory. Furthermore, Crypto IPs and USB are AHB controller as well.

The ETB RAM, the main RAM, ROM, and FLASH controllers are part of the CPU subsystem and provide interfaces to the bare memory modules which are typically located outside at the top level of the system.

The DMA subsystem consists of two DMA controllers of type PL080, and both are sharing the two available AHB DMA controller ports at the AHB interconnect. One DMAC is intended to be accessible in Secured CPU mode only, whereas the other is accessible in both Secured and Non-secured CPU Mode. The sharing is done to keep the number of AHB controllers small which is beneficial also for the firewall, since every AHB controller introduces a new port to be monitored and an AHB blocker in this IP.

Another AHB controller port is the Buffer Management and Arbitration Unit's (BMA) port, which can be considered a special purpose DMA port, whose one side will always be an external communication unit. Its other side will always be the system RAM where the BMA maps its receive/transmit buffers. The PN7642 contains a separate communication option for USB which implements its own AHB controller interface. BMA and USB controller normally are never active in parallel, so sharing the AHB lite controller port is acceptable. However in case of access collisions between BMA and USB, the latter takes precedence because the IP does not implement any deep buffering of its data streams.

Firewall and an individual IDAU per CPU AHB port monitor any AHB activities of any AHB controller, and decide based on the given access rights and CPU mode whether access is granted or will lead to an exception.

The AHB-to-ABP bridge translates the high performance AHB protocol into the more compact APB protocol which is the standard protocol for peripherals in an Arm CPU system. The bridge acts on one side like an AHB target. It dissolves the address space into apertures of 4 kB which are assigned to the peripherals of the PN7642 system. Any accesses to non-assigned apertures cause an exception.

Furthermore, the AHB-to-APB bridge supports power down monitoring for each of its APB targets. If an APB target is powered down or its system clock is gated, respectively, it typically indicates this by a flag that is connected to the bridge. If the CPU tries to access such an IP, the bridge converts this access into an exception (HRESP will be set to “ERROR”). This is important for clock gated IPs in particular because otherwise access will never be terminated and the system would stall.

Note: The PN7642 supports a system clock of 90 MHz but the Flash controller 45 MHz only. In order to benefit from the 90 MHz for the rest of the system, the AHB as well as the APB ports of the FLASH controller are connected to the AHB interconnect and the APB bridge via special clock scalers. They guarantee a division of the FLASH controller’s system clock by two if the high system clock option is active. If 45 MHz are selected as system clock, then the scalers are bypassed.

9.3.4 System tick timer

The system tick timer (SysTick timer) is an integral part of the Arm Cortex-M33 core. It is basically a 24 bit down counter which can be started and configured with an automatic reload value. If the timer is running and its IRQ is enabled, it generates periodic interrupts intended to be used, for example, by an operating system, in particular Real-Time operating Systems (RTOS) or other system management software. The intent is to provide a fixed time interval between interrupts so that the OS can carry out task management — for example, to allow multiple tasks to run at different time slots and to make sure that no single task can lock up the whole system. The SysTick timer is clocked internally by a dedicated system tick timer clock.

9.3.4.1 Features

- 24-bit timer
- Uses dedicated exception vector
- Dedicated system tick timer clock
- Clock source configurable (system clock or SYSTICK clock)

9.3.5 Memories maps

9.3.5.1 General

The PN7642 contains 256 kB on-chip flash programming memory, where parts are reserved for the system. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip bootloader software.

The following section gives an overview on the PN7642 memories.

9.3.5.2 Main memory map

The following table shows, how the Cortex M33 global AHB address space is dissolved into regions, and what AHB controllers and targets can be accessed via what memory window. Accesses to the gaps in between are caught by a “default target” which is connected to every AHB controller port as a terminal unit in order to avoid deadlocks by unauthorized memory access request. The default targets make sure that access is correctly handled and raises a bus fault.

Note: From the user application, only a reduced part of the AHB addresses is accessible. The remaining peripherals can be accessed via the System Services API only.

Table 6. Global AHB Memory map

Address Range	Region	Size	Application
0xE0100000 - 0xFFFFFFFF	System	Reserved	Default target error response
0xE00FF000 - 0xE00FFFFF	External PPB bus	4 kB	Reserved
0xE00FE000 - 0xE00FEFFF		4 kB	Reserved
0xE0046000 - 0xE00FDFFF		Reserved	Default target error response
0xE0046000 - 0xE0046FFF		4 kB	Reserved
0xE0045000 - 0xE0045FFF		4 kB	Reserved
0xE0044000 - 0xE0044FFF		4 kB	Reserved
0xE0043000 - 0xE0043FFF		Reserved	Default target error response
0xE0042000 - 0xE0042FFF		4 kB	Reserved
0xE0041000 - 0xE0041FFF		4 kB	Reserved
0xE0040000 - 0xE0040FFF		4 kB	Reserved
0xE003E000 - 0xE003FFFF	PPB internal	Reserved	Default target error response
0xE002E000 - 0xE002EFFF		4 kB	Reserved
0xE000F000 - 0xE001EFFF		Reserved	Default target error response
0xE000E000 - 0xE000EFFF		4 kB	Reserved
0xE0003000 - 0xE000DFFF		Reserved	Default target error response
0xE0002000 - 0xE0002FFF		4 kB	Reserved
0xE0001000 - 0xE0001FFF		4 kB	Reserved
0xE0000000 - 0xE0000FFF		4 kB	Reserved
0xA0000000 - 0xDFFFFFFF	EXT Device	Reserved	Default target error response
0x60000000 - 0x9FFFFFFF	EXT Ram	Reserved	Default target error response
0x40029000 - 0x5FFFFFFF	Peripheral	Reserved	Default target error response
0x40028000 - 0x40028FFF		4 kB	Reserved
0x40023000 - 0x40027FFF		Reserved	Default target error response
0x40022000 - 0x40022FFF		4 kB	SPI controller
0x40021000 - 0x40021FFF		4 kB	PWM control (utimer)
0x40020000 - 0x40020FFF		4 kB	DMAC Configuration
0x40010000 - 0x4001FFFF		64 kB	Reserved
0x40000000 - 0x4000FFFF		64 kB	Application accessible APB-Peripherals
0x20020000 - 0x3FFFFFFF	SRAM	Reserved	Default target error response
0x2001C000 - 0x2001FFFF		16 kB	Reserved
0x20018000 - 0x2001BFFF		16 kB	Reserved
0x20011000 - 0x20017FFF		Reserved	Default target error response
0x20010000 - 0x20010FFF		4 kB	Reserved
0x20009000 - 0x2000FFFF		Reserved	Default target error response
0x20008000 - 0x20008FFF		4 kB	NFC_RAM_ALV

Table 6. Global AHB Memory map*...continued*

Address Range	Region	Size	Application
0x20000000 - 0x20007FFF		32 kB	NFC_RAM
0x00240000 - 0x1FFFFFFF	Code	Reserved	Default target error response
0x00200000 - 0x0023FFFF		256 kB	NFC_FLASH
0x00040000 - 0x001FFFFF		Reserved	Default target error response
0x00000000 - 0x0003FFFF		256 kB	Reserved

9.3.5.3 Peripheral memory map

PN7642 incorporates a total number of 19 peripherals which area accessible by the CPU via an AHBtoAPB bridge. This bridge reacts like an AHB target toward the CPU and translates AHB accessed into APB accesses toward the addressed peripheral. The bridge is configured for peripheral aperture sizes of 0x1000 bytes (4 kB), and maps all peripherals into the global 64 kB AHB windows. The following subset of the peripherals is accessible from the user area directly.

Table 7. Peripheral memory map

APB ID	APB interface	Start Address	End Address	Size (kB)
15	Reserved	0x4000F000	0x4000FFFF	4
14	Reserved	0x4000E000	0x4000EFFF	4
13	Reserved	0x4000D000	0x4000DFFF	4
12	Reserved	0x4000C000	0x4000CFFF	4
11	LP_UART	0x4000B000	0x4000BFFF	4
10	Reserved	0x4000A000	0x4000AFFF	4
9	BMA_APB	0x40009000	0x40009FFF	4
8	Reserved	0x40008000	0x40008FFF	4
7	Reserved	0x40007000	0x40007FFF	4
6	Reserved	0x40006000	0x40006FFF	4
5	TIMERS_APB	0x40005000	0x40005FFF	4
4	CRC_APB	0x40004000	0x40004FFF	4
3	CT_APB	0x40003000	0x40003FFF	4
2	I2CM_APB	0x40002000	0x40002FFF	4
1	USB_APB	0x40001000	0x40001FFF	4
0	HOSTIF_APB	0x40000000	0x40000FFF	4

9.3.5.4 On-chip flash memory map

The flash memory mapping is described in the following table.

Table 8. Flash memory map

Description	Size	Start - End
NXP firmware	32 kB	0x200000 - 0x207FFF
User application	180 kB	0x208000 - 0x234FFF

Table 8. Flash memory map*...continued*

Description	Size	Start - End
NXP firmware	44 kB	0x235000 - 0x23FFFF

The memory region described as "User application" is the region that is accessible by the developer and from where the user application is being executed. The regions described as "NXP firmware" cannot be accessed from the "User application" region.

9.3.5.5 On-chip RAM memory map

The PN7642 contains a total of 32 kB of RAM memory. The memory mapping is shown in the table below.

Table 9. RAM memory map

Description	Size	Start - End
System reserved	12 kB	0x20000000 - 0x20002FFF
User	20 kB	0x20003000 - 0x20007FFF
Application ALV (Always On) RAM	2.5 kB	0x20008000 - 0x20008A3F

9.3.5.6 On-chip ROM memory

The PN7642 includes 256 kB of on-chip ROM memory. The on-chip ROM contains the bootloader, USB mass storage primary download and parts of the NXP firmware.

9.3.5.7 On-chip flash data memory

The PN7642 includes 9.5 kB of on-chip flash data memory. The flash data memory is accessible via the EEPROM HAL APIs from the user application. It used to store persistent configuration data of the PN7642.

Table 10. EEPROM memory map

Description	Size	Start - End
User flash data memory	9.5 kB	0x0000 - 0x25FF

9.4 NFC Sub System

9.4.1 Initial calibration

The PN7642 requires a calibration before the RF field is switched on for the first time with unloaded condition.

"Unloaded" means: Without any additional metal in proximity of the antenna, except for the NFC reader components itself.

During development of new readers, this calibration shall be done each time the antenna design, antenna matching, or EMC filter is modified.

The calibration sequence is the following:

Write EEPROM CfgNovCal

Write REGISTER TX_NOV_CALIBRATE_AND_STORE

Write EEPROM CfgNovCal

9.4.2 Transmitter overcurrent and temperature protection

The PN7642 implements different mechanisms to protect the chip against damage.

On the one hand, an overcurrent protection exists which shuts down the Transmitter Driver in case of a out of spec current. This can be enabled in EEPROM TXLDO_CONFIG, bit 11: overcurrent enable (0: disable, 1: enable)

The actual measured temperature is available in the register TEMP_SENSOR (005Bh).

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

9.4.3 Dynamic power control (DPC)

The DPC is used for a special antenna tuning, called "symmetric antenna tuning". For an "asymmetric antenna tuning", the DPC is not required.

However, even for "asymmetric antenna tuning" with high output power needs, it might turn out that the RF field is too strong in close proximity of the antenna to be compliant with ISO/IEC14443 requirements. In this case, the DPC can be used as well to reduce the RF output power dependent on the distance of the card from the reader antenna.

The DPC works very well with a tuning called "symmetric tuning". With symmetric tuning, a detuning of the antenna is causing a reduction of the antenna impedance. This low antenna impedance might lead to a current which is too high for the targeted application. The DPC allows to limit the transmitter current even under antenna detuning conditions.

DPC is useful:

- To achieve NFC Forum and ISO/IEC 14443 compliancy (e.g. NFC Forum Power Transfer Maximum, ISO/IEC 14443 Field Emission Maximum)
- To improve interoperability

The Dynamic Power Control (DPC 2.0) allows controlling the transmitter driver voltage in 100 mV steps dependent on the actual transmitter current.

A lookup table is used to configure the transmitter output voltage and by this control the RF output power.

Features of the Dynamic power control (DPC 2.0):

- True current measurement provides maximum information for the regulation loop
- The transmitter current can be limited and additionally reduced according to detected transmitter current condition / antenna detuning condition
- DPC works autonomously without host interaction causing no additional processing load on the host
- Fastest response time of 1 ms for regulation
- Used for adaptive waveshape control (AWC)
- Used for adaptive RX sensitivity control (ARC)

The DPC is able to operate in two modes:

1. Current limiting mode
2. Current limiting + Current reduction mode

The DPC is configured in the EEPROM, this configuration is used after startup. This avoids that the host needs to configure the chip after each reset or power-off.

The following EEPROM registers are most relevant for the DPC configuration:

DPC_Config: Enables/Disables the DPC (enable: 0x39, disable: 0x00)

DPC_TargetCurrent: Unloaded VDDPA target current in mA, the target current +/- Hysteresis is limiting the current for the DPC.

- The DPC_TargetCurrent is the current which can be measured for the selected antenna impedance and transmitter supply voltage in unloaded condition. This is the current the system is designed to operate at.

DPC_Hysteresis: Absolute difference to current target current in mA that triggers a DPC update event.

- The configuration of the hysteresis ensures, that the DPC is not regulating if small changes of the transmitter current occur due to external disturbances. A typical value for the DPC_Hysteresis is e.g. 20 mA.

DPC_Lookup_Table: configures the current reduction

The DPC_LOOKUP_TABLE allows in addition to the limitation of the current, to configure

- an additional current reduction on top of the current limitation, achieved by further lowering the transmitter supply voltage
- a relative change of modulated amplitude level
- and a relative change of falling and raising edge time constant for ASK10% and ASK100% modulations

This lookup table is initialized with 0x00 for devices delivered from the factory. (The customer development board is already initialized with useful data in EEPROM which work well with the antenna of the board).

The 0x00 entry in the DPC_LOOKUP_TABLE means that no additional function then the current limitation takes place for the DPC.

In order to achieve a limitation of the current even in the case of an antenna impedance that is lowered, the Transmitter supply voltage is reduced accordingly.

This transmitter supply voltage reduction is now used as index for the DPC_LOOKUP_TABLE.

For a specific transmitter supply voltage, it is possible to further reduce the current below the value of DPC_TargetCurrent or to configure parameters for waveshaping and modulation. All these entries are relative values, granularity of the entries dependent on the transmitter supply voltage is 0.1 V, resulting in 42 table entries.

The DPC updates the content of the following register dependent on the antenna load / lookup table configuration:

DGRM_RSSI

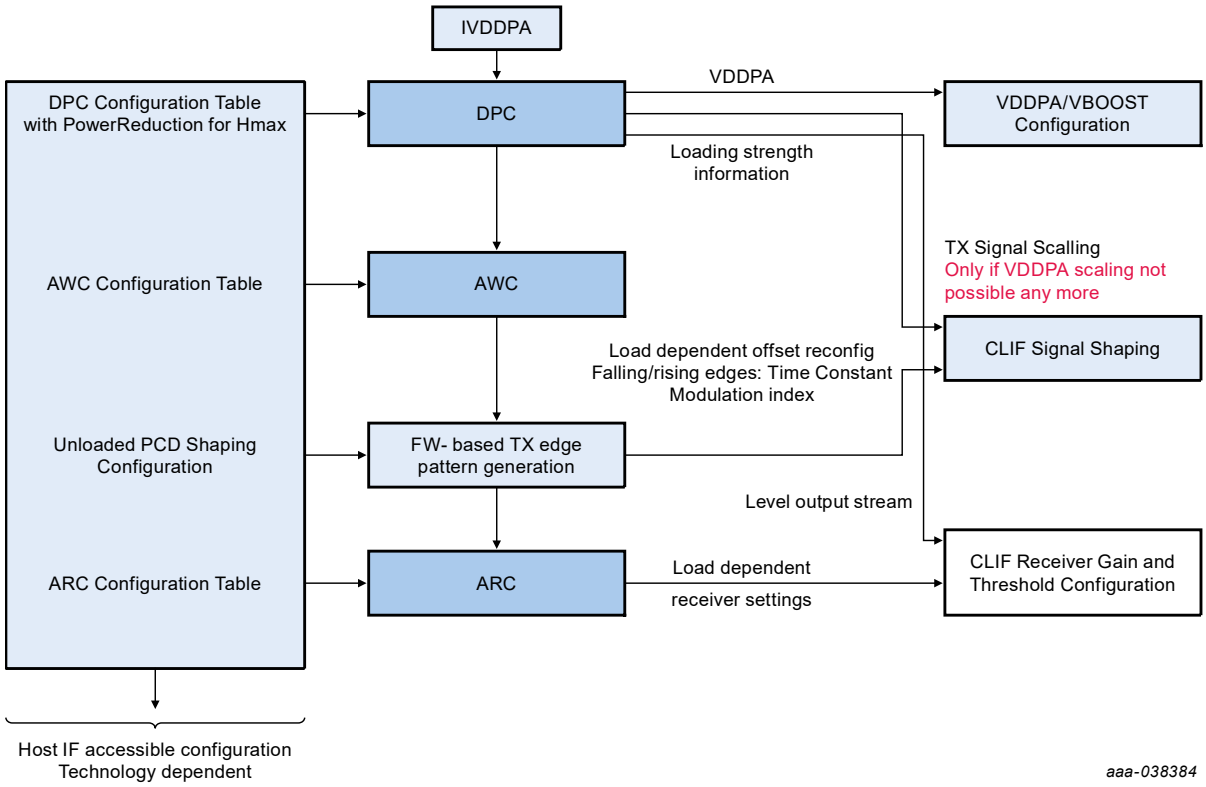


Figure 5. System overview: DPC, AWC and ARC

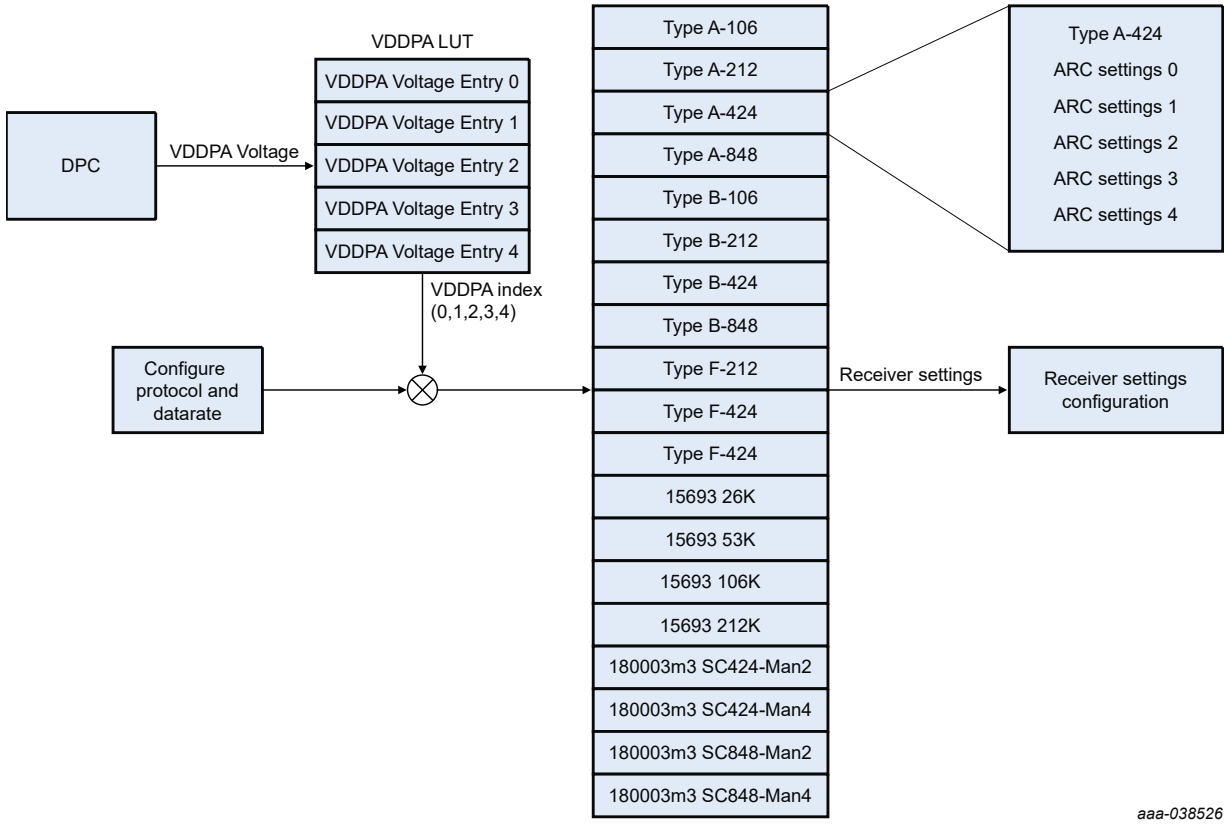


Figure 6. System overview: DPC, AWC and ARC

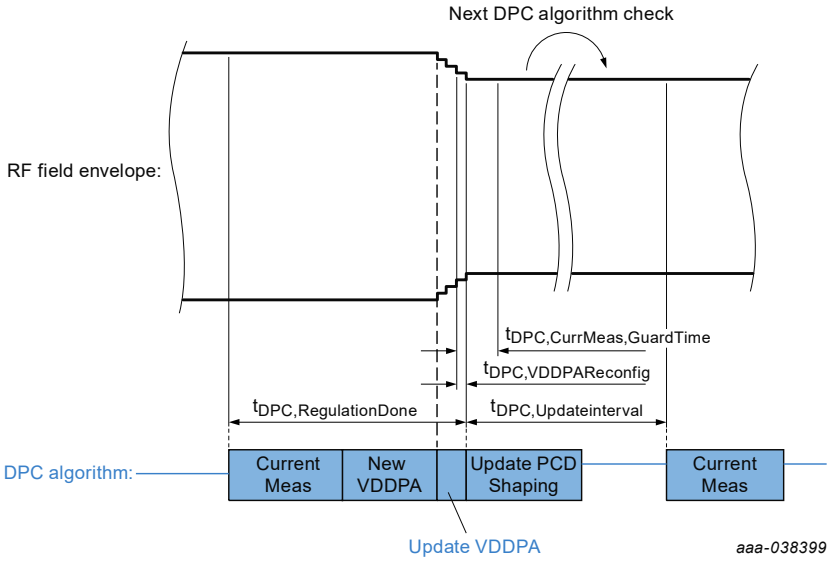


Figure 7. System overview: DPC, AWC and ARC

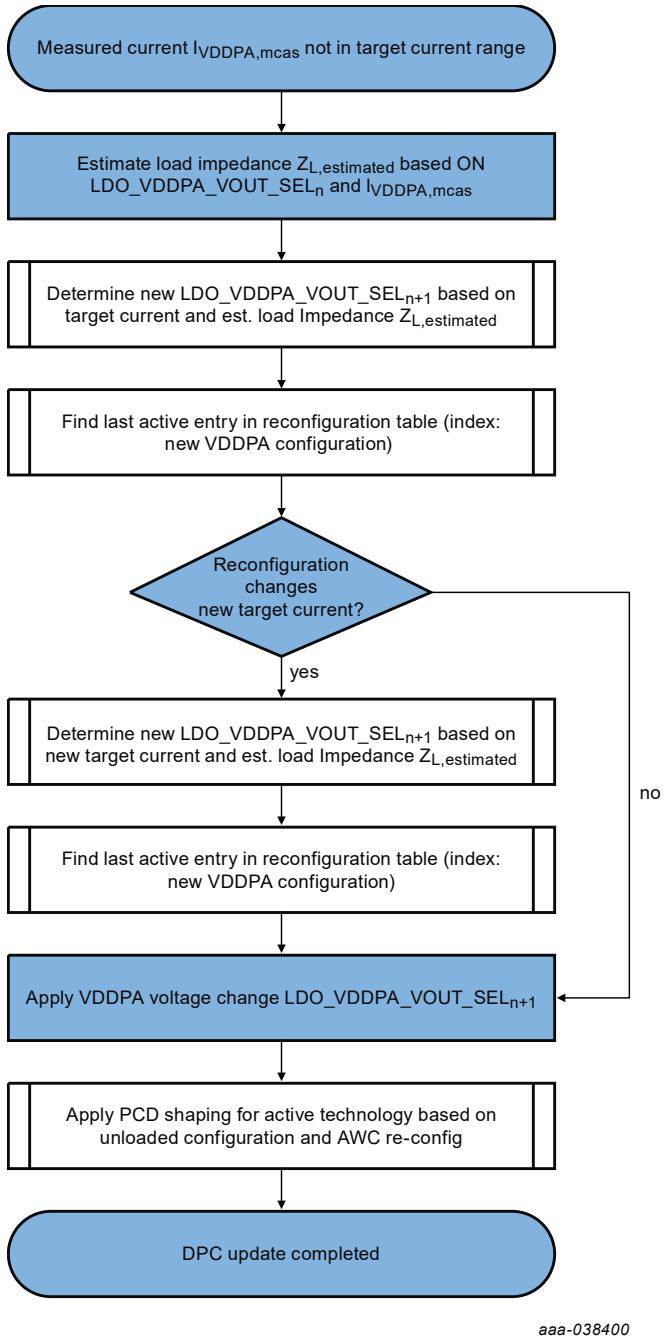


Figure 8. System overview: DPC, AWC and ARC

9.4.3.1 DPC algorithm

The DPC algorithm is controlling the transmitter current. It is using the following states:

1. Current measurement: Performs VDDPA current measurement
2. New VDDPA: Determine new VDDPA configuration based on measured current
   VDDPA New (for target current of Itarget) = VDDPA Voltage / VDDPA current * Itarget
3. Update VDDPA: Perform output power update

4. Update PCD Shaping: Apply AWC configuration updates for active technology
5. Update RX sensitivity parameter only for short duration

Reconfiguration table includes Relative changes of target current and of waveform parameters adaption for all VDDPA voltage configurations. The VDDPA configuration is implicitly defined by the row index. The first row refers to LDO_VDDPA_VOUT_SEL=0 (represents 1V5).

EXAMPLE:

Unloaded configuration After Field ON:

VDDPA max set to 42 (5.7 V) ·Target current set to 280 mA

Technology B106: amp_mod=200

Falling edge time constant=rising edge time constant=3

Table 11. DPC_LOOKUP_TABLE element, defining the configuration for one dedicated VDDPA voltage

Function	Bit	Description
ENTRY 0	31:0	This is the entry for 1.5 V.
Target current reduction	31:23	ENTRY 0 -LSB - byte 0 Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V bEntry_00 = 1V5 ... bEntry_42 = 5V7 Bits[7:0] = Target current reduction in mA (unsigned)
AWC amp mod change	23:16	ENTRY 0 - byte 1 Bits[7:0] = Relative change of modulated amplitude level (signed)
AWC edge time constant for ASK100	15:8	ENTRY 0 - byte 2 Bits[3:0] = ASK100, Relative change of falling edge time constant (signed) Bits[7:4] = ASK100, Relative change of rising edge time constant (signed)
AWC falling edge time constant for ASK10	7:0	ENTRY 0 -MSB - byte 4 Bits[3:0] = ASK10, Relative change of falling edge time constant (signed) Bits[7:4] = ASK10, Relative change of rising edge time constant (signed)

Loaded configuration After Field ON:

DPC regulates from unloaded VDDPA configuration 42 to 31. Consequently, new configuration to be applied based on index entry 31.

Target current stays at 280 mA.

Technology B106: amp_mod=205, falling edge time constant=2, rising edge time constant=0

9.4.3.2 DPC characteristics

Table 12. Dynamic power control characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Minimum hysteresis configured in EEPROM DPC_HYSTERESIS	Depends on application target current	ApplicationTargetCurrent * 0.0609 + 2 mA	-	-	mA
	Max target current configured in EEPROM DPC_TARGET_CURRENT	Hysteresis as configured in DPC_HYSTERESIS		-	350-Hysteresis	mA

9.4.4 Adaptive waveshape control (AWC)

Depending on the level of detected detuning of the antenna, wave shaping related register settings can be automatically updated.

Two different waveshaping mechanisms can be used:

1. Firmware based shaping (1,2,3)
2. Lookup table based shaping (4,5,6)

The Firmware based shaping allows to correct rise times and overshoot with linear transition shapes.

The lookup table based shaping allows maximum flexibility and enables to configure almost any possible correction.

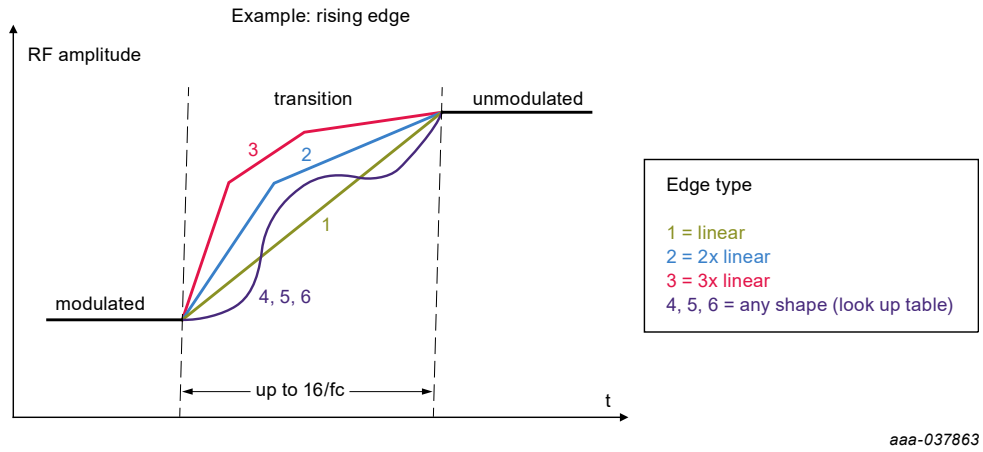


Figure 9. Waveshaping transitions (example falling edge)

The shaping related register settings are stored in a lookup table located in EEPROM, and selected dependent on the actual detected detuning condition.

Each lookup table entry allows the configuration not only of a dedicated wave shaping configuration for the corresponding detuning condition. But allows in addition to configure the wave shaping individually dependent on the actual protocol which is active.

Features of the Adaptive Waveshape Control:

- No external components required
- No need to compromise antenna matching to meet waveshape requirements

- Waveshapes automatically adapted according to detected detuning condition
- RF standards define envelope timing and residual carrier parameters required for compliance and interoperability.

The device supports the design of compliant antennas by allowing to actively shaping the style of edge transition for falling and rising edges. The shaping of modulation edges is achieved by selecting one from three edge transition styles:

1. Linear transition between two amplitude levels

2. Two linear transition´s between amplitude levels and

3. Three linear transitions between amplitude levels.

The type of the transition is selected in the EEPROM registers EDGE_TYPE_(protocol), and can be defined independent for each RF protocol and data rate - for both falling and rising edge.

The EEPROM registers EDGE_STYLE_(protocol) define the time constant "s" of falling/rising edge (depends on edge style).

The EEPROM registers EDGE_LENGTH_(protocol) define the total length of the edge pattern.

The figures below illustrate the edge type for the falling edge.

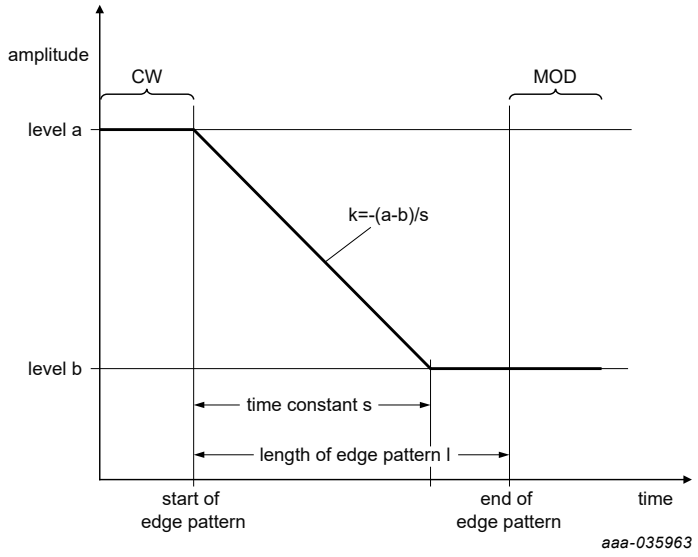


Figure 10. One linear transition (example falling edge)

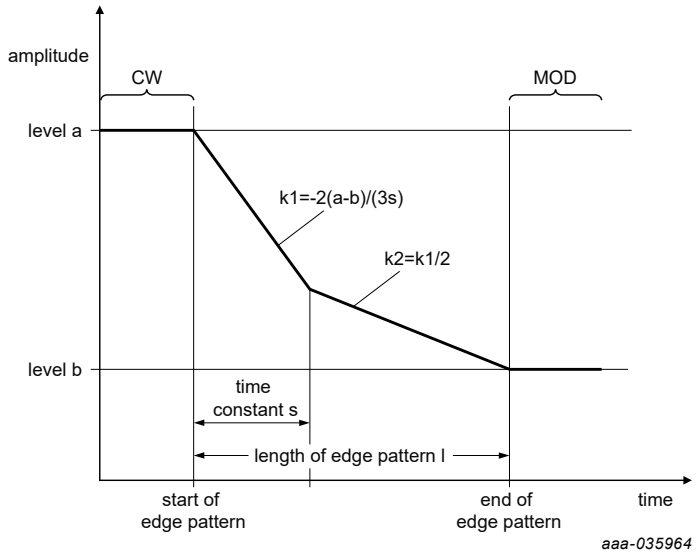


Figure 11. Two linear transitions (example falling edge)

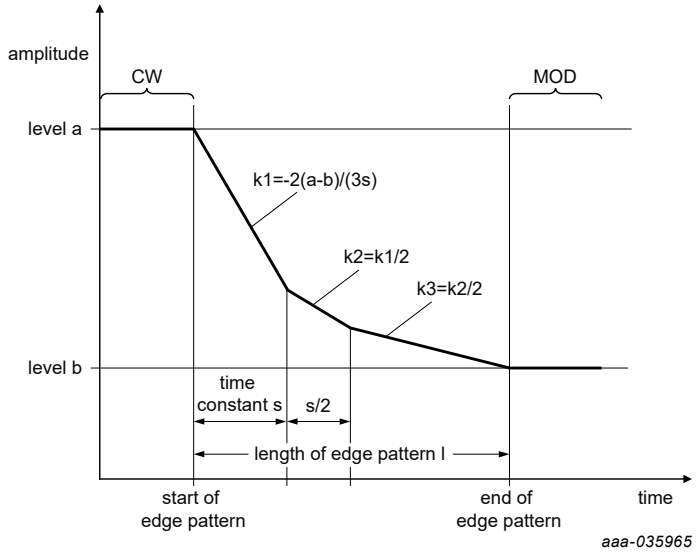


Figure 12. Three linear transitions (example falling edge)

The transition patterns are used as implicit pre-distortion to compensate effects of TX loading circuitry (e.g. resonant circuitry parameters) to the emitted RF envelope.

9.4.5 Adaptive receiver control (ARC)

Depending on the level of detected antenna detuning, receiver-related register settings can be automatically updated. The receiver-related registers which are allowed to be dynamically controlled are:

DGRM_RSSI_REG ->DGRM_SIGNAL_DETECT_TH_OVR_VAL

SIGPRO_RM_TECH_REG ->RM_MF_GAIN,

The adaptive receiver control settings override the default RM_MF_GAIN and DGRM_SIGNAL_DETECT_TH_OVR_VAL settings configured by the command LOAD_RF_CONFIGURATION.

The ARC algorithm is called when VDDPA voltage changes after DPC. There are two lookup tables used in ARC algorithm i.e VDDPA lookup and ARC lookup. In case of a VDDPA change, an EEPROM lookup (at current protocol and baud rate) is performed. The receiver-related settings i.e RM_MF_GAIN, DGRM_SIGNAL_DETECT_TH_OVR_VAL and IIR_ENABLE are read from EEPROM lookup table and configured in registers.

VDDPA lookup table:

VDDPA lookup table define maximum five voltage ranges. Number of VDDPA voltage ranges used in ARC algorithm is configured in bArcConfig[2:0]. VDDPA voltage output from DPC algorithm is input to VDDPA lookup. VDDPA lookup returns VDDPA_range_index (i.e 0,1,2,3,4).

Table 13. ARC_VDDPA EEPROM configuration bit description

Function	Bit	Description
ARC VDDPA Setting	7:0	Byte[4] = ARC_VDDPA_0: ARC_VDDPA_3 > VDDPA < ARC_VDDPA_4
	7:0	Byte[3] = ARC_VDDPA_0: ARC_VDDPA_2 > VDDPA < ARC_VDDPA_3
	7:0	Byte[2] = ARC_VDDPA_0: ARC_VDDPA_1 > VDDPA < ARC_VDDPA_2
	7:0	Byte[1] = ARC_VDDPA_0: ARC_VDDPA_0 > VDDPA < ARC_VDDPA_1
	7:0	Byte[0] = ARC_VDDPA_0: 1.5 > VDDPA < ARC_VDDPA_0

ARC lookup table:

VDDPA index and **RF protocol/datarates** are input to ARC lookup. There are five Receiver settings entries for each protocol and data rates. ARC algorithm select one out of five entries (at current protocol and baud rate) based on VDDPA_range_index.

Following table show ARC settings for Type A-106.

Table 14. ARC_RM_A106 EEPROM configuration bit description

Function	Bit	Description
RM_RX_ ARC_4	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ ARC_3	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Table 14. ARC_RM_A106 EEPROM configuration bit description*...continued*

Function	Bit	Description
RM_RX_ ARC_2	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ ARC_1	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *For ISO14443-A: In case ARC is disabled, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default))*

Note: *For ISO14443-A: In case Bit[15] is configured to 0, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default)) if the ARC is enabled.*

9.4.6 Energy saving card detection

There is no trimming for the Low Frequency Timer required.

9.4.6.1 Ultra low-power card detection (ULPCD)

The ULPCD (ultra low-power card detection) offers highest current saving. In this mode, the only wake-up sources to escape from the card detection loop are either a detected antenna detuning, a signal on GPIO3 or a reset (RESET_N) of the PN7642.

The ULPCD cannot be used together with the DC-DC function. A connection as described in the chapter "TX_LDO transmitter supply" or "Direct transmitter supply" is recommended.

Only the wake-up timer is active during ULP Standby state.

The ULPCD comprises 2 phases:

1. **Calibration phase**
   In this phase, an RF field is established and the field strength(RSSI) for the unloaded state of the antenna is measured to be used during the measurement phase and stored in a low-power persistent register.
2. **Measurement phase**
   In the measurement phase, the card detection activity is performed autonomously by the hardware at configurable time intervals. This configuration is passed as a parameter to the SWITCH_MODE_LPCD command. The RSSI value is measured and compared against the reference value measured in the calibration phase. A card is detected to be in the proximity of the reader when the measured RSSI differs from the reference RSSI by more than a configurable threshold.

The host can set the PN7642 into ultra-low power card detection state (ULP Standby state) via the instruction SWITCH_MODE_LPCD.

XTAL_CHECK_DELAY allows to optimize the startup of the crystal for the LPCD and ULPCD modes.

The following EEPROM configuration is available:

- ULPCD_VOLTAGE_CTRL
- ULPCD_RSSI_GUARD_TIME
- ULPCD_RSSI_SAMPLE_CFG
- ULPCD_THRESH_LVL
- ULPCD_GPIO3 - Allows to abort the ULPCD based on GPIO input.

9.4.7 Automatic EMD error handling

The PN7642 supports a configurable EMD handling according to the ISO14443 or EMVCo standard. To support further extensions or changes of these standards, the EMD block is configurable.

After being configured, the PN7642 restarts both the receiver and a timeout timer automatically without host interaction in case of a detected EMD event.

Features of the Automatic EMD Error Handling:

- No real-time constraints
- Less processing load on the host processor
- Configurable, anticipating future specification changes

In addition to the EMD error handling according to ISO14443 and EMVCo, the PN7642 implements special features for FeliCa™ preamble processing.

Registers CLIF_RX_EMD_1_CONFIG and CLIF_RX_EMD_0_CONFIG hold the configurations for the EMD configurations for ISO/IEC14443, and NFC Forum.

EMVCo EMD configuration is supported in the register EMD_CONTROL.

9.4.8 Autocoll (card emulation)

The Autocoll state machine performs the time critical activation for Type-A PICC and for NFC-Forum Active and Passive Target activation (card emulation mode).

The PICC state machine supports three configurations:

- Autocoll mode0: Autocoll mode is left when no RF field is present
- Autocoll mode1: Autocoll mode is left when one technology is activated by an external reader. During RFoff, the chip enters standby mode automatically

- Autocoll mode2: Autocoll mode is left when one technology is activated by an external reader. During RFoff, the chip does not enter standby mode.

At start-up, the Autocoll state machine automatically performs a LOAD_RF_CONFIG with the General Target Mode Settings. When a technology is detected during activation, the Autocoll state machine performs an additional LOAD_RF_CONFIG with the corresponding technology.

The card configuration for the activation is stored in EEPROM. If RandomUID is enabled (EEPROM configuration), a random UID is generated after each RF-off.

For all active target modes, the own RF field is automatically switched on after the initiator has switched off its own filed.

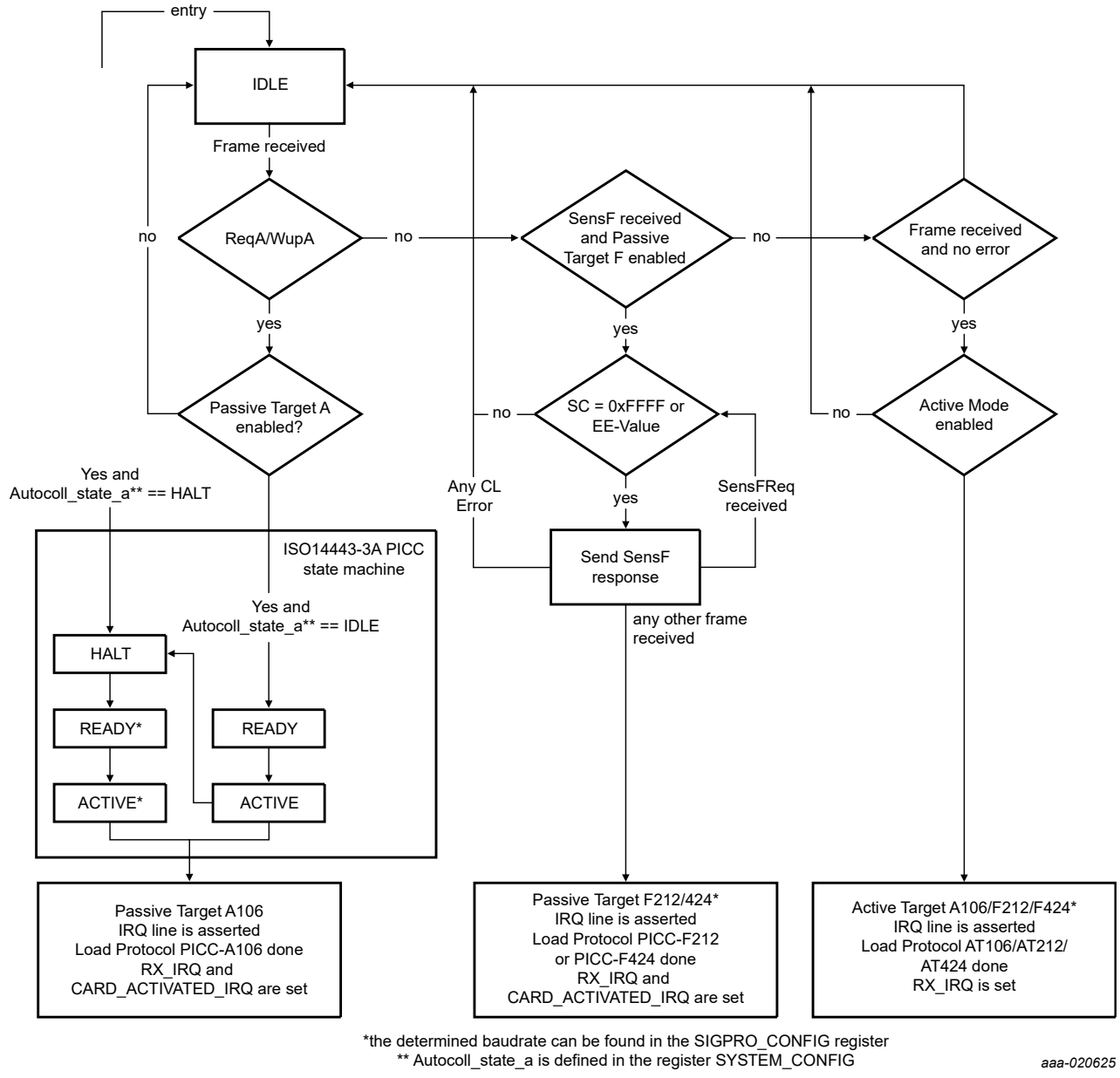


Figure 13. Autocall state machine

9.4.9 RF-level detection

The PN7642 implements an RF level detector (RFLD) and an NFC level detector (NFCLD) which allows to detect the presence of an external RF field.

RF Level Detector:

During low-power card detection (LPCD), the RF level detector (RFLD) acts as wake-up source from power-saving mode.

During ultra low-power card detection (ULPCD), a specific ultra low-power RF level detector is used as RF level detector(RFLD). This can be enabled as wake-up source.

The purpose of the RFLD function is to detect any signal at 13.56 MHz in order to wake up the PN7642 from power-saving mode.

NFC Level Detector:

The NFC Level detector (NFCLD) is used during full power mode. The NFCLD function is required by NFC Forum to support the "RF collision avoidance".

The sensitivity of the NFCLD sensor can be configured by EEPROM register to meet the NFC Forum requirements.

It can be used as well in card mode to detect an external field.

9.4.10 Antenna tuning with variable capacitors

The PN7642 allows the tuning of the connected antenna based on variable capacitors.

Variable capacitors are devices which allow to change their capacity dependent on a supplied control voltage. Typically, these capacitors are used as serial and parallel capacitors in an antenna matching network.

The PN7642 allows to measure a detuning of the connected antenna caused e.g. by surrounding metal and correct the actual detuning by applying an appropriate control voltage on 2 analog outputs.

To correct a potential detuning of the connected antenna, a phase measurement needs to be performed. The following sequence is required to read out the phase information:

Step 1: Disable DPC

Step 2: Perform Type A-106 load protocol

Step 3: Set the VDDPA Voltage as $V\_(Vddpa\_AAT)$

Step 4: Perform RF ON

Step 5: Read out RXM phase

Step 6: Perform RF OFF

Step 7: Enable DPC

For reading the RXM phase, refer to the related application note. Based on the phase information, a host is able to calculate the DAC output voltages to correct a detuning.

The antenna tuning requires the DPC to be disabled, and is typically not suitable for dynamic tuning e.g. during card communication.

Note:

Since disabling of the DPC requires a modification of the EEPROM is required, care must be taken not to exceed the maximum permitted number of Erase/Write cycles.

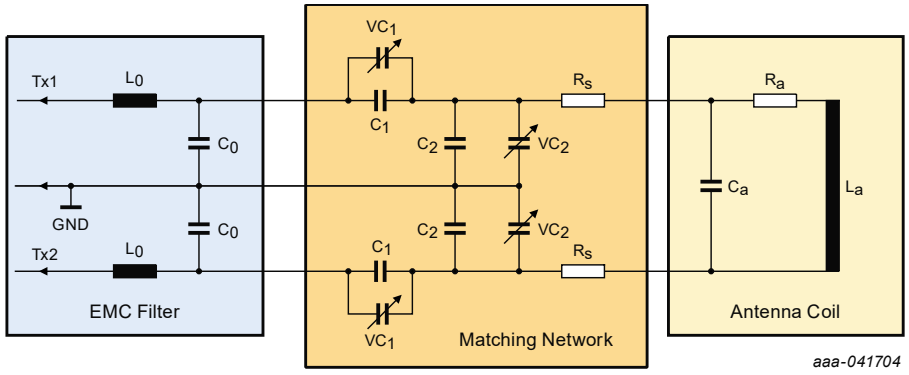


Figure 14. Antenna connection using variable capacitors

9.4.11 RF debug signals

The following signals are available for debugging purposes:

The test signals are selected by sending a command string to the PN7642. The commands CONFIGURE_TESTBUS_DIGITAL and CONFIGURE_TESTBUS_ANALOG are used to configure the dedicated signal on an output pin.

If used, **ADC-Q needs to be routed always to AUX1, ADC-I needs to be routed always to AUX2**

The analog test signals are analog representation of an internal digital value. The internal digital signal is converted by an 8-bit wide DAC to the analog signal.

This overview indicates the signals which are available for debugging purposes (indicated by numbers):

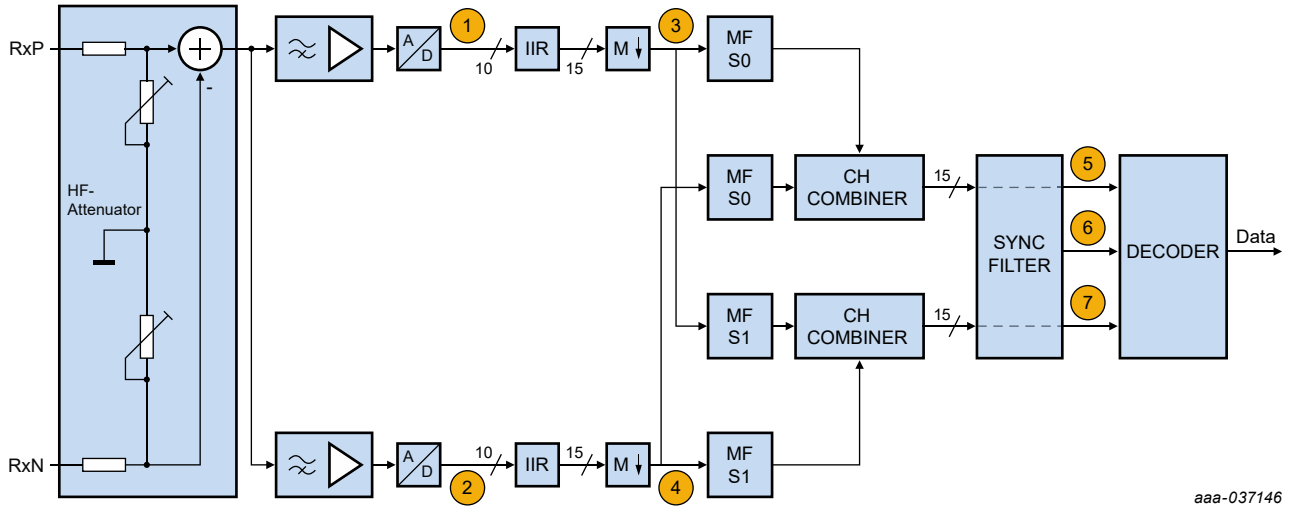


Figure 15. Receiver block diagram

Table 15. DEBUG SIGNALS

Signal	REGISTER	SIGNAL NAME	BITS	Description
ADC Data I Channel (1)	obs_clif_ tbcontrol_ patchbox0	adc_ data_i_i	9:2	Unfiltered I channel signal upper 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
	obs_clif_ tbcontrol_ patchbox1		9; 6:0	Unfiltered I channel signal lower 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
ADC Data Q Channel (2)	obs_clif_ tbcontrol_ patchbox2	adc_ data_q_i	9:2	Unfiltered Q channel signal upper 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
	obs_clif_ tbcontrol_ patchbox3		9; 6:0	Unfiltered Q channel signal lower 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
Preprocessor Out I Channel (3)	obs_clif_sigpro_ rm0	rm_cor_ adc_i_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data I channel, after IIR Filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_ rm1		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data I channel, after IIR Filter and down-sampling
Preprocessor Out Q Channel (4)	obs_clif_sigpro_ rm2	rm_cor_ adc_q_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data Q channel, after IIR Filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_ rm3		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data Q channel, after IIR Filter and down-sampling
Output MF S0 (5)	obs_clif_sigpro_ rm4	mf_pt_ s0_d	14:8	Delayed matched filter S0 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_ rm5		7:0	Delayed matched filter S0 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner
Output MF S1 (6)	obs_clif_sigpro_ rm6	mf_pt_ s1_d	14:8	Delayed matched filter S1 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore) Remark: S1 is not relevant for type A 106
	obs_clif_sigpro_ rm7		7:0	Delayed matched filter S1 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner Remark: S1 is not relevant for type A 106
Output Synchronization Filter (7)	obs_clif_sigpro_ rm8	sync_filt_ out	14:8	Synchronization filter output upper 7 bit of the 15 bit signed synchronization filter output including sign (bit14) bit 15: RFU (ignore)

Table 15. DEBUG SIGNALS *...continued*

Signal	REGISTER	SIGNAL NAME	BITS	Description
	obs_clif_sigpro_rm9		7:0	Synchronization filter output lower 8 bit of the 15 bit signed synchronization filter output
clif_status	transceive_state		7:5	
	rx_cl_error		4	
	tx_envelope		3	
	rx_enevelope		2	
	svalid		1	
	sdata		0	
clif_transceive	rx_start_receive		7	
	rx_over_ok		6	
	rx_over_term		5	
	rx_resume		4	
	sgp_msg_busy		3	
	fig_reset_sigpro		2	
	fig_reset_rxdec		1	
	cfg_sw_reset_sigpro		0	

Table 16. TRIGGER SIGNALS

TRIGGER	REGISTER	SIGNAL NAME	BITS	Description
TX Active	obs_clif_txenc1	tx_active_o	1	high level indicates transmission of data Remark: Falling edge can be used to trigger on end of transmission.
RX Enable	obs_clif_sigpro_rm15	rx_enable_o	1	high level indicates that the reception is ongoing Remark: can be used to trigger on the start /end of reception
RX collision detected	obs_clif_sigpro_rm14	rm_scoll_o	1	high-level pulse indicates that the collision is detected during reception

9.5 Power, Clock and Reset Management

9.5.1 General

In PN7642 the Power, Clock and Reset Management (PCRM) Unit is a collection of sub systems whose key functions are:

- Controlling the PN7642 system’s hardware boot sequence
- Managing the power modes the system can operate in, inclusively power domain enabling/disabling and isolation control
- Managing wake-up event capturing and the transitions between the power modes (i.e. make sure that blocks are enabled/disabled according to their power profiles in the currently active power mode)

- Monitoring environmental conditions (supply state, battery power state, temperature, IO pad state, etc.)
- Digital clock management, clock distribution and architectural clock gating
- Digital reset management and reset distribution
- General-purpose AD converter with 10 logical channels and various data post processing options (filtering, min, max, moving average, etc.)
- IO pad control
- Interrupt controller
- 2 Antenna tuning control (Antenna Tuning DACs)
- Low-power and ultra low-power field/card detection controller

9.5.2 Interrupt controller

The power, clock and reset (PCRM) unit of PN7642 implements various interrupt sources which are collected to a single interrupt line, connected to the Cortex M33's Nested Vectored Interrupt Controller (NVIC). The PCRM interrupt controller manages these triggers, allows for masking them, resp. for configuration whether an interrupt request should be generated based on an interrupt source's rising or falling edge or whether a request shall be generated on both edges.

The following figure shows a high-level view of the interrupt controller and its connectivity to the PCRM configuration registers:

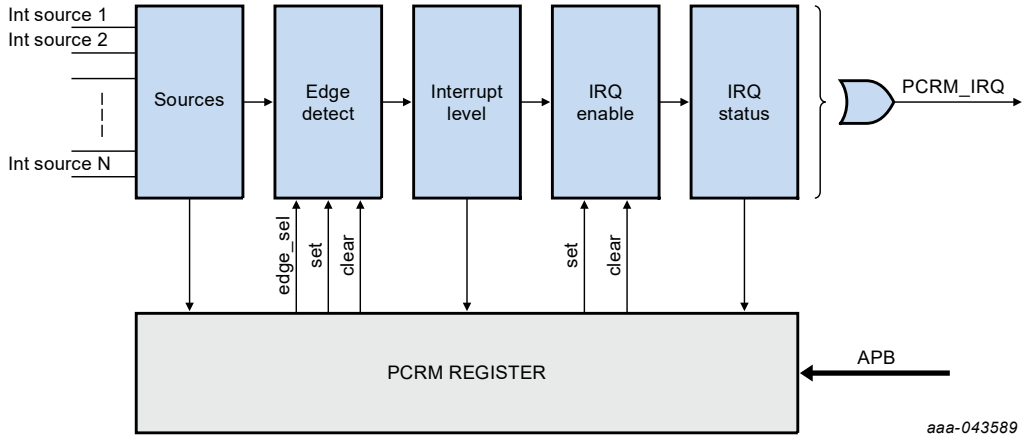


Figure 16. PCRM Interrupt controller

The following table shows a consolidated list of PCRM interrupt events, and their configuration options:

Table 17. PCRM Interrupt Sources

Source / Event	Possible Event Type
GPIO 0 Activity	Rising / Falling / Both
GPIO 2 Activity	Rising / Falling / Both
GPIO 3 Activity	Rising / Falling / Both
GPIO X Common Activity	Rising / Falling / Both
VDDIO OK	Rising / Falling
XTAL Ready	Rising
XTAL Error	Rising
GPADC Channel 0	Rising
GPADC Channel 1	Rising

Table 17. PCRM Interrupt Sources*...continued*

Source / Event	Possible Event Type
GPADC Channel 2	Rising
GPADC Channel 3	Rising
GPADC Channel 4	Rising
GPADC Channel 5	Rising
GPADC Channel 6	Rising
GPADC Channel 7	Rising
NFC Temperature warning	Rising / Falling
PMU Temperature warning	Rising
PMU ADPLL Locked	Rising / Falling
Field Clock OK	Rising / Falling / Both
VUP OK	Rising / Falling
VDDPA over current	Rising
RX Protection Alarm	Rising

9.5.3 Brownout detection

The PN7642 includes a Brownout detector to monitor the voltage of VBAT. If the voltage falls below the specified threshold, the BOD generates a shutdown request to the system.

In order to avoid any ringing of the generated status output, the voltage is expected to be in good condition for a certain time interval during the checking window, otherwise it is considered being a false signal and will be ignored.

9.5.4 VEN monitor

The VEN monitor is implemented as a small Finite State Machine (FSM), and is in charge of

- monitoring the VEN pad status
- monitoring whether the external PADIO voltage was lost
- generating a request to either HARD POWER DOWN or PMU OFF mode.

The FSM is clocked by the LFO and similar to the Brownout detector, it introduces some filtering when sampling the VEN pad. Furthermore, the VEN low pulse width is used to distinguish between a standard system reset and a request to go to either HARD POWER DOWN or PMU OFF mode.

9.5.5 VDDIO monitor

The VDDIO is supplying the NFC pads. The Analog Power Management Unit (PMU_ANA) has a monitor which outputs VDDIO_OK to the PCRM. The PCRM requires to monitor VDDIO_OK continuously in order to initiate power down to HPD or OFF mode. Or initiate a wake-up from HPD mode depending on the value of VEN internal.

The VDDIO loss detection can be also a condition to exit OFF-mode. The behavior is configurable through the PMU_ANA which is supplied even in OFF-mode.

9.6 Peripherals

9.6.1 Communication peripherals

The PN7642 embeds the following interfaces for host connection:

- USB
- SPI target
- I^2C target
- I^3C target
- UART
- SPI controller
- I^2C controller

The host interfaces share the same pins and cannot be used at the same time. The type of host interface is selected by configuring the PCRM registers.

Table 18. Pin description for host interface

Pin name	SPI	I^2C	USB
ATX_A	SPI MISO	I^2C SDA	-
ATX_B	SPI SCK	I^2C SCL	-
ATX_C	SPI NSS	I^2C Adr Bit 0	USB D+
ATX_D	SPI MOSI	I^2C Adr Bit 1	USB D-

Note: The host interface pins should not be kept floating.

The host interfaced to be used on the product must be selected by the pins HOST_IF_SEL0 and HOST_IF_SEL1 according to the following table.

Table 19. Selection of the host interface

HOST_IF_SEL1	HOST_IF_SEL0	Resulting interface
LOW	LOW	I^2C target
LOW	HIGH	SPI target
HIGH	LOW	UART
HIGH	HIGH	I^3C target

9.6.1.1 SPI target interface

The maximum SPI speed is 15 Mbit/s and fixed to CPOL = 0 and CPHA = 0. Only a half-duplex data transfer is supported. There is no chaining allowed, meaning that the whole instruction has to be sent or the whole receive buffer has to be read out. The whole transmit buffer shall be written at once as well. No NSS assertion is allowed during data transfer.

The SPI host interface is designed to support the typical interface supply voltages of 1.8 V and 3.3 V of CPUs. A dedicated supply input which defines the host interface supply voltage independent from other supplies is available (pin VDDIO).

There is no external pull-up / pull-down resistor required, the SPI pads are automatically configured by the PN7642.

Only a voltage of 1.8 V or 3.3 V is supported, but no voltage in the range of 1.95 V to 2.4 V.

Note: The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT.

Controller in target out (MISO)

The MISO line is configured as an output in a target device. It is used to transfer data from the target to the controller, with the most significant bit sent first. The MISO signal is put into 3-state mode when NSS is high.

Controller out target in (MOSI)

The MOSI line is configured as an input in a target device. It is used to transfer data from the controller to a target, with the most significant bit sent first.

Serial clock (SCK)

The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines.

Not target select (NSS)

The target select input (NSS) line is used to select a target device. It shall be set to low before any data transaction starts and must stay low during the transaction.

9.6.1.2 I^2C target interface

The I^2C interface is compliant with the I^2C Bus Specification 3.0.

Key features of the I^2C target interface are:

- 8-bit I^2C target address, where 2 LSBs can be configured.
- Supported transfer modes

Table 20. I^2C modes and maximum bit rates

Mode	Max Bitrate
Standard-mode (Sm)	100 Kbit/s
Fast-mode (Fm)	400 Kbit/s
Fast-mode Plus (Fm+)	1 Mbit/s
High-speed mode (Hs-mode)	3.4 Mbit/s

- Half duplex mode
- I^2C target mode
- Selection of the I^2C address done by two pins. I^2C_ADR1 and I^2C_ADR0.
  - It supports multiple addresses
  - The upper bits of the I^2C target address are hard-coded. The value corresponds to the NXP identifier for I^2C blocks. The value is 01010XXb

Table 21. I²C interface addressing

I^2C_ADR1	I^2C_ADR0	I^2C address (R/W = 0, write)	I^2C address (R/W = 0, read)
0	0	0x28	0x28
0	1	0x29	0x29
1	0	0x2A	0x2A
1	1	0x2B	0x2B

9.6.1.3 I^3C target interface

The I^3C target interface is compliant to the MIPI I^3C standard. It implements major improvements in terms of usage and power consumption and therefore can be used as an alternative to SPI communication for mid-level communication speeds.

Key features of the I^3C target interface are:

- 2 wire multi-drop bus capable of 12 MHz clock speeds with up to 11 devices
- Target addresses are dynamically assigned, but may have a static address at start
- In-Band interrupts, allowing Targets to notify the Controller without requiring a separate GPIO
- Interrupts can be started even when Controller is not active on the bus, and yet no free running clock is needed
- Built-in commands in separate "space" do not collide with normal Controller to Target messages
- Hot-join onto bus allows devices to get online later than the initial bus bring up. Hot-join is supported to request for a new dynamic address after wake-up
- High Data Rate DDR option (HDR-DDR) provides about twice the data rate of SDR (about 20 Mbit/s)

9.6.1.4 UART interface

The PN7642 integrates a Low-Power Universal Asynchronous Receiver / Transmitter (LPUART) module.

The LPUART shares the pins with the I2C, I3C, SPI, and USB interfaces. The LPUART operation need to be selected by configuring the pins HOST_IF_SEL0 and HOST_IF_SEL1 accordingly.

The following features are supported:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock:
  - Baud rate can be configured independently of the bus clock frequency
  - Supports operation in Stop modes
- Hardware parity generation and checking
- Programmable 7-bit, 8-bit, 9-bit, or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
  - Receiver data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- Independent FIFO structure for transmit and receive
  - Separate configurable watermark for receive and transmit requests
  - Option for receiver to assert request after a configurable number of idle characters if receive FIFO is not empty

9.6.1.5 USB device interface

PN7642 incorporates a USB 2.0 Full-Speed device, compliant with USB 3.0 Hub connectivity capability.

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer.

The status of a completed USB transfer or error condition is indicated via status registers. If enabled, an interrupt is generated.

Features:

- Fully compliant with USB 2.0 specification (full speed)
- Dedicated USB PLL available
- Supports 12 physical endpoints including one control endpoint (3 Irq-In, 3 Irq-Out, 3 Bulk-In and 3 Bulk-Out). The first generic endpoint starts at logical endpoint number 1.
- Supports 6 logical endpoints
- Single or double buffering allowed
- Resume By Host
- Wake-up from suspend mode on USB activity and remote wake-up
- Suspend and Resume for power management
- SoftConnect Supported

9.6.1.5.1 Connecting the USB interface

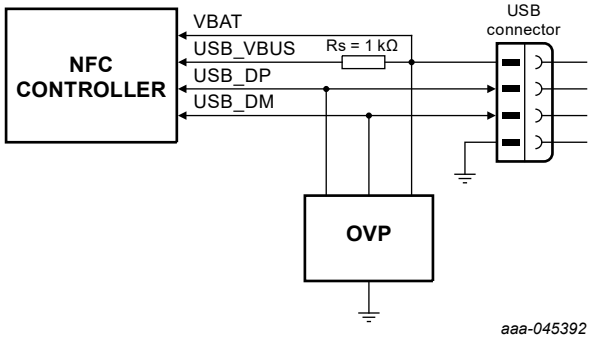


Figure 17. USB interface on a bus-powered device

The resistor R_s is used to minimize the impact of transient responses on the USB line. The resistance must be greater or equal to 1 kΩ to avoid damage to the device. When the USB interface is not used, the USB_VBUS pin shall be connected to the ground.

9.6.1.6 SPI controller interface

The device implements an SPI controller interface to connect to any external SPI devices.

The SPI controller interface implements separate receive and transmit FIFOs for data buffering and also implements separate DMA control for reception and transmission.

The SPI controller interface supports data frames of 1 to 16 bits. The transmit and receive FIFOs have a capacity of 8 entries each, whereas an entry represents 16 bits.

Up to four target select inputs/outputs are available. Clock phase/polarity and frame/transfer delays of the SPI protocol are all programmable through registers.

Features:

- Motorola SPI-compatible interface
- Data frames of 8 bits
- DMA support for both transmit and receive (full duplex)
- Option to "write without read" and "simultaneous control with data"
- Multiple target select pins
- Programmable delays (Pre delay, Post delay, Frame delay, Transfer delay)
- FIFOs have 8 entries with 16 bits each
- Data rate is firmware configurable.
- Max baud rate is ~22.5 MHz, considering clock of 45 MHz.
- Configurable Clock polarity and phase (SPO/SPH)
- Supports MSB/LSB first switch
- Supports generation of EOT, EOF

The SPI subsystem can be configured to drive up to four targets. Different protocol parameters (e.g. frame, transfer delays) are programmable. Data transmission and reception from/to the system memory is done via FIFOs in order to bridge any wait cycles in case of an access conflict to the system RAM.

Interrupt requests to the CPU occur on receiver data availability or on transmitter readiness to accept data. Also, the FIFOs can be programmed with a certain trigger level so that interrupts occur before the FIFOs run empty or reach a critical filling level.

DMA requests to the DMA controller occur as soon as space is available in TX FIFO or as soon as data becomes available in RX FIFO.

9.6.1.7 I^2C controller interface

The device implements an I^2C controller interface in order to connect any external I^2C target device.

The I^2C controller interface allows for operation in controller mode, target mode and also supports monitor mode. It is able to handle the following communication modes:

- Standard Mode (up to 100 kbit/s)
- Fast Mode (up to 400 kbits/s)
- Fast Mode (up to 1 Mbit/s)
- Fast Mode Plus (up to 3.4 Mbit/s)

Features:

- Independent controller, target and monitor functions
- Supports both
  multi controller
  multi controller with target
- Multiple I^2C target addresses supported in hardware
- One target address can be selectively qualified with an address range in order to allow versatile responses to multiple I^2C target addresses
- 10-bit addressing supported with software assistance
- Support for control and data transfer via DMA in all three modes (controller, target, monitor)
  – AMBA 3.0 compliant APB interface
- Automatic target acknowledgment or non-acknowledgement in conjunction with DMA
- The I^2C target function needs no on-chip clock to receive and compare an address and can thus wake up the host CPU from power down. The monitor function can also wake up the host.
- Supports System Management Bus (SMBus)
- Extra GPIO available to indicate data available to the I^2C controller
- Supports Device ID command

(with firmware assistance. Payload prepared by firmware to map to this command)
- Supports Generic Call Address command
  (with firmware assistance. Payload prepared by firmware to map this command)
- Supports Soft Reset command
  (with firmware assistance. Payload prepared by firmware to map to this command)

The I2C controller interface can be configured as Controller or Target. The default application mode is controller.

9.6.2 Digital peripherals

9.6.2.1 General-purpose I/O

The PN7642 provides 6 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

9.6.2.1.1 Features

- Bit-level set, clear, and toggle registers allow a single instruction set, clear or toggle of any number of bits in one port.
- Direction control of individual bits.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- All GPIO pins can be used to wake up the device from different power-saving modes.

9.7 System power states

The PN7642 can operate in different power states. The functionality and current consumption is dependent on the actual system power state.

Power states can be changed by the level on the pin RESET_N and by connecting/disconnecting the power supply of VBAT.

In addition, state changes are triggered from the user application of the device.

Disconnecting and connecting the power supply on VBAT restarts the PN7642 always in Active State after releasing the pin RESET_N (transition low to high).

A transition of low to high on pin RESET_N restarts the PN7642 always in Active State.

The following power states are supported:

Power state	Description
Power OFF state	The PN7642 device (supply pin VBAT, RF transmitter) is not supplied by a battery/system PMU. Other domains might be supplied (for example, IO pad interface on pin VDDIO)
PMU OFF state	The PN7642 device is disabled via a low signal on pin RESET_N. No internal clocks of the PN7642 are active. Wake-up events to change PMU OFF state: Power reset on pin VBAT, VEN rising edge, RX ULPCD detect, ULP abort signal on PIN3
ULPCD state	The ULPCD (ultra low-power card detection) offers highest current saving. In this mode, the only wake-up sources to escape from the card detection loop are either a detected antenna detuning or a reset (RESET_N) of the PN7642. Only the wake-up timer is active during ULP Standby state.

Power state	Description
	The ULPCD comprises 2 phases: 1. Calibration phase: In this phase, an RF field is established and the field strength(RSSI) for the unloaded state of the antenna is measured to be used during the measurement phase and stored in a low-power persistent register. 2. Measurement phase: In the measurement phase, the card detection activity is performed autonomously by the hardware at configurable time intervals. This configuration is passed as a parameter to the SWITCH_MODE_LPCD command. The RSSI value is measured and compared against the reference value measured in the calibration phase. A card is detected to be in the proximity of the reader when the measured RSSI differs from the reference RSSI by more than a configurable threshold. The user application can set the PN7642 into Ultra-low power card detection state (ULP Standby state) via programming of the ULPCD bit. XTAL_CHECK_DELAY allows to optimize the startup of the crystal for the LPCD and ULPCD modes. The following EEPROM configuration is available: ULPCD_VOLTAGE_CTRL ULPCD_RSSI_GUARD_TIME ULPCD_RSSI_SAMPLE_CFG ULPCD_THRESH_LVL ULPCD_GPIO3
Hard power down state	The PN7642 is disabled via the reset/enable signal on VEN or by detecting an external condition (for example, battery voltage monitor). The power dissipation is reduced to a minimum. No power dissipation or leakage is expected on the different interfaces. Low-power resources are enabled (VDDC_LP, VHV_LP, LQ_REF, LQ-BIAS). LFO clock is available. PCRM is supplied and is running in low-power state. I/Os are supplied by VDDC_HP. Wake-up events: Power reset on pin VBAT, VEN rising edge, RX ULP detect
Standby state	The user application can set the PN7642 into a low-power mode to minimize power dissipation. The state of external interfaces is maintained properly. PMU operates in low-power state. Wake-up counter clock is available. PCRM is supplied and running in low-power mode. I/Os are supplied by VDDC_LP. PMU FSM in PCRM manages the transition in power state. Wake-up sources: Activity on host IF, SWPM communication, ULPDET, LPDET, wake-up counter, power loss on VDDIO, GPIO, RxPROT, No High Temp on TX and so on.
Suspend state	Suspend state is associated to the operation of the USB interface but can also be applied for other purposes. During Suspend state, the NFC digital subsystem including NV memory is kept powered. System RAM state is maintained. ROM is put to ShutDown mode. The I/O state is maintained. USB main clock supply is gated off under control of usb_need_clk. The HFO is switched off. The LFO is active. Wake-up sources: USB, host IF, wake-up counter, ULPDET, LPDET, Temp sensor, GPIO, VUP detected, power loss on VDDIO, interrupt from ISO AUX IF, RxPROT
Active state	The PN7642 is able to process internal or external events or data. All external power supply sources and the external clock need to be available, and all internal clocks are active.

9.8 Power supply

The device allows to configure different power supply options for the transmitter power amplifier. To make use of them, a combination of external connections and chip internal configurations needs to be done. The following supply options are available:

- Internal VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO). In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.
- Direct VDDPA configuration: This configuration is recommended for applications which require highest efficiency, like battery supplied devices. In this configuration, a battery can be connected directly to the

transmitter supply avoiding the voltage drop of approximately 0.3 V caused by the TX_LDO. A clean supply voltage without noise is required to achieve a good RF performance.
In this configuration the DPC, current measurement and overcurrent protection is not available.

9.8.1 System power supply overview

The PN7642 is using three different supplies each for the following functional blocks:

1. Supply for the host interface and GPIO's (VDDIO)

2. Supply for the analog and digital blocks (VBAT/VBAT_PWR)

3. Supply of the RF drivers (VDDPA), DC-DC (VBAT_PWR) and TX_LDO (VUP)

The functionality of the GPIO's, Host Interface and internal analog and digital blocks is independent from the supply of the RF Driver. This allows to configure a dedicated transmitter supply configuration at any time. Care shall be taken to switch on the RF field only after the transmitter-related power supply had been configured according to the external physical supply connections (VDDPA, VBAT_PWR, VUP).

The power supply configuration is configured in EEPROM and therefore will not get lost in case of power supply loss or reset of the chip. Typically, this configuration is only performed once during the production of a reader.

RF field shall not be turned on without setting the correct power supply configuration in the EEPROM.

Note: The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT. This limitation is not applicable in Power off mode.

9.8.2 Connecting blocking capacitors

Some pins are connected to blocking supply capacitors. PCB traces to these capacitors need to be as short as possible, and a low-ohmic grounding of the GND-side of the capacitors is required for optimized RF performance.

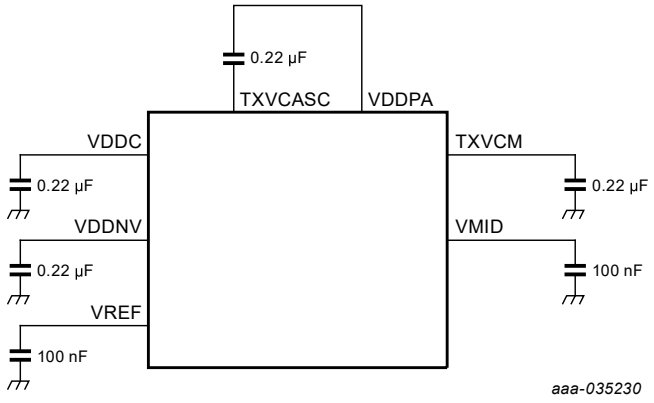


Figure 18. Blocking capacitors

9.8.3 Transmitter power supply

The PN7642 is configured by EEPROM for the different power supply options.

The following EEPROM Addresses are used to configure the power supply of the transmitter:

DCDC_PWR_CONFIG - Enables/disables and configures the DC-DC according to the external supply connections.

TX_LDO_CONFIG - Enables/disables and configures the TX_LDO.

TX_LDO_VDDPA_HIGH - initial out voltage when DPC is used.

TX_LDO_VDDPA_LOW - lowest VDDPA when DPC is used.

TX_LDO_VDDPA_MAX_RDR - maximum voltage to be set in reader mode used by DPC.

TX_LDO_VDDPA_MAX_CARD - VDDPA maximum voltage to be set in card mode used by DPC.

No specific registers are required to configure the pad supply (VDDIO) or the supply for the analog and digital blocks (VUP).

9.8.3.1 TX_LDO transmitter supply

TX_LDO supplied VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO).

In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.

A decoupling cap is required on VDDPA pin.

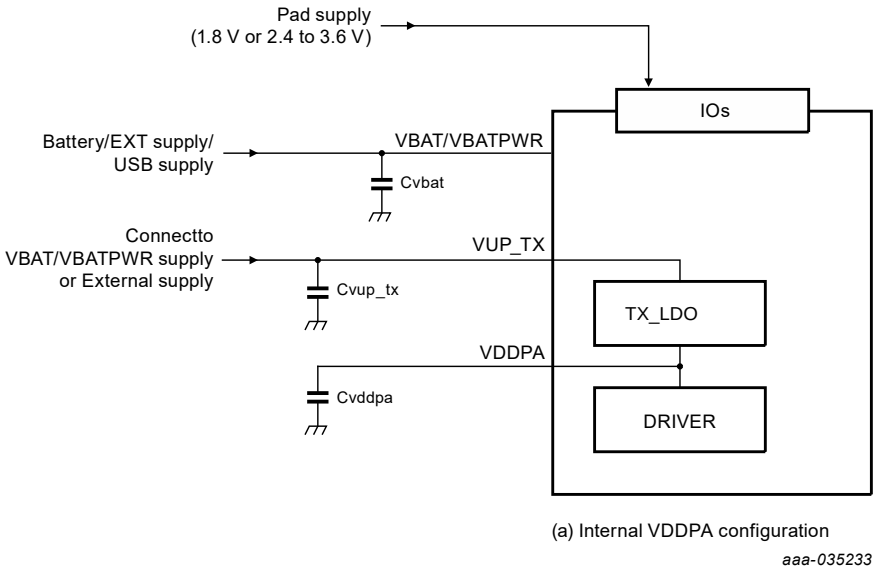


Figure 19. Transmitter supply

9.8.3.2 Direct transmitter supply

Direct VDDPA configuration:

TX_LDO must be configured OFF by SW configuration. VUP_TX and VDDPA connected to VBAT/VBATPWR.

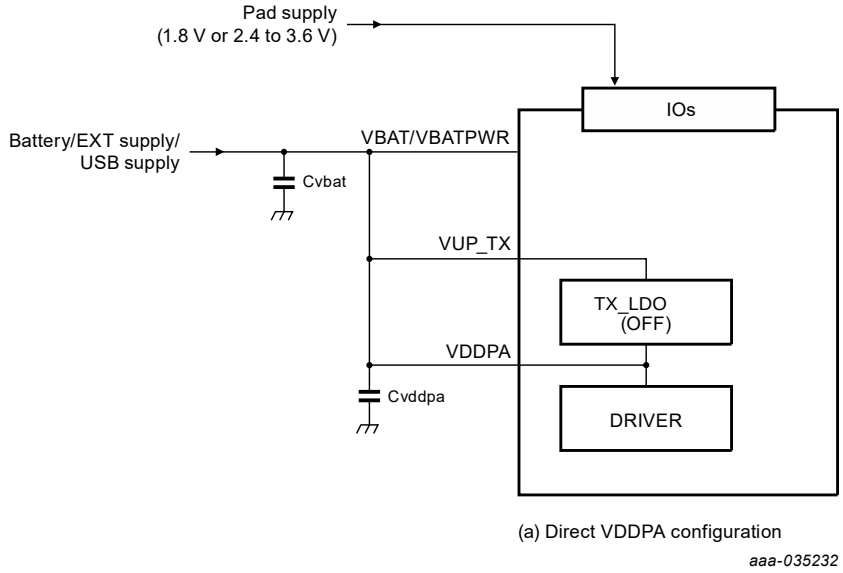


Figure 20. Direct transmitter supply

9.8.3.3 DC-DC (boost) supply

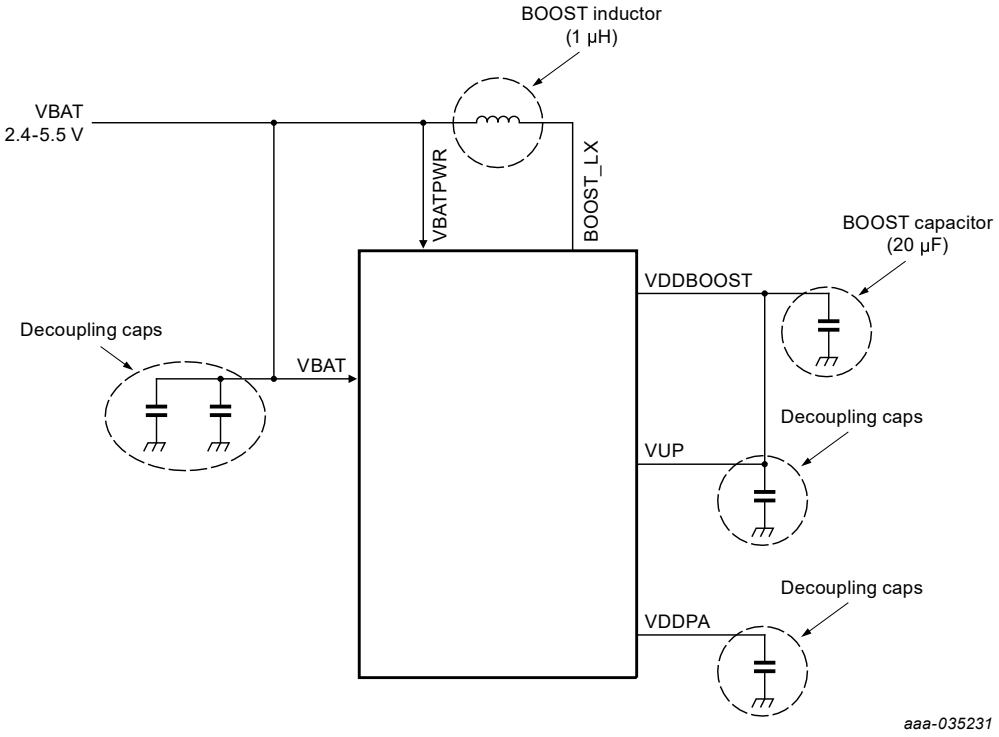


Figure 21. Transmitter supply by DC-DC

9.8.3.4 Configuration example 1: TX_LDO transmitter supply - DC-DC active

VBAT is connected to VBATPWR.

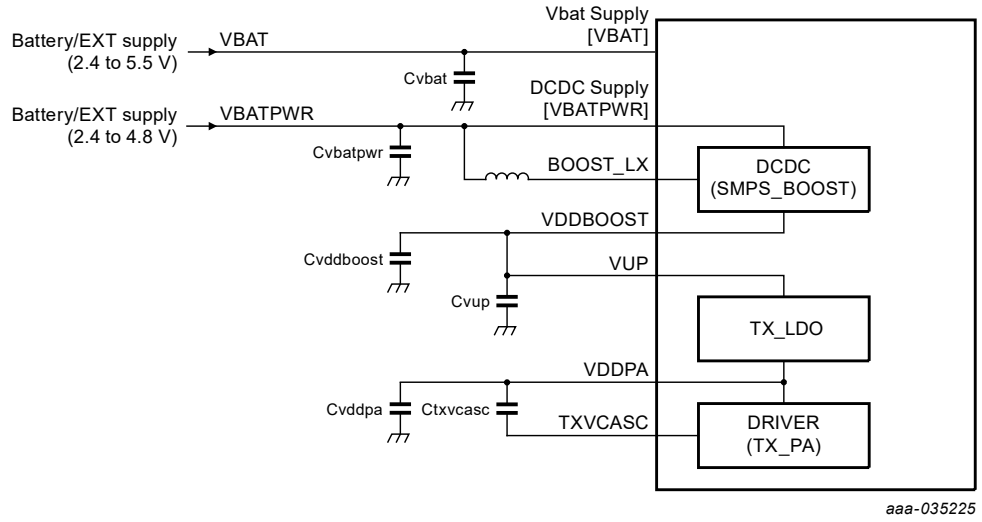


Figure 22. DC-DC active

9.8.3.5 Configuration example 2: TX_LDO transmitter supply - DC-DC bypassed

VBAT is connected to VBATPWR.

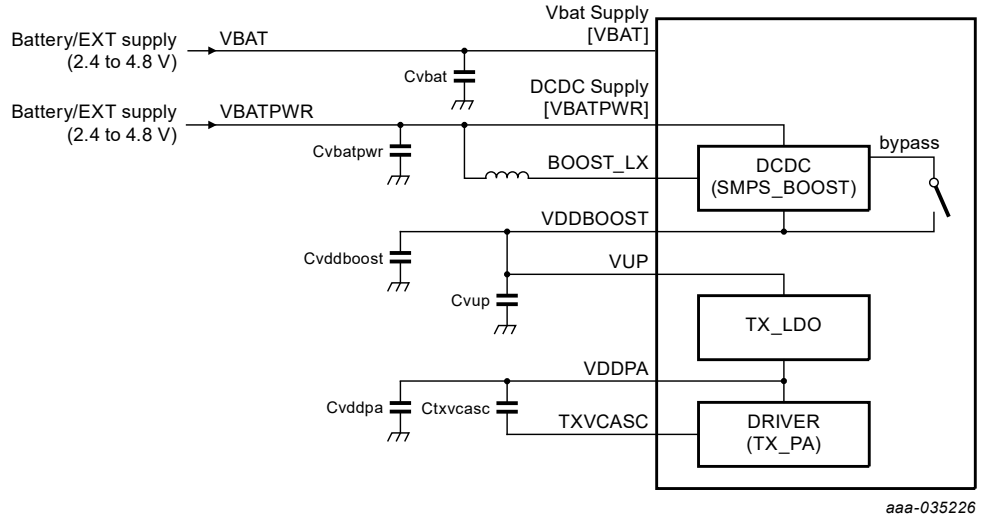


Figure 23. DC-DC bypassed (in DCDC_PWR_CONFIG)

9.8.3.6 Configuration example 3: TX_LDO transmitter supply connected to VBAT - no DC-DC

VBAT is connected to VBATPWR.

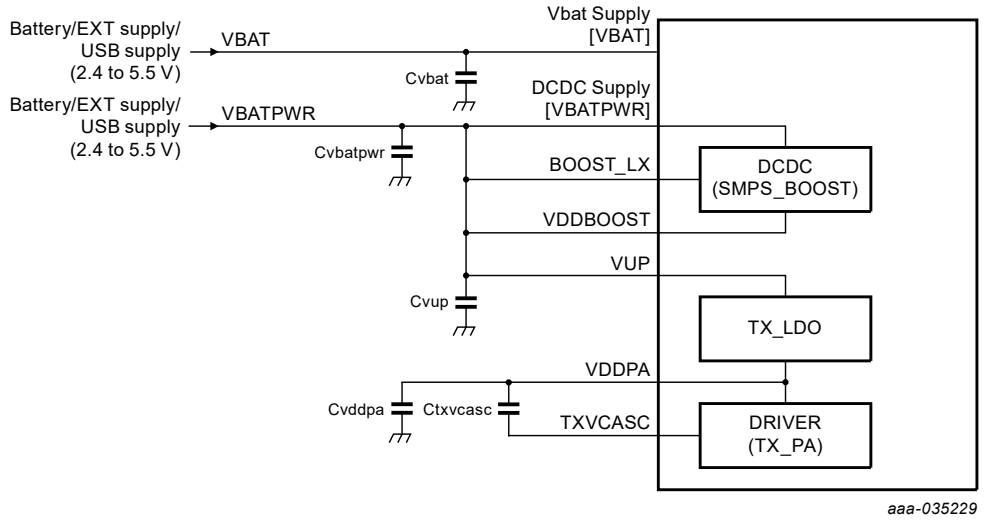


Figure 24. No DC-DC used

9.8.3.7 Configuration example 4: TX_LDO supplied independent from VBAT - no DC-DC

VBAT is connected to VBATPWR.

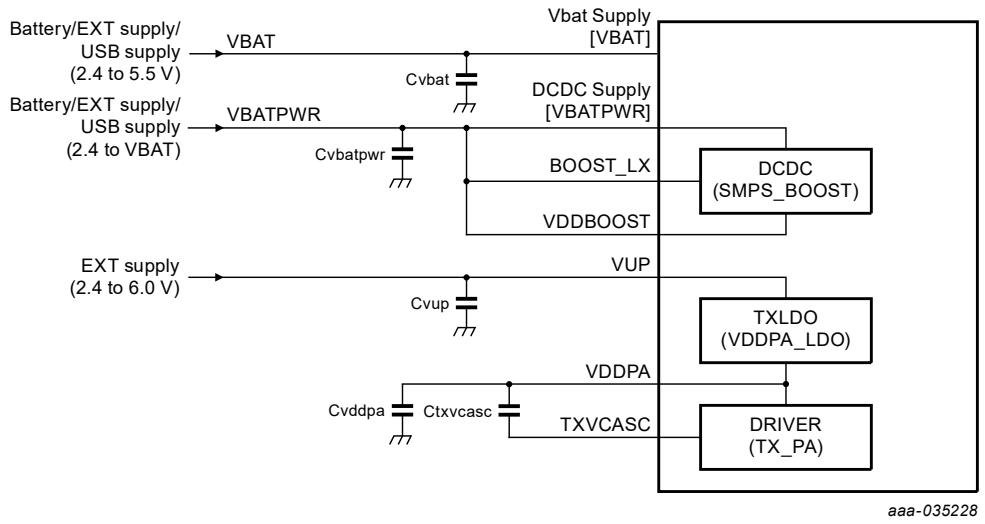


Figure 25. No DC-DC used

9.8.3.8 Configuration example 5: TX_LDO not used - no DC-DC

VBAT is connected to VBATPWR.

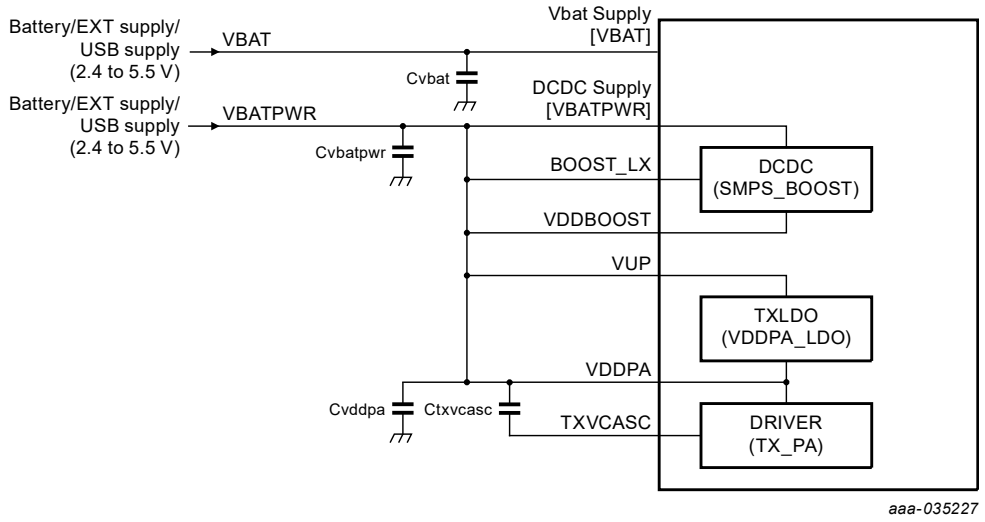


Figure 26. No DC-DC used - no TX_LDO

9.8.3.9 Supply voltage range for transmitter supply configuration examples

Table 22. Supply voltage range configuration

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independent from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
EEPROM configuration for DPC ENABLED - configured in DPC_CONFIG (address 0076h)					
DCDC_PWR_CONFIG (address 0000h)	- 0xE4(Variable BOOST with Auto Bypass). - 0xE2(Fixed BOOST)	0xE4 (Variable BOOST with Auto Bypass)	0x21	0x21	NA
TXLDO_VDDPA_HIGH (0x06)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	NA
TXLDO_VDDPA_MAX_RDR (0008h)	0x2A (5.7 V)	0x1C (4.3 V)	0x25 (5.2 V)	0x2A (5.7 V)	NA
BOOST_DEFAULT_VOLTAGE (000Ah)	0x1D (6 V).	NA	NA	NA	NA
EEPROM configuration - DPC DISABLED - configured in DPC_CONFIG (address 0076h)					
DCDC_PWR_CONFIG (address 0000h)	- 0xE4(Variable BOOST with Auto Bypass). - 0xE2(Fixed BOOST)	0xE4 (Variable BOOST with Auto Bypass)	0x01	0x01	0x00
TXLDO_VDDPA_HIGH (0x06)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)
TXLDO_VDDPA_MAX_RDR (0008h)	NA	NA	NA	NA	NA
BOOST_DEFAULT_VOLTAGE (000Ah)	0x1D (6 V).	NA	NA	NA	NA

Table 23. Supply voltage range

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independent from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
VBAT	2.8 V … 4.8 V	2.8 V … 4.8 V	2.4 V … 5.5 V	2.4 V … 5.5 V	2.4 V … 5.5 V
VBATPWR	2.8 V ... 4.8 V	2.8 V … 4.8 V	2.4 V … 5.5 V	2.4 V ... 5.5 V	2.4 V … 5.5 V
VUP	3.1 V … 6.0 V	2.8 V … < VBATPWR	2.4 V ... 5.5 V	2.4 V … 6.0 V	2.4 V … 5.5 V
VDDPA	VUP-0.3V drop of TX_LDO. max 5.7 V	VBATPWR - 0.5 V voltage drop	VUP-0.3V drop of TX_LDO	VUP-0.3V drop of TX_LDO	2.4 V … 5.5 V

9.9 Energy saving card detection

There is no trimming for the Low Frequency Timer required.

9.9.1 Low-power card detection (LPCD)

The low-power card detection (LPCD) is an energy-saving card polling configuration for the PN7642. During LPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required. The host microcontroller is woken up from power-saving mode by an IRQ send by the PN7642.

The LPCD mode offers highest sensitivity at the cost of slightly higher current consumption compared to the ULPCD mode.

A low frequency oscillator (there is no trimming for the low frequency oscillator required) is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short RF pulse. This RF pulse allows to detect a detuning of the antenna by presence of conductive objects in proximity of the antenna (card, cell phone, metal).

In case of a detected antenna detuning, the system wakes up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

A low frequency oscillator (LFO) is implemented to drive a wake-up counter, waking-up PN7642 from Standby mode. This allows implementation of low-power card detection polling loop at application level.

The host microcontroller can then perform a card polling sequence to verify if the technology of the object causing the antenna detuning is supported by the system.

The SWITCH_MODE instruction allows entering the LPCD mode with a given standby duration value.

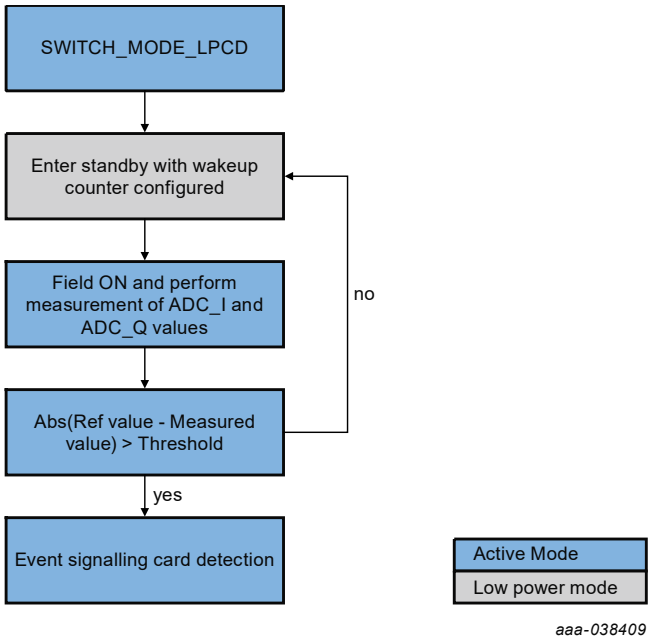


Figure 27. LPCD configuration

The LPCD mode is entered by the instruction SWITCH_MODE_LPCD, and terminated by toggling a GPIO, by a reset (VEN) of the PN7642 or a signal of the RF Level detector.

Before entering the LPCD mode, ADC_I and ADC_Q reference value needs to be determined. This is done during the so called calibration.

LPCD calibration phase

a) An initial calibration measurement is performed to set up the RX chain parameters namely HFATT, DCO_DAC_I_CTRL and DCO_DAC_Q_CTRL values.

b) The next measurement is done using the RX chain parameters that are set up, to arrive at the ADC_I and ADC_Q values which are used as reference values. All following LPCD measurements are done relative to the LPCD calibration measurement.

The LPCD loop itself works in two phases:

First the standby phase is controlled by the wake-up counter (timing defined in the instruction), which defines the duration of the standby of the PN7642.

Second phase is the detection-phase. The RF field is switched on for a defined time (EEPROM configuration) and then the ADC_I and ADC_Q values are compared to a reference value.

- If the ADC_I and ADC_Q values exceed the reference value, a LPCD_IRQ is raised to the host. The register configurations done by the host to support a dedicated RF protocol are not restored after wake-up command. The host has to configure the NFC frontend for a dedicated protocol operation to allow a polling for a card.
- If the ADC_I and ADC_Q values do not exceed the thresholds of the reference value, no LPC_IRQ is raised and the IC is set to the first phase (Standby mode) again.

These two phases are executed in a loop until:

- Card / metal is detected (LPCD_IRQ is raised).

- Reset occurs, which resets all the system configurations. The LPCD is also terminated in this case.

- NSS on host interface
- RF Level Detected
- GPIO toggle

The behavior of the generated field is different dependent on the activation state of the DPC function:

- If the DPC feature is not active, the ISO/IEC14443 type A 106 kbit/s settings are used during the sensing time.
- If the DPC is active, the RF_ON command is executed. The RF field is switched on as soon as the timer configured by the SWITCH_MODE command elapses. The RF field is switched on for a duration as defined for an activated DPC. The timer for the LPCD_FIELD_ON_TIME starts to count as soon as the RF_ON command terminates.

Table 24. Low-Power Card Detection: relevant EEPROM configuration

Name	Description
LPCD_AVG_SAMPLES	Defines how many samples of the I and Q values are used for the averaging. Used to optimize the system to achieve highest detection sensitivity versus false alarms.
LPCD_RSSI_TARGET	Value to be used as the RSSI target in the calibration phase to arrive at the RX chain parameters. This parameter is used to arrive at an optimal target voltage level at RXP.
LPCD_RSSI_HYST	Value to be used as the RSSI hysteresis in the calibration phase to arrive at the RX chain parameters. This is used to avoid oscillations while arriving at the target voltage level at RXP.
LPCD_THRESHOLD	If the difference between the measured value of I/Q and the reference value for I/Q is greater than the threshold on either channels, then a card is detected.
LPCD_VDDPA	VDDPA voltage when DC-DC (internal or external) or external power source is used to feed TXLDO
XTAL_CHECK_DELAY	Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18,8us). For fastest startup this time, a check is performed at a time slightly higher than the expected startup time of the crystal.

9.9.2 Semi-autonomous mode (LPCD)

LPCD semi-autonomous mode

The LPCD can be invoked by the host in the semi-autonomous mode wherein the ADC_I and ADC_Q values that are measured is returned back to the host.

In this mode, standby is not entered and the difference between the measured and reference values are not checked against the threshold. Nevertheless, the host may check the measured values against a reference and threshold to detect a card and also put the PN7642 in standby mode between measurements, using the SWITCH_MODE_STANDBY command.

This mode is especially useful to find optimized settings for the LPCD, since it does not offer no significant current saving.

9.9.3 Ultra low-power card detection (ULPCD)

The ULPCD (ultra low-power card detection) offers highest current saving. In this mode, the only wake-up sources to escape from the card detection loop are either a detected antenna detuning, a signal on GPIO3 or a reset (RESET_N) of the PN7642.

The ULPCD cannot be used together with the DC-DC function. A connection as described in the chapter "TX_LDO transmitter supply" or "Direct transmitter supply" is recommended.

Only the wake-up timer is active during ULP Standby state.

The ULPCD comprises 2 phases:

1. **Calibration phase**
   In this phase, an RF field is established and the field strength(RSSI) for the unloaded state of the antenna is measured to be used during the measurement phase and stored in a low-power persistent register.
2. **Measurement phase**
   In the measurement phase, the card detection activity is performed autonomously by the hardware at configurable time intervals. This configuration is passed as a parameter to the SWITCH_MODE_LPCD command. The RSSI value is measured and compared against the reference value measured in the calibration phase. A card is detected to be in the proximity of the reader when the measured RSSI differs from the reference RSSI by more than a configurable threshold.

The host can set the PN7642 into ultra-low power card detection state (ULP Standby state) via the instruction SWITCH_MODE_LPCD.

XTAL_CHECK_DELAY allows to optimize the startup of the crystal for the LPCD and ULPCD modes.

The following EEPROM configuration is available:

- ULPCD_VOLTAGE_CTRL
- ULPCD_RSSI_GUARD_TIME
- ULPCD_RSSI_SAMPLE_CFG
- ULPCD_THRESH_LVL
- ULPCD_GPIO3 - Allows to abort the ULPCD based on GPIO input.

9.10 External interfaces

The PN7642 requires the connection of a power supply, and a clock source like crystal or external clock.

Additional connections of the package require the connection of stabilizing capacitors and ground.

The RF interface connects transmitter and receiver to the EMC filter of a connected antenna matching network. Additional connections are available for the GPIO's and 2x DAC functionality (analog outputs).

The GPIO's implement internal Pull-up/Pull-down resistors. The output of the GPIO's can be configured in the pad configuration PAD_CONFIG.

9.11 Secure firmware update

The PN7642 supports a secure update of the implemented firmware.

The secure firmware download mode is using dedicated commands, but does not require a dedicated physical handling of the host interface lines.

The secure firmware download mode is entered by setting a register in non-volatile memory followed by a trigger of the VEN pin.

As an alternative, the firmware download mode can be activated by asserting the DWL_REQ pin as well.

The firmware binary file which is used to update the PN7642 is protected with an RSA signature and AES encryption.

The key length of the RSA is 2048 bits, the public exponent supports any 32-bit integer value.

A pre-computed Montgomery format of signature is used, and the signature hash computation is based on SHA256 algorithm.

This prevents a download of any other software which is not released by NXP.

The customer firmware of the user area has to be encrypted using the same cryptographic scheme as described above. The keys for signing and encryption can be provisioned and set by the customer.

To download unencrypted and unsigned firmware binary, the USB or SWD interfaces can be used.

An anti-tearing function is implemented in order to detect supply voltage removal or memory fault.

During the secure firmware download, the NFC operation is not available, only the command set defined for the secure firmware download is valid.

Updating the PN7642 with the default firmware binaries programs the memories for user configuration with default values. Any previous user configuration is overwritten. The user has to take care to restore the data of these memories after a secure firmware update.

If this is not intended, special firmware versions are available which do not overwrite the configuration. If the standard firmware file is named e.g. FW XX.YY, the name of the firmware which does not overwrite existing settings is then FW XX.FY. (The "F" is indicating the non-overwrite version)

The PN7642 checks if the new major version number is equal or higher than the current one. In case the major version number of the new firmware to be installed is smaller than the already installed version number of the firmware, the secure firmware update is rejected. Downgrading major firmware versions is therefore not possible. Upgrading and therefore increasing major firmware versions is always possible.

In case of any failure or exception during the download (e.g. caused by a communication error or power off), the PN7642 remains in the secure firmware download mode until a complete and valid NXP firmware is available in the device.

In case the firmware download of the user firmware was interrupted, but the NXP firmware is still valid, the device will boot into the application after a reset, except the DWL_REQ pin is still asserted.

Features of the automatic secure firmware update:

- Works without download request pin
- No special implementation of host interface handling
- Maximum integrity: Only encrypted and signed firmware images download possible via the secure firmware update functionality
- Updating the firmware overwrites existing all previous EEPROM configurations, unless a special version of the firmware was used.

9.12 Security Sub System

9.12.1 Asymmetric crypto unit

PN7642 provides an asymmetric cryptography coprocessor in order to support public-key cryptographic algorithms like RSA, ECC in finite prime and binary fields including Montgomery multiplication and reduction, plain and modular addition and subtraction. Additionally, this coprocessor can also be used to support other cryptographic operations like SHA, SM4, SEED, shift and rotate, logical functions (AND/OR/XOR), comparison and substitution.

All asymmetric cryptographic features are made available through a so called wrapper API based on mbedTLS library.

9.12.1.1 Features

- HKDF

- HMAC
- Elliptic Curve algorithms
  - ECKA
  - ECC key generation
  - ECDSA signing and verification
  - EdDSA signature generation and verification for Edward curve
  - Curves
    - Brainpool P256r1
    - Brainpool P384r1
    - SECP256
    - SECP384
    - Ed25519 signature generation and verification
    - Additional curves on Weierstrass and Prime are supported by feeding the specific domain parameters

9.12.2 Symmetric crypto unit

PN7642 implements a symmetric cryptography coprocessor that allows for fast execution of cryptographically strong en- and decryption based on the AES standard, and also supports fast hashing based on SHA256. Furthermore, it contains units for true and pseudo random number generation and secure key handling.

The symmetric crypto unit implements a separate protected communication channel into a special section in the FLASH memory where master keys, download keys, etc. are stored. This section is neither accessible for the CPU nor via any other AHB bus controller. This so-called Secure Key Transfer Unit manages the transfers between memory and crypto core, it automatically obfuscates the key material before physically writing it into the FLASH key store, generates a de-obfuscation mask upon reading from key store, and protects the communication channel between FLASH and crypto cores with transaction-specific masks.

All symmetric cryptographic features are made available through a so called wrapper API based on mbedTLS library.

9.12.2.1 Features

- Fast AES-128 or AES-256 en/decryption
- Support for chaining modes: CBC, CTR
- SHA256 coprocessor
- AES en/decryption via DMA
- SHA256 hashing via DMA
- Random number generator (RNG)
- Countermeasures against side channel information leakage
- Supported algorithms
  - AES-CCM
  - AES-CBC
  - AES-ECB
  - AES-CTR
  - AES-GCM (in software)
  - AES-GMAC
  - SHA-256

9.12.2.2 Random number generator

The random number generator (RNG) is a digital module composed of a pseudo random number generator (PRNG) and an APB registers bank for control and access to the pseudo random number material. To provide the complete random number generation functionality within PN7642, the RNG module is directly linked to the analog random number generator (ARNG), also called true random number generator (TRNG). The ARNG/TRNG is needed for loading a new seed into the PRNG at start-up and for increasing entropy of the system when generating random numbers while the PRNG is used to generate the final 32-bit random number.

Features

- Generates a 32-bit random number
- 32-bit APB target register interface

9.12.2.2.1 PRNG unit

The pseudo random number generator (PRNG) is used for the following purposes:

- Generating mask data for secure key transfer
- Generate mask and blinding bits for the symmetric crypto core

It is based on two cross coupled linear feedback shift registers.

9.12.2.2.2 TRNG unit

The analog true random number generator (TRNG) unit is used for:

- Generating high-quality random numbers for firmware use
- Generating a random bit stream towards the contactless interface

The TRNG is directly incorporated into the symmetric crypto unit.

9.12.3 Secure key store

The secure key store is a subsystem that secures key material stored in the flash memory and manages the access rights toward the CPU and cryptographic components.

Note: The device is provisioned with factory default transport keys. These transport keys are considered public information and it is strongly recommended to replace these keys by customer-specific secret keys. Information about how to replace the factory default transport key can be found in [2]. Refer to Table 4 to obtain the factory default keys for the specific product.

Features

- 1 APP_ROOT_KEY AES-128
- 1 APP_ROOT_KEY AES-256
- Up to 13 pcs of AES-128 bit keys OR up to 6 pcs AES-256 bit keys (APP_MASTER_KEYs)
- 11 pcs of AES-128 or AES-256 keys stored in extended key store (APP_FIXED_KEYs)
- 7 pcs of Asymmetric keys (APP_ASYMM_KEY) with any of the key curves (NIST SECP256R1 / NIST SECP384R1 / BP256R1 (Brainpool) / BP384R1 (Brainpool))

The secure key store component has its own AHB controller port that completely bypasses the CPU subsystem's firewall and AHB interconnect matrix. The 4 kB large "key store" can only be accessed via the key store unit but not by any other AHB controller because the firewall implements a special rule that does not allow any access.

The PN7642 key management system differentiates between the following key types:

1. NXP_TPT_KEY

These AES 128/256 bit keys are by default provisioned in the NXP factory in each of the IC and are published. These keys are referred as NXP Transport Keys. These keys are loaded onto the internal security IP, where in a key must be derived from these keys to perform the operations required. These keys are stored in secure key storage enclave, where the CPU will not have access.

2. APP_ROOT_KEY
   These AES 128/256 bit symmetric keys are provisioned by application in place of NXP_TPT_KEYs. These keys are the application root keys which can be provisioned as long as these are not locked out. The application can lock the APP_ROOT_KEYs from further provisioning once the application development is complete and ready to be roll-out to production. These keys are loaded onto the internal security IP, where in a key must be derived from these keys to perform the operations required. These keys are stored in secure key storage enclave, where in CPU will not access.
3. APP_MASTER_KEY
   The secure key storage enclave can store additional application keys. A mix of 128-bit and 256-bit keys can also be stored. These keys are derived from NXP_TPT_KEY/APP_ROOT_KEY. A key must be derived from these keys for further operations. These keys are stored in secure key storage enclave, where in CPU will not have access.
4. APP_FIXED_KEY
   To enhance the storage of fixed keys, PN7642 provides a way to store the AES 128/256 symmetric keys in a secure flash. Only the encrypted key data and wrapping key derivation message is stored in secure flash. These keys are stored in secure key storage extension enclave, where in keys are stored in encrypted format. These encrypted keys are loaded onto secure key IP, where in key can be used directly with the key properties for the operations. The CPU will not have access to the loaded keys in secure key IP.
5. APP_ASYMM_KEY
   Secure key store also supports storing of asymmetric keys with different key length and different key curve types. The asymmetric private keys are encrypted with a key derived from NXP_TPT_KEY/ APP_ROOT_KEY.

9.12.4 General-purpose CRC unit

A cyclic redundancy check (CRC) is a type of hash function used to produce a checksum for a block of data. The checksum is used to detect errors after transmission or storage. A CRC is computed and appended before transmission or storage and verified afterwards by recipient to confirm that no changes occurred on transit.

The general purposes CRC coprocessor is used to speed up these kinds of operations, since they are quite time consuming or require large lookup tables if emulated in software. The coprocessor is accessible by the CPU via the AHBtoAPB bridge. Control and data transfer is done via the corresponding APB registers.

9.12.4.1 Features

- Supports 16-bit CRC compliant to CRC-16-CCITT
- Supports 32-bit CRC compliant to IEEE 802.3
- Supports PRBS9 and PRBS15 modes (pseudo random bit stream mode)
- Configurable seed value
- Optional MSB or LSB first data processing
- BYTE, WORD or DWORD data input

9.12.4.2 Functional description

This block implements a configurable 16/32bit parallel CRC and serial PRBS9/15 coprocessor. The 16-bit CRC is compliant to X.25 (CRC-CCITT, ISO/IEC13239) standard with a polynomial generator of:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

The 32-bit CRC is compliant to the Ethernet / AAL5 (IEEE 802.3) standard with a polynome generator of:

$$g(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

Note: No final XORing or inversion is performed.

CRC calculation is done in parallel, meaning that the CRC computation for a complete 8/16/32 bit data input is performed within one clock cycle from the moment an input data is written.

For the PRBS9 (and PRBS15), the sequence is generated in a nine-stage (fifteen stage for PRBS15) shift register shared with the CRC16 shift register.

The PRBS9 generator polynome used in this block is:

$$g(x) = x^9 + x^5 + 1$$

The PRBS15 generator polynome used in this block is:

$$g(x) = x^{15} + x^{14} + 1$$

Note: No automatic clearing is performed on the shift registers implementing the aforementioned generator polynomials, if the CRC mode is changed. It is at the responsibility of the user to correctly initialize them after a mode change.

9.13 Firmware Partitioning

9.13.1 General

The PN7642 differentiates between two execution environments. The secure area and the Application area. Software that is executed in the secure area is running in the Arm Trust Zone environment. Most parts of the NXP firmware are running in this secure area.

In contrast, the user application is running entirely in the Application area. Every time a peripheral from the secure firmware needs to be accessed (e.g accessing the contactless interface or the security subsystem), a context switch from the Application area to the secure area needs to happen. In order to provide a controlled interface from the secure area to the Application area, the System Service API Layer is implemented into the NXP firmware. This API layer is the only possibility to exchange data between Application and secure execution environments.

9.13.2 System service API

The following figure illustrates the firmware architecture design and the separation between secure and application area of the PN7642.

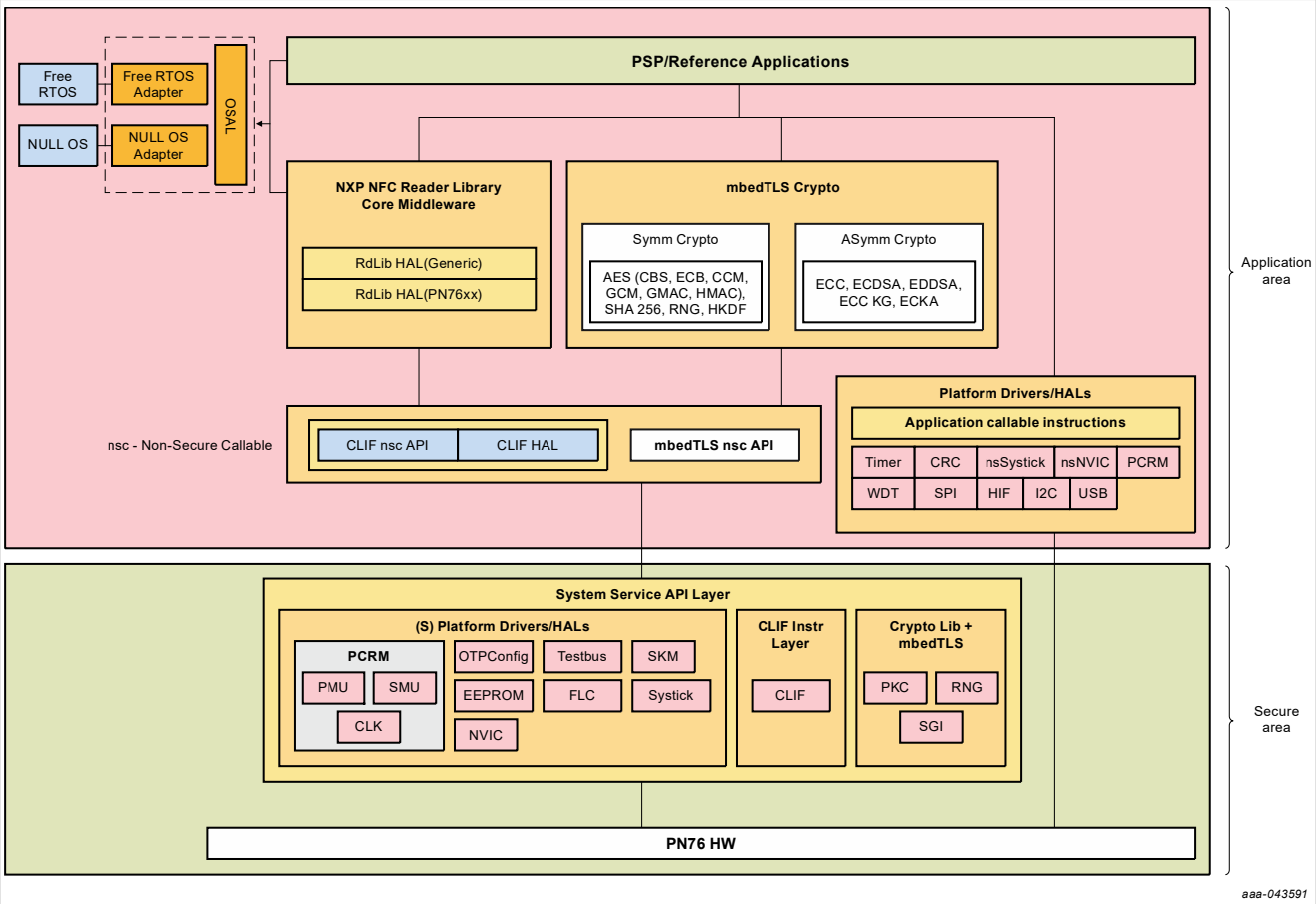


Figure 28. Firmware Architecture Design

The system service API is implemented as part of the NXP firmware within the secure area of the flash memory that is executed in secure execution environment. These APIs are callable from the application area.

The APIs can be broadly divided into following categories:

- In application programming API
- Lifecycle management API
- Boot/download configuration API
- CLIF HAL/instruction API
- PCRM HAL API
- Symmetric crypto wrapper API
- Asymmetric crypto wrapper API
- Secure Key Mode API
- Utility APIs

Note: A customer can call these APIs by a valid code executing from flash memory or RAM memory. Hence during initial boot, the configuration set by some of these APIs are default set and used by the boot and primary download function in ROM.

9.13.2.1 In application programming API

This API is used by a customer during upgrade of the customer developed firmware (also called secondary firmware). Since customer's secondary downloader executes in Flash memory, it cannot write(programmed) at the same time. Hence the programming of flash page is performed from ROM memory with the help of this API.

This API returns error if Code Write Protection is enabled in Secrow.

9.13.2.2 Lifecycle management API

There are 4 lifecycle parameters that can be used by customers at various stages of product development. They are:

1. USB-based download / Mass Storage disable: Customer can use this API to set this parameter to 1 and during subsequent boots, the ROM will not execute primary download function even if DWL_REQ pin is HIGH and USB VBUS is sensed.
2. Secrow Lock: The Secrow contains some lifecycle parameters such as SWD Access and Code Write Protection. Using this API, any further writes to Secrow is prevented permanently.
3. SWD Access Level: SWD Access can have 2 configurations:
   a. Customer enabled access used by customers to debug their flash code
   b. No Access enabling customers to deploy their product

   When the IC is delivered from production, the default SWD access will be "Customer enabled access". Customers can irreversibly change this to No Access before deploying in the field. When SECROW LOCK is set, SWD is changed to No Access.
4. Code Write Protection (CWP): Using this API, a customer can prevent any intentional/unintentional over writing of Flash memory at the hardware level. If CWP is enabled, USB primary download does not expose the flash memory as mass storage device.

9.13.2.3 Boot/download configuration API

Three configurations are required during boot and primary download.

1. USB Configuration: This API is used to set the USB descriptors used during primary download function. Eg: PID, VID, Manufacturer String, Product String, Self/Bus Powered and MaxPower. By default, the PID and VID are NXP assigned {0x1FC9, 0x0117}.
2. Primary Download Configuration: This API is used to set the Code Read Protection Levels and Data Read Protection Levels during USB Primary download function. Refer to Table 25.
3. PVDD Config: The customer can configure whether the boot should wait for external PVDD or turn on the internal PVDD LDO to generate the requisite PVDD. It also provides options to configure, how long the boot code should wait for PVDD to ramp up if external PVDD LDO is used (depending on the characteristic of external PVDD LDO). There are 2 timeouts (in steps of 100us and max of 200 ms).

Table 25. CRP Levels

CRP Level	CRP / DRP explanation
No CRP	The user flash can be read or written
CRP1	The user flash cannot be read, flash memory regions are updated depending on the new firmware/data image
CRP2	The user flash cannot be read, flash memory regions are entirely erased before copying new firmware/data
CRP3	The user flash cannot be read/written

9.13.2.4 Contactless interface HAL / instruction API

The contactless interface HAL / instruction API can be divided into the following categories:

1. Register manipulation API
2. User flash data manipulation API
3. Protocol configuration API
4. Transceiver abstraction API
5. RF ISR callback API

9.14 System settings and configuration

The configuration and behavior of the device is controlled at a central place.

EEPROM settings are a collection of all available configuration parameters that are needed for different operation modes. EEPROM settings serve as the source for the register settings.

The following two chapters list down the registers that are available to the user, as well as all available EEPROM configuration options.

9.14.1 Register description

The default setting of a bit within a register is indicated by the "*". Value indicates the allowed range for the bits of a symbol.

Note, that some registers change its content by the Firmware between an RF Exchange followed by an RF Reset command.

9.14.1.1 Register overview

Table 26. Register overview

Address (HEX)	Address (decimal)	Name
0h	0	SYSTEM_CONFIG
1h	1	EVENT_ENABLE
2h	2	EVENT_STATUS
3h	3	EMD_CONTROL
4h	4	FELICA_EMD_CONTROL
5h	5	RX_STATUS
6h	6	RX_STATUS_ERROR
7h	7	CLIF_STATUS
8h	8	TRANSCEIVE_CONTROL
9h	9	TX_SYMBOL01_MOD
Ah	10	TX_SYMBOL1_DEF
Bh	11	TX_SYMBOL0_DEF
Ch	12	TX_SYMBOL23_MOD
Dh	13	TX_SYMBOL23_DEF
Eh	14	TX_SYMBOL_CONFIG
Fh	15	TX_FRAME_CONFIG

Table 26. Register overview*...continued*

Address (HEX)	Address (decimal)	Name
10h	16	TX_DATA_MOD
11h	17	TX_WAIT
12h	18	TX_CRC_CONFIG
13h	19	RFU
14h	20	RFU
15h	21	SS_TX_CONFIG
16h	22	SS_TX1_RMCFG
17h	23	SS_TX2_RMCFG
18h	24	RFU
19h	25	SS_TX_TRANS_CFG
1A-1C	26-28	RFU
1D	29	SIGPRO_CONFIG
1E	30	RFU
1F	31	PUBLIC_RESERVED
20	32	SIGPRO_RM_PATTERN
21	33	PUBLIC RESERVED
22	34	RFU
23-24	35-36	PUBLIC RESERVED
25	37	RX_PROTOCOL_CONFIG
26	38	RX_FRAME_LENGTH
27	39	RFU
28	40	RX_CTRL_STATUS
29	41	PUBLIC RESERVED
2A	42	SIGPRO_IIR_CONFIG0
2B-2C	43-44	PUBLIC RESERVED
2Dh	45	DGRM_BBA
2E	46	PUBLIC RESERVED
2Fh	47	RFU
30h	48	DGRM_RSSI
31h	49	RX_CRC_CONFIG
32h	50	RX_WAIT
33	51	DCOC_CONFIG
34	52	RFU
35	53	RXM_CTRL
36	54	ANA_AGC_DCO_CTRL
37	55	RFU

Table 26. Register overview*...continued*

Address (HEX)	Address (decimal)	Name
38-3A	56-58	PUBLIC RESERVED
3B	59	SS_TX1_CMCFG
3C	60	SS_TX2_CMCFG
3Dh	61	TIMER0_CONFIG
3Eh	62	TIMER0_RELOAD
3Fh	63	RFU
40h	64	RFU
41	65	ANA_STATUS
42h	66	RFU
42	67	ANA_RX_CTRL
44	68	ANACTRL_TX_CONFIG
45-46	68-70	RFU
47h	71	EMD_1_CONFIG
48h	72	EMD_0_CONFIG
49-4F	73-79	RFU
50	80	LPCD_CALIBRATE_CTRL
51	81	IQ_CHANNEL_VALS
52	82	PAD_CONFIG
53	83	CALIBRATE_STATUS
54	84	TXLDO_VDDPA_CONFIG
55	85	GENERAL_ERROR_STATUS
56	86	TXLDO_VOUT_CURR
57	87	DAC
58	88	PMU_ANA_SMPS_CTRL_REG
59	89	RXM_FREQ
5A	90	RXM_RSSI
5B	91	TEMP_SENSOR
5D	93	TX_NOV_CALIBRATE_AND_STORE
5E	94	DPC_CONFIFG
5F	95	TIMER0_OUTPUT (from FW 2.05 onwards)
60	96	TIMER1_OUTPUT (from FW 2.05 onwards)
61	97	TIMER2_CONFIG (from FW 2.05 onwards)
62	98	TIMER2_RELOAD (from FW 2.05 onwards)
63	99	TIMER2_OUTPUT (from FW 2.05 onwards)
80	128	SS_TX1_RTRANS0
81	129	SS_TX1_RTRANS1

Table 26. Register overview*...continued*

Address (HEX)	Address (decimal)	Name
82	130	SS_TX1_RTRANS2
83	131	SS_TX1_RTRANS3
84	132	SS_TX1_RTRANS4
85	133	SS_TX1_RTRANS5
86	134	SS_TX1_RTRANS6
87	135	SS_TX1_RTRANS7
88	136	SS_TX1_RTRANS8
89	137	SS_TX1_RTRANS9
8A	138	SS_TX1_RTRANS10
8B	139	SS_TX1_RTRANS11
8C	140	SS_TX1_RTRANS12
8D	141	SS_TX1_RTRANS13
8E	142	SS_TX1_RTRANS14
8F	143	SS_TX1_RTRANS15

9.14.1.2 SYSTEM_CONFIG (0000h)

Table 27. SYSTEM_CONFIG register (address 0000h) bit description

Bit	Symbol	Access	Value	Description
31:9	RFU	r/w	0*,1	-
8	TX_NOV_CALIBRATION	r/w	0*,1	One time calibration when the host writes a 1 into this register, a one time calibration is performed. ***Note:*** The calibration is resulting a short RF-on. All the power configurations shall the configured before setting this bit.
7	RFU	r/w	0	-
6:5	15693_CHANGE_DATARATE	r/w	0*,1	15693_changedatarate 0 - RFU 1 - Change data rate to 53kB/sec 2 - Change data rate to 106kB/sec 3 - Change data rate to 212kB/sec By default, the basic data rate of 26kB/sec is loaded, switching to a different higher data rate requires this config register to be updated. All relevant related registers are updated automatically.
4	up to FW 2.03: RFU	r/w	0*,1	-
	from FW 2.05 onwards: FAST_FIELD_ON	r/w	0*,1	0 - Field ON Duration includes time interval to start TXLDO and DC-DC as part of RF ON

Table 27. SYSTEM_CONFIG register (address 0000h) bit description*...continued*

Bit	Symbol	Access	Value	Description
				1 - Field ON Duration is reduced as TXLDO and DC-DC remains ON and only TX Driver is Enabled/ Disabled as part of RF ON
3	AUTOCOLL STATE A	r/w	0*,1	0: TypeA Card mode: Autocoll entry with IDLE state of the card 1: TypeA Card mode: Autocoll entry with HALT state of the card
2	SOFT RESET	r/w	0*,1	Performs a soft reset of the system, all registers are set to default values
1	MF CRYPTO ON	r/w	0*,1	If set to 1 the MIFARE - crypto bit is generated for MIFARE Classic en-/de-cryption
0	RFU	r/w	0*,1	-

9.14.1.3 EVENT_ENABLE (0001h)

Table 28. EVENT_ENABLE register (address 0001h) bit description

Bit	Symbol	Access	Value	Description
31:8	RFU	r	0*,1	-
11	CTS_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
10	IDLE_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
9	LP_CALIBRATION_EVENT_ ENABLE	r/w	0*,1	Enable the corresponding event
8	LPCD_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
7	AUTOCOLL_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
6	TIMER0_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
5	TX_OVERCURRENT_ERROR_ EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
4	RFON_DET_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
3	RFOFF_DET_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
2	STANDBY_PREV_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
1	GENERAL_ERROR_EVENT_ ENABLE	r/w	0*,1	Enable the corresponding event
0	BOOT_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event

9.14.1.4 EVENT_STATUS (0002h)

Table 29. EVENT_STATUS register (address 0002h) bit description

Bit	Symbol	Access	Value	Description
31:12	RFU	r	0*,1	-
11	CTS_EVENT	r	0*,1	Indicated the availability of CTS Event
10	IDLE_EVENT	r	0*,1	Indicated the availability of IDLE event.
9	LP_CALIBRATION_EVENT	r	0*,1	Indicated the availability of LP Calibration event

Table 29. EVENT_STATUS register (address 0002h) bit description*...continued*

Bit	Symbol	Access	Value	Description
8	LPCD_EVENT	r	0*,1	Indicated the availability of LPCD event.
7	AUTOCOLL_EVENT	r	0*,1	Indicated the availability of Autocoll event
6	TIMER0_EVENT	r	0*,1	Indicated the availability of Timer0 event
5	TX_OVERCURRENT_ERROR_EVENT	r	0*,1	Indicated the availability of transmitter over current error. This bit is set, when the current on the TX driver is higher than the defined threshold in the EEPROM. Upon this condition, the field is automatically switched OFF before the notification to the host.
4	RFON_DET_EVENT	r	0*,1	Indicated the availability of RF ON detected.
3	RFOFF_DET_EVENT	r	0*,1	Indication of external RF OFF detected
2	STANDBY_PREV_EVENT	r	0*,1	Indicated the availability of Standby Prevention reason.
1	GENERAL_ERROR_EVENT	r	0*,1	Indicated the availability of General Error event.
0	BOOT_EVENT	r	0*,1	Indicated the availability of Boot event.

9.14.1.5 EMD_CONTROL (0003h)

To activate the EMVCo EMD handling of the PN7642, the following bits of the register need to be set as follows:

0001b: EMD_ENABLE

1b: EMD_TRANSMISSION_ERROR_ABOVE_NOISE_THRESHOLD_IS_NO_EMD

0001b: EMD_NOISE_BYTES_THRESHOLD

Table 30. EMD_CONTROL register (address 0003h) bit description

Bit	Symbol	Access	Value	Description
31:12	RFU	rw	0*,1	-
11:10	EMD_RM_EMD_SENSITIVITY	rw	0*,1	RM EMD SENSITIVITY value that will be applied to SIGPRO_RM_CONFIG, At layer 4, when EMD is enabled, the value of EMD_RM_SENSITIVITY can be lowered to ensure robust EMD suppression, if during the layer 3 activation, the value of EMD_RM_SENSITIVITY in the protocol area is set to a high value to ensure collision detection and resolution when multiple typeA cards are presented at close distance to the antenna.
9:8	EMD_TRANSMISSION_TIMER_USED	rw	0*,1	Timer used for RF communication.
7	EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_B	rw	0*,1	Missing CRC treated as protocol error in » case of Type B based communication P » case of Type B based communication
6	EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_A	rw	0*,1	Missing CRC treated as protocol error in » case of Type A based communication P » case of Type A based communication

Table 30. EMD_CONTROL register (address 0003h) bit description*...continued*

Bit	Symbol	Access	Value	Description
5:2	EMD_NOISE_BYTES_THRESHOLD	rw	0*,1	Defines the threshold under which transmission errors are treated as noise. Note: CRC bytes are NOT included/counted!
1	EMD_TRANSMISSION_ERROR_ABOVE_NOISE_THRESHOLD_IS_NO_EMD	rw	0*,1	Transmission errors with received byte length >= EMD_NOISE_BYTES_THRESHOLD is never treated as EMD (can be used for versions below EMVCo3.0)
0	EMD_ENABLE	rw	0*,1	EMD handling enabled If this register is enabled by setting EMVCO_EMD_ENABLE=1, the registers EMD_0_CONFIG and EMD_1_CONFIG is ignored for the EMVCO_EMD function.

9.14.1.6 FELICA_EMD_CONTROL (0004h)

Table 31. FELICA_EMD_CONTROL register (address 0004h) bit description

Bit	Symbol	Access	setting for FeliCa EMD handlir	Value	Description
31:24	FELICA_EMD_RC_BYTE_VALUE	rw	0	0*,1	FeliCa RC byte value that needs to be received does not treat the frame as EMD
23:16	FELICA_EMD_LENGTH_BYTE_MAX	rw	0	0*,1	Maximum Length byte value that needs to be received does not treat the frame as EMD
15:8	FELICA_EMD_LENGTH_BYTE_MIN	rw	0	0*,1	Minimum Length byte value that needs to be received does not treat the frame as EMD
7:5	RESERVED	rw	0	0*,1	-
6	FELICA_EMD_LOG_ENABLE	rw	0 or 1	0*1	Log Enable bit to send RX Status during EMD
5	FELICA_EMD_RC_CHECK_ON_CRC_CORRECT_ENABLE	rw	0 or 1	0*1	RC byte check enabled for FeliCa EMD handling on complete RF Frame when there is no Integrity Error observed
4	FELICA_EMD_INTEGRITY_ERR_CHECK_ENABLE	rw	1	0*,1	FeliCa EMD handling enabled when integrity error is set
3	FELICA_EMD_PROTOCOL_ERR_CHECK_ENABLE	rw	1	0*,1	FeliCa EMD handling enabled when protocol error is set
2	FELICA_EMD_RC_CHECK_ENABLE	rw	0	0*,1	FeliCa RC byte check enabled for FeliCa EMD handling
1	FELICA_EMD_LEN_CHECK_ENABLE	rw	0	0*,1	FeliCa Length byte check enabled for FeliCa EMD handling
0	FELICA_EMD_ENABLE	rw	1	0*,1	FeliCa EMD handling enabled

Recommended value for FeliCa EMD handling: 00FF0019h

9.14.1.7 RX_STATUS (0005h)

Table 32. RX_STATUS register (address 0005h) bit description

Bit	Symbol	Access	Value	Description
31:27	RFU	r	0*,1	-
26:20	RX_COLL_POS	r	0*,1	Status indicating the bit position of the first collision detected in the data bit. The value is valid only when RX_COLLISION_DETECTED==1. The value of the RX_BIT_ALIGN is also taken into account (RX_ COLL_POS = physical bit position in the flow + RX_ BIT_ALIGN value). Indicates the collision position in the first 8 bytes only. Can be used during the TypeA/ICODE/EPC anti-collision procedure.0x00 - first bit 0x01 - second bit... 0x7F - 128th bit. The status register is not updated by the collision detected on stop or parity bit.
19:17	RX_NUM_LAST_BITS	r	0*,1	Indicating the number of valid bits in the last byte received. 0: all bits are valid 1: 1 bit is valid …. 7: - 7 bits are valid This is generally used during ISO/IEC14443 type A anti-collision
16:13	RX_NUM_FRAMES_RECEIVED	r	0*,1	Indicates the number of frames received. The value is updated after every normal frame reception in RX_ MULTIPLE mode. The value is valid only if the bit RX_MULTIPLE_ ENABLE==’1’.
12:0	RX_NUM_BYTES_RECEIVED	r	0*,1	Number of bytes received on the RF interface. This field is not relevant when RX_MULTIPLE_ ENABLE=='1'.

9.14.1.8 RX_STATUS_ERROR (0006h)

Table 33. RX_STATUS_ERROR register (address 0006h) bit description

Bit	Symbol	Access	Value	Description
31:30	RFU	r	0*,1	
29	EMD_DETECTED_IN_RXDEC	r	0*,1	The high level indicates that the EMD was detected (in the SigPro or in the RxDecoder or in both) during the reception.
28	EMD_DETECTED_IN_SIGPRO	r	0*,1	The high level indicates that the EMD was detected on the Physical layer (in the SigPro) during the reception.
27	EXT_RFOFF_DETECTED	r	0*,1	The high level indicates that the external RF-field vanished during the reception
26	RX_FRAME_MAXLEN_VIOL	r	0*,1	The high level indicates that the received frame length violated the configured maximum limit

Table 33. RX_STATUS_ERROR register (address 0006h) bit description*...continued*

Bit	Symbol	Access	Value	Description
25	RX_FRAME_MINLEN_VIOL	r	0*,1	The high level indicates that the received frame length violated the configured minimum limit.
24	RX_FRAME_LE_CRC	r	0*,1	The high level indicates that the received frame length is less or equal to the expected CRC field length.
23	RX_NOT_FULL_BYTE	r	0*,1	The high level indicates that the last received character in the frame has less than 8 bits.
22	RX_MISSING_PARBIT_ DETECTED	r	0*,1	The high level indicates that the last received character in the frame has 8 data bits but the expected parity bit is absent.
21	RX_MISSING_STOPBIT_ DETECTED	r	0*,1	The high level indicates that the last received character in the frame has 8 data bits but the expected stop bit is absent.
20	RX_COLLISION_PARBIT_ DETECTED	r	0*,1	The high level indicates that the collision was detected on the parity bit position.
19	RX_COLLISION_STOPBIT_ DETECTED	r	0*,1	The high level indicates that the collision was detected on the stop bit position.
18	RX_COLLISION_DETECTED	r	0*,1	The high level indicates that the collision was detected during the frame reception.
17	RX_STOP_ON_RXOVER	r	0*,1	The high level indicates that the frame reception was stopped by SGP_MSG_RXOVER_* message reception.
16	RX_STOP_ON_RFOFF	r	0*,1	The high level indicates that the frame reception was interrupted by external RF-field vanishing event.
15	RX_STOP_ON_ERR	r	0*,1	The high level indicates that the frame reception was stopped by detected communication error event.
14	RX_STOP_ON_LEN	r	0*,1	The high level indicates that the frame reception was normally stopped by byte counter expiration event. Relates to the protocols where the LEN field is used in the frame format (FeliCa RM/CM, FWEC RM/CM).
13	RX_STOP_ON_INVPAR	r	0*,1	The high level indicates that the frame reception was normally stopped by the inverted parity detection event. Relates to the TypeA RM 212-848 kbit/s modes.
12	RX_STOP_ON_PATTERN	r	0*,1	The high level indicates that the frame reception was normally stopped by EOF pattern detection event. Relates to the TypeB RM/CM, B prime RM/ CM modes.
11	RX_STOP_ON_ANTICOLL	r	0*,1	The high level indicates that the frame reception was normally stopped by collision detected on data bit position. Relates to the bit-oriented frame reception in TypeA RM 106 kbit/s mode during the anti-collision procedure.
10	RX_CRC_ERROR	r	0*,1	The high level indicates that the CRC error is detected in the received frame.

Table 33. RX_STATUS_ERROR register (address 0006h) bit description*...continued*

Bit	Symbol	Access	Value	Description
9	RX_LEN_ERROR	r	0*,1	The high level is set if the received frame is shorter than the length stated in the received frame LEN field OR if the LEN parameter in the received frame violates the configured [RX_FRAME_MINLEN:RX_FRAME_MAX LEN] limits. Can assert only in the mode where the LEN field is used in the frame format (FeliCa RM/CM, FWEC RM/CM).
8	RX_SIGPRO_ERROR	r	0*,1	The high level indicates that the communication error/errors were detected during the frame reception on physical layer(in the SigPro).
7	RX_PARITY_ERROR	r	0*,1	The high level indicates that the parity error was detected during the frame reception.
6	RX_STOPBIT_ERROR	r	0*,1	The high level indicates that the stop bit error (‘0’ level instead of ‘1’ on the stop bit position) was detected during the frame reception.
5	RX_WRITE_ERROR	r	0*,1	The high level indicates that the error acknowledge status was received on the CLIF-system interface during the received frame transmission to the System RAM.
4	RX_BUFFER_OVFL_ERROR	r	0*,1	The high level indicates that the data payload length in the received frame exceeds the 28 bytes limit. Relates to the PollReq procedure in the FeliCa RM mode only.
3	RX_LATENCY_ERROR	r	0*,1	The high level indicates that the write request flow was corrupted due to traffic congestion on the system interface during the received frame transmission to the System RAM.
2	RX_DATA_INTEGRITY_ERROR	r	0*,1	The high level indicates that the data integrity corruption (parity/CRC/etc error) was detected in the received frame.
1	RX_PROTOCOL_ERROR	r	0*,1	The high level indicates that the protocol requirements violation (stop bit error, missing parity bit, not full byte received, etc.) was detected in the received frame.
0	RX_CL_ERROR	r	0*,1	The high level indicates that some protocol/data integrity erorr/errors were detected during the frame reception

9.14.1.9 CLIF_STATUS (0007h)

Table 34. CLIF_STATUS register (address 0007h) bit description

Bit	Symbol	Access	Value	Description
31:30	RFU	r	0*,1	-
29	CRC_OK	r	0*,1	This bit indicates the status of the actual CRC calculation. If 1 the CRC is correct. meaning the CRC register has the value 0 or the residue value if inverted CRC is used. Note: This flag should only be evaluated at the end of a communication

Table 34. CLIF_STATUS register (address 0007h) bit description*...continued*

Bit	Symbol	Access	Value	Description
28	RX_SC_DETECTED	r	0*,1	Status signal indicating that a subcarrier is detected.
27	RX_SOF_DETECTED	r	0*,1	Status signal indicating that a SOF has been detected.
26	TX_RF_STATUS	r	0*,1	If set to 1 this bit indicates that the drivers are turned on. meaning an RF-Field is created by the device itself.
25	RF_DET_STATUS	r	0*,1	If set to 1 this bit indicates that an external RF-Field is detected by the RF level detectors (after digital filtering)
24	ADC_Q_CLIPPING	r	0*,1	Indicates that the Q-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver).
23	ADC_I_CLIPPING	r	0*,1	Indicates that the I-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver).
22:12	RFU	r	0*,1	-
11	TX_NO_DATA_ERROR	r	0*,1	This error flag is set to 1. in case a transmission is started but no data is available (register NumBytes ToSend == 0).
10:8	RF_ACTIVE_ERROR_CAUSE	r	0*,1	This status flag indicates the cause of an NFC-Active error. Note: These bits are only valid when the RF_ACTIVE_ERROR_IRQ is raised and will be cleared as soon as the bit TX_RF_ENABLE is set to 1. 0* No Error. reset value 1 External field was detected on within TIDT timing 2 External field was detected on within TADT timing 3 No external field was detected within TADT timings 4 Peer did switch off RF Field without but no RX event was raised (no data received) 5 - 7 Reserved.
7:6	RFU	r	0*,1	-
5	RX_ENABLE	r	0*,1	This bit indicates if the RxDecoder is enabled. If 1 the RxDecoder was enabled and is now ready for data reception
4	TX_ACTIVE	r	0*,1	This bit indicates activity of the TxEncoder. If 1 a transmission is ongoing otherwise the TxEncoder is in idle state.
3	RX_ACTIVE	r	0*,1	This bit indicates activity of the RxDecoder. If 1 a data reception is ongoing. otherwise the RxDecoder is in idle state.
2:0	RF_EXCHANGE_STATE	r	0*,1	These registers hold the command bits 0* IDLE state 1 WaitTransmit state 2 Transmitting state 3 WaitReceive state 4 WaitForData state 5 Receiving state 6 LoopBack state

Table 34. CLIF_STATUS register (address 0007h) bit description*...continued*

Bit	Symbol	Access	Value	Description
				7 reserved

9.14.1.10 RF_EXCHANGE_CONTROL (0008h)

To meet the ISO14443A FDT with an accuracy of 1 carrier clock cycle, there is support implemented to synchronize the guard time pre-scaler to the modified Miller envelope pulses (end of pulse). For adjustment, there is a 7-bit wide configuration register - TX_BITPHASE - which is allows to adjust the FDT in the range of 0 to 128 carrier clock cycles. As defined in the ISO14443 the adjustment is different, depending on the data bit value of the data stream. For correct bit grid calculation, the pre-scaler must be set to a value corresponding exactly to one etu - for 106 kbit/s this corresponds to 0x7F. Otherwise the FdT will be incorrect.

Table 35. RF_EXCHANGE_CONTROL register (address 0008h) bit description

Bit	Symbol	Access	Value	Description
31:16	RFU	r	0*,1	-
15:8	TX_BITPHASE	r/w	0*,1	Defines the number of 13.56 MHz cycles used for adjustment of TX_WAIT to meet the FDT. This is applicable for CardMode only.
7:3	RFU	r/w	0*,1	-
2	RX_MULTIPLE_ENABLE	r/w	0*,1	If this bit is set to 1. the receiver is reactivated after the end of a reception.
1:0	RFU	r/w	0*,1	-

9.14.1.11 TX_SYMBOL01_MOD (0009h)

Table 36. TX_SYMBOL01_MOD register (address 0009h) bit description

Bit	Symbol	Access	Value	Description
31:24	RFU	rw	0*,1	-
23:16	TX_S01_MODWIDTH	rw	0*,1	Specifies the length of a pulse for sending data of symbol 0/1. The length is given by the number of carrier clocks + 1.
15:9	RFU	rw	0*,1	-
8	TX_S01_MILLER_ENABLE	rw	0*,1	If set to 1. pulse modulation is applied according to modified miller coding.
7	TX_S01_INV_ENV	rw	0*,1	If set to 1. the output envelope is inverted.
6:4	TX_S01_ENV_TYPE	rw	0*,1	Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b Direct output 001b Manchester code 010b Manchester code with subcarrier 011b BPSK 100b RZ (pulse of half bit length at beginning of second half of bit) 101b RZ (pulse of half bit length at beginning of bit) 110b Manchester tupple 111b RFU.
3	TX_S01_SC_FREQ	rw	0*,1	Specifies the frequency of the subcarrier. 0 424 kHz 1 848 kHz
2:0	TX_S01_BIT_FREQ	rw	0*,1	Specifies the frequency of the bit-stream. 000b -> 1.695 MHz.

Table 36. TX_SYMBOL01_MOD register (address 0009h) bit description*...continued*

Bit	Symbol	Access	Value	Description
				001b -> Reserved. 010b -> 26 kHz. 011b -> 53 kHz. 100b -> 106 kHz. 101b -> 212 kHz. 110b -> 424 kHz. 111b -> 848 kHz.

9.14.1.12 TX_SYMBOL1_DEF (000Ah)

Table 37. TX_SYMBOL1_DEF register (address 000Ah) bit description

Bit	Symbol	Access	Value	Description
31:0	TX_SYMBOL1_DEF	rw	0*,1	Pattern definition for Symbol1

9.14.1.13 TX_SYMBOL0_DEF (000Bh)

Table 38. TX_SYMBOL0_DEF register (address 000Bh) bit description

Bit	Symbol	Access	Value	Description
31:0	TX_SYMBOL0_DEF	rw	0*,1	Pattern definition for Symbol0

9.14.1.14 TX_SYMBOL23_MOD (000Ch)

Table 39. TX_SYMBOL23_MOD register (address 000Ch) bit description

Bit	Symbol	Access	Value	Description
31:24	RFU	r	0*,1	-
23:16	TX_S23_MODWIDTH	r/w	0*,1	Specifies the length of a pulse for sending data of symbol 2/3. The length is given by the number of carrier clocks + 1.
15:9	RFU	r/w	0*,1	-
8	TX_S23_MILLER_ENABLE	r/w	0*,1	If set to 1 pulse modulation is applied according to modified miller coding
7	TX_S23_INV_ENV	r/w	0*,1	If set to 1 the output envelope is inverted.
6:4	TX_S23_ENV_TYPE	r/w	0*,1	Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b Direct output 001b Manchester code 010b Manchester code with subcarrier 011b BPSK 100b RZ (pulse of half bit length at beginning of second half of bit) 101b RZ (pulse of half bit length at beginning of bit) 110b Manchester tupple 111b RFU
3	TX_S23_SC_FREQ	r/w	0*,1	Specifies the frequency of the subcarrier. 0 424 kHz 1 848 kHz
2:0	TX_S23_BIT_FREQ	r/w	0*,1	Specifies the frequency of the bit-stream. 000b -> 1.695 MHz. 001b -> Reserved. 010b -> 26 kHz. 011b -> 53 kHz. 100b -> 106 kHz. 101b -> 212 kHz. 110b -> 424 kHz. 111b -> 848 kHz.

9.14.1.15 TX_SYMBOL23_DEF (000Dh)

Table 40. TX_SYMBOL23_DEF register (address 000Dh) bit description

Bit	Symbol	Access	Value	Description
31:24	RFU	r	0*,1	-
23:16	TX_SYMBOL3_DEF	r/w	0*,1	Pattern definition for Symbol3
15:8	RFU	r/w	0*,1	-
7:0	TX_SYMBOL2_DEF	r/w	00000h* - FFFFFh	Pattern definition for Symbol2

9.14.1.16 TX_SYMBOL_CONFIG (000Eh)

Table 41. TX_SYMBOL_CONFIG register (address 000Eh) bit description

Bit	Symbol	Access	Value	Description
31	RFU		0*,1	-
30:27	TX_SYMBOL1_BURST_LEN	r/w	00000h* - FFFFFh	Specifies the number of bits issued for symbol 1 burst. The 3 bits encode a range from 8 to 256 bit length: 0000b 8 bit 0001b 12 bit 0010b 16 bit 0011b 24 bit 0100b 32 bit 0101b 40 bit 0110b 48 bit 0111b 64 bit 1000b 80 bit 1001b 96 bit 1010b 112 bit 1011b 128 bit 1100b 160 bit 1101b 192 bit 1110b 224 bit 1111b 256 bit
26	TX_SYMBOL1_BURST_TYPE	r/w	0*,1	Specifies the type of the burst of Symbol1 (logical zero / logical one)
25	TX_SYMBOL1_BURST_ONLY	r/w	0*,1	If set to 1. Symbol1 consists only of a burst and no symbol pattern
24	TX_SYMBOL1_BURST_ ENABLE	r/w	0*,1	If set to 1. the burst of Symbol0 of the length defined in bit field SYMBOL1_BURST_LEN is enabled
23	RFU	r	0*,1	-
22:19	TX_SYMBOL0_BURST_LEN	r/w	0*,1	Specifies the number of bits issued for symbol 0 burst. The 3 bits encode a range from 8 to 256 bit length: 0000b 8 bit 0001b 12 bit 0010b 16 bit 0011b 24 bit 0100b 32 bit 0101b 40 bit 0110b 48 bit 0111b 64 bit 1000b 80 bit 1001b 96 bit 1010b 112 bit 1011b 128 bit 1100b 160 bit 1101b 192 bit 1110b 224 bit 1111b 256 bit
18	TX_SYMBOL0_BURST_TYPE	r/w	0*,1	Specifies the type of the burst of Symbol0 (logical zero / logical one)
17	TX_SYMBOL0_BURST_ONLY	r/w	0*,1	If set to 1. Symbol0 consists only of a burst and no symbol pattern
16	TX_SYMBOL0_BURST_ ENABLE	r/w	0*,1	If set to 1. the burst of Symbol0 of the length defined in bit field SYMBOL0_BURST_LEN is enabled
15:13	TX_SYMBOL3_LEN	r/w	0*,1	Specifies the number of valid bits of the symbol definition of Symbol3. The range is from 1 bit (value 0000) to 8 bit (value 111)
12:10	TX_SYMBOL2_LEN	r/w	0*,1	Specifies the number of valid bits of the symbol definition of Symbol2. The range is from 1 bit (value 0000) to 8 bit (value 111)

Table 41. TX_SYMBOL_CONFIG register (address 000Eh) bit description*...continued*

Bit	Symbol	Access	Value	Description
9:5	TX_SYMBOL1_LEN	r/w	0*,1	Specifies the number of valid bits of the symbol definition of Symbol1. The range is from 1 bit (value 0000) to 31 bits (value 11110)
4:0	TX_SYMBOL0_LEN	r/w	0*,1	Specifies the number of valid bits of the symbol definition of Symbol0. The range is from 1 bit (value 0000) to 31 bits (value 11110)

9.14.1.17 TX_FRAME_CONFIG (000Fh)

Table 42. TX_FRAME_CONFIG register (address 000Fh) bit description

Bit	Symbol	Access	Value	Description
31:19	RFU	r	0*,1	-
18:16	TX_DATA_CODE_TYPE	r/w	0*,1	Specifies the type of encoding of data to be used 000b No special code 001b 1 out of 4 code [ICODE SLI] 010b 1 out of 256 code [ICODE SLI] 011b Pulse interval encoding (PIE) [ICODE EPC-V2] 100b 2bit tupple code (intended only for test purpose) 101-111b Reserved
15:13	TX_STOPBIT_TYPE	r/w	0*,1	Enables the stop bit (logic 1) and extra guard time (logic 1). The value 0 disables transmission of stop-bits. 000b no stop-bit. no EGT 001b stop-bit. no EGT 010b stop-bit + 1 EGT 011b stop-bit + 2 EGT 100b stop-bit + 3 EGT 101b stop-bit + 4 EGT 110b stop-bit + 5 EGT 111b stop-bit + 6 EGT
12	TX_STARTBIT_ENABLE	r/w	0*,1	If set to 1. a start-bit (logic 0) will be sent
11	TX_MSB_FIRST	r/w	0*,1	If set to 1. data bytes are interpreted MSB first for data transmission
10	TX_PARITY_LAST_INV_ ENABLE	r/w	0*,1	If set to 1. the parity bit of last sent data byte is inverted
9	TX_PARITY_TYPE	r/w	0*,1	Defines the type of the parity bit 0 Even Parity is calculated 1 Odd parity is calculated
8	TX_PARITY_ENABLE	r/w	0*,1	If set to 1. a parity bit is calculated and appended to each byte transmitted. If the Transmission Of Data Is Enabled and TX_NUM_BYTES_2_SEND is zero. then a NO_DATA_ERROR occurs.
7:5	RFU	r	0*,1	-
4	TX_DATA_ENABLE	r/w	0*,1	If set to 1. transmission of data is enabled otherwise only symbols are transmitted.
3:2	TX_STOP_SYMBOL	r/w	0*,1	Defines which pattern symbol is sent as frame stop-symbol 00b No symbol is sent 01b Symbol1 is sent 10b Symbol2 is sent 11b Symbol3 is sent
1:0	TX_START_SYMBOL	r/w	0*,1	Defines which symbol pattern is sent as frame start-symbol 00b No symbol pattern is sent 01b Symbol0 is sent 10b Symbol1 is sent 11b Symbol2 is sent

9.14.1.18 TX_DATA_MOD (0010h)

Table 43. TX_DATA_MOD register (address 0010h) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	r	0*,1	-
24	TX_ICODE_DATA_MODWIDTH_ENABLE	r/w	0*,1	Enables modulation width of icode data. Width of modulation is defined by the TX_DATA_MODWIDTH field. When 1, we should have TX_DATA_ENV_TYPE=0 and TX_DATA_INV_ENV=0
23:16	TX_DATA_MODWIDTH	r/w	0*,1	Specifies the length of a pulse for sending data with miller pulse modulation enabled. The length is given by the number of carrier clocks + 1.
15:9	RFU	r	0*,1	-
8	TX_DATA_MILLER_ENABLE	r/w	0*,1	If set to 1 pulse modulation is applied according to modified miller coding
7	TX_DATA_INV_ENV	r/w	0*,1	If set to 1 the output envelope is inverted
6:4	TX_DATA_ENV_TYPE	r/w	0*,1	Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b Direct output 001b Manchester code 010b Manchester code with subcarrier 011b BPSK 100b RZ (pulse of half bit length at beginning of second half of bit) 101b RZ (pulse of half bit length at beginning of bit) 110b Manchester tupple coding 111b RFU
3	TX_DATA_SC_FREQ	r/w	0*,1	Specifies the frequency of the subcarrier. 0 424 kHz 1 848 kHz
2:0	TX_DATA_BIT_FREQ	r/w	0*,1	Specifies the frequency of the bit-stream. 000b -> 1.695 MHz. 001b -> Reserved. 010b -> 26 kHz. 011b -> 53 kHz. 100b -> 106 kHz. 101b -> 212 kHz. 110b -> 424 kHz. 111b -> 848 kHz.

9.14.1.19 TX_WAIT (0011h)

To guarantee correct protocol timing a guard period timer is implemented for the RF_EXCHANGE command in reception and transmission mode.

These guard times are not available for Transmit or Receive command.

The guard time TX_WAIT is started after the end of a reception no matter if the frame is correct or erroneous.

It is not started in case the reception is restarted because of an EMD-event or in case the RX_MULTIPLE_ENABLE bit is set to 1 the TX_WAIT.

In case the register flag TX_WAIT_RFON_ENABLE is set to 1 the guard time timer is started when the devices own RF-Field was switched on.

It is possible to disable the guard time tx_wait by setting the register TX_WAIT_VALUE to 00h.

TX_WAIT can be used for 2 different purposes:

1. It can be used to prevent start of transmission before a certain period has expired - even if FW already finished data processing and set the START_SEND bit. This behavior is mainly intended for reader mode to guaranteed PICC to PCD frame delay time (FDT).

2. TX_WAIT time can be used to start the transmission at an exactly defined time.

Table 44. TX_CLIF_WAIT register (address 0011h) bit description

Bit	Symbol	Access	Value	Description
31:28	RFU	r	0*,1	-
27:8	TX_WAIT_VALUE	r/w	0*,1	Defines the tx_wait timer reload value. Note: If set to 00000h the tx_wait timer guard time is disabled Note: This bit is set by HW a protocol is detected in automatic mode detection
0	TX_WAIT_PRESCALER	r/w	0*,1	Defines the prescaler reload value for the tx_wait timer. Note: This bit is set by HW a protocol is detected in automatic mode detection

9.14.1.20 TX_CRC_CONFIG (0012h)

Table 45. TX_CRC_CONFIG (address 0012h) bit description

Bit	Symbol	Access	Value	Description
31:16	TX_CRC_PRESET_VALUE	r/w	0*-FFFFh	Arbitrary preset value for the TX-Encoder CRC calculation.
15:7	RFU	r/w	0	Reserved
6	TX_CRC_BYTE2_ENABLE	r/w	0*,1	If set; the CRC is calculated from the second byte onwards (intended for HID). This option is used in the TX-Encoder.
5:3	TX_CRC_PRESET_SEL	r/w	000-101b	Preset values of the CRC register for the TX-Encoder. For a CRC calculation using 5 bits, only the LSByte is used.
			000b*	0000h, reset value
			001b	6363h
			010b	A671h
			011b	FFFFh
			100b	0012h
			101b	E012h
			110b	RFU
			111b	Use arbitrary preset value TX_CRC_PRESET_ VALUE
2	TX_CRC_TYPE	r/w	0*,1	Controls the type of CRC calculation for the TX-Encoder
			0*	16-bit CRC calculation, reset value
			1	5-bit CRC calculation
1	TX_CRC_INV	r/w	0*,1	Controls the sending of an inverted CRC value by the TX-Encoder
			0*	Not inverted CRC checksum, reset value
			1	Inverted CRC checksum
0	TX_CRC_ENABLE	r/w	0*, 1	If set to one, the TX-Encoder computes and transmits a CRC.

9.14.1.21 SS_TX_CONFIG (00015h)

Table 46. SS_TX_CONFIG register (address 0015h) bit description

Bit	Symbol	Access	Value	Description
31:14	RFU	r	0*,1	-
13	TX2_USE_TX1_CONF	r/w	0*,1	When 1, the tx1 configuration is used also for tx2: all SS_TX2_* registers are discarded and configurations from corresponding SS_TX1_* register is used.
12:6	RFU	r/w	0*,1	-
5:3	TX2_CLK_MODE_DEFAULT	r/w	0*,1	TX2 clk mode without field (RM and CM)
2:0	TX1_CLK_MODE_DEFAULT	r/w	0*,1	TX1 clk mode without field (RM and CM)

There are 5 choices for the RF output stage behavior during 100 % modulation, and one setting for 10 % modulation. The antenna driver TX1 clk mode and TX2 clk mode are possible to be configured as such:

Table 47. Settings for Antenna drivers TX1 and TX2

TX_CLK_MODE_RM (binary)	Tx1 and TX2 output	Remarks
000	High-impedance	High-impedance of the transmitters (field-off)
001	0	Output pulled to 0 in any case
010	1	Output pulled to 1 in any case
110	RF high side push	Open-drain, only high side (push) MOS supplied with clock
101	RF low side pull	Open-drain, only low side (pull) MOS supplied with clock
111	13.56 MHz clock	Push/pull operation

9.14.1.22 SS_TX1_RMCFG (00016h)

Table 48. SS_TX1_RMCFG register (address 0016h) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	r	0*,1	-
24:22	TX1_CLK_MODE_TRANS_RM	r/w	0*,1	TX1 clock mode in RM during transition
21:19	TX1_CLK_MODE_MOD_RM	r/w	0*,1	TX1 clock mode of modulated wave in RM 000: TX1=High-Z 001: TX1=VSS_PA 010 - 110: RFU 111: TX1 clocked normal operation
18:16	TX1_CLK_MODE_CW_RM	r/w	0*,1	TX1 clock mode of modulated wave in RM 000: TX1=High-Z 001: TX1=VSS_PA 010 - 110: RFU 111: TX1 clocked normal operation
15:8	TX1_AMP_MOD_RM	r/w	0*,1	TX1 amplitude of modulated wave in RM (0x00 = 0% modulaton, 0xFF: 100% modulation)
7:0	TX1_AMP_CW_RM	r/w	0*,1	TX1 amplitude of unmodulated wave in RM (0x00 = 0% signal, 0xFF: 100% signal)

9.14.1.23 SS_TX2_RMCFG (00017h)

These settings for TX_2 are only applied, if the bit 13 in TX_CONFIG (TX2_USE_TX1_CONF is set to 0.

Table 49. SS_TX2_RMCFG register (address 0017h) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	r	0*,1	-
24:22	TX2_CLK_MODE_TRANS_RM	r/w	0*,1	TX2 clock mode in RM during transition
21:19	TX2_CLK_MODE_MOD_RM	r/w	0*,1	TX2 clock mode of modulated wave in RM 000: TX2=High-Z 001: TX2=VSS_PA 010 - 110: RFU 111: TX2 clocked normal operation
18:16	TX2_CLK_MODE_CW_RM	r/w	0*,1	TX2 clock mode of modulated wave in RM 000: TX2=High-Z 001: TX2=VSS_PA 010 - 110: RFU 111: TX2 clocked normal operation
15:8	TX2_AMP_MOD_RM	r/w	0*,1	TX2 amplitude of modulated wave in RM (0x00 = 0% modulaton, 0xFF: 100% modulation)
7:0	TX2_AMP_CW_RM	r/w	0*,1	TX2 amplitude of unmodulated wave in RM (0x00 = 0% signal, 0xFF: 100% signal)

9.14.1.24 SS_TX_TRANS_CFG (00019h)

Table 50. SS_TX_TRANS_CFG register (address 0019h) bit description

Bit	Symbol	Access	Value	Description
31:12	RFU	rw	0*,1	-
11	TX2_SS_TRANS_RATE	rw	0*,1	TX2 shaping edge rate: 0: 1/fc, 1: 2/fc. 1/fc should be selected for CM.
10	TX1_SS_TRANS_RATE	rw	0*,1	TX1 shaping edge rate: 0: 1/fc, 1: 2/fc. 1/fc should be selected for CM
9:5	TX2_SS_TRANS_LENGTH	rw	0*,1	TX2 shaping edge length: from 0 (disable) to 16. for CM, only 0 or 4 values are valid
4:0	TX1_SS_TRANS_LENGTH	rw	0*,1	TX1 shaping edge length: from 0 (disable) to 16. for CM, only 0 or 4 values are valid

9.14.1.25 SIGPRO_RM_PATTERN (0020h)

Table 51. SIGPRO_RM_PATTERN register (address 0020h) bit description

Bit	Symbol	Access	Value	Description
31:16	RM_SYNC_PATTERN	r/w	0*,1	Sync pattern for FeliCa. LSB transmitted last
15	RM_SYNC_PATTERN_EXT4	r/w	0*,1	Extend FeliCa sync pattern with 16 leading 0s
14	RM_SYNC_PATTERN_EXT2	r/w	0*,1	Extend FeliCa sync pattern with 8 leading 0s
13	RM_RECEIVE_TILL_END	r/w	0*,1	Do not stop the reception before RxDecoder sends a stop command.

Table 51. SIGPRO_RM_PATTERN register (address 0020h) bit description*...continued*

Bit	Symbol	Access	Value	Description
12	RFU	r	0*,1	-
11:0	RM_SOF_PATTERN	r/w	0*,1	SOF pattern for Type B. LSB transmitted last or Start Byte pattern for NFC passive.

9.14.1.26 SIGPRO_RM_TECH (0022h)

Table 52. SIGPRO_RM_TECH register (address 0022h) bit description

Bit	Symbol	Access	Value	Description
31:17	RFU	rw	0	-
16:15	RM_MF_GAIN	rw	0	Defines the gain of the Matched-Filters 00: Minimum Gain, 11: Maximum Gain
14:0	RFU	rw	0	-

9.14.1.27 RX_PROTOCOL_CONFIG (0025h)

Table 53. RX_PROTOCOL_CONFIG register (address 0025h) bit description

Bit	Symbol	Access	Value	Description
31:6	RFU	r	0*,1	-
5:3	RX_BIT_ALIGN	r/w	0*,1	Defines the position of the 1st received data bit in the formed data byte.000b - 0 position...111b - 7th position
2	RX_PARITY_TYPE	r/w	0*,1	0 - data + parity bits contain even number of “1”. 1 - data + parity bits contain odd number of “1”. Valid if cfg_rx_parity_enable_i ==1.
1	RX_PARITY_ENABLE	r/w	0*,1	If set to ‘1’, the bit following last data bit in the frame character is considered as parity bit.
0	RFU	r/w	0*,1	-

9.14.1.28 RX_FRAME_LENGTH (0026h)

Table 54. RX_FRAME_LENGTH register (address 0026h) bit description

Bit	Symbol	Access	Value	Description
31	RFU	r	0*,1	-
30:16	RX_FRAME_MAXLEN	r/w	0*,1	Maximal number of received [DATA + CRC] bits in the frame. The violation of the maximum length limit can be also configured as an Error/EMD condition. If the max length violation is configured as error - the frame reception is stopped in case of maximum length limit exceeding. Otherwise the reception is continued. 0x0000 - 1 bit...0x7FFF - 32 kbit
15	RFU	r	0*,1	-
14:0	RX_FRAME_MINLEN	r/w	0*,1	Minimal number of received [DATA + CRC] bits in the frame. The violation of the minimum length limit can be also configured as an Error/EMD condition. The

Table 54. RX_FRAME_LENGTH register (address 0026h) bit description*...continued*

Bit	Symbol	Access	Value	Description
				parameter also defines the number of received[DATA + CRC] bits before which any of the EOF patterns or INVPAR stop condition events are ignored.0x0000 - 1 bit...0x7FFF - 32 kbit

9.14.1.29 RX_ERROR_CONFIG (0027h)

Table 55. RX_ERROR_CONFIG register (address 0027h) bit description

Bit	Symbol	Access	Value	Description
31:0		rw		Type A/B and Type F tech all baudrates: 0x00003FFF

9.14.1.30 RX_CTRL_STATUS (0028h)

Table 56. RX_CTRL_STATUS register (address 0028h) bit description

Bit	Symbol	Access	Value	Description
31:9	RFU	r	dyn	-
8:3	RXCTRL_HF_ATT_VAL	r	dyn	HF attenuator value
2:0	RFU	r	dyn	-

9.14.1.31 SIGPRO_IIR_CONFIG0 (002Ah)

Table 57. SIGPRO_IIR_CONFIG0 register (address 002Ah) bit description

Bit	Symbol	Access	Value	Description
31:1	RFU	rw	0*,1	-
0	IIR_ENABLE	rw	0*,1	Enable the IIR filter

9.14.1.32 DGRM_BBA (002Dh)

Table 58. DGRM_BBA register (address 002Dh) bit description

Bit	Symbol	Access	Value	Description
31:17	RFU	r	0*,1	-
16:14	DGRM_BBA_MIN_VAL	r/w	0*,1	Defines the minimum value of BBA gain: 5: +24dB 4: +18dB 3: +12dB 2: +6dB 1: 0dB 0: -6dB
13:11	DGRM_BBA_MAX_VAL	r/w	0*,1	Defines the maximum value of BBA gain. 5: +24dB 4: +18dB 3: +12dB 2: +6dB 1: 0dB

Table 58. DGRM_BBA register (address 002Dh) bit description*...continued*

Bit	Symbol	Access	Value	Description
				0: -6dB
10:8	DGRM_BBA_INIT_VAL	r/w	0*,1	Defines initial value of BBA gain. 5: +24dB 4: +18dB 3: +12dB 2: +6dB 1: 0dB 0: -6dB
7:0	RFU	r	0*,1	-

9.14.1.33 DGRM_RSSI (0030h)

This register is updated dynamically by the firmware if the DPC is enabled.

Table 59. DGRM_RSSI register (address 0030h) bit description

Bit	Symbol	Access	Value	Description
31:30	RFU			-
29	DGRM_SIGNAL_DETECT_TH_OVR	r/w	0*,1	Enables the override of signal detect threshold. Override value is set based on DGRM_SIGNAL_DETECT_TH_OVR_VAL.
28:23	RFU	r/w	0*,1	-
22:17	DGRM_RSSI_HYST	r/w	0*,1	Hysteresis value for RSSI target
16:7	DGRM_RSSI_TARGET	r/w	0*,1	RSSI target value
6:0	DGRM_SIGNAL_DETECT_TH_OVR_VAL	r/w	0*,1	Defines the override value for signal detect threshold when DGRM_SIGNAL_DETECT_TH_OVR is set. These bits are modified dynamically by the ARC algorithm based on the DPC voltage. Only if the ARC is disabled, the value written during LOAD_RF_CONFIGURATION(0x0D) is retained throughout the RF Field session.

9.14.1.34 RX_CRC_CONFIG (0031h)

Table 60. RX_CRC_CONFIG register (address 0031h) bit description

Bit	Symbol	Access	Value	Description
31:16	RX_CRC_PRESET_VALUE	r	0*,1	Arbitrary preset value for the Rx-Decoder CRC calculation.
15:8	RFU	r/w	0*,1	-
7	RX_FORCE_CRC_WRITE	r/w	0*,1	If set. the Rx-Decoder will send to the RAM the CRC bits as well.
6	RX_CRC_ALLOW_BITS	r/w	0*,1	If activated the frame with length =< CRC_length will be always sent to the System RAM as is, without CRC bits removal.
5:3	RX_CRC_PRESET_SEL	r/w	0*,1	Preset value of the CRC register for the Rx-Decoder. For a CRC calculation using 5bits only the LSByte is used.

Table 60. RX_CRC_CONFIG register (address 0031h) bit description*...continued*

Bit	Symbol	Access	Value	Description
				000b* 0000h reset value. Note that this configuration is set by the Mode detector for FeliCa. 001b 6363h Note that this configuration is set by the Mode detector for ISO14443 type A. 010b A671h 011b FFFFh Note that this configuration is set by the Mode detector for ISO14443 type B. 100b 0012h 101b E012h 110b RFU 111b Use arbitrary preset value RX_CRC_PRESET_VALUE
2	RX_CRC_TYPE	r/w	0*,1	Controls the type of CRC calculation for the Rx-Decoder 0* 16bit CRC calc
1	RX_CRC_INV	r/w	0*,1	Controls the comparison of the CRC checksum for the Rx-Decoder 0*: Not inverted CRC value: 0000h reset value. Note that this bit is cleared by the Mode detector for ISO14443 type A and FeliCa. 1: Inverted CRC value: F0B8h Note that this bit is set by the Mode detector for ISO14443 type B
0	RX_CRC_ENABLE			If set. the Rx-Decoder will check the CRC for correctness. Note that this bit is set by the Mode Detector when ISO14443 type B. or FeliCa (212 kBd or 424 kBd) is detected.

9.14.1.35 RX_WAIT (0032h)

To guarantee correct protocol timing a guard period timer is implemented for the RF_EXCHANGE command in reception and transmission mode.

These guard times are not available for Transmit or Receive command.

The guard time RX_WAIT is started after the end of a transmission. The guard time RX_WAIT can be disabled by setting the register RX_WAIT_VALUE to 00h meaning the receiver is immediately enabled.

Table 61. RX_WAIT register (address 0032h) bit description

Bit	Symbol	Access	Value	Description
31:28	RFU	r	0*,1	-
27:8	RX_WAIT_VALUE	r/w	0*,1	Defines the rx_wait timer reload value. Note: If set to 00000h the rx_wait guard time is disabled
7:0	RX_WAIT_PRESCALER	r/w	0*,1	Defines the prescaler reload value for the rx_wait timer.

9.14.1.36 DCOC_CONFIG (0033h)

Table 62. DCOC_CONFIG register (address 0033h) bit description

Bit	Symbol	Access	Value	Description
31:22	RFU	rw	0*,1	-
21	DCOC_CAL_DONE_FORCE	rw	0*,1	forces the signal dcoc_cal_done to 1
20:0	RFU	rw	0*,1	-

9.14.1.37 RXM_CTRL (0035h)

Table 63. RXM_CTRL register (address 0035h) bit description

Bit	Symbol	Access	Value	Description
31:3	RFU			-
2	RXM_FRQ_CHECK_PCRM_ ENABLE	r/w		enable frequency check from PCRM
1	RXM_FRQ_CHECK_CORDIC_ ENABLE	r/w		enable precise frequency check from cordic phase (+/- 1.7 MHz multiples)
0	RXM_ENABLE	r/w		enable the all RxMeasure module

9.14.1.38 ANA_AGC_DCO_CTRL (0036h)

Table 64. ANA_AGC_DCO_CTRL register (address 0036h) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	rw	0*,1	-
24	RX_DCO_C_EN	rw	0*,1	Enable signal for the DCO coarse DAC
23:4	RFU	rw	0*,1	-
3	RX_DCO_F_EN	rw	0*,1	enable signal for the DCO fine DAC
2:0	RFU	rw	0*,1	-

9.14.1.39 SS_TX1_CMCFG (0003Bh)

Table 65. SS_TX1_CMCFG register (address 003Bh) bit description

Bit	Symbol	Access	Reset Value	Description
31:22	RFU	rw	0	-
21:19	TX1_CLK_MODE_MOD_CM	rw	0	TX1 clock mode of modulated wave in CM
18:16	TX1_CLK_MODE_CW_CM	rw	0	TX1 clock mode of unmodulated wave in CM
15:8	TX1_AMP_MOD_CM	rw	0	TX1 clock mode of modulated wave in CM
7:0	TX1_AMP_CW_CM	rw	0xFF	TX1 clock mode of unmodulated wave in CM

9.14.1.40 SS_TX2_CMCFG (0003Ch)

Table 66. SS_TX2_CMCFG register (address 003Ch) bit description

Bit	Symbol	Access	Reset Value	Description
31:22	RFU	rw	0	-
21:19	TX2_CLK_MODE_MOD_CM	rw	0	TX2 clock mode of modulated wave in CM
18:16	TX2_CLK_MODE_CW_CM	rw	0	TX2 clock mode of unmodulated wave in CM
15:8	TX2_AMP_MOD_CM	rw	0	TX2 clock mode of modulated wave in CM
7:0	TX2_AMP_CW_CM	rw	0xFF	TX2 clock mode of unmodulated wave in CM

9.14.1.41 TIMER0_CONFIG (003Dh)

Table 67. TIMER0_CONFIG register (address 003Dh) bit description

Bit	Symbol	Access	Value	Description
31:9	RFU	r	0*,1	-
8	T0_START_NOW	r/w	0*,1	T0_START_EVENT: If set. the timer T0 is started immediately
7	RFU	r	0*,1	-
6	T0_ONE_SHOT_MODE	r/w	0*,1	When set to 1, the counter value does not reload again until the counter value has reached zero
5:3	T0_PRESCALE_SEL	r/w	0*,1	Controls input frequency/period of the timer T0 when the prescaler is activated in T0_MODE_SEL. 000b - 6.78 MHz counter 001b - 3.39 MHz counter 010b - 1.70 MHz counter 011b - 848 kHz counter 100b - 424 kHz counter 101b - 212 kHz counter 110b - 106 kHz counter 111b - 53 kHz counter
2	T0_MODE_SEL	r/w	0*,1	Configuration of the timer T0 clock. 0b - Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1b - Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T0_ PRESCALE_SEL).
1	T0_RELOAD_ENABLE	r/w	0*,1	If set to 0b - the timer T0 will stop on expiration. 0* After expiration the timer T0 will stop counting. i.e. remain zero. reset value. 1b - After expiration the timer T0 will reload its preset value and continue counting down.
0	T0_ENABLE	r/w	0*,1	Enables the timer T0

9.14.1.42 TIMER0_RELOAD (003Eh)

Table 68. TIMER0_RELOAD register (address 003Eh) bit description

Bit	Symbol	Access	Value	Description
31:20	RFU	r	0*,1	-
19:0	T0_RELOAD_VALUE	r/w	0*,1	Reload value of the timer T0.

9.14.1.43 TIMER1_CONFIG (003Fh)

Timer 1 is typically used for the FDT configuration. Configuration can be done from the host but the associated IRQ is handled by the firmware of the PN7642.

Table 69. TIMER1_CONFIG register (address 003Fh) bit description

Bit	Symbol	Access	Value	Description
31	RFU	r	0*,1	-
30	T1_STOP_ON_RX_STARTED	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when a data reception begins (1st bit is received).
29	T1_STOP_ON_TX_STARTED	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when a data transmission begins.
28	T1_STOP_ON_RF_ON_EXT	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when the external RF field is detected.
27	T1_STOP_ON_RF_OFF_EXT	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when the external RF field vanishes.
26	T1_STOP_ON_RF_ON_INT	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned on.
25	T1_STOP_ON_RF_OFF_INT	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned off.
24	T1_STOP_ON_RX_ENDED	r/w	0*,1	T1_STOP_EVENT: If set the timer T1 is stopped when an activity on RX is detected.
23:18	RFU	r	0*,1	-
17	T1_START_ON_RX_STARTED	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when a data reception begins (1st bit is received).
16	T1_START_ON_RX_ENDED	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when a data reception ends.
15	T1_START_ON_TX_STARTED	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when a data transmission begins.
14	T1_START_ON_TX_ENDED	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when a data transmission ends.
13	T1_START_ON_RF_ON_EXT	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when the external RF field is detected.
12	T1_START_ON_RF_OFF_EXT	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when the external RF field is not detected anymore.
11	T1_START_ON_RF_ON_INT	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned on.

Table 69. TIMER1_CONFIG register (address 003Fh) bit description *...continued*

Bit	Symbol	Access	Value	Description
10	T1_START_ON_RF_OFF_INT	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned off.
9	T1_START_ON_TX_ FRAMESTEP	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when an activity on Frame step is detected.
8	T1_START_NOW	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started immediately.
7	RFU	r	0*,1	-
6	T1_ONE_SHOT_MODE	r/w	0*,1	When set to 1, the counter value does not reload again until the counter value has reached zero
5:3	T1_PRESCALE_SEL	r/w	0*,1	Controls input frequency/period of the timer T0 when the prescaler is activated in T1_MODE_SEL. 000b - 6.78 MHz counter 001b - 3.39 MHz counter 010b - 1.70 MHz counter 011b - 848 kHz counter 100b - 424 kHz counter 101b - 212 kHz counter 110b - 106 kHz counter 111b - 53 kHz counter
2	T1_MODE_SEL	r/w	0*,1	If set. the timer T1 is started the prescaler for the timer T1 is enabled. 0* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1 Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T1_ PRESCALE_SEL).
1	T1_RELOAD_ENABLE	r/w	0*,1	If set to 0.the timer T1 will stop on expiration. 0* After expiration the timer T1 will stop counting. i.e. remain zero. reset value. 1 After expiration the timer T1 will reload its preset value and continue counting down.
0	T1_ENABLE	r/w	0*,1	Enables the timer T1

9.14.1.44 TIMER1_RELOAD (0040h)

Table 70. TIMER1_RELOAD register (address 0040h) bit description

Bit	Symbol	Access	Value	Description
31:20	RFU	r	0*,1	-
19:0	T1_RELOAD_VALUE	r/w	0*,1	Reload value of the timer T1.

9.14.1.45 ANA_STATUS (0041h)

Table 71. ANA_STATUS register (address 0041h) bit description

Bit	Symbol	Access	Value	Description
31:21	RFU	rw	0.1	-

Table 71. ANA_STATUS register (address 0041h) bit description*...continued*

Bit	Symbol	Access	Value	Description
20:11	ADC_DATA_I	rw	0.1	RX adc I output for validation purposes
10:1	ADC_DATA_Q	rw	0.1	RX adc Q output for validation purposes
0	PLL_LOCK_STATUS	rw	0.1	PLL lock status indicator

9.14.1.46 ANA_RX_CTRL (0043h)

Table 72. ANA_RX_CTRL register (address 00434h) bit description

Bit	Symbol	Access	Value	Description
31:7	RFU	rw	0.1	-
6	RX_MIXER_SE_MODE_EN	rw	0.1	enable signal for selecting single ended mode
5:0	RFU	rw	0.1	-

9.14.1.47 ANACTRL_TX_CONFIG (0044h)

Table 73. ANACTRL_TX_CONFIG register (address 0044h) bit description

Bit	Symbol	Access	Value	Description
31:6	RFU	rw	0.1	-
5:4	TX_INVP_RM	rw	0.1	shift driver waves of 180 degrees in RM. Index 0: TX1; index 1: TX2 This value is initialized with data from TX_INV_RM (address 0018h) EEPROM bit 0.1 during Load protocol.
3:2	RFU	rw	0.1	-
1	TX_PWM_MODE_RM	rw	0.1	PWM scheme for RM: 0: TX1/2 3-levels (If at least either clk_mode_tx1 or clk_mode_tx2 is set on a clocked mode) 1: TX1/2 2-levels with differentiated pulses This value is initialized with data from TX_SHAPING_CONFIG (address 0017h) EEPROM bit 0 during Load protocol.
0	RFU	rw	0.1	-

9.14.1.48 EMD_1_CFG (0047h)

This register allows to configure the ISO14443 and NFC-Forum EMD handling.

This register shall not be modified in case EMVCO or FeliCa EMD is activated.

Table 74. EMD_1_CFG register (address 0047h) bit description

Bit	Symbol	Access	Value	Description
31:0	EMD_1_Configuration	r/w		0000 FF03h EMD ISO 0000 FF04h EMD NFC Forum

9.14.1.49 EMD_0_CONFIG (0048h)

This register allows to configure the ISO14443 and NFC-Forum EMD handling.

This register shall not be modified in case EMVCO or FeliCa EMD is activated.

Table 75. EMD_0_CONFIG register (address 0048h) bit description

Bit	Symbol	Access	Value	Description
31:0	EMD_0_Configuration	r/w		176003FFh EMD ISO14443 1F6003FFh EMD NFC Forum

9.14.1.50 LPCD_CALIBRATE_CTRL (00050h)

This register is used for LPCD semi autonomous mode. Writing to this register triggers the LPCD calibration with the RSSI_HYSTERESIS and RSSI_TARGET values as given in bits 23:16 and 15:0. After calibration is completed, calibration status is available in LPCD_CALIBRATE_STATUS. If the calibration is successful, the I/Q channel values can be read from register IQ_CHANNEL_VALS (51h).

Table 76. LPCD_CALIBRATE_CTRL register (address 0050h) bit description

Bit	Symbol	Access	Value	Description
31	RFU	r	0*,1	-
30	FREEZE_VALUE	r/w	0*,1	Write RSSI_TARGET and RSSI_HYSTERESIS into LPCD_CALIBRATE_CTRL: 1. **FREEZE_VALUE = 0:** This calibrates the Semi autonomous LPCD. The calibration status can be checked in bit 31 of CALIBRATE_STATUS register (0x53). 2. **FREEZE_VALUE = 1:** This writes the RSSI_ TARGET and RSSI_HYSTERESIS into the EEPROM LPCD_RSSI_TARGET (0x494) and LPCD_RSSI_ HYSTERESIS (0x496).
29:24	RFU	r	0*,1	-
23:16	RSSI_HYSTERESIS	r/w	0*,1	Value to be set in DGRM_RSSI_HYST used for calibration
15:0	RSSI_TARGET	r/w	0*,1	Value to be set in DGRM_RSSI_TARGET used for calibration

9.14.1.51 IQ_CHANNEL_VALS (00051h)

Table 77. IQ_CHANNEL_VALS register (address 0051h) bit description

Bit	Symbol	Access	Value	Description
31:16	Q_CHANNEL_VAL	r	-	Q Channel value
15:0	I_CHANNEL_VAL	r	-	I Channel value

9.14.1.52 PAD_CONFIG (0052h)

Table 78. PAD_CONFIG register (address 0052h) bit description

Bit	Symbol	Access	Value	Description
31:7	RFU	rw		-
6	AUX3_OUTPUT_VAL	rw		Output value for AUX3 0: Low 1: High

Table 78. PAD_CONFIG register (address 0052h) bit description*...continued*

Bit	Symbol	Access	Value	Description
5	AUX2_OUTPUT_VAL	rw		Output value for AUX2 0: Low 1: High
4	AUX1_OUTPUT_VAL	rw		Output value for AUX1 0: Low 1: High
3	GPIO3_OUTPUT_VAL	rw		Output value for GPIO3 0: Low 1: High
2	GPIO2_OUTPUT_VAL	rw		Output value for GPIO2 0: Low 1: High
1	GPIO1_OUTPUT_VAL	rw		Output value for GPIO1 0: Low 1: High
0	GPIO0_OUTPUT_VAL	rw		Output value for GPIO0 0: Low 1: High

9.14.1.53 CALIBRATE_STATUS (00053h)

Table 79. CALIBRATE_STATUS register (address 0053h) bit description

Bit	Symbol	Access	Value	Description
31	LPCD_CALIBRATION_STATUS	r	-	Calibration Status 0 - Calibration Not Done, 1- Calibration Done
30:1	RFU	r	-	-
0	TXNOV_CALIBRATION_STATUS			Calibration Status 0 - Calibration Not Done, 1- Calibration Done

9.14.1.54 TXLDO_VDDPA_CONFIG (00054h)

If DPC is disabled, the VDDPA supply voltage can be set with this register. These register settings are overruled by the DPC.

This register does allow to read the actual VDDPA supply voltage independent from having the DPC enabled/ disabled, this allows to read-out the actual transmitter supply voltage.

Table 80. TXLDO_VDDPA_CONFIG register (address 0054h) bit description

Bit	Symbol	Access	Value	Description
31:8	RFU	rw		-
7:0	VDDPA CONFIG	rw		TX_LDO output voltage VDDPA_1V50 /* 0x00 */ VDDPA_1V60, /* 0x01 */ VDDPA_1V70, /* 0x02 */ VDDPA_1V80, /* 0x03 */ VDDPA_1V90, /* 0x04 */ VDDPA_2V00, /* 0x05 */

Table 80. TXLDO_VDDPA_CONFIG register (address 0054h) bit description*...continued*

Bit	Symbol	Access	Value	Description
				VDDPA_2V10, /* 0x06 */ VDDPA_2V20, /* 0x07 */ VDDPA_2V30, /* 0x08 */ VDDPA_2V40, /* 0x09 */ VDDPA_2V50, /* 0x0A */ VDDPA_2V60, /* 0x0B */ VDDPA_2V70, /* 0x0C */ VDDPA_2V80, /* 0x0D */ VDDPA_2V90, /* 0x0E */ VDDPA_3V00, /* 0x0F */ VDDPA_3V10, /* 0x10 */ VDDPA_3V20, /* 0x11 */ VDDPA_3V30, /* 0x12 */ VDDPA_3V40, /* 0x13 */ VDDPA_3V50, /* 0x14 */ VDDPA_3V60, /* 0x15 */ VDDPA_3V70, /* 0x16 */ VDDPA_3V80, /* 0x17 */ VDDPA_3V90, /* 0x18 */ VDDPA_4V00, /* 0x19 */ VDDPA_4V10, /* 0x1A */ VDDPA_4V20, /* 0x1B */ VDDPA_4V30, /* 0x1C */ VDDPA_4V40, /* 0x1D */ VDDPA_4V50, /* 0x1E */ VDDPA_4V60, /* 0x1F */ VDDPA_4V70, /* 0x20 */ VDDPA_4V80, /* 0x21 */ VDDPA_4V90, /* 0x22 */ VDDPA_5V00, /* 0x23 */ VDDPA_5V10, /* 0x24 */ VDDPA_5V20, /* 0x25 */ VDDPA_5V30, /* 0x26 */ VDDPA_5V40, /* 0x27 */ VDDPA_5V50, /* 0x28 */ VDDPA_5V60, /* 0x29 */ VDDPA_5V70, /* 0x2A */

9.14.1.55 GENERAL_ERROR_STATUS (0055h)

Table 81. GENERAL_ERROR_STATUS register (address 0055h) bit description

Bit	Symbol	Access	Value	Description
31:3	RFU	r	0*,1	-
2	TXLDO_ERROR	r	0*,1	TXLDO does not start
1	CLOCK_ERROR	r	0*,1	XTAL or PLL does not start
0	GPADC_ERROR	r	0*,1	GPADC initialization fail

9.14.1.56 TXLDO_VOUT_CURR (0056h)

Table 82. TXLDO_VOUT_CURR register (address 0056h) bit description

Bit	Symbol	Access	Value	Description
31:24	RFU	r		-
23:8	TXLDO_CURRENT	r		Indicates the TXLDO Current, measured value is indicated in mA (1 bit = 1 mA)
7:0	VDDPA_VOUT	r		VDDPA output voltage VDDPA_1V50 /* 0x00 */ VDDPA_1V60, /* 0x01 */ VDDPA_1V70, /* 0x02 */ VDDPA_1V80, /* 0x03 */ VDDPA_1V90, /* 0x04 */ VDDPA_2V00, /* 0x05 */ VDDPA_2V10, /* 0x06 */ VDDPA_2V20, /* 0x07 */ VDDPA_2V30, /* 0x08 */ VDDPA_2V40, /* 0x09 */ VDDPA_2V50, /* 0x0A */ VDDPA_2V60, /* 0x0B */ VDDPA_2V70, /* 0x0C */ VDDPA_2V80, /* 0x0D */ VDDPA_2V90, /* 0x0E */ VDDPA_3V00, /* 0x0F */ VDDPA_3V10, /* 0x10 */ VDDPA_3V20, /* 0x11 */ VDDPA_3V30, /* 0x12 */ VDDPA_3V40, /* 0x13 */ VDDPA_3V50, /* 0x14 */ VDDPA_3V60, /* 0x15 */ VDDPA_3V70, /* 0x16 */ VDDPA_3V80, /* 0x17 */ VDDPA_3V90, /* 0x18 */ VDDPA_4V00, /* 0x19 */

Table 82. TXLDO_VOUT_CURR register (address 0056h) bit description*...continued*

Bit	Symbol	Access	Value	Description
				VDDPA_4V10, /* 0x1A */ VDDPA_4V20, /* 0x1B */ VDDPA_4V30, /* 0x1C */ VDDPA_4V40, /* 0x1D */ VDDPA_4V50, /* 0x1E */ VDDPA_4V60, /* 0x1F */ VDDPA_4V70, /* 0x20 */ VDDPA_4V80, /* 0x21 */ VDDPA_4V90, /* 0x22 */ VDDPA_5V00, /* 0x23 */ VDDPA_5V10, /* 0x24 */ VDDPA_5V20, /* 0x25 */ VDDPA_5V30, /* 0x26 */ VDDPA_5V40, /* 0x27 */ VDDPA_5V50, /* 0x28 */ VDDPA_5V60, /* 0x29 */ VDDPA_5V70, /* 0x2A */

9.14.1.57 DAC (00057h)

This register allows configuring the output voltage of VTUNE1, VTUNE2.

Table 83. DAC register (address 0057h) bit description

Bit	Symbol	Access	Value	Description
31:28	RFU			-
27:24	TUNING_DAC_2_RANGE			Reference voltage of the DAC, allows increasing the resolution in case a limited output voltage is required. For max output voltage, TUNING_DAC_2_RANGE needs to be configured to 111. Available range: 0000=2 V 0001=3 V 0011=3.45 V 0111=3.8 V If the VDDIO is 1.8 V, then configuration 000 shall be used. This applies only to DAC2.
23:17	TUNING_DAC_2_VALUE			Output voltage of DAC2 according to 1/128 *<TUNING_DAC_2_VALUE> * <Range in V>
16	TUNING_DAC_2_PD			0=DAC Turned off, 1=DAC enabled
15:12	RFU			-
11:8	TUNING_DAC_1_RANGE			Reference voltage of the DAC, allows increasing the resolution in case a limited output voltage is required. For max output voltage, TUNING_DAC_2_RANGE needs to be configured to 111. Available range: 0000=2 V 0001=3 V 0011=3.45 V 0111=3.8 V
7:1	TUNING_DAC_1_VALUE			Output voltage of DAC1 according to 1/128 * <TUNING_DAC_1_VALUE> * <Range in V>
0	TUNING_DAC_1_PD			0=DAC Turned off, 1=DAC enabled

9.14.1.58 PMU_ANA_SMPS_CTRL_REG (00058h)

Table 84. PMU_ANA_SMPS_CTRL_REG register (address 0058h) bit description

Bit	Symbol	Access	Value	Description
31:30	RFU			-
29:27	SMPS_MAXDT_SEL			SMPS max duty cycle value, valid when SMPS_MAX_DTC_BYPASS is set
26	SMPS_MAXDT_SEL_BYPASS			SMPS max duty cycle lookup table bypass
25:24	SMPS_GM			SMPS Gm setup
23:22	SMPS_RSENSE			SMPS Rsense setup
21:20	SMPS_SOFT_START			SMPS Soft Start setup
19:17	SMPS_SAWTOOTHGEN			SMPS Sawtooth generator setup
16:14	RFU			-
13:12	SMPS_PROT_UNDERSHOOT_VTH			SMPS
11:10	SMPS_REG_SPARE_0			SMPS
9:7	SMPS_PID			SMPS PID filter setup
6:1	SMPS_VDDBOOST_VOUT_SEL			SMPS Output voltage selection
0	SMPS_EN			SMPS enable

9.14.1.59 RXM_FREQ (00059h)

Table 85. RXM_FREQ register (address 0059h) bit description

Bit	Symbol	Access	Value	Description
31	RXM_FREQ_REG_VALID	r	-	CLIF_RXM_FREQ_REG fields are valid
30:25	RFU	r	-	-
24:16	RXM_FREQ	r	-	frequence difference between the last two consecutive measures at 1.7 MHz (multiple of 13.56 MHz/4096). Signed. 2-Complement coded
15:9	RFU	r	-	-
0:8	RXM_PHASE	r	-	phase value

9.14.1.60 RXM_RSSI (0005Ah)

Table 86. RXM_RSSI register (address 005Ah) bit description

Bit	Symbol	Access	Reset Value	Description
31	RFU	r	-	-
22	RXM_RSSI_FROZEN	r	-	The RSSI value is not currently updated
21	RXM_FRQ_OK	r	-	The carrier frequency detected is OK.
20	RXM_RSSI_REG_VALID	r	-	CLIF_RXM_RSSI_REG fields are valid
19:14	RXM_HFATT	r	-	HFAtt latched with RSSI
13:0	RXM_RSSI	r	-	RSSI value

9.14.1.61 TEMP_SENSOR (005Bh)

Table 87. TEMP_SENSOR register (address 005Bh) bit description

Bit	Symbol	Access	Value	Description
31:16	-	r	0*,1	RFU
15-0	TEMP_SENSOR_DATA	r	0*,1	Indicates the current temperature of the chip in degree celsius. This is the actual temperature data of the sensor which is used for the overheat protection. Maximum temperature readable will be the maximum temperature threshold configured in EEPROM TEMP_WARNING address 0x14.

9.14.1.62 TX_NOV_CALIBRATE_AND_STORE (005Dh)

Table 88. TX_NOV_CALIBRATE_AND_STORE register (address 005Dh) bit description

Bit	Symbol	Access	Value	Description
31:30	RFU	rw	0*,1	-
0	TX_NOV_CALIBRATE_AND_STORE_VAL	rw		Calibrates the TX NOV and stores the resulting value in EEPROM

9.14.1.63 DPC_CONFIG (005Eh)

Table 89. DPC_CONFIG register (address 005Eh) bit description

Bit	Symbol	Access	Value	Description
31	DPC_REG_ACCESS	r/w	0*,1	This bit is used to enable the DPC enable / disable control via register. 1: DPC enabled / disabled via register. 0: DPC enabled / disabled via EEPROM (default) This bit needs to be SET to enable/disable the functionality of bit 0.
30:1	RFU	r/w	0*,1	-
0	ENABLE_DISABLE_DPC	r/w	0*,1	1: DPC enabled, if bit 31 is enabled. 0: DPC disabled, if bit 31 is enabled. The DPC can only be enabled or disabled during RF off.

9.14.1.64 SS_TX1_RTRTRANS0 (00080h)

Table 90. SS_TX1_RTRTRANS0 register (address 0080h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_RTRANS3	rw		TX1 rising transition value 3
23:16	TX1_SS_RTRANS2	rw		TX1 rising transition value 2
15:8	TX1_SS_RTRANS1	rw		TX1 rising transition value 1
7:0	TX1_SS_RTRANS0	rw		TX1 rising transition value 0

9.14.1.65 SS_TX1_RTRTRANS1 (00081h)

Table 91. SS_TX1_RTRTRANS1 register (address 0081h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_RTRANS7	rw		TX1 rising transition value 7
23:16	TX1_SS_RTRANS6	rw		TX1 rising transition value 6
15:8	TX1_SS_RTRANS5	rw		TX1 rising transition value 5
7:0	TX1_SS_RTRANS4	rw		TX1 rising transition value 4

9.14.1.66 SS_TX1_RTRTRANS2 (00082h)

Table 92. SS_TX1_RTRTRANS2 register (address 0082h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_RTRANS11	rw		TX1 rising transition value 11
23:16	TX1_SS_RTRANS10	rw		TX1 rising transition value 10
15:8	TX1_SS_RTRANS9	rw		TX1 rising transition value 9
7:0	TX1_SS_RTRANS8	rw		TX1 rising transition value 8

9.14.1.67 SS_TX1_RTRTRANS3 (00083h)

Table 93. SS_TX1_RTRTRANS0 register (address 0080h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_RTRANS15	rw		TX1 rising transition value 15
23:16	TX1_SS_RTRANS14	rw		TX1 rising transition value 14
15:8	TX1_SS_RTRANS13	rw		TX1 rising transition value 13
7:0	TX1_SS_RTRANS12	rw		TX1 rising transition value 12

9.14.1.68 SS_TX2_RTRTRANS0 (00084h)

Table 94. SS_TX2_RTRTRANS0 register (address 0084h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_RTRANS3	rw	0*,1	TX2 rising transition value 3
23:16	TX2_SS_RTRANS2	rw	0*,1	TX2 rising transition value 2
15:8	TX2_SS_RTRANS1	rw	0*,1	TX2 rising transition value 1
7:0	TX2_SS_RTRANS0	rw	0*,1	TX2 rising transition value 0

9.14.1.69 SS_TX2_RTRTRANS1 (00085h)

Table 95. SS_TX2_RTRTRANS1 register (address 0085h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_RTRANS7	rw		TX2 rising transition value 7
23:16	TX2_SS_RTRANS6	rw		TX2 rising transition value 6
15:8	TX2_SS_RTRANS5	rw		TX2 rising transition value 5

Table 95. SS_TX2_RTRTRANS1 register (address 0085h) bit description*...continued*

Bit	Symbol	Access	Value	Description
7:0	TX2_SS_RTRANS4	rw		TX2 rising transition value 4

9.14.1.70 SS_TX2_RTRTRANS2 (00086h)

Table 96. SS_TX2_RTRTRANS2 register (address 0086h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_RTRANS11	rw		TX2 rising transition value 11
23:16	TX2_SS_RTRANS10	rw		TX2 rising transition value 10
15:8	TX2_SS_RTRANS9	rw		TX2 rising transition value 9
7:0	TX2_SS_RTRANS8	rw		TX2 rising transition value 8

9.14.1.71 SS_TX2_RTRTRANS3 (00087h)

Table 97. SS_TX2_RTRTRANS3 register (address 0087h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_RTRANS15	rw		TX2 rising transition value 15
23:16	TX2_SS_RTRANS14	rw		TX2 rising transition value 14
15:8	TX2_SS_RTRANS13	rw		TX2 rising transition value 13
7:0	TX2_SS_RTRANS12	rw		TX2 rising transition value 12

9.14.1.72 SS_TX1_FTRTRANS0 (00088h)

Table 98. SS_TX1_FTRTRANS0 register (address 0088h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_FTRANS3	rw	0*,1	TX1 falling transition value 3
23:16	TX1_SS_FTRANS2	rw	0*,1	TX1 falling transition value 2
15:8	TX1_SS_FTRANS1	rw	0*,1	TX1 falling transition value 1
7:0	TX1_SS_FTRANS0	rw	0*,1	TX1 falling transition value 0

9.14.1.73 SS_TX1_FTRTRANS1 (00089h)

Table 99. SS_TX1_FTRTRANS1 register (address 0089h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_FTRANS7	rw		TX1 falling transition value 7
23:16	TX1_SS_FTRANS6	rw		TX1 falling transition value 6
15:8	TX1_SS_FTRANS5	rw		TX1 falling transition value 5
7:0	TX1_SS_FTRANS4	rw		TX1 falling transition value 4

9.14.1.74 SS_TX1_FTRTRANS2 (0008Ah)

Table 100. SS_TX1_FTRTRANS2 register (address 008Ah) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_FTRANS11	rw		TX1 rising transition value 11
23:16	TX1_SS_FTRANS10	rw		TX1 rising transition value 10
15:8	TX1_SS_FTRANS9	rw		TX1 rising transition value 9
7:0	TX1_SS_FTRANS8	rw		TX1 rising transition value 8

9.14.1.75 SS_TX1_FTRTRANS3 (0008Bh)

Table 101. SS_TX1_FTRTRANS3 register (address 008Bh) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_FTRANS15	rw		TX1 rising transition value 15
23:16	TX1_SS_FTRANS14	rw		TX1 rising transition value 14
15:8	TX1_SS_FTRANS13	rw		TX1 rising transition value 13
7:0	TX1_SS_FTRANS12	rw		TX1 rising transition value 12

9.14.1.76 SS_TX2_FTRTRANS0 (0008Ch)

Table 102. SS_TX2_FTRTRANS0 register (address 008Ch) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_FTRANS3	rw		TX2 falling transition value 3
23:16	TX2_SS_FTRANS2	rw		TX2 falling transition value 2
15:8	TX2_SS_FTRANS1	rw		TX2 falling transition value 1
7:0	TX2_SS_FTRANS0	rw		TX2 falling transition value 0

9.14.1.77 SS_TX2_FTRTRANS1 (0008Dh)

Table 103. SS_TX2_FTRTRANS1 register (address 008Dh) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_FTRANS7	rw		TX2 falling transition value 7
23:16	TX2_SS_FTRANS6	rw		TX2 falling transition value 6
15:8	TX2_SS_FTRANS5	rw		TX2 falling transition value 5
7:0	TX2_SS_FTRANS4	rw		TX2 falling transition value 4

9.14.1.78 SS_TX2_FTRTRANS2 (0008Eh)

Table 104. SS_TX2_FTRTRANS2 register (address 008Eh) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_FTRANS11	rw		TX2 falling transition value 11
23:16	TX2_SS_FTRANS10	rw		TX2 falling transition value 10
15:8	TX2_SS_FTRANS9	rw		TX2 falling transition value 9

Table 104. SS_TX2_FTRTRANS2 register (address 008Eh) bit description...*continued*

Bit	Symbol	Access	Value	Description
7:0	TX2_SS_FTRANS8	rw		TX2 falling transition value 8

9.14.1.79 SS_TX2_FTRTRANS3 (0008Fh)

Table 105. SS_TX2_FTRTRANS3 register (address 008Fh) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_FTRANS15	rw		TX2 falling transition value 15
23:16	TX2_SS_FTRANS14	rw		TX2 falling transition value 14
15:8	TX2_SS_FTRANS13	rw		TX2 falling transition value 13
7:0	TX2_SS_FTRANS12	rw		TX2 falling transition value 12

9.14.2 EEPROM configuration description

The settings done in EEPROM are used for basic configuration which does not change frequently. Typically it is performed once during trimming or configuration of a product. The EEPROM has a limited number of erase/write cycles that can be performed. This means, that configurations that change frequently must be performed in standard registers which do not keep their value during reset and power-off.

This section describes the EEPROM configuration of the PN7642.

Writing to the EEPROM has to be performed with Read-Modify-Write for all memory addresses which contain RFU bits.

9.14.2.1 EEPROM configuration overview

Table 106. EEPROM CONFIGURATION REGISTER

Address (HEX)	Name
0	DCDC_PWR_CONFIG
1	DCDC_CONFIG
2	TXLDO_CONFIG
6	TXLDO_VDDPA_HIGH
7	RFU
8	TXLDO_VDDPA_MAX_RDR
9	TXLDO_VDDPA_HIGH_MAX_CARD
A	BOOST_DEFAULT_VOLTAGE
10	XTAL_CONFIG
11	XTAL_TIMEOUT
12	CLK_INPUT_FREQ
13	XTAL_CHECK_DELAY
14	TEMP_WARNING
15	RFU

Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (HEX)	Name
16	ENABLE_GPIO0_ON_OVERTEMP
17	TX_SHAPING_CONFIG
18	TX_INV_RM
19	TX_CLK_MODE_1
1A	TX_CLK_MODE_2
1B	RFU
1C	RFU
1D	RFU
1E	RFU
1F	RFU
20	RFU
21	RFU
22	RESIDUAL_AMP_LEVEL_A106
23	EDGE_TYPE_A106
24	EDGE_STYLE_A106
25	EDGE_LENGTH_A106
26	RESIDUAL_AMP_LEVEL_A212
27	EDGE_TYPE_A212
28	EDGE_STYLE_A212
29	EDGE_LENGTH_A212
2A	RESIDUAL_AMP_LEVEL_A424
2B	EDGE_TYPE_A424
2C	EDGE_STYLE_A424
2D	EDGE_LENGTH_A424
2E	RESIDUAL_AMP_LEVEL_A848
2F	EDGE_TYPE_A848
30	EDGE_STYLE_A848
31	EDGE_LENGTH_A848
32	RESIDUAL_AMP_LEVEL_B106
33	EDGE_TYPE_B106
34	EDGE_STYLE_B106
35	EDGE_LENGTH_B106
36	RESIDUAL_AMP_LEVEL_B212
37	EDGE_TYPE_B212
38	EDGE_STYLE_B212
39	EDGE_LENGTH_B212

Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (HEX)	Name
3A	RESIDUAL_AMP_LEVEL_B424
3B	EDGE_TYPE_B424
3C	EDGE_STYLE_B424
3D	EDGE_LENGTH_B424
3E	RESIDUAL_AMP_LEVEL_B848
3F	EDGE_TYPE_A848
40	EDGE_STYLE_A848
41	EDGE_LENGTH_A848
42	RESIDUAL_AMP_LEVEL_F212
43	EDGE_TYPE_F212
44	EDGE_STYLE_F212
45	EDGE_LENGTH_F212
46	RESIDUAL_AMP_LEVEL_F424
47	EDGE_TYPE_F424
48	EDGE_STYLE_F424
49	EDGE_LENGTH_F424
4A	RESIDUAL_AMP_LEVEL_V100_26
4B	EDGE_TYPE_V100_26
4C	EDGE_STYLE_V100_26
4D	EDGE_LENGTH_V100_26
4E	RESIDUAL_AMP_LEVEL_V100_53
4F	EDGE_TYPE_V100_53
50	EDGE_STYLE_V100_53
51	EDGE_LENGTH_V100_53
52	RESIDUAL_AMP_LEVEL_V100_106
53	EDGE_TYPE_V100_106
54	EDGE_STYLE_V100_106
55	EDGE_LENGTH_V100_106
56	RESIDUAL_AMP_LEVEL_V100_212
57	EDGE_TYPE_V100_212
58	EDGE_STYLE_V100_212
59	EDGE_LENGTH_V100_212
5A	RESIDUAL_AMP_LEVEL_V10_26
5B	EDGE_TYPE_V10_26
5C	EDGE_STYLE_V10_26
5D	EDGE_LENGTH_V10_26

Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (HEX)	Name
5E	RESIDUAL_AMP_LEVEL_V10_53
5F	EDGE_TYPE_V10_53
60	EDGE_STYLE_V10_53
61	EDGE_LENGTH_V10_53
62	RESIDUAL_AMP_LEVEL_V10_106
63	EDGE_TYPE_V10_106
64	EDGE_STYLE_V10_106
65	EDGE_LENGTH_V10_106
66	RESIDUAL_AMP_LEVEL_V10_212
67	EDGE_TYPE_V10_212
68	EDGE_STYLE_V10_212
69	EDGE_LENGTH_V10_212
66	RESIDUAL_AMP_LEVEL_V10_212
67	EDGE_TYPE_V10_212
68	EDGE_STYLE_V10_212
69	EDGE_LENGTH_V10_212
6A	RESIDUAL_AMP_LEVEL_180003m3_tari18p88
6B	EDGE_TYPE_180003m3_tari18p88
6C	EDGE_STYLE_180003m3_tari18p88
6D	EDGE_LENGTH_180003m3_tari18p88
6E	RESIDUAL_AMP_LEVEL_180003m3_tari9p44
6F	EDGE_TYPE_180003m3_tari9p44
70	EDGE_STYLE_180003m3_tari9p44
71	EDGE_LENGTH_180003m3_tari9p44
72	RESIDUAL_AMP_LEVEL_B_PRIME_106
73	EDGE_TYPE_B_PRIME_106
74	EDGE_STYLE_B_PRIME_106
75	EDGE_LENGTH_B_PRIME_106
76	DPC_CONFIG
77	DPC_TARGET_CURRENT
79	DPC_HYSTERESIS_LOADING
7A	RFU
7B	RFU
7C	DPC_HYSTERESIS_UNLOADING
7D	DPC_TXLDOVDDPALow
7E	DPC_TXGSN

Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (HEX)	Name
7F	DPC_RDON_Control
80	DPC_InitialRDOn_RFOn
81	DPC_TXLDO_MAX_DROP
83	RFU
85	RFU
87	DPC_GUARD_TIME
88	DPC_ENABLE_DURING_FDT
89	DPC_GUARD_TIME_AFTER_RX
8A	RFU
8B	DPC_LOOKUP_TABLE
137	ARC_CONFIG
139	ARC_VDDPA
13E	ARC_RM_A106
148	ARC_RM_A212
152	ARC_RM_A424
15C	ARC_RM_A848
166	ARC_RM_B106
170	ARC_RM_B212
17A	ARC_RM_B424
184	ARC_RM_B848
18E	ARC_RM_F212
198	ARC_RM_F424
1A2	ARC_RM_V6p6
1AC	ARC_RM_V26
1B6	ARC_RM_V53
1C0	ARC_RM_V106
1CA	ARC_RM_V212
1D4	ARC_RM_18003m3_SC424_4MAN
1DE	ARC_RM_18003m3_SC848_2MAN
1E8	ARC_RM_18003m3_SC848_4MAN
1F2	ARC_RM_18003m3_SC848_2MAN
1FC	ARC_RM_AI106
206	ARC_RM_AI212
210	ARC_RM_AI424
2B2	RF_DEBOUNCE_TIMEOUT
2B3	SENSE_RES

Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (HEX)	Name
2B5	NFC_ID1
2B8	SEL_RES
2B9	FELICA_POLL_RES
2CB	RANDOM_UID_ENABLE
2CC	MFC_AUTH_TIMEOUT
2DA	RSSI_TIMER
2DC	RSSI_TIMER_FIRST_PERIOD
2DE	RSSI_CTRL_00_AB
2DF	RSSI_NB_ENTRIES_AB
2E0	RSSI_THRESHOLD_PHASE_TABLE
3A2	TX_PARAM_ENTRY_TABLE
492	LPCD_AVG_SAMPLES
494	LPCD_RSSI_TARGET
496	LPCD_RSSI_HYST
497-499	RFU
49A	LPCD_THRESHOLD
49B-4AA	RFU
4AB	WAIT_RX_SETTLE
4AF	LPCD_VDDPA
4BF	ULPCD_VDDPA_CTRL
4C2	ULPCD_TIMING_CTRL
4C6	ULPCD_VOLTAGE_CTRL
4C7	RFU
4C9	ULPCD_RSSI_GUARD_TIME
4CA	ULPCD_RSSI_SAMPLE_CFG
4CB	ULPCD_THRESH_LVL
4CC	ULPCD_GPIO3
559	TXIRQ_GUARDTIME
55D	FDT_DEFAULTVAL
561	RXIRQ_GUARDTIME
562-6D2	RFU
6D3	NFCLD_RFLD_Valid
6D4-ABB	RFU
ABC	CurrentSensorTrimConfig
ABD-BD9	RFU
BDA	CORRECTION_ENTRY_TABLE

Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (HEX)	Name
C03	RTRANS_FRTANS_TABLE
C83	CFG_NOV_CAL
C84	NOV_CAL_VAL1
C85	NOV_CAL_VAL2
C86	NOV_CAL_THRESHOLD
C87	NOV_CAL_OFFSET1
C8B	NOV_CAL_OFFSET2
C8F	VDDPA_DISCHARGE
C9D	ARC_RM_A106_FDT
CA8-CC4	RFU
CC5	Tx_Symbol23_Mod_Reg_BR_53
CC9	Tx_Data_Mod_Reg_BR_53
CCD	Tx_Symbol23_Mod_Reg_BR_106
CD1	Tx_Data_Mod_Reg_BR_106
CD5	Tx_Symbol23_Mod_Reg_BR_212
CD9	Tx_Data_Mod_Reg_BR_212
CDA-CDE	RFU
CDF	CardModeUltraLowPowerEnabled
CE0	Up to FW2.01: RFU from FW2.02 onwards: LPCD_EXT_DCDC_ENABLE
CE1	Up to FW2.01: RFU from FW2.02 onwards: LPCD_EXT_DCDC_DELAY_TO_ON
CE2	Up to FW2.01: RFU from FW2.02 onwards: LPCD_EXT_DCDC_DELAY_TO_ON
CE3-CE7	DO NOT MODIFY - INTERNAL SETTINGS
CE8	RxGuardTO_Multiple
CE9	up to FW 2.03: RFU from FW2.05 onwards: DigitalTBSignalIndex
CEA	up to FW 2.03: RFU from FW2.05 onwards: DigitalTBSignalBit
CEB	up to FW 2.03: RFU from FW2.05 onwards: AnalogTBSignal
CEC-D2C	RFU
D2D-D3C	up to FW 2.03: RFU from FW2.05 onwards: USER DATA
D3Dh-1400h	DO NOT MODIFY - INTERNAL SETTINGS

9.14.2.2 DCDC_PWR_CONFIG (0000h)

Table 107. PWR_CONFIG (address 0000h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
0	DC-DC usage in card mode	7	0b: DC-DC is not powered and set to bypass 1b: DC-DC is powered and not bypassed
	DC-DC usage in reader mode	6	0b: DC-DC is not powered and set to bypass 1b: DC-DC is powered and not bypassed
	RFU	5	Do not touch, default value 01b
	VUP input voltage	4..0	0x00: Not connected or 0 V 0x01: No DC-DC and internal VDDPA_LDO: VUP supplied by VBAT / VBATPWR (pin VUP_TX connected to VBAT/VBATPWR) 0x02: Internal DC-DC: with fixed VDDBOOST 0x04: Internal DC-DC: with auto by pass and variable boost w.r.t VDDPA (internal DPC controls VDDBOOST): DC-DC goes into pass through mode when the VDDPA goes below 3.3 V. When VDDPA is greater than 3.3 V, the DC-DC is configured to boost voltage in range of 3.3 V to 6 V. 0x05 - 0x09: RFU 0x10: No DC-DC and internal VDDPA_LDO: VUP supplied by external LDO (not connected to VBAT)

9.14.2.3 DCDC_CONFIG (0001h)

Table 108. DCDC_CONFIG (address 0001h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1	DC-DC configuration	7:5	RFU
		4	DC-DC passthrough feature is: 0: Not supported (Vout = 0v or +5v) 1: Supported (Vout = 0v, Vin or +5v)
		3	Use of DC-DC for LPCD (attention: not ULPCD) 1: enabled 0: disabled
		2:0	RFU

9.14.2.4 TXLDO_CONFIG (0002h)

Table 109. TXLDO_CONFIG (address 0002h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2	TX_LDO Configuration	31:2	RFU
		1	Overcurrent protection (0: Disable, 1: Enable)
		0	Enable TXLDO 0b: disabled - no voltage output of the TXLDO 1b: enabled - regulated output of the TXLDO

9.14.2.5 TXLDO_VDDPA_HIGH (0006h)

Table 110. TXLDO_VDDPA_HIGH (address 0006h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
6	TX_LDO output: initial voltage in case the DPC is used. Applies directly at the beginning of the RF-field-on before any DPC regulation takes place. (Initial VDDPA Voltage at RF ON). These values define as well the TX_LDO output voltage in case the DPC is disabled and not used.	7:0	0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

9.14.2.6 TXLDO_VDDPA_LOW (0007h)

Table 111. TXLDO_VDDPA_LOW (address 0007h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
7	TX_LDO output voltage in case the DPC is disabled and not used.	7:0	0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

9.14.2.7 TXLDO_VDDPA_MAX_RDR (0008h)

Table 112. TXLDO_VDDPA_MAX_RDR (address 0008h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
8	VDDPA maximum output voltage in case the DPC is enabled in reader mode. This is used only when DPC is enabled. This ensures the Maximum Voltage up to which VDDPA reached during DPC Regulation.	7:0	0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

9.14.2.8 TXLDO_VDDPA_MAX_CARD (0009h)

Table 113. TXLDO_VDDPA_MAX_CARD (address 0009h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
9	VDDPA maximum output voltage in case the APC is enabled in card mode	7:0	0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

9.14.2.9 BOOST_DEFAULT_VOLTAGE (000Ah)

Table 114. BOOST_DEFAULT_VOLTAGE (address 000Ah) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
0A	DC-DC configuration This Field is Used only in case of Fixed BOOST. In case of Variable BOOST the value is calculated based on the VDDPA.	7:0	VDDBOOST output voltage in case of DC-DC with fixed VDDBOOST is enabled (PWR_CONFIG) 0x00: 3.1 V 0x01: 3.2 V 0x02: 3.3 V 0x03: 3.4 V 0x04: 3.5 V 0x05: 3.6 V 0x06: 3.7 V 0x07: 3.8 V 0x08: 3.9 V 0x09: 4.0 V 0x0A: 4.1 V 0x0B: 4.2 V 0x0C: 4.3 V 0x0D: 4.4 V 0x0E: 4.5 V 0x0F: 4.6 V 0x10: 4.7 V 0x11: 4.8 V 0x12: 4.9 V 0x13: 5.0 V 0x14: 5.1 V 0x15: 5.2 V 0x16: 5.3 V 0x17: 5.4 V 0x18: 5.5 V 0x19: 5.6 V 0x1A: 5.7 V 0x1B: 5.8 V 0x1C: 5.9 V 0x1D: 6.0 V all other values: RFU

9.14.2.10 XTAL_CONFIG (0010h)

Table 115. XTAL_CONFIG (address 0010h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
10	Configuration for the XTAL startup procedure	7:1	RFU
		0	Crystal recalibration start after wake-up from standby 1: enable 0: disable

9.14.2.11 XTAL_TIMEOUT (0011h)

Table 116. XTAL_TIMEOUT (address 0011h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
11	Configuration for the XTAL startup procedure	7:0	Timeout for XTAL to be ready (in *128us), if the timeout happens, an XTAL error event will be raised. This configuration does not speed up the boot time.

9.14.2.12 CLK_INPUT_FREQ (0012h)

Table 117. CLK_INPUT_FREQ (address 0012h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
12	Configuration for the PLL input clock frequency	7:4	RFU
		3:0	0010b: 16 MHz 0011b: 24 MHz 0100b: 32 MHz 0101b: 48 MHz 1000b: XTAL 27.12 MHz All others: RFU

9.14.2.13 XTAL_CHECK_DELAY (0013h)

Correct Crystal clocking is detected by locking the crystal to the PLL. This allows the system to start quick independent from the crystal startup time. High-quality crystals will start up typically fast and allow by this optimized current consumption, e.g, during ULPCD.

A user needs to find an optimized balance between retry numbers of checking for a proper locking and the interval for checking for a locked PLL.

This allows to configure a timeout value for locking the crystal to the PLL. The timeout value is defined by **Retry_number** x **Interval**. If the timeout is reached, a clock error is raised.

Table 118. XTAL_CHECK_DELAY (address 0013h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
13	**Retry_number**	7:5	Max Number of retries before a clock error is raised
	Interval	4:0	Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 us). This is the time to try to lock the PLL, a stable crystal clock is required for locking. If the PLL is not locked, a next retry to lock the PLL will be done after this interval. This value can be used to optimize the startup time dependent on the crystal characteristics. This is important, e.g., for optimization of the LPCD and ULPCD.

9.14.2.14 TEMP_WARNING (0014h)

Table 119. TEMP_WARNING (address 0014h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
14	CLIF and PMU temperature warning	7:6	PMU high threshold (0: disabled, 1:114degC, 2:125degC, 3:130degC)
		5:4	PMU low threshold (0: disabled, 1:114degC, 2:125degC, 3:130degC)
		3:2	high threshold (0: disabled, 1:114 °C, 2:125 °C, 3:130 °C) - in case temp sensor is triggered, transmitter and TX_LDO are shut down, system goes in low-power mode - default is 130 °C. This event is not indicated by an IRQ to the host, instead GPIO0 is used to indicate this critical event (Register PAD_CONFIG 0x52). GPIO0 is set from LOW to HIGH before the IC enters standby. To enable this event on GPIO0, the EEPROM configuration ENABLE_GPIO0_ON_ OVERTEMP (0016h) must be set. **Remark:** As soon as the chip enters standby, the GPIO0 will go to LOW
		1:0	low threshold (0: disabled, 1:114 °C, 2:125 °C, 3:130 °C) - in case temperature sensed is lower than threshold, system wakes up from low-power mode indicated by an IRQ - default is 114 °C. As soon as the chip wakes up, the wake-up source shall be checked to ensure a wake-up due to the low threshold sensing.

9.14.2.15 ENABLE_GPIO0_ON_OVERTEMP (0016h)

Table 120. ENABLE_GPIO0_ON_OVERTEMP (address 0016h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
16	RFU	7..1	-
	Set/Clear GPIO0 during over temperature.	0	If set, the GPIO0 is used to indicate a temperature event. The temperature warning levels are configured in the Register TEMP_WARNING (0014h).

9.14.2.16 TX_SHAPING_CONFIG (0017h)

Table 121. TX_SHAPING_CONFIG (address 0017h) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
17		7:1	RFU
		0	PWM scheme for RM 0: defining 3-levels for drivers TX1/2 - required for balanced antenna (default) 1: defining 2-levels for drivers TX1/2 - required for single ended antenna This value is written into CLIF_ANACTROL_TX_CONFIG_REG during Load protocol.

9.14.2.17 TX_INV_RM (0018h)

Table 122. TX_INV_RM (address 0018h) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
18	Transmitter configuration	7:6	RFU
		5	0: TX1 non-inverted output (output zero remains zero) 1: TX1 inverted output (common mode operation, output zero becomes one) This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol.
		4	0: TX2 non-inverted output (output zero remains zero) 1: TX2 inverted output (common mode operation, output zero becomes one) This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol.
		3:2	RFU
		1	0: TX1 no phase shift, 0° 1: TX1 phase shifted by 180° This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol.
		0	0: TX2 no phase shift, 0° 1: TX2 phase shifted by 180° This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol.

9.14.2.18 TX_CLK_MODE_1 (0019h)

Table 123. TX_CLK_MODE_1 (address 0019h) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
19	Transmitter clock configuration	7	RFU
		6:4	CLK_MODE_CW_RM
		3	RFU
		2:0	CLK_MODE_MOD_RM

9.14.2.19 TX_CLK_MODE_2 (001Ah)

Table 124. TX_CLK_MODE_2 (address 001Ah) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
1A	Transmitter clock configuration	7	RFU
		6:4	CLK_MODE_DEFAULT
		3	RFU
		2:0	CLK_MODE_TRANS_RM

9.14.2.20 RESIDUAL_AMPL_LEVEL_A106 (0022h)

Table 125. RESIDUAL_AMPL_LEVEL_A106 (address 0022h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0% carrier FF: 100% carrier

9.14.2.21 EDGE_TYPE_A106 (0023h)

Table 126. EDGE_TYPE_A106 (address 0023h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.22 EDGE_STYLE_A106 (0024h)

Table 127. EDGE_STYLE_A106 (address 0024h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6:

Table 127. EDGE_STYLE_A106 (address 0024h) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
	configuration falling edge		This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.23 EDGE_LENGTH_A106 (0025h)

Table 128. EDGE_LENGTH_A106 (address 0025h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.24 RESIDUAL_AMPL_LEVEL_A212 (0026h)

Table 129. RESIDUAL_AMPL_LEVEL_A212 (address 0026h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.25 EDGE_TYPE_A212 (0027h)

Table 130. EDGE_TYPE_A212 (address 0027h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

Table 130. EDGE_TYPE_A212 (address 0027h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.26 EDGE_STYLE_A212 (0028h)

Table 131. EDGE_STYLE_A212 (address 0028h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.27 EDGE_LENGTH_A212 (0029h)

Table 132. EDGE_LENGTH_A212 (address 0029h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.28 RESIDUAL_AMPL_LEVEL_A424 (002Ah)

Table 133. RESIDUAL_AMPL_LEVEL_A424 (address 002Ah) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
2A	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.29 EDGE_TYPE_A424 (002Bh)

Table 134. EDGE_TYPE_A424 (address 002Bh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.30 EDGE_STYLE_A424 (002Ch)

Table 135. EDGE_STYLE_A424 (address 002Ch) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6:

Table 135. EDGE_STYLE_A424 (address 002Ch) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
	configuration falling edge		This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.31 EDGE_LENGTH_A424 (002Dh)

Table 136. EDGE_LENGTH_A424 (address 002Dh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.32 RESIDUAL_AMPL_LEVEL_A848 (002Eh)

Table 137. RESIDUAL_AMPL_LEVEL_A848 (address 002Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.33 EDGE_TYPE_A848 (002Fh)

Table 138. EDGE_TYPE_A848 (address 002Fh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

Table 138. EDGE_TYPE_A848 (address 002Fh) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.34 EDGE_STYLE_A848 (0030h)

Table 139. EDGE_STYLE_A848 (address 0030h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.35 EDGE_LENGTH_A848 (0031h)

Table 140. EDGE_LENGTH_A848 (address 0031h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.36 RESIDUAL_AMPL_LEVEL_B106 (0032h)

Table 141. RESIDUAL_AMPL_LEVEL_B106 (address 0032h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.37 EDGE_TYPE_B106 (0033h)

Table 142. EDGE_TYPE_B106 (address 0033h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.38 EDGE_STYLE_B106 (0034h)

Table 143. EDGE_STYLE_B106 (address 0034h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6:

Table 143. EDGE_STYLE_B106 (address 0034h) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
	configuration falling edge		This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.39 EDGE_LENGTH_B106 (0035h)

Table 144. EDGE_LENGTH_B106 (address 0035h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.40 RESIDUAL_AMPL_LEVEL_B212 (0036h)

Table 145. RESIDUAL_AMPL_LEVEL_B212 (address 0036h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.41 EDGE_TYPE_B212 (0037h)

Table 146. EDGE_TYPE_B212 (address 0037h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

Table 146. EDGE_TYPE_B212 (address 0037h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.42 EDGE_STYLE_B212 (0038h)

Table 147. EDGE_STYLE_B212 (address 0038h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.43 EDGE_LENGTH_B212 (0039h)

Table 148. EDGE_LENGTH_B212 (address 0039h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.44 RESIDUAL_AMPL_LEVEL_B424 (003Ah)

Table 149. RESIDUAL_AMPL_LEVEL_B424 (address 003Ah) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.45 EDGE_TYPE_B424 (003Bh)

Table 150. EDGE_TYPE_B424 (address 003Bh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.46 EDGE_STYLE_B424 (003Ch)

Table 151. EDGE_STYLE_B424 (address 003Ch) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1,2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6:

Table 151. EDGE_STYLE_B424 (address 003Ch) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
	configuration falling edge		This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1,2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.47 EDGE_LENGTH_B424 (003Dh)

Table 152. EDGE_LENGTH_B424 (address 003Dh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.48 RESIDUAL_AMPL_LEVEL_B848 (003Eh)

Table 153. RESIDUAL_AMPL_LEVEL_B848 (address 003Eh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.49 EDGE_TYPE_B848 (003Fh)

Table 154. EDGE_TYPE_B848 (address 003Fh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

Table 154. EDGE_TYPE_B848 (address 003Fh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.50 EDGE_STYLE_B848 (0040h)

Table 155. EDGE_STYLE_B848 (address 0040h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.51 EDGE_LENGTH_B848 (0041h)

Table 156. EDGE_LENGTH_B848 (address 0041h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.52 RESIDUAL_AMPL_LEVEL_F212 (0042h)

Table 157. RESIDUAL_AMPL_LEVEL_F212 (address 0042h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.53 EDGE_TYPE_F212 (0043h)

Table 158. EDGE_TYPE_F212 (address 0043h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.54 EDGE_STYLE_F212 (0044h)

Table 159. EDGE_STYLE_F212 (address 0044h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6:

Table 159. EDGE_STYLE_F212 (address 0044h) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
	configuration falling edge		This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.55 EDGE_LENGTH_F212 (0045h)

Table 160. EDGE_LENGTH_F212 (address 0045h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.56 RESIDUAL_AMPL_LEVEL_F424 (0046h)

Table 161. RESIDUAL_AMPL_LEVEL_F424 (address 0046h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.57 EDGE_TYPE_F424 (0047h)

Table 162. EDGE_TYPE_F424 (address 0047h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

Table 162. EDGE_TYPE_F424 (address 0047h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.58 EDGE_STYLE_F424 (0048h)

Table 163. EDGE_STYLE_F424 (address 0048h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.59 EDGE_LENGTH_F424 (0049h)

Table 164. EDGE_LENGTH_F424 (address 0049h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.60 RESIDUAL_AMPL_LEVEL_V100_26 (004Ah)

Table 165. RESIDUAL_AMPL_LEVEL_V100_26 (address 004Ah) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.61 EDGE_TYPE_V100_26 (004Bh)

Table 166. EDGE_TYPE_V100_26 (address 004Bh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.62 EDGE_STYLE_V100_26 (004Ch)

Table 167. EDGE_STYLE_V100_26 (address 004Ch) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6:

Table 167. EDGE_STYLE_V100_26 (address 004Ch) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
	configuration falling edge		This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.63 EDGE_LENGTH_V100_26 (004Dh)

Table 168. EDGE_LENGTH_V100_26 (address 004Dh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.64 RESIDUAL_AMPL_LEVEL_V100_53 (004Eh)

Table 169. RESIDUAL_AMPL_LEVEL_V100_53 (address 004Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.65 EDGE_TYPE_V100_53 (004Fh)

Table 170. EDGE_TYPE_V100_53 (address 004Fh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

Table 170. EDGE_TYPE_V100_53 (address 004Fh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.66 EDGE_STYLE_V100_53 (0050h)

Table 171. EDGE_STYLE_A106 (address 0050h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.67 EDGE_LENGTH_V100_53 (0051h)

Table 172. EDGE_LENGTH_V100_53 (address 0051h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.68 RESIDUAL_AMPL_LEVEL_V100_106 (0052h)

Table 173. RESIDUAL_AMPL_LEVEL_V100_106 (address 0052h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.69 EDGE_TYPE_V100_106 (0053h)

Table 174. EDGE_TYPE_V100_106 (address 0053h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.70 EDGE_STYLE_V100_106 (0054h)

Table 175. EDGE_STYLE_V100_106 (address 0054h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6:

Table 175. EDGE_STYLE_V100_106 (address 0054h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
	configuration falling edge		This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.71 EDGE_LENGTH_V100_106 (0055h)

Table 176. EDGE_LENGTH_V100_106 (address 0055h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.72 RESIDUAL_AMPL_LEVEL_100_212 (0056h)

Table 177. RESIDUAL_AMPL_LEVEL_100_212 (address 0056h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.73 EDGE_TYPE_V100_212 (0057h)

Table 178. EDGE_TYPE_V100_212 (address 0057h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

Table 178. EDGE_TYPE_V100_212 (address 0057h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.74 EDGE_STYLE_V100_212 (0058h)

Table 179. EDGE_STYLE_V100_212 (address 0058h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.75 EDGE_LENGTH_V100_212 (0059h)

Table 180. EDGE_LENGTH_V100_212 (address 0059h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.76 RESIDUAL_AMPL_LEVEL_V10_26 (005Ah)

Table 181. RESIDUAL_AMPL_LEVEL_V10_26 (address 005Ah) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.77 EDGE_TYPE_V10_26 (005Bh)

Table 182. EDGE_TYPE_V10_26 (address 005Bh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.78 EDGE_STYLE_V10_26 (005Ch)

Table 183. EDGE_STYLE_V10_26 (address 005Ch) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6:

Table 183. EDGE_STYLE_V10_26 (address 005Ch) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
	configuration falling edge		This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.79 EDGE_LENGTH_V10_26 (005Dh)

Table 184. EDGE_LENGTH_V10_26 (address 005Dh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.80 RESIDUAL_AMPL_LEVEL_V10_53 (005Eh)

Table 185. RESIDUAL_AMPL_LEVEL_V10_53 (address 005Eh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.81 EDGE_TYPE_V10_53 (005Fh)

Table 186. EDGE_TYPE_V10_53 (address 005Fh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

Table 186. EDGE_TYPE_V10_53 (address 005Fh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.82 EDGE_STYLE_V10_53 (0060h)

Table 187. EDGE_STYLE_V10_53 (address 0060h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.83 EDGE_LENGTH_V10_53 (0061h)

Table 188. EDGE_LENGTH_V10_53 (address 0061h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.84 RESIDUAL_AMPL_LEVEL_V10_106 (0062h)

Table 189. RESIDUAL_AMPL_LEVEL_V10_106 (address 0062h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.85 EDGE_TYPE_V10_106 (0063h)

Table 190. EDGE_TYPE_V10_106 (address 0063h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.86 EDGE_STYLE_V10_106 (0064h)

Table 191. EDGE_STYLE_V100_212 (address 0064h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6:

Table 191. EDGE_STYLE_V100_212 (address 0064h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
	configuration falling edge		This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.87 EDGE_LENGTH_V10_106 (0065h)

Table 192. EDGE_LENGTH_V10_106 (address 0065h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.88 RESIDUAL_AMPL_LEVEL_V10_212 (0066h)

Table 193. RESIDUAL_AMPL_LEVEL_V10_212 (address 0066h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.89 EDGE_TYPE_V10_212 (0067h)

Table 194. EDGE_TYPE_V10_212 (address 0067h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

Table 194. EDGE_TYPE_V10_212 (address 0067h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.90 EDGE_STYLE_V10_212 (0068h)

Table 195. EDGE_STYLE_V10_212 (address 0068h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.91 EDGE_LENGTH_V10_212 (0069h)

Table 196. EDGE_LENGTH_V100_212 (address 0069h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.92 RESIDUAL_AMPL_LEVEL_180003m3_tari18p88 (006Ah)

Table 197. RESIDUAL_AMPL_LEVEL_180003m3_tari18p88 (address 006Ah) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.93 EDGE_TYPE_180003m3_tari18p88 (006Bh)

Table 198. EDGE_TYPE_180003m3_tari18p88 (address 006Bh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.94 EDGE_STYLE_180003m3_tari18p88 (006Ch)

Table 199. EDGE_STYLE_180003m3_tari18p88 (address 006Ch) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style)

Table 199. EDGE_STYLE_180003m3_tari18p88 (address 006Ch) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
	configuration falling edge		If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.95 EDGE_LENGTH_180003m3_tari18p88 (006Dh)

Table 200. EDGE_LENGTH_180003m3_tari18p88 (address 006Dh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.96 RESIDUAL_AMPL_LEVEL_180003m3_tari9p44 (006Eh)

Table 201. RESIDUAL_AMPL_LEVEL_180003m3_tari9p44 (address 006Eh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.97 EDGE_TYPE_180003m3_tari9p44 (006Fh)

Table 202. EDGE_TYPE_180003m3_tari9p44 (address 006Fh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

Table 202. EDGE_TYPE_180003m3_tari9p44 (address 006Fh) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.98 EDGE_STYLE_180003m3_tari9p44 (0070h)

Table 203. EDGE_STYLE_180003m3_tari9p44 (address 0070h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.99 EDGE_LENGTH_180003m3_tari9p44 (0071h)

Table 204. EDGE_LENGTH_180003m3_tari9p44 (address 0071h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.100 RESIDUAL_AMPL_LEVEL_B_PRIME_106 (0072h)

Table 205. RESIDUAL_AMPL_LEVEL_180003m3_tari18p88 (address 0072h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.14.2.101 EDGE_TYPE_B_PRIME_106 (0073h)

Table 206. EDGE_TYPE_B_PRIME_106 (address 0073h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.14.2.102 EDGE_STYLE_B_PRIME_106 (0074h)

Table 207. EDGE_STYLE_B_PRIME_106 (address 0074h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style)

Table 207. EDGE_STYLE_B_PRIME_106 (address 0074h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
	configuration falling edge		If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.14.2.103 EDGE_LENGTH_B_PRIME_106 (0075h)

Table 208. EDGE_LENGTH_B_PRIME_106 (address 0075h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.14.2.104 DPC_CONFIG (0076h)

Table 209. DPC_CONFIG (address 0076h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
76	DPC Configuration	7:3	RFU
		2	DPC in Active Target Mode: 0: disabled, 1: enabled
		1	DPC in Active Initiator Mode: 0: disabled, 1: enabled
		0	DPC in Reader/ Passive Initiator Mode: 0: disabled, 1: enabled

9.14.2.105 DPC_TARGET_CURRENT (077h)

Table 210. DPC_TARGET_CURRENT (address 077h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
77	DPC Configuration	15:0	VDDPA target current in mA. The target current +/- hysteresis defines the limiting maximum current for the DPC.

Table 210. DPC_TARGET_CURRENT (address 077h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
			This configuration shall not exceed 350 mA - hysteresis.

Note: *The resulting current that is driven by the transmitter can be further reduced based on the current reduction lookup table entries.*

9.14.2.106 DPC_HYSTERESIS_LOADING (079h)

The hysteresis (DPC_HYSTERESIS_LOADING, DPC_HYSTERESIS_UNLOADING) together with the target current (DPC_TARGET_CURRENT) defines the current limit, at which the DPC automatically decreases or increases the VDDPA.

The VDDPA is automatically reduced, as soon as the current exceeds the DPC_TARGET_CURRENT + DPC_HYSTERESIS_LOADING, and the VDDPA is automatically increased again, as soon as the current is below DPC_TARGET_CURRENT – DPC_HYSTERESIS_UNLOADING.

Table 211. DPC_HYSTERESIS_LOADING (address 079h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
79	DPC Configuration	7:0	Absolute difference of measured transmitter current (target current incl. current reduction) in mA that triggers a DPC update event during loading.

Note: *If the hysteresis is configured too small, it might cause an oscillation of the transmitted field.*

Note: *In most application, the default values work well and do not need to be modified.*

9.14.2.107 DPC_HYSTERESIS_UNLOADING (07Ch)

The hysteresis (DPC_HYSTERESIS_LOADING, DPC_HYSTERESIS_UNLOADING) together with the target current (DPC_TARGET_CURRENT) defines the current limit, at which the DPC automatically decreases or increases the VDDPA.

The VDDPA is automatically reduced, as soon as the current exceeds the DPC_TARGET_CURRENT + DPC_HYSTERESIS_LOADING, and the VDDPA is automatically increased again, as soon as the current is below DPC_TARGET_CURRENT – DPC_HYSTERESIS_UNLOADING.

Table 212. DPC_HYSTERESIS_UNLOADING (address 07Ch) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
7C	DPC Configuration	7:0	Absolute difference of measured transmitter current (target current incl. current reduction) in mA that triggers a DPC update event during unloading.

Note: *If the hysteresis is configured too small, it might cause an oscillation of the transmitted field.*

Note: *In most application, the default values work well and do not need to be modified.*

9.14.2.108 DPC_TXLDOVDDPALow (007Dh)

Table 213. DPC_TXLDOVDDPALow (address 007Dh) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
7D	DPC Configuration	7:0	VDDPA Low Limit for RDON

9.14.2.109 DPC_TXGSN (007Eh)

Table 214. DPC_TXGSN (address 007Eh) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
7E	DPC Configuration	7:0	for tx1_gsn < 20: resistance = 10 Ohm / (tx1_gsn + 1) for tx1_gsn >= 20: resistance = 0.5 Ohm

9.14.2.110 DPC_RDON_Control (007Fh)

Table 215. DPC_RDON_Control (address 007Fh) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
7F	DPC Configuration	7:0	00: Disabled 01: RdON Control 02-FF: RFU

9.14.2.111 DPC_InitialRDOn_RFOn (0080h)

Table 216. DPC_InitialRDOn_RFOn (address 0080h) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
80	DPC Configuration	7:0	Initial GSP TX1/TX2 value during FieldON

9.14.2.112 DPC_GUARD_TIME (087h)

Table 217. DPC_GUARD_TIME (address 087h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
87	DPC guard time configuration	7:0	Guard time before TX and after RX. 1unit = 1us. The DPC regulation is done once before TX and once after RX. The guard time parameter is the time between DPC regulation completion and TX start. The guard time parameter is the time between RX stop and DPC regulation start. The guard time is always enabled for TX

Note: *Recommendation is not to modify the default value.*

9.14.2.113 DPC_ENABLE_DURING_FDT (088h)

Table 218. DPC_ENABLE_DURING_FDT (address 088h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
88	RFU	7-1	-
	DPC Configuration	0	DPC regulation enable during FDT 0: DPC disabled during FDT (debug purpose only) 1: DPC enabled during FDT (recommendation)

9.14.2.114 DPC_GUARD_TIME_AFTER_RX (089h)

Table 219. DPC_GUARD_TIME_AFTER_RX (address 089h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
89	RFU	7:1	-
89	DPC Configuration	0	Enable DPC guard time after RX 0: disable (debug purposes) 1: enable (recommended) The guard time can be configured in register DPC_GUARD_TIME

Note: *The guard time is always enabled for TX and cannot be disabled.*

9.14.2.115 DPC_LOOKUP_TABLE (008Bh-0133h)

Table 220. DPC_LOOKUP_TABLE (008Bh-0133h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
	ENTRY 0	31:0	This is the entry for 1.5 V
08B	Target current reduction	31:23	ENTRY 0 -LSB - byte 0 Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V bEntry_00 = 1V5 ... bEntry_42 = 5V7 Bits[7:0] = Target current reduction in mA (unsigned)
08C	AWC amp mod change	23:16	ENTRY 0 - byte 1 Bits[7:0] = Relative change of modulated amplitude level (signed)
08D	AWC edge time constant for ASK100	15:8	ENTRY 0 - byte 2 Bits[3:0] = ASK100, Relative change of falling edge time constant (signed) Bits[7:4] = ASK100, Relative change of rising edge time constant (signed)
08E	AWC falling edge time constant for ASK10	7:0	ENTRY 0 -MSB - byte 4 Bits[3:0] = ASK10, Relative change of falling edge time constant (signed) Bits[7:4] = ASK10, Relative change of rising edge time constant (signed)
08F	ENTRY 1	31:0	This is the entry for 1.6 V
….			….
093	ENTRY 2	31:0	This is the entry for 1.7 V
…..			….
….			This is the entry for 5.6 V
0133	ENTRY 42	31:0	This is the entry for 5.7 V

9.14.2.116 ARC_CONFIG (0137h)

Table 221. ARC_CONFIG (address 0137h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
137	ARC Setting configuration	7	ARC algorithm enable 0: Disable

Table 221. ARC_CONFIG (address 0137h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: Enable
		6:3	RFU
		2:0	Number of entries in ARC table. (value between 0 to 4) 0: one entry 1: two entries 2: three entries 3: four entries 4: five entries

9.14.2.117 ARC_VDDPA (0139h)

Table 222. ARC_VDDPA (0139Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
13D	VDDPA_4	7:0	Byte[4] = VDDPA range_index 4: if VDDPA voltage between VDDPA_3 to ARC_VDDPA_4
13C	VDDPA_3	7:0	Byte[3] = VDDPA_range_index 3: if VDDPA voltage between VDDPA_2 to ARC_VDDPA_3 - 0.1
13B	VDDPA_2	7:0	Byte[2] = VDDPA_range_index 2: if VDDPA voltage between VDDPA_1 to ARC_VDDPA_2 - 0.1
13A	VDDPA_1	7:0	Byte[1] = VDDPA_range_index 1: if VDDPA voltage between VDDPA_0 to (ARC_VDDPA_1 - 0.1)
139	VDDPA_0	7:0	Byte[0] = VDDPA_range_index 0: if VDDPA voltage between 1.5 to (VDDPA_0 - 0.1)

Note: *VDDPA setting for Bytes 0...4:*

0x00: 1V50

0x01: 1V60

0x02: 1V70

0x03: 1V80

0x04: 1V90

0x05: 2V00

0x06: 2V10

0x07: 2V20

0x08: 2V30

0x09: 2V40

0x0A: 2V50

0x0B: 2V60

0x0C: 2V70

0x0D: 2V80

0x0E: 2V90

0x0F: 3V00

0X10: 3V10

0x11: 3V20

0x12: 3V30

0x13: 3V40

0x14: 3V50

0x15: 3V60

0x16: 3V70

0x17: 3V80

0x18: 3V90

0x19: 4V00

0x1A: 4V10

0x1B: 4V20

0x1C: 4V30

0x1D: 4V40

0x1E: 4V50

0x1F: 4V60

0x20: 4V70

0x21: 4V80

0x22: 4V90

0x23: 5V00

0x24: 5V10

0x25: 5V20

0x26: 5V30

0x27: 5V40

0x28: 5V50

0x29: 5V60

0x2A: 5V70

9.14.2.118 ARC_RM_A106 (013Eh)

This is the setting for type A-106.

Table 223. ARC_RM_A106 (address 013Eh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
146	RM_RX_ARC_4	15:0	Bit[15] This setting is only taken into account if bit 14 of address 13E is set.

Table 223. ARC_RM_A106 (address 013Eh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
144	RM_RX_ARC_3	15:0	Bit[15] This setting is only taken into account if bit 14 of address 13E is set. 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
142	RM_RX_ARC_2	15:0	Bit[15] This setting is only taken into account if bit 14 of address 13E is set. 0: ARC settings always apply, bits 0...9 from the table ARC_RM_106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
140	RM_RX_ARC_1	15:0	Bit[15] This setting is only taken into account if bit 14 of address 13E is set. 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
13E	RM_RX_ARC_0	15:0	Bit[15] This setting is only taken into account if bit 14 of address 13E is set. 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used Bit [14]:

Table 223. ARC_RM_A106 (address 013Eh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: ARC enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

9.14.2.119 ARC_RM_A212 (0148h)

This is the setting for type A-212.

Table 224. ARC_RM_A212 (address 0148h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
150	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
14E	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
14C	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)

Table 224. ARC_RM_A212 (address 0148h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
14A	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
148	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.120 ARC_RM_A424 (0152h)

This is the setting for type A-424.

Table 225. ARC_RM_A424 (address 0152h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
15A	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424 Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Table 225. ARC_RM_A424 (address 0152h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
158	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
156	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
154	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
152	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.121 ARC_RM_A848 (015Ch)

This is the setting for type A-848.

Table 226. ARC_RM_A848 (address 015Ch) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
164	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
162	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
160	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
15E	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
15C	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter.

Table 226. ARC_RM_A848 (address 015Ch) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.122 ARC_RM_B106 (0166h)

This is the setting for type B-106.

Table 227. ARC_RM_B106 (address 0166h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
16E	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
16C	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
16A	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
168	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used

Table 227. ARC_RM_B106 (address 0166h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
166	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.123 ARC_RM_B212 (0170h)

This is the setting for type B-212.

Table 228. ARC_RM_B212 (address 0170h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
178	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
176	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter.

Table 228. ARC_RM_B212 (address 0170h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
174	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
172	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
170	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.124 ARC_RM_B424 (017Ah)

This is the setting for type B-424.

Table 229. ARC_RM_B424 (address 017Ah) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
182	RM_RX_ARC_4	15:0	Bit[15]

Table 229. ARC_RM_B424 (address 017Ah) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			0: ARC settings always apply, bits 0...9 from the table ARC_RM_B424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
180	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
17E	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
17C	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
17A	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)

Table 229. ARC_RM_B424 (address 017Ah) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.125 ARC_RM_B848 (0184h)

This is the setting for type B-848.

Table 230. ARC_RM_B848 (address 0184h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
18C	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
18A	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
188	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
186	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used

Table 230. ARC_RM_B848 (address 0184h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
184	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.126 ARC_RM_F212 (018Eh)

This is the setting for type F-212.

Table 231. ARC_RM_F212 (address 018Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
196	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
194	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter.

Table 231. ARC_RM_F212 (address 018Eh) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
192	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
190	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
18E	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.127 ARC_RM_F424 (0198h)

This is the setting for type F-424.

Table 232. ARC_RM_F424 (address 0198h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
1A0	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
19E	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
19C	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
19A	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
198	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter.

Table 232. ARC_RM_F424 (address 0198h) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.128 ARC_RM_V_6p6 (01A2h)

This is the setting for type A-106.

Table 233. ARC_RM_V_6p6 (address 01A2h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
1AA	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1A8	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1A6	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1A4	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used

Table 233. ARC_RM_V_6p6 (address 01A2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1A2	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.129 ARC_RM_V_26 (01ACh)

This is the setting for type V 26.

Table 234. ARC_RM_V_26 (address 01ACh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1B4	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V26 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1B2	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V26 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26 Bits[14:10] = RFU Bit [9] = Enable the IIR filter.

Table 234. ARC_RM_V_26 (address 01ACh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1B0	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V26 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1AE	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V26 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1AC	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.130 ARC_RM_V53 (01B6h)

This is the setting for type V53.

Table 235. ARC_RM_V53(address 01B6h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1BE	RM_RX_ARC_4	15:0	Bit[15]

Table 235. ARC_RM_V53(address 01B6h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			0: ARC settings always apply, bits 0...9 from the table ARC_RM_V53 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1BC	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V53 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1BA	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V53 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1B8	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V53 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1B6	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)

Table 235. ARC_RM_V53(address 01B6h) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
			Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.131 ARC_RM_V106 (01C0h)

This is the setting for type V106.

Table 236. ARC_RM_V106(address 01C0h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
1C8	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1C6	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1C4	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1C2	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212

Table 236. ARC_RM_V106(address 01C0h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1C0	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.132 ARC_RM_V212 (01CAh)

This is the setting for type V212.

Table 237. ARC_RM_V212(address 01CAh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1D2	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1D0	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)

Table 237. ARC_RM_V212(address 01CAh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1CE	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1CC	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1CA	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.133 ARC_RM_180003m3_SC424_4Man (01D4h)

This is the setting for type 180003m3_SC424_4Man.

Table 238. ARC_RM_180003m3_SC424_4Man (address 01D4h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1DC	RM_RX_ARC_4	15:0	Bit[15]

Table 238. ARC_RM_180003m3_SC424_4Man (address 01D4h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1DA	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1D8	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1D6	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1D4	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU

Table 238. ARC_RM_180003m3_SC424_4Man (address 01D4h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.134 ARC_RM_180003m3_SC424_2Man (01DEh)

This is the setting for type 180003m3_SC424_2Man.

Table 239. ARC_RM_180003m3_SC424_2Man (address 01DEh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1E6	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1E4	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1E2	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN Bits[14:9] = RFU Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)

Table 239. ARC_RM_180003m3_SC424_2Man (address 01DEh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1E0	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1DE	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.135 ARC_RM_180003m3_SC848_4Man (01E8h)

This is the setting for type 180003m3_SC848_4Man.

Table 240. ARC_RM_180003m3_SC848_4Man (address 01E8h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1F0	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1EE	RM_RX_ARC_3	15:0	Bit[15]

Table 240. ARC_RM_180003m3_SC848_4Man (address 01E8h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1EC	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1EA	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1E8	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.136 ARC_RM_180003m3_SC848_2Man (01F2h)

This is the setting for type 180003m3_SC848_2Man.

Table 241. ARC_RM_180003m3_SC848_2Man (address 01F2h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
1FA	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2 MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1F8	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2 MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1F6	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2 MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1F4	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2 MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Table 241. ARC_RM_180003m3_SC848_2Man (address 01F2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
1F2	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.137 ARC_RM_AI106 (01FCh)

This is the setting for type AI106.

Table 242. ARC_RM_AI106 (address 01FCh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
204	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
202	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
200	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106 Bits[14:10] = RFU

Table 242. ARC_RM_AI106 (address 01FCh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1FE	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1FC	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.138 ARC_RM_AI212 (0206h)

This is the setting for type AI212.

Table 243. ARC_RM_AI212 (0206h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
20E	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Table 243. ARC_RM_AI212 (0206h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
20C	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
20A	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
208	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
206	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.139 ARC_RM_AI424 (0210h)

This is the setting for type AI424.

Table 244. ARC_RM_AI424 (0210h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
218	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
216	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
214	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
212	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
210	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change

Table 244. ARC_RM_AI424 (0210h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.14.2.140 RF_DEBOUNCE_TIMEOUT (02B2h)

Table 245. RF_DEBOUNCE_TIMEOUT (address 02B2h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2B2	DEBOUNCE_ TIMEOUT	7:0	Timeout used after the RF detection during the AUTOCOLL to detect if there is a glitch or continuous RF Value is entered in micro seconds, each bit represents 1 micro second

9.14.2.141 SENSE_RES (02B3h)

Table 246. SENSE_RES (address 02B3) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2B3	AUTOCOLL configuration	16:0	ATQA in order byte 0, byte 1
		16:8	Byte1
		7:0	Byte0

9.14.2.142 NFC_ID1 (02B5h)

Table 247. SIGNAL_SCALING_CONFIG (address 2B5h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2B5	AUTOCOLL configuration		If Random UID is disabled (EEPROM address 0x2CB), the content of these addresses is used to generate a Fixed UID. The order is byte 0, Byte 1, Byte 2; Byte3 - which is the first NFCID1 byte - is fixed to 08h, the check byte is calculated automatically
		23:16	Byte2
		15:8	Byte1:
		7:0	Byte0:

9.14.2.143 SEL_RES (02B8h)

Table 248. SEL_RES (address 2B8h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2B8	AUTOCOLL configuration	7:0	Response to Select: SAK

9.14.2.144 FELICA_POLL_RES (02B9h)

The FeliCa response is configured by 18 bytes.

Table 249. FELICA_POLL_RES (address 02B9) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2B9	AUTOCOLL configuration	15:0	FeliCa polling response: shall be 01h, FEh (2 bytes)
2BB		47:0	FeliCa polling response: NFCID2 (6 bytes)
2C1		63:0	FeliCa polling response: PAD (8 bytes)
2C9		15:0	FeliCa polling response: system code (2 bytes)

9.14.2.145 RANDOM_UID_ENABLE (02CBh)

Table 250. RANDOM_UID_ENABLE (address 2CBh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2CB	RFU	7:1	-
	Random UID Enable	0	0: Use UID stored in EEPROM 1: Randomly generate the UID in which the first byte is fixed and the remaining 3 bytes are random A new random number is generated after each RF-OFF to RF-ON.

9.14.2.146 MFC_AUTH_TIMEOUT (02CCh)

Table 251. MFC_AUTH_TIMEOUT (address 2CCh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2CC	RFU	15:0	Timeout value in micro seconds used for Auth1 and Auth2 stages during MIFARE Classic Authenticate

9.14.2.147 RSSI_TIMER (02DAh)

Configuration for Card Emulation mode only.

Table 252. RSSI_TIMER (address 2DAh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2DA	RSSI_TIMER	15:0	Default: 423

9.14.2.148 RSSI_TIMER_FIRST_PERIOD (02DCh)

Table 253. RSSI_TIMER_FIRST_PERIOD (address 2DCh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2DC	RSSI	15:0	First period duration after Rffield ON. Unit is 128/fc (106 kHz) if set to 0 it means that feature is not used 0D2 => ~2 ms

9.14.2.149 RSSI_CTRL_00_AB (02DEh)

Table 254. RSSI_CTRL_00_AB (address 2DEh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2DE	RSSI	7:6	Bits [6:7] = RFU
		5:0	Bits [0:5] = (APC_ID_REF_AB) ID of APC_TX entry that is equiv to RSSI = 0 (for Type AB)

9.14.2.150 RSSI_NB_ENTRIES_AB (02DFh)

Table 255. RSSI_NB_ENTRIES_AB (address 2DFh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2DF	RSSI	7:5	RFU
		4:0	For Initial RF ON, CEA and CEB Number of entries in RSSI lookup table (it refers to dwRssiEntryAB_01 to dwRssiEntry AB_X);

9.14.2.151 RSSI_THRESHOLD_PHASE_TABLE (02E0h)

Table 256. RSSI_THRESHOLD_PHASE_TABLE (address 2E0h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2E0	wRssiThresholdF_01	15:0	bit[0:12] - RSSI Value bit[13:15] - RFU Note: dwRssiEntryAB_00 = 0 (not in EEPROM) Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2)
2E2	ArbPhaseF_01	15:0	wArbPhaseF_xx: Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2)
	RssiThresholdF_02	15:0	
	ArbPhaseF_02	15:0	
	RssiThresholdF_03	15:0	
	ArbPhaseF_03	15:0	
	RssiThresholdF_04	15:0	
	ArbPhaseF_04	15:0	
	RssiThresholdF_05	15:0	
	ArbPhaseF_05	15:0	

Table 256. RSSI_THRESHOLD_PHASE_TABLE (address 2E0h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
	RssiThresholdF_06	15:0	
	ArbPhaseF_06	15:0	
	RssiThresholdF_07	15:0	
	ArbPhaseF_07	15:0	
	RssiThresholdF_08	15:0	
	ArbPhaseF_08	15:0	
	RssiThresholdF_09	15:0	
	ArbPhaseF_09	15:0	
	RssiThresholdF_0A	15:0	
	ArbPhaseF_0A	15:0	
	RssiThresholdF_0B	15:0	
	ArbPhaseF_0B	15:0	
	RssiThresholdF_0C	15:0	
	ArbPhaseF_0C	15:0	
	RssiThresholdF_0D	15:0	
	ArbPhaseF_0D	15:0	
	RssiThresholdF_0E	15:0	
	ArbPhaseF_0E	15:0	
	RssiThresholdF_0F	15:0	
	ArbPhaseF_0F	15:0	
	RssiThresholdF_10	15:0	
	ArbPhaseF_10	15:0	
	RssiThresholdF_11	15:0	
	ArbPhaseF_11	15:0	
	RssiThresholdF_12	15:0	
	ArbPhaseF_12	15:0	
	RssiThresholdF_13	15:0	
	ArbPhaseF_13	15:0	
	RssiThresholdF_14	15:0	
	ArbPhaseF_14	15:0	
	RssiThresholdF_15	15:0	
	ArbPhaseF_15	15:0	
	RssiThresholdF_16	15:0	
	ArbPhaseF_16	15:0	
	RssiThresholdF_17	15:0	
	ArbPhaseF_17	15:0	

Table 256. RSSI_THRESHOLD_PHASE_TABLE (address 2E0h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
	RssiThresholdF_18	15:0	
	ArbPhaseF_18	15:0	

9.14.2.152 TX_PARAM_ENTRY_TABLE (03A2h)

Table 257. TX_PARAM_ENTRY_TABLE (address 3A2h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
3A2	TxParamEntry_00_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_00_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_00_Tx2	7:0	Scaling factor for TX1 and TX2
3A5	TxParamEntry_01_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_01_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_01_Tx2	7:0	Scaling factor for TX1 and TX2
3A8	TxParamEntry_02_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_02_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_02_Tx2	7:0	Scaling factor for TX1 and TX2
3AB	TxParamEntry_03_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver

Table 257. TX_PARAM_ENTRY_TABLE (address 3A2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_03_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_03_Tx2	7:0	Scaling factor for TX1 and TX2
3AE	TxParamEntry_04_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_04_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_04_Tx2	7:0	Scaling factor for TX1 and TX2
3B1	TxParamEntry_05_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_05_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_05_Tx2	7:0	Scaling factor for TX1 and TX2
3B4	TxParamEntry_06_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_06_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_06_Tx2	7:0	Scaling factor for TX1 and TX2
3B7	TxParamEntry_07_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver

Table 257. TX_PARAM_ENTRY_TABLE (address 3A2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_07_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_07_Tx2	7:0	Scaling factor for TX1 and TX2
3BA	TxParamEntry_08_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_08_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_08_Tx2	7:0	Scaling factor for TX1 and TX2
3BD	TxParamEntry_09_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_09_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_09_Tx2	7:0	Scaling factor for TX1 and TX2
3C1	TxParamEntry_0A_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_0A_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_0A_Tx2	7:0	Scaling factor for TX1 and TX2
3C3	TxParamEntry_0B_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver

Table 257. TX_PARAM_ENTRY_TABLE (address 3A2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_0B_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_0B_Tx2	7:0	Scaling factor for TX1 and TX2

9.14.2.153 LPCD_AVG_SAMPLES (0492h)

Configuration for the Switch mode LPCD

Table 258. LPCD_AVG_SAMPLES (address 0492h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
492	LPCD setting	7:0	Defining how many samples of the I and Q values are used for the averaging. Average of samples in power of 2 0->1 sample 1->2 samples 2->4 samples 3->8 samples 4->16 samples 5-> 32 samples 6-> 64 samples

9.14.2.154 LPCD_RSSI_TARGET (0494h)

Table 259. LPCD_RSSI_TARGET (address 0494h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
494	RFU	15:10	
	LPCD setting	9:0	This value is used for the LPCD as DGRM_RSSI_TARGET. Typically the same values as for Type A106 LOAD_RF_CONFIGURATION(0x0D) (DGRM_RSSI register) are used.

9.14.2.155 LPCD_RSSI_HYST (0496h)

Table 260. LPCD_RSSI_HYST (address 0496h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
496	LPCD setting	7:0	This value is used for the LPCD as DGRM_RSSI_HYST Typically the same values as for Type A106 LOAD_RF_CONFIGURATION(0x0D) (DGRM_RSSI register) are used

9.14.2.156 LPCD_CONFIG (0497h)

Table 261. LPCD_CONFIG (address 0497h) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
497	RFU	15:6	-
		5	Immediate RF OFF before TXLDO shutdown to save power 0 - Disable 1 - Enable
		4	VDDPA fast discharge 0 - Disable 1 - Enable
		3	TX Drivers 0 - Enable Single driver 1 - Enable both drivers
	Acquisition channels:	2:0	0:1 = RFU 2 = Magnitude 3 = I and Q 4 =M, I and Q 5:7 = RFU

9.14.2.157 LPCD_THRESHOLD_COARSE (049Ah)

Table 262. LPCD_THRESHOLD_COARSE (address 049Ah) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
49A	LPCD Q channel threshold	31:16	ADC LSB granularity of threshold depends on avg_samples_meas value 5: unit 1/32; 4: unit 1/16; 3: unit 1/8; 2: unit 1/4; 1: unit 1/2; 0: unit 1
	LPCD I channel threshold	0:15	ADC LSB granularity of threshold depends on avg_samples_meas value 5: unit 1/32; 4: unit 1/16; 3: unit 1/8; 2: unit 1/4; 1: unit 1/2; 0: unit 1

Note: *If the difference between the measured value and the reference is greater than the threshold on either channels, then a card is detected.*

9.14.2.158 WAIT_RX_SETTLE (04ABh)

Table 263. WAIT_RX_SETTLE (address 04ABh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
4AB	LPCD Delay	7:0	Delay between Field-On and starting ADC data averaging for the LPCD. Value in us, default 14h = 20us

9.14.2.159 LPCD_VDDPA (04AFh)

Table 264. LPCD_VDDPA (address 04AFh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
4AF	VDDPA voltage during LPCD when DC-DC (internal or external) or external power source is used to feed TXLDO	7:0	TXLDO output voltage: 0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

9.14.2.160 ULPCD_VDDPA_CTRL (04BFh)

Table 265. ULPCD_VDDPA_CTRL (address 4BFh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
	RFU	15:9	-
	LDO_VDDPA_ VOUT_SEL	8:3	TXLDO output voltage during ULPCD polling VDDPA_1V50 /* 0x00 */ VDDPA_1V60, /* 0x01 */ VDDPA_1V70, /* 0x02 */ VDDPA_1V80, /* 0x03 */ VDDPA_1V90, /* 0x04 */ VDDPA_2V00, /* 0x05 */ VDDPA_2V10, /* 0x06 */ VDDPA_2V20, /* 0x07 */ VDDPA_2V30, /* 0x08 */ VDDPA_2V40, /* 0x09 */ VDDPA_2V50, /* 0x0A */ VDDPA_2V60, /* 0x0B */ VDDPA_2V70, /* 0x0C */ VDDPA_2V80, /* 0x0D */ VDDPA_2V90, /* 0x0E */ VDDPA_3V00, /* 0x0F */ VDDPA_3V10, /* 0x10 */ VDDPA_3V20, /* 0x11 */ VDDPA_3V30, /* 0x12 */ VDDPA_3V40, /* 0x13 */ VDDPA_3V50, /* 0x14 */ VDDPA_3V60, /* 0x15 */ VDDPA_3V70, /* 0x16 */ VDDPA_3V80, /* 0x17 */ VDDPA_3V90, /* 0x18 */ VDDPA_4V00, /* 0x19 */ VDDPA_4V10, /* 0x1A */ VDDPA_4V20, /* 0x1B */ VDDPA_4V30, /* 0x1C */ VDDPA_4V40, /* 0x1D */ VDDPA_4V50, /* 0x1E */ VDDPA_4V60, /* 0x1F */ VDDPA_4V70, /* 0x20 */ VDDPA_4V80, /* 0x21 */ VDDPA_4V90, /* 0x22 */ VDDPA_5V00, /* 0x23 */ VDDPA_5V10, /* 0x24 */ VDDPA_5V20, /* 0x25 */ VDDPA_5V30, /* 0x26 */ VDDPA_5V40, /* 0x27 */ VDDPA_5V50, /* 0x28 */ VDDPA_5V60, /* 0x29 */ VDDPA_5V70, /* 0x2A */

Table 265. ULPCD_VDDPA_CTRL (address 4BFh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
4BF	RFU	2:0	-

9.14.2.161 ULPCD_TIMING_CTRL (04C2h)

Table 266. ULPCD_TIMING_CTRL (address 4C2h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4C2	RFON_GUARD_TIME	7:4	RFON guard time: (RFON_GUARD_TIME + 2) * LFO-Freq (380 kHz) Guard time: Time between RF-ON and first sampling of data
	RFU	3:0	-

9.14.2.162 ULPCD_VOLTAGE_CTRL (04C6h)

Table 267. ULPCD_VOLTAGE_CTRL (address 4C6h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4C6	ULPCD configuration	7:5	RFU
		4:2	RFU
		1	TX_SUPPLY by VUP_TX 0: VUP externally supplied (2.8 V to 6.0 V) 1: VUP supplied by PN7642 itself (pin VUP_TX connected to VBAT/VBATPWR)
		0	RFU

9.14.2.163 ULPCD_RSSI_GUARD_TIME (04C9h)

Table 268. ULPCD_RSSI_GUARD_TIME (address 4C9h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4C9	ULPCD RSSI sampling guard time	15	RFU
		14:0	This is the time between consecutive RSSI samples: Range: 0 - 127 in micro seconds

9.14.2.164 ULPCD_RSSI_SAMPLE_CFG (04CAh)

Table 269. ULPCD_RSSI_SAMPLE_CFG (address 4CAh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4CA	ULPCD configuration	7:0	Number of RSSI Samples which are internally averaged: 0: 4 samples, 1: 8 samples 2: 16 samples 3: 32 samples

9.14.2.165 ULPCD_THRESH_LVL(04CBh)

Table 270. ULPCD_THRESH_LVL (address 4CBh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4CB	ULPCD configuration	8:0	RSSI Threshold level Range 0 - 31 If the difference between the measured RSSI value and the reference (which is derived during calibration) is greater than the threshold, then a card is detected.

9.14.2.166 ULPCD_GPIO3 (04CCh)

Table 271. ULPCD_GPIO3 (address 4CCh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4CC	RFU	7:1	-
4CC	ULPCD GPIO3 configuration	0	GPIO3 abort polarity configuration. If PN7642 is using the ULPCD, GPIO3 cannot be used for any other purpose than aborting the ULPCD. 1: high-level aborts ULPCD 0: low-level aborts ULPCD

9.14.2.167 TXIRQ_GuardTime (0559h)

Table 272. TXIRQ_GuardTime (address 0559) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
559	TXIRQ_Guard Time	31:0	0 - Disabled 0x1-0xFFFFF (Enabled - 1 unit corresponds to 1 us) Maximum timeout of 1.048 s

9.14.2.168 FDT_default_val (055Dh)

Table 273. FDT_default_val (address 055D) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
55D	FDT_default_val	31:0	0x00 - Disabled others - enabled (1 unit is 18.86us) Default fixed to 5.5 secs

9.14.2.169 RXIRQ_GuardTime (0561h)

Table 274. RXIRQ_GuardTime (address 0561h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
55D	RXIRQ_Guard Time	31:0	0x00 Disabled 0x1-0xFFFFF (Enabled - 1 unit corresponds to 1 us) Maximum timeout of 1.048 s Default value = 0xF4240 (1 s)

9.14.2.170 NFCLD_RFLD_Valid (006D3h)

Table 275. NFCLD_RFLD_Valid (address 06D3h) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
6D3	RFU	7:1	-
	RFLD_ CALIBRATE	0	This bit allows to calibrate the RFLD / NFCLD. This calibration is required only once in the lifetime of the chip for increased RFLD / NFCLD accuracy, independent from the value of this bit (0 or 1). Clearing this bit (0) will calibrate the RFLD /RFLD during the next boot-up, precondition for the proper calibration is an unloaded condition and no external field applied. After calibration this bit is set (1) and indicates that the RFLD /RFLD Threshold is a valid data.

9.14.2.171 CurrentSensorTrimConfig (0ABCh)

Table 276. CurrentSensorTrimConfig (address 0CACh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
ABC	RFU	7:1	-
	Current_Sensor_ Calib_Bypass	0	1: current sensor calibration offset is used by DPC; 0: Current sensor calibration offset is bypassed by DPC

Note: *The default value should only be modified for debug purpose.*

9.14.2.172 CORRECTION_ENTRY_TABLE (0BADh)

Table 277. CORRECTION_ENTRY_TABLE (address 0BADh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
0BAD	sCorrection_Entry0	15:0	The correction that is applied when lookup table based shaping with scaling is enabled. Range is -128 to +127, sCorrection_Entry0 corresponds to correction applied at VDDPA = 1V5, Correction_Entry42 corresponds to correction applied at VDDPA = 5V7 For each entry: BYTE 0: Bits[7:0] = define the correction which is applied for ASK100 BYTE 1: Bits[15:8] = define the correction which is applied for ASK10
BAF	sCorrection_Entry1	15:0	
BB1	sCorrection_Entry2	15:0	
BB3	sCorrection_Entry3	15:0	
BB5	sCorrection_Entry4	15:0	
BB7	sCorrection_Entry5	15:0	

Table 277. CORRECTION_ENTRY_TABLE (address 0BADh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
BB9	sCorrection_Entry6	15:0	
BBB	sCorrection_Entry7	15:0	
BBD	sCorrection_Entry8	15:0	
BBF	sCorrection_Entry9	15:0	
BC1	sCorrection_Entry10	15:0	
BC3	sCorrection_Entry11	15:0	
BC5	sCorrection_Entry12	15:0	
BC7	sCorrection_Entry13	15:0	
BC9	sCorrection_Entry14	15:0	
BCB	sCorrection_Entry15	15:0	
BCD	sCorrection_Entry16	15:0	
BCF	sCorrection_Entry17	15:0	
BD1	sCorrection_Entry18	15:0	
BD3	sCorrection_Entry19	15:0	
BD5	sCorrection_Entry20	15:0	
BD7	sCorrection_Entry21	15:0	
BD9	sCorrection_Entry22	15:0	
BDB	sCorrection_Entry23	15:0	
BDD	sCorrection_Entry24	15:0	
BDF	sCorrection_Entry25	15:0	
BE1	sCorrection_Entry26	15:0	
BE3	sCorrection_Entry27	15:0	
BE5	sCorrection_Entry28	15:0	
BE7	sCorrection_Entry29	15:0	
BE9	sCorrection_Entry30	15:0	
BEB	sCorrection_Entry31	15:0	
BED	sCorrection_Entry32	15:0	
BEF	sCorrection_Entry33	15:0	
BF1	sCorrection_Entry34	15:0	
BF3	sCorrection_Entry35	15:0	
BF5	sCorrection_Entry36	15:0	
BF7	sCorrection_Entry37	15:0	
BF9	sCorrection_Entry38	15:0	
BFB	sCorrection_Entry39	15:0	
BFD	sCorrection_Entry40	15:0	
BFF	sCorrection_Entry41	15:0	

Table 277. CORRECTION_ENTRY_TABLE (address 0BADh) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
C01	sCorrection_Entry42	15:0	

9.14.2.173 RTRANS_FTRANS_TABLE (0C03h)

Table 278. RTRANS_FTRANS_TABLE (address C03h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
C03	RTRANS0	31:0	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
C07	RTRANS1	31:0	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
C0B	RTRANS2	31:0	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
C0F	RTRANS3	31:0	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
C13	FTRANS0	31:0	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
C17	FTRANS1	31:0	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
C1B	FTRANS2	31:0	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
C1F	FTRANS3	31:0	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
C23	RTRANS0	31:0	These values apply in case EDGE_STYLE = 1 is configured for the rising edge
C27	RTRANS1	31:0	These values apply in case EDGE_STYLE = 1 is configured for the rising edge
C2B	RTRANS2	31:0	These values apply in case EDGE_STYLE = 1 is configured for the rising edge
C2F	RTRANS03	31:0	These values apply in case EDGE_STYLE = 1 is configured for the rising edge
C33	FTRANS0	31:0	These values apply in case EDGE_STYLE = 1 is configured for the falling edge
C37	FTRANS1	31:0	These values apply in case EDGE_STYLE = 1 is configured for the falling edge
C3B	FTRANS2	31:0	These values apply in case EDGE_STYLE = 1 is configured for the falling edge
C3F	FTRANS3	31:0	These values apply in case EDGE_STYLE = 1 is configured for the falling edge
C43	RTRANS0	31:0	These values apply in case EDGE_STYLE = 2 is configured for the rising edge
C47	RTRANS1	31:0	These values apply in case EDGE_STYLE = 2 is configured for the rising edge
C4B	RTRANS2	31:0	These values apply in case EDGE_STYLE = 2 is configured for the rising edge
C4F	RTRANS03	31:0	These values apply in case EDGE_STYLE = 2 is configured for the rising edge
C53	FTRANS0	31:0	These values apply in case EDGE_STYLE = 2 is configured for the falling edge
C57	FTRANS1	31:0	These values apply in case EDGE_STYLE = 2 is configured for the falling edge
C5B	FTRANS2	31:0	These values apply in case EDGE_STYLE = 2 is configured for the falling edge
C5F	FTRANS3	31:0	These values apply in case EDGE_STYLE = 2 is configured for the falling edge
C63	RTRANS0	31:0	These values apply in case EDGE_STYLE = 3 is configured for the rising edge
C67	RTRANS1	31:0	These values apply in case EDGE_STYLE = 3 is configured for the rising edge
C6B	RTRANS2	31:0	These values apply in case EDGE_STYLE = 3 is configured for the rising edge
C6F	RTRANS03	31:0	These values apply in case EDGE_STYLE = 3 is configured for the rising edge
C73	FTRANS0	31:0	These values apply in case EDGE_STYLE = 3 is configured for the falling edge
C77	FTRANS1	31:0	These values apply in case EDGE_STYLE = 3 is configured for the falling edge

Table 278. RTRANS_FTRANS_TABLE (address C03h) EEPROM configuration bit description*...continued*

Addres (hex)	Function	Bit	Description
C7B	FTRANS2	31:0	These values apply in case EDGE_STYLE = 3 is configured for the falling edge
C7F	FTRANS3	31:0	These values apply in case EDGE_STYLE = 3 is configured for the falling edge

This table applies only, if the transmitter shaping configuration is (EDGE_TYPE_xx) 4, 5, or 6.

Which of the entries RTRANS0..3 (rising transition) / FTRANS0..3 (falling transition) is applied, is defined by the EDGE_STYLE.

9.14.2.174 USER_DATA (0D2Dh)

Table 279. USER_DATA (0D2Dh) EEPROM configuration bit description

available only from FW 2.5 onwards

Addres (hex)	Function	Bit	Description
0D2D	USER_DATA Byte1	7:0	Custom defined R/W user data. Content does not have any impact on the functionality of the device. Note that frequent (e.g. automatic triggered) R/W cycles to this DWORD have an impact on the lifetime of the EEPROM as described in the chapter "EEPROM characteristics". ATTENTION: Any user data will be erased during a Firmware update.
	USER_DATA Byte2	7:0	
	USER_DATA Byte3	7:0	
	USER_DATA Byte4	7:0	
	USER_DATA Byte5	7:0	
	USER_DATA Byte6	7:0	
	USER_DATA Byte7	7:0	
	USER_DATA Byte8	7:0	
	USER_DATA Byte9	7:0	
	USER_DATA Byte10	7:0	
	USER_DATA Byte11	7:0	
	USER_DATA Byte12	7:0	
	USER_DATA Byte13	7:0	
	USER_DATA Byte14	7:0	
	USER_DATA Byte15	7:0	

Table 279. USER_DATA (0D2Dh) EEPROM configuration bit description*...continued*

available only from FW 2.5 onwards

Addres (hex)	Function	Bit	Description
	USER_DATA Byte16	7:0	

9.14.2.175 CFG_NOV_CAL (0C83h)

TX non-overlap feature - defines the non-overlap time of TX1, TX2.

Table 280. CFG_NOV_CAL (address 0083h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
1	RFU	7:2	-
	CALIBRATION_ TYPE	1:0	00 = No calibration performed, needs to be updated to 01 or 10 before the first RF on of the chip is performed 01 = Enable FW calibration after every cold boot 10 = Use calibration value coming from EEPROM NOV_CAL_VAL1, NOV_CAL_VAL2 **(Default)** 11 = RFU

9.14.2.176 NOV_CAL_VAL1 (0C84h)

Table 281. NOV_CAL_VAL1 (address 0C84h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
1	VddpaCalVal1	7:0	It defines the VDDPA value that FW uses to perform NOV calibration group #1. value = 03h (1.8 V) value = 0Dh (2.8 V) See "TxLdoVddpaHigh" parameter for list of voltage

9.14.2.177 NOV_CAL_VAL2 (0C85h)

Table 282. NOV_CAL_VAL2 (0C85h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
1	VddpaCalVal2	7:0	It defines the VDDPA value that FW uses to perform NOV calibration group #2. default value = 15h (3.6 V) default value = 24h (5.1 V) See "TxLdoVddpaHigh" parameter for list of voltage

9.14.2.178 NOV_CAL_THRESHOLD (0C86h)

Table 283. NOV_CAL_THRESHOLD (address 0C86h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
1	CfgThreshold	7:0	It defines VDDPA threshold that FW will use to select Group #1 or Group #2 NOV offset values.

Table 283. NOV_CAL_THRESHOLD (address 0C86h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
			default value = 08h (2.3 V) default value = 16h (3.7 V) See "TxLdoVddpaHigh" parameter for list of voltage

9.14.2.179 NOV_CAL_OFFSET1 (0C87h)

Table 284. NOV_CAL_OFFSET1 (address 0C87h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
C87	RFU	31:29	
	UserOffsets1	28:0	It defines user static offsets applied if CFG_NOV_CAL[1:0] = 10b bits[04:00] Group #1 (CfgThreshold to VDDPA max), offset_3l bits[12:08] Group #1 (CfgThreshold to VDDPA max), offset_3l_p2 bits[20:16] Group #1 (CfgThreshold to VDDPA max), offset_2l<0> bits[28:24] Group #1 (CfgThreshold to VDDPA max), offset_2l<1>

9.14.2.180 NOV_CAL_OFFSET2 (0C8Bh)

Table 285. NOV_CAL_OFFSET1 (address 0C8Bh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
C8B	RFU	31:29	
	UserOffsets2	28:0	It defines user static offsets applied if CFG_NOV_CAL1:0] = 10b bits[04:00] Group #2 (CfgThreshold to VDDPA max), offset_3l bits[12:08] Group #2 (CfgThreshold to VDDPA max), offset_3l_p2 bits[20:16] Group #2 (CfgThreshold to VDDPA max), offset_2l<0> bits[28:24] Group #2 (CfgThreshold to VDDPA max), offset_2l<1>

9.14.2.181 VDDPA_DISCHARGE (0C8Fh)

Table 286. VDDPA_DISCHARGE (address 0C8Fh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
C8F	RFU	7:1	RFU
	EnableFast VDDPADischarge	0	1 - Enables fast discharge of VDDPA by setting VDDPA=5.7 and then to 1.5 V, during RF OFF (default) 0 - Disables fast discharge of VDDPA by setting VDDPA=5.7 and then to 1.5 V, during RF OFF

9.14.2.182 ARC_RM_A106_FDT (0C9Dh)

This is the setting for type A-106.

Table 287. ARC_RM_A106_FDT (address 0C9Dh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CA5	RM_RX_ARC_ FDT_4	15:0	Bit[15]: RFU Bit [14]: Has to be always "0" Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
CA3	RM_RX_ARC_ FDT_3	15:0	Bit[15]: RFU Bit [14]: Has to be always "0" Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
CA1	RM_RX_ARC_ FDT_2	15:0	Bit[15]: RFU Bit [14]: Has to be always "0" Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
C9F	RM_RX_ARC_ FDT_1	15:0	Bit[15]: RFU Bit [14]: Has to be always "0" Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
C9D	RM_RX_ARC_ FDT_0	15:0	Bit[15]: RFU Bit [14]: Has to be always "0" Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *For ISO14443-A: In case ARC is disabled, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default))*

Note: *For ISO14443-A: In case Bit[15] is configured to 0, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default)) if the ARC is enabled.*

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

9.14.2.183 Tx_Symbol23_Mod_Reg_BR_53 (0CC5h)

Table 288. Tx_Symbol23_Mod_Reg_BR_53 (0CC5Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CC5	15693_BR_CFG	31:0	CLIF_TX_SYMBOL23_MOD_REG value loaded for 15693 BR 53 kbit/s

9.14.2.184 Tx_Data_Mod_Reg_BR_53 (0CC9h)

Table 289. Tx_Data_Mod_Reg_BR_53 (0CC9Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CC9	15693_BR_CFG	31:0	CLIF_TX_Data_MOD_REG value loaded for 15693 BR 53 kbit/s

9.14.2.185 Tx_Symbol23_Mod_Reg_BR_106 (0CCDh)

Table 290. Tx_Symbol23_Mod_Reg_BR_106 (0CCDEh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CCD	15693_BR_CFG	31:0	CLIF_TX_Symbol23_MOD_REG value loaded for 15693 BR 106 kbit/s

9.14.2.186 Tx_Data_Mod_Reg_BR_106 (0CD1h)

Table 291. Tx_Data_Mod_Reg_BR_106 (0CD1Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CD1	15693_BR_CFG	31:0	CLIF_TX_Data_MOD_REG value loaded for 15693 BR 106 kbit/s

9.14.2.187 Tx_Symbol23_Mod_Reg_BR_212 (0CD5h)

Table 292. Tx_Symbol23_Mod_Reg_BR_212 (0CD5Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CD5	15693_BR_CFG	31:0	CLIF_TX_Symbol23_MOD_REG value loaded for 15693 BR 212 kbit/s

9.14.2.188 Tx_Data_Mod_Reg_BR_212 (0CD9h)

Table 293. Tx_Data_Mod_Reg_BR_212 (0CD9Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CD9	15693_BR_CFG	31:0	CLIF_TX_Data_MOD_REG value loaded for 15693 BR 212 kbit/s

9.14.2.189 CardModeUltraLowPowerEnabled (0CDFh)

Table 294. CardModeUltraLowPowerEnabled (address 00DFh) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
CDF	RFU	7:1	-
	CALIBRATION_ TYPE	0	Enable Ultra Low-Power standby for CardMode.

Note: *Note: When bit 0 = 1, Switch Standby instruction with ULP mode cannot be used*

9.14.2.190 LPCD_EXT_DCDC_ENABLE (0CE0h)

Table 295. LPCD_EXT_DCDC_ENABLE (0CE0h) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
CE0	up to FW 2.02: RFU	7:0	-
	from FW 2.03. onwards: RFU	7:1	-
	from FW 2.03. onwards: GPIO1 configuration for LPCD	0	Enables the use of GPIO to wake up EXT DC-DC from power saving during LPCD. This function is not available for the ULPCD.

9.14.2.191 LPCD_EXT_DCDC_DELAY_TO_ON (0CE1h)

Table 296. LPCD_EXT_DCDC_DELAY_TO_ON (0CE1h) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
CE1	up to FW 2.02: RFU	7:0	-
	from FW 2.03. onwards: GPIO1 configuration for LPCD	7:0	The value defines the time between setting GPIO1 until Field is switched on. Time in us * 8 to wait for the Ext DC-DC to be started

9.14.2.192 LPCD_EXT_DCDC_DELAY_TO_OFF (0CE2h)

Table 297. LPCD_EXT_DCDC_DELAY_TO_OFF (0CE2h) EEPROM configuration register bit description

Addres (hex)	Function	Bit	Description
CE2	until FW2.02: RFU	7:0	-
	from FW 2.03. onwards:	7:0	Value defines the time between Field Off and clear GPIO1. Time in us * 8 to wait for the Ext DC-DC to be shut down

Table 297. LPCD_EXT_DCDC_DELAY_TO_OFF (0CE2h) EEPROM configuration register bit description...*continued*

Addres (hex)	Function	Bit	Description
	GPIO1 configuration for LPCD		

9.14.2.193 RxGuardTO_Multiple (0CE8h)

Table 298. RxGuardTO_Multiple (address 00CE8h) EEPROM configuration bit description

Addres (hex)	Function	Bit	Description
0CE8	RxGuardTO_ Multiple	7:0	This field configures the RxGuard Timeout configuration in multiple of Timeout configured using RXIRQ_GuardTime EEPROM Field (Address 0561h). Default value is 1. Indicating RX_TIMEOUT shall be triggered due to expiry of RXIRQ_GUARD first time only.

10 Limiting values

Table 299. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(VUP\_TX)}$	supply voltage on pin VUP_TX	-	-0.3	6.3	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT	-	-0.3	5.8	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO	on pin VDDIO, power supply for host interface and GPIOs	-0.3	3.8	V
$V_{DD(GPIO\_x)}$	input voltage on pin used as GPIO	-	-0.3	3.8	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA	maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated	-	6.0	V
$V_{i(RXP)}$	input voltage on pin RXP	-	-0.3	+ 2.0	V
$V_{i(RXN)}$	input voltage on pin RXN	-	-0.3	+ 2.0	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1]	-2000	2000	V
		charge device model (CDM)[2]	-500	+500	V
$T_{j(max)}$	junction temperature	-	-	125	°C
T_{stg}	storage temperature	no supply voltage applied	-55	+150	°C

[1] According to ANSI/ESDA/JEDEC JS-001
[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime.

Product might not behave according to specification.

11 Characteristics

This chapter describes the electrical characteristics for the usage of the product.

Functionality according to this specification and compliancy to referred standards is guaranteed if the device is operated within the limits.

For further information, refer to the PQP (product qualification package) which summarizes the results of the characterization and qualification performed.

11.1 Thermal characteristics

Table 300. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB, transmitter output current up to 350 mA	-40	+25	+85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA=3.6 V	-40	+25	+105	°C

Table 301. Thermal characteristics VFBGA64 package

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB, package VFBGA64	53	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	-	22	K/W

Table 302. Junction Temperature

Symbol	Parameter	Conditions	Min	Max	Unit
T_{j_max}	maximum junction temperature	-	-	+125	°C

Table 303. Thermal Shutdown Temperature

Symbol	Parameter	Conditions	Typ	Unit
$T_{shutdown}$	shutdown of chip due to high temperature detected by temp sensor	-	125	°C

11.2 Static characteristics

Table 304. Supply voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBAT\_PWR)}$	supply voltage on pin VBAT_PWR (DC-DC input pin)	DC-DC disabled	2.4	-	5.5	V
		DC-DC enabled	2.8	-	4.8	V
$V_{DD(VUP\_TX)}$	supply voltage on pin VUP_TX (TX_LDO input pin)	Remark: If DC-DC is used, its output $V_{DD(BOOST)}$ Min is limited to 3.1 V	2.4	-	6.0	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	-	1.5	-	5.7	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT >= VDDIO	2.4	-	5.5	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	typical 1.8 V interface supply voltage	1.62	-	1.98	V
		typical 3.3 V interface supply voltage	2.4	-	3.6	V
$V_{I(RXP)}$	input voltage on pin RXP	-	-0.5	-	1.8	V
$V_{I(RXN)}$	input voltage on pin RXN	-	-0.5	-	1.8	V
$V_{O(LDO)}$	LDO output voltage on pin PVDD_LDO		3	3.4	3.6	V

Note: The voltage on pin VDDIO must always be smaller or equal to the voltage on pin VBAT.

Note: *$V_{O(LDO)}$ is designed to supply only the peripherals of the chip. It is not allowed to use this output to supply any other "off chip" components by this output.*

Table 305. Current consumption in active mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(VBAT)}$	system supply		-	-	20	mA
$I_{DD(VDDIO)}$		This current depends on the output current of peripherals. At no time, the sum of the maximum output currents shall exceed $I_{DD(VDDIO)}$ max	-	-	30	mA
$I_{DD(BOOST\_IN)}$	DC-DC boost supply	average input current	-	-	1.0	A
		peak input current (short peak)	-	-	1.7	A
$I_{DD(VUP\_TX)}$	input supply for transmitter LDO	-	-	-	350	mA
$I_{DD(VDDPA)}$	RF power amplifier (transmitter) current	supplied via VUP_TX (TX_LDO active)	-	-	350	mA

Table 305. Current consumption in active mode*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		supplied without DC-DC and without TXLDO active	-	-	400	mA
$I_{DD(PVDD\_OUT)}$	maximum supply current of PVDD_LDO	for pin PVDD_OUT	-	-	30	mA

Table 306. Current consumption during power-saving modes

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OFF\ Plus\ Mode\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in OFF Plus mode	25 °C ambient operating temperature	-	5	-	µA
$I_{OFF\ Plus\ ULFO\ Mode\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in OFF Plus mode, ULFO active (ULPCD during RF-OFF)	25 °C ambient operating temperature	-	5	-	µA
$I_{hard\ power\ down\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in hard Power-down mode	25 °C ambient operating temperature	-	40	105	µA
$I_{standby\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in Standby mode	25 °C ambient operating temperature	-	45	110	µA
$I_{suspend\ (VBAT)}$	supply current on pin VBAT in suspend mode	25 °C ambient operating temperature	-	2.5	-	mA
$I_{ULPCD\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in ULPCD (Ultra Low-Power Card Detection) mode	25 °C ambient operating temperature, VBAT supply voltage 3.3 V, antenna matching 50 R, 3.3 V antenna supply voltage, 3x RF-on per second	-	22	-	µA
$I_{LPCD\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in LPCD (Enhanced Low-Power Card Detection with highest sensitivity) mode, without DC-DC used	25 °C ambient operating temperature, VBAT supply voltage 3.3 V, antenna matching 50 R, 3.3 V antenna supply voltage, 3x RF-on per second	-	240	-	µA

Table 307. Overcurrent detection function

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(VUP\_TX)}$	current of overcurrent detection becoming active	-	450	550	650	mA

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

Table 308. VEN pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$	0.7 * $V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$	V
V_{IL}	LOW-level input voltage		0	-	0.3 * $V_{DD(VDDIO)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{DD(VBAT)}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V	-1	-	-	µA
C_i	input capacitance		-	5	-	pF
$t_{(ULPCD\_abort)}$	VEN time required to abort ULPCD		5	-	-	ms

Table 309. GPIO input / output pins (GPIO_0 - 5, SWDIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	0.65x VDDIO	-	VDDIO+0.5	V
V_{IL}	LOW-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	- 0.5	-	0.35 × VDDIO	V
V_{OH}	HIGH-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	VDDIO - 0.4	-	VDDIO	V
V_{OH}	LOW-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	0	-	0.4	V
I_{OH}	HIGH-level output current	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	3	mA
I_{OL}	LOW-level output current	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	3	mA
I_{IH}	HIGH-level input current	2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	1	µA
I_{IL}	LOW-level input current	2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-1	-	-	µA
R_{PU}	Weak pullup resistor		40	50	62	kΩ
R_{PD}	Weak pulldown resistor		40	50	62	kΩ
C_L	Load capacitance		-	-	20	pF
C_{IN}	Input capacitance		-	-	5	pF
I_{OSH}	Short circuit current output high	1.62 <= VDDIO <= 1.98	-	-	16	mA
I_{OSH}	Short circuit current output high	2.4 <= VDDIO <= 3.6	-	-	44	mA

Table 310. GPIO output pins (UART_RX, SPI_MISO, SPIM_MISO, IRQ, PWM 0-3, AUX_1, AUX_2, AUX_3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	VDDIO - 0.4	-	VDDIO	V
V_{OH}	LOW-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	0	-	0.4	V
I_{OH}	HIGH-level output current	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	3	mA
I_{OL}	LOW-level output current	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	3	mA
R_{PU}	Weak pullup resistor		40	50	62	kΩ
R_{PD}	Weak pulldown resistor		40	50	62	kΩ
C_L	load capacitance		-	-	20	pF

Table 311. GPIO input pins (DWL_REQ, SWD_CLK, HOST_IF_SEL0, HOST_IF_SEL1, AD1, UART_CTS, SPI_SCK, UART_RTS, SPI_NSS, I^2C_ADR_BIT_0, I^3C_ADR_BIT_0, UART_TX, I^2C_ADR_BIT_1, I^3C_ADR_BIT_1, SPI_MOSI, SPIM_MOSI, SPIM_SCLK, SPIM_NSS)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	0.65x VDDIO	-	VDDIO+0.5	V
V_{IL}	LOW-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	- 0.5	-	0.35 × VDDIO	V
I_{IH}	HIGH-level input current	2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-	-	1	µA
I_{IL}	LOW-level input current	2.4 <= VDDIO <= 3.6 1.62 <= VDDIO <= 1.98	-1	-	-	µA
R_{PU}	Weak pullup resistor		40	50	62	kΩ
R_{PD}	Weak pulldown resistor		40	50	62	kΩ
C_{IN}	input capacitance		-	-	5	pF

Table 312. XTAL1, XTAL2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(p-p)}$	peak-to-peak input voltage	-	0.4	-	1.65	V
I_{IH}	HIGH-level input current	VI= 1.65 V, no power saving, active mode	-	-	5	µA

Table 312. XTAL1, XTAL2 pins *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	LOW-level input current	VI = 0 V, no power saving, active mode	-	-	1	µA
δ	duty cycle	-	35	-	65	%
$C_{i(CLK1)}$	input capacitance on pin CLK1	VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 V (p-p)	-	1	-	pF
$C_{i(CLK2)}$	input capacitance on pin CLK2	VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 V (p-p)	-	1	-	pF

Table 313. RXp, RXn pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(dyn)}$	dynamic input voltage		-	-	1.8	V
C_i	input capacitance		-	1	-	pF
Z_i	input impedance from RXN, RXP pins to VMID	Reader, card, and P2P modes	-	-	15	kΩ

Table 314. TX1, TX2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(VDDPA)}$=5.0 V; with internal VDDPA LDO	-	$V_{DD(VDDPA)}$ -150 mV	$V_{DD(VDDPA)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(VDDPA)}$=5.0 V;with internal VDDPA LDO	0	200	-	m

Table 315. VTUNE0 and VTUNE1 output pins (Tuning DAC)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{O_max}	HIGH-level maximum output voltage	connected to a variable capacitor (varicap), VDDIO = 3.3 V	-	$V_{DD(VDDIO)}$	3.65	V
V_{O_min}	LOW-level minimum output voltage	connected to a variable capacitor (varicap)	- 0.3	0	200	mV
	DAC resolution		-	-	8	bits
C_{O_LOAD}	output capacitance load of pin		0	-	4	nF

Table 316. USB pins (ATX_C (USB D+) ATX_D (USB D-))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	OFF-state output current	0 V < Vi < 3.3 V	-10	-	10	µA

Table 316. USB pins (ATX_C (USB D+) ATX_D (USB D-))*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DI}	Differential input sensitivity voltage	(D+) - (D-)	0.2	-	-	V
V_{CM}	Differential common mode voltage range	Includes V_{DI} range	0.8	-	2.5	V
$V_{th(rs)se}$	Single-ended receiver switching threshold voltage		0.8	-	2	V
V_L	low-level input voltage		0.8	-	-	V
V_{IH}	high-level input voltage		-	-	2	V
V_{OH}	high-level output voltage		3	3.3	3.6	pF
C_{trans}	transceiver capacitance	Pin to GND	-	15	-	
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	28	-	44	Ω
V_{CRS}	output signal crossover voltage		1.3	-	2	V

Table 317. I2C / I3C input pins (ATX_B pin (I^2C (SCL), I^3C (SCL))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	high-level input voltage		0.65 x $V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$ + 0.5	V
V_{IL}	low-level input voltage		0.5	-	0.35 x $V_{DD(VDDIO)}$	V
I_{IH}	high-level input current		-	-	1	µA
I_{IL}	low-level input current		-1	-	-	µA
C_{IN}	input capacitance		-	-	5	pF

Table 318. I2C / I3C output pins (ATX_A pin (I^2C (SDA), I^3C (SDA))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	$V_{DD(VDDIO)}$ = 1.62, 1.8, 1.98: I2C (I_{OH} = 14.5 mA)	0.3 x $V_{DD(VDDIO)}$	-	0.7 x $V_{DD(VDDIO)}$	V
V_{OL}	low-level output voltage	$V_{DD(VDDIO)}$ = 1.62, 1.8, 1.98: I2C (I_{OL} = 6 mA)	0	-	0.4	V
V_{OH}	high-level output voltage	$V_{DD(VDDIO)}$ = 2.4, 3.3, 3.6: I2C (I_{OH} = 13.6 mA)	0.3 x $V_{DD(VDDIO)}$	-	0.7 x $V_{DD(VDDIO)}$	V
V_{OL}	low-level output voltage	$V_{DD(VDDIO)}$ = 2.4, 3.3, 3.6: I2C (I_{OL} = 11.5 mA)	0	-	0.4	V
I_{OH}	high-level output current	$V_{DD(VDDIO)}$ = 1.62, 1.8, 1.98: I2C At 0.3 × VDDE < VOH < 0.7 × VDDE	3	-	14.5	mA
I_{OL}	low-level output current	$V_{DD(VDDIO)}$ = 1.62, 1.8, 1.98: I2C At VOL = 0.4 V	6	-	-	mA
I_{OH}	high-level output current	$V_{DD(VDDIO)}$ = 2.4, 3.3, 3.6: I2C At 0.3 × VDDE < VOH < 0.7 × VDDE	3.5	-	13.6	mA
I_{OL}	low-level output current	$V_{DD(VDDIO)}$ = 2.4, 3.3, 3.6: I2C At VOL = 0.4 V	11.5	-	-	mA
C_L	load capacitance		-	-	20	pF

Table 319. ISO AUX pins (ISO_INT_AUX, ISO_IO_AUX, ISO_CLK_AUX)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	high-level input voltage		0.65 x $V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$	V
V_{IL}	low-level input voltage		0	-	0.35 x $V_{DD(VDDIO)}$	V

Table 319. ISO AUX pins (ISO_INT_AUX, ISO_IO_AUX, ISO_CLK_AUX)*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HYS}	input hysteresis voltage		0.05 x $V_{DD(VDDIO)}$	-	-	V
V_{OH}	high-level output voltage by “medium” pullup (only in “quasi-bidirectional” mode)	IOH = –20 µA	0.7 x $V_{DD(VDDIO)}$	-	-	V
V_{OH2}	high-level output voltage by strong pullup	IOH = –0.1 mA	$V_{DD(VDDIO)}$ - 0.2	-	-	V
V_{OL}	low-level output voltage	IOL = 1.0 mA	-	-	0.3	V
V_{OL2}	low-level output voltage	IOL = 0.75 mA; 1.8 V	-	-	0.15 x $V_{DD(VDDIO)}$	V
C_{IN}	Input capacitance		-	-	5	pF

11.3 Timing characteristics

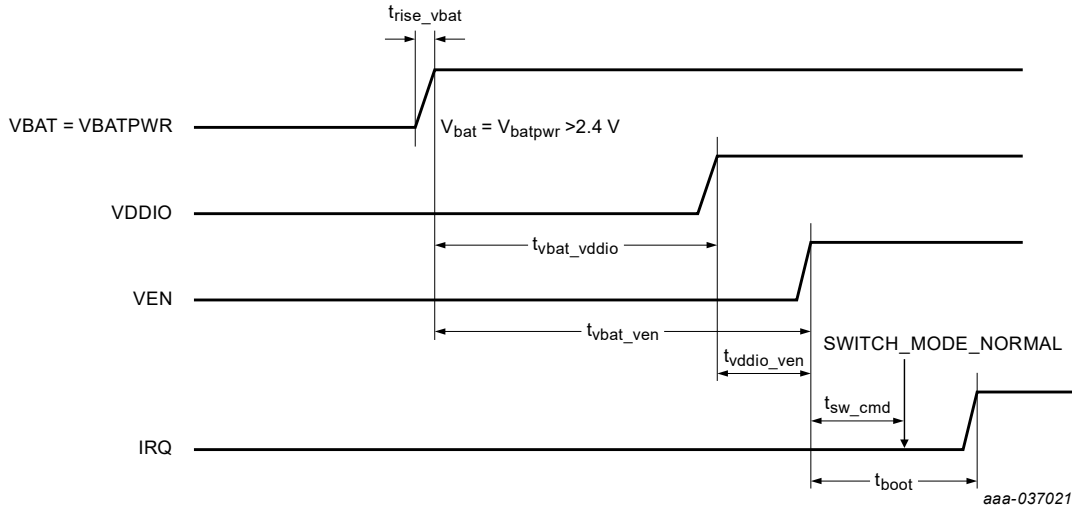


Figure 29. Startup timing

After VEN reset and tswcmd are lapsed, SWITCH_MODE_NORMAL command shall be issued to enter normal mode of operation. Recommended value of tswcmd = 500 µs.

Table 320. Power supply connection timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rise_vbat}	VBAT supply ramp	VEN = Low	0	-	2.75	V/µs
t_{vbat_vddio}	time between ramping up VBAT and ramping VDDIO	vddio condition: VBAT>2.4 V, VDDIO supply	0	500	1000	ms

Table 320. Power supply connection timing *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		(External), hpd_off_sel = x				
t_{vbat_ven}	time between ramping VBAT and VEN	vddio condition: VBAT>2.4 V, VDDIO supply (External), hpd_off_sel = x	0	500.5	1001	ms
t_{boot}	start-up time[1]	vddio condition: VBAT>2.4 V, VDDIO supply (External), hpd_off_sel = x	3.2	3.27	dependent on configuration of XTAL_CHECK_DELAY (0013h) in EEPROM. This configuration can be used to optimize the boot time for crystals which allow a fast settling. This allows to optimize the average current consumption during ULPCD and LPCD. default EEPROM configuration: 3.4	ms

[1] (PN7642 ready to receive commands on the host interface). For ULPCD and LPCD, the PN7642 indicates the ability to receive commands from a host by raising an IDLE IRQ.

Table 321. Pulse length

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(VEN)}$	on Pin VEN, pulse width to reset the chip or exit from ULPCD / Hard Power Down State	-	5	-	-	ms
$t_{(wake-up)}$	on pin GPIOx, pulse width to wake up	-	1	-	-	µs
$t_{VEN(GPIO)}$	time from VEN high to GPIO's available for use	-	100	-	-	ms

Table 322. SPI interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCKL}	SCK LOW time	33.3	-	-	ns
t_{SCKH}	SCK HIGH time	33.3	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	16.65	-	-	ns
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	16.65	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time	0	-	-	ns

Table 322. SPI interface*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
t_{NSSH}	NSS HIGH time	33.3	-	-	ns

Table 323. Timing characteristics for GPIO, UART (GPIO Low Speed), PWM (GPIO Low Speed)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	VDDIO = 1.8 V; high speed	0.8	-	1.9	ns
		VDDIO = 3.3 V; high speed	0.6	-	1.5	ns
		VDDIO = 1.8 V; fast speed	1.2	-	3.3	ns
		VDDIO = 3.3 V; fast speed	0.8	-	1.9	ns
		VDDIO = 1.8 V; medium speed	2	-	4.6	ns
		VDDIO = 3.3 V; medium speed	1.4	-	2.9	ns
		VDDIO = 1.8 V; low speed	20	-	43	ns
		VDDIO = 3.3 V; low speed	15	-	28	ns
t_f	fall time	VDDIO = 1.8 V; high speed	0.8	-	1.9	ns
		VDDIO = 3.3 V; high speed	0.6	-	1.5	ns
		VDDIO = 1.8 V; fast speed	1.2	-	3.3	ns
		VDDIO = 3.3 V; fast speed	0.8	-	1.9	ns
		VDDIO = 1.8 V; medium speed	2	-	4.6	ns
		VDDIO = 3.3 V; medium speed	1.4	-	2.9	ns
		VDDIO = 1.8 V; low speed	15	-	25	ns
		VDDIO = 3.3 V; low speed	14	-	21	ns

Table 324. Timing characteristics for ATX_, ATX_B in I^2C configuration

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	VDDIO = 1.8 V; high speed - input	18	-	35	ns

Table 324. Timing characteristics for ATX_, ATX_B in I^2C configuration*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		VDDIO = 3.3 V; high speed - input	17	-	39	ns
		VDDIO = 1.8 V; standard, fast, fast+ speed - input	68	-	120	ns
		VDDIO = 3.3 V; standard, fast, fast+ speed - input	66	-	115	ns
		VDDIO = 1.8 V; high-speed clock - output	14	-	40	ns
		VDDIO = 3.3 V; high-speed clock - output	11	-	35	ns
		VDDIO = 1.8 V; high-speed data - output	25	-	90	ns
		VDDIO = 3.3 V; high-speed data - output	15	-	90	ns
t_f	fall time	VDDIO = 1.8 V; high speed - input	18	-	35	ns
		VDDIO = 3.3 V; high speed - input	17	-	30	ns
		VDDIO = 1.8 V; standard, fast, fast+ speed - input	70	-	125	ns
		VDDIO = 3.3 V; standard, fast, fast+ speed - input	67	-	120	ns
		VDDIO = 1.8 V; high-speed clock - output	15	-	35	ns
		VDDIO = 3.3 V; high-speed clock - output	13.5	-	28	ns
		VDDIO = 1.8 V; high-speed data - output	15	-	35	ns

Table 324. Timing characteristics for ATX_, ATX_B in I^2C configuration*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		VDDIO = 3.3 V; high-speed data - output	13.5	-	28	ns

Table 325. RF_ON command timing following a previous RF_OFF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(RF\_OFF-RF\_ON)}$	RF_ON command timing	guard time between command sends for RF_OFF and command send for RF_ON, capacitors on transmitter need to be fully de-charged before RF_ON command is sent	5.1	5.6	-	ms

Table 326. I^2C timing specification: Standard, Fast Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 400 pF	0	-	0.4	MHz
t_{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 400 pF	600	-	-	ns
t_{HD} START	hold time of a (repeated) START condition	Load capacitance < 400 pF	600	-	-	ns
t_{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 400 pF	1.3	-	-	µs
t_{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 400 pF	600	-	-	ns
t_{SU} DATA	DATA set-up time	Load capacitance < 400 pF	100	-	-	ns
t_{HD} DATA	DATA hold-up time	Load capacitance < 400 pF	0	-	900	ns

Table 326. I^2C timing specification: Standard, Fast Mode*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tr_{DA}	Rise time of SDA	Load capacitance < 400 pF	30	-	250	ns
tf_{DA}	Fall time of SDA	Load capacitance < 400 pF	30	-	250	ns

Table 327. I^2C timing specification: High-Speed Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 100 pF	0	-	3.4	MHz
t_{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 100 pF	160	-	-	ns
t_{HD} START	hold time of a (repeated) START condition	Load capacitance < 100 pF	160	-	-	ns
t_{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 100 pF	160	-	-	ns
t_{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 100 pF	60	-	-	ns
t_{SU} DATA	DATA set-up time	Load capacitance < 100 pF	10	-	-	ns
t_{HD} DATA	DATA hold-up time	Load capacitance < 100 pF	0	-	-	ns
tr_{DA}	Rise time of SDA	Load capacitance < 100 pF	10	-	80	ns
tf_{DA}	Fall time of SDA	Load capacitance < 100 pF	10	-	80	ns

Table 328. I^2C timing specification: Fast + Speed Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 100 pF	0	-	1	MHz

Table 328. I^2C timing specification: Fast + Speed Mode*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 100 pF	260	-	-	ns
t_{HD} START	hold time of a (repeated) START condition	Load capacitance < 100 pF	260	-	-	ns
t_{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 100 pF	500	-	-	ns
t_{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 100 pF	260	-	-	ns
t_{SU} DATA	DATA set-up time	Load capacitance < 100 pF	50	-	-	ns
t_{HD} DATA	DATA hold-up time	Load capacitance < 100 pF	0	-	-	ns
tr_{DA}	Rise time of SDA	Load capacitance < 100 pF	-	-	120	ns
tf_{DA}	Fall time of SDA	Load capacitance < 100 pF	-	-	120	ns

Table 329. Timing characteristics for I^3C interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LOW}	Low period of SCL clock		200	-	-	ns
t_{HIGH}	High period of SCL clock		-	-	41	ns
tf_{DA}	Fall time of SDA		t_{CF}	-	12	ns
t_{CAS}	Clock after START (S) condition	ENTAS0	38.4 nano	-	1 µ	s
		ENTAS1			100 µ	s
		ENTAS2			2 mill	s
		ENTAS3			50 mill	s
t_{CBP}	Clock before STOP (P) condition		t_{CAS}min / 2	-	-	s
t_{AVAL}	BUS available condition		1	-	-	ns

Table 329. Timing characteristics for I^3C interface*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{IDLE}	BUS IDLE condition		1	-	-	ms
t_{MMLock}	Time Internal where new Controller must not drive SDA LOW		t_{AVAL}min	-	-	us

Table 330. Timing characteristics for USB interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	4	-	20	ns
t_f	fall time	10 % to 90 %	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f	-	-	10	%
V_{CRS}	output signal crossover voltage		1.3	-	2	V
t_{FEOPT}	source SE0 interval of EOP	T = 25 °C	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	T = 25 °C	-2	-	+5	ns
t_{JR1}	receiver jitter to next transition	T = 25 °C	-18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %; T = 25 °C	-9	-	+9	ns
t_{FEOPR}	receiver SE0 interval of EOP	must accept as EOP; T = 25 °C	82	-	-	ns

Table 331. Timing characteristics ISO AUX interface (ISO_INT_AUX, ISO_IO_AUX, ISO_CLK_AUX)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	output rise time at IO	VDDIO = 1.8 V; EHS = L	50	-	125	ns
	output rise time at IO	VDDIO = 3.3 V; EHS = L	32	-	86	ns
	output rise time at IO	VDDIO = 1.8 V; EHS = H	25	-	63	ns
	output rise time at IO	VDDIO = 3.3 V; EHS = H	16	-	43	ns

Table 331. Timing characteristics ISO AUX interface (ISO_INT_AUX, ISO_IO_AUX, ISO_CLK_AUX)*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	input rise time at IO	VDDIO = 1.8 V	1.2	-	3.2	ns
	input rise time at IO	VDDIO = 3.3 V	1.2	-	3.2	ns
t_f	output fall time at IO	VDDIO = 1.8 V; EHS = L	11	-	31	ns
	output fall time at IO	VDDIO = 3.3 V; EHS = L	8	-	22	ns
	output fall time at IO	VDDIO = 1.8 V; EHS = H	9	-	25	ns
	output fall time at IO	VDDIO = 3.3 V; EHS = H	6	-	16	ns
	input fall time at IO	VDDIO = 1.8 V	0.9	-	2.3	ns
	input fall time at IO	VDDIO = 3.3 V	0.9	-	2.3	ns

11.4 Clock input

Table 332. Crystal requirements for ISO/IEC14443 compliant operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC compliancy	-	27.12	-	MHz
delta f_{xtal}	crystal frequency accuracy	for full RF operating range	-40	-	+40	ppm
ESR	equivalent series resistance	-	10	30	100	Ω
C_L	load capacitance	-	6	8	10	pF
$t_{startup}$	crystal startup time	-	-	-	1	ms
P_{xtal}	crystal power dissipation	-	-	-	100	µW

Table 333. Frequency requirements for a direct clock input (no crystal)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	ISO/IEC compliancy	-	24	-	MHz
			-	32	-	
			-	48	-	
delta f_{clk}	clock frequency accuracy	for full RF operating range	-40	-	+40	ppm
φ_n	phase noise	input phase noise floor at 100 kHz offset	-	- 150	-145	dBc/Hz

Table 333. Frequency requirements for a direct clock input (no crystal) *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
φ_n	phase noise	input phase noise floor at 1 MHz offset	-	- 152	-149	dBc/Hz
V_i	Input voltage boundary	sinus signal	0	-	1.8	V
$V_{i(p-p)}$	peak-to-peak Input voltage	sinus signal	0.4	-	1.8	V
$V_{i(clk)}$	clock input voltage	square signal	0	-	1.8 +/-10%	V

11.5 EEPROM characteristics

Table 334. EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{endu(W)}$	write endurance	at ambient temperature T_a = +25 °C	100	-	-	K cycles
t_{ret}	retention time	at ambient temperature T_a =+25 °C	25	-	-	years

12 Package outline

12.1 VFBGA64 package

Table 335. Package outline VFBGA64 (SOT1307-2)

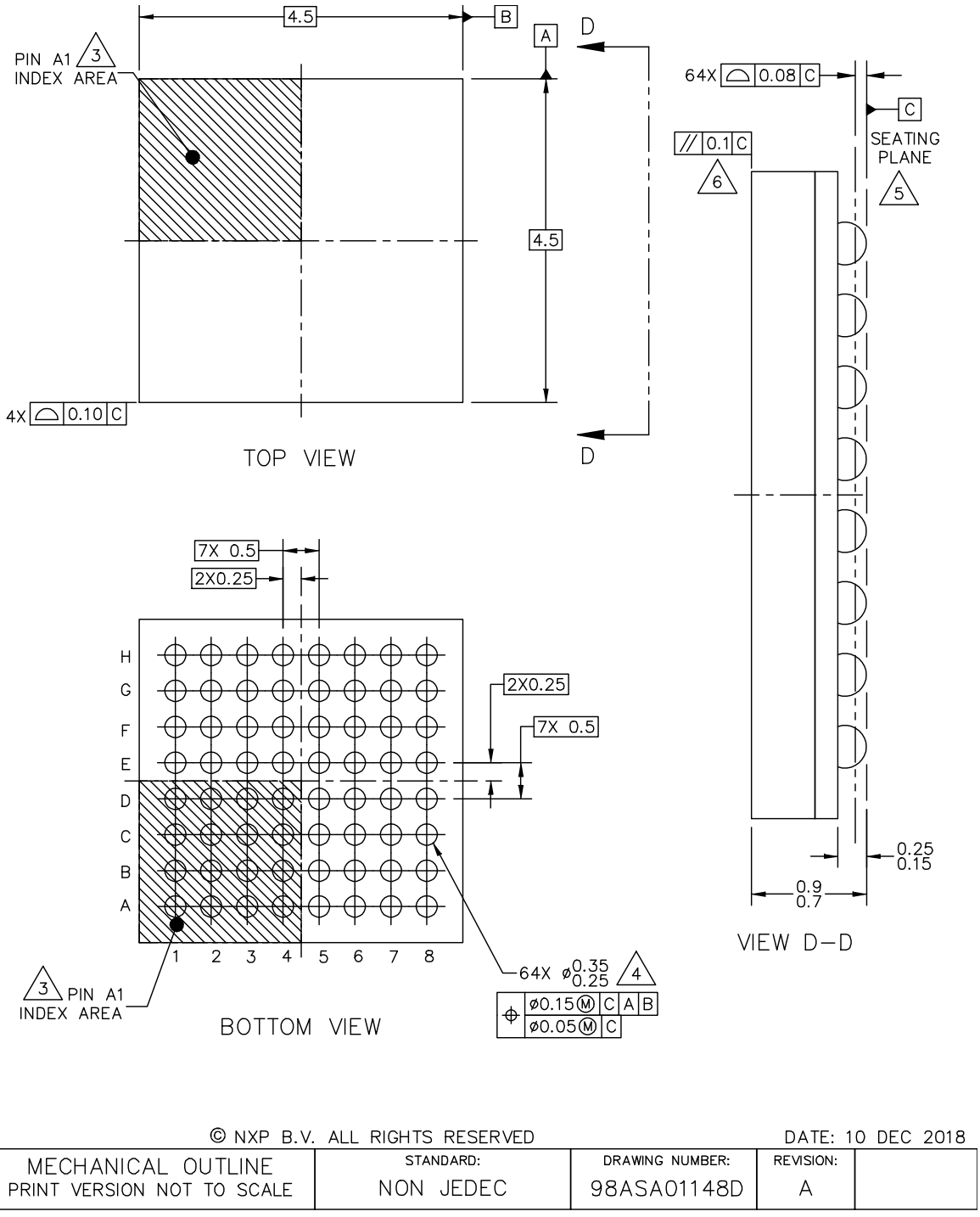


Figure 30. Package outline VFBGA64 (SOT1307-2)

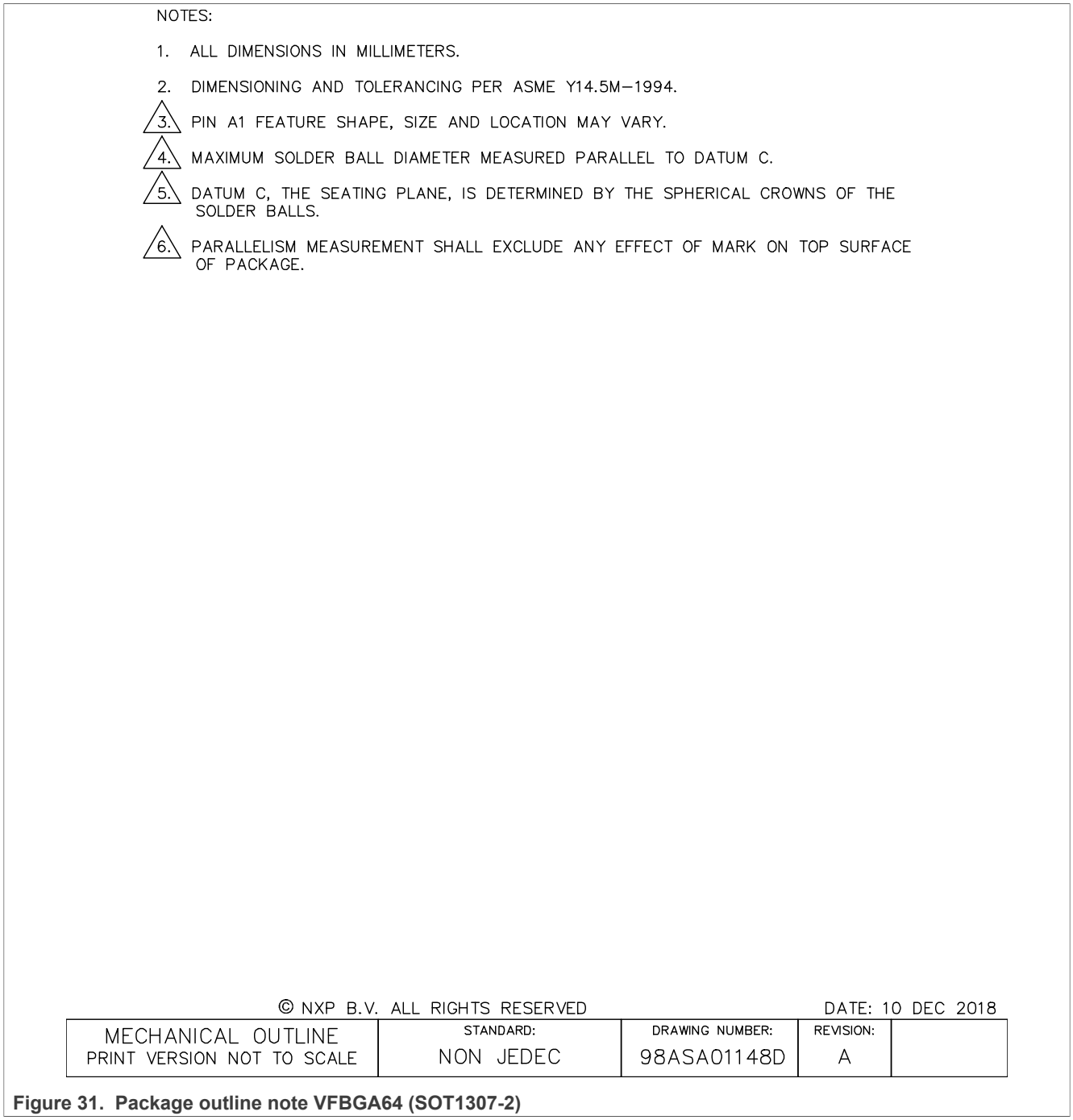


Figure 31. Package outline note VFBGA64 (SOT1307-2)

13 Package marking

13.1 Package marking drawing VFBGA64

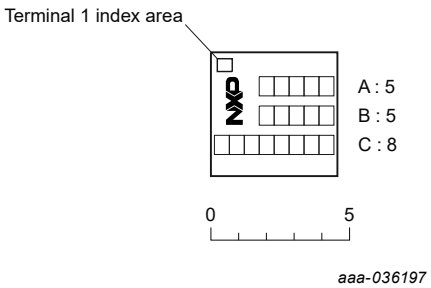


Figure 32. VFBGA64 Package 3 line marking

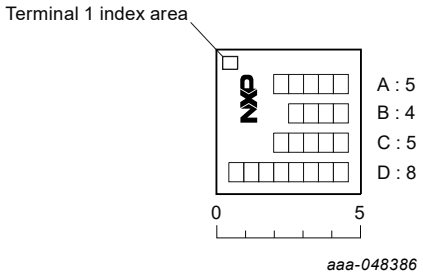


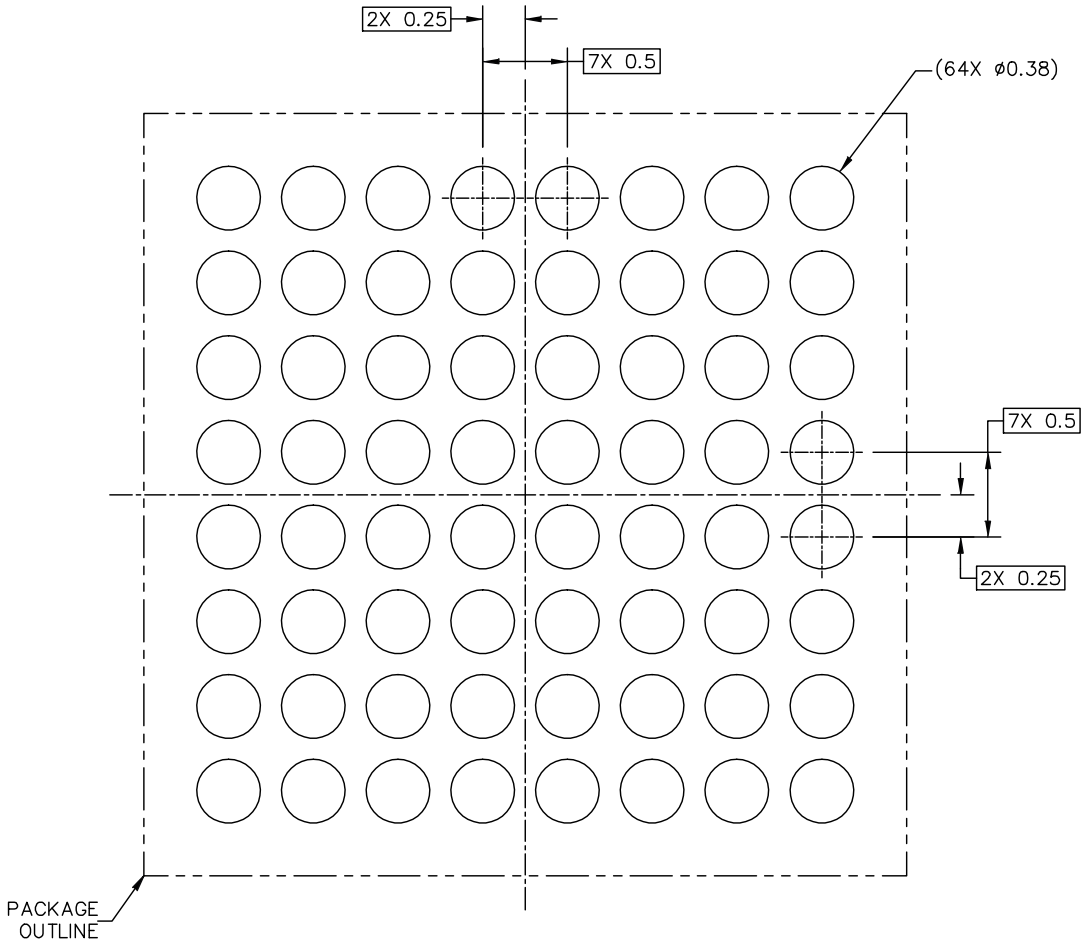
Figure 33. VFBGA64 Package 4 line marking

Line A: 5 characters; e.g. "7640" for PN7640

Line C: 5 characters; contains the DB ID and AS ID

Line D: 8 characters; stDYYWW(X) - contains information assembly center, date code and maturity level (“X” = engineering samples, “ “ = released product)

14 Reflow soldering footprint VFBGA64



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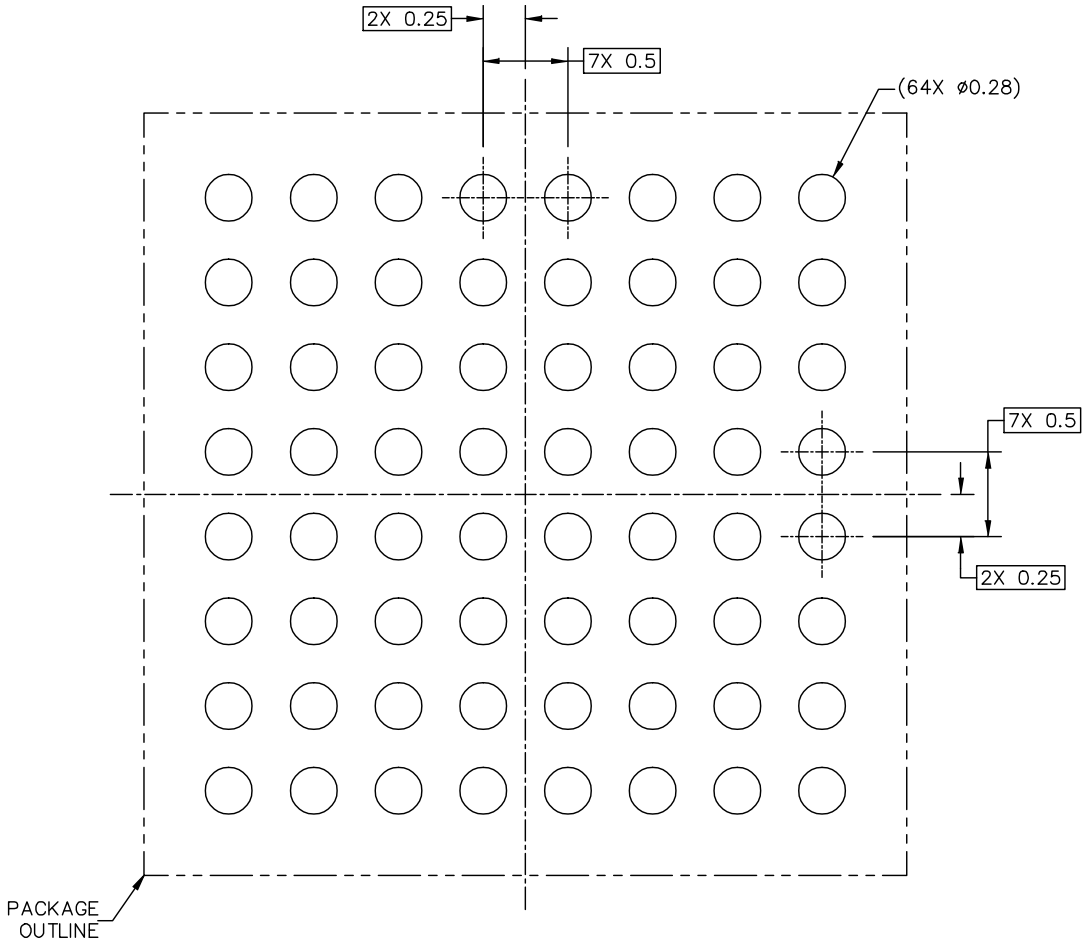
DATE: 10 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01148D	REVISION: A	

Figure 34. Reflow soldering footprint part1 for VFBGA64 (SOT1307-2)



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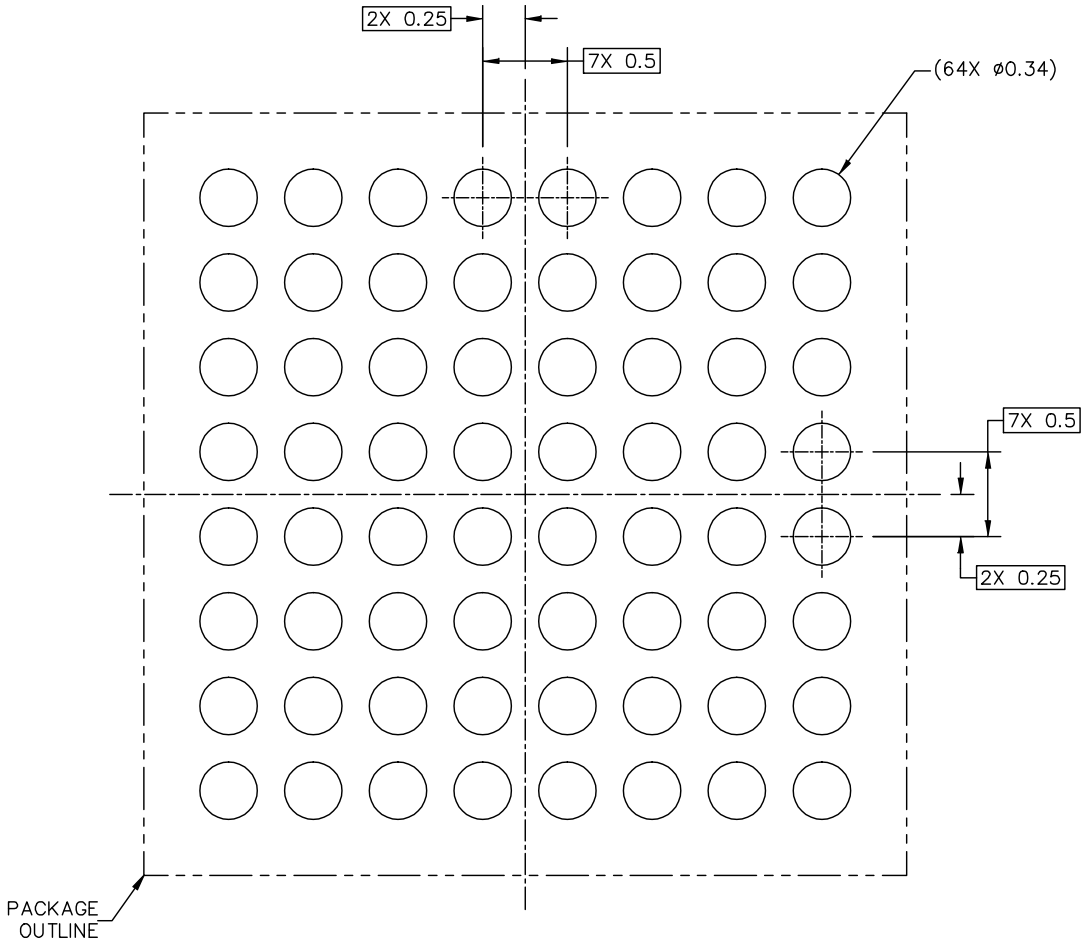
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01148D	REVISION: A	

Figure 35. Reflow soldering footprint part2 for VFBGA64 (SOT1307-2)



RECOMMENDED STENCIL THICKNESS 0.125

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DATE: 10 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01148D	REVISION: A	

Figure 36. Reflow soldering footprint part3 for VFBGA64 (SOT1307-2)

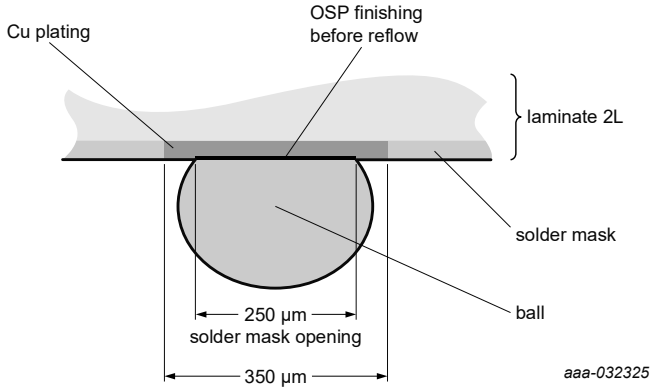

Figure 37. Soldering and footprint representative illustration for VFBGA64 (SOT1307-2)

15 Surface mount reflow soldering

For information on surface mount, reflow soldering and component handling please refer to the related application note.

This application note provides guidelines for the board mounting and handling of NXP Semiconductor packages:

https://www.nxp.com/docs/en/application-note/AN10365.pdf

16 Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*.

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow soldering, in order to remove any moisture that might have soaked into the package.

For MSL3:

168h out-of-pack floor life at maximum ambient temperature, conditions < 30 °C / 60 % RH.

For MSL2:

- 1 year out-of-pack floor life at maximum ambient temperature, conditions < 30 °C° / 60 % RH.

For MSL1:

- No out-of-pack floor live spec. required. Conditions: <30 °C° / 85 % RH.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

17 Abbreviations

Table 336. Abbreviations

Acronym	Description
AA	audio accelerator
ADC	analog-to-digital converter
AGC	automatic gain control
AHB	advanced high-performance bus
AHB-Lite	advanced high-performance bus (single-controller implementation)
AHB Bus	advanced high-performance bus
APB	advanced peripheral bus
API	application programming interface
ARC	adaptive receiver control
Arm	Advanced RISC Machine
AWC	adaptive waveshape control
BBA	baseband amplifier
BOD	brownout detection
CLIF	contactless interface
CPU	central processing unit
CRC	cyclic redundancy check
CTR	current transfer ratio
CTS	clear to send
DAC	digital-to-analog converter
DC-DC	switch-mode voltage regulator which uses an inductor to store and transfer energy to the output, used for a power supply voltage conversion. PN7642 integrates a step-up/boost converter
DDR	double data rate
DMA	direct memory access
DPC	dynamic power control
ECC	elliptic curve cryptography
EEPROM	electrically erasable programmable read-only memory
EMC	electromagnetic compatibility
EMD	electromagnetic disturbance
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macro
EOF	end-of-frame
Fm+	Fast-mode Plus
FSM	finite state machine
GND	Ground
GPIO	general-purpose input output

Table 336. Abbreviations...*continued*

Acronym	Description
HID	human interface device
HPD	hard power down
HW	hardware
IC	Integrated Circuit
IIR	infinite impulse response
IrDA	Infrared Data Association
IAP	In-Application Programming
ISP	In-System Programming
I/O	input/output
I/Q	in-phase/quadrature-phase
JEDEC	Joint Electron Device Engineering Council
LDO	low dropout regulator
LPCD	low-power card detection
LPUART	Low-Power Universal Asynchronous Receiver / Transmitter
LSB	least significant bit
LSByte	least significant byte
MISO	SPI interface controller in target out
MSL	moisture sensitivity level
MOSI	SPI interface controller out target In
NFC	near-field communication
NRZ	non-return-to-zero
NSS	SPI interface active-low target-select signal
NVIC	nested vectored interrupt controller
OS	operating system
OTP	one time programmable
PCB	printed-circuit board
PC	personal computer
PCD	power card detection
PICC	proximity inductive coupling card
PLL	phase-locked loop
PMU	power management unit
PWM	pulse width modulation
RAM	random-access memory
RF	radio frequency
RNG	random number generator
ROM	read-only memory

Table 336. Abbreviations...*continued*

Acronym	Description
RSA	Rivest, Shamir, and Adleman public key cryptosystem
RSSI	receiver signal strength indicator
RTOS	real-time operating system
RTS	request to send
SCK	SPI interface serial clock
SCL	I^2C interface serial clock
SDA	serial data
SMPS	switch mode power supply
SPI	serial peripheral interface
SRAM	static random-access memory
SWD	serial wire debug
TFT	display technology: thin-film transistor-display
TX	transmit
UART	universal asynchronous receiver transmitter
UID	Unique identifier of a card, used during anti-collision sequence to select one out of multiple cards.
ULPCD	ultra low-power card detection
USB	universal serial bus
VREF	voltage reference

18 References

[1] Apple Enhanced Contactless Polling Specification: Version 1.1.
[2] User manual - UM11905 PN76 instruction manual

19 Revision history

Table 337. Revision history

Document ID	Release date	Data sheet status	Supersedes
PN7642 v.3.0	20230314	Product data sheet	PN7642 v.1.2
Modifications:	• Data sheet status changed to product data sheet, security status changed to public		
PN7642 v.1.2	20221108	Objective data sheet	PN7642 v.1.1
Modifications:	• Product name "PN76 family" changed into PN7642 throughout the document • Section 2.2 "Product comparison": updated		
PN7642 v.1.1	20221019	Objective data sheet	PN7642 v.1.0
Modifications:	• Entry for HFQNF40 deleted • The replacement of "master/slave" by "controller/target" in this document follows the recommendation of the NXP - I^2C and JEDEC SPI standards organizations. • Section 9.4.6 "Energy saving card detection" and subchapters added • Section 2.2 "Product comparison": updated • Section 9.3.5.4 "On-chip flash memory map": updated • Section 5 "Ordering information": updated		
PN7642 v.1.0	20220927	Objective data sheet	-

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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