User's Manual

32

Renesas RA6T1 Group

User's Manual: Hardware

32-Bit MCU

Renesas Advanced (RA) Family
Renesas RA6 Series

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Preface

1. About this Document

This manual is generally organized into an overview of the product, descriptions of the CPU, system control functions, peripheral functions, electrical characteristics, and usage notes. This manual describes the product specification of the microcontroller (MCU) superset. Depending on your product, some pins, registers, or functions might not exist. Address space that store unavailable registers are reserved.

2. Audience

This manual is written for system designers who are designing and programming applications using this MCU. The user is expected to have basic knowledge of electrical circuits, logic circuits, and the MCU.

3. Related documents

Renesas provides the following documents for this MCU.

Document type	Description
Datasheet	Features, overview, and electrical characteristics of the MCU
User's Manual: Hardware	MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions
Application Notes	Technical notes, board design guidelines, and software migration information
Technical Update (TU)	Preliminary reports on product specifications such as restriction and errata

4. Numbering Notation

The following numbering notation is used throughout this manual:

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b.
1Fh	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 1Fh. In some cases, a hexadecimal number is shown with the prefix 0x, based on C/C++ formatting.
1234	Decimal number. Decimal numbers are generally shown without a suffix.

5. Typographic Notation

The following typographic notation is used throughout this manual:

Example	Description
ICU.NMICR.NMIMD	Periods separate a function module symbol (ICU), register symbol (NMICR), and bit field symbol (NMIMD)
ICU.NMICR	A period separates a function module symbol (ICU) and register symbol (NMICR)
NMICR.NMIMD	A period separates a register symbol (NMICR) and bit field symbol (NMIMD)
NFCLKSEL[1:0]	In a register bit name, the bit range enclosed in square brackets indicates the number of bits in the field at this location. In this example, NFCLKSEL[1:0] represents a 2-bit field at the specified location in the NMI Pin Interrupt Control Register (NMICR).

6. Unit Prefix

The following unit prefixes are sometimes misleading. Those unit prefixes are described throughout this manual with the following meaning:

Prefix	Description
b	Bit
B	Byte. This unit prefix is generally used for memory specification of the MCU and address space.
k	1000 = 10^3. k is also used to denote 1024 (2^{10}) but this unit prefix is used to denote 1000 (10^3) throughout this manual.
K	1024 = 2^{10}. This unit prefix is used to denote 1024 (2^{10}) not 1000 (10^3) throughout this manual.

7. Special Terms

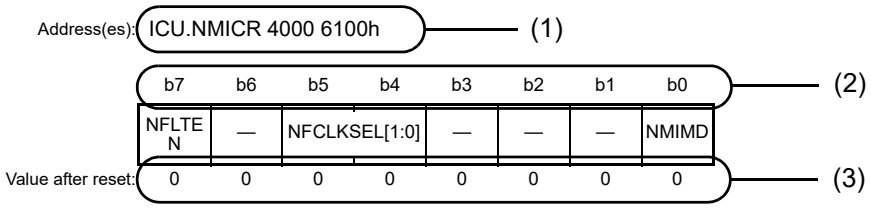
The following terms have special meanings:

Term	Description
NC	Not connected pin. NC means the pin is not connected to the MCU.
Hi-Z	High impedance

8. Register Description

Each register description includes both a register diagram that shows the bit assignments and a register bit table that describes the content of each bit. The example of symbols used in these tables are described in the sections that follow. The following is an example of a register description and associated bit field definition.

X.X.X NMI Pin Interrupt Control Register (NMICR)



(4) (5) (6)

Bit	Symbol	Bit name	Description	R/W
b0	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	NFLTEN	NMI Digital Filter Enable	0: Disable the digital filter 1: Enable the digital filter.	R/W

(1) Function module symbol, register symbol, and address assignment

Function module symbol, register symbol, and address assignment of this register are generally expressed. ICU.NMICR 4000 6100h means NMI Pin Interrupt Control Register (NMICR) of Interrupt Controller Unit (ICU) is assigned to address 4000 6100h.

(2) Bit number

This number indicates the bit number. These bits are shown in order from b31 to b0 for a 32-bit register, from b15 to b0 for a 16-bit register, and from b7 to b0 for an 8-bit register.

(3) Value after reset

This symbol or number indicates the value of each bit after a reset. The value is shown in binary unless specified otherwise.
0: Indicates that the value is 0 after a reset.
1: Indicates that the value is 1 after a reset.
x: Indicates that the value is undefined after a reset.

(4) Bit symbol

Bit symbol indicates the short name of the bit field. Reserved bit is expressed with a —.

(5) Bit name

Bit name indicates the full name of the bit field.

(6) R/W

The R/W column indicates access type: whether the bit field is read or write.
R/W: The bit field is read and write.
R/(W): The bit field is read and write. But writing to this bit field has some limitations. For details on the limitations, see the description or notes of respective registers.
R: The bit field is read-only. Writing to this bit field has no effect.
W: The bit field is write-only. The read value is undefined.

9. Abbreviations

Abbreviations used in this manual are shown in the following table:

Abbreviation	Description
AES	Advanced Encryption Standard
AHB	Advanced High-Performance Bus
AHB-AP	AHB Access Port
APB	Advanced Peripheral Bus
ARC	Alleged RC
ATB	Advanced Trace Bus
BCD	Binary Coded Decimal
BSDL	Boundary Scan Description Language
DES	Data Encryption Standard
DSA	Digital Signature Algorithm
ECC	Elliptic Curve Cryptography
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
FLL	Frequency Locked Loop
FPU	Floating-Point Unit
GSM	Global System for Mobile communications
HMI	Human Machine Interface
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NVIC	Nested Vector Interrupt Controller
PC	Program Counter
PFS	Port Function Select
PLL	Phase Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RSA	Rivest Shamir Adleman
SHA	Secure Hash Algorithm
S/H	Sample and Hold
SP	Stack Pointer
SWD	Serial Wire Debug
SW-DP	Serial Wire-Debug Port
TRNG	True Random Number Generator
UART	Universal Asynchronous Receiver/Transmitter

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Contents

Features 38

1. Overview 39
   1.1 Function Outline 39
   1.2 Block Diagram 43
   1.3 Part Numbering 44
   1.4 Function Comparison 45
   1.5 Pin Functions 46
   1.6 Pin Assignments 49
   1.7 Pin Lists 51

2. CPU 53
   2.1 Overview 53
      2.1.1 CPU 53
      2.1.2 Debug 53
      2.1.3 Operating Frequency 54
   2.2 MCU Implementation Options 55
   2.3 Trace Interface 55
   2.4 JTAG/SWD Interface 55
   2.5 Debug Mode 56
      2.5.1 Debug Mode Definition 56
      2.5.2 Debug Mode Effects 56
   2.6 Programmers Model 57
      2.6.1 Address Spaces 57
      2.6.2 Cortex-M4 Peripheral Address Map 57
      2.6.3 CoreSight ROM Table 58
      2.6.4 DBGREG Module 59
      2.6.5 OCDREG Module 61
   2.7 CoreSight ATB Funnel 63
   2.8 Flash Patch and Break Unit 64
   2.9 SysTick System Timer 64
   2.10 CoreSight Time Stamp Generator 64
   2.11 OCD Emulator Connection 64
      2.11.1 DBGEN 65
      2.11.2 Unlock ID Code 65
      2.11.3 Restrictions on Connecting an OCD Emulator 65
   2.12 References 67

3. Operating Modes 68
   3.1 Overview 68
   3.2 Details of Operating Modes 68
      3.2.1 Single-Chip Mode 68

3.2.2 SCI Boot Mode 68
3.3 Operating Mode Transitions 68
3.3.1 Operating Mode Transitions as Determined by the Mode-Setting Pin 68
4. Address Space 69
4.1 Overview 69
5. Memory Mirror Function (MMF) 70
5.1 Overview 70
5.2 Register Descriptions 70
5.2.1 MemMirror Special Function Register (MMSFR) 70
5.2.2 MemMirror Enable Register (MMEN) 71
5.3 Operation 71
5.3.1 MMF Operation 71
5.3.2 Setting Example 74
6. Resets 76
6.1 Overview 76
6.2 Register Descriptions 80
6.2.1 Reset Status Register 0 (RSTSR0) 80
6.2.2 Reset Status Register 1 (RSTSR1) 81
6.2.3 Reset Status Register 2 (RSTSR2) 83
6.2.4 Reset Control Register 1 (RCR1) 84
6.2.5 Reset Control Register 2 (RCR2) 84
6.2.6 Reset Control Register 4 (RCR4) 84
6.3 Operation 85
6.3.1 RES Pin Reset 85
6.3.2 Power-On Reset 85
6.3.3 Voltage Monitor Reset 86
6.3.4 Deep Software Standby Reset 87
6.3.5 Independent Watchdog Timer Reset 87
6.3.6 Watchdog Timer Reset 88
6.3.7 Software Reset 88
6.3.8 Determination of Cold/Warm Start 88
6.3.9 Determination of Reset Generation Source 88
6.4 Initialization Procedure Required after Reset 89
7. Option-Setting Memory 91
7.1 Overview 91
7.2 Register Descriptions 91
7.2.1 Option Function Select Register 0 (OFS0) 91
7.2.2 Option Function Select Register 1 (OFS1) 94
7.2.3 Access Window Setting Register (AWS) 95
7.2.4 OCD/Serial Programmer ID Setting Register (OSIS) 97
7.3 Setting the Option-Setting Memory 98

7.3.1 Allocation of Data in the Option-Setting Memory 98
7.3.2 Setting Data for Programming the Option-Setting Memory 98
7.4 Usage Notes 98
7.4.1 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting Memory 98
8. Low Voltage Detection (LVD) 99
8.1 Overview 99
8.2 Register Descriptions 101
8.2.1 Voltage Monitor 1 Circuit Control Register 1 (LVD1CR1) 101
8.2.2 Voltage Monitor 1 Circuit Status Register (LVD1SR) 102
8.2.3 Voltage Monitor 2 Circuit Control Register 1 (LVD2CR1) 102
8.2.4 Voltage Monitor 2 Circuit Status Register (LVD2SR) 103
8.2.5 Voltage Monitor Circuit Control Register (LVCMPCR) 103
8.2.6 Voltage Detection Level Select Register (LVDLVLR) 104
8.2.7 Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0) 104
8.2.8 Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0) 105
8.3 VCC Input Voltage Monitor 106
8.3.1 Monitoring Vdet0 106
8.3.2 Monitoring Vdet1 106
8.3.3 Monitoring Vdet2 107
8.4 Reset from Voltage Monitor 0 107
8.5 Interrupt and Reset from Voltage Monitor 1 108
8.6 Interrupt and Reset from Voltage Monitor 2 111
8.7 Event Link Output 113
8.7.1 Interrupt Handling and Event Linking 114
9. Clock Generation Circuit 115
9.1 Overview 115
9.2 Register Descriptions 118
9.2.1 System Clock Division Control Register (SCKDIVCR) 118
9.2.2 System Clock Source Control Register (SCKSCR) 122
9.2.3 PLL Clock Control Register (PLLCCR) 124
9.2.4 PLL Control Register (PLLCR) 125
9.2.5 Main Clock Oscillator Control Register (MOSCCR) 125
9.2.6 Subclock Oscillator Control Register (SOSCCR) 126
9.2.7 Low-Speed On-Chip Oscillator Control Register (LOCOCR) 127
9.2.8 High-Speed On-Chip Oscillator Control Register (HOCOCR) 128
9.2.9 High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR) 128
9.2.10 Middle-Speed On-Chip Oscillator Control Register (MOCOCR) 129
9.2.11 FLL Control Register 1 (FLLCR1) 130
9.2.12 FLL Control Register 2 (FLLCR2) 131
9.2.13 Oscillation Stabilization Flag Register (OSCSF) 132

9.2.14 Oscillation Stop Detection Control Register (OSTDCR) 133
9.2.15 Oscillation Stop Detection Status Register (OSTDSR) 134
9.2.16 Main Clock Oscillator Wait Control Register (MOSCWTCR) 135
9.2.17 Main Clock Oscillator Mode Oscillation Control Register (MOMCR) 136
9.2.18 Subclock Oscillator Mode Control Register (SOMCR) 136
9.2.19 Clock Out Control Register (CKOCR) 137
9.2.20 LOCO User Trimming Control Register (LOCOUTCR) 138
9.2.21 MOCO User Trimming Control Register (MOCOUTCR) 138
9.2.22 HOCO User Trimming Control Register (HOCOUTCR) 139
9.2.23 Trace Clock Control Register (TRCKCR) 139
9.3 Main Clock Oscillator 139
9.3.1 Connecting the Crystal Resonator 140
9.3.2 External Clock Input 140
9.3.3 Notes on External Clock Input 140
9.4 Sub-Clock Oscillator 141
9.4.1 Connecting a 32.768-kHz Crystal Resonator 141
9.4.2 Handling of Pins when the Sub-Clock Oscillator Is Not Used 141
9.5 Oscillation Stop Detection Function 142
9.5.1 Oscillation Stop Detection and Operation after Detection 142
9.5.2 Oscillation Stop Detection Interrupts 143
9.6 PLL Circuit 144
9.7 Internal Clock 144
9.7.1 System Clock (ICLK) 144
9.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD) 145
9.7.3 Flash Interface Clock (FCLK) 146
9.7.4 CAN Clock (CANMCLK) 146
9.7.5 CAC Clock (CACCLK) 146
9.7.6 IWDT-Dedicated Clock (IWDTCLK) 146
9.7.7 AGT-Dedicated Clock (AGTSCLK, AGTLCLK) 146
9.7.8 SysTick Timer-Dedicated Clock (SYSTICCLK) 146
9.7.9 Clock/Buzzer Output Clock (CLKOUT) 146
9.7.10 JTAG Clock (JTAGTCK) 146
9.8 Usage Notes 147
9.8.1 Notes on Clock Generation Circuit 147
9.8.2 Notes on Resonator 147
9.8.3 Notes on Board Design 147
9.8.4 Notes on the Resonator Connect Pin 147
9.8.5 Notes on the Main Clock Oscillator Drive Capability Auto Switching Function 147
10. Clock Frequency Accuracy Measurement Circuit (CAC) 149
10.1 Overview 149
10.2 Register Descriptions 150

10.2.1 CAC Control Register 0 (CACR0) 150
10.2.2 CAC Control Register 1 (CACR1) 151
10.2.3 CAC Control Register 2 (CACR2) 152
10.2.4 CAC Interrupt Control Register (CAICR) 153
10.2.5 CAC Status Register (CASTR) 154
10.2.6 CAC Upper-Limit Value Setting Register (CAULVR) 155
10.2.7 CAC Lower-Limit Value Setting Register (CALLVR) 155
10.2.8 CAC Counter Buffer Register (CACNTBR) 155
10.3 Operation 155
10.3.1 Measuring Clock Frequency 155
10.3.2 Digital Filtering of Signals on CACREF Pin 156
10.4 Interrupt Requests 157
10.5 Usage Notes 157
10.5.1 Settings for the Module-Stop Function 157
11. Low Power Modes 158
11.1 Overview 158
11.2 Register Descriptions 161
11.2.1 Standby Control Register (SBYCR) 161
11.2.2 Module Stop Control Register A (MSTPCRA) 162
11.2.3 Module Stop Control Register B (MSTPCRB) 163
11.2.4 Module Stop Control Register C (MSTPCRC) 164
11.2.5 Module Stop Control Register D (MSTPCRD) 165
11.2.6 Operating Power Control Register (OPCCR) 166
11.2.7 Sub Operating Power Control Register (SOPCCR) 167
11.2.8 Snooze Control Register (SNZCR) 168
11.2.9 Snooze End Control Register (SNZEDCR) 169
11.2.10 Snooze Request Control Register (SNZREQCR) 170
11.2.11 Deep Software Standby Control Register (DPSBYCR) 172
11.2.12 Deep Software Standby Interrupt Enable Register 0 (DPSIER0) 173
11.2.13 Deep Software Standby Interrupt Enable Register 1 (DPSIER1) 173
11.2.14 Deep Software Standby Interrupt Enable Register 2 (DPSIER2) 174
11.2.15 Deep Software Standby Interrupt Enable Register 3 (DPSIER3) 175
11.2.16 Deep Software Standby Interrupt Flag Register 0 (DPSIFR0) 175
11.2.17 Deep Software Standby Interrupt Flag Register 1 (DPSIFR1) 176
11.2.18 Deep Software Standby Interrupt Flag Register 2 (DPSIFR2) 177
11.2.19 Deep Software Standby Interrupt Flag Register 3 (DPSIFR3) 178
11.2.20 Deep Software Standby Interrupt Edge Register 0 (DPSIEGR0) 179
11.2.21 Deep Software Standby Interrupt Edge Register 1 (DPSIEGR1) 179
11.2.22 Deep Software Standby Interrupt Edge Register 2 (DPSIEGR2) 180
11.2.23 System Control OCD Control Register (SYOCDCR) 180
11.2.24 Standby Condition Register (STCONR) 181

11.3 Reducing Power Consumption by Switching Clock Signals 181
11.4 Module-Stop Function 182
11.5 Function for Lower Operating Power Consumption 182
11.5.1 Setting the Operating Power Control Mode 182
11.6 Sleep Mode 183
11.6.1 Transitioning to Sleep Mode 183
11.6.2 Canceling Sleep Mode 184
11.7 Software Standby Mode 184
11.7.1 Transitioning to Software Standby Mode 184
11.7.2 Canceling Software Standby Mode 187
11.7.3 Example of Software Standby Mode Application 188
11.8 Snooze Mode 189
11.8.1 Transitioning to Snooze Mode 189
11.8.2 Canceling Snooze Mode 190
11.8.3 Returning to Software Standby Mode 190
11.8.4 Snooze Operation Example 192
11.9 Deep Software Standby Mode 196
11.9.1 Transitioning to Deep Software Standby Mode 196
11.9.2 Canceling Deep Software Standby Mode 196
11.9.3 Pin States when Deep Software Standby Mode is Canceled 197
11.9.4 Example of Deep Software Standby Mode Application 197
11.9.5 Usage Flow for Deep Software Standby Mode 198
11.10 Usage Notes 199
11.10.1 Register Access 199
11.10.2 I/O Port States 201
11.10.3 Module-Stop State of DMAC and DTC 201
11.10.4 Internal Interrupt Sources 201
11.10.5 Input Buffer Control by the DIRQnE Bit (n = 0, 1, 4 to 12) 201
11.10.6 Transitioning to Low Power Modes 201
11.10.7 Timing of WFI Instruction 201
11.10.8 Writing to the WDT and IWDT Registers by the DMAC or DTC in Sleep Mode or Snooze Mode 201
11.10.9 Oscillators in Snooze Mode 202
11.10.10 Snooze Mode Entry by RXD0 Falling Edge 202
11.10.11 Using SCI0 in Snooze Mode 202
11.10.12 Conditions of A/D Conversion Start in Snooze Mode 202
11.10.13 ELC Events in Snooze Mode 202
12. Register Write Protection 203
12.1 Overview 203
12.2 Register Descriptions 203
12.2.1 Protect Register (PRCR) 203

13. Interrupt Controller Unit (ICU) 204
13.1 Overview 204
13.2 Register Descriptions 206
13.2.1 IRQ Control Register i (IRQCRi) (i = 0 to 13) 206
13.2.2 Non-Maskable Interrupt Status Register (NMISR) 207
13.2.3 Non-Maskable Interrupt Enable Register (NMIER) 209
13.2.4 Non-Maskable Interrupt Status Clear Register (NMICLR) 210
13.2.5 NMI Pin Interrupt Control Register (NMICR) 212
13.2.6 ICU Event Link Setting Register n (IELSRn) (n = 0 to 95) 213
13.2.7 DMAC Event Link Setting Register n (DELSRn) (n = 0 to 7) 214
13.2.8 SYS Event Link Setting Register (SELSR0) 215
13.2.9 Wake Up Interrupt Enable Register (WUPEN) 215
13.3 Vector Table 216
13.3.1 Interrupt Vector Table 217
13.3.2 Event Numbers 219
13.4 Interrupt Operation 226
13.4.1 Detecting Interrupts 226
13.4.2 Selecting Interrupt Request Destinations 227
13.4.3 Digital Filter 229
13.4.4 External Pin Interrupts 229
13.5 Non-Maskable Interrupt Operation 230
13.6 Return from Low Power Modes 230
13.6.1 Return from Sleep Mode 230
13.6.2 Return from Software Standby Mode 230
13.6.3 Return from Snooze Mode 231
13.7 Using the WFI Instruction with Non-Maskable Interrupts 231
13.8 Reference 231
14. Buses 232
14.1 Overview 232
14.2 Description of Buses 233
14.2.1 Main Buses 233
14.2.2 Slave Interface 233
14.2.3 Parallel Operations 234
14.2.4 Restrictions on Endianness 234
14.3 Register Descriptions 234
14.3.1 Master Bus Control Register (BUSMCNT<master>) 234
14.3.2 Slave Bus Control Register (BUSSCNT<slave>) 235
14.3.3 Bus Error Address Register (BUSnERRADD) (n = 1 to 4) 236
14.3.4 Bus Error Status Register (BUSnERRSTAT) (n = 1 to 4) 237
14.4 Bus Error Monitoring 237
14.4.1 Bus Error Types 237

14.4.2 Operation when a Bus Error Occurs 238
14.4.3 Conditions Leading to Illegal Address Access Errors 238
14.4.4 Timeout 239
14.5 Notes on using Flash Cache 239
14.6 References 239
15. Memory Protection Unit (MPU) 240
15.1 Overview 240
15.2 CPU Stack Pointer Monitor 240
15.2.1 Register Descriptions 243
15.2.2 Operation 247
15.3 Arm MPU 248
15.4 Bus Master MPU 248
15.4.1 Register Descriptions 249
15.4.2 Operation 254
15.5 Bus Slave MPU 256
15.5.1 Register Descriptions 257
15.5.2 Operation 261
15.6 Security MPU 262
15.6.1 Register Descriptions (Option-Setting memory) 262
15.6.2 Memory Protection 269
15.6.3 Usage Notes 270
15.7 References 270
16. DMA Controller (DMAC) 271
16.1 Overview 271
16.2 Register Descriptions 273
16.2.1 DMA Source Address Register (DMSAR) 273
16.2.2 DMA Destination Address Register (DMDAR) 273
16.2.3 DMA Transfer Count Register (DMCRA) 274
16.2.4 DMA Block Transfer Count Register (DMCRB) 275
16.2.5 DMA Transfer Mode Register (DMTMD) 275
16.2.6 DMA Interrupt Setting Register (DMINT) 276
16.2.7 DMA Address Mode Register (DMAMD) 277
16.2.8 DMA Offset Register (DMOFR) 279
16.2.9 DMA Transfer Enable Register (DMCNT) 279
16.2.10 DMA Software Start Register (DMREQ) 280
16.2.11 DMA Status Register (DMSTS) 281
16.2.12 DMAC Module Activation Register (DMAST) 282
16.3 Operation 282
16.3.1 Transfer Mode 282
16.3.2 Extended Repeat Area Function 285
16.3.3 Address Update Function Using Offset 287

16.3.4 Activation Sources 291
16.3.5 Operation Timing 291
16.3.6 Execution Cycles of DMAC 292
16.3.7 Activating the DMAC 293
16.3.8 Starting DMA Transfer 295
16.3.9 Registers during DMA Transfer 295
16.3.10 Channel Priority 296
16.4 Ending DMA Transfer 296
16.4.1 Transfer End by Completion of Specified Total Number of Transfer Operations 296
16.4.2 Transfer End by Repeat Size End Interrupt 296
16.4.3 Transfer End by Interrupt on Extended Repeat Area Overflow 296
16.4.4 Precautions for the End of DMA Transfer 297
16.5 Interrupts 297
16.6 Event Link 298
16.7 Low Power Consumption Function 298
16.8 Usage Notes 299
16.8.1 Access to Registers during DMA Transfer 299
16.8.2 DMA Transfer to Reserved Areas 299
16.8.3 Setting the DMAC Event Link Setting Register of the Interrupt Controller Unit (ICU.DELSRn) 299
16.8.4 Suspending or Restarting DMA Activation 299
17. Data Transfer Controller (DTC) 300
17.1 Overview 300
17.2 Register Descriptions 302
17.2.1 DTC Mode Register A (MRA) 302
17.2.2 DTC Mode Register B (MRB) 303
17.2.3 DTC Transfer Source Register (SAR) 304
17.2.4 DTC Transfer Destination Register (DAR) 304
17.2.5 DTC Transfer Count Register A (CRA) 305
17.2.6 DTC Transfer Count Register B (CRB) 306
17.2.7 DTC Control Register (DTCCR) 306
17.2.8 DTC Vector Base Register (DTCVBR) 307
17.2.9 DTC Module Start Register (DTCST) 307
17.2.10 DTC Status Register (DTCSTS) 308
17.3 Activation Sources 308
17.3.1 Allocating Transfer Information and the DTC Vector Table 309
17.4 Operation 310
17.4.1 Transfer Information Read Skip Function 313
17.4.2 Transfer Information Write-Back Skip Function 314
17.4.3 Normal Transfer Mode 314
17.4.4 Repeat Transfer Mode 315
17.4.5 Block Transfer Mode 316

17.4.6 Chain Transfer 317
17.4.7 Operation Timing 318
17.4.8 Execution Cycles of DTC 320
17.4.9 DTC Bus Mastership Release Timing 320
17.5 DTC Setting Procedure 320
17.6 Examples of DTC Usage 321
17.6.1 Normal Transfer 322
17.6.2 Chain Transfer 322
17.6.3 Chain Transfer when Counter = 0 324
17.7 Interrupt Sources 325
17.8 Event Link 325
17.9 Snooze Control Interface 325
17.10 Module-Stop Function 325
17.11 Usage Notes 326
17.11.1 Transfer Information Start Address 326
18. Event Link Controller (ELC) 327
18.1 Overview 327
18.2 Register Descriptions 328
18.2.1 Event Link Controller Register (ELCR) 328
18.2.2 Event Link Software Event Generation Register n (ELSEGRn) (n = 0, 1) 328
18.2.3 Event Link Setting Register n (ELSRn) (n = 0 to 17) 329
18.3 Operation 335
18.3.1 Relation between Interrupt Handling and Event Linking 335
18.3.2 Linking Events 335
18.3.3 Example Procedure for Linking Events 336
18.4 Usage Notes 336
18.4.1 Linking DMAC or DTC Transfer End Signals as Events 336
18.4.2 Setting the Clocks 336
18.4.3 Setting the Module-Stop Function 336
18.4.4 ELC delay time 336
19. I/O Ports 338
19.1 Overview 338
19.2 Register Descriptions 340
19.2.1 Port Control Register 1 (PCNTR1/PODR/PDR) 340
19.2.2 Port Control Register 2 (PCNTR2/EIDR/PIDR) 341
19.2.3 Port Control Register 3 (PCNTR3/PORR/POSR) 342
19.2.4 Port Control Register 4 (PCNTR4/EORR/EOSR) 343
19.2.5 Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 7; n = 00 to 15) 344
19.2.6 Write-Protect Register (PWPR) 346
19.2.7 AGT Input Control Register (VBTICTLR) 346
19.3 Operation 346

19.3.1 General I/O Ports 346
19.3.2 Port Function Select 347
19.3.3 Port Group Function for the ELC 347
19.4 Handling of Unused Pins 349
19.5 Usage Notes 350
19.5.1 Procedure for Specifying the Pin Functions 350
19.5.2 Procedure for Using Port Group Input 350
19.5.3 Port Output Data Register (PODR) Summary 350
19.5.4 Notes on Using Analog Functions 350
19.5.5 I/O Buffer Specification 350
19.6 Peripheral Select Settings for each Product 352
19.7 Notes on the PmnPFS Register Setting 352
20. Key Interrupt Function (KINT) 363
20.1 Overview 363
20.2 Register Descriptions 365
20.2.1 Key Return Control Register (KRCTL) 365
20.2.2 Key Return Flag Register (KRF) 365
20.2.3 Key Return Mode Register (KRM) 365
20.3 Operation 366
20.3.1 Operation When Not Using Key Interrupt Flag (KRMD = 0) 366
20.3.2 Operation When Using the Key Interrupt Flags (KRMD = 1) 366
20.4 Usage Notes 368
21. Port Output Enable for GPT (POEG) 369
21.1 Overview 369
21.2 Register Descriptions 371
21.2.1 POEG Group n Setting Register (POEGGn) (n = A to D) 371
21.3 Output-Disable Control Operation 372
21.3.1 Pin Input Level Detection Operation 372
21.3.2 Output-Disable Requests from the GPT 373
21.3.3 Comparator Interrupt Detection 373
21.3.4 Output-Disable Control Using Detection of Stopped Oscillation 373
21.3.5 Output-Disable Control Using Registers 373
21.3.6 Release from Output-Disable 373
21.4 Interrupt Sources 374
21.5 External Trigger Output to the GPT 375
21.6 Usage Notes 375
21.6.1 Transition to Software Standby Mode 375
21.6.2 Specifying Pins Associated with the GPT 375
22. General PWM Timer (GPT) 376
22.1 Overview 376
22.2 Register Descriptions 380

22.2.1 General PWM Timer Write Protection Register (GTWP) 382
22.2.2 General PWM Timer Software Start Register (GTSTR) 382
22.2.3 General PWM Timer Software Stop Register (GTSTP) 383
22.2.4 General PWM Timer Software Clear Register (GTCLR) 383
22.2.5 General PWM Timer Start Source Select Register (GTSSR) 384
22.2.6 General PWM Timer Stop Source Select Register (GTPSR) 387
22.2.7 General PWM Timer Clear Source Select Register (GTCSR) 390
22.2.8 General PWM Timer Up Count Source Select Register (GTUPSR) 393
22.2.9 General PWM Timer Down Count Source Select Register (GTDNSR) 396
22.2.10 General PWM Timer Input Capture Source Select Register A (GTICASR) 399
22.2.11 General PWM Timer Input Capture Source Select Register B (GTICBSR) 402
22.2.12 General PWM Timer Control Register (GTCR) 405
22.2.13 General PWM Timer Count Direction and Duty Setting Register (GTUDDTYC) 407
22.2.14 General PWM Timer I/O Control Register (GTIOR) 409
22.2.15 General PWM Timer Interrupt Output Setting Register (GTINTAD) 413
22.2.16 General PWM Timer Status Register (GTST) 415
22.2.17 General PWM Timer Buffer Enable Register (GTBER) 420
22.2.18 General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register (GTITC) 423
22.2.19 General PWM Timer Counter (GTCNT) 425
22.2.20 General PWM Timer Compare Capture Register n (GTCCRn) (n = A to F) 425
22.2.21 General PWM Timer Cycle Setting Register (GTPR) 426
22.2.22 General PWM Timer Cycle Setting Buffer Register (GTPBR) 426
22.2.23 General PWM Timer Cycle Setting Double-Buffer Register (GTPDBR) 426
22.2.24 A/D Converter Start Request Timing Register n (GTADTRn) (n = A, B) 427
22.2.25 A/D Converter Start Request Timing Buffer Register n (GTADTBRn) (n = A, B) 427
22.2.26 A/D Converter Start Request Timing Double-Buffer Register n (GTADTDBRn) (n = A, B) 428
22.2.27 General PWM Timer Dead Time Control Register (GTDTCR) 428
22.2.28 General PWM Timer Dead Time Value Register n (GTDVn) (n = U, D) 430
22.2.29 General PWM Timer Dead Time Buffer Register n (GTDBn) (n = U, D) 430
22.2.30 General PWM Timer Output Protection Function Status Register (GTSOS) 431
22.2.31 General PWM Timer Output Protection Function Temporary Release Register (GTSOTR) 431
22.2.32 Output Phase Switching Control Register (OPSCR) 432
22.3 Operation 434
22.3.1 Basic Operation 434
22.3.2 Buffer Operation 444
22.3.3 PWM Output Operating Mode 455
22.3.4 Automatic Dead Time Setting Function 468
22.3.5 Count Direction Changing Function 473

22.3.6 Function of Output Duty 0% and 100% 474
22.3.7 Hardware Count Start/Count Stop and Clear Operation 475
22.3.8 Synchronized Operation 482
22.3.9 PWM Output Operation Examples 486
22.3.10 Phase Counting Function 492
22.3.11 Output Phase Switching (GPT_OPS) 499
22.4 Interrupt Sources 506
22.4.1 DMAC/DTC Activation 512
22.4.2 Interrupt and A/D Conversion Request Skipping Function 512
22.5 A/D Converter Start Request 516
22.6 Operations Linked by the ELC 519
22.6.1 Event Signal Output to the ELC 519
22.6.2 Event Signal Inputs from the ELC 519
22.7 Noise Filter Function 519
22.8 Protection Function 520
22.8.1 Write-Protection for Registers 520
22.8.2 Disabling of Buffer Operation 520
22.8.3 GTIOC Pin Output Negate Control 521
22.8.4 Output Protection Function for GTIOC Pin Output 522
22.9 Initialization Method of Output Pins 529
22.9.1 Pin Settings after Reset 529
22.9.2 Pin Initialization Caused by Error during Operation 530
22.10 Usage Notes 530
22.10.1 Module-Stop Function Setting 530
22.10.2 GTCCRn Settings during Compare Match Operation (n = A to F) 530
22.10.3 Setting Range for the GTCNT Counter 531
22.10.4 Starting and Stopping the GTCNT Counter 531
22.10.5 Priority Order of Each Event 532
23. PWM Delay Generation Circuit 533
23.1 Overview 533
23.2 Register Descriptions 534
23.2.1 PWM Output Delay Control Register (GTDLYCR) 534
23.2.2 PWM Output Delay Control Register 2 (GTDLYCR2) 534
23.2.3 GTIOCnA Rising Output Delay Register (GTDLYRnA) (n = 0 to 3) 536
23.2.4 GTIOCnA Falling Output Delay Register (GTDLYFnA) (n = 0 to 3) 537
23.2.5 GTIOCnB Rising Output Delay Register (GTDLYRnB) (n = 0 to 3) 538
23.2.6 GTIOCnB Falling Output Delay Register (GTDLYFnB) (n = 0 to 3) 539
23.3 Operation 539
23.3.1 Adjustments to the Timing of Rising and Falling Edges in PWM Waveforms 539
23.3.2 Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings 541
23.4 Usage Notes 542

23.4.1 Module-Stop Function Settings 542
23.4.2 Notes on Delay Settings for PWM Delay Generation Circuit 542
24. Low Power Asynchronous General-Purpose Timer (AGT) 544
24.1 Overview 544
24.2 Register Descriptions 546
24.2.1 AGT Counter Register (AGT) 546
24.2.2 AGT Compare Match A Register (AGTCMA) 546
24.2.3 AGT Compare Match B Register (AGTCMB) 547
24.2.4 AGT Control Register (AGTCR) 547
24.2.5 AGT Mode Register 1 (AGTMR1) 549
24.2.6 AGT Mode Register 2 (AGTMR2) 550
24.2.7 AGT I/O Control Register (AGTIOC) 550
24.2.8 AGT Event Pin Select Register (AGTISR) 551
24.2.9 AGT Compare Match Function Select Register (AGTCMSR) 552
24.2.10 AGT Pin Select Register (AGTIOSEL) 552
24.3 Operation 553
24.3.1 Reload Register and Counter Rewrite Operation 553
24.3.2 Reload Register and Compare Register A/B Rewrite Operation 555
24.3.3 Timer Mode 556
24.3.4 Pulse Output Mode 557
24.3.5 Event Counter Mode 558
24.3.6 Pulse Width Measurement Mode 560
24.3.7 Pulse Period Measurement Mode 560
24.3.8 Compare Match Function 561
24.3.9 Output Settings for Each Mode 563
24.3.10 Standby Mode 564
24.3.11 Interrupt Sources 565
24.3.12 Event Signal Output to ELC 565
24.4 Usage Notes 565
24.4.1 Count Operation Start and Stop Control 565
24.4.2 Access to Counter Register 566
24.4.3 When Changing Mode 566
24.4.4 Digital Filter 566
24.4.5 How to Calculate Event Number, Pulse Width, and Pulse Period 566
24.4.6 When Count Is Forcibly Stopped by TSTOP Bit 566
24.4.7 When Selecting AGT0 Underflow as the Count Source 566
24.4.8 Reset of I/O Register 567
24.4.9 When Selecting PCLKB, PCLKB/8, or PCLKB/2 as the Count Source 567
24.4.10 When Selecting AGTSCLK or AGTLCLK as the Count Source 567
24.4.11 When Switching Source Clock 567

25. Watchdog Timer (WDT) 568
25.1 Overview 568
25.2 Register Descriptions 569
25.2.1 WDT Refresh Register (WDTRR) 569
25.2.2 WDT Control Register (WDTCR) 570
25.2.3 WDT Status Register (WDTSR) 572
25.2.4 WDT Reset Control Register (WDTRCR) 573
25.2.5 WDT Count Stop Control Register (WDTCSTPR) 574
25.2.6 Option Function Select Register 0 (OFS0) 574
25.3 Operation 574
25.3.1 Count Operation in each Start Mode 574
25.3.2 Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers 577
25.3.3 Refresh Operation 578
25.3.4 Reset Output 579
25.3.5 Interrupt Sources 579
25.3.6 Reading the Down-Counter Value 579
25.3.7 Association between Option Function Select Register 0 (OFS0) and WDT Registers 580
25.4 Link Operation by ELC 580
25.5 Usage Notes 580
25.5.1 ICU Event Link Setting Register n (IELSRn) Setting 580
26. Independent Watchdog Timer (IWDT) 581
26.1 Overview 581
26.2 Register Descriptions 582
26.2.1 IWDT Refresh Register (IWDTRR) 582
26.2.2 IWDT Status Register (IWDTSR) 583
26.2.3 Option Function Select Register 0 (OFS0) 584
26.3 Operation 586
26.3.1 Auto Start Mode 586
26.3.2 Refresh Operation 587
26.3.3 Status Flags 588
26.3.4 Reset Output 589
26.3.5 Interrupt Sources 589
26.3.6 Reading the Down-Counter Value 589
26.4 Link Operation by the ELC 590
26.5 Usage Notes 590
26.5.1 Refresh Operations 590
26.5.2 Restrictions on the Clock Division Ratio Setting 590
27. Serial Communications Interface (SCI) 591
27.1 Overview 591
27.2 Register Descriptions 595
27.2.1 Receive Shift Register (RSR) 595

27.2.2 Receive Data Register (RDR) 595
27.2.3 Receive 9-Bit Data Register (RDRHL) 595
27.2.4 Receive FIFO Data Register H, L, HL (FRDRH, FRDRL, FRDRHL) 596
27.2.5 Transmit Data Register (TDR) 597
27.2.6 Transmit 9-Bit Data Register (TDRHL) 597
27.2.7 Transmit FIFO Data Register H, L, HL (FTDRH, FTDRL, FTDRHL) 598
27.2.8 Transmit Shift Register (TSR) 599
27.2.9 Serial Mode Register (SMR) for Non-Smart Card Interface Mode (SCMR.SMIF = 0) 599
27.2.10 Serial Mode Register for Smart Card Interface Mode (SMR_SMCI) (SCMR.SMIF = 1) . 600
27.2.11 Serial Control Register (SCR) for Non-Smart Card Interface Mode (SCMR.SMIF = 0) .. 602
27.2.12 Serial Control Register for Smart Card Interface Mode (SCR_SMCI) (SCMR.SMIF = 1) 604
27.2.13 Serial Status Register (SSR) for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0) 605
27.2.14 Serial Status Register for Non-Smart Card Interface and FIFO Mode (SSR_FIFO) (SCMR.SMIF = 0 and FCR.FM = 1) 608
27.2.15 Serial Status Register for Smart Card Interface Mode (SSR_SMCI) (SCMR.SMIF = 1) . 611
27.2.16 Smart Card Mode Register (SCMR) 613
27.2.17 Bit Rate Register (BRR) 614
27.2.18 Modulation Duty Register (MDDR) 623
27.2.19 Serial Extended Mode Register (SEMR) 625
27.2.20 Noise Filter Setting Register (SNFR) 627
27.2.21 I²C Mode Register 1 (SIMR1) 627
27.2.22 I²C Mode Register 2 (SIMR2) 628
27.2.23 I²C Mode Register 3 (SIMR3) 629
27.2.24 I²C Status Register (SISR) 631
27.2.25 SPI Mode Register (SPMR) 631
27.2.26 FIFO Control Register (FCR) 632
27.2.27 FIFO Data Count Register (FDR) 634
27.2.28 Line Status Register (LSR) 634
27.2.29 Compare Match Data Register (CDR) 635
27.2.30 Data Compare Match Control Register (DCCR) 636
27.2.31 Serial Port Register (SPTR) 637
27.3 Operation in Asynchronous Mode 638
27.3.1 Serial Data Transfer Format 638
27.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode 640
27.3.3 Clock 641
27.3.4 Double-Speed Operation and Frequency of 6 Times the Bit Rate 641
27.3.5 CTS and RTS Functions 641

27.3.6 Address Match (Receive Data Match Detection) Function 642
27.3.7 SCI Initialization in Asynchronous Mode 645
27.3.8 Serial Data Transmission in Asynchronous Mode 647
27.3.9 Serial Data Reception in Asynchronous Mode 651
27.4 Multi-Processor Communication Function 658
27.4.1 Multi-Processor Serial Data Transmission 659
27.4.2 Multi-Processor Serial Data Reception 662
27.5 Operation in Clock Synchronous Mode 667
27.5.1 Clock 667
27.5.2 CTS and RTS Functions 668
27.5.3 SCI Initialization in Clock Synchronous Mode 668
27.5.4 Serial Data Transmission in Clock Synchronous Mode 670
27.5.5 Serial Data Reception in Clock Synchronous Mode 674
27.5.6 Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode 679
27.6 Operation in Smart Card Interface Mode 681
27.6.1 Example Connection 681
27.6.2 Data Format (Except in Block Transfer Mode) 682
27.6.3 Block Transfer Mode 683
27.6.4 Receive Data Sampling Timing and Reception Margin 683
27.6.5 SCI Initialization 684
27.6.6 Serial Data Transmission (Except in Block Transfer Mode) 686
27.6.7 Serial Data Reception (Except in Block Transfer Mode) 688
27.6.8 Clock Output Control 690
27.7 Operation in Simple IIC Mode 690
27.7.1 Generation of Start, Restart, and Stop Conditions 691
27.7.2 Clock Synchronization 692
27.7.3 SDA Output Delay 693
27.7.4 SCI Initialization in Simple IIC Mode 694
27.7.5 Operation in Master Transmission in Simple IIC Mode 695
27.7.6 Master Reception in Simple IIC Mode 697
27.8 Operation in Simple SPI Mode 699
27.8.1 States of Pins in Master and Slave Modes 699
27.8.2 SS Function in Master Mode 700
27.8.3 SS Function in Slave Mode 700
27.8.4 Relationship between Clock and Transmit/Receive Data 700
27.8.5 SCI Initialization in Simple SPI Mode 701
27.8.6 Transmission and Reception of Serial Data in Simple SPI Mode 701
27.9 Bit Rate Modulation Function 701
27.10 Interrupt Sources 702
27.10.1 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (non-FIFO selected) 702
27.10.2 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (FIFO selected) 702

27.10.3 Interrupts in Asynchronous, Clock Synchronous, and Simple SPI Modes 702
27.10.4 Interrupts in Smart Card Interface Mode 704
27.10.5 Interrupts in Simple IIC Mode 704
27.11 Event Linking 705
27.12 Address Mismatch Event Output (SCI0_DCUF) 706
27.13 Noise Cancellation Function 706
27.14 Usage Notes 707
27.14.1 Settings for the Module-Stop State 707
27.14.2 SCI Operation during Low Power State 707
27.14.3 Break Detection and Processing 711
27.14.4 Mark State and Production of Breaks 712
27.14.5 Receive Error Flags and Transmit Operation in Clock Synchronous and Simple SPI Modes 712
27.14.6 Restrictions on Clock Synchronous Transmission in Clock Synchronous Mode and Simple SPI Mode 712
27.14.7 Restrictions on Using DMAC or DTC 713
27.14.8 Notes on Starting Transfer 714
27.14.9 External Clock Input in Clock Synchronous Mode and Simple SPI Mode 714
27.14.10 Limitations on Simple SPI Mode 714
28. IrDA Interface 716
28.1 Overview 716
28.2 Register Descriptions 717
28.2.1 IrDA Control Register (IRCR) 717
28.3 Operation 717
28.3.1 IrDA Interface Setup Procedure 717
28.3.2 Transmission 717
28.3.3 Reception 718
28.4 Usage Notes 718
28.4.1 Settings for the Module-Stop State 718
28.4.2 Asynchronous Reference Clock for SCI1 718
29. I²C Bus Interface (IIC) 719
29.1 Overview 719
29.2 Register Descriptions 721
29.2.1 I²C Bus Control Register 1 (ICCR1) 721
29.2.2 I²C Bus Control Register 2 (ICCR2) 723
29.2.3 I²C Bus Mode Register 1 (ICMR1) 726
29.2.4 I²C Bus Mode Register 2 (ICMR2) 727
29.2.5 I²C Bus Mode Register 3 (ICMR3) 728
29.2.6 I²C Bus Function Enable Register (ICFER) 730
29.2.7 I²C Bus Status Enable Register (ICSER) 732
29.2.8 I²C Bus Interrupt Enable Register (ICIER) 733
29.2.9 I²C Bus Status Register 1 (ICSR1) 734

29.2.10 I2C Bus Status Register 2 (ICSR2) 736
29.2.11 I2C Bus Wakeup Unit Register (ICWUR) 739
29.2.12 I2C-Bus Wakeup Unit Register 2 (ICWUR2) 740
29.2.13 Slave Address Register L y (SARLy) (y = 0 to 2) 741
29.2.14 Slave Address Register U y (SARUy) (y = 0 to 2) 742
29.2.15 I2C Bus Bit Rate Low-Level Register (ICBRL) 742
29.2.16 I2C Bus Bit Rate High-Level Register (ICBRH) 743
29.2.17 I2C Bus Transmit Data Register (ICDRT) 744
29.2.18 I2C Bus Receive Data Register (ICDRR) 744
29.2.19 I2C Bus Shift Register (ICDRS) 745
29.3 Operation 745
29.3.1 Communication Data Format 745
29.3.2 Initial Settings 746
29.3.3 Master Transmit Operation 747
29.3.4 Master Receive Operation 750
29.3.5 Slave Transmit Operation 755
29.3.6 Slave Receive Operation 758
29.4 SCL Synchronization Circuit 760
29.5 SDA Output Delay Function 761
29.6 Digital Noise Filter Circuits 762
29.7 Address Match Detection 762
29.7.1 Slave-Address Match Detection 762
29.7.2 Detection of General Call Address 764
29.7.3 Device ID Address Detection 765
29.7.4 Host Address Detection 766
29.8 Wakeup Function 766
29.8.1 Normal Wakeup Mode 1 767
29.8.2 Normal Wakeup Mode 2 770
29.8.3 Command Recovery Mode and EEP Response Mode (Special Wakeup Modes) 772
29.8.4 Precautions for WFI Instruction Execution 775
29.9 Automatic Low-Hold Function for SCL 775
29.9.1 Function to Prevent Wrong Transmission of Transmit Data 775
29.9.2 NACK Reception Transfer Suspension Function 776
29.9.3 Function to Prevent Failure to Receive Data 777
29.10 Arbitration-Lost Detection Functions 778
29.10.1 Master Arbitration-Lost Detection (MALE Bit) 778
29.10.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit) 780
29.10.3 Slave Arbitration-Lost Detection (SALE Bit) 781
29.11 Start, Restart, and Stop Condition Issuing Function 782
29.11.1 Issuing a Start Condition 782
29.11.2 Issuing a Restart Condition 782

29.11.3 Issuing a Stop Condition 784
29.12 Bus Hanging 784
29.12.1 Timeout Function 784
29.12.2 Extra SCL Clock Cycle Output Function 785
29.12.3 IIC Reset and Internal Reset 786
29.13 SMBus Operation 786
29.13.1 SMBus Timeout Measurement 787
29.13.2 Packet Error Code (PEC) 788
29.13.3 SMBus Host Notification Protocol (Notify ARP Master Command) 788
29.14 Interrupt Sources 788
29.14.1 Buffer Operation for IICn_TXI and IICn_RXI Interrupts 789
29.15 State of Registers when Issuing each Condition 789
29.16 Event Link Output 790
29.16.1 Interrupt Handling and Event Linking 790
29.17 Usage Notes 791
29.17.1 Settings for the Module-Stop State 791
29.17.2 Notes on Starting Transfer 791
30. Controller Area Network (CAN) Module 792
30.1 Overview 792
30.2 Register Descriptions 794
30.2.1 Control Register (CTLR) 794
30.2.2 Bit Configuration Register (BCR) 797
30.2.3 Mask Register k (MKRk) (k = 0 to 7) 799
30.2.4 FIFO Received ID Compare Registers 0 and 1 (FIDCR0 and FIDCR1) 799
30.2.5 Mask Invalid Register (MKIVLR) 800
30.2.6 Mailbox Register j (MBj_ID, MBj_DL, MBj_Dm, MBj_TS) (j = 0 to 31; m = 0 to 7) 801
30.2.7 Mailbox Interrupt Enable Register (MIER) 805
30.2.8 Mailbox Interrupt Enable Register for FIFO Mailbox Mode (MIER_FIFO) 805
30.2.9 Message Control Register for Transmit (MCTL_TXj) (j = 0 to 31) 806
30.2.10 Message Control Register for Receive (MCTL_RXj) (j = 0 to 31) 808
30.2.11 Receive FIFO Control Register (RFCR) 810
30.2.12 Receive FIFO Pointer Control Register (RFPCR) 812
30.2.13 Transmit FIFO Control Register (TFCR) 812
30.2.14 Transmit FIFO Pointer Control Register (TFPCR) 814
30.2.15 Status Register (STR) 814
30.2.16 Mailbox Search Mode Register (MSMR) 816
30.2.17 Mailbox Search Status Register (MSSR) 817
30.2.18 Channel Search Support Register (CSSR) 818
30.2.19 Acceptance Filter Support Register (AFSR) 818
30.2.20 Error Interrupt Enable Register (EIER) 819
30.2.21 Error Interrupt Factor Judge Register (EIFR) 820

30.2.22 Receive Error Count Register (RECR) 822
30.2.23 Transmit Error Count Register (TECR) 823
30.2.24 Error Code Store Register (ECSR) 823
30.2.25 Time Stamp Register (TSR) 824
30.2.26 Test Control Register (TCR) 825
30.3 Operation Modes 826
30.3.1 CAN Reset Mode 827
30.3.2 CAN Halt Mode 828
30.3.3 CAN Sleep Mode 829
30.3.4 CAN Operation Mode (Excluding Bus-Off State) 829
30.3.5 CAN Operation Mode (Bus-Off State) 829
30.4 Data Transfer Rate Configuration 830
30.4.1 Clock Setting 830
30.4.2 Bit Timing Setting 830
30.4.3 Data Transfer Rate 831
30.5 Mailbox and Mask Register Structure 831
30.6 Acceptance Filtering and Masking Functions 832
30.7 Reception and Transmission 835
30.7.1 Reception 835
30.7.2 Transmission 837
30.8 Interrupts 838
30.9 Usage Notes 839
30.9.1 Settings for the Module-Stop State 839
30.9.2 Settings for the Operating Clock 839
31. Serial Peripheral Interface (SPI) 840
31.1 Overview 840
31.2 Register Descriptions 843
31.2.1 SPI Control Register (SPCR) 843
31.2.2 SPI Slave Select Polarity Register (SSLP) 845
31.2.3 SPI Pin Control Register (SPPCR) 845
31.2.4 SPI Status Register (SPSR) 846
31.2.5 SPI Data Register (SPDR/SPDR_HA) 848
31.2.6 SPI Sequence Control Register (SPSCR) 851
31.2.7 SPI Sequence Status Register (SPSSR) 851
31.2.8 SPI Bit Rate Register (SPBR) 852
31.2.9 SPI Data Control Register (SPDCR) 853
31.2.10 SPI Clock Delay Register (SPCKD) 855
31.2.11 SPI Slave Select Negation Delay Register (SSLND) 855
31.2.12 SPI Next-Access Delay Register (SPND) 856
31.2.13 SPI Control Register 2 (SPCR2) 856
31.2.14 SPI Command Registers 0 to 7 (SPCMD0 to SPCMD7) 857

31.2.15 SPI Data Control Register 2 (SPDCR2) 859
31.3 Operation 860
31.3.1 Overview of SPI Operation 860
31.3.2 Controlling the SPI Pins 861
31.3.3 SPI System Configuration Examples 862
31.3.4 Data Format 867
31.3.5 Transfer Format 875
31.3.6 Data Transfer Modes 877
31.3.7 Transmit Buffer Empty and Receive Buffer Full Interrupts 878
31.3.8 Error Detection 880
31.3.9 Initializing the SPI 884
31.3.10 SPI Operation 884
31.3.11 Clock Synchronous Operation 896
31.3.12 Loopback Mode 902
31.3.13 Self-Diagnosis of Parity Bit Function 902
31.3.14 Interrupt Sources 903
31.4 Output to the Event Link Controller (ELC) 904
31.4.1 Receive Buffer Full Event Output 904
31.4.2 Transmit Buffer Empty Event Output 904
31.4.3 Mode-Fault, Underrun, Overrun, or Parity Error Event Output 905
31.4.4 SPI Idle Event Output 905
31.4.5 Transmission-Completed Event Output 905
31.5 Usage Notes 905
31.5.1 Settings for the Module-Stop State 905
31.5.2 Constraints on Low Power Functions 906
31.5.3 Constraints on Starting Transfer 906
31.5.4 Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output 906
31.5.5 Constraints on SPRF/SPTEF Flags 906
32. Cyclic Redundancy Check (CRC) Calculator 907
32.1 Overview 907
32.2 Register Descriptions 908
32.2.1 CRC Control Register 0 (CRCCR0) 908
32.2.2 CRC Control Register 1 (CRCCR1) 908
32.2.3 CRC Data Input Register (CRCDIR/CRCDIR_BY) 909
32.2.4 CRC Data Output Register (CRCDOR/CRCDOR_HA/CRCDOR_BY) 909
32.2.5 Snoop Address Register (CRCSAR) 910
32.3 Operation 910
32.3.1 Basic Operation 910
32.3.2 CRC Snoop 913
32.4 Usage Notes 914
32.4.1 Settings for the Module-Stop State 914

32.4.2 Note on Transmission 914
33. Boundary Scan 915
33.1 Overview 915
33.2 Register Descriptions 916
33.2.1 Instruction Register (JTIR) 916
33.2.2 ID Code Register (JTIDR) 917
33.2.3 Bypass Register (JTBPR) 917
33.2.4 Boundary Scan Register (JTBSR) 917
33.3 Operation 917
33.3.1 TAP Controller 917
33.3.2 Commands 918
33.4 Usage Notes 919
34. Secure Cryptographic Engine (SCE7) 921
34.1 Overview 921
34.2 Operation 923
34.2.1 Encryption Engine 923
34.2.2 Encryption and Decryption 924
34.3 Usage Notes 924
34.3.1 Software Standby Mode 924
34.3.2 Settings for the Module-Stop Function 924
35. 12-Bit A/D Converter (ADC12) 925
35.1 Overview 925
35.2 Register Descriptions 930
35.2.1 A/D Data Registers y (ADDRy), A/D Data Duplexing Register (ADDBLDR), A/D Data Duplexing Register A (ADDBLDRA), A/D Data Duplexing Register B (ADDBLDRB), A/D Temperature Sensor Data Register (ADTSDR), A/D Internal Reference Voltage Data Register (ADOCDR) 930
35.2.2 A/D Self-Diagnosis Data Register (ADRD) 934
35.2.3 A/D Control Register (ADCSR) 937
35.2.4 A/D Channel Select Register A0 (ADANSA0) 941
35.2.5 A/D Channel Select Register A1 (ADANSA1) 941
35.2.6 A/D Channel Select Register B0 (ADANSB0) 942
35.2.7 A/D Channel Select Register B1 (ADANSB1) 942
35.2.8 A/D-Converted Value Addition/Average Channel Select Register 0 (ADADS0) 943
35.2.9 A/D-Converted Value Addition/Average Channel Select Register 1 (ADADS1) 943
35.2.10 A/D-Converted Value Addition/Average Count Select Register (ADADC) 944
35.2.11 A/D Control Extended Register (ADCER) 945
35.2.12 A/D Conversion Start Trigger Select Register (ADSTRGR) 947
35.2.13 A/D Conversion Extended Input Control Register (ADEXICR) 948
35.2.14 A/D Sampling State Register n (ADSSTRn) (n = 00 to 03, 05 to 07, L, T, O) 950
35.2.15 A/D Sample and Hold Circuit Control Register (ADSHCR) 951
35.2.16 A/D Sample and Hold Operation Mode Selection Register (ADSHMSR) 951

35.2.17 A/D Disconnection Detection Control Register (ADDISCR) 952
35.2.18 A/D Group Scan Priority Control Register (ADGSPCR) 953
35.2.19 A/D Compare Function Control Register (ADCMPCR) 954
35.2.20 A/D Compare Function Window A Channel Select Register 0 (ADCMPANSR0) 955
35.2.21 A/D Compare Function Window A Channel Select Register 1 (ADCMPANSR1) 956
35.2.22 A/D Compare Function Window A Extended Input Select Register (ADCMPANSER) 956
35.2.23 A/D Compare Function Window A Comparison Condition Setting Register 0 (ADCMPLR0) 957
35.2.24 A/D Compare Function Window A Comparison Condition Setting Register 1 (ADCMPLR1) 959
35.2.25 A/D Compare Function Window A Extended Input Comparison Condition Setting Register (ADCMPLER) 960
35.2.26 A/D Compare Function Window A Lower-Side Level Setting Register (ADCMPDR0), A/D Compare Function Window A Upper-Side Level Setting Register (ADCMPDR1), A/D Compare Function Window B Lower-Side Level Setting Register (ADWINLLB), A/D Compare Function Window B Upper-Side Level Setting Register (ADWINULB) 961
35.2.27 A/D Compare Function Window A Channel Status Register 0 (ADCMPSR0) 962
35.2.28 A/D Compare Function Window A Channel Status Register1 (ADCMPSR1) 963
35.2.29 A/D Compare Function Window A Extended Input Channel Status Register (ADCMPSER) 964
35.2.30 A/D Compare Function Window B Channel Select Register (ADCMPBNSR) 965
35.2.31 A/D Compare Function Window B Status Register (ADCMPBSR) 967
35.2.32 A/D Compare Function Window A/B Status Monitor Register (ADWINMON) 967
35.2.33 A/D Programmable Gain Amplifier Control Register (ADPGACR) 968
35.2.34 A/D Programmable Gain Amplifier Gain Setting Register 0 (ADPGAGS0) 970
35.2.35 A/D Programmable Gain Amplifier Pseudo-Differential Input Control Register (ADPGADCR0) 971
35.3 Operation 972
35.3.1 Scanning Operation 972
35.3.2 Single Scan Mode 972
35.3.3 Continuous Scan Mode 981
35.3.4 Group Scan Mode 988
35.3.5 Compare Function for Windows A and B 997
35.3.6 Analog Input Sampling and Scan Conversion Time 1001
35.3.7 Usage Example of A/D Data Register Automatic Clearing Function 1003
35.3.8 A/D-Converted Value Addition/Average Mode 1004
35.3.9 Disconnection Detection Assist Function 1004
35.3.10 Starting A/D Conversion with an Asynchronous Trigger 1006
35.3.11 Starting A/D Conversion with a Synchronous Trigger from a Peripheral Module 1006
35.3.12 Programmable Gain Amplifiers 1006
35.4 Vs: PGAVSS00, PGAVSS001Interrupt Sources and DTC/DMAC Transfer Requests 1007
35.4.1 Interrupt Requests 1007
35.5 Event Link Function 1010

35.5.1 Event Output to the ELC ... 1010
35.5.2 ADC12 Operation through an Event from the ELC ... 1010
35.6 Usage Notes ... 1010
35.6.1 Constraints on Reading the Data Registers ... 1010
35.6.2 Constraints on Stopping A/D Conversion ... 1010
35.6.3 A/D Conversion Restart and Termination Timing ... 1011
35.6.4 Constraints on Scan End Interrupt Handling ... 1011
35.6.5 Settings for the Module-Stop Function ... 1011
35.6.6 Notes on Entering the Low Power States ... 1012
35.6.7 Error in Absolute Accuracy when Disconnection Detection Assistance Is in Use ... 1012
35.6.8 Available functions and register settings of AN000 to AN002, AN007, AN100 to AN102, and AN107 ... 1012
35.6.9 Notes on Operating Modes and Status Bits ... 1013
35.6.10 Notes on Board Design ... 1013
35.6.11 Constraints on Noise Prevention ... 1014
35.6.12 Port Settings when Using the ADC12 Input ... 1014
35.6.13 Relationship between ADC12 Units 0 and 1 and the ACMPHS ... 1014
36. 12-Bit D/A Converter (DAC12) ... 1016
36.1 Overview ... 1016
36.2 Register Descriptions ... 1017
36.2.1 D/A Data Register m (DADRm) (m = 0, 1) ... 1017
36.2.2 D/A Control Register (DACR) ... 1017
36.2.3 DADRm Format Select Register (DADPR) ... 1019
36.2.4 D/A A/D Synchronous Start Control Register (DAADSCR) ... 1019
36.2.5 D/A Output Amplifier Control Register (DAAMPCR) ... 1020
36.2.6 D/A Amplifier Stabilization Wait Control Register (DAASWCR) ... 1020
36.2.7 D/A A/D Synchronous Unit Select Register (DAADUSR) ... 1021
36.3 Operation ... 1021
36.3.1 Reducing Interference between D/A and A/D Conversion ... 1022
36.4 Event Link Operation Setting Procedure ... 1024
36.4.1 DA0 Event Link Operation Setting Procedure ... 1024
36.4.2 DA1 Event Link Operation Setting Procedure ... 1024
36.5 Usage Notes on Event Link Operation ... 1024
36.6 Usage Notes ... 1024
36.6.1 Settings for the Module-Stop Function ... 1024
36.6.2 DAC12 Operation in the Module-Stop State ... 1024
36.6.3 DAC12 Operation in Software Standby Mode ... 1025
36.6.4 Restriction on Entering Deep Software Standby Mode ... 1025
36.6.5 Initialization Procedure with the Output Amplifier ... 1025
36.6.6 Restriction on Usage when Interference Reduction between D/A and A/D Conversion is Enabled ... 1025

37. Temperature Sensor (TSN) 1026
37.1 Overview 1026
37.2 Register Descriptions 1027
37.2.1 Temperature Sensor Control Register (TSCR) 1027
37.2.2 Temperature Sensor Calibration Data Register (TSCDR) 1027
37.3 Using the Temperature Sensor 1027
37.3.1 Preparation for Using the Temperature Sensor 1027
37.3.2 Procedure for Using the Temperature Sensor 1028
37.4 Usage Notes 1030
37.4.1 Settings for the Module-Stop Function 1030
37.4.2 Constraints 1030
38. High-Speed Analog Comparator (ACMPHS) 1031
38.1 Overview 1031
38.2 Register Descriptions 1032
38.2.1 Comparator Control Register (CMPCTL) 1032
38.2.2 Comparator Input Select Register (CMPSEL0) 1033
38.2.3 Comparator Reference Voltage Select Register (CMPSEL1) 1033
38.2.4 Comparator Output Monitor Register (CMPMON) 1034
38.2.5 Comparator Output Control Register (CPIOC) 1034
38.3 Operation 1034
38.4 Noise Filter 1036
38.5 ACMPHS Interrupts 1037
38.6 ACMPHS Output to the Event Link Controller (ELC) 1037
38.7 ACMPHS Pin Output 1037
38.8 Usage Notes 1037
38.8.1 Settings for the Module-Stop Function 1037
38.8.2 Relationship with the ADC12 1037
39. Data Operation Circuit (DOC) 1038
39.1 Overview 1038
39.2 Register Descriptions 1039
39.2.1 DOC Control Register (DOCR) 1039
39.2.2 DOC Data Input Register (DODIR) 1040
39.2.3 DOC Data Setting Register (DODSR) 1040
39.3 Operation 1040
39.3.1 Data Comparison Mode 1040
39.3.2 Data Addition Mode 1041
39.3.3 Data Subtraction Mode 1041
39.4 Interrupt Request and Output to the Event Link Controller (ELC) 1042
39.5 Usage Notes 1042
39.5.1 Settings for the Module-Stop State 1042

40. SRAM 1043
40.1 Overview 1043
40.2 Register Descriptions 1043
40.2.1 SRAM Parity Error Operation After Detection Register (PARIOAD) 1043
40.2.2 SRAM Protection Register (SRAMPRCR) 1044
40.3 Operation 1044
40.3.1 Low-Power Functions 1044
40.3.2 Parity Calculation Function 1044
40.3.3 SRAM Error Sources 1046
40.3.4 Access Cycles 1046
40.4 Usage Notes 1047
40.4.1 Instruction Fetch from SRAM Area 1047
40.4.2 Store Buffer of SRAM 1047
41. Flash Memory 1048
41.1 Overview 1048
41.2 Memory Structure 1049
41.3 Flash Cache 1050
41.3.1 Overview 1050
41.3.2 Register Descriptions 1051
41.4 Operation 1052
41.4.1 Notice to use Flash Cache 1053
41.5 Operating Modes Associated with the Flash Memory 1053
41.5.1 ID Code Protection 1053
41.6 Overview of Functions 1054
41.6.1 Configuration Area Bit Map 1056
41.6.2 Startup Area Select 1056
41.6.3 Protection by Access Window 1057
41.7 Programming Commands 1059
41.8 Suspend Operation 1059
41.9 Protection 1060
41.10 Serial Programming Mode 1060
41.10.1 SCI Boot Mode 1060
41.11 Using a Serial Programmer 1060
41.11.1 Serial Programming 1061
41.11.2 Programming Environments 1061
41.12 Self-Programming 1061
41.12.1 Overview 1061
41.12.2 Background Operation 1061
41.13 Reading the Flash Memory 1062
41.13.1 Reading the Code Flash Memory 1062
41.13.2 Reading the Data Flash Memory 1062
41.14 Usage Notes 1062

41.14.1 Reading Areas where Programming or Erasure was Interrupted 1062
41.14.2 Restrictions on Additional Writes 1062
41.14.3 Reset during Programming and Erasure 1062
41.14.4 Allocation of Vectors for Interrupts and Other Exceptions during Programming and Erasure 1062
41.14.5 Restrictions during Programming and Erasure 1062
41.14.6 Abnormal Termination of Programming and Erasure 1062
42. Internal Voltage Regulator 1063
42.1 Overview 1063
42.2 Operation 1063
43. Electrical Characteristics 1064
43.1 Absolute Maximum Ratings 1064
43.2 DC Characteristics 1065
43.2.1 T_j/T_a Definition 1065
43.2.2 I/O V_{IH}, V_{IL} 1065
43.2.3 I/O I_{OH}, I_{OL} 1066
43.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics 1067
43.2.5 Operating and Standby Current 1068
43.2.6 VCC Rise and Fall Gradient and Ripple Frequency 1071
43.3 AC Characteristics 1071
43.3.1 Frequency 1071
43.3.2 Clock Timing 1072
43.3.3 Reset Timing 1075
43.3.4 Wakeup Timing 1076
43.3.5 NMI and IRQ Noise Filter 1078
43.3.6 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing 1079
43.3.7 PWM Delay Generation Circuit Timing 1081
43.3.8 CAC Timing 1081
43.3.9 SCI Timing 1082
43.3.10 SPI Timing 1087
43.3.11 IIC Timing 1091
43.4 ADC12 Characteristics 1094
43.5 DAC12 Characteristics 1098
43.6 TSN Characteristics 1098
43.7 OSC Stop Detect Characteristics 1098
43.8 POR and LVD Characteristics 1099
43.9 ACMPHS Characteristics 1102
43.10 PGA Characteristics 1102
43.11 Flash Memory Characteristics 1103
43.11.1 Code Flash Memory Characteristics 1103
43.11.2 Data Flash Memory Characteristics 1105
43.12 Boundary Scan 1105

43.13 Joint Test Action Group (JTAG) 1107
43.14 Serial Wire Debug (SWD) 1108
43.15 Embedded Trace Macro Interface (ETM) 1109
Appendix 1. Port States in Each Processing Mode 1110
Appendix 2. Package Dimensions 1113
Appendix 3. I/O Registers 1115
3.1 Peripheral Base Addresses 1115
3.2 Access Cycles 1117
3.3 Register Descriptions 1118
Revision History 1144

Leading performance 120-MHz Arm® Cortex®-M4 core, up to 512 KB of code flash memory, 64-KB SRAM, security and safety features, and advanced analog.

Features

■ Arm Cortex-M4 Core with Floating Point Unit (FPU)
- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 120 MHz
- Support for 4-GB address space
- On-chip debugging system: JTAG, SWD, and ETM
- Boundary scan and Arm Memory Protection Unit (Arm MPU)

■ Memory
- Up to 512-KB code flash memory (40 MHz zero wait states)
- 8-KB data flash memory (125,000 erase/write cycles)
- 64-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

■ Connectivity
- Serial Communications Interface (SCI) with FIFO × 7
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 2
- CAN module (CAN) × 1
- IrDA interface

■ Analog
- 12-bit A/D Converter (ADC12) with 3 sample-and-hold circuits each × 2
- 12-bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 6
- Programmable Gain Amplifier (PGA) × 6
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-bit Enhanced High Resolution (GPT32EH) × 4
- General PWM Timer 32-bit Enhanced (GPT32E) × 4
- General PWM Timer 32-bit (GPT32) × 5
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management
- Low power modes
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 8
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption
- AES128/192/256
- 3DES/ARC4
- SHA1/SHA224/SHA256/MD5
- GHASH
- RSA/DSA/ECC
- True Random Number Generator (TRNG)

■ Multiple Clock Sources
- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General-Purpose I/O Ports
- Up to 76 input/output pins
  - Up to 9 CMOS input
  - Up to 67 CMOS input/output
    - Up to 14 input/output 5 V tolerant
    - Up to 13 high current (20 mA)

■ Operating Voltage
- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages
- Ta = -40°C to +105°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M4 core running up to 120 MHz with the following features:

- Up to 512-KB code flash memory
- 64-KB SRAM
- Security and safety features
- 12-bit A/D Converter (ADC12)
- 12-bit D/A Converter (DAC12)
- Analog peripherals.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M4 core	• Maximum operating frequency: up to 120 MHz • Arm Cortex-M4 core: - Revision: r0p1-01rel0 - Armv7E-M architecture profile - Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008. • Arm Memory Protection Unit (Arm MPU): - Armv7 Protected Memory System Architecture - 8 protect regions. • SysTick timer: - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Up to 512-KB code flash memory. See section 41, Flash Memory.
Data flash memory	8-KB data flash memory. See section 41, Flash Memory.
Memory Mirror Function (MMF)	The Memory Mirror Function (MMF) can be configured to mirror the target application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. Your application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF).
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory.
SRAM	On-chip high-speed SRAM. See section 40, SRAM.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI boot mode. See section 3, Operating Modes.

Table 1.3 System (2 of 2)

Feature	Functional description
Resets	14 resets: • RES pin reset • Power-on reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • Independent watchdog timer reset • Watchdog timer reset • Deep Software Standby reset • SRAM parity error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD).
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • IDWT-dedicated on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC).
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 13, Interrupt Controller Unit (ICU).
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 20, Key Interrupt Function (KINT).
Low power modes	Power consumption can be reduced in multiple ways, such as by setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 12, Register Write Protection.
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 15, Memory Protection Unit (MPU).
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 25, Watchdog Timer (WDT).
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 26, Independent Watchdog Timer (IWDT).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 18, Event Link Controller (ELC).

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 17, Data Transfer Controller (DTC).
DMA Controller (DMAC)	An 8-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 16, DMA Controller (DMAC).

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with 13 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 22, General PWM Timer (GPT).
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 21, Port Output Enable for GPT (POEG).
Low Power Asynchronous General-Purpose Timer (AGT)	The Low Power Asynchronous General-Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 24, Low Power Asynchronous General-Purpose Timer (AGT).

Table 1.7 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 27, Serial Communications Interface (SCI).
IrDA Interface (IrDA)	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 28, IrDA Interface.
I^2C bus interface (IIC)	The 2-channel I^2C bus interface (IIC) conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions. See section 29, I^2C Bus Interface (IIC).
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 31, Serial Peripheral Interface (SPI).

Table 1.7 Communication interfaces (2 of 2)

Feature	Functional description
Controller Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 30, Controller Area Network (CAN) Module.

Table 1.8 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	Up to two successive approximation 12-bit A/D Converters (ADC12) are provided. In unit 0, up to 11 analog input channels are selectable. In unit 1, up to eight analog input channels, the temperature sensor output, and an internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit, 10-bit, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 35, 12-Bit A/D Converter (ADC12).
12-bit D/A Converter (DAC12)	A 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 36, 12-Bit D/A Converter (DAC12).
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 37, Temperature Sensor (TSN).
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 38, High-Speed Analog Comparator (ACMPHS).

Table 1.9 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 32, Cyclic Redundancy Check (CRC) Calculator.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 39, Data Operation Circuit (DOC).

Table 1.10 Security

Feature	Functional description
Secure Crypto Engine 7 (SCE7)	• Security algorithms: - Symmetric algorithms: AES, 3DES, and ARC4 - Asymmetric algorithms: RSA, DSA, and ECC. • Other support features: - TRNG (True Random Number Generator) - Hash-value generation: SHA1, SHA224, SHA256, GHASH, and MD5 - 128-bit unique ID.

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

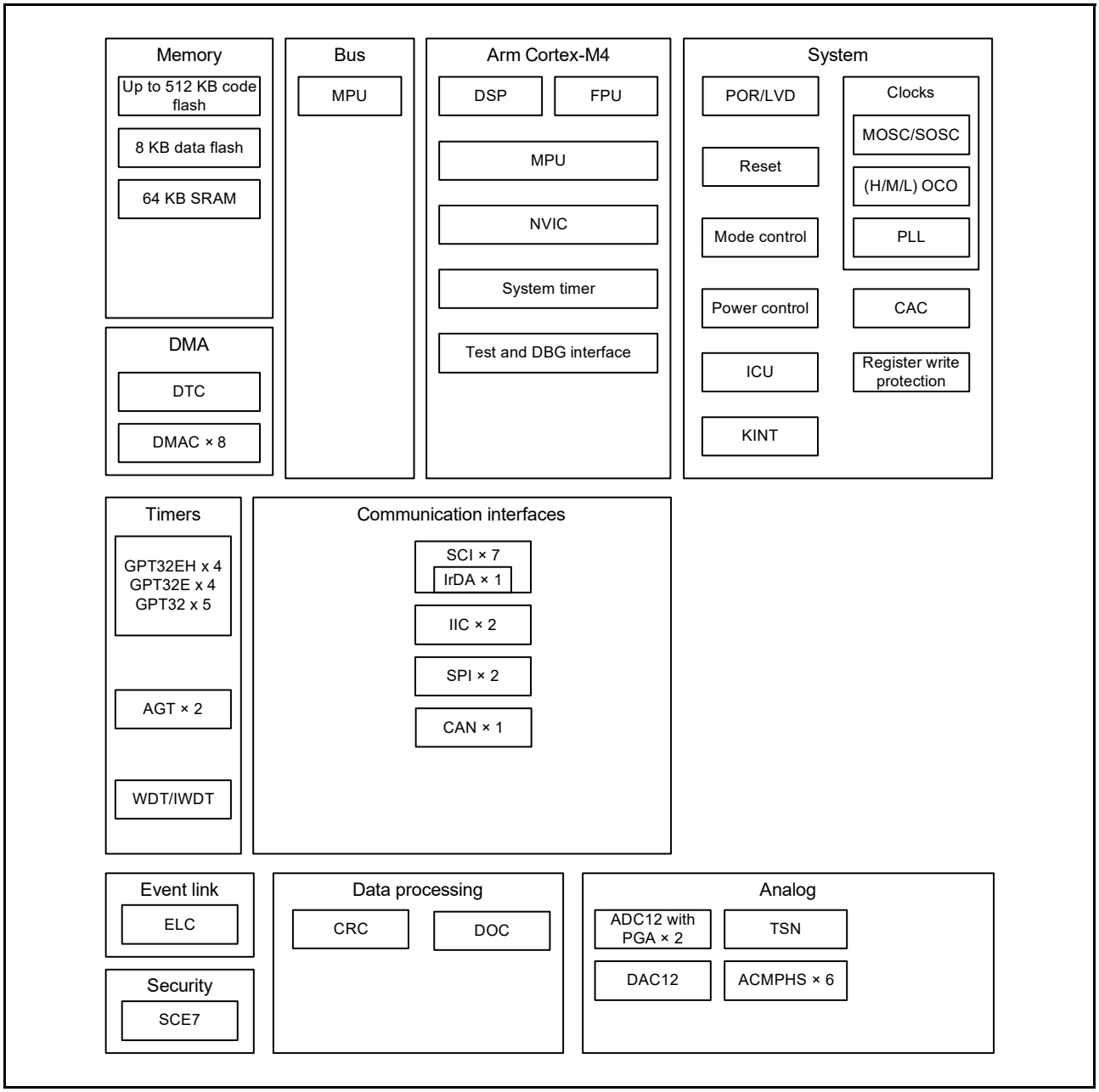


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.11 shows a list of products.

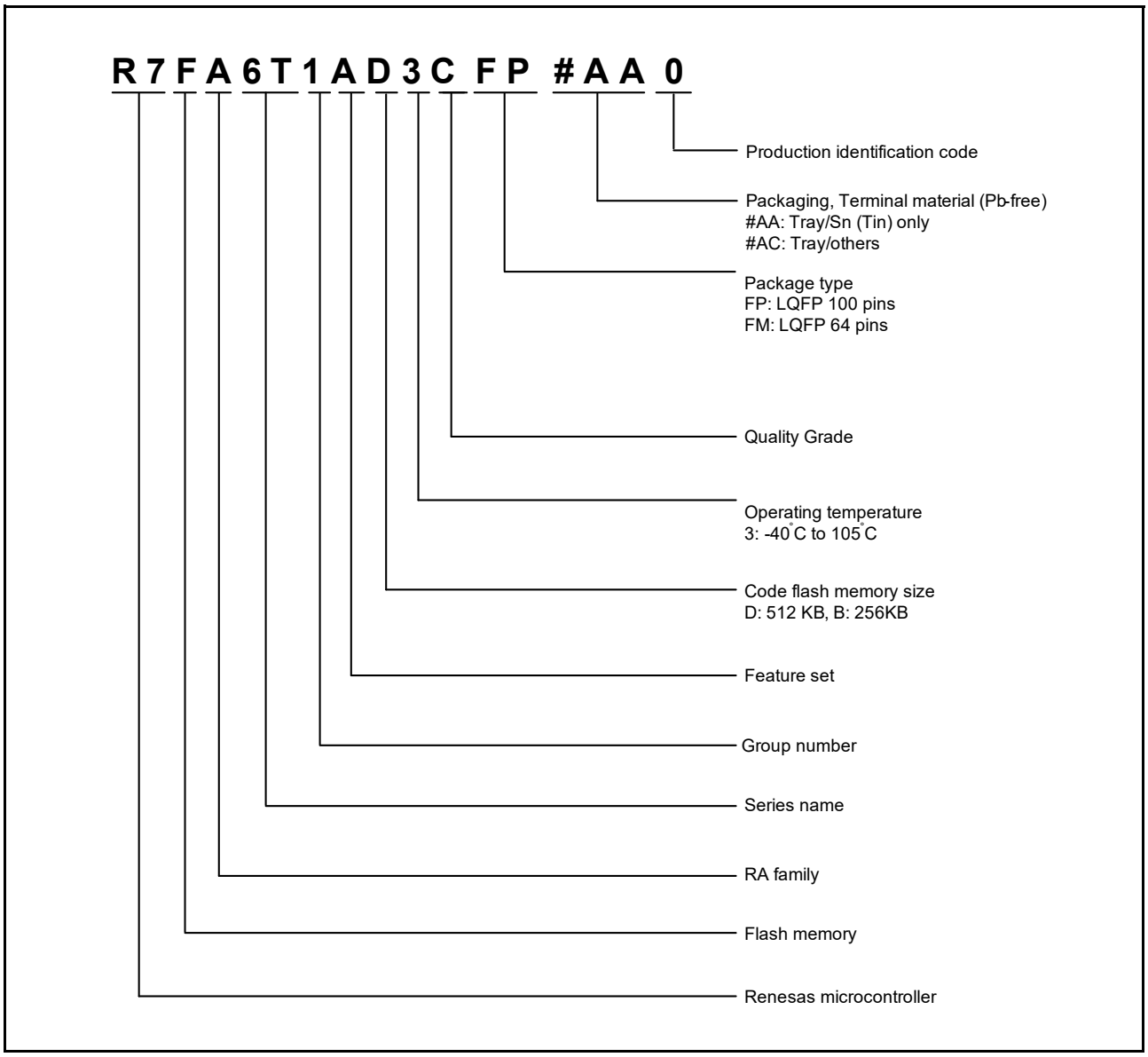


Figure 1.2 Part numbering scheme

Table 1.11 Product list

Product part number	Orderable part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA6T1AD3CFP	R7FA6T1AD3CFP#AA0	PLQP0100KB-B	512 KB	8 KB	64 KB	-40 to +105°C
R7FA6T1AB3CFP	R7FA6T1AB3CFP#AA0	PLQP0100KB-B	256 KB			-40 to +105°C
R7FA6T1AD3CFM	R7FA6T1AD3CFM#AA0	PLQP0064KB-C	512 KB			-40 to +105°C
R7FA6T1AB3CFM	R7FA6T1AB3CFM#AA0	PLQP0064KB-C	256 KB			-40 to +105°C

1.4 Function Comparison

Table 1.12 Functional comparison

Function		Part numbers			
		R7FA6T1AD3CFP	R7FA6T1AB3CFP	R7FA6T1AD3CFM	R7FA6T1AB3CFM
Pin count		100		64	
Package		LQFP		LQFP	
Code flash memory		256 KB/512 KB			
Data flash memory		8 KB			
SRAM		64 KB			
	Parity	64 KB			
System	CPU clock	120 MHz			
	Backup registers	512 Bytes			
	ICU	Yes			
	KINT	8			
Event link	ELC	Yes			
DMA	DTC	Yes			
	DMAC	8			
Timers	GPT32EH	4			
	GPT32E	4		3	
	GPT32	5		4	
	AGT	2			
	WDT/IWDT	Yes			
Communication	SCI	7			
	IIC	2			
	SPI	2			
	CAN	1			
Analog	ADC12	19		10	
	DAC12	2			
	ACMPHS	6			
	TSN	Yes			
Data processing	CRC	Yes			
	DOC	Yes			
Security		SCE7			

1.5 Pin Functions

Table 1.13 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. This is used as the digital power supply for the respective modules and internal voltage regulator, and used to monitor the voltage of the POR/LVD. Connect this pin to the system power supply. Connect it to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin.
	VCL0	Input	Connect this pin to VSS through a 0.1-μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VCL	Input	
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ13	Input	Maskable interrupt request pins
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins
On-chip emulator	TMS	I/O	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	This pin outputs the clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
	SWO	Output	Serial wire trace output pin
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOC0A to GTIOC12A, GTIOC0B to GTIOC12B	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable signals
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Output compare match A output pins
	AGTOB0, AGTOB1	Output	Output compare match B output pins

Table 1.13 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCK0 to SCK4, SCK8, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0 to RXD4, RXD8, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0 to TXD4, TXD8, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0 to CTS4_RTS4, CTS8_RTS8, CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0 to SCL4, SCL8, SCL9	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDA0 to SDA4, SDA8, SDA9	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCK0 to SCK4, SCK8, SCK9	I/O	Input/output pins for the clock (simple SPI mode)
	MISO0 to MISO4, MISO8, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI0 to MOSI4, MOSI8, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SS0 to SS4, SS8, SS9	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCL0, SCL1	I/O	Input/output pins for the clock
	SDA0, SDA1	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to VCC when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002
	VREFH	Input	Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to VCC when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to VSS when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.
ADC12	AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020	Input	Input pins for the analog signals to be processed by the ADC12
	AN100 to AN102, AN105 to AN107, AN116, AN117	Input	
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion
	ADTRG1	Input	
	PGAVSS000, PGAVSS100	Input	Pseudo-differential input pins

Table 1.13 Pin functions (3 of 3)

Function	Signal	I/O	Description
DAC12	DA0, DA1	Output	Output pins for the analog signals processed by the D/A converter
ACMPHS	VCOUT	Output	Comparator output pin
	IVREF0 to IVREF3	Input	Reference voltage input pins for comparator
	IVCMP0 to IVCMP3	Input	Analog voltage input pins for comparator
I/O ports	P000 to P007	Input	General-purpose input pins
	P008, P014, P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P205 to P214	I/O	General-purpose input/output pins
	P300 to P307	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P504, P508	I/O	General-purpose input/output pins
	P600 to P602, P608 to P610	I/O	General-purpose input/output pins
	P708	I/O	General-purpose input/output pin

1.6 Pin Assignments

Figure 1.3 and Figure 1.4 show the pin assignments.

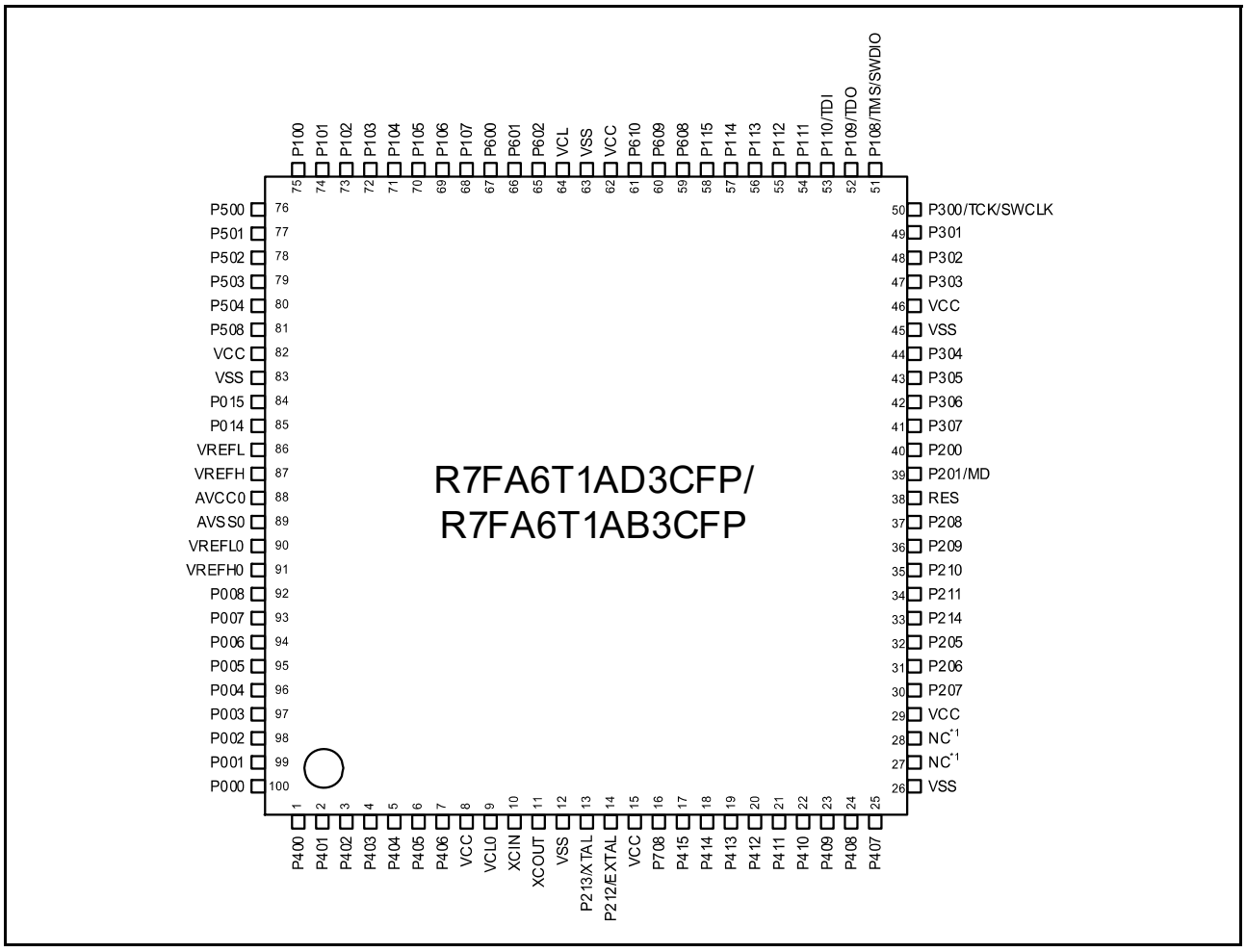


Figure 1.3 Pin assignment for 100-pin LQFP (top view)

Note 1. This pin should be left floating.

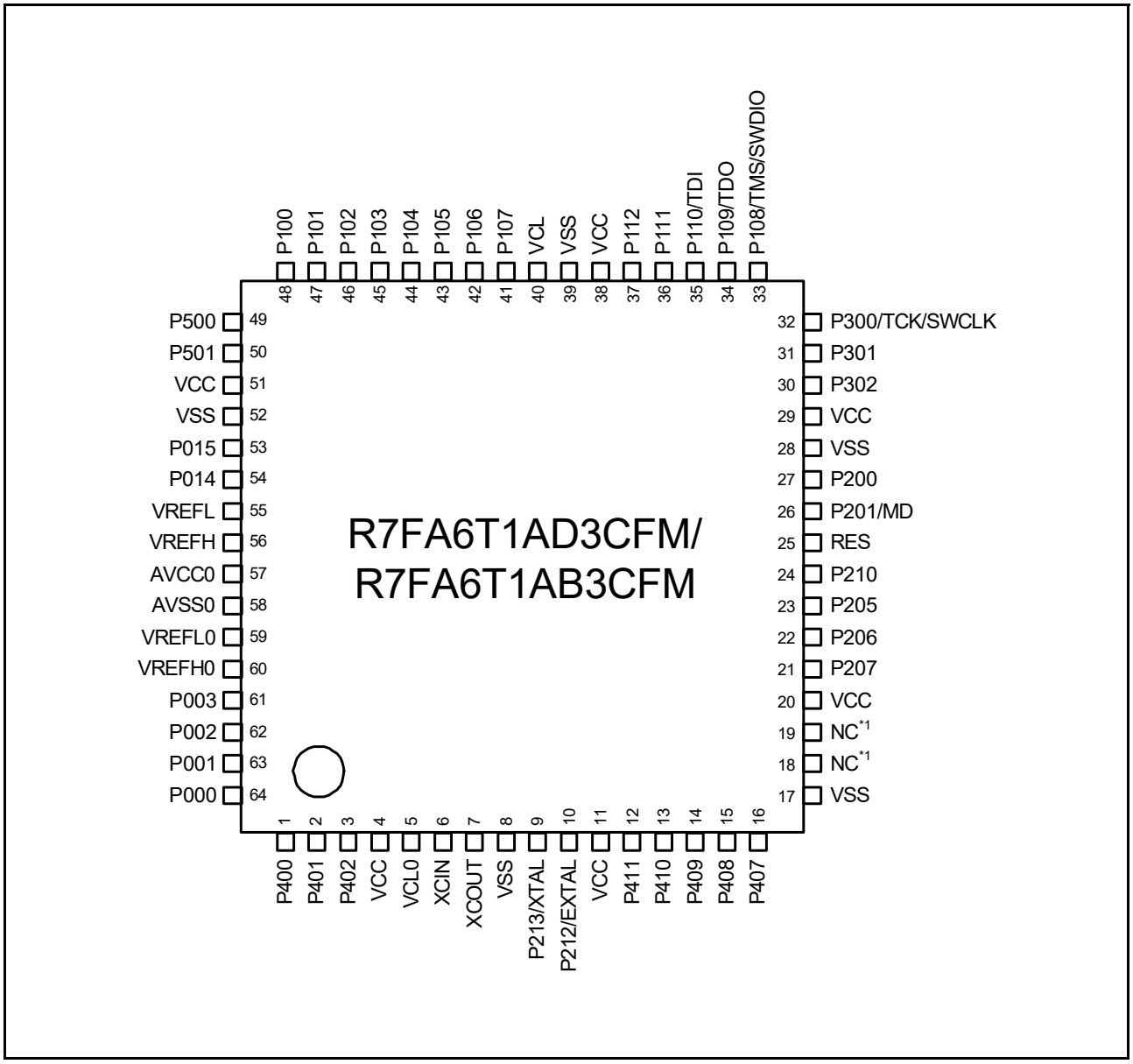


Figure 1.4 Pin assignment for 64-pin LQFP (top view)

Note 1. This pin should be left floating.

1.7 Pin Lists

Pin number					Timers			Communication interfaces					Analog	
LQFP100	LQFP64	Power, System, Clock, Debug, CAC	Interrupt	I/O port	AGT	GPT	GPT	CAN	SCI0,2,4,8 (30 MHz)	SCI1,3,9 (30 MHz)	IIC	SPI	ADC12	DAC12, ACMPHS
1	1	-	IRQ0	P400	AGTIO1	-	GTIOC6A	-	SCK4	-	SCL0_A	-	ADTRG1	-
2	2	-	IRQ5-DS	P401	-	GTETRGA	GTIOC6B	CTX0	CTS4_RTS4/SS4	-	SDA0_A	-	-	-
3	3	CACREF	IRQ4-DS	P402	AGTIO0/AGTIO1	-	-	CRX0	-	-	-	-	-	-
4	-	-	-	P403	AGTIO0/AGTIO1	-	GTIOC3A	-	-	-	-	-	-	-
5	-	-	-	P404	-	-	GTIOC3B	-	-	-	-	-	-	-
6	-	-	-	P405	-	-	GTIOC1A	-	-	-	-	-	-	-
7	-	-	-	P406	-	-	GTIOC1B	-	-	-	-	-	-	-
8	4	VCC	-	-	-	-	-	-	-	-	-	-	-	-
9	5	VCL0	-	-	-	-	-	-	-	-	-	-	-	-
10	6	XCIN	-	-	-	-	-	-	-	-	-	-	-	-
11	7	XCOUT	-	-	-	-	-	-	-	-	-	-	-	-
12	8	VSS	-	-	-	-	-	-	-	-	-	-	-	-
13	9	XTAL	IRQ2	P213	-	GTETRGC	GTIOC0A	-	-	TXD1/MOSI1/SDA1	-	-	ADTRG1	-
14	10	EXTAL	IRQ3	P212	AGTEE1	GTETRGD	GTIOC0B	-	-	RXD1/MISO1/SCL1	-	-	-	-
15	11	VCC	-	-	-	-	-	-	-	-	-	-	-	-
16	-	CACREF	IRQ11	P708	-	-	-	-	-	RXD1/MISO1/SCL1	-	SSLA3_B	-	-
17	-	-	IRQ8	P415	-	-	GTIOC0A	-	-	-	-	SSLA2_B	-	-
18	-	-	IRQ9	P414	-	-	GTIOC0B	-	-	-	-	SSLA1_B	-	-
19	-	-	-	P413	-	GTOUUP	-	-	CTS0_RTS0/SS0	-	-	SSLA0_B	-	-
20	-	-	-	P412	AGTEE1	GTOULO	-	-	SCK0	-	-	RSPCKA_B	-	-
21	12	-	IRQ4	P411	AGTOA1	GTOVUP	GTIOC9A	-	TXD0/MOSI0/SDA0	CTS3_RTS3/SS3	-	MOSIA_B	-	-
22	13	-	IRQ5	P410	AGTOB1	GTOVLO	GTIOC9B	-	RXD0/MISO0/SCL0	SCK3	-	MISOA_B	-	-
23	14	-	IRQ6	P409	-	GTOWUP	GTIOC10A	-	-	TXD3/MOSI3/SDA3	-	-	-	-
24	15	-	IRQ7	P408	-	GTOWLO	GTIOC10B	-	-	RXD3/MISO3/SCL3	SCL0_B	-	-	-
25	16	-	-	P407	AGTIO0	-	-	-	CTS4_RTS4/SS4	-	SDA0_B	-	ADTRG0	-
26	17	VSS	-	-	-	-	-	-	-	-	-	-	-	-
27	18	-	-	-	-	-	-	-	-	-	-	-	-	-
28	19	-	-	-	-	-	-	-	-	-	-	-	-	-
29	20	VCC	-	-	-	-	-	-	-	-	-	-	-	-
30	21	-	-	P207	-	-	-	-	-	-	-	-	-	-
31	22	-	IRQ0-DS	P206	-	GTIU	-	-	RXD4/MISO4/SCL4	-	SDA1_A	-	-	-
32	23	CLKOUT	IRQ1-DS	P205	AGTO1	GTIV	GTIOC4A	-	TXD4/MOSI4/SDA4	CTS9_RTS9/SS9	SCL1_A	-	-	-
33	-	TRCLK	-	P214	-	GTIU	-	-	-	-	-	-	-	-
34	-	TRDATA0	-	P211	-	GTIV	-	-	-	-	-	-	-	-
35	24	TRDATA1	-	P210	-	GTIW	-	-	-	-	-	-	-	-
36	-	TRDATA2	-	P209	-	GTOVUP	-	-	-	-	-	-	-	-
37	-	TRDATA3	-	P208	-	GTOVLO	-	-	-	-	-	-	-	-
38	25	RES	-	-	-	-	-	-	-	-	-	-	-	-
39	26	MD	-	P201	-	-	-	-	-	-	-	-	-	-
40	27	-	NMI	P200	-	-	-	-	-	-	-	-	-	-
41	-	-	-	P307	-	GTOUUP	-	-	-	-	-	-	-	-
42	-	-	-	P306	-	GTOULO	-	-	-	-	-	-	-	-
43	-	-	IRQ8	P305	-	GTOWUP	-	-	-	-	-	-	-	-
44	-	-	IRQ9	P304	-	GTOWLO	GTIOC7A	-	-	-	-	-	-	-
45	28	VSS	-	-	-	-	-	-	-	-	-	-	-	-
46	29	VCC	-	-	-	-	-	-	-	-	-	-	-	-
47	-	-	-	P303	-	-	GTIOC7B	-	-	-	-	-	-	-
48	30	-	IRQ5	P302	-	GTOUUP	GTIOC4A	-	TXD2/MOSI2/SDA2	-	-	SSLB3_B	-	-
49	31	-	IRQ6	P301	AGTIO0	GTOULO	GTIOC4B	-	RXD2/MISO2/SCL2	CTS9_RTS9/SS9	-	SSLB2_B	-	-
50	32	TCK/SWCLK	-	P300	-	GTOUUP	GTIOC0A_A	-	-	-	-	SSLB1_B	-	-
51	33	TMS/SWDIO	-	P108	-	GTOULO	GTIOC0B_A	-	-	CTS9_RTS9/SS9	-	SSLB0_B	-	-
52	34	CLKOUT/TDO/SWO	-	P109	-	GTOVUP	GTIOC1A_A	-	-	TXD9/MOSI9/SDA9	-	MOSIB_B	-	-
53	35	TDI	IRQ3	P110	-	GTOVLO	GTIOC1B_A	-	CTS2_RTS2/SS2	RXD9/MISO9/SCL9	-	MISOB_B	-	VCOUT
54	36	-	IRQ4	P111	-	-	GTIOC3A_A	-	SCK2	SCK9	-	RSPCKB_B	-	-
55	37	-	-	P112	-	-	GTIOC3B_A	-	TXD2/MOSI2/SDA2	SCK1	-	SSLB0_B	-	-
56	-	-	-	P113	-	-	GTIOC2A	-	RXD2/MISO2/SCL2	-	-	-	-	-
57	-	-	-	P114	-	-	GTIOC2B	-	-	-	-	-	-	-
58	-	-	-	P115	-	-	GTIOC4A	-	-	-	-	-	-	-
59	-	-	-	P608	-	-	GTIOC4B	-	-	-	-	-	-	-

Pin number					Timers			Communication interfaces					Analog	
LQFP100	LQFP64	Power, System, Clock, Debug, CAC	Interrupt	I/O port	AGT	GPT	GPT	CAN	SCI0,2,4,8 (30 MHz)	SCI1,3,9 (30 MHz)	IIC	SPI	ADC12	DAC12, ACMPHS
60	-	-	-	P609	-	-	GTIOC5A	-	-	-	-	-	-	-
61	-	-	-	P610	-	-	GTIOC5B	-	-	-	-	-	-	-
62	38	VCC	-	-	-	-	-	-	-	-	-	-	-	-
63	39	VSS	-	-	-	-	-	-	-	-	-	-	-	-
64	40	VCL	-	-	-	-	-	-	-	-	-	-	-	-
65	-	-	-	P602	-	-	GTIOC7B	-	-	TXD9	-	-	-	-
66	-	-	-	P601	-	-	GTIOC6A	-	-	RXD9	-	-	-	-
67	-	CLKOUT/CACREF	-	P600	-	-	GTIOC6B	-	-	SCK9	-	-	-	-
68	41	-	KR07	P107	AGTOA0	-	GTIOC8A	-	CTS8_RTS8/SS8	-	-	-	-	-
69	42	-	KR06	P106	AGTOB0	-	GTIOC8B	-	SCK8	-	-	SSLA3_A	-	-
70	43	-	IRQ0/KR05	P105	-	GTETRGA	GTIOC1A	-	TXD8/MOSI8/SDA8	-	-	SSLA2_A	-	-
71	44	-	IRQ1/KR04	P104	-	GTETRGB	GTIOC1B	-	RXD8/MISO8/SCL8	-	-	SSLA1_A	-	-
72	45	-	KR03	P103	-	GTOWUP	GTIOC2A_A	CTX0	CTS0_RTS0/SS0	-	-	SSLA0_A	-	-
73	46	-	KR02	P102	AGTO0	GTOWLO	GTIOC2B_A	CRX0	SCK0	-	-	RSPCKA_A	ADTRG0	-
74	47	-	IRQ1/KR01	P101	AGTEE0	GTETRGB	GTIOC5A	-	TXD0/MOSI0/SDA0	CTS1_RTS1/SS1	SDA1_B	MOSIA_A	-	-
75	48	-	IRQ2/KR00	P100	AGTIO0	GTETRGA	GTIOC5B	-	RXD0/MISO0/SCL0	SCK1	SCL1_B	MISOA_A	-	-
76	49	-	-	P500	AGTOA0	GTIU	GTIOC11A	-	-	-	-	-	AN016	IVREF0
77	50	-	IRQ11	P501	AGTOB0	GTIV	GTIOC11B	-	-	-	-	-	AN116	IVREF1
78	-	-	IRQ12	P502	-	GTIW	GTIOC12A	-	-	-	-	-	AN017	IVCMP0
79	-	-	-	P503	-	GTETRGC	GTIOC12B	-	-	-	-	-	AN117	-
80	-	-	-	P504	-	GTETRGD	-	-	-	-	-	-	AN018	-
81	-	-	-	P508	-	-	-	-	-	-	-	-	AN020	-
82	51	VCC	-	-	-	-	-	-	-	-	-	-	-	-
83	52	VSS	-	-	-	-	-	-	-	-	-	-	-	-
84	53	-	IRQ13	P015	-	-	-	-	-	-	-	-	AN006/AN106	DA1/IVCMP1
85	54	-	-	P014	-	-	-	-	-	-	-	-	AN005/AN105	DA0/IVREF3
86	55	VREFL	-	-	-	-	-	-	-	-	-	-	-	-
87	56	VREFH	-	-	-	-	-	-	-	-	-	-	-	-
88	57	AVCC0	-	-	-	-	-	-	-	-	-	-	-	-
89	58	AVSS0	-	-	-	-	-	-	-	-	-	-	-	-
90	59	VREFL0	-	-	-	-	-	-	-	-	-	-	-	-
91	60	VREFH0	-	-	-	-	-	-	-	-	-	-	-	-
92	-	-	IRQ12-DS	P008	-	-	-	-	-	-	-	-	AN003	-
93	-	-	-	P007	-	-	-	-	-	-	-	-	PGAVSS100/AN107	-
94	-	-	IRQ11-DS	P006	-	-	-	-	-	-	-	-	AN102	IVCMP2
95	-	-	IRQ10-DS	P005	-	-	-	-	-	-	-	-	AN101	IVCMP2
96	-	-	IRQ9-DS	P004	-	-	-	-	-	-	-	-	AN100	IVCMP2
97	61	-	-	P003	-	-	-	-	-	-	-	-	PGAVSS000/AN007	-
98	62	-	IRQ8-DS	P002	-	-	-	-	-	-	-	-	AN002	IVCMP2
99	63	-	IRQ7-DS	P001	-	-	-	-	-	-	-	-	AN001	IVCMP2
100	64	-	IRQ6-DS	P000	-	-	-	-	-	-	-	-	AN000	IVCMP2

Note: Some pin names have the added suffix of _A and _B. When assigning the GPT, IIC, and SPI functionality, select the functional pins with the same suffix.

2. CPU

The MCU is based on the Arm® Cortex®-M4 core.

2.1 Overview

2.1.1 CPU

- Arm Cortex-M4
  - Revision: r0p1-01rel0
  - Armv7E-M architecture profile
  - Single Precision Floating-Point Unit compliant with the ANSI/IEEE Std 754-2008.
- Memory Protection Unit (MPU)
  - Armv7 Protected Memory System Architecture
  - 8 protected regions.
- SysTick timer
  - Driven by SYSTICCLK (LOCO) or ICLK.

See reference 1. and reference 2. for details.

2.1.2 Debug

- Arm CoreSight™ ETM-M4
  - Revision: r0p1-00rel0
  - Arm ETM architecture version 3.5.
- CoreSight Instrumentation Trace Macrocell (ITM)
- Data Watchpoint and Trace Unit (DWT)
  - 4 comparators for watchpoints and triggers.
- Flash Patch and Breakpoint Unit (FPB)
  - Flash Patch (remap) function is not available, only Breakpoint function is available.
  - 6 instruction comparators
  - 2 literal comparators.
- CoreSight Time Stamp Generator (TSG)
  - Time stamp for ETM and ITM
  - Driven by CPU clock.
- Debug Register Module (DBGREG)
  - Reset control
  - Halt control.
- CoreSight Debug Access Port (DAP)
  - JTAG Debug Port (JTAG-DP)
  - Serial Wire Debug Port (SW-DP).
- Cortex-M4 Trace Port Interface Unit (TPIU)
  - 4-bit TPIU formatter output
  - Serial Wire Output.

- CoreSight Embedded Trace Buffer (ETB)
  - CoreSight Trace Memory Controller with ETB configuration
  - Buffer size: 2 KB.

See reference 1. and reference 2. for details.

2.1.3 Operating Frequency

The operating frequencies for the MCU are as follows:

- CPU: maximum 120 MHz
- 4-bit TPIU trace interface: maximum 60 MHz
- Serial Write Output (SWO) trace interface: maximum 60 MHz
- Joint Test Action Group (JTAG) interface: maximum 25 MHz
- Serial Wire Data (SWD) interface: maximum 25 MHz.

Figure 2.1 shows a block diagram of the Cortex-M4 core.

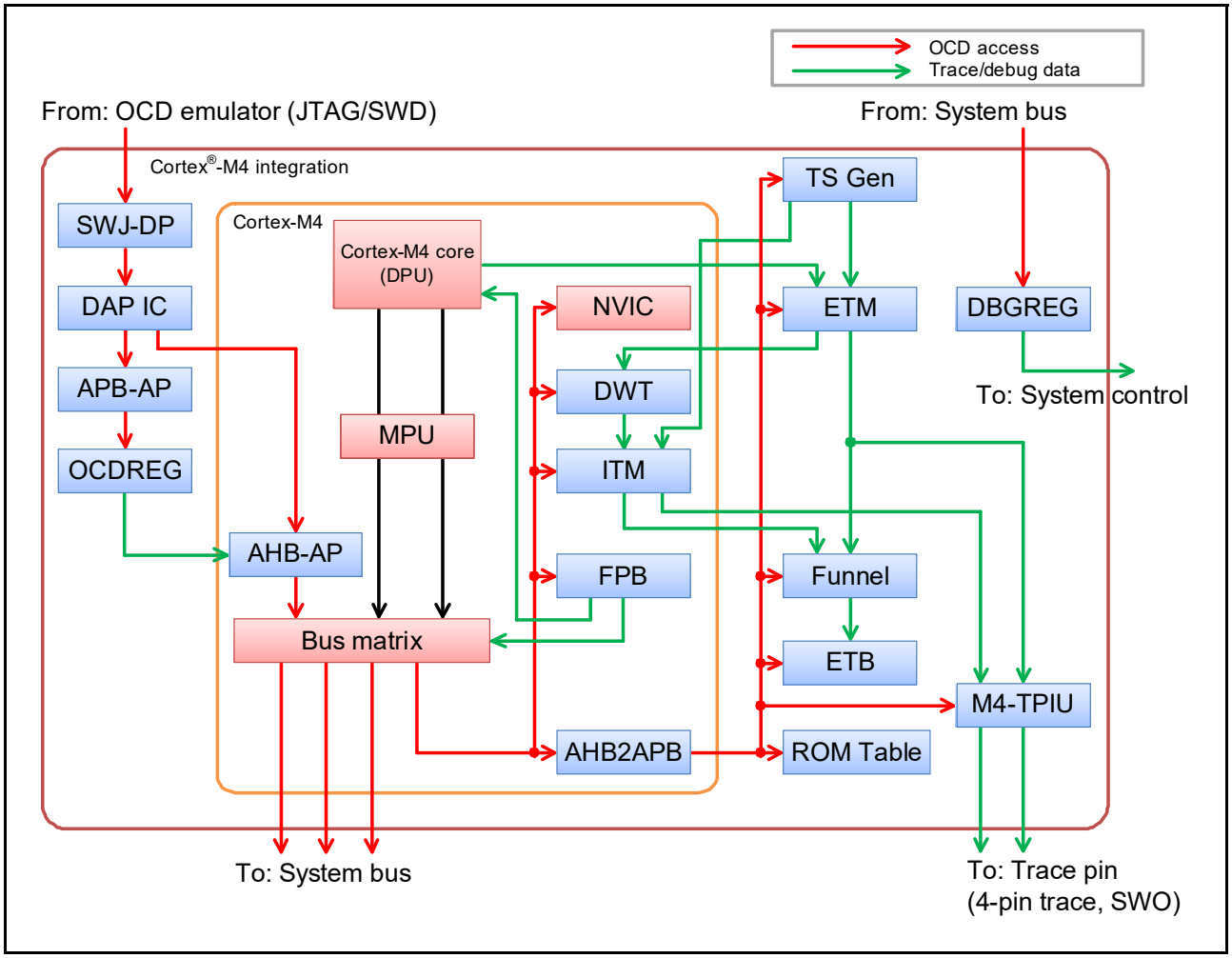


Figure 2.1 Cortex-M4 block diagram

2.2 MCU Implementation Options

Table 2.1 shows the implementation options of the MCU and is based on the configurable options in reference 2.

Table 2.1 Implementation options

Option	Implementation
MPU	Included, 8 protect regions
FPB	Flash Patch (remap) function is not available, only Breakpoint function is available
Breakpoint function	Included
FPU	Included
Number of interrupts	96
Number of priority bits	4
Number of Wakeup Interrupt Controllers (WIC*1)	Not included
Sleep mode power saving	Sleep mode and other low power modes are supported. For more details, see section 11, Low Power Modes. SCB.SCR.SLEEPDEEP is ignored.
Endianness	Little-endian
SysTick SYST_CALIB register	SYST_CALIB = 4000 0147h Bit [31] = 0 Reference clock provided Bit [30] = 1 TERMS value is inexact Bits [29:24] = 00h Reserved Bits [23:0] = 000147h TERM: (32768 × 10 ms) - 1 / 32.768 kHz = 326.66 decimal = 327 with skew = 000147h
Event input/output	Not implemented
System reset request output	The SYSRESETREQ bit in the Application Interrupt and Reset Control Register causes a CPU reset
Auxiliary fault inputs (AUXFAULT)	Not implemented

Note 1. The ICU can wake up the CPU instead of the Wakeup Interrupt Controller (WIC). For details, see section 13, Interrupt Controller Unit (ICU).

2.3 Trace Interface

A Trace Port Interface Unit (TPIU) and Serial Wire Output (SWO) provide trace output. Table 2.2 shows the MCU pins for the function. These pins are multiplexed with other functions.

Table 2.2 Trace function pins

Name	I/O	Width	Function
TCLK	Output	1 bit	Trace clock
TDATA0	Output	1 bit	Trace data output 0
TDATA1	Output	1 bit	Trace data output 1
TDATA2	Output	1 bit	Trace data output 2
TDATA3	Output	1 bit	Trace data output 3
TDO/SWO	Output	1 bit	Serial wire output multiplexed with JTAG TDO pin

2.4 JTAG/SWD Interface

Table 2.3 shows the JTAG/SWD pins.

Table 2.3 JTAG/SWD pins

Name	I/O	P/N	Width	Function	When not in use
TCK/SWCLK	Input	Positive	1 bit	JTAG clock pin	Pull-up
TMS/SWDIO	I/O	Negative	1 bit	JTAG TMS pin SWD I/O pin	Pull-up
TDI	Input	Positive	1 bit	JTAG TDI pin	Pull-up
TDO/SWO	Output	Negative	1 bit	JTAG TDO pin multiplexed with serial wire output	Open

2.5 Debug Mode

2.5.1 Debug Mode Definition

In single chip mode, the debugger connection state is defined as On-Chip Debugger (OCD) mode, and the non-connected debugger state is defined as User mode. Table 2.4 shows the CPU debug modes and usage conditions.

Table 2.4 CPU debug mode and conditions

Conditions		Mode	
OCD connect	**JTAG/SWD authentication**	**Debug mode**	**Debug authentication**
Not connected	—	User mode	Disabled
Connected	Failed	User mode	Disabled
Connected	Passed	OCD mode	Enabled

Note 1. OCD connect is determined by the CDBGPWRUPREQ bit output in the SWJ-DP register. The bit can only be written by the OCD. However, the level of the bit can be confirmed by reading the DBGSTR.CDBGPWRUPREQ bit.
Note 2. Debug authentication is defined by the Armv7-M architecture. Enabled means that both invasive and non-invasive CPU debugging are permitted. Disabled means that both are not permitted.

2.5.2 Debug Mode Effects

This section describes the effects of debug mode, which occur both internally and externally to the CPU.

2.5.2.1 Low power mode

All CoreSight debug components can store the register settings even when the CPU enters Software Standby, Snooze, or Deep Software Standby mode. However, AHB-AP cannot respond to On-Chip Debug (OCD) access in these low power modes. The OCD must wait for cancellation of the low power mode to access the CoreSight debug components. To request low power mode cancellation, the OCD can set the DBIRQ bit in the MCUCTRL register. For details, see section 2.6.5.3, MCU Control Register (MCUCTRL).

2.5.2.2 Reset

In OCD mode, some resets depend on the CPU status and the DBGSTOPCR setting.

Table 2.5 Reset or interrupt and mode setting (1 of 2)

	Control in On-Chip Debug (OCD) mode	
Reset or interrupt name	**OCD break mode**	**OCD run mode**
RES pin reset	Same as user mode	
Power-on reset	Same as user mode	
Independent watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting*2
Watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting*2
Voltage monitor 0 reset	Depends on DBGSTOPCR setting*3	
Voltage monitor 1 reset/interrupt	Depends on DBGSTOPCR setting*3	
Voltage monitor 2 reset/interrupt	Depends on DBGSTOPCR setting*3	

Table 2.5 Reset or interrupt and mode setting (2 of 2)

Reset or interrupt name	Control in On-Chip Debug (OCD) mode	
	OCD break mode	OCD run mode
SRAM parity error reset/interrupt	Depends on DBGSTOPCR setting*3	
MPU bus master reset/interrupt	Same as user mode	
MPU bus slave reset/interrupt	Same as user mode	
Stack pointer error reset/interrupt	Same as user mode	
Deep software standby reset	Same as user mode	
Software reset	Same as user mode	

Note: In OCD break mode, the CPU is halted. In OCD run mode, the CPU is in OCD mode and the CPU is not halted.
Note 1. The IWDT and WDT always stop in this mode.
Note 2. The IWDT and WDT operation depends on the DBGSTOPCR setting.
Note 3. Reset or interrupt masking depends on the DBGSTOPCR setting.

2.6 Programmers Model

2.6.1 Address Spaces

The MCU debug system includes two CoreSight Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCD register.

Figure 2.2 shows a block diagram of the AP connection and address spaces.

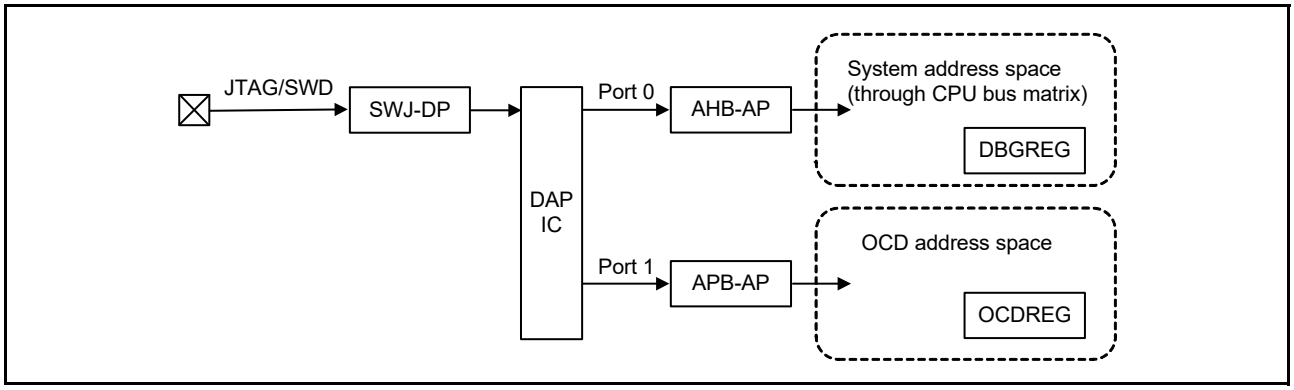


Figure 2.2 JTAG/SWD authentication block diagram

For debugging purposes, there are two register modules, DBGREG and OCDREG. DBGREG is located in the system address space and can be accessed from the OCD emulator, the CPU, and other bus masters in the MCU. OCDREG is located in the OCD address space and can only be accessed from the OCD tool. The CPU and other bus masters cannot access the OCD registers.

2.6.2 Cortex-M4 Peripheral Address Map

In the system address space, the Cortex-M4 core has a Private Peripheral Bus (PPB) that can only be accessed from the CPU and OCD emulator. The PPB is expanded from the Cortex-M4 original implementation for the MCU. Table 2.6 shows the address map of the MCU.

Table 2.6 Cortex-M4 peripheral address map (1 of 2)

Component name	Start address	End address	Note
ITM	E000 0000h	E000 0FFFh	See reference 2.
DWT	E000 1000h	E000 1FFFh	See reference 2.

Table 2.6 Cortex-M4 peripheral address map (2 of 2)

Component name	Start address	End address	Note
FPB	E000 2000h	E000 2FFFh	See reference 2.
SCS	E000 E000h	E000 EFFFh	See reference 2.
TPIU	E004 0000h	E004 0FFFh	See reference 2.
ETM	E004 1000h	E004 1FFFh	See reference 5.
ATB funnel	E004 2000h	E004 2FFFh	See section 2.7 and reference 4.
ETB	E004 3000h	E004 3FFFh	See reference 6.
Time Stamp Generator	E004 4000h	E004 4FFFh	See section 2.10 and reference 4.
ROM Table	E00F F000h	E00F FFFFh	See section 2.6.3 and reference 7.

2.6.3 CoreSight ROM Table

The MCU contains one CoreSight ROM Table, which lists the Arm components.

2.6.3.1 ROM entries

Table 2.7 shows the ROM entries in the CoreSight ROM Table. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 7. for details.

Table 2.7 CoreSight ROM Table

#	Address	Access size	R/W	Value	Component
0	E00F F000h	32 bits	R	FFF0 F003h	NVIC
1	E00F F004h	32 bits	R	FFF0 2003h	SWT
2	E00F F008h	32 bits	R	FFF0 3003h	FPB
3	E00F F00Ch	32 bits	R	FFF0 1003h	ITM
4	E00F F010h	32 bits	R	FFF4 1003h	TPIU
5	E00F F014h	32 bits	R	FFF4 2003h	ETM
6	E00F F018h	32 bits	R	FFF4 3003h	Funnel
7	E00F F01Ch	32 bits	R	FFF4 4003h	ETB
8	E00F F020h	32 bits	R	FFF4 5003h	TSG
9	E00F F024h	32 bits	R	0000 0000h	End of entries

2.6.3.2 CoreSight component registers

The CoreSight ROM Table lists the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.8 shows the registers. See reference 7. for details of each register.

Table 2.8 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
DEVTYPE	E00F FFCCh	32 bits	R	0000 0001h
PID4	E00F FFD0h	32 bits	R	0000 0004h
PID5	E00F FFD4h	32 bits	R	0000 0000h
PID6	E00F FFD8h	32 bits	R	0000 0000h
PID7	E00F FFDCh	32 bits	R	0000 0000h
PID0	E00F FFE0h	32 bits	R	0000 0027h
PID1	E00F FFE4h	32 bits	R	0000 0030h
PID2	E00F FFE8h	32 bits	R	0000 000Ah

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID3	E00F FFECh	32 bits	R	0000 0000h
CID0	E00F FFF0h	32 bits	R	0000 000Dh
CID1	E00F FFF4h	32 bits	R	0000 0010h
CID2	E00F FFF8h	32 bits	R	0000 0005h
CID3	E00F FFFCh	32 bits	R	0000 00B1h

2.6.4 DBGREG Module

The DBGREG module controls the debug functionalities and is implemented as a CoreSight-compliant component.

Table 2.9 shows the DBGREG registers other than the CoreSight component registers.

Table 2.9 Non-CoreSight DBGREG registers

Name		DAP port	Address	Access size	R/W
Debug Status Register	DBGSTR	Port 0	4001 B000h	32 bits	R
Debug Stop Control Register	DBGSTOPCR	Port 0	4001 B010h	32 bits	R/W
Trace Control Register	TRACECTR	Port 0	4001 B020h	32 bits	R/W

2.6.4.1 Debug Status Register (DBGSTR)

Address(es): DBG.DBGSTR 4001 B000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0	R
b28	CDBGPWRUPREQ	Debug power-up request	0: OCD is not requesting debug power-up 1: OCD is requesting debug power-up.	R
b29	CDBGPWRUPACK	Debug power-up acknowledge	0: Debug power-up request is not acknowledged 1: Debug power-up request is acknowledged.	R
b31, b30	—	Reserved	These bits are read as 0	R

2.6.4.2 Debug Stop Control Register (DBGSTOPCR)

Address(es): DBG.DBGSTOPCR 4001 B010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b0	DBGSTOP_IWDT	Mask bit for IWDT reset/interrupt	0: Enable IWDT reset/interrupt 1: Mask IWDT reset/interrupt and stop WDT count when CPU is in OCD break mode.	R/W
b1	DBGSTOP_WDT	Mask bit for WDT reset/interrupt	0: Enable WDT reset/interrupt 1: Mask WDT reset/interrupt and stop WDT count when CPU is in OCD break mode.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	DBGSTOP_LVD[2:0]	Mask bit for LVD0 reset	0: Enable LVD0 reset 1: Mask LVD0 reset.	R/W
b17		Mask bit for LVD1 reset/interrupt	0: Enable LVD1 reset/interrupt 1: Mask LVD1 reset/interrupt.	R/W
b18		Mask bit for LVD2 reset/interrupt	0: Enable LVD2 reset/interrupt 1: Mask LVD2 reset/interrupt.	R/W
b23 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	DBGSTOP_RPER	Mask bit for SRAM parity error reset/interrupt	0: Enable SRAM parity error reset/interrupt 1: Mask SRAM parity error reset/interrupt.	R/W
b31 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The Debug Stop Control Register (DBGSTOPCR) specifies the functional stop in OCD mode. All bits in the register are regarded as 0 when the MCU is not in OCD mode.

2.6.4.3 Trace Control Register (TRACECTR)

Address(es): DBG.TRACECTR 4001 B020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ENETBFULL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b30 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	ENETBFULL	Enable bit for halt request on ETB full	0: ETB full does not cause a CPU halt 1: ETB full causes a CPU halt.	R/W

2.6.4.4 DBGREG CoreSight component registers

The DBGREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.10 shows these registers. See reference 7. for details of each register.

Table 2.10 DBGREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	4001 BFD0h	32 bits	R	0000 0004h
PID5	4001 BFD4h	32 bits	R	0000 0000h
PID6	4001 BFD8h	32 bits	R	0000 0000h
PID7	4001 BFDCh	32 bits	R	0000 0000h
PID0	4001 BFE0h	32 bits	R	0000 0005h
PID1	4001 BFE4h	32 bits	R	0000 0030h
PID2	4001 BFE8h	32 bits	R	0000 001Ah
PID3	4001 BFECh	32 bits	R	0000 0000h
CID0	4001 BFF0h	32 bits	R	0000 000Dh
CID1	4001 BFF4h	32 bits	R	0000 00F0h
CID2	4001 BFF8h	32 bits	R	0000 0005h
CID3	4001 BFFCh	32 bits	R	0000 00B1h

2.6.5 OCDREG Module

The OCDREG register module controls the On-Chip Debug (OCD) emulator functionalities and is implemented as a CoreSight-compliant component.

Table 2.11 shows the OCDREG registers other than the CoreSight component registers.

Table 2.11 Non-CoreSight OCDREG registers

Name		DAP port	Address	Access size	R/W
ID Authentication Code Register 0	IAUTH0	Port 1	8000 0000h	32 bits	W
ID Authentication Code Register 1	IAUTH1	Port 1	8000 0100h	32 bits	W
ID Authentication Code Register 2	IAUTH2	Port 1	8000 0200h	32 bits	W
ID Authentication Code Register 3	IAUTH3	Port 1	8000 0300h	32 bits	W
MCU Status Register	MCUSTAT	Port 1	8000 0400h	32 bits	R
MCU Control Register	MCUCTRL	Port 1	8000 0410h	32 bits	R/W

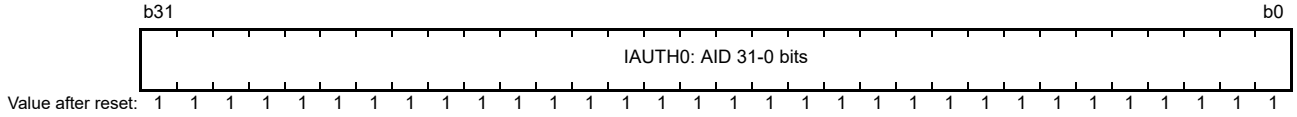
Note: OCDREG is located in the dedicated OCD address space. This address map is independent from the system address map. See section 2.6.2, Cortex-M4 Peripheral Address Map.

2.6.5.1 ID Authentication Code Register (IAUTH0 to 3)

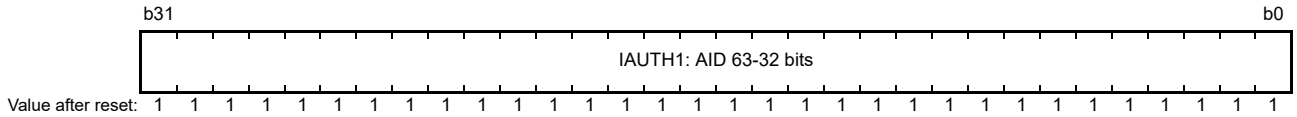
Four authentication registers are provided for writing the 128-bit key. These registers must be written in sequential order from IAUTH0 to IAUTH3. If the set of register writes is not compliant with this order, the result is unpredictable.

Only 32-bit writes are permitted. The initial value of the registers is all 1s. This means that JTAG/SWD access is initially permitted when the ID code in the OSIS register has the initial value. See section 2.11.2, Unlock ID Code.

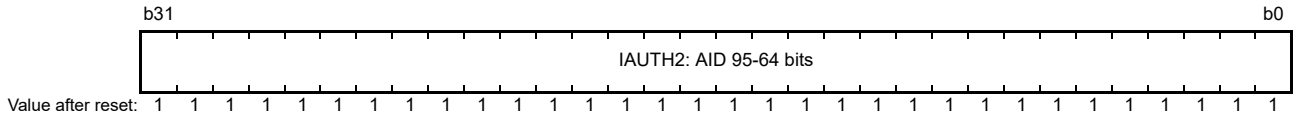
Address(es): IAUTH0 8000 0000h



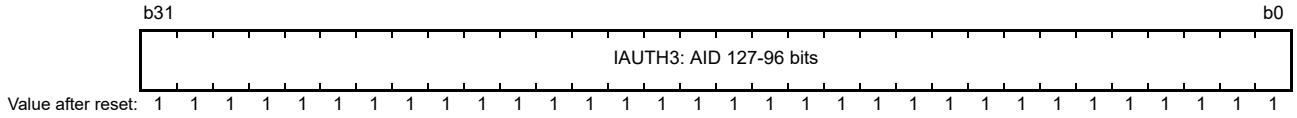
Address(es): IAUTH1 8000 0100h



Address(es): IAUTH2 8000 0200h



Address(es): IAUTH3 8000 0300h



2.6.5.2 MCU Status Register (MCUSTAT)

Address(es): MCUSTAT 8000 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	AUTH
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1/0*1	1/0*1	0

Bit	Symbol	Bit name	Description	R/W
b0	AUTH	Authentication status	0: Authentication failed 1: Authentication succeeded.	R
b1	CPUSLEEP		0: CPU is not in Sleep mode 1: CPU is in Sleep mode.	R
b2	CPUSTOPCLK		0: CPU clock is not stopped. This indicates that the MCU is in Normal or Sleep mode 1: CPU clock is stopped. This indicates that the MCU is in Snooze or Software Standby mode.	R
b31 to b3	—	Reserved	These bits are read as 0.	R

Note 1. Depends on the MCU status.

2.6.5.3 MCU Control Register (MCUCTRL)

Address(es): MCUCTRL 8000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	EDBGRQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EDBGRQ	External Debug Request	Writing 1 to the bit causes a CPU halt or debug monitor exception: 0: Debug event not requested 1: Debug event requested. When the EDBGRQ bit is set to 0 or the CPU is halted, the EDBCRQ bit is cleared.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DBIRQ	Debug Interrupt Request	Writing 1 to the bit wakes up the MCU from low power mode: 0: Debug interrupt not requested 1: Debug interrupt requested. The condition can be cleared by writing 0 to the DBIRQ bit.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set DBIRQ and EDBGRQ to the same value.

2.6.5.4 OCDREG CoreSight component registers

The OCDREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.12 shows these registers. See reference 7. for details of each register.

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	8000 0FD0h	32 bits	R	0000 0004h
PID5	8000 0FD4h	32 bits	R	0000 0000h
PID6	8000 0FD8h	32 bits	R	0000 0000h
PID7	8000 0FDCh	32 bits	R	0000 0000h
PID0	8000 0FE0h	32 bits	R	0000 0004h
PID1	8000 0FE4h	32 bits	R	0000 0030h
PID2	8000 0FE8h	32 bits	R	0000 000Ah
PID3	8000 0FECh	32 bits	R	0000 0000h
CID0	8000 0FF0h	32 bits	R	0000 000Dh
CID1	8000 0FF4h	32 bits	R	0000 00F0h
CID2	8000 0FF8h	32 bits	R	0000 0005h
CID3	8000 0FFCh	32 bits	R	0000 00B1h

2.7 CoreSight ATB Funnel

There is one CoreSight ATB funnel in the MCU. The funnel has two ATB slaves and one ATB master, and it selects the debug trace source from ETM and ITM to ETB. Figure 2.3 shows the CoreSight ATB connection in the MCU.

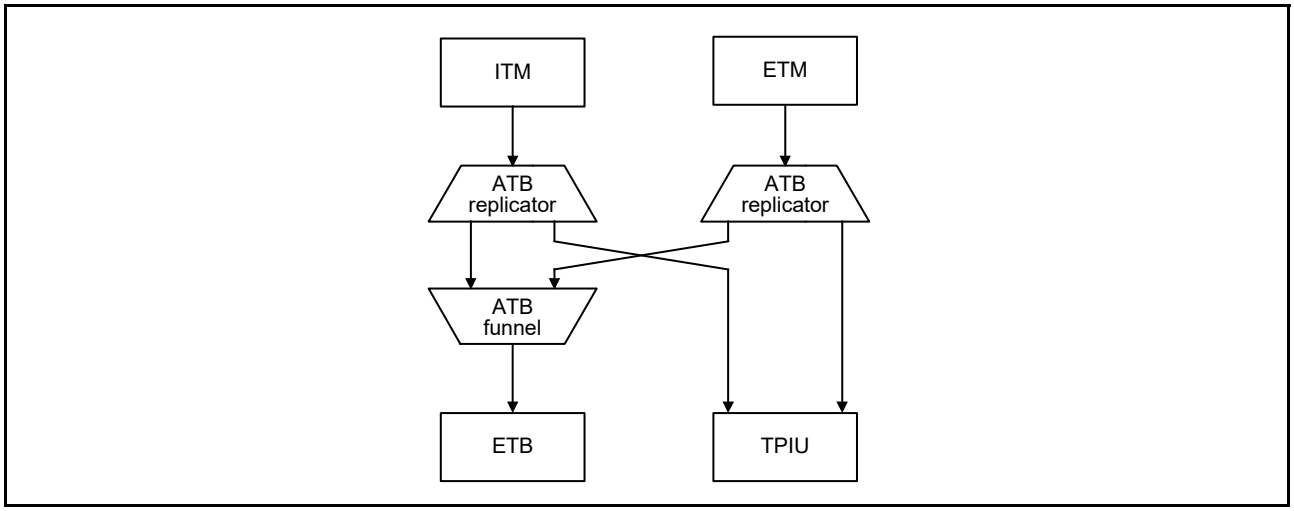


Figure 2.3 CoreSight ATB connection

Table 2.13 shows the ATB slave connection for the funnel.

Table 2.13 ATB slave connection

ATB slave number	Connected trace source
#0	ITM
#1	ETM

For details of the ATB and funnel, see reference 4.

2.8 Flash Patch and Break Unit

The MCU has a flash patch and break unit. Breakpoint function is available, but flash patch (remap) function is not available. Therefore, do not set the REPLACE bits [31:30] in the FP_COMPn register to 0. Bit [28] of FP_REMAP register is always set to 1. When writing to this register, write 1 to bit [28]. When reading this register, bit [28] is always read as 1. See reference 1.*2.9 for details.

2.9 SysTick System Timer

The SysTick system timer provides a simple 24-bit down counter. The reference clock for the timer can be selected as the CPU clock (ICLK) or SysTick Timer clock (SYSTICCLK). See section 9, Clock Generation Circuit and reference 1.*1 for details.

Note 1. In the reference, the IMPLEMENTATION DEFINED external reference clock is SYSTICCLK (LOCO) and the processor clock is ICLK.

2.10 CoreSight Time Stamp Generator

A CoreSight Time Stamp Generator provides a CPU clock-based timestamp to ITM and ETM. The 48 LSB bits of the 64-bit counter are used for the two components. See reference 4. for details.

2.11 OCD Emulator Connection

A JTAG/SWD authentication mechanism checks access permission for debug and MCU resources. To obtain full debug functionality, a pass result of the authentication mechanism is required.

Figure 2.4 shows a block diagram of the authentication mechanism.

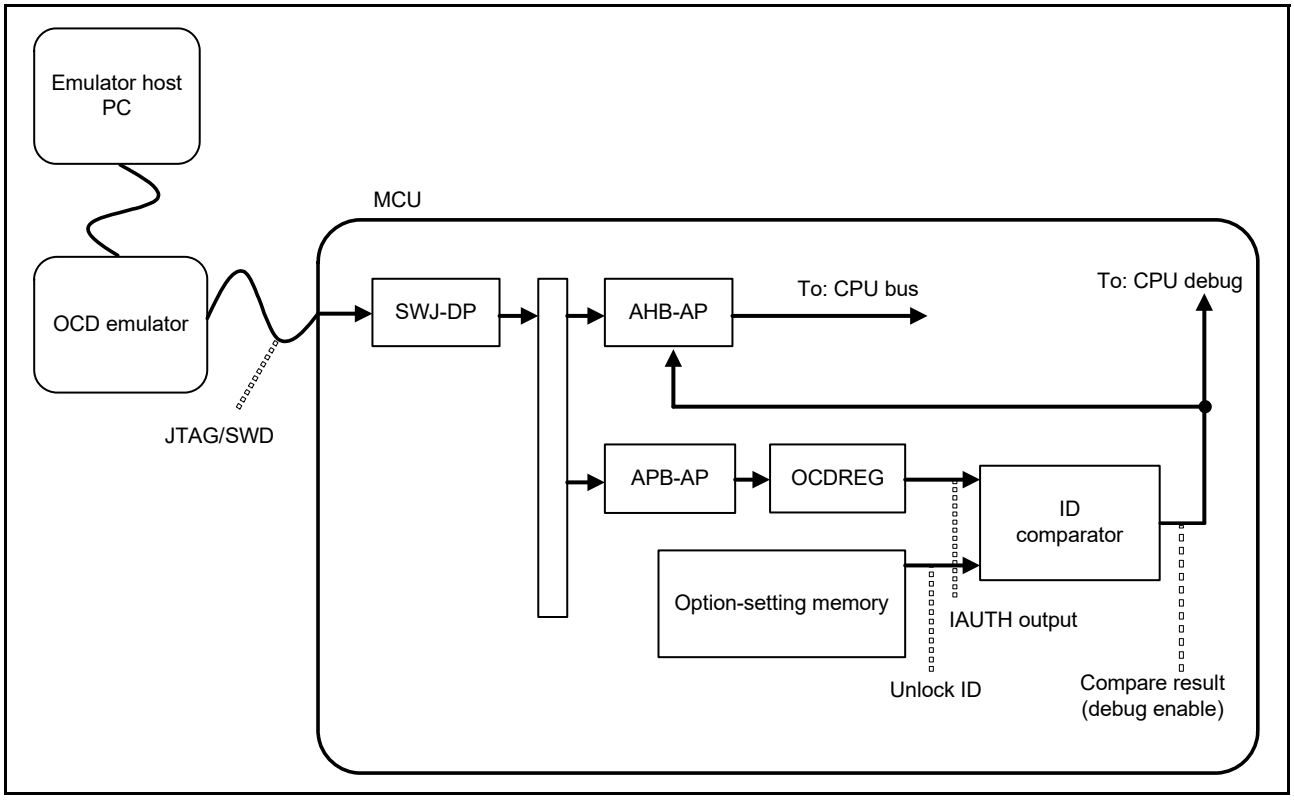


Figure 2.4 Authentication mechanism block diagram

An ID comparator is available in the MCU for authentication. The comparator compares the 128-bit IAUTH output from OCDREG and the 128-bit unlock ID code from the option-setting memory. When the two outputs are identical, the CPU debug functions and system bus access from the OCD emulator are permitted.

2.11.1 DBGEN

After the OCD emulator gets access permission, the OCD emulator must set the DBGEN bit in the System Control OCD Control Register (SYOCDCR). In addition, the OCD emulator must clear the DBGEN bit before disconnecting it. See section 11, Low Power Modes for details.

2.11.2 Unlock ID Code

The unlock ID code is used for checking permissions for debug and access to on-chip resources. If the unlock ID code matches the 128-bit data written in ID Authentication Registers 0 to 3, the JTAG/SWD debugger obtains access permission. Unlock ID code is written in the OCD/Serial Programmer ID Setting Register (OSIS) in the option-setting memory. The initial value of the unlock ID code is all 1s (FFFFFFFF_FFFFFFFF_FFFFFFFFh). See section 7, Option-Setting Memory for details.

2.11.3 Restrictions on Connecting an OCD Emulator

This section describes the restrictions on emulator access.

2.11.3.1 Starting connection while in low power mode

When starting a JTAG/SWD connection from an OCD emulator, the MCU must be in Normal or Sleep mode. If the MCU is in Software Standby, Snooze, or Deep Software Standby mode, the OCD emulator can cause the MCU to hang.

2.11.3.2 Changing low power mode while in OCD mode

When the MCU is in OCD mode, the low power mode can be changed. However, system bus access from AHB-AP is prohibited in Software Standby, Snooze, or Deep Software Standby mode. Only SWJ-DP, APB-AP, and OCDREG can be accessed from the OCD emulator in these modes. Table 2.14 shows the restrictions.

Table 2.14 Restrictions by mode

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Normal	Yes	Yes	Yes	Yes
Sleep	Yes	Yes	Yes	Yes
Software Standby	No	Yes	No	Yes
Snooze	No	Yes	No	Yes
Deep Software Standby	No	Yes	No	Yes

If system bus access is required in Software Standby, Snooze, or Deep Software Standby mode, set the OCUCTRL.DBIRG bit in OCDREG to wake up the MCU from the low power modes. Simultaneously, using the OCUCTRL.EDBGRQ bit in OCDREG, the OCD emulator can wake up the MCU without starting CPU execution by using a CPU break.

2.11.3.3 Modifying the unlock ID code in OSIS

After modifying the unlock ID code in the OSIS, the OCD emulator must reset the MCU by asserting the RES pin or setting the SYSRESETREQ bit of the Application Interrupt and Reset Control Register in the system control block to 1. The modified unlock ID code is reflected after reset.

2.11.3.4 Connecting sequence and JTAG/SWD authentication

Because the OCD emulator is protected by the JTAG/SWD authentication mechanism, the OCD might be required to input the ID code to the authentication registers. The OSIS value in the option-setting memory determines whether the code is required.

After the negation of the reset, a 5 µs wait time is required before comparing the OSIS value at cold start.

(1) When MSB of OSIS is 0 (bit [127] = 0)

The ID code is always mismatching and connection to the OCD is prohibited.

(2) When OSIS is all 1s (default)

OCD authentication is not required and the OCD can use the AHB-AP without authentication.

1. Connect the OCD emulator to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJ-DP Control Status Register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up the AHB-AP to access the system address space. The AHB-AP is connected to the DAP bus port 0.
4. Start accessing the CPU debug resources using the AHB-AP.

(3) When OSIS[127:126] = 10b

OCD authentication is required and the OCD must write the unlock ID code to the IAUTH registers 0 to 3 in the OCDREG before using the AHB-AP.

1. Connect the OCD debugger to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJ-DP Control Status Register, and wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up the APB-AP to access OCDREG. The APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in the OCDREG using the APB-AP.
5. If the 128-bit ID code matches the OSIS value, the AHB-AP is authorized to issue an AHB transaction. The authorization result can be confirmed by the AUTH bit in the MCUSTAT Register or the DbgStatus bit in the AHB-AP Control Status Word Register.
   - When the DbgStatus bit is 1, the 128-bit ID code is a match with the OSIS value. AHB transfers are permitted.

- When the DbgStatus bit is 0, the 128-bit ID code is not a match with the OSIS value. AHB transfers are not permitted.

6. Set up the AHB-AP to access the system address space. The AHB-AP is connected to the DAP bus port 0.
7. Start accessing the CPU debug resources using the AHB-AP.

(4) When OSIS[127:126] is 11b

OCD authentication is required and the OCD must write the unlock ID code to IAUTH registers 0 to 3 in the OCDREG. The connection sequence is the same when OSIS[127:126] is 10b except for "ALeRASE" capability.

When IATUH registers 0 to 3 are written with "ALeRASE" in ASCII code (414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the contents of the code flash, data flash, and configuration area are erased at once. See section 41, Flash Memory for details.

The ALeRASE sequence is as follows:

1. Connect the OCD debugger to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJDP Control Status Register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set the APB-AP to access OCDREG. The APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in the OCDREG using the APB-AP.
5. If the 128-bit ID code is "ALeRASE" in ASCII code, the contents of the code flash, data flash, and configuration area are erased. Thereafter, the MCU transitions to Sleep mode.

2.12 References

1. *ARM®v7-M Architecture Reference Manual* (ARM DDI 0403D).
2. *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D).
3. *ARM® Cortex®-M4 Devices Generic User Guide* (ARM DUI 0553A).
4. *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480F).
5. *ARM® CoreSight™ ETM-M4 Technical Reference Manual* (ARM DDI 0440C).
6. *ARM® CoreSight™ Trace Memory Controller Technical Reference Manual* (ARM DDI 0461B).
7. *ARM® CoreSight™ Architecture Specification* (ARM IHI 0029D).

3. Operating Modes

3.1 Overview

Table 3.1 shows the selection of operating modes by the mode-setting pin. For details, see section 3.2, Details of Operating Modes. Operation starts with the on-chip flash memory enabled, regardless of the mode in which operation started.

Table 3.1 Selection of operating modes by the mode-setting pin

Mode-setting pin MD	Operating mode	On-chip flash memory	External bus
1	Single-chip mode	Enable	Disable
0	SCI boot mode	Enable	Disable

3.2 Details of Operating Modes

3.2.1 Single-Chip Mode

In single-chip mode, all I/O pins are available for use as input or output port, inputs or outputs for peripheral functions, or as interrupt inputs. When a reset is released while the MD pin is high, the MCU starts in single-chip mode and the on-chip flash is enabled.

3.2.2 SCI Boot Mode

In this mode, the on-chip flash memory programming routine (SCI boot program), stored in a dedicated area within the MCU, is used. The on-chip flash, including the code flash memory and data flash memory, can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (UART) SCI. For details, see section 41, Flash Memory. The MCU starts in SCI boot mode if the MD pin is held low on release from the reset state.

3.3 Operating Mode Transitions

3.3.1 Operating Mode Transitions as Determined by the Mode-Setting Pin

Figure 3.1 shows operating mode transitions determined by the settings of the MD pin.

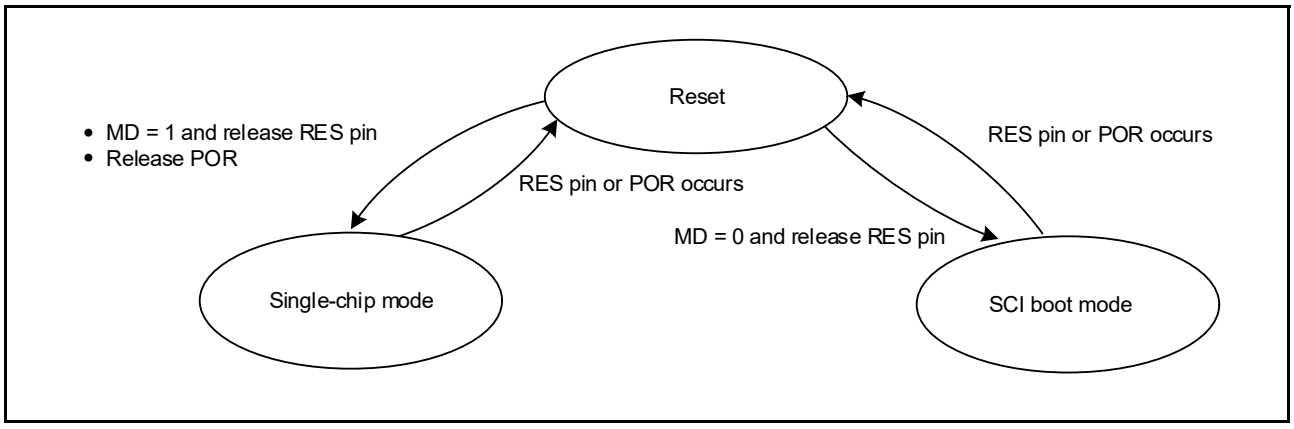
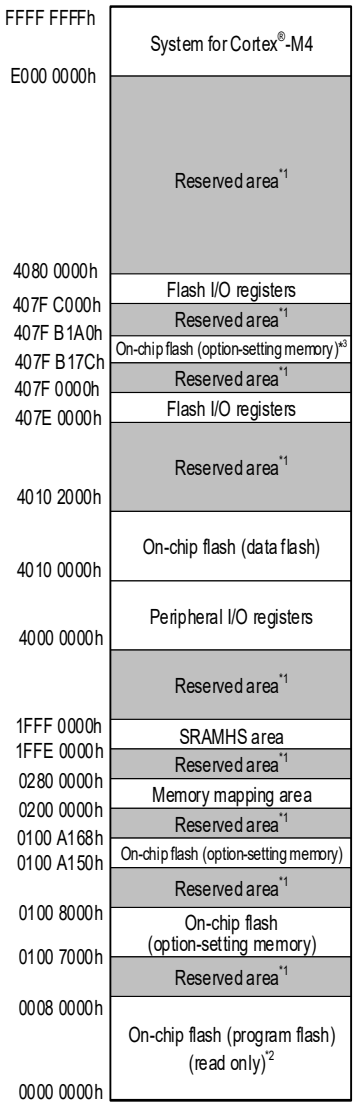


Figure 3.1 Mode-setting pin level and operating mode

4. Address Space

4.1 Overview

The MCU supports a 4-GB linear address space ranging from 0000 0000h to FFFF FFFFh that can contain both program and data. Figure 4.1 shows the memory map.



Note 1. Do not access reserved areas.
Note 2. Some regions are reserved for the option-setting memory. For details, see section 7, Option-Setting Memory.
Note 3. Do not access from 407F B180h to 407F B19Bh.

Figure 4.1 Memory map

5. Memory Mirror Function (MMF)

5.1 Overview

The MCU provides a Memory Mirror Function (MMF). You can configure the MMF to map an application image load address in the code flash memory to the application image link address in the unused 23-bit memory mirror space addresses. Your application code must be developed and linked to run from this MMF destination address. The application code is not required to know the load location where it is stored in the code flash memory.

Table 5.1 lists the MMF specifications.

Table 5.1 MMF specifications

Parameter	Specifications
Memory mirror space	8 MB (0200 0000h to 027F FFFFh)
Memory mirror boundary	128 bytes

5.2 Register Descriptions

5.2.1 MemMirror Special Function Register (MMSFR)

Address(es): MMF.MMSFR 4000 1000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	KEY[7:0]								—	MEMMIRADDR[15:9]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MEMMIRADDR[8:0]									—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b22 to b7	MEMMIRADDR[15:0]	Memory Mirror Address	0000h to FFFFh (8 MB)	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b31 to b24	KEY[7:0]	MMSFR Key Code	These bits enable or disable rewriting of the MEMMIRADDR bits	R/W

MEMMIRADDR[15:0] bits (Memory Mirror Address)

The MEMMIRADDR[15:0] bits specify bits [22:7] of the memory mirror address. They define where the start address of the memory mirror space addresses (0200 0000h) is linked to. Writing to these bits is enabled only when this register is accessed in 32-bit words and the value DBh is written to the KEY[7:0] bits.

KEY[7:0] bits (MMSFR Key Code)

The KEY[7:0] bits enable or disable rewriting of the MEMMIRADDR[15:0] bits. Data written to the KEY bits is not saved. These bits are read as 0. The KEY code and MEMMIRADDR[15:0] bits must be written in the same cycle.

5.2.2 MemMirror Enable Register (MMEN)

Address(es): MMF.MMEN 4000 1004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	KEY[7:0]								—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b0	EN	Memory Mirror Function Enable	0: Disable MMF 1: Enable MMF.	R/W
b23 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b24	KEY[7:0]	MMEN Key Code	These bits enable or disable rewriting of the EN bit.	R/W

EN bit (Memory Mirror Function Enable)

Writing to the EN bit is enabled only when the MemMirror Enable Register is accessed in 32-bit words and the value DBh is written to the KEY[7:0] bits.

KEY[7:0] bits (MMEN Key Code)

The KEY[7:0] bits enable or disable rewriting of the EN bit. Data written to the KEY[7:0] bits is not saved. These bits are read as 0. The KEY code and the EN bit must be written in the same cycle.

5.3 Operation

5.3.1 MMF Operation

The MMF links the memory mirror space (0200 0000h to 027F FFFFh) to the code flash area. If MMEN.EN = 1, the CPU can access code flash using both normal addresses (starting at 0000 0000h) and memory mirror space addresses (starting at 0200 0000h). Figure 5.1 shows an overview of the MMF. The MMSFR.MEMMIRADDR[15:0] bits specify where the start address of the memory mirror space addresses (0200 0000h) is linked to. Figure 5.2, Figure 5.3, and Figure 5.4 show the MMF operation. Figure 5.5 shows the setting procedure of the MMF.

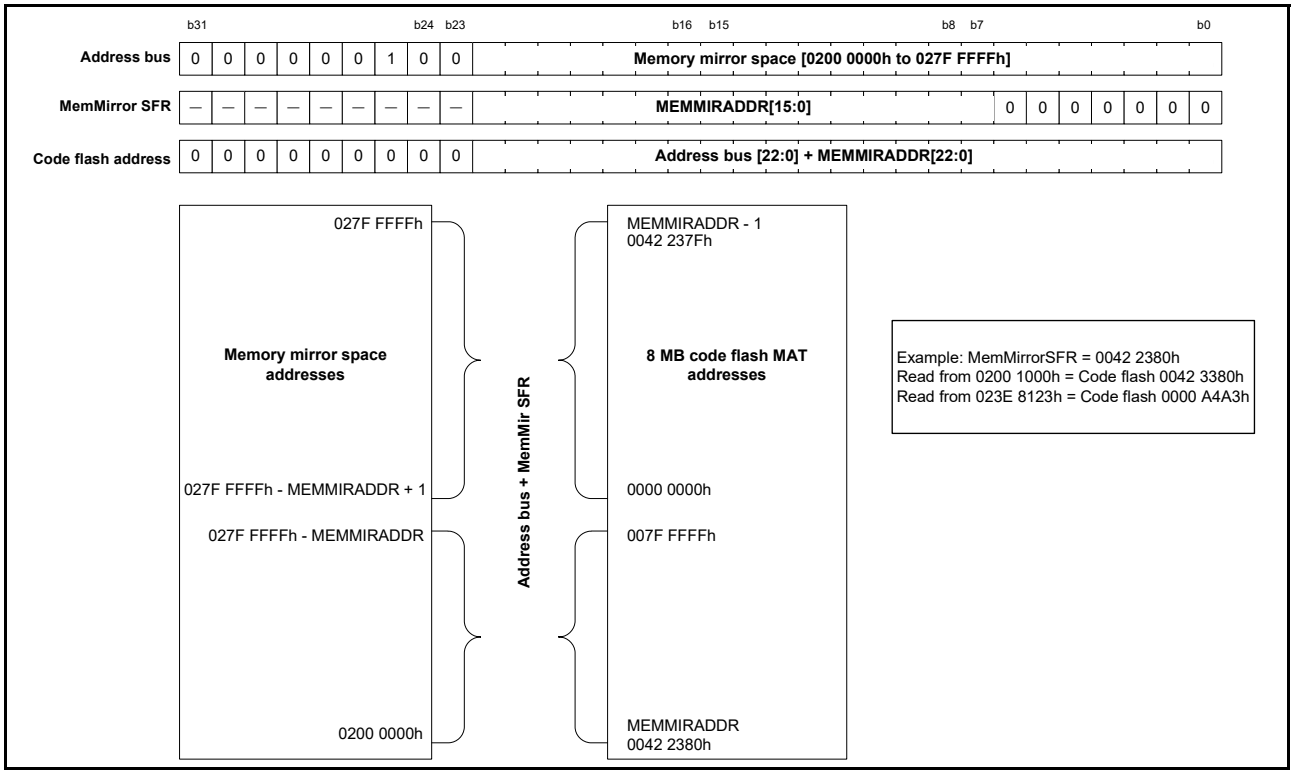
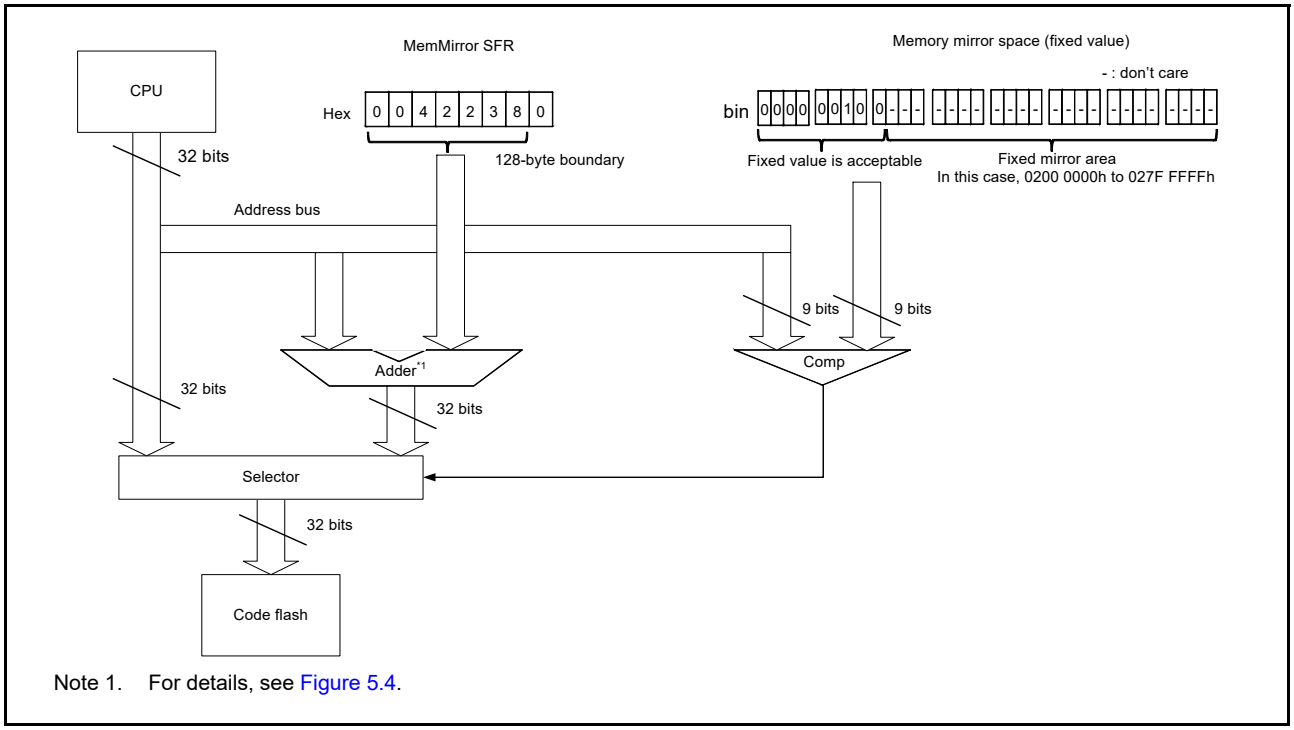


Figure 5.1 MMF operation



Note 1. For details, see Figure 5.4.

Figure 5.2 MMF block diagram

Figure 5.3 shows the addresses handled by each module. The Arm® MPU uses the original address of the CPU. The Security MPU and code flash memory each uses an address after conversion through the Memory Mirror Function.

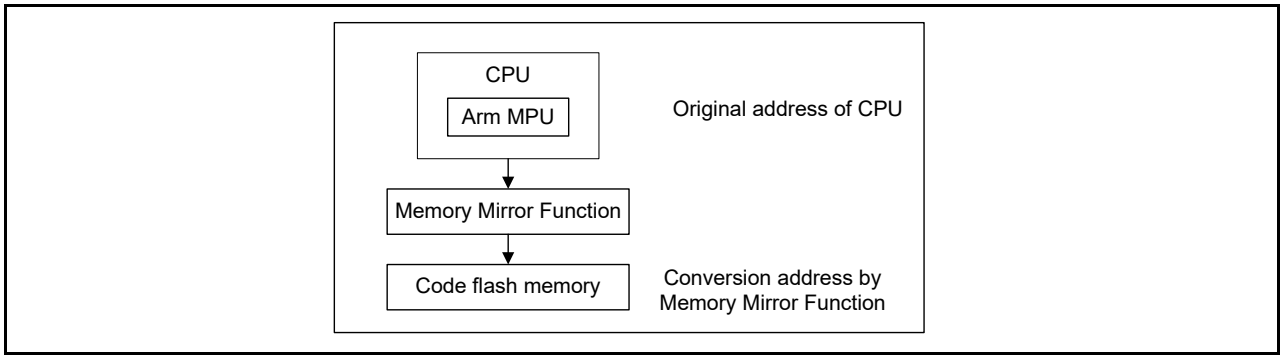


Figure 5.3 MMF address handling

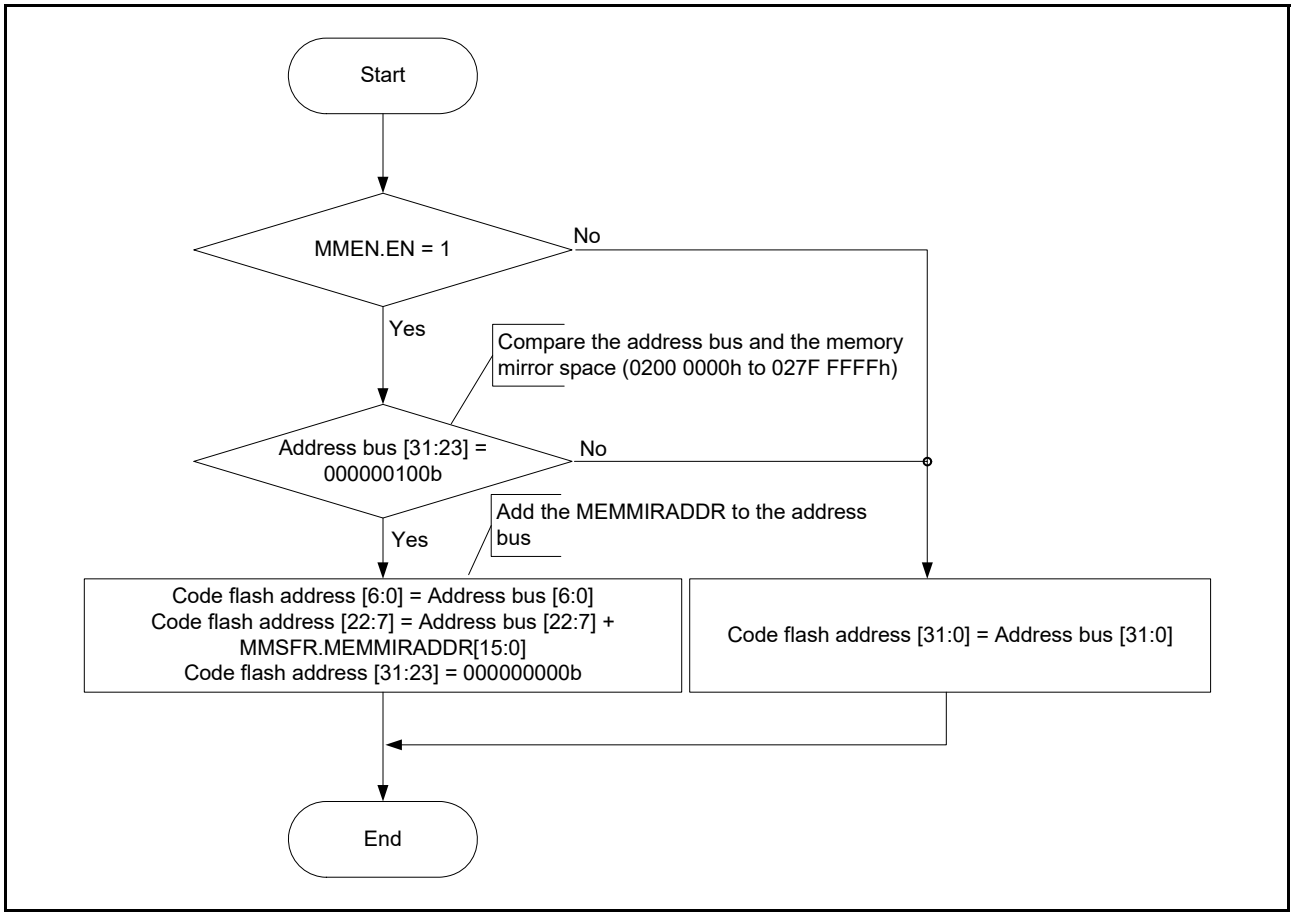


Figure 5.4 MMF operation flow

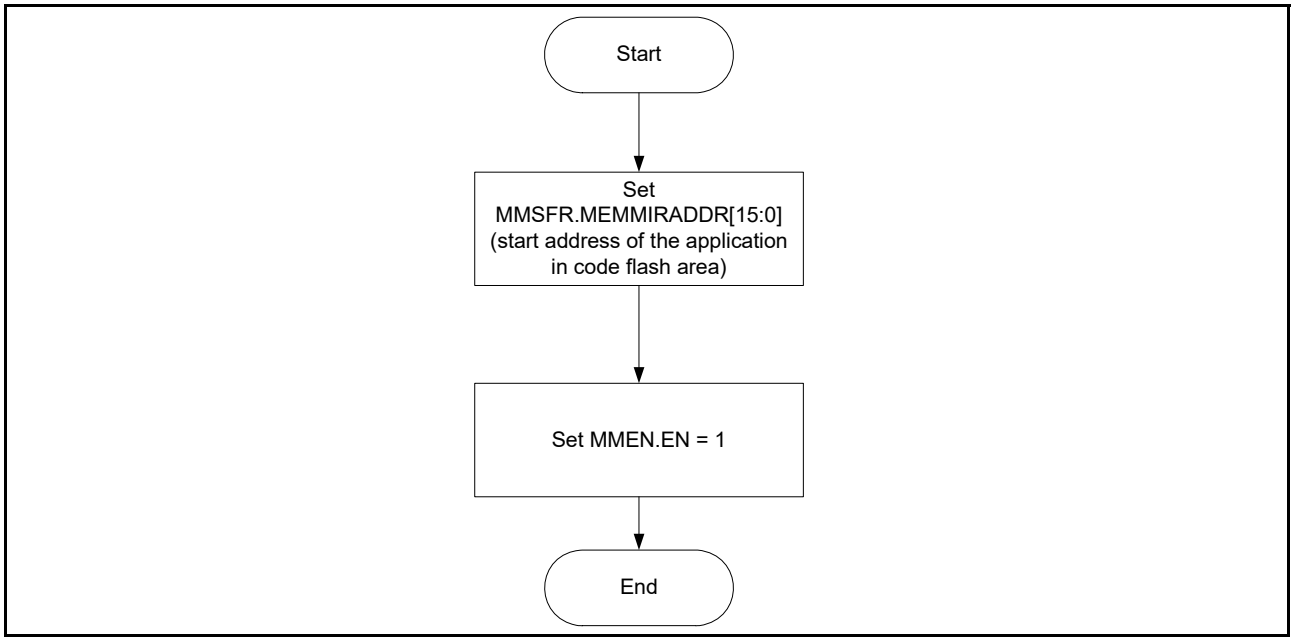


Figure 5.5 MMF setup flow

5.3.2 Setting Example

The target application code on the code flash can be accessed from the address 0200 0000h on the memory mirror space by setting up the code flash start address in MMSFR.MEMMIRADDR[15:0] and setting MMEN.EN = 1.

Figure 5.6 shows an example of how to use the MMF.

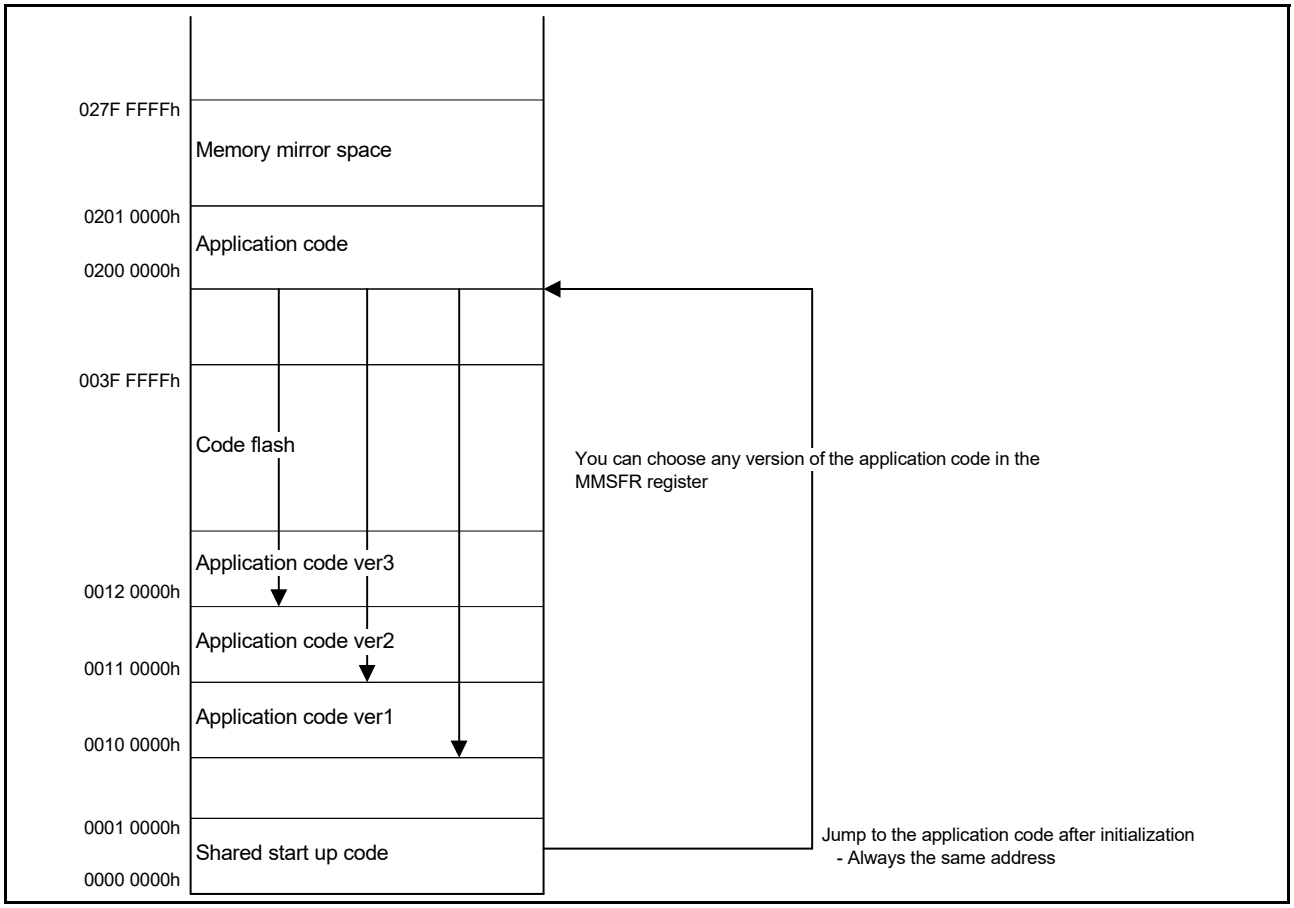


Figure 5.6 MMF setting example

Setting the MMSFR register to DB10 0000h to use the application code ver1.

Setting the MMSFR register to DB11 0000h to use the application code ver2.

Setting the MMSFR register to DB12 0000h to use the application code ver3.

6. Resets

6.1 Overview

The MCU provides 13 resets:

- RES pin reset
- Power-on reset
- Independent watchdog timer reset
- Watchdog timer reset
- Voltage monitor 0 reset
- Voltage monitor 1 reset
- Voltage monitor 2 reset
- SRAM parity error reset
- Bus master MPU error reset
- Bus slave MPU error reset
- Stack pointer error reset
- Deep Software Standby reset
- Software reset.

Table 6.1 lists the reset names and sources.

Table 6.1 Reset names and sources

Reset name	Source
RES pin reset	Voltage input to the RES pin is driven low
Power-on reset	VCC rise (voltage detection V_{POR})*1
Independent watchdog timer reset	IWDT underflow or refresh error
Watchdog timer reset	WDT underflow or refresh error
Voltage monitor 0 reset	VCC fall (voltage detection V_{det0})*1
Voltage monitor 1 reset	VCC fall (voltage detection V_{det1})*1
Voltage monitor 2 reset	VCC fall (voltage detection V_{det2})*1
SRAM parity error reset	SRAM parity error detection
Bus master MPU error reset	Bus master MPU error detection
Bus slave MPU error reset	Bus slave MPU error detection
Stack pointer error reset	Stack pointer error detection
Deep software standby reset	Canceling of Deep Software Standby mode by an interrupt
Software reset	Register setting (use the Arm® software reset bit AIRCR.SYSRESETREQ)

Note 1. For details on the voltages to be monitored (V_{POR}, V_{det0}, V_{det1}, and V_{det2}), see section 8, Low Voltage Detection (LVD) and section 43, Electrical Characteristics.

The internal state and pins are initialized by a reset. Table 6.2 and Table 6.3 list the targets initialized by resets.

Table 6.2 Reset detect flags initialized by each reset source (1 of 2)

	Reset source							
Flags to be initialized	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Power-On Reset Detect Flag (RSTSR0.PORF)	✓	×	×	×	×	×	×	×

Table 6.2 Reset detect flags initialized by each reset source (2 of 2)

Flags to be initialized	Reset source							
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	✓	✓	×	×	×	×	×	×
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	✓	✓	✓	×	×	×	×	×
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	✓	✓	✓	×	×	×	×	×
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	✓	✓	✓	×	×	×	×	×
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	✓	✓	✓	×	×	×	×	×
Software Reset Detect Flag (RSTSR1.SWRF)	✓	✓	✓	×	×	×	×	×
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	✓	✓	✓	×	×	×	×	×
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	✓	✓	✓	×	×	×	×	×
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	✓	✓	✓	×	×	×	×	×
Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	✓	✓	✓	×	×	×	×	×
Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	✓	✓	✓	×	×	×	×	×
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	×	✓	×	×	×	×	×	×

Flags to be initialized	Reset source					
	SRAM parity error reset	Bus master MPU error reset	Bus slave MPU error reset	Stack pointer error reset	Deep Software Standby reset	
					DEEPCUT[0] = 0	DEEPCUT[0] = 1
Power-On Reset Detect Flag (RSTSR0.PORF)	×	×	×	×	×	×
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	×	×	×	×	×	×
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	×	×	×	×	✓	✓
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	×	×	×	×	✓	✓
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	×	×	×	×	×	×
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	×	×	×	×	×	×
Software Reset Detect Flag (RSTSR1.SWRF)	×	×	×	×	✓	✓
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	×	×	×	×	✓	✓
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	×	×	×	×	✓	✓
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	×	×	×	×	✓	✓
Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	×	×	×	×	✓	✓
Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	×	×	×	×	×	×
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	×	×	×	×	×	×

✓: initialized to 0

×: Not initialized

Table 6.3 Module-related registers initialized by each reset source (1 of 2)

Registers to be initialized		Reset source							
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Watchdog timer registers	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓	✓
Voltage monitor function 1 registers	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	✓	✓	✓	✓	✓	×	×	×
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	×	×	×

Table 6.3 Module-related registers initialized by each reset source (2 of 2)

Registers to be initialized		Reset source							
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Voltage monitor function 2 registers	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	✓	✓	✓	✓	✓	×	×	×
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓	×	×	×
SOSC registers	SOSCCR	×	✓*1	×	×	×	×	×	×
	SOMCR	×	×	×	×	×	×	×	×
LOCO registers	LOCOCR	✓	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	×	✓	✓	×	×	✓	✓	×
MOSC register	MOMCR	✓	✓	✓	✓	✓	✓	✓	✓
AGT register		×	✓	✓	×	×	✓	✓	×
MPU register		✓	✓	✓	✓	✓	✓	✓	✓
Pin state (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	✓	✓	✓
Pin state (XCIN/XCOUT pin)		×	×	×	×	×	×	×	×
Low-power function registers	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	✓	✓	✓
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓	✓

Registers to be initialized		Reset source					
		SRAM parity error reset	Bus master MPU error reset	Bus slave MPU error reset	Stack pointer error reset	Deep Software Standby reset	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
Watchdog timer registers	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓
Voltage monitor function 1 registers	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	×	×	×	×	×	×
	LVD1CR1/LVD1SR	×	×	×	×	✓	✓
Voltage monitor function 2 registers	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	×	×	×	×	×	×
	LVD2CR1/LVD2SR	×	×	×	×	✓	✓
SOSC registers	SOSCCR	×	×	×	×	×	×
	SOMCR	×	×	×	×	×	×
LOCO registers	LOCOCR	✓	✓	✓	✓	✓	✓
	LOCOUTCR	×	×	×	×	×	✓
MOSC register	MOMCR	✓	✓	✓	✓	×	×
AGT register		×	×	×	×	×	✓
MPU register		✓	×	×	×	✓	✓
Pin states (except XCIN/XCOUT pin)		✓	✓	✓	✓	*2	*2
Pin states (XCIN/XCOUT pin)		×	×	×	×	×	×
Low-power function registers	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	×	×
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓	✓

✓: Initialized
×: Not initialized

Note 1. For the initial value of each register, see section 9, Clock Generation Circuit.
Note 2. Depends on the setting of DPSBYCR.IOKEEP.

Table 6.4 and Table 6.5 show the states of SOSC and LOCO when a reset occurs.

Table 6.4 States of SOSC when a reset occurs

		Reset source	
		POR	**Other**
SOSC	Enable or disable	Initialized to enable	Continue with the state that was selected before the reset occurred
	Drive capability	Continue with the state that was selected before the reset occurred	

Table 6.5 States of LOCO when a reset occurs

		Reset source	
		POR, LVD0, LVD1, LVD2/ Deep Software Standby (DEEPCUT[0] = 1)	**Other**
LOCO	Enable or disable	Initialized to enable	
	Oscillation accuracy*1	Initialized to accuracy before trimming by LOCOUTCR (accuracy: ± 15%)	Continue with the accuracy that was trimmed by LOCOUTCR

Note 1. The LOCO User Trimming Control Register (LOCOUTCR) is reset by POR, LVD0, LVD1, LVD2, and Deep Software Standby (DEEPCUT[0] = 1) resets, returning the LOCO to the default oscillation accuracy. To restore the pre-reset LOCO oscillation accuracy, reload the required trimming value into LOCOUTCR after any of these resets.

Table 6.6 lists the pin related to the reset function.

Table 6.6 Reset I/O pin

Pin name	I/O	Function
RES	Input	Reset pin

6.2 Register Descriptions

6.2.1 Reset Status Register 0 (RSTSR0)

Address(es): SYSTEM.RSTSR0 4001 E410h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSRSTF	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
Value after reset:	x*1	0	0	0	x*1	x*1	x*1	x*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	PORF	Power-On Reset Detect Flag	0: Power-on reset not detected 1: Power-on reset detected.	R(/W)*2
b1	LVD0RF	Voltage Monitor 0 Reset Detect Flag	0: Voltage monitor 0 reset not detected 1: Voltage monitor 0 reset detected.	R(/W)*2
b2	LVD1RF	Voltage Monitor 1 Reset Detect Flag	0: Voltage monitor 1 reset not detected 1: Voltage monitor 1 reset detected.	R(/W)*2
b3	LVD2RF	Voltage Monitor 2 Reset Detect Flag	0: Voltage monitor 2 reset not detected 1: Voltage monitor 2 reset detected.	R(/W)*2
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DPSRSTF	Deep Software Standby Reset Flag	0: Deep Software Standby mode cancellation not requested by an interrupt 1: Deep Software Standby mode cancellation requested by an interrupt.	R(/W)*2

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

PORF flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset occurred.

[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to PORF.

LVD0RF flag (Voltage Monitor 0 Reset Detect Flag)

The LVD0RF flag indicates that the VCC voltage fell below V_{det0}.

[Setting condition]

- When a voltage monitor 0 reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to LVD0RF.

LVD1RF flag (Voltage Monitor 1 Reset Detect Flag)

The LVD1RF flag indicates that the VCC voltage fell below V_{det1}.

[Setting condition]

- When a voltage monitor 1 reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to LVD1RF.

LVD2RF flag (Voltage Monitor 2 Reset Detect Flag)

The LVD2RF flag indicates that the VCC voltage fell below V_{det2}.

[Setting condition]

- When a voltage monitor 2 reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to LVD2RF.

DPSRSTF flag (Deep Software Standby Reset Flag)

The DPSRSTF flag indicates that Deep Software Standby mode is canceled by an external or internal interrupt, and that an internal reset (Deep Software Standby reset) occurs when an exception from Deep Software Standby mode occurs.

[Setting condition]

- When Deep Software Standby mode is canceled by an external or internal interrupt. For details, see section 11, Low Power Modes.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to DPSRSTF.

6.2.2 Reset Status Register 1 (RSTSR1)

Address(es): SYSTEM.RSTSR1 4001 E0C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPERF	BUSMRF	BUSSRF	—	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
Value after reset:	0	0	0	x*1	x*1	x*1	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	IWDTRF	Independent Watchdog Timer Reset Detect Flag	0: Independent watchdog timer reset not detected 1: Independent watchdog timer reset detected.	R(/W) *2
b1	WDTRF	Watchdog Timer Reset Detect Flag	0: Watchdog timer reset not detected 1: Watchdog timer reset detected.	R(/W) *2
b2	SWRF	Software Reset Detect Flag	0: Software reset not detected 1: Software reset detected.	R(/W) *2
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	RPERF	SRAM Parity Error Reset Detect Flag	0: SRAM parity error reset not detected 1: SRAM parity error reset detected.	R(/W) *2
b9	—	Reserved	The write value should be 0.	R/W
b10	BUSSRF	Bus Slave MPU Error Reset Detect Flag	0: Bus slave MPU error reset not detected 1: Bus slave MPU error reset detected.	R(/W) *2
b11	BUSMRF	Bus Master MPU Error Reset Detect Flag	0: Bus master MPU error reset not detected 1: Bus master MPU error reset detected.	R(/W) *2
b12	SPERF	SP Error Reset Detect Flag	0: SP error reset not detected 1: SP error reset detected.	R(/W) *2

Bit	Symbol	Bit name	Description	R/W
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

IWDTRF flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset occurs.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to IWDTRF.

WDTRF flag (Watchdog Timer Reset Detect Flag)

The WDTRF flag indicates that a watchdog timer reset occurs.

[Setting condition]

- When a watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to WDTRF.

SWRF flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset occurs.

[Setting condition]

- When a software reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to SWRF.

RPERF flag (SRAM Parity Error Reset Detect Flag)

The RPERF flag indicates that a SRAM parity error reset occurs.

[Setting condition]

- When a SRAM parity error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to RPERF.

BUSSRF flag (Bus Slave MPU Error Reset Detect Flag)

The BUSSRF flag indicates that a bus slave MPU error reset occurs.

[Setting condition]

- When a bus slave MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs

- When 1 is read from and then 0 is written to BUSSRF.

BUSMRF flag (Bus Master MPU Error Reset Detect Flag)

The BUSMRF flag indicates that a bus master MPU error reset occurs.

[Setting condition]

- When a bus master MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to BUSMRF.

SPERF flag (SP Error Reset Detect Flag)

The SPERF flag indicates that a stack pointer error reset occurs.

[Setting condition]

- When a stack pointer error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to SPERF.

6.2.3 Reset Status Register 2 (RSTSR2)

Address(es): SYSTEM.RSTSR2 4001 E411h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CWSF
Value after reset:	0	0	0	0	0	0	0	x*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	CWSF	Cold/Warm Start Determination Flag	0: Cold start 1: Warm start.	R(/W) *2
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 1 can be written to set the flag.

RSTSR2 determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

CWSF flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing, either cold start or warm start. The CWSF flag is initialized by a power-on reset. It is not initialized by a reset signal generated by the RES pin.

[Setting condition]

- When 1 is written by software. Writing 0 to CWSF does not set it to 0.

[Clearing condition]

- When a reset listed in Table 6.2 occurs.

6.2.4 Reset Control Register 1 (RCR1)

Address(es): RTC.RCR1 4004 4022h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	0	x	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	The write value should be 0.	R/W
b1	—	Reserved	The write value should be 0.	R/W
b2	—	Reserved	The write value should be 0.	R/W
b3	—	Reserved	The write value should be 0.	R/W
b7 to b4	—	Reserved	The write value should be 0.	R/W

6.2.5 Reset Control Register 2 (RCR2)

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	RESET	—
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	The write value should be 0.	R/W
b1	RESET	Software Reset	• In writing 0: Invalid (writing 0 has no effect) 1: The target registers for software reset are initialized. • In reading 0: Software reset has completed 1: Software reset in progress.	R/W
b3 to b2	—	Reserved	The write value should be 0.	R/W
b7 to b4	—	Reserved	The write value should be 0.	R/W

6.2.6 Reset Control Register 4 (RCR4)

Address(es): RTC.RCR4 4004 4028h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RCKSEL
Value after reset:	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RCKSEL	Count Source Select	0: Sub-clock oscillator is not used 1: Sub-clock oscillator is used.	R/W
b7 to b1	—	Reserved	The write value should be 0.	R/W

6.3 Operation

6.3.1 RES Pin Reset

The RES pin generates this reset. When the RES pin is driven low, all the processing in progress is aborted and the MCU enters a reset state. To successfully reset the MCU, the RES pin must be held low for the power supply stabilization time specified at power-on.

When the RES pin is driven high from low, the internal reset is canceled after the post-RES cancellation wait time (t_{RESWT}) elapses. The CPU then starts the reset exception handling.

For details, see section 43, Electrical Characteristics.

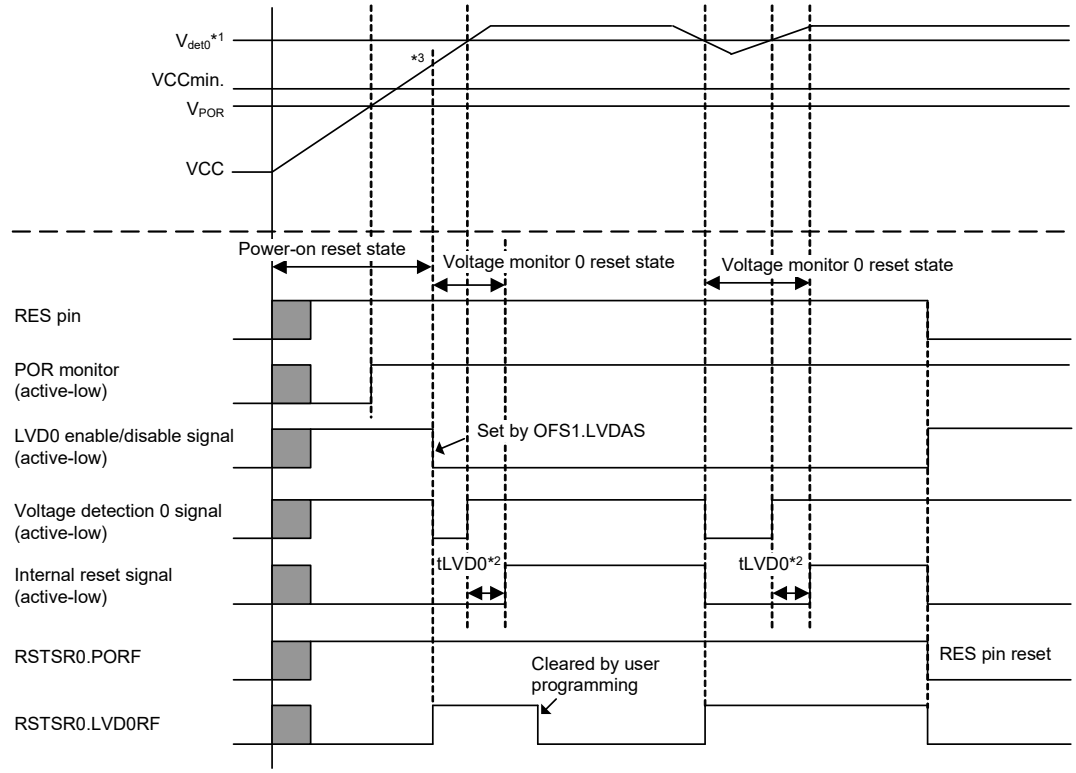
6.3.2 Power-On Reset

The power-on reset (POR) is an internal reset generated by the power-on reset circuit. If the RES pin is in a high-level state when power is supplied, a power-on reset is generated. After VCC exceeds V_{POR} and the specified power-on reset time elapses, the internal reset is canceled and the CPU starts the reset exception handling. The power-on reset time is the stabilization period for the external power supply and the MCU circuit. After a power-on reset is generated, the PORF flag in the RSTSR0 is set to 1. The PORF flag is initialized by the RES pin reset.

The voltage monitor 0 reset is an internal reset generated by the voltage monitor circuit. If the Voltage Detection 0 Circuit Start (LVDAS) bit in the Option Function Select Register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below V_{det0}, the RSTSR0.LVD0RF flag is set to 1 and the voltage detection circuit generates voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used.

After VCC exceeds V_{det0} and the voltage monitor 0 reset time (tLVD0) elapses, the internal reset is canceled and the CPU starts the reset exception handling. The V_{det0} voltage detection level can be changed by the setting in the VDSEL[1:0] bits in Option Function Select Register 1 (OFS1).

Figure 6.1 shows example of operations during a power-on reset and voltage monitor 0 reset.



Note: For details on the electrical characteristics, see section 43, Electrical Characteristics.
Note 1. V_{det0} shows a voltage monitor 0 reset detection level, V_{POR} shows a power-on reset detection level, and VCCmin shows minimum guaranteed voltage of MCU.
Note 2. tLVD0 shows a time for voltage monitor 0 reset.
Note 3. At power-on, VCC should have risen to the minimum guaranteed voltage before the POR reset is released.

Figure 6.1 Example of operations during power-on and voltage monitor 0 resets

6.3.3 Voltage Monitor Reset

The voltage monitor 0 reset is an internal reset generated by the voltage monitor circuit. If the Voltage Detection 0 Circuit Start (LVDAS) bit in the Option Function Select Register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below V_{det0}, the RSTSR0.LVD0RF flag becomes 1 and the voltage detection circuit generates a voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used. After VCC exceeds V_{det0} and the voltage monitor 0 reset time (tLVD0) elapses, the internal reset is canceled and the CPU starts the reset exception handling.

When the Voltage Monitor 1 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 1 Circuit Mode Select bit (LVD1CR0.RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in the Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 1 reset if VCC falls to or below V_{det1}.

Likewise, when the Voltage Monitor 2 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 2 Circuit Mode Select bit (LVD2CR0.RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0), the RSTSR0.LVD2RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 2 reset if VCC falls to or below V_{det2}.

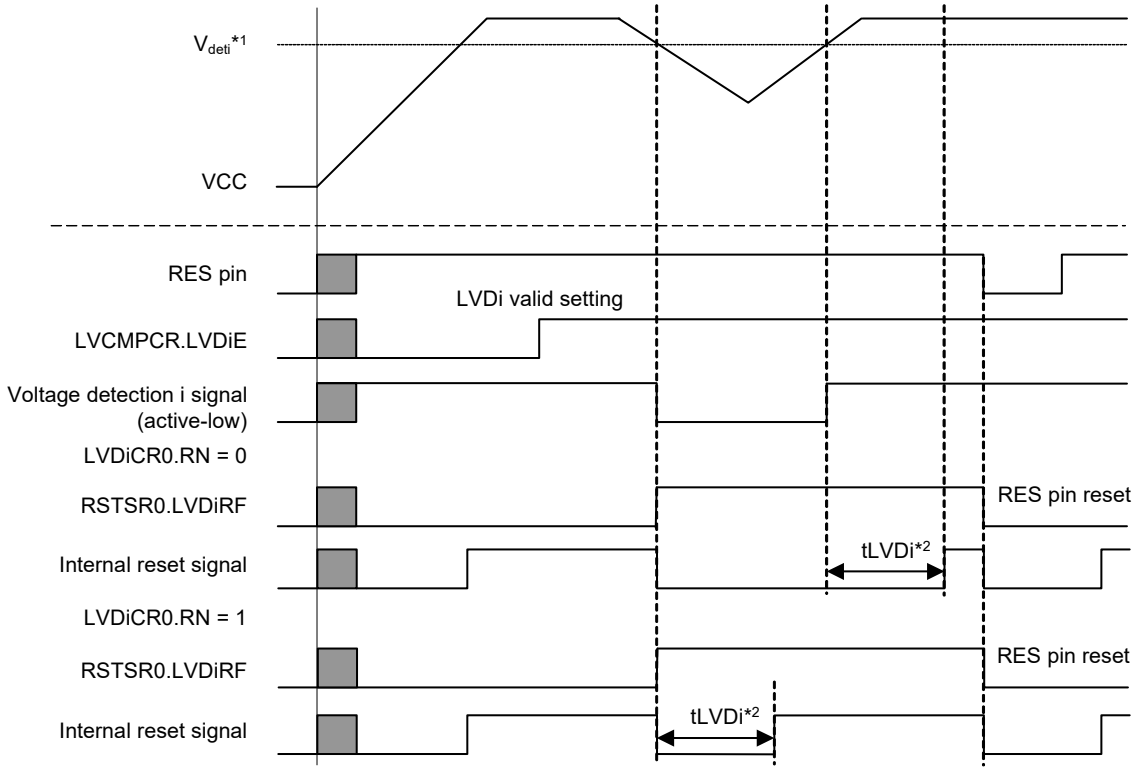
Similarly, timing for release from the voltage monitor 1 reset state is selectable in the Voltage Monitor 1 Reset Negate Select bit (RN) in the LVD1CR0 register. When the LVD1CR0.RN bit is 0 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (tLVD1) elapses after VCC rises above V_{det1}. When the LVD1CR0.RN bit is 1 and VCC falls to or below V_{det1}, the CPU is released from the

internal reset state and starts reset exception handling when the LVD1 reset time (tLVD1) elapses.

Likewise, timing for release from the voltage monitor 2 reset state is selectable in the Voltage Monitor 2 Reset Negate Select bit (RN) in the LDV2CR0 register.

Detection levels V_{det1} and V_{det2} can be changed in the Voltage Detection Level Select Register (LDVLVLR).

Figure 6.2 shows an example of operations during voltage monitor 1 and 2 resets. For details on the voltage monitor 1 reset and voltage monitor 2 reset, see section 8, Low Voltage Detection (LVD).



Note: For details on the electrical characteristics, see section 43, Electrical Characteristics.
Note 1. V_{deti} indicates the detection level of a voltage monitor 1 reset and voltage monitor 2 reset (i = 1, 2).
Note 2. tLVDi indicates the time for a voltage monitor 1 reset and voltage monitor 2 reset (i = 1, 2).

Figure 6.2 Example of operations during voltage monitor 1 and voltage monitor 2 resets

6.3.4 Deep Software Standby Reset

The deep software standby reset is an internal reset generated when Deep Software Standby mode is canceled by an associated interrupt. The deep software standby reset is canceled after tDSBY (return time after Deep Software Standby mode cancellation) elapses.

When tDSBYWT (wait time after Deep Software Standby mode cancellation) elapses after Deep Software Standby mode is canceled, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the deep software standby reset, see section 11, Low Power Modes.

6.3.5 Independent Watchdog Timer Reset

The independent watchdog timer reset is an internal reset generated from the Independent Watchdog Timer (IWDT). Output of the reset from the IWDT can be selected in the Option Function Select Register 0 (OFS0).

When output of the independent watchdog timer reset is selected, the reset is generated if the IWDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (tRESW2) elapses after the independent watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the independent watchdog timer reset, see section 26, Independent Watchdog Timer (IWDT).

6.3.6 Watchdog Timer Reset

The watchdog timer reset is an internal reset generated from the Watchdog Timer (WDT). Output of the reset from the WDT can be selected in the WDT Reset Control Register (WDTRCR) or Option Function Select Register 0 (OFS0).

When output of the watchdog timer reset is selected, the reset is generated if the WDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (tRESW2) elapses after the watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the watchdog timer reset, see section 25, Watchdog Timer (WDT).

6.3.7 Software Reset

Software reset is an internal reset generated by a software setting of the SYSRESETREQ bit in the AIRCR register in the Arm core. When the SYSRESETREQ bit is set to 1, a software reset is generated. When the internal reset time (tRESW2) elapses after a software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the SYSRESETREQ bit, see the *ARM® Cortex®-M4 Technical Reference Manual*.

6.3.8 Determination of Cold/Warm Start

Read the CWSF flag in RSTSR2 to determine the cause of reset processing. This flag indicates whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

The CWSF flag is set to 0 when a power-on reset occurs (cold start). Otherwise, the flag is not set to 0. The flag is set to 1 when 1 is written to it through software. It is not set to 0 even on writing 0 to it.

Figure 6.3 shows an example of a cold/warm start determination operation.

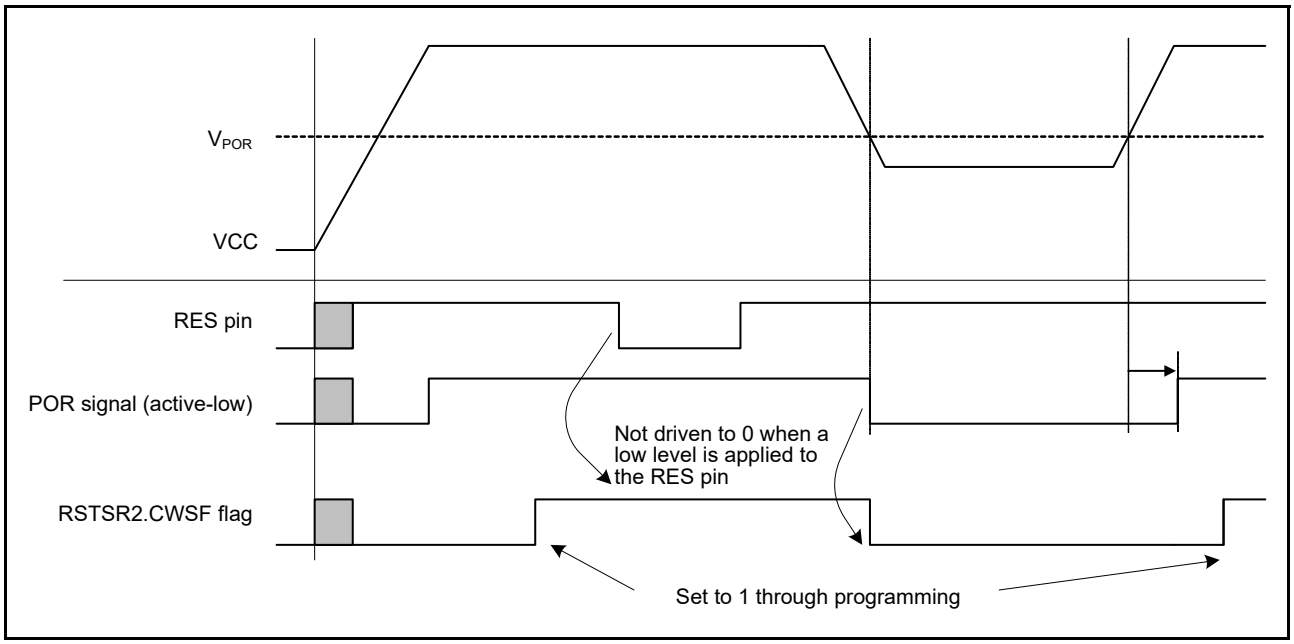
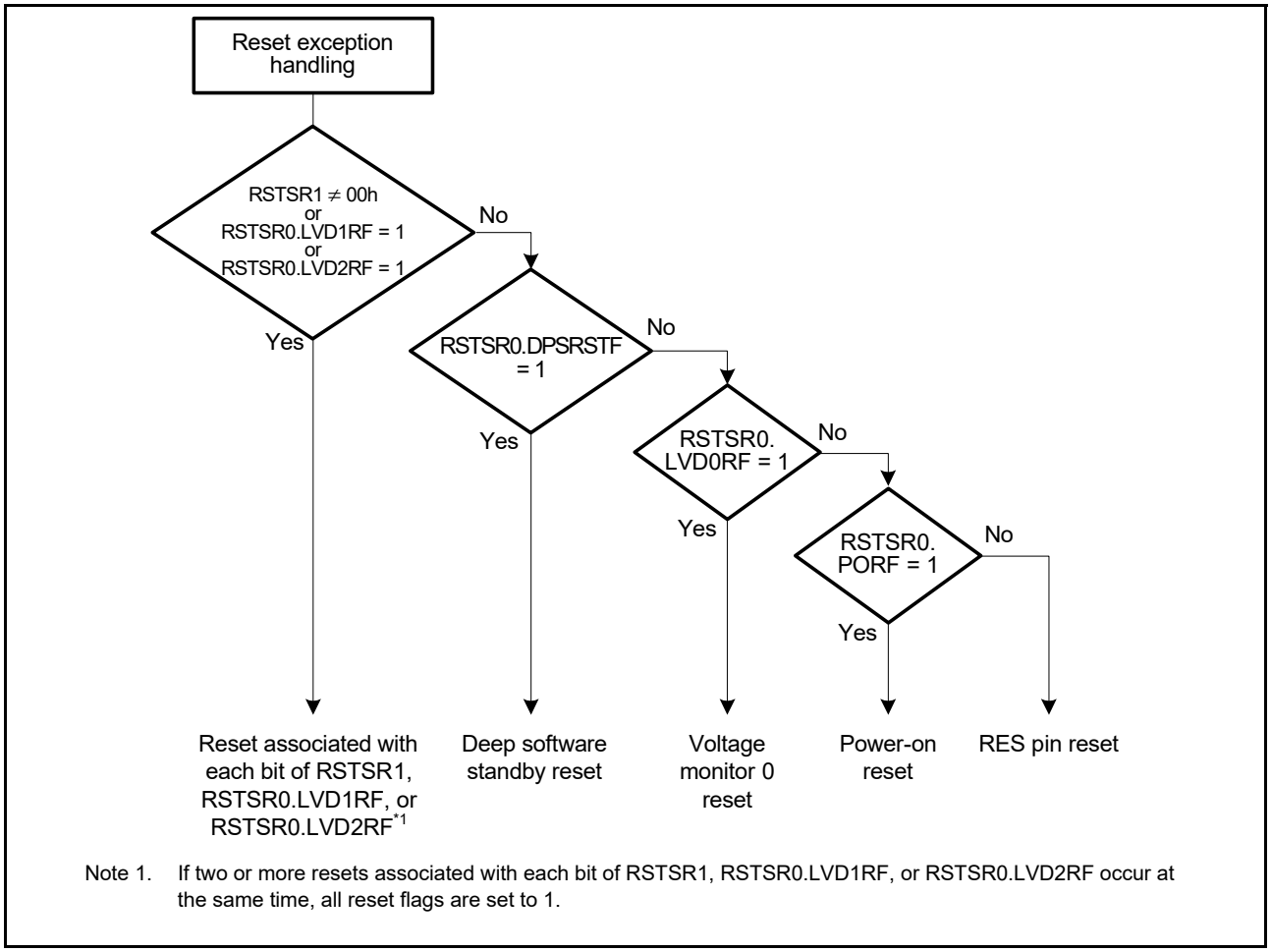


Figure 6.3 Example of a cold/warm start determination operation

6.3.9 Determination of Reset Generation Source

Read RSTSR0 and RSTSR1 to determine which reset executes the reset exception handling. Figure 6.4 shows an example of the flow to identify a reset generation source. The reset flag must be written with 0 after it is read as 1.



Note 1. If two or more resets associated with each bit of RSTSR1, RSTSR0.LVD1RF, or RSTSR0.LVD2RF occur at the same time, all reset flags are set to 1.

Figure 6.4 Example of reset generation source determination flow

6.4 Initialization Procedure Required after Reset

The MCU has registers that are not initialized after reset. In some cases, an unintended interrupt request may cause an increase in power consumption or malfunction. Therefore, initialize these registers after reset according to one of the procedures described in Figure 6.5 and Figure 6.6.

Figure 6.5 shows the initialization procedure in all cases and Figure 6.6 shows the initialization procedure that can be applied when the sub-clock oscillator is not used.

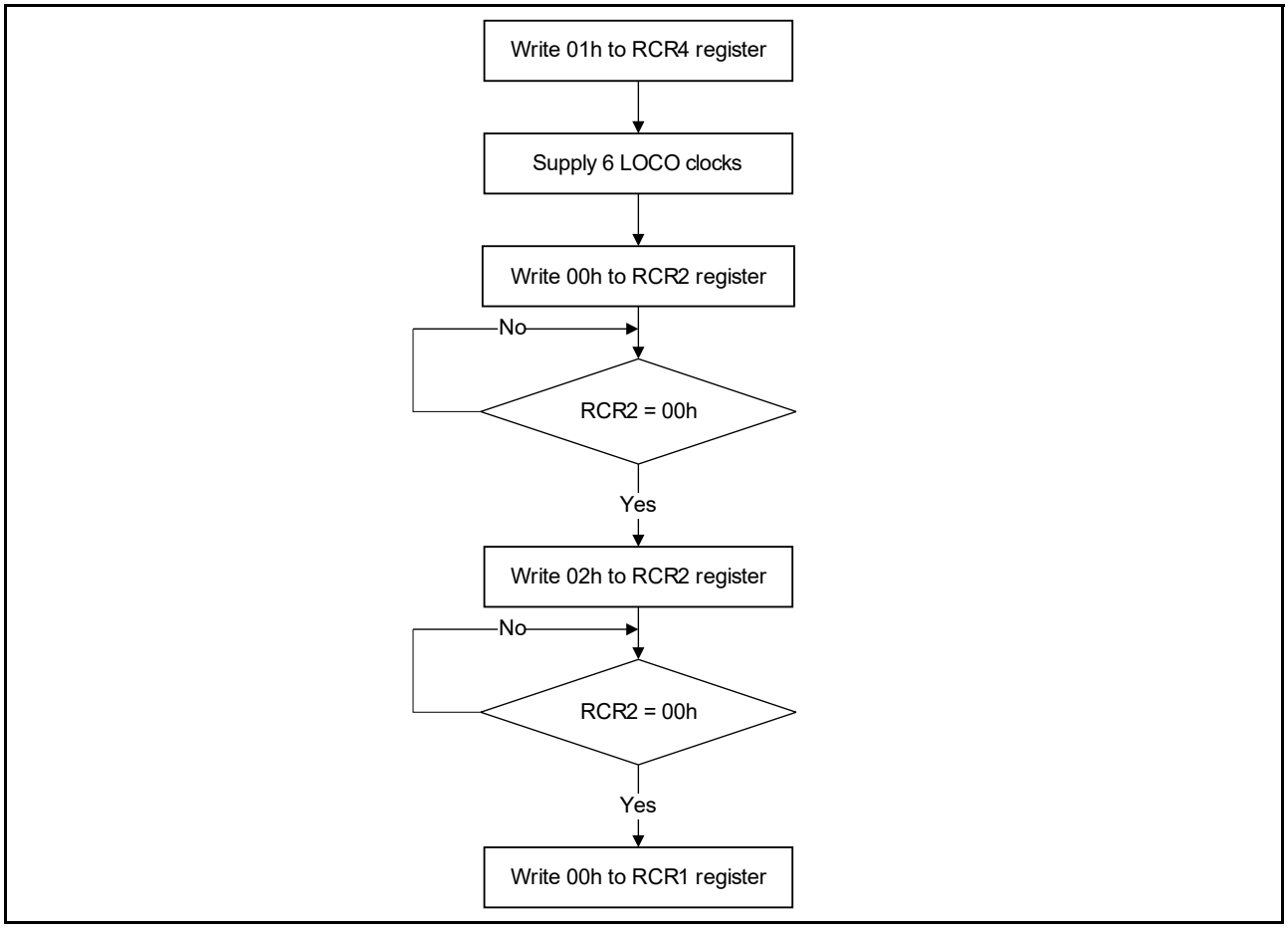


Figure 6.5 Initialization procedure for all cases

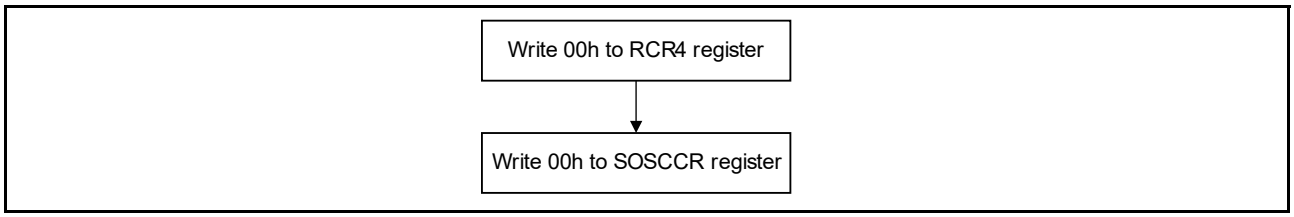


Figure 6.6 Initialization procedure when the sub-clock oscillator is not used

For more information on the SOSCCR register, see section 9, Clock Generation Circuit.

7. Option-Setting Memory

7.1 Overview

The option-setting memory determines the state of the MCU after a reset. The option-setting memory is allocated to the configuration setting area and the program flash area of the flash memory. The available methods of setting are different for the two areas.

Figure 7.1 shows the option-setting memory area.

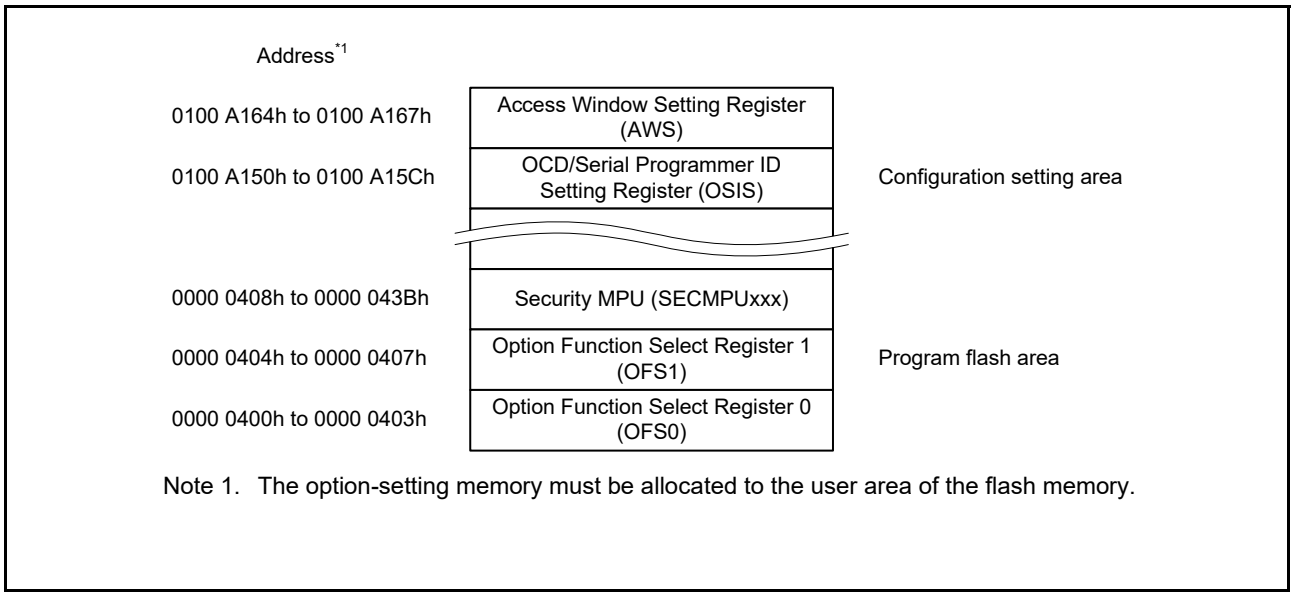


Figure 7.1 Option-setting memory area

7.2 Register Descriptions

7.2.1 Option Function Select Register 0 (OFS0)

Address(es): OFS0 0000 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	WDTSTPCTL	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
Value after reset:							User setting*1									

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IWDTSTPCTL	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
Value after reset:							User setting*1									

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b1	IWDTSTRT	IWDT Start Mode Select	0: Automatically activate IWDT after a reset (auto start mode) 1: Disable IWDT.	R
b3, b2	IWDTTOPS[1:0]	IWDT Timeout Period Select	b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh).	R

Bit	Symbol	Bit name	Description	R/W
b7 to b4	IWDTCKS[3:0]	IWDT-Dedicated Clock Frequency Division Ratio Select	b7 b4 0 0 0 0: × 1 0 0 1 0: × 1/16 0 0 1 1: × 1/32 0 1 0 0: × 1/64 1 1 1 1: × 1/128 0 1 0 1: × 1/256. Other settings are prohibited.	R
b9, b8	IWDTRPES[1:0]	IWDT Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting).	R
b11, b10	IWDTRPSS[1:0]	IWDT Window Start Position Select	b11 b10 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting).	R
b12	IWDTRSTIRQS	IWDT Reset Interrupt Request Select	0: Enable non-maskable interrupt request or interrupt request 1: Enable reset.	R
b13	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b14	IWDTSTPCTL	IWDT Stop Control	0: Continue counting 1: Stop counting when in Sleep, Snooze, or Software Standby mode.	R
b16, b15	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b17	WDTSTRT	WDT Start Mode Select	0: Automatically activate WDT after a reset (auto start mode) 1: Stop WDT after a reset (register start mode).	R
b19, b18	WDTTOPS[1:0]	WDT Timeout Period Select	b19 b18 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh).	R
b23 to b20	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select	b23 b20 0 0 0 1: PCLKB divided by 4 0 1 0 0: PCLKB divided by 64 1 1 1 1: PCLKB divided by 128 0 1 1 0: PCLKB divided by 512 0 1 1 1: PCLKB divided by 2048 1 0 0 0: PCLKB divided by 8192. Other settings are prohibited.	R
b25, b24	WDTRPES[1:0]	WDT Window End Position Select	b25 b24 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (No window end position setting).	R
b27, b26	WDTRPSS[1:0]	WDT Window Start Position Select	b27 b26 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (No window start position setting).	R
b28	WDTRSTIRQS	WDT Reset Interrupt Request Select	WDT Behavior Select 0: Interrupt 1: Reset.	R
b29	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b30	WDTSTPCTL	WDT Stop Control	0: Continue counting 1: Stop counting when entering Sleep mode.	R
b31	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R

Note 1. The value in a blank product is FFFF FFFFh. It is set to the value written by your application.

IWDTSTRT bit (IWDT Start Mode Select)

The IWDTSTRT bit selects the mode in which the IWDT is activated after a reset (stopped state or activated state).

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits select the timeout period, that is, the time it takes for the down counter to underflow, as 128, 512, 1024, or 2048 cycles of the frequency-divided clock set in the IWDTCKS[3:0] bits. The number of clock cycles that the counter takes to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits.

For details, see section 26, Independent Watchdog Timer (IWDT).

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits select the division ratio of the prescaler for dividing the frequency of the clock for the IWDT as 1/1, 1/16, 1/32, 1/64, 1/128, or 1/256. Using this setting combined with the IWDTTOPS[1:0] bit setting, the IWDT counting period can be set from 128 to 524288 IWDT clock cycles.

For details, see section 26, Independent Watchdog Timer (IWDT).

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits select the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the count value. The value of the window end position must be smaller than the value of the window start position. Otherwise, only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window, in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits vary with the setting in the IWDTTOPS[1:0] bits.

For details, see section 26, Independent Watchdog Timer (IWDT).

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits select the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the positions where the window starts and ends becomes the period in which a refresh is possible. However, refresh is not possible outside this period.

For details, see section 26, Independent Watchdog Timer (IWDT).

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The selected operation can be an independent watchdog timer reset, non-maskable interrupt request, or interrupt request.

For details, see section 26, Independent Watchdog Timer (IWDT).

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit specifies whether to stop counting when entering Sleep, Snooze, or Software Standby mode.

For details, see section 26, Independent Watchdog Timer (IWDT).

WDTSTRT bit (WDT Start Mode Select)

The WDTSTRT bit selects the mode in which the WDT is activated after a reset (stopped state or activated state). When the WDT is activated in auto start mode, the OFS0 register setting for the WDT is valid.

WDTTOPS[1:0] bits (WDT Timeout Period Select)

The WDTTOPS[1:0] bits select the timeout period, that is, the time it takes for the down counter to underflow, as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set in the WDTCKS[3:0] bits. The number of PCLKB cycles that the counter takes to underflow after a refresh operation is determined by the combination of the WDTCKS[3:0] and WDTTOPS[1:0] bits.

For details, see section 25, Watchdog Timer (WDT).

WDTCKS[3:0] bits (WDT Clock Frequency Division Ratio Select)

The WDTCKS[3:0] bits select the division ratio of the prescaler to divide the PCLKB frequency as 1/4, 1/64, 1/128, 1/512, 1/2048, or 1/8192. Using this setting combined with the WDTTOPS[1:0] bit setting, the WDT counting period can be set from 4096 to 134217728 PCLKB cycles.

For details, see section 25, Watchdog Timer (WDT).

WDTRPES[1:0] bits (WDT Window End Position Select)

The WDTRPES[1:0] bits select the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the counted value. The value of the window end position must be smaller than the value of the window start position. Otherwise, only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window, in the WDTRPSS[1:0] and WDTRPES[1:0] bits, vary with the setting of the WDTTOPS[1:0] bits.

For details, see section 25, Watchdog Timer (WDT).

WDTRPSS[1:0] bits (WDT Window Start Position Select)

The WDTRPSS[1:0] bits select the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the positions where the window starts and ends becomes the period in which a refresh is possible. However, refresh is not possible outside this period.

For details, see section 25, Watchdog Timer (WDT).

WDTRSTIRQS bit (WDT Reset Interrupt Request Select)

The WDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The selected operation can be a watchdog timer reset, non-maskable interrupt request, or interrupt request.

For details, see section 25, Watchdog Timer (WDT).

WDTSTPCTL bit (WDT Stop Control)

The WDTSTPCTL bit specifies whether to stop counting when entering Sleep mode. For details, see section 25, Watchdog Timer (WDT).

7.2.2 Option Function Select Register 1 (OFS1)

Address(es): OFS1 0000 0404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
								User setting*1								

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	HOCOFRQ0[1:0]		HOCOEN	—	—	—	—	—	LVDAS	VDSEL0[1:0]	
								User setting*1								

Bit	Symbol	Bit name	Description	R/W
b1, b0	VDSEL0[1:0]	Voltage Detection 0 Level Select	b1 b0 0 0: Setting prohibited 0 1: Select 2.94 V 1 0: Select 2.87 V 1 1: Select 2.80 V.	R
b2	LVDAS	Voltage Detection 0 Circuit Start	0: Enable voltage monitor 0 reset after a reset 1: Disable voltage monitor 0 reset after a reset.	R
b7 to b3	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Bit	Symbol	Bit name	Description	R/W
b8	HOCOEN	HOCO Oscillation Enable	0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset.	R
b10, b9	HOCOFRQ0[1:0]	HOCO Frequency Setting 0	b10 b9 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz 1 1: Setting prohibited.	R
b31 to b11	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Note 1. The value in a blank product is FFFF FFFFh. It is set to the value written by your application.

VDSEL0[1:0] bits (Voltage Detection 0 Level Select)

The VDSEL0[1:0] bits select the voltage detection level of the voltage detection 0 circuit.

LVDAS bit (Voltage Detection 0 Circuit Start)

The LVDAS bit selects whether the voltage monitor 0 reset is enabled or disabled after a reset.

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ0 bit to an optimum value.

HOCOFRQ0[1:0] bits (HOCO Frequency Setting 0)

The HOCOFRQ0[1:0] bits specify the HOCO frequency after a reset as 16, 18, or 20 MHz.

7.2.3 Access Window Setting Register (AWS)

Address(es): AWS 0100 A164h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BTFLG	—	—	—	—	FAWE[10:0]										
Value after reset:						User setting										

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FSPR	—	—	—	—	FAWS[10:0]										
Value after reset:						User setting										

Bit	Symbol	Bit name	Description	R/W
b10 to b0	FAWS[10:0]	Access Window Start Block Address	These bits specify the start block address for the access window. They do not represent the block number of the access window. The access window is only valid in the program flash area. The block address specifies the first address of the block and consists of address bits [23:13].	R
b14 to b11	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Bit	Symbol	Bit name	Description	R/W
b15	FSPR	Protection of Access Window and Startup Area Select Function	This bit controls the programming of the write/erase protection for the access window, the Startup Area Select flag (AWS.BTFLG), and the temporary boot swap control. When this bit is set to 0, it cannot be changed to 1. 0: Executing the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the Startup Area Select flag (AWS.BTFLG) is invalid 1: Executing the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the Startup Area Select flag (AWS.BTFLG) is valid.	R
b26 to b16	FAWE[10:0]	Access Window End Block Address	These bits specify the end block address for the access window. They do not represent the block number of the access window. The access window is only valid in the program flash area. The end block address for the access window is the next block to the region acceptable for programming and erasure defined by the access window. The block address specifies the first address of the block and consists of the address bits [23:13].	R
b30 to b27	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b31	BTFLG	Startup Area Select Flag	This bit specifies whether the address of the startup area is exchanged for the boot swap function or not: 0: First 8-KB area (0000 0000h to 0000 1FFFh) and second 8-KB area (0000 2000h to 0000 3FFFh) are exchanged 1: First 8-KB area (0000 0000h to 0000 1FFFh) and second 8-KB area (0000 2000h to 0000 3FFFh) are not exchanged.	R

Issuing the program or erase (P/E) command to an area outside the access window causes a command-locked state. The access window is only valid in the program flash area. The access window provides protection in self-programming mode, serial programming mode, and on-chip debug mode. The access window can be locked by the FSPR bit.

The access window is specified in both the FAWS[10:0] and FAWE[10:0] bits: The settings for the bits are as follows:

- FAWE[10:0] = FAWS[10:0]: The P/E command is allowed to execute in the full program flash area
- FAWE[10:0] > FAWS[10:0]: The P/E command is only allowed to execute in the window from the block pointed to by the FAWS[10:0] bits to the block one lower than the block pointed to by the FAWE[10:0] bits
- FAWE[10:0] < FAWS[10:0]: The P/E command is not allowed to execute in the program flash area.

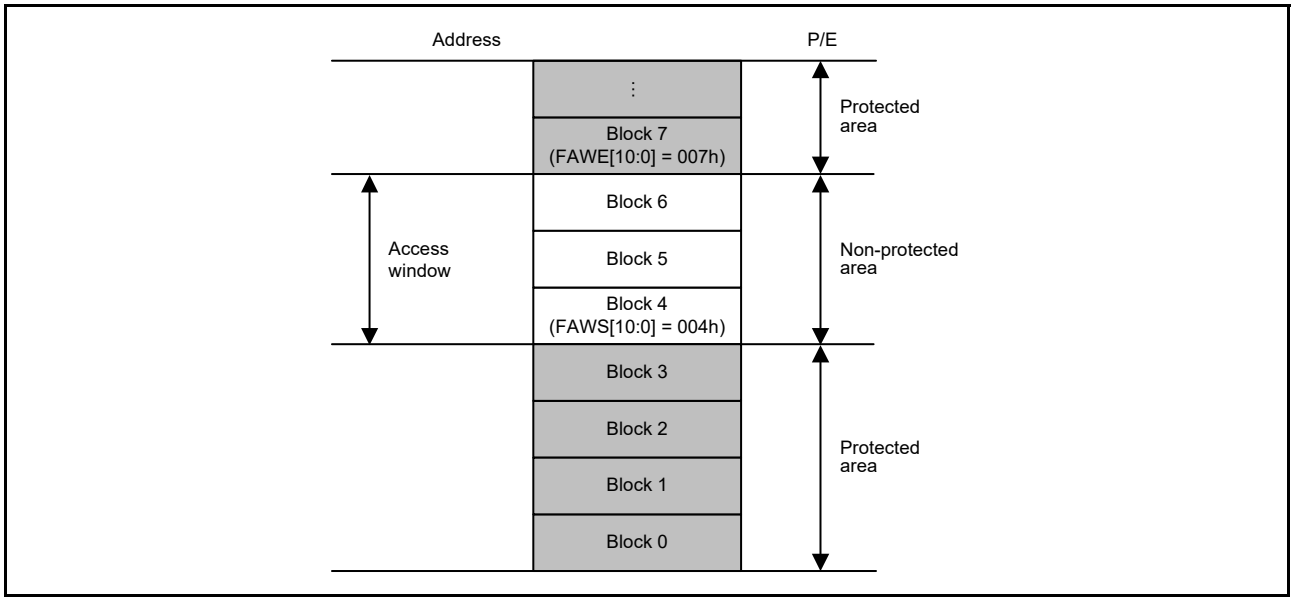


Figure 7.2 Access window overview

7.2.4 OCD/Serial Programmer ID Setting Register (OSIS)

The OSIS register stores the ID for ID code protection of the OCD/serial programmer. When connecting the OCD/serial programmer, write values so that the MCU can determine whether to permit the connection. Use this register to check whether a code transmitted from the OCD/serial programmer matches the ID code in the option-setting memory.

When the ID codes match, connection with the OCD/serial programmer is permitted, if not, connection with the OCD/serial programmer is not possible. The OSIS register must be set in 32-bit words.

Address(es): OSIS 0100 A150h, OSIS 0100 A154h, OSIS 0100 A158h, OSIS 0100 A15Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	User setting															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	User setting															

These fields hold the ID for use in ID authentication for the OCD/serial programmer.

ID code bits [127] and [126] determine whether ID code protection is enabled, and the authentication method to use with the host. Table 7.1 shows how the ID code determines the authentication method.

Setting bit [127] to 0 prevents Renesas from accessing the test mode. Therefore, Renesas cannot perform failure analysis unless provided with bits [126:0]. To process any warranty claim, Renesas must be able to perform failure analysis.

Table 7.1 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection to programmer or on-chip debugger
Serial programming mode (SCI boot mode) On-chip debug mode (JTAG/SWD boot mode)	FFh, …, FFh (all bytes are FFh)	Protection disabled	The ID code is not checked, the ID code always matches, and the connection to programmer or on-chip debugger is permitted
	Bit [127] = 1, bit [126] = 1, and at least one of the 16 bytes is not FFh.	Protection enabled	Matching ID code indicates that authentication is complete and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code indicates that transition to the ID code protection wait state. When the ID code sent from the programmer or the on-chip debugger is ALeRASE in ASCII code (414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the content of the user flash (code and data) area, and configuration area are erased. However, forced erasure is not executed when the FSPR bit is 0.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code indicates that authentication is complete and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state.
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always mismatching, the connection to the programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.

7.3 Setting the Option-Setting Memory

7.3.1 Allocation of Data in the Option-Setting Memory

Programming data is allocated to the addresses in the option-setting memory shown in Figure 7.1. The allocated data is used by tools such as a flash programming software or an on-chip debugger.

Note: Programming formats vary depending on the compiler. See the compiler manual for details.

7.3.2 Setting Data for Programming the Option-Setting Memory

Allocating data according to the procedure described in section 7.3.1, Allocation of Data in the Option-Setting Memory, alone does not actually write the data to the option-setting memory. You must also follow one of the actions described in this section.

(1) Changing the option-setting memory by self-programming

To write data to the program flash area, use the programming command. To write data to the option-setting memory in the configuration setting area, use the configuration setting command. In addition, use the startup area select function to safely update the boot program that includes the option-setting memory.

For details on the programming command, the configuration setting command, and the startup area select function, see section 41, Flash Memory.

Note: While programming the configuration setting area, the following restrictions apply:

- The code must not access addresses that satisfy the ranges described by the expression defined in Expression 1 from all bus masters
- The code must not execute on addresses that satisfy the ranges described by the expression defined in Expression 1.

Expression 1

If (((address & 0x0101F800) = = 0x01010000) || ((address & 0x0101FC00) = = 0x01012000))

For example, the ranges of addresses 0x1FFF0000 to 0x1FFF07FF or 0x1FFF2000 to 0x1FFF23FF are associated with the SRAMHS area that is tagged as restricted. Also, interrupts are allowed, however, the ISR has these specified restrictions. Therefore, it is highly recommended that you disable all interrupts, and bus masters except the CPU while programming the configuration setting area because the interrupts and these modules might access prohibited area in Expression 1.

(2) Debugging through an OCD or programming by a flash writer

This procedure depends on the tool in use, see the tool manual for details.

The MCU provides two setting procedures as follows:

- Read the data allocated as described in section 7.3.1, Allocation of Data in the Option-Setting Memory, from an object file or Motorola S-format file generated by the compiler, and write the data to the MCU
- Use the GUI interface of the tool to program the same data allocated as described in section 7.3.1, Allocation of Data in the Option-Setting Memory.

Note: While programming the OSIS or AWS registers, the following restrictions apply:

- The code must not access addresses that satisfy the ranges described by the expression defined in Expression 1 from all bus masters
- The code must not execute on addresses that satisfy the ranges described by the expression defined in Expression 1.

7.4 Usage Notes

7.4.1 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting Memory

When reserved areas and reserved bits in the option-setting memory are available for programming, write 1 to all bits in reserved areas and all reserved bits. If 0 is written to these bits, normal operation cannot be guaranteed.

8. Low Voltage Detection (LVD)

8.1 Overview

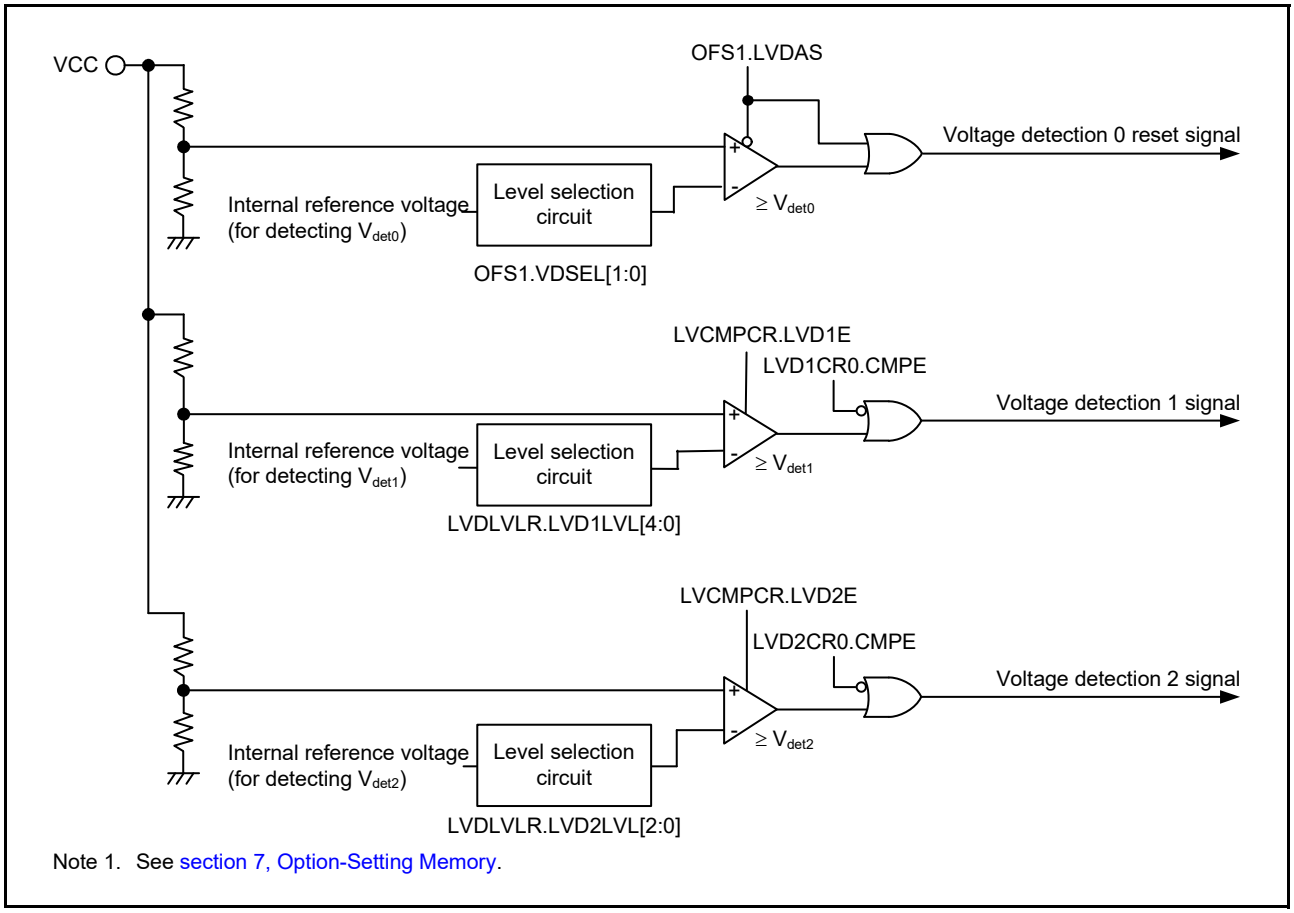
The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. The LVD module consists of three separate voltage level detectors, 0, 1, and 2, which measure the voltage level input to the VCC pin. LVD voltage detection registers allow your application to configure detection of VCC changes at various voltage thresholds.

Each voltage level detector has a voltage monitor associated with it, for example voltage monitors 0, 1, and 2. Voltage monitor registers are used to configure the LVD to trigger an interrupt, event link output, or reset when the thresholds are crossed.

Table 8.1 lists the LVD specifications. Figure 8.1 shows a block diagram of voltage detectors 0, 1, and 2, Figure 8.2 shows a block diagram of the voltage monitor 1 interrupt/reset circuit, and Figure 8.3 shows a block diagram of the voltage monitor 2 interrupt/reset circuit.

Table 8.1 LVD specifications

Parameter		Voltage monitor 0 specifications	Voltage monitor 1 specifications	Voltage monitor 2 specifications
VCC monitoring	Monitored voltage	V_{det0}	V_{det1}	V_{det2}
	Detected event	Voltage falls past V_{det0}	Voltage rises or falls past V_{det1}	Voltage rises or falls past V_{det2}
	Detected voltage	Selectable from three different levels in the OFS1.VDSEL0[1:0] bits	Selectable from three different levels in the LVDLVLR.LVD1LVL[4:0] bits	Selectable from three different levels in the LVDLVLR.LVD2LVL[2:0] bits
	Monitor flag	None	LVD1SR.MON flag: Monitors whether voltage is higher or lower than V_{det1}	LVD2SR.MON flag: Monitors whether voltage is higher or lower than V_{det2}
			LVD1SR.DET flag: V_{det1} passage detection	LVD2SR.DET flag: V_{det2} passage detection
Process on voltage detection	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset when V_{det0} > VCC CPU restart after specified time with VCC > V_{det0}	Reset when V_{det1} > VCC CPU restart timing selectable: after specified time with VCC > V_{det1} or V_{det1} > VCC	Reset when V_{det2} > VCC CPU restart timing selectable: after specified time with VCC > V_{det2} or Vd_{det2} > VCC
	Interrupt	No interrupt	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable interrupt selectable	Non-maskable or maskable interrupt selectable
			Interrupt request issued when V_{det1} > VCC or VCC > V_{det1}	Interrupt request issued when V_{det2} > VCC or VCC > V_{det2}
Digital filter	Enable/ Disable switching	Digital filter function not available	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event linking		None	Available Output of event signals on detection of V_{det1} crossings	Available Output of event signals on detection of V_{det2} crossings



Note 1. See section 7, Option-Setting Memory.

Figure 8.1 Voltage detection 0, 1, and 2 block diagram

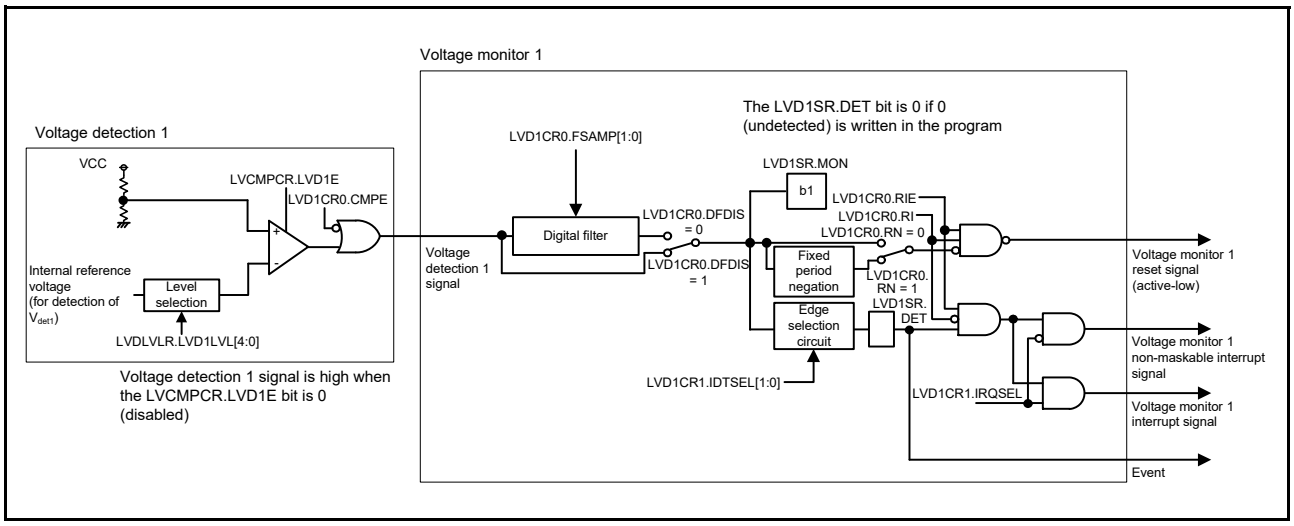


Figure 8.2 Voltage monitor 1 interrupt and reset circuit block diagram

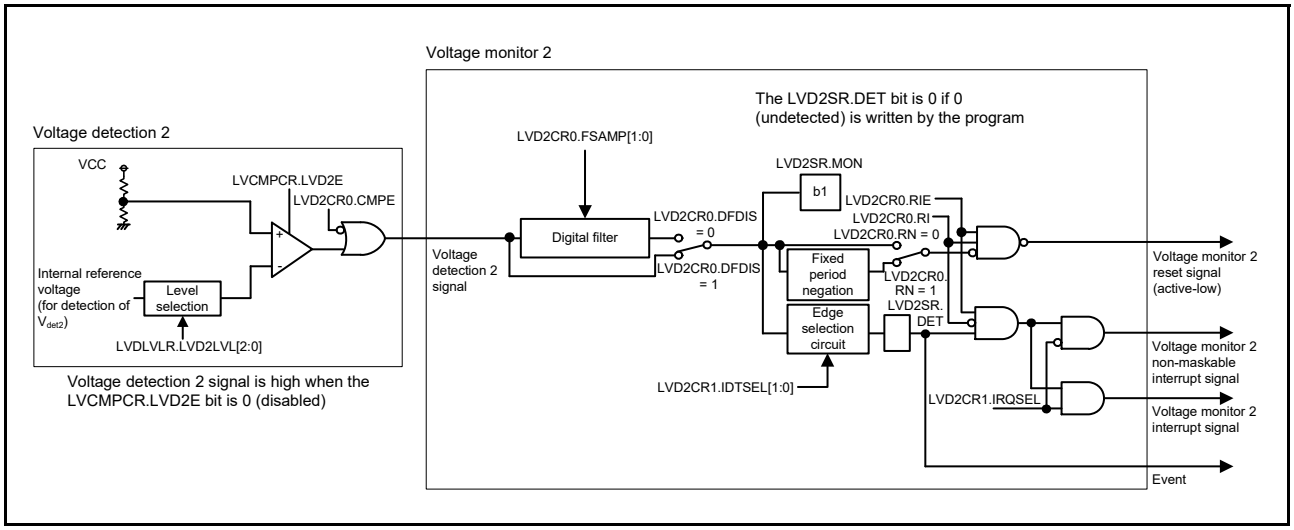


Figure 8.3 Voltage monitor 2 interrupt/reset circuit block diagram

8.2 Register Descriptions

8.2.1 Voltage Monitor 1 Circuit Control Register 1 (LVD1CR1)

Address(es): SYSTEM.LVD1CR1 4001 E0E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	IDTSEL[1:0]	Voltage Monitor 1 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ V_{det1} (rise) is detected 0 1: When VCC < V_{det1} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited.	R/W
b2	IRQSEL	Voltage Monitor 1 Interrupt Type Select	0: Non-maskable interrupt 1: Maskable interrupt.*1	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the NMIER.LVD1EN bit value in the ICU from the reset state.

8.2.2 Voltage Monitor 1 Circuit Status Register (LVD1SR)

Address(es): SYSTEM.LVD1SR 4001 E0E1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	DET	Voltage Monitor 1 Voltage Change Detection Flag	0: Not detected 1: V_{det1} passage detected.	R(/W) *1
b1	MON	Voltage Monitor 1 Signal Monitor Flag	0: VCC < V_{det1} 1: VCC ≥ V_{det1} or MON is disabled.	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 1 Voltage Change Detection Flag)

The DET flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

Set the DET flag to 0 after LVD1CR0.RIE is set to 0 (disabled). LVD1CR0.RIE can be set to 1 (enabled) after 2 or more PCLKB cycles elapse.

MON flag (Voltage Monitor 1 Signal Monitor Flag)

The MON flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

8.2.3 Voltage Monitor 2 Circuit Control Register 1 (LVD2CR1)

Address(es): SYSTEM.LVD2CR1 4001 E0E2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	IDTSEL[1:0]	Voltage Monitor 2 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ V_{det2} (rise) is detected 0 1: When VCC < V_{det2} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited.	R/W
b2	IRQSEL	Voltage Monitor 2 Interrupt Type Select	0: Non-maskable interrupt 1: Maskable interrupt.*1	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the NMIER.LVD1EN bit value in the ICU from the reset state.

8.2.4 Voltage Monitor 2 Circuit Status Register (LVD2SR)

Address(es): SYSTEM.LVD2SR 4001 E0E3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	DET	Voltage Monitor 2 Voltage Change Detection Flag	0: Not detected 1: V_{det2} passage detected.	R(/W) *1
b1	MON	Voltage Monitor 2 Signal Monitor Flag	0: VCC < V_{det2} 1: VCC ≥ V_{det2} or MON is disabled.	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 2 Voltage Change Detection Flag)

The DET flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

Set the DET flag to 0 after LVD2CR0.RIE is set to 0 (disabled). LVD2CR0.RIE can be set to 1 (enabled) after 2 or more PCLKB cycles have elapsed.

MON flag (Voltage Monitor 2 Signal Monitor Flag)

The MON flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

8.2.5 Voltage Monitor Circuit Control Register (LVCMPCR)

Address(es): SYSTEM.LVCMPCR 4001 E417h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	LVD2E	LVD1E	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	LVD1E	Voltage Detection 1 Enable	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled.	R/W
b6	LVD2E	Voltage Detection 2 Enable	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD1E bit (Voltage Detection 1 Enable)

When using voltage detection 1 interrupt/reset or the LVD1SR.MON bit, set the LVD1E bit to 1. The voltage detection 1 circuit starts when $t_{d(E-A)}$ elapses after the LVD1E bit value is changed from 0 to 1. When using the voltage detection 1 circuit in Deep Software Standby mode, do not set the DPSBYCR.DEEPCUT[1:0] bits to 11b.

LVD2E bit (Voltage Detection 2 Enable)

When using voltage detection 2 interrupt/reset or the LVD2SR.MON bit, set the LVD2E bit to 1. The voltage detection 2 circuit starts when $t_{d(E-A)}$ elapses after the LVD2E bit value is changed from 0 to 1. When using the voltage detection 2 circuit in Deep Software Standby mode, do not set the DPSBYCR.DEEPCUT[1:0] bits to 11b.

8.2.6 Voltage Detection Level Select Register (LVDLVLR)

Address(es): SYSTEM.LVDLVLR 4001 E418h

	b7	b6	b5	b4	b3	b2	b1	b0
	LVD2LVL[2:0]			LVD1LVL[4:0]				
Value after reset	1	1	1	1	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	LVD1LVL[4:0]	Voltage Detection 1 Level Select (standard voltage during fall in voltage)	b4 b0 1 0 0 0 1: 2.99 V (V_{det1_1}) 1 0 0 1 0: 2.92 V (V_{det1_2}) 1 0 0 1 1: 2.85 V (V_{det1_3}). Other settings are prohibited.	R/W
b7 to b5	LVD2LVL[2:0]	Voltage Detection 2 Level Select (standard voltage during fall in voltage)	b7 b5 1 0 1: 2.99 V (V_{det2_1}) 1 1 0: 2.92 V (V_{det2_2}) 1 1 1: 2.85 V (V_{det2_3}). Other settings are prohibited.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The contents of the LVDLVLR register can only be changed if the LVCMPCR.LVD1E and LVCMPCR.LVD2E bits (voltage detection n circuit disable, n = 1, 2) are both 0. Do not set LVD detectors 1 and 2 to the same voltage detection level.

8.2.7 Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0)

Address(es): SYSTEM.LVD1CR0 4001 E41Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
Value after reset:	1	0	0	0	x	0	1	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RIE	Voltage Monitor 1 Interrupt/Reset Enable	0: Disable 1: Enable.	R/W
b1	DFDIS	Voltage Monitor 1 Digital Filter Disable Mode Select	0: Enable digital filter 1: Disable digital filter.	R/W
b2	CMPE	Voltage Monitor 1 Circuit Comparison Result Output Enable	0: Disable voltage monitor 1 circuit comparison result output 1: Enable voltage monitor 1 circuit comparison result output.	R/W
b3	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b5, b4	FSAMP[1:0]	Sampling Clock Select	b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency.	R/W

Bit	Symbol	Bit name	Description	R/W
b6	RI	Voltage Monitor 1 Circuit Mode Select	0: Generate voltage monitor 1 interrupt on V_{det1} passage 1: Enable voltage monitor 1 reset when the voltage falls to and below V_{det1}.	R/W
b7	RN	Voltage Monitor 1 Reset Negate Select	0: Negate after a stabilization time (t_{LVD1}) when VCC > V_{det1} is detected 1: Negate after a stabilization time (t_{LVD1}) on assertion of the LVD1 reset.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 1 Interrupt/Reset Enable)

The RIE bit enables or disables the voltage monitor 1 interrupt/reset. Set this bit to ensure that neither a voltage monitor 1 interrupt nor a voltage monitor 1 reset is generated during programming or erasure of the flash memory.

DFDIS bit (Voltage Monitor 1 Digital Filter Disable Mode Select)

The DFDIS bit enables the digital filter circuit. Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) if this bit is 0 (enabled). Set the bit to 1 (disabled) when using the voltage monitor 1 circuit in Software Standby or Deep Software Standby mode.

FSAMP[1:0] bits (Sampling Clock Select)

Only change the FSAMP[1:0] bits when the LVD1CR0.DFDIS bit is 1 (digital filter circuit disabled) but not when LVD1CR0.DFDIS is 0 (digital filter circuit enabled).

RI bit (Voltage Monitor 1 Circuit Mode Select)

When the RI bit is 1 (voltage monitor 1 reset selected) or when the LVD2CR0.RI bit is 1 (voltage monitor 2 reset selected), transition to Software Standby mode can be made but not to Deep Software Standby mode. To enter Deep Software Standby mode, set the RI bit to 0 (voltage monitor 1 interrupt selected) and the LVD2CR0.RI bit to 0 (voltage monitor 2 interrupt selected).

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time on assertion of the LVD1 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). In addition, for a transition to Software Standby or Deep Software Standby, the only possible value for the RN bit is 0 (negation follows a stabilization time when VCC > V_{det1} is detected). Do not set the RN bit to 1 when this is the case.

8.2.8 Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0)

Address(es): SYSTEM.LVD2CR0 4001 E41Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
Value after reset:	1	0	0	0	x	0	1	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RIE	Voltage Monitor 2 Interrupt/Reset Enable	0: Disable 1: Enable.	R/W
b1	DFDIS	Voltage Monitor 2 Digital Filter Disable Mode Select	0: Enable digital filter 1: Disable digital filter.	R/W
b2	CMPE	Voltage Monitor 2 Circuit Comparison Result Output Enable	0: Disable voltage monitor 2 circuit comparison result output 1: Enable voltage monitor 2 circuit comparison result output.	R/W
b3	—	Reserved	The read value is undefined. The write value should be 1.	R/W

Bit	Symbol	Bit name	Description	R/W
b5, b4	FSAMP[1:0]	Sampling Clock Select	b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency.	R/W
b6	RI	Voltage Monitor 2 Circuit Mode Select	0: Generate voltage monitor 2 interrupt on V_{det2} passage 1: Enable voltage monitor 2 reset when the voltage falls to and below V_{det2}.	R/W
b7	RN	Voltage Monitor 2 Reset Negate Select	0: Negate after a stabilization time (t_{LVD2}) when VCC > V_{det2} is detected 1: Negate after a stabilization time (t_{LVD2}) on assertion of the LVD2 reset.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 2 Interrupt/Reset Enable)

The RIE bit enables or disables voltage monitor 2 interrupt/reset. Set this bit to ensure that neither a voltage monitor 2 interrupt nor a voltage monitor 2 reset is generated during programming or erasure of the flash memory.

DFDIS bit (Voltage Monitor 2 Digital Filter Disable Mode Select)

The DFDIS bit enables the digital filter circuit. Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) if this bit is 0 (enabled). Set the bit to 1 (disabled) when using the voltage monitor 2 circuit in Software Standby or Deep Software Standby mode.

FSAMP[1:0] bits (Sampling Clock Select)

Only change the FSAMP[1:0] bits when the LVD2CR0.DFDIS bit is 1 (digital filter circuit disabled), but not when LVD2CR0.DFDIS is 0 (digital filter circuit enabled).

RI bit (Voltage Monitor 2 Circuit Mode Select)

When the RI bit is 1 (voltage monitor 2 reset selected) or when the LVD1CR0.RI bit is 1 (voltage monitor 1 reset selected), transition to Software Standby mode can be made but not to Deep Software Standby mode. To enter Deep Software Standby mode, set the RI bit to 0 (voltage monitor 2 interrupt selected) and the LVD1CR0.RI bit to 0 (voltage monitor 1 interrupt selected).

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is set to 1 (negation follows a stabilization time on assertion of the LVD2 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). Additionally, for a transition to Software Standby or Deep Software Standby mode, the only possible value for the RN bit is 0 (negation follows a stabilization time when VCC > V_{det2} is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal) when this is the case.

8.3 VCC Input Voltage Monitor

8.3.1 Monitoring V_{det0}

The comparison results from voltage monitor 0 are not available for reading.

8.3.2 Monitoring V_{det1}

Table 8.2 shows the procedure to set up monitoring against V_{det1}. After the settings are complete, the comparison results from voltage monitor 1 can be monitored with the LVD1SR.MON flag.

Table 8.2 Procedure to set up monitoring against V_{det1}

Step		Monitoring the comparison results from voltage monitor 1
Setting the voltage detection 1 circuit	1	Set LVCMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVDLVLR register.
	2	Select the detection voltage in the LVDLVLR.LVD1LVL[4:0] bits.
	3	Set LVCMPCR.LVD1E = 1 to enable voltage detection 1.
	4	Wait for at least $t_{d(E-A)}$ for the LVD operation stabilization time after LVD is enabled.*1
Setting the digital filter*2	5	Select the sampling clock for the digital filter in the LVD1CR0.FSAMP[1:0] bits.
	6	Set LVD1CR0.DFDIS = 0 to enable the digital filter.
	7	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, 16 and the sampling clock for the digital filter is the LOCO frequency divided by n.
Enabling output	8	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.

Note 1. Steps 5 to 7 can be performed during the wait time in step 4. For details on $t_{d(E-A)}$, see section 43, Electrical Characteristics.

Note 2. Steps 5 to 7 are not required if the digital filter is not in use.

8.3.3 Monitoring V_{det2}

Table 8.3 shows the procedure to set up monitoring against V_{det2}. After the settings are complete, the comparison results from voltage monitor 2 can be monitored with the LVD2SR.MON flag.

Table 8.3 Procedure to set up monitoring against V_{det2}

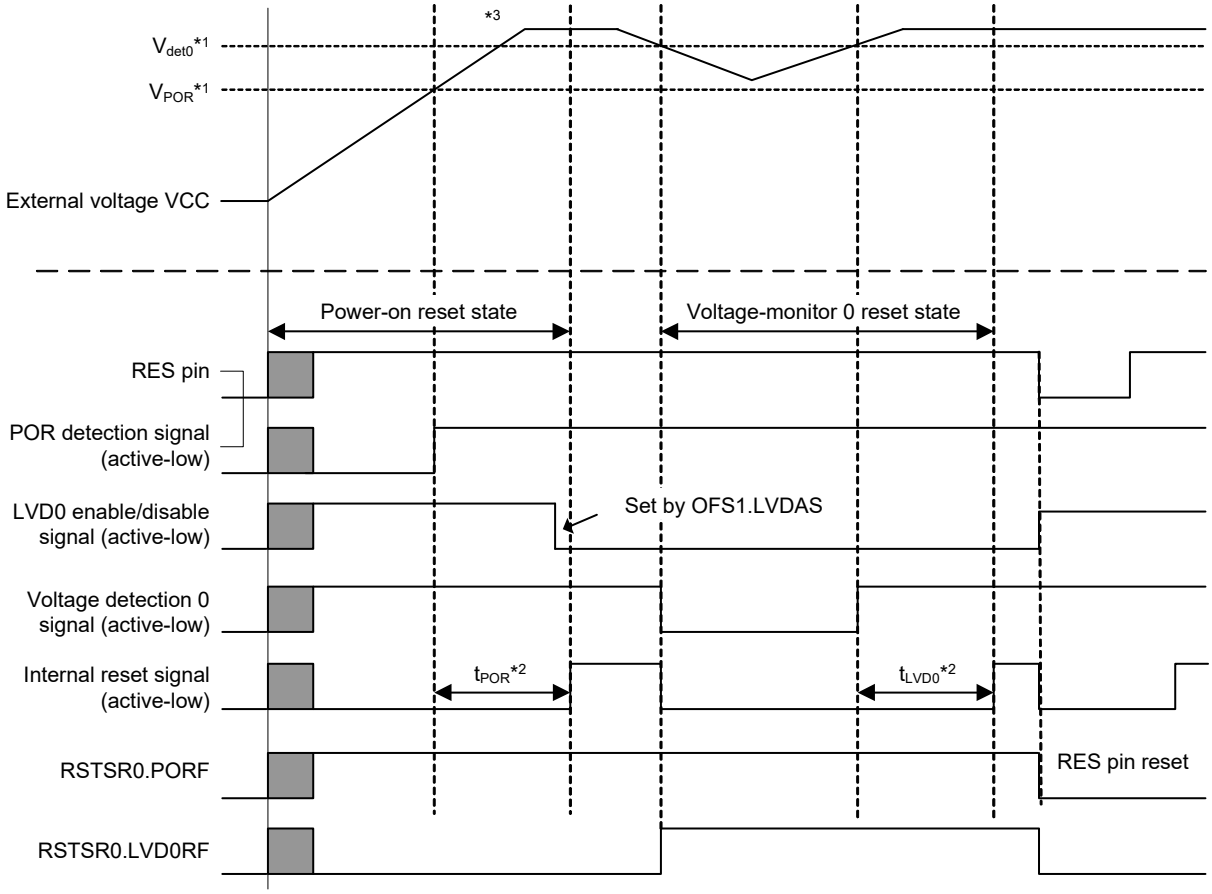
Step		Monitoring the comparison results by voltage monitor 2
Setting up the voltage detection 2 circuit	1	Set LVCMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVDLVLR register.
	2	Select the detection voltage in the LVDLVLR.LVD2LVL[2:0] bits.
	3	Set LVCMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.
	4	Wait for at least $t_{d(E-A)}$ for the LVD operation stabilization time after LVD is enabled.*1
Setting up the digital filter*2	5	Select the sampling clock for the digital filter in the LVD2CR0.FSAMP[1:0] bits.
	6	Set LVD2CR0.DFDIS = 0 to enable the digital filter.
	7	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, 16 and the sampling clock for the digital filter is the LOCO frequency divided by n.
Enabling output	8	Set LVD2CR0.CMPE = 1 to enable output of the comparison results by voltage monitor 2.

Note 1. Steps 5 to 7 can be performed during the wait time in step 4. For details on $t_{d(E-A)}$, see section 43, Electrical Characteristics.

Note 2. Steps 5 to 7 are not required if the digital filter is not in use.

8.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the OFS1.LVDAS bit to 0 to enable the voltage monitor 0 reset after a reset. However, at boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit. Figure 8.4 shows an example of operations for a voltage monitor 0 reset.



Note: For details of the electrical characteristics, see section 43, Electrical Characteristics.
Note 1. V_{POR} indicates the detection level for a power-on reset and V_{det0} indicates the detection level for a voltage monitor 0 reset.
Note 2. t_{POR} indicates the period of a power-on reset and t_{LVD0} indicates the period of a voltage monitor 0 reset.
Note 3. At power-on, raise VCC to the minimum guaranteed voltage before releasing the POR reset.

Figure 8.4 Example of voltage monitor 0 reset operation

8.5 Interrupt and Reset from Voltage Monitor 1

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 1 circuit.

Table 8.4 shows the procedure for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring operates. Table 8.5 shows the procedure for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring stops. Figure 8.5 shows an example of operations for a voltage monitor 1 interrupt. For the operation of the voltage monitor 1 reset, see Figure 6.2 in section 6, Resets.

When using the voltage monitor 1 circuit in Software Standby or Deep Software Standby, set the circuit with the following procedures.

(1) Settings in Software Standby mode

- Disable the digital filter (LVD1CR0.DFDIS = 1)
- When VCC > V_{det1} is detected, negate the voltage monitor 1 reset signal (LVD1CR0.RN = 0) following a stabilization time.

(2) Settings in Deep Software Standby mode

- Disable the digital filter (LVD1CR0.DFDIS = 1)

- Enable voltage monitor 1 interrupts (LVD1CR0.RI = 0). If the voltage monitor 1 reset is enabled (LVD1CR0.RI = 1), a transition to Deep Software Standby mode is not possible, and the operation transitions to Software Standby mode instead
- When the DPSBYCR.DEEPCUT[1:0] bits are 11b, the voltage monitor 1 circuit stops. To use the voltage monitor 1 circuit in Deep Software Standby mode, set the DPSBYCR.DEEPCUT[1:0] bits to a value other than 11b.

Table 8.4 Procedure for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring operates

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output)	Voltage monitor 1 reset
Setting the voltage detection 1 circuit	1	Set LVCMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVDLVLR register.	
	2	Select the detection voltage in the LVDLVLR.LVD1LVL[3:0] bits.	
	3	Set LVCMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.	
	4	Wait for at least $t_{d(E-A)}$ for the LVD operation stabilization time after LVD is enabled.*1	
Setting the digital filter *2	5	Select the sampling clock for the digital filter in the LVD1CR0.FSAMP[1:0] bits.	
	6	Set LVD1CR0.DFDIS = 0 to enable the digital filter.	
	7	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, 16 and the sampling clock for the digital filter is the LOCO frequency divided by n.*4	
Setting the voltage monitor 1 interrupt or reset	8	Set LVD1CR0.RI = 0 to select the voltage monitor 1 interrupt.	• Set LVD1CR0.RI = 1 to select the voltage monitor 1 reset • Select the type of reset negation in the LVD1CR0.RN bit.
	9	• Select the interrupt request timing in the LVD1CR1.IDTSEL[1:0] bits • Select the interrupt type in the LVD1CR1.IRQSEL bit.	—
Enabling output	10	Set LVD1SR.DET = 0.	
	11	Set LVD1CR0.RIE = 1 to enable the voltage monitor 1 interrupt or reset.*3	
	12	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.	

Note 1. Steps 5 to 11 can be performed during the wait time in step 4. For details on $t_{d(E-A)}$, see section 43, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.
Note 3. Step 11 is not required if only the ELC event signal is to be output.
Note 4. Steps 8 to 11 can be performed during the wait time in step 7.

Table 8.5 Procedure for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring stops

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output), voltage monitor 1 reset
Stopping the enabling of output	1	Set LVD1CR0.CMPE = 0 to disable output of the comparison results by voltage monitor 1.
	2	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, 16 and the sampling clock for the digital filter is the LOCO frequency divided by n.*1
	3	Set LVD1CR0.RIE = 0 to disable the voltage monitor 1 interrupt or reset.*2
Stopping the digital filter	4	Set LVD1CR0.DFDIS = 1 to disable the digital filter.*1, *3
Stopping the voltage detection 1 circuit	5	Set LVCMPCR.LVD1E = 0 to disable the voltage detection 1 circuit.

Note 1. Steps 2 and 4 are not required if the digital filter is not in use.
Note 2. Step 3 is not required if only the ELC event signal is to be output.
Note 3. To disable the digital filter from its enabled state and then re-enable it, disable it and wait for at least 2 LOCO clock cycles before re-enabling it.

If the voltage monitor 1 interrupt or reset setting is to be made again after it is used and stopped once, omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting or stopping the voltage detection 1 circuit is not required if the settings for the circuit do not change
- Setting or stopping the digital filter is not required if the settings for the digital filter do not change
- Setting the voltage monitor 1 interrupt or reset is not required if the settings for the voltage monitor 1 interrupt or reset do not change.

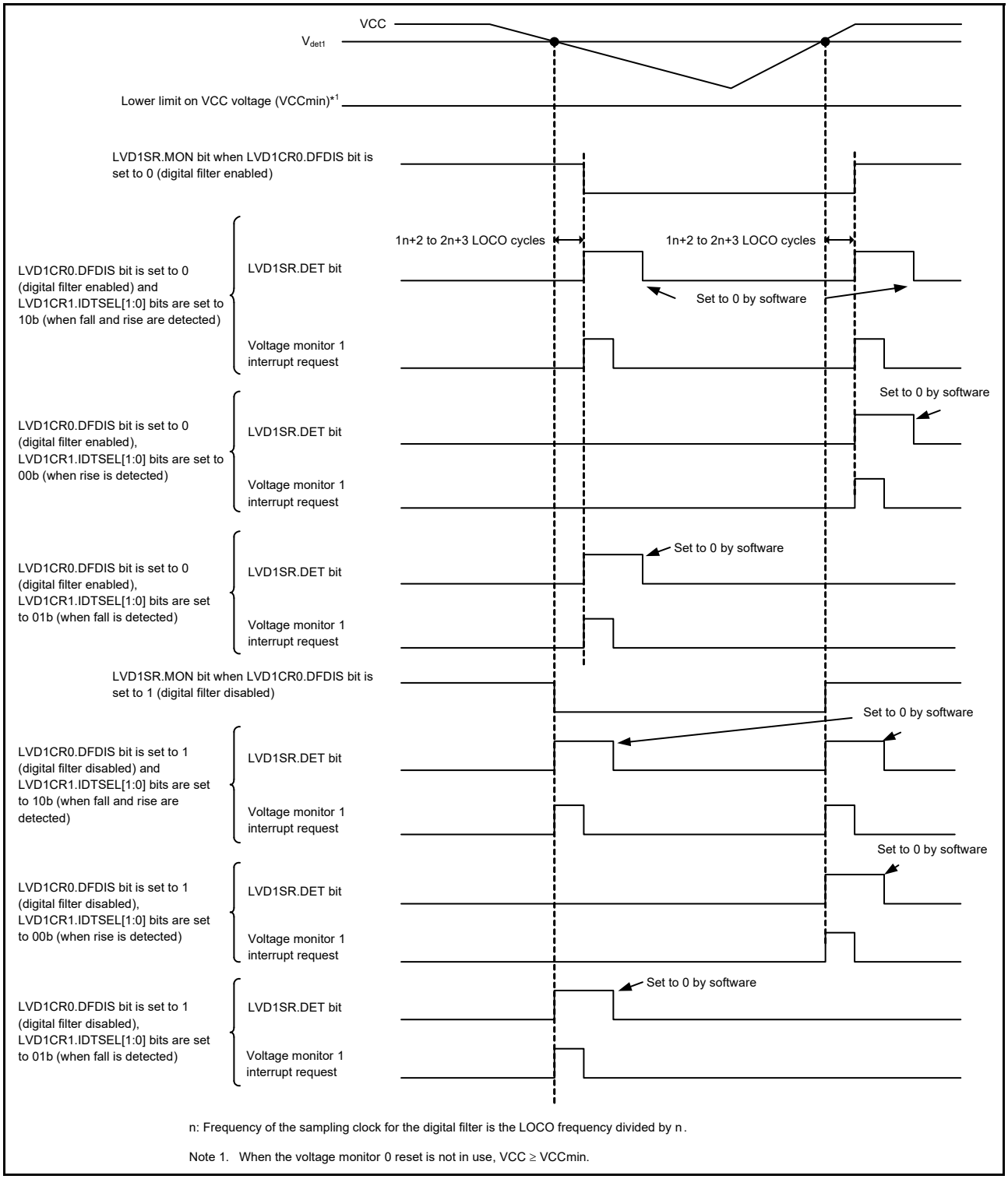


Figure 8.5 Voltage monitor 1 interrupt operation example

8.6 Interrupt and Reset from Voltage Monitor 2

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 2 circuit.

Table 8.6 shows the procedure for setting bits related to the voltage monitor 2 interrupt and reset so that voltage monitoring operates. Table 8.7 shows the procedure for setting bits related to the voltage monitor 2 interrupt and reset so that voltage monitoring stops. Figure 8.6 shows an example of operations for a voltage monitor 2 interrupt. For the operation of the voltage monitor 2 reset, see Figure 6.2 in section 6, Resets.

When using the voltage monitor 2 circuit in Software Standby or Deep Software Standby, set up the circuit with the following procedures.

(1) Setting in Software Standby mode

- Disable the digital filter (LVD2CR0.DFDIS = 1)
- When VCC > V_{det2} is detected, negate the voltage monitor 2 reset signal (LVD2CR0.RN = 0) following the stabilization time.

(2) Setting in Deep Software Standby mode

- Disable the digital filter (LVD2CR0.DFDIS = 1)
- Enable voltage monitor 2 interrupts (LVD2CR0.RI = 0). If the voltage monitor 2 reset is enabled (LVD2CR0.RI = 1), a transition to Deep Software Standby mode is not possible, and the operation transitions to Software Standby mode instead.
- When the DPSBYCR.DEEPCUT[1:0] bits are 11b, the voltage monitor 2 circuit stops. To use the voltage monitor 2 circuit in Deep Software Standby mode, set the DPSBYCR.DEEPCUT[1:0] bits to a value other than 11b.

Table 8.6 Procedure for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring operates

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output)	Voltage monitor 2 reset
Setting the voltage detection 2 circuit	1	Set LVCMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVDLVLR register.	
	2	Select the detection voltage in the LVDLVLR.LVD2LVL[2:0] bits.	
	3	Set LVCMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.	
	4	Wait for at least $t_{d(E-A)}$ for the LVD operation stabilization time after LVD is enabled.*1	
Setting the digital filter *2	5	Select the sampling clock for the digital filter in the LVD2CR0.FSAMP[1:0] bits.	
	6	Set LVD2CR0.DFDIS = 0 to enable the digital filter.	
	7	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n.*4	
Setting the voltage monitor 2 interrupt or reset	8	Set LVD2CR0.RI = 0 to select the voltage monitor 2 interrupt.	• Set LVD2CR0.RI = 1 to select the voltage monitor 2 reset • Select the type of reset negation in the LVD2CR0.RN bit.
	9	• Select the interrupt request timing in the LVD2CR1.IDTSEL[1:0] bits • Select the interrupt type in the LVD2CR1.IRQSEL bit.	—
Enabling output	10	Set LVD2SR.DET = 0.	
	11	Set LVD2CR0.RIE = 1 to enable the voltage monitor 2 interrupt or reset.*3	
	12	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.	

Note 1. Steps 5 to 11 can be performed during the wait time in step 4. For details on $t_{d(E-A)}$, see section 43, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.
Note 3. Step 11 is not required if only the ELC event signal is to be output.
Note 4. Steps 8 to 10 can be performed during the wait time in step 7.

Table 8.7 Procedure for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring stops

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output), voltage monitor 2 reset
Stopping the enabling output	1	Set LVD2CR0.CMPE = 0 to disable output of the comparison results by voltage monitor 2.
	2	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n.*1
	3	Set LVD2CR0.RIE = 0 to disable the voltage monitor 2 interrupt or reset.*2
Stopping the digital filter	4	Set LVD2CR0.DFDIS = 1 to disable the digital filter.*1, *3
Stopping the voltage detection 1 circuit	5	Set LVCMPCR.LVD2E = 0 to disable the voltage detection 2 circuit.

Note 1. Steps 2 and 4 are not required if the digital filter is not in use.
Note 2. Step 3 is not required if only the ELC event signal is to be output.
Note 3. To disable the digital filter from its enabled state and then re-enable it, disable it and wait for at least 2 LOCO cycles before re-enabling it.

If the voltage monitor 2 interrupt or reset setting is to be made again after it is used and stopped once, omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting or stopping the voltage detection 2 circuit is not required if the settings for the circuit do not change
- Setting or stopping the digital filter is not required if the settings for the digital filter do not change
- Setting the voltage monitor 2 interrupt or reset is not required if the settings for the voltage monitor 2 interrupt or voltage monitor 2 reset do not change.

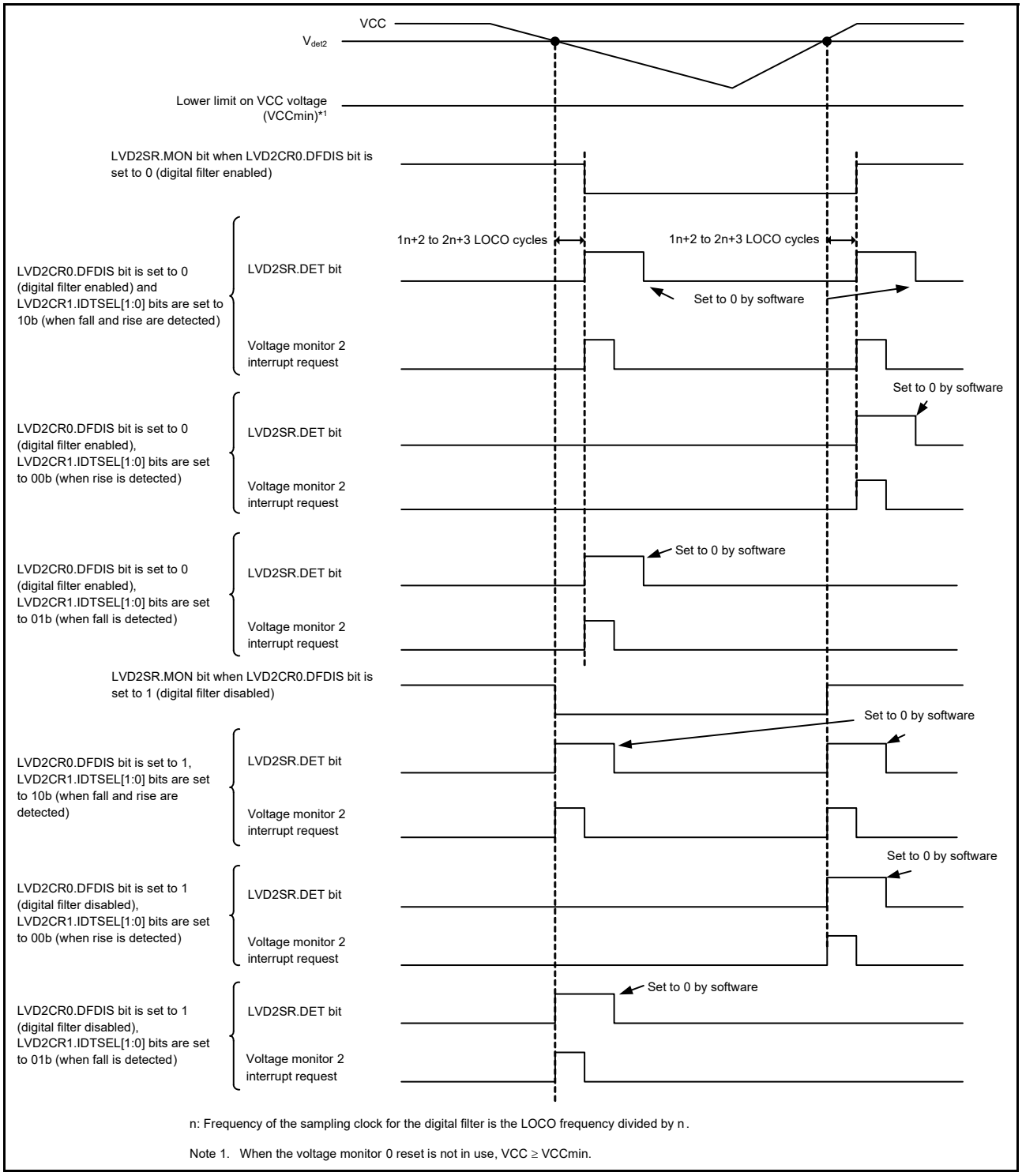


Figure 8.6 Example of voltage monitor 2 interrupt operation

8.7 Event Link Output

The LVD can output the event signals to the Event Link Controller (ELC).

(1) V_{det1} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det1} voltage while both the voltage detection 1 circuit and the voltage monitor 1 circuit comparison result output are enabled.

(2) V_{det2} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det2} voltage while both the voltage detection 2 circuit and the voltage monitor 2 circuit comparison result output are enabled.

When enabling the event link output function of the LVD, you must enable the LVD before enabling the LVD event link function of the ELC. To stop the event link output function of the LVD, you must stop the LVD after disabling the LVD event link function of the ELC.

8.7.1 Interrupt Handling and Event Linking

The LVD provides bits to individually enable or disable the voltage monitor 1 and 2 interrupts. When an interrupt source is generated and the interrupt is enabled by the interrupt enable bit, the interrupt signal (LVD1CR0.RIE or LVD2CR0.RIE) is output to the CPU.

On the other hand, as soon as an interrupt source is generated, an event link signal is output as the event signal to the other module through the ELC, regardless of the state of the interrupt enable bit.

It is possible to output voltage monitor 1 and 2 interrupts in Software Standby and Deep Software Standby modes. The event signals for the ELC in Software Standby and Deep Software Standby modes are output as follows:

- When a V_{det1} or V_{det2} passage event is detected in Software Standby mode, event signals are not generated for the ELC because the clock is not supplied in Software Standby mode. Because the V_{det1} and V_{det2} passage detection flags are saved, when the clock supply resumes after returning from Software Standby mode, the event signals for the ELC are output based on the state of the V_{det1} and V_{det2} detection flags.
- When a V_{det1} or V_{det2} passage events is detected in Deep Software Standby mode, event signals are not generated for the ELC.

9. Clock Generation Circuit

9.1 Overview

The MCU provides a clock generation circuit.

Table 9.1 and Table 9.2 list the clock generation circuit specifications. Figure 9.1 shows a block diagram, and Table 9.3 lists the I/O pins.

Table 9.1 Clock generation circuit specifications for the clock sources

Clock source	Description	Specifications
Main clock oscillator (MOSC)	Resonator frequency	8 MHz to 24 MHz
	External clock input frequency	Up to 24 MHz
	External resonator or additional circuit: ceramic resonator, crystal	Available
	Connection pins EXTAL, XTAL	
	Drive capability switching	
	Oscillation stop detection function	
Sub-clock oscillator (SOSC)	Resonator frequency	32.768 kHz
	External resonator or additional circuit: crystal resonator	Available
	Connection pins: XCIN, XCOUT	
	Drive capability switching	
PLL circuit	Input clock source	MOSC, HOCO
	Input pulse frequency division ratio	Selectable from 1, 2, and 3
	Input frequency	8 MHz to 24 MHz
	Frequency multiplication ratio	Selectable from 10 to 30 (0.5 steps)
	PLL output frequency	120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency	16/18/20 MHz
	User trimming	Available
Middle-speed on-chip oscillator (MOCO)	Oscillation frequency	8 MHz
	User trimming	Available
Low-speed on-chip oscillator (LOCO)	Oscillation frequency	32.768 kHz
	User trimming	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	Oscillation frequency	15 kHz
External clock input for JTAG (TCK)	Input clock frequency	Up to 25 MHz
External clock input for SWD (SWCLK)	Input clock frequency	Up to 25 MHz

Table 9.2 Clock generation circuit specifications for the internal clocks (1 of 2)

Parameter	Clock sources	Clock supply	Specifications
System clock (ICLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	CPU, DTC, DMAC, Flash, SRAM	Up to 120 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Peripheral module clock A (PCLKA)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	Peripheral modules (SPI, SCI, SCE7, CRC, IrDA, GPT bus clock)	Up to 120 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64

Table 9.2 Clock generation circuit specifications for the internal clocks (2 of 2)

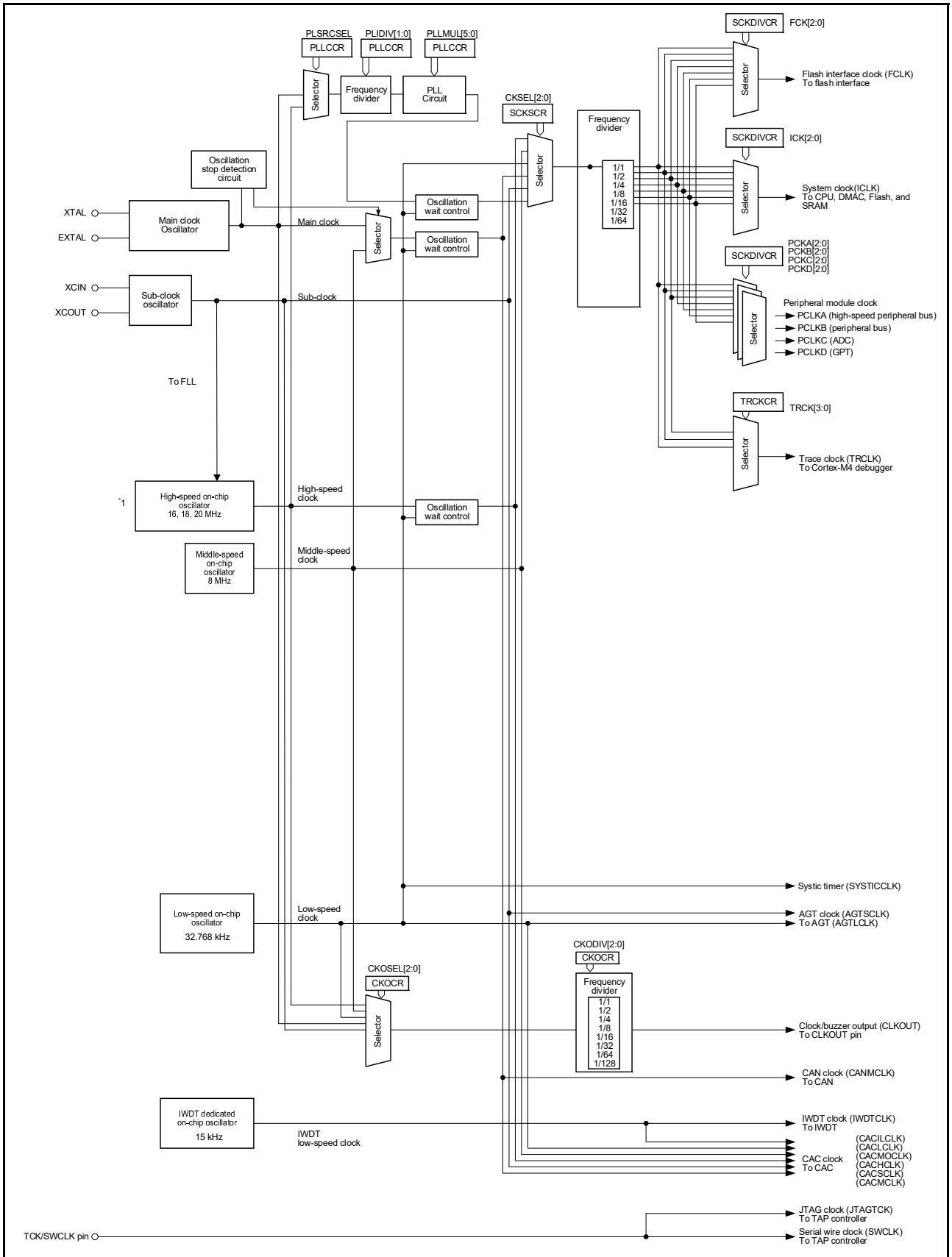
Parameter	Clock sources	Clock supply	Specifications
Peripheral module clock B (PCLKB)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	Peripheral modules (IIC, DOC, CAC, CAN, DAC12, POEG, AGT, ELC, I/O ports, WDT, IWDT, ADC12, KINT, ACMPHS, TSN)	Up to 60 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Peripheral module clock C (PCLKC)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	Peripheral module (ADC12 conversion clock)	Up to 60 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Peripheral module clock D (PCLKD)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	Peripheral module (GPT count clock)	Up to 120 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Flash interface clock (FCLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	Flash interface	4 to 60 MHz (P/E) Up to 60 MHz (read) *1 Division ratios: 1, 2, 4, 8, 16, 32, 64
CAN clock (CANMCLK)	MOSC	CAN	8 to 24 MHz
AGT clock (AGTSCLK, AGTLCLK)	SOSC, LOCO	AGT	32.768 kHz
CAC main clock (CACMCLK)	MOSC	CAC	Up to 24 MHz
CAC sub-clock (CACSCLK)	SOSC	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz
CAC HOCO clock (CACHCLK)	HOCO	CAC	16, 18, 20 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick timer clock (SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
JTAG clock (JTAGTCK)	TCK pin	JTAG	Up to 25 MHz
Clock and buzzer output (CLKOUT)	MOSC, SOSC, LOCO, MOCO, HOCO	CLKOUT pin	Up to 24 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64, 128
Serial wire clock (SWCLK)	SWCLK pin	OCD	Up to 25 MHz
Trace clock (TRCLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	CPU-OCD	Up to 60 MHz Division ratios: 1, 2, 4
TCLK pin output (TCLK)	1/2 TRCLK	TCLK pin	Up to 30 MHz

Note: Restrictions on setting the clock frequency: ICLK ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKA ≥ PCLKB
Restrictions on the clock frequency ratio (N: integer, and up to 64):
ICLK:FCLK = N:1, ICLK:PCLKA = N:1, ICLK:PCLKB = N:1
ICLK:PCLKC = N:1 or 1:N, ICLK:PCLKD = N:1 or 1:N
If the A/D converter is enabled, the clock frequency ratio is constrained as follows:
PCLKB:PCLKC = 1:1 or 1:2 or 1:4 or 2:1 or 4:1 or 8:1.

Note: Clocks have a permissible frequency range. See Table 9.2.
Flash memory also has a permissible operating frequency range in each wait cycle setting. See section 41, Flash Memory.
Those clock frequency ranges must be satisfied even when the HOCO has its maximum or minimum frequency. See section 43, Electrical Characteristics.

Note: If the PLL reference clock source is HOCO, the PLL multiplication setting must be set to 120 MHz - 240 MHz in consideration of HOCO frequency (minimum/maximum).

Note 1. The minimum FCLK frequency is 4 MHz in Programming/Erasure (P/E) mode.



Note 1. HOCO has FLL.

Figure 9.1 Clock generation circuit block diagram

Table 9.3 Clock Generation Circuit I/O pins

Pin name	I/O	Description
XTAL	Output	These pins are used to connect a crystal resonator. The EXTAL pin can also be used to input an external clock. For details, see section 9.3.2, External Clock Input.
EXTAL	Input	
XCIN	Input	These pins are used to connect to a 32.768-kHz crystal resonator
XCOUT	Output	
TCK/SWCLK	Input	This pin is used to input the clock for the JTAG
CLKOUT	Output	This pin is used to output the CLKOUT/BUZZER clock

9.2 Register Descriptions

9.2.1 System Clock Division Control Register (SCKDIVCR)

Address(es): SYSTEM.SCKDIVCR 4001 E020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
Value after reset:	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	PCKD[2:0]	Peripheral Module Clock D (PCLKD) Select*3	b2 b0 0 0: ×1/1 0 1: ×1/2 1 0: ×1/4 1 1: ×1/8 0 0: ×1/16 0 1: ×1/32 1 0: ×1/64. Other settings are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	PCKC[2:0]	Peripheral Module Clock C (PCLKC) Select*3	b6 b4 0 0: ×1/1 0 1: ×1/2 1 0: ×1/4 1 1: ×1/8 0 0: ×1/16 0 1: ×1/32 1 0: ×1/64. Other settings are prohibited.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10 to b8	PCKB[2:0]	Peripheral Module Clock B (PCLKB) Select*2	b10 b8 0 0: ×1/1 0 1: ×1/2 1 0: ×1/4 1 1: ×1/8 0 0: ×1/16 0 1: ×1/32 1 0: ×1/64. Other settings are prohibited.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b14 to b12	PCKA[2:0]	Peripheral Module Clock A (PCLKA) Select*2	b14 b12 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b16, b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b23 to b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b24	ICK[2:0]	System Clock (ICLK) Select*1*2*3*4	b26 b24 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b30 to b28	FCK[2:0]	Flash Interface Clock (FCLK) Select*1	b30 b28 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. The association between the frequencies of the system clock (ICLK) and the flash interface clock (FCLK) should be ICLK:FCLK = N:1 (N: integer).
If a setting is made where ICLK < FCLK, then that setting is ignored.
Note 2. The association between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKA, PCLKB) should be ICLK:PCLKA = N:1, ICLK:PCLKB = N:1 (N: integer).
If a setting is made where ICLK < PCLKA or ICLK < PCLKB, then that setting is ignored.
Note 3. The association between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKC, PCLKD) should be ICLK:PCLKC, PCLKD = N:1 or 1:N (N: integer).
Note 4. The frequency of the system clock (ICLK) is limited to the Flash Wait Cycle register (FLWT). See section 41, Flash Memory.

The SCKDIVCR register selects the frequencies of the system clock (ICLK), the peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), and the flash interface clock (FCLK).

When the PLL is selected as the clock source, set the following modules to the module-stop state before changing the value of SCKDIVCR:

- SCE7
- GPT32EH
- GPT32E.

In addition, when changing a value in SCKDIVCR from a lower division ratio to a higher division ratio, wait at least 750 ns before changing the value. When changing a value from a higher division ratio to a lower division ratio, wait at least 250 ns after changing the value, before starting subsequent processing.

The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

Figure 9.2 shows an example flow for changing the value of SCKDIVCR.

PCKD[2:0] bits (Peripheral Module Clock D (PCLKD) Select*3)

The PCKD[2:0] bits select the frequency of peripheral module clock D (PCLKD).

PCKC[2:0] bits (Peripheral Module Clock C (PCLKC) Select*3)

The PCKC[2:0] bits select the frequency of peripheral module clock C (PCLKC).

PCKB[2:0] bits (Peripheral Module Clock B (PCLKB) Select*2)

The PCKB[2:0] bits select the frequency of peripheral module clock B (PCLKB).

PCKA[2:0] bits (Peripheral Module Clock A (PCLKA) Select*2)

The PCKA[2:0] bits select the frequency of peripheral module clock A (PCLKA).

ICK[2:0] bits (System Clock (ICLK) Select*1*2*2*3*4)

The ICK[2:0] bits select the frequency of the system clock for the CPU, DMAC, and DTC.

FCK[2:0] bits (Flash Interface Clock (FCLK) Select*1)

The FCK[2:0] bits select the frequency of the flash interface clock (FCLK).

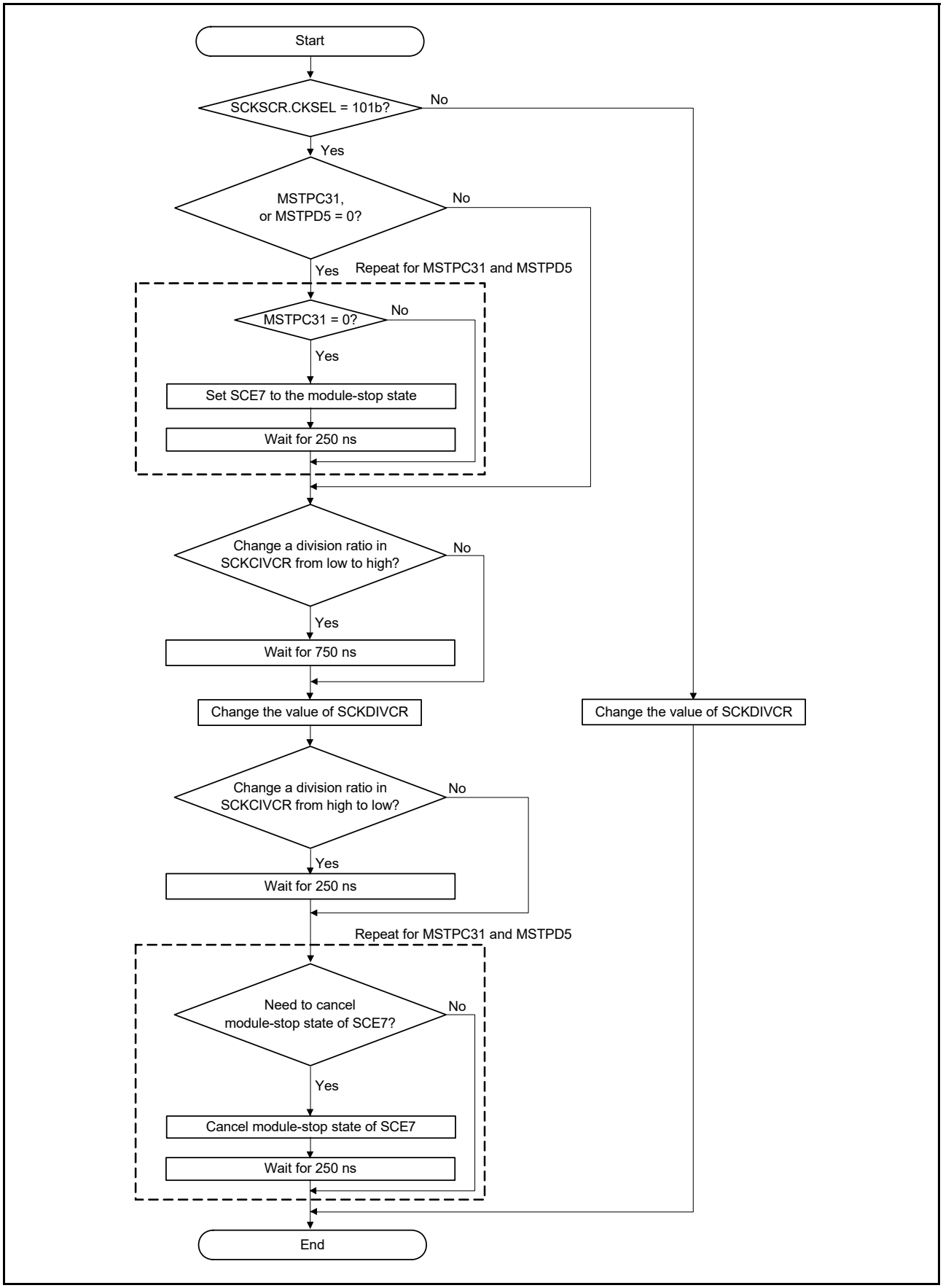


Figure 9.2 Example flow for changing the SCKDIVCR value

9.2.2 System Clock Source Control Register (SCKSCR)

Address(es): SYSTEM.SCKSCR 4001 E026h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKSEL[2:0]	Clock Source Select	b2 b0 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: Main clock oscillator 1 0 0: Sub-clock oscillator 1 0 1: PLL. Other settings are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Write to SCKSCR by 8-bit access.

The SCKSCR register selects the clock source for the system clock.

When changing the value of SCKSCR to either select or deselect the PLL, set the following modules to the module-stop state before changing the SCKSCR value:

- SCE7
- GPT32EH
- GPT32E.

In addition, when changing the value of SCKSCR from the PLL to a different clock source, wait at least 750 ns before changing the value. When changing the value from a non-PLL clock source to the PLL, wait at least 250 ns after changing the value, before starting subsequent processing.

The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

Figure 9.3 shows an example flow for changing the value of SCKSCR.

CKSEL[2:0] bits (Clock Source Select)

The CKSEL[2:0] bits select the clock source for the following modules:

- System clock (ICLK)
- Peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD)
- Flash interface clock (FCLK).

The bits select from one of the following sources:

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)
- Main clock oscillator
- Sub-clock oscillator
- PLL circuit.

The clock sources should be switched when there are no occurring internal asynchronous interrupt. Transitions to clock sources that are not in operation are prohibited.

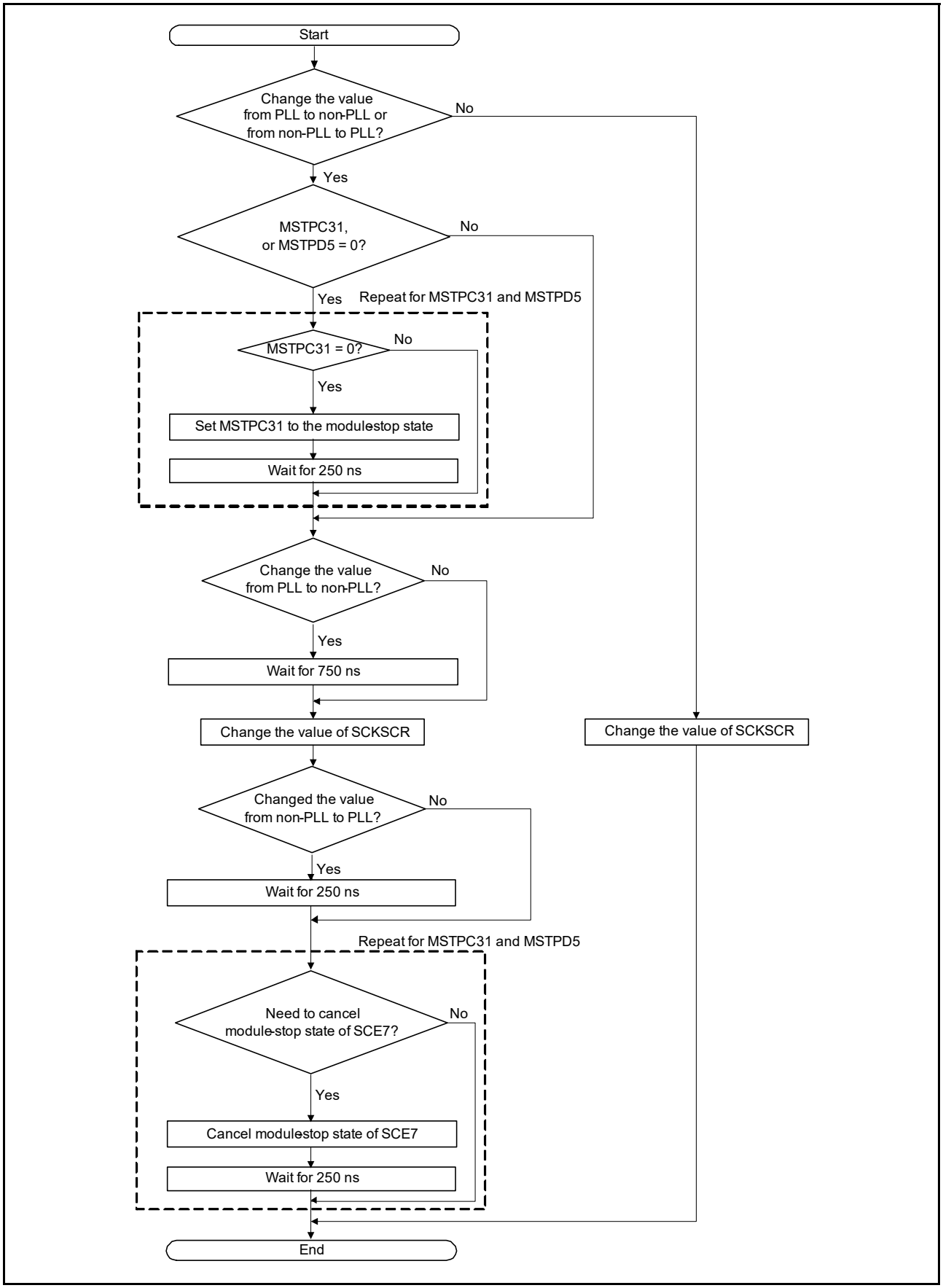


Figure 9.3 Example flow for changing the value of SCKSCR

9.2.3 PLL Clock Control Register (PLLCCR)

Address(es): SYSTEM.PLLCCR 4001 E028h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PLLMUL[5:0]						—	—	—	PLSRCSEL	—	—	PLIDIV[1:0]	
Value after reset:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PLIDIV[1:0]	PLL Input Frequency Division Ratio Select*1	b1 b0 0 0: × 1 0 1: × 1/2 1 0: × 1/3 1 1: Setting prohibited.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	PLSRCSEL	PLL Clock Source Select	0: Main clock oscillator 1: HOCO.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	PLLMUL[5:0]	PLL Frequency Multiplication Factor Select*2	b13 b8 0 1 0 0 1 1: × 10.0 0 1 0 1 0 0: × 10.5 0 1 0 1 0 1: × 11.0 … 0 1 1 1 0 0: × 14.5 0 1 1 1 0 1: × 15.0 0 1 1 1 1 0: × 15.5 … 1 1 1 0 1 0: × 29.5 1 1 1 0 1 1: × 30.0. Other settings are prohibited.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. PLIDIV[1:0] must be set so that the frequency of the PLL input signal is within the range listed in Table 9.1.
Note 2. PLLMUL[5:0] must be set so that the frequency of the PLL output signal is within the range listed in Table 9.1.

The PLLCCR register sets the operation of the PLL circuit. Writing to the PLLCCR is prohibited when the PLLCR.PLLSTP bit is 0, that is, when the PLL is operating.

PLIDIV[1:0] bits (PLL Input Frequency Division Ratio Select*1)

The PLIDIV[1:0] bits select the frequency division ratio for the PLL clock source.

PLSRCSEL bit (PLL Clock Source Select)

The PLSRCSEL bit selects the clock source for the PLL.

PLLMUL[5:0] bits (PLL Frequency Multiplication Factor Select*2)

The PLLMUL[5:0] bits select the frequency multiplication factor for the PLL circuit.

9.2.4 PLL Control Register (PLLCR)

Address(es): SYSTEM.PLLCR 4001 E02Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PLLSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	PLLSTP	PLL Stop Control	0: Operate the PLL 1: Stop the PLL.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PLLCR register controls the operation of the PLL circuit.

PLLSTP bit (PLL Stop Control)

The PLLSTP bit starts or stops the PLL circuit. When selecting the main clock oscillator as the clock source for the PLL in the PLLCCR.PLSRCSEL bit, you must also set the Main Clock Oscillator Wait Control Register (MOSCWTCR).

After setting the PLLSTP bit to 0, confirm that the OSCSF.PLLSF bit is set to 1 before using the PLL clock. A fixed stabilization wait is required after setting the PLL to start operation. A fixed wait time for the oscillation to stop is also required after stopping the PLL operation.

The following restrictions apply when starting and stopping the PLL operation:

- After stopping the PLL, confirm that the OSCSF.PLLSF bit is 0 before restarting the PLL
- Confirm that the PLL operates and that the OSCSF.PLLSF bit is 1 before stopping the PLL
- Regardless of whether the PLL clock is selected as the system clock, after setting the PLL to start operation, confirm that the OSCSF.PLLSF is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the PLL, confirm that the OSCSF.PLLSF bit is set to 0 before executing the WFI instruction.

Writing 1 to PLLSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL).

Make sure the following conditions apply before writing 0 to PLLSTP:

- When PLL source clock = MOSC, OSCSF.MOSCSF bit is 1
- When PLL source clock = HOCO, OSCSF.HOCOSF bit is 1.

9.2.5 Main Clock Oscillator Control Register (MOSCCR)

Address(es): SYSTEM.MOSCCR 4001 E032h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	MOSTP	Main Clock Oscillator Stop	0: Operate the main clock oscillator*1 1: Stop the main clock oscillator.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The MOMCR register must be set before setting MOSTP to 0.

The MOSCCR register controls the main clock oscillator.

MOSTP bit (Main Clock Oscillator Stop)

The MOSTP bit starts or stops the main clock oscillator. To start the main clock oscillator, set this bit to 0. When changing the value of this bit, only execute subsequent instructions after reading the bit to check that its value is updated.

When using the main clock oscillator, you must set the Main Clock Oscillator Mode Oscillation Control Register (MOMCR) and the Main Clock Oscillator Wait Control Register (MOSCWTCR) before setting MOSTP to 0.

After setting the MOSTP bit to 0, confirm that the OSCSF.MOSCSF bit is set to 1 before using the main clock oscillator. A fixed stabilization wait is required after setting the main clock oscillator to start operation. A fixed wait time for the oscillation to stop is also required after stopping the main clock oscillator.

The following restrictions apply when starting and stopping the main clock oscillator operation:

- After stopping the main clock oscillator, confirm that the OSCSF.MOSCSF bit is 0 before restarting the main clock oscillator
- Confirm that the main clock oscillator operates and that the OSCSF.MOSCSF bit is 1 before stopping the main clock oscillator
- Regardless of whether the main clock oscillator is selected as the system clock, confirm that the OSCSF.MOSCSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the main clock oscillator, confirm that the OSCSF.MOSCSF bit is set to 0 before executing the WFI instruction.

Writing 1 to MOSTP is prohibited under the following conditions:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC)
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and PLLCR.PLLSTP = 0 (PLL is operating).

9.2.6 Subclock Oscillator Control Register (SOSCCR)

Address(es): SYSTEM.SOSCCR 4001 E480h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SOSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SOSTP	Sub-Clock Oscillator Stop	0: Operate the sub-clock oscillator*1 1: Stop the sub-clock oscillator.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The SOMCR register must be set before setting SOSTP to 0.

The SOSCCR register controls the sub-clock oscillator.

SOSTP bit (Sub-Clock Oscillator Stop)

The SOSTP bit starts or stops the sub-clock oscillator.

When changing the value of the SOSTP bit, only execute subsequent instructions after reading the bit and checking that its value is updated. Use the SOSTP bit when using the sub-clock oscillator as the source for a peripheral module.

When using the sub-clock oscillator, you must set the Sub-Clock Oscillator Mode Control Register (SOMCR) before setting SOSTP to 0.

After setting SOSTP to 0, only use the sub-clock oscillator after the sub-clock oscillation stabilization wait time (tSUBOSCOWT) elapses. A fixed stabilization wait is required after setting the sub-clock oscillator to start operation. A fixed wait time for the oscillation to stop is also required after setting the SOSTP bit.

The following restrictions apply when starting and stopping operation:

- After stopping the sub-clock oscillator, allow a stop interval of at least 5 SOSC clock cycles before restarting it
- Confirm that sub-clock oscillation is stable before stopping the sub-clock oscillator
- Regardless of whether the sub-clock oscillator is selected as the system clock, confirm that the sub-clock oscillation is stable before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the sub-clock oscillator, wait for at least 3 SOSC clock cycles before executing the WFI instruction.

Writing 1 to SOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 100b (system clock source = SOSC).

9.2.7 Low-Speed On-Chip Oscillator Control Register (LOCOCR)

Address(es): SYSTEM.LOCOCR 4001 E490h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	LCSTP	LOCO Stop	0: Operate the LOCO clock 1: Stop the LOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The LOCOCR register controls the LOCO clock.

LCSTP bit (LOCO Stop)

The LCSTP bit starts or stops the LOCO clock.

After setting the LCSTP bit to 0 to start the LOCO clock, only use the clock after the LOCO clock oscillation stabilization wait time (tLOCOWT) elapses. A fixed stabilization wait is required after setting the LOCO clock to start operation. A fixed wait time for the oscillation to stop is also required.

The following restrictions apply when starting and stopping operation:

- After stopping the LOCO clock, allow a stop interval of at least 5 LOCO clock cycles before restarting it
- Confirm that LOCO oscillation is stable before stopping the LOCO clock
- Regardless of whether the LOCO clock is selected as the system clock, confirm that LOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the LOCO clock, wait for at least 3 LOCO clock cycles before executing the WFI instruction.

Writing 1 to LOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 010b (system clock source = LOCO).

Because the LOCO clock measures the wait time for other oscillators, it continues to oscillate while measuring this time, regardless of the setting in LOCOCR.LCSTP. As a result, the LOCO clock might be unintentionally supplied even when the LCSTP is set to stop.

9.2.8 High-Speed On-Chip Oscillator Control Register (HOCOCR)

Address(es): SYSTEM.HOCOCR 4001 E036h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	HCSTP
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit name	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. If you use the HOCO (HCSTP = 0), you must set the OFS1.HOCOFRQ1 bit to an optimum value.

The HOCOCR register controls the HOCO clock.

HCSTP bit (HOCO Stop)

The HCSTP bit starts or stops the HOCO clock.

After setting the HCSTP bit to 0 to start the HOCO clock, confirm that the OSCSF.HOSCSF bit is set to 1 before using the clock. A fixed stabilization wait is required after setting the HOCO clock to start operation. A fixed wait time for oscillation to stop is also required. For the HOCO to operate, the HOCO Wait Control Register (HOCOWTCR) must also be set.

The following restrictions apply when starting and stopping operation:

- After stopping the HOCO, confirm that the OSCSF.HOCOSF bit is 0 before restarting the HOCO clock
- Confirm that the HOCO clock operates and that the OSCSF.HOCOSF bit is 1 before stopping the HOCO clock
- Regardless of whether the HOCO clock is selected as the system clock, confirm that the OSCSF.HOSCSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the HOCO clock, confirm that the OSCSF.MOSCSF bit is set to 0, before executing the WFI instruction.

Writing 1 to HCSTP is prohibited under the following conditions:

- SCKSCR.CKSEL[2:0] = 000b (system clock source = HOCO)
- PLLCCR.PLSRCSEL = 1 (PLL source clock = HOCO) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
- PLLCCR.PLSRCSEL = 1 (PLL source clock = HOCO) and PLLCR.PLLSTP = 0 (PLL is operating).

9.2.9 High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR)

Address(es): SYSTEM.HOCOWTCR 4001 E0A5h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HSTS[2:0]		
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	HSTS[2:0]	HOCO Wait Time Setting	Wait time (s) = (HSTS[2:0] setting +3) / fLOCO	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R

HSTS[2:0] bits (HOCO Wait Time Setting)

The HSTS[2:0] bits must be set to 110b, except when using SCI0 in Snooze mode. When using SCI0 in Snooze mode, these bits must be set to 010b.

9.2.10 Middle-Speed On-Chip Oscillator Control Register (MOCOCR)

Address(es): SYSTEM.MOCOCR 4001 E038h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MCSTP	MOCO Stop	0: Operate the MOCO clock 1: Stop the MOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The MOCOCR register controls the MOCO clock.

MCSTP bit (MOCO Stop)

The MCSTP bit starts or stops the MOCO clock.

After setting the MCSTP bit to 0 to start the MOCO clock, only use the clock after the MOCO clock oscillation stabilization time (tMOCOWT) elapses. A fixed stabilization wait is required after setting the MOCO clock to start operation. A fixed wait time for oscillation to stop is also required after setting MCSTP to 1.

The following restrictions apply when starting and stopping operation:

- After stopping the MOCO clock, allow a stop interval of at least 5 MOCO clock cycles before restarting it
- Confirm that MOCO oscillation is stable before stopping the MOCO clock
- Regardless of whether the MOCO clock is selected as the system clock, confirm that MOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the MOCO clock, wait for at least 3 MOCO clock cycles before executing the WFI instruction.

Writing 1 to MCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 001b (system clock source = MOCO).

Writing 1 to the MCSTP bit (stopping the MOCO) is prohibited if oscillation stop detection is enabled in the Oscillation Stop Detection Enable bit (OSTDCR.OSTDE) in the Oscillation Stop Detection Control Register.

9.2.11 FLL Control Register 1 (FLLCR1)

Address(es): SYSTEM.FLLCR1 4001 E039h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FLLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FLLEN	FLL Enable	0: FLL function is disabled 1: FLL function is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: HOCO must be stopped (HOCOCR.HCSTP = 1) before FLLCR1.FLLEN is changed.
SOSC must operate with stabilization while FLL is enabled (FLLCR1.FLLEN = 1).

The FLLCR1 register controls the FLL function of the HOCO. The FLL function uses SOSC when available for better accuracy in HOCO.

FLLEN bit (FLL Enable)

The FLLEN bit enables or disables the FLL function of the HOCO.

If the FLL function is enabled, the frequency accuracy is guaranteed after the FLL is stabilized. The FLL stabilization can be checked by the frequency measurement of the Clock Frequency Accuracy Measurement Circuit (CAC) after the HOCO is stabilized.

The FLL function must be disabled by setting the FLLEN bit to 0 before transitioning to Software Standby mode.

Figure 9.4 and Figure 9.5 show an example flow of the FLL setting in each case.

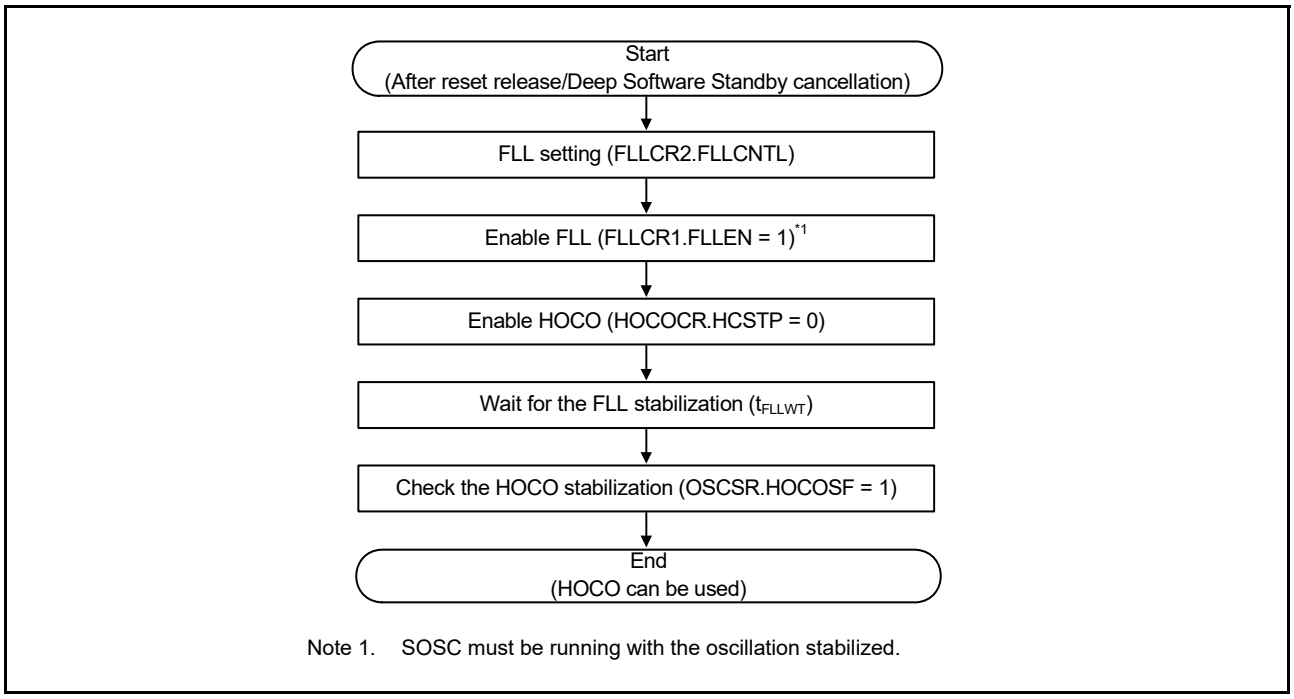
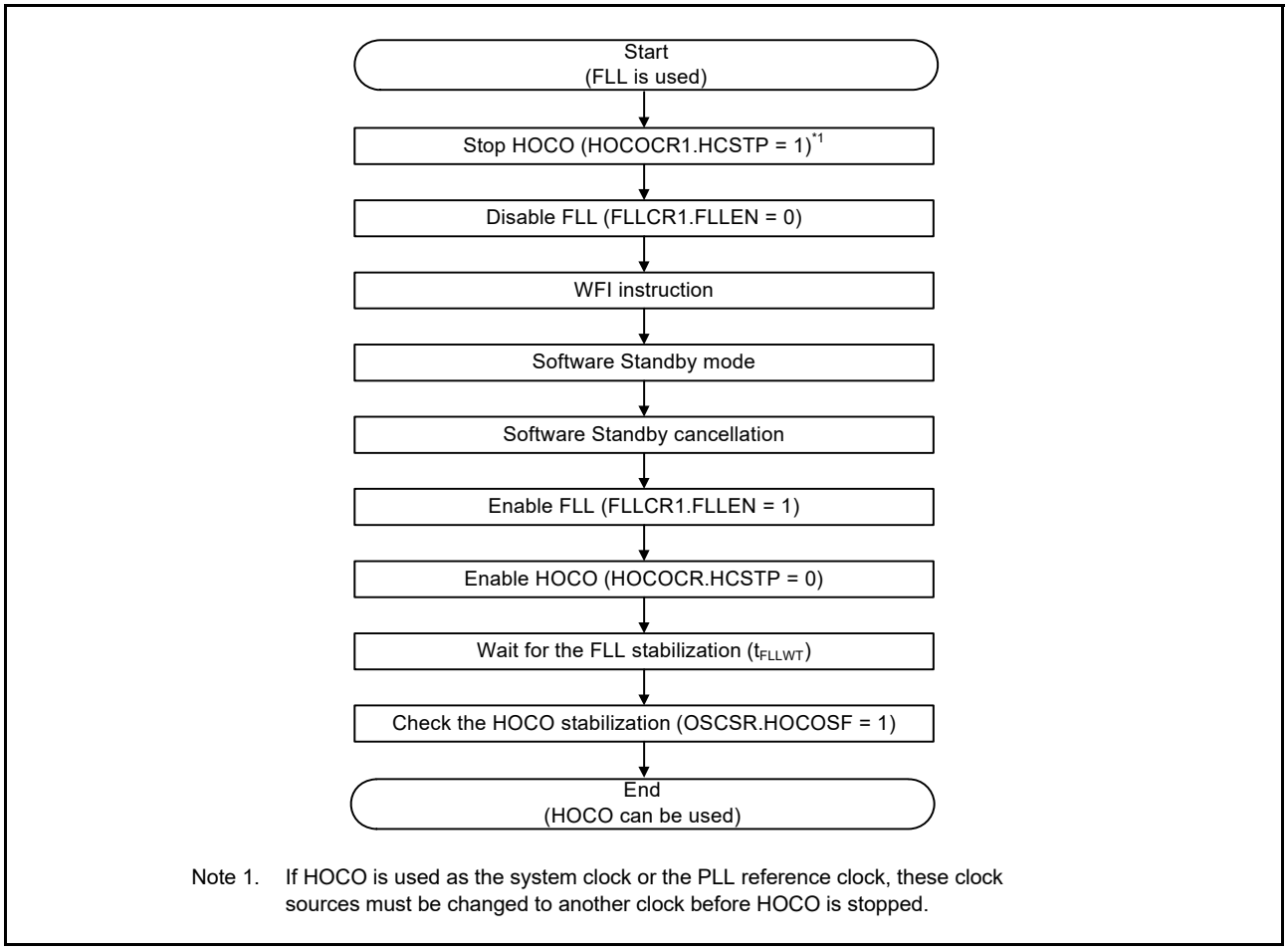


Figure 9.4 FLL setting flow after reset release/Deep Software Standby cancellation



Note 1. If HOCO is used as the system clock or the PLL reference clock, these clock sources must be changed to another clock before HOCO is stopped.

Figure 9.5 Software Standby transition/cancellation flow

9.2.12 FLL Control Register 2 (FLLCR2)

Address(es): SYSTEM.FLLCR2.4001 E03Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	FLLCNTL[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	FLLCNTL[10:0]	FLL Multiplication Control	• When OFS1.HOCOFRQ0[1:0] is 00b (16 MHz), these bits must be set to 1E9h • When OFS1.HOCOFRQ0[1:0] is 01b (18 MHz), these bits must be set to 226h • When OFS1.HOCOFRQ0[1:0] is 10b (20 MHz), these bits must be set to 263h. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The FLLCR2 register controls the FLL function of the HOCO.

FLLCNTL[10:0] bits (FLL Multiplication Control)

The FLLCNTL[10:0] bits select the multiplication ratio of the FLL reference clock. These bits must be set before FLL is enabled (FLLCR1.FLLEN = 1).

9.2.13 Oscillation Stabilization Flag Register (OSCSF)

Address(es): SYSTEM.OSCSF 4001 E03Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PLLSF	—	MOSCSF	—	—	HOCOSF
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit name	Description	R/W
b0	HOCOSF	HOCO Clock Oscillation Stabilization Flag	0: The HOCO clock is stopped or is not yet stable 1: The HOCO clock is stable, and is available for use as the system clock.	R
b2, b1	—	Reserved	These bits are read as 0.	R
b3	MOSCSF	Main Clock Oscillation Stabilization Flag	0: The main clock oscillator is stopped (MOSTP = 1) or is not yet stable*2 1: The main clock oscillator is stable, and is available for use as the system clock.	R
b4	—	Reserved	This bit is read as 0.	R
b5	PLLSF	PLL Clock Oscillation Stabilization Flag	0: The PLL clock is stopped or is not yet stable 1: The PLL clock is stable, and is available for use as the system clock.	R
b7, b6	—	Reserved	These bits are read as 0	R

Note 1. The value after reset depends on the OFS1.HOCOEN setting.
When OFS1.HOCOEN = 1, the HOCOSF value after reset is 0.
When OFS1.HOCOEN = 0, the HOCOSF value becomes 0 after reset is released, and HOCOSF is set to 1 after the HOCO oscillation stabilization wait time elapses.

Note 2. An appropriate value is set in the Wait Control Register for the given oscillator. If the wait time value is not sufficient, the oscillation stabilization flag is set to 1 and supply of the clock signal to the internal circuits starts before oscillation is stable.

The OSCSF register contains flags to indicate the operating status of the counters in the oscillation stabilization wait circuits for the individual oscillators.

After oscillation starts, these counters measure the wait time until each oscillator output clock is supplied to the internal circuits. An overflow of a counter indicates that the clock supply is stable and available for the associated circuit.

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

The HOCOSF flag indicates the operating status of the counter that measures the wait time for the HOCO. Confirm that the OSCSF.HOCOSF is set to 1 before using the HOCO clock.

[Setting condition]

- After the HOCO clock stops and the HOCOCR.HCSTP bit is set to 0, supply of the MCU clock starts after the number of LOCO cycles associated with the HOCOWTCR register setting elapses.

[Clearing condition]

- When the HOCO clock is operating and then is deactivated because the HOCOCR.HCSTP bit is set to 1.

MOSCSF flag (Main Clock Oscillation Stabilization Flag)

The MOSCSF flag indicates the operating status of the counter that measures the wait time for the main clock oscillator.

[Setting condition]

- After the main clock oscillator stops and the MOSCCR.MOSTP bit is set to 0, supply of the MCU clock starts after the number of LOCO cycles associated with the MOSCWTCR register setting elapses.

[Clearing condition]

- When the main clock oscillator is operating and then is deactivated because the MOSCCR.MOSTP bit is set to 1.

PLLSF flag (PLL Clock Oscillation Stabilization Flag)

The PLLSF flag indicates the operating status of the counter that measures the wait time for the PLL.

[Setting condition]

- After the PLL stops and the PLLCR.PLLSTP bit is set to 0, supply of the MCU clock starts after 31 LOCO cycles. If oscillation by the PLL clock source selected in the PLLCCR.PLSRCSEL bit is not stable when the PLLSTP bit is set to 0, counting of the LOCO cycles continues after the PLL clock source oscillation is stabilized. Wait time is calculated as:

  1 cycle = LOCO (32.768 kHz) x 8 (3.81 µs typical).

[Clearing condition]

- When the PLL is operating and then is deactivated because the PLLCCR.PLLSTP bit is set to 1.

9.2.14 Oscillation Stop Detection Control Register (OSTDCR)

Address(es): SYSTEM.OSTDCR 4001 E040h

	b7	b6	b5	b4	b3	b2	b1	b0
	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OSTDIE	Oscillation Stop Detection Interrupt Enable	0: Disable oscillation stop detection interrupt (do not notify the POEG) 1: Enable oscillation stop detection interrupt (notify the POEG).	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OSTDE	Oscillation Stop Detection Function Enable	0: Disable oscillation stop detection function 1: Enable oscillation stop detection function.	R/W

The OSTDCR register controls the oscillation stop detection function.

OSTDIE bit (Oscillation Stop Detection Interrupt Enable)

The OSTDIE bit enables the oscillation stop detection function interrupt. This bit also controls whether oscillation stop detection is reported to the POEG.

If the Oscillation Stop Detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) requires clearing, set the OSTDIE bit to 0 before clearing OSTDF. Wait for at least 2 PCLKB cycles before setting the OSTDIE bit to 1. A longer PCLKB wait time might be required, depending on the number of cycles required to read a given I/O register.

OSTDE bit (Oscillation Stop Detection Function Enable)

The OSTDE bit enables the oscillation stop detection function.

When the OSTDE bit is 1 (enabled), the MOCO stop bit (MOCOCR.MCSTP) is set to 0 and MOCO operation starts. The MOCO clock cannot be stopped when the oscillation stop detection function is enabled. Writing 1 to the MOCOCR.MCSTP bit (MOCO stopped) is invalid.

When the Oscillation Stop Detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) is 1 (main clock oscillation stop detected), writing 0 to the OSTDE bit is invalid.

The OSTDE bit must be set to 0 before transitioning to Software Standby or Deep Software Standby mode. To transition to either of these modes, first set the OSTDE bit to 0, then execute the WFI instruction.

The following restrictions apply when using the oscillation stop detection function:

- In low-speed mode, selecting division by 1, 2, 4, 8 for ICLK, FCLK, PCLKA, PCLKB, PCLKC, PCLKD is prohibited.

9.2.15 Oscillation Stop Detection Status Register (OSTDSR)

Address(es): SYSTEM.OSTDSR 4001 E041h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OSTDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OSTDF	Oscillation Stop Detection Flag	0: Main clock oscillation stop not detected 1: Main clock oscillation stop detected.	R(/W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit can only be set to 0.

The OSTDSR register indicates the stop detection status of the main clock oscillator.

OSTDF flag (Oscillation Stop Detection Flag)

The OSTDF flag indicates the main clock oscillator status. When this flag is 1, it indicates that the main clock oscillation stop was detected. After this stop is detected, the OSTDF flag is not set to 0 even when the main clock oscillation is restarted. The OSTDF flag is set to 0 by writing 0 after reading it as 1.

At least 3 ICLK cycles of wait time are required between writing 0 to OSTDF and reading it as 0. If the OSTDF flag is set to 0 when the main clock oscillation is stopped, the OSTDF flag becomes 0 then returns to 1.

The OSTDF flag cannot be set to 0 under the following conditions:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC)
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL).

The OSTDF flag must be set to 0 after switching the clock source to sources other than the main clock oscillator and PLL.

[Setting condition]

- The main clock oscillator is stopped when OSTDCR.OSTDE = 1 (oscillation stop detection function enabled).

[Clearing condition]

- 1 is read and then 0 is written when the SCKSCR.CKSEL[2:0] bits are neither 011b (system clock = MOSC) nor 101b (system clock = PLL), and the PLLCCR.PLSRCSEL bit is not 0 (PLL source clock = MOSC).

9.2.16 Main Clock Oscillator Wait Control Register (MOSCWTCR)

Address(es): SYSTEM.MOSCWTCR 4001 E0A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MSTS[3:0]			
Value after reset:	0	0	0	0	0	1	0	1

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MSTS[3:0]	Main Clock Oscillator Wait Time Setting	When drive capability automatic switching function is disabled (MOMCR.AUTODRVEN = 0 [default]): b3 b0 0 0 0 1: Wait time = 35 cycles (133.5 µs) 0 0 1 0: Wait time = 67 cycles (255.6 µs) 0 0 1 1: Wait time = 131 cycles (499.7 µs) 0 1 0 0: Wait time = 259 cycles (988.0 µs) 0 1 0 1: Wait time = 547 cycles (2086.6 µs) (value after reset) 0 1 1 0: Wait time = 1059 cycles (4039.8 µs) 0 1 1 1: Wait time = 2147 cycles (8190.2 µs) 1 0 0 0: Wait time = 4291 cycles (16368.9 µs) 1 0 0 1: Wait time = 8163 cycles (31139.4 µs). When drive capability automatic switching function is enabled (MOMCR.AUTODRVEN = 1): b3 b0 0 0 0 1: Wait time = 36 cycles (137.3 µs) 0 0 1 0: Wait time = 68 cycles (259.4 µs) 0 0 1 1: Wait time = 132 cycles (503.5 µs) 0 1 0 0: Wait time = 260 cycles (991.8 µs) 0 1 0 1: Wait time = 548 cycles (2090.5 µs) (value after reset) 0 1 1 0: Wait time = 1060 cycles (4043.6 µs) 0 1 1 1: Wait time = 2148 cycles (8194.0 µs) 1 0 0 0: Wait time = 4292 cycles (16372.7 µs) 1 0 0 1: Wait time = 8164 cycles (31143.2 µs). Other settings are prohibited. Wait time is calculated as: 1 cycle (µs) = 1 / (f_LOCO [MHz] × 8) = 1 / (0.032768 × 8) = 3.81 µs	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

MSTS[3:0] bits (Main Clock Oscillator Wait Time Setting)

The MSTS[3:0] bits specify the oscillation stabilization wait time for the main clock oscillator.

Set the main clock oscillation stabilization time to a period longer than or equal to the stabilization time recommended by the oscillator manufacturer. When the main clock is input externally, set these bits to 0001b, because the oscillation stabilization time is not required.

The wait time set in the MSTS[3:0] bits is counted using:

1 cycle (µs) = 1 / (f_ LOCO [MHz] × 8) = 1 / (0.032768 × 8) = 3.81 (µs).

The LOCO clock automatically oscillates when necessary, regardless of the LOCOCR.LOSTP bit value. After the specified wait time elapses, supply of the main clock oscillator starts internally in the MCU, and the OSCSF.MOSCSF flag is set to 1. If the specified wait time is short, supply of the main clock oscillator starts before oscillation of the clock becomes stable.

Only rewrite the MOSCWTCR register when the MOSCCR.MOSTP bit is 1 and the OSCSF.MOSCSF flag is 0. Do not rewrite this register under any other conditions.

9.2.17 Main Clock Oscillator Mode Oscillation Control Register (MOMCR)

Address(es): SYSTEM.MOMCR 4001 E413h

	b7	b6	b5	b4	b3	b2	b1	b0
	AUTODRVEN	MOSEL	MODRV0[1:0]		—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	MODRV0[1:0]	Main Clock Oscillator Drive Capability 0 Switching	b5 b4 0 0: 20 MHz to 24 MHz 0 1: 16 MHz to 20 MHz 1 0: 8 MHz to 16 MHz 1 1: 8 MHz.	R/W
b6	MOSEL	Main Clock Oscillator Switching	0: Resonator 1: External clock input.	R/W
b7	AUTODRVEN	Main Clock Oscillator Drive Capability Auto Switching Enable	0: Disable 1: Enable.	R/W

Note: The EXTAL/XTAL pin is also used as a port. In the initial state, the port function is selected.
Note: The MOSTP bit must be 1 (MOSC = stopped) before changing this register.

MODRV0[1:0] bits (Main Clock Oscillator Drive Capability 0 Switching)

The MODRV0[1:0] bits switch the drive capability of the main clock oscillator.

MOSEL bit (Main Clock Oscillator Switching)

The MOSEL bit switches the source for the main clock oscillator.

AUTODRVEN bit (Main Clock Oscillator Drive Capability Auto Switching Enable)

The AUTODRVEN bit controls the drive capability auto switching of the main clock oscillator.

When the AUTODRVEN bit is 1, after the time set in the MSTS bits in the Main Clock Oscillator Wait Control Register elapses, the drive capability of the main clock oscillator is automatically set to the lowest, regardless of the MOMCR.MODRV0[1:0] setting. The main clock oscillator restarts oscillation with MODRV0[1:0] bits set to switch the drive capability after oscillation stops by the MOSCCR.MOSTP setting or by entering Software Standby mode.

9.2.18 Subclock Oscillator Mode Control Register (SOMCR)

Address(es): SYSTEM.SOMCR 4001 E481h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	SODRV1	—
Value after reset:	0	0	0	0	0	0	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	SODRV1	Sub-Clock Oscillator Drive Capability Switching	0: Standard 1: Low.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: The SOSCCR.SOSTP bit must be 1 (SOSC = stopped) before changing this register.

SODRV1 bit (Sub-Clock Oscillator Drive Capability Switching)

The SODRV1 bit switches the drive capability of the sub-clock oscillator. This bit is undefined at the first power on, but the value after reset of SOSCCR.SOSTP is 0 (SOSC = operating). Set up the SOSC as follows at the first power on:

1. Set the SOSCCR.SOSTP bit to 1 (SOSC = stopped).
2. Set the SODRV1 bit to the correct value for the current capacitor.
3. Set the SOSCCR.SOSTP bit to 0 (SOSC = operating).

9.2.19 Clock Out Control Register (CKOCR)

Address(es): SYSTEM.CKOCR 4001 E03Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKOSEL[2:0]	Clock Out Source Select	b2 b0 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: MOSC 1 0 0: SOSC. Other settings are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	CKODIV[2:0]	Clock Out Input Frequency Division Select	b6 b4 0 0 0: ×1 0 0 1: /2 0 1 0: /4 0 1 1: /8 1 0 0: /16 1 0 1: /32 1 1 0: /64 1 1 1: /128.	R/W
b7	CKOEN	Clock Out Enable	0: Disable clock out 1: Enable clock out.	R/W

CKOSEL[2:0] bits (Clock Out Source Select)

The CKOSEL[2:0] bits specify the HOCO, MOCO, LOCO, MOSC, or SOSC clock as the source of the clock to be output from the CLKOUT pin. When changing the CLKOUT source clock, set the CKOEN bit to 0.

CKODIV[2:0] bits (Clock Out Input Frequency Division Select)

The CKODIV[2:0] bits specify the clock division ratio. Set the CKOEN bit to 0 when changing the division ratio. The division ratio of the output clock frequency must be set to a value no higher than the characteristics of the CLKOUT pin output frequency. For details on the characteristics of the CLKOUT pin, see section 43, Electrical Characteristics.

CKOEN bit (Clock Out Enable)

The CKOEN bit enables output from the CLKOUT pin. When CKOEN is set to 1, the selected clock is output. When CKOEN is set to 0, low is output. When changing this bit, confirm that the clock out source clock selected in the CKOSEL[2:0] bits is stable. Otherwise, a glitch might be generated in the output.

The CKOEN bit must be cleared before entering Software Standby or Deep Software Standby mode if the selected clock out source clock is stopped in that mode.

9.2.20 LOCO User Trimming Control Register (LOCOUTCR)

Address(es): SYSTEM.LOCOUTCR 4001 E492h

	b7	b6	b5	b4	b3	b2	b1	b0
	LOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	LOCOUTRM[7:0]	LOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127. These bits are added to the original LOCO trimming bits.	R/W

Note: MCU operation is not guaranteed when LOCOUTCR is set to a value that causes the LOCO frequency to be outside of the specification range.

Note: When LOCOUTCR is changed, the time that the frequency is stabilized corresponds to the frequency stabilization time at the start of the MCU operation.

9.2.21 MOCO User Trimming Control Register (MOCOUTCR)

Address(es): SYSTEM.MOCOUTCR 4001 E061h

	b7	b6	b5	b4	b3	b2	b1	b0
	MOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	MOCOUTRM[7:0]	MOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127. These bits are added to the original MOCO trimming bits.	R/W

Note: MCU operation is not guaranteed when MOCOUTCR is set to a value that causes the MOCO frequency to be outside of the specification range.

Note: When MOCOUTCR is changed, the time that the frequency is stabilized corresponds to the frequency stabilization time at the start of the MCU operation.

9.2.22 HOCO User Trimming Control Register (HOCOUTCR)

Address(es): SYSTEM.HOCOUTCR 4001 E062h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	HOCOUTRM[7:0]	HOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127. These bits are added to the original HOCO trimming bits.	R/W

Note: MCU operation is not guaranteed when HOCOUTCR is set to a value that causes the HOCO frequency to be outside of the specification range.
Note: When HOCOUTCR is changed, the time that the frequency is stabilized corresponds to the frequency stabilization time at the start of the MCU operation.
Note: These bits must be 00000000b when FLL is enabled (FLLCR1.FLLEN = 1).

9.2.23 Trace Clock Control Register (TRCKCR)

Address(es): SYSTEM.TRCKCR 4001 E03Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRCKEN	—	—	—	TRCK[3:0]			
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b3 to b0	TRCK[3:0]	Trace Clock Operating Frequency Select	b3 b0 0 0 0 0: /1 0 0 0 1: /2 (value after reset) 0 0 1 0: /4. Other settings are prohibited.	R/W
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TRCKEN	Trace Clock Operation Enable	0: Disable operation 1: Enable operation.	R/W

The Trace Clock Control Register controls the switching of the trace clock. Before changing the TRCLK frequency, set the TRCKEN bit to 0. The TRCKCR register is initialized by all reset sources.

9.3 Main Clock Oscillator

To supply the clock signal to the main clock oscillator, use one of the following ways:

- Connect an oscillator
- Connect the input of an external clock signal.

9.3.1 Connecting the Crystal Resonator

Figure 9.6 shows an example of connecting a crystal resonator. A damping resistor (R_d) can be added, if required. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the manufacturer recommends using an external feedback resistor (R_f), insert an R_f between EXTAL and XTAL by following the instructions.

When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the main clock oscillator as described in Table 9.1.

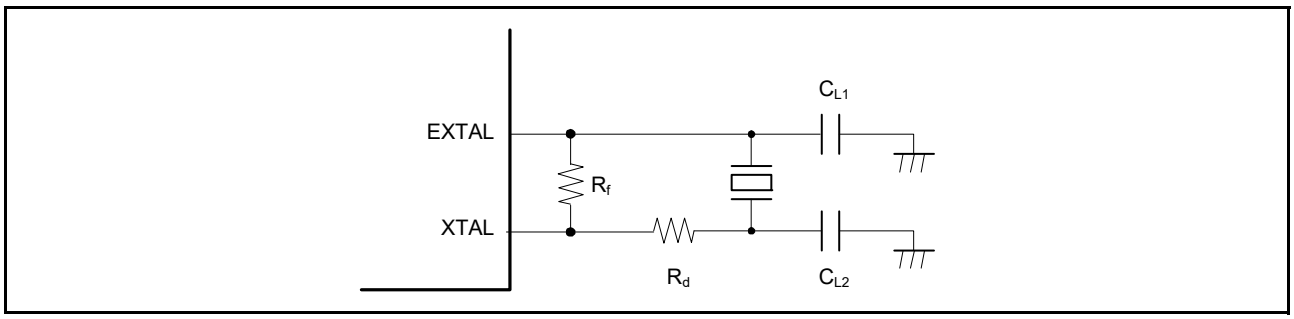


Figure 9.6 Example of crystal resonator connection

Figure 9.7 shows an equivalent circuit of the crystal resonator.

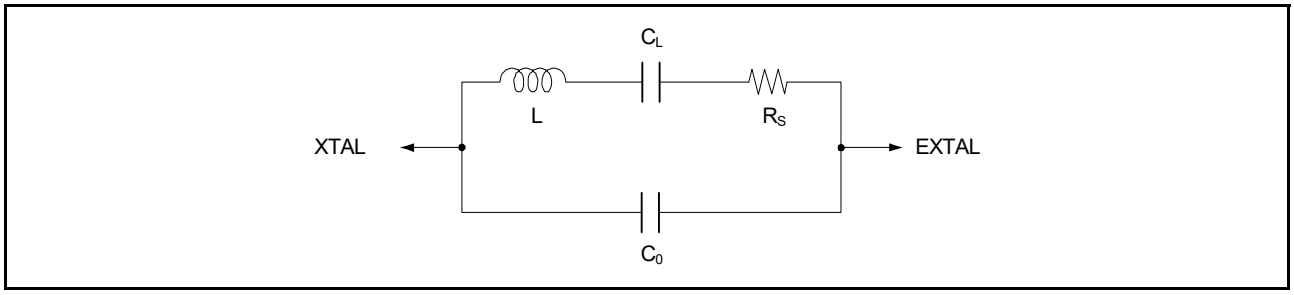


Figure 9.7 Equivalent circuit of the crystal resonator

9.3.2 External Clock Input

Figure 9.8 shows an example for connecting an external clock input. To operate the oscillator with an external clock signal, set the MOMCR.MOSEL bit to 1. The XTAL pin is the function that is set in PFS.P213PFS.

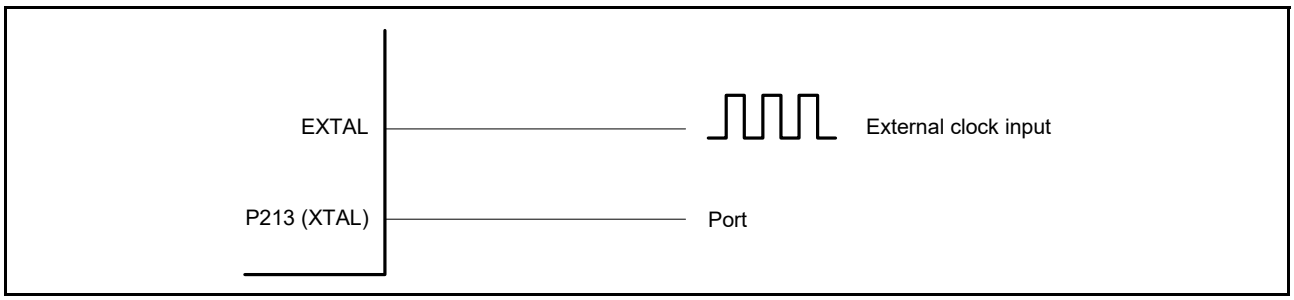


Figure 9.8 Equivalent circuit for external clock

9.3.3 Notes on External Clock Input

The frequency of the external clock input can only be changed when the main clock oscillator is stopped. Do not change the frequency of the external clock input when the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is 0.

9.4 Sub-Clock Oscillator

The only way of supplying a clock signal to the sub-clock oscillator is by connecting a crystal oscillator.

9.4.1 Connecting a 32.768-kHz Crystal Resonator

To supply a clock to the sub-clock oscillator, connect a 32.768-kHz crystal resonator as shown in Figure 9.9. A damping resistor (R_d) can be added, if required. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the manufacturer recommends using an external feedback resistor (R_f), insert an R_f between XCIN and XCOUT by following the instructions.

When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the sub-clock oscillator as described in Table 9.1.

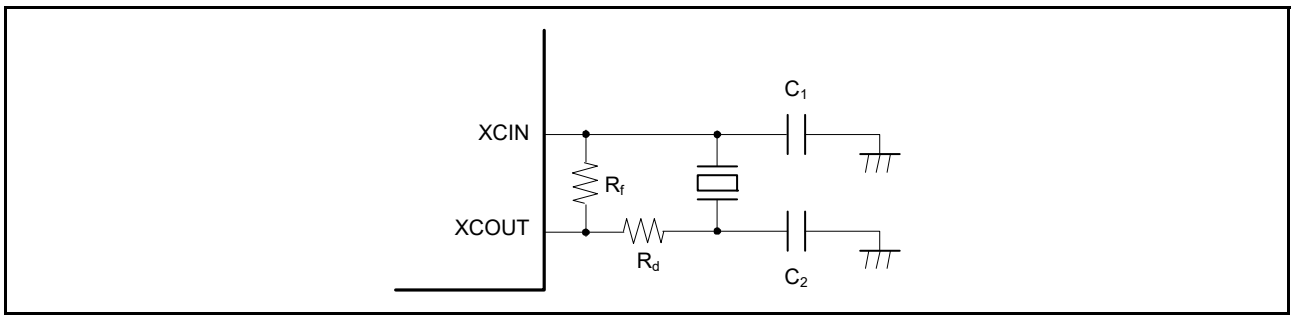


Figure 9.9 Connection example of 32.768-kHz crystal resonator

Figure 9.10 shows an equivalent circuit for the 32.768-kHz crystal resonator.

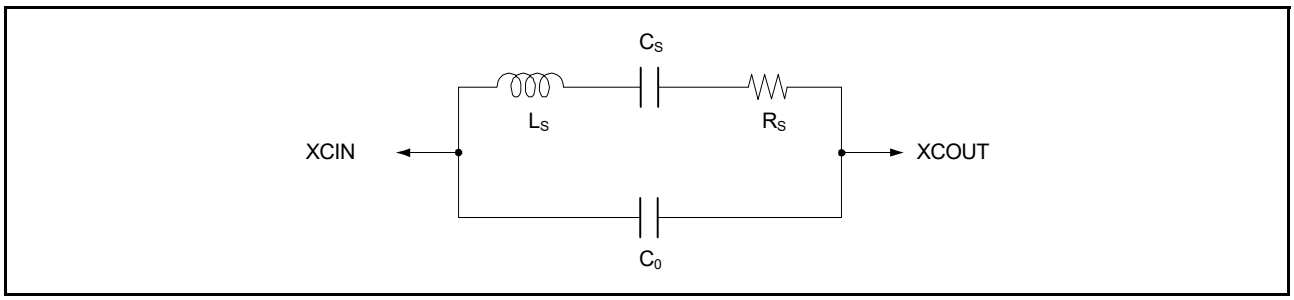


Figure 9.10 Equivalent circuit for the 32.768-kHz crystal resonator

9.4.2 Handling of Pins when the Sub-Clock Oscillator Is Not Used

When the sub-clock oscillator is not in use, connect the XCIN pin to VSS through a resistor (to pull VSS down) and leave the XCOUT pin open as shown in Figure 9.11. In addition, if an oscillator is not connected, set the Sub-clock Oscillator Stop bit (SOSCCR.SOSTP) to 1 to stop the oscillator.

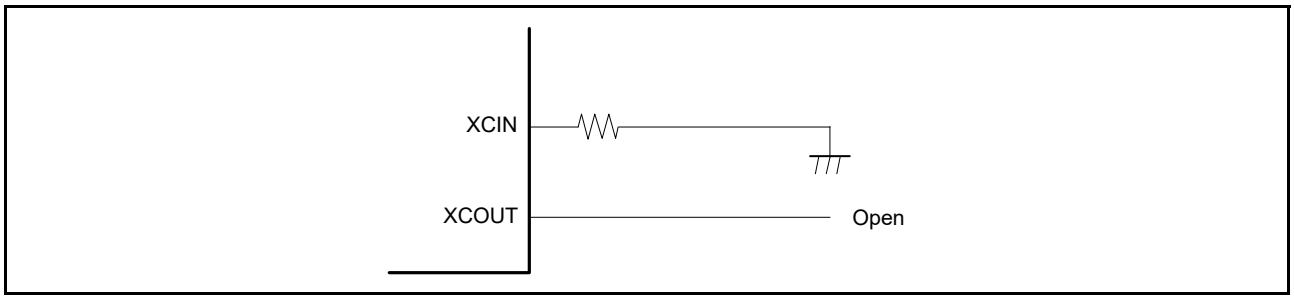


Figure 9.11 Pin handling when the sub-clock oscillator is not used

9.5 Oscillation Stop Detection Function

9.5.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function detects the main clock oscillator stop. When an oscillation stop is detected, the system clock switches as follows:

- If an oscillation stop is detected with SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC), the system clock source switches to the MOCO clock
- If an oscillation stop is detected with PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL), the PLL clock remains as the system clock source. The frequency becomes a free-running oscillation frequency, and the setting of SCKSCR.CKSEL[2:0] bits does not change.

An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the General PWM Timer (GPT) output can be forced to a high-impedance state on detection.

The main clock oscillation stop is detected when the input clock remains at 0 or 1 for a certain period, for example, when a malfunction occurs in the main clock oscillator. See section 43, Electrical Characteristics.

Switching between the main clock oscillator and the MOCO clock or between the PLL clock and the PLL free-running clock is controlled by the Oscillation Stop Detection flag (OSTDSR.OSTDF).

The OSTDF flag controls the switched clock as follows:

- When SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC):
  - When OSTDF changes from 0 to 1, the clock source switches to the MOCO clock
  - When OSTDF changes from 1 to 0, the clock source switches to MOSC again.
- When PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL):
  - When OSTDF changes from 0 to 1, the clock source switches to the PLL free-running oscillation clock
  - When OSTDF changes from 1 to 0, the clock source switches to PLL again.

To switch the clock source to the main clock oscillator or PLL clock again after oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock oscillator or PLL clock, and clear the OSTDF flag to 0. Also, check that the OSTDF flag is not 1, and then set the CKSEL[2:0] bits to the main clock oscillator or PLL clock after the specified oscillation stabilization time elapses.

After a reset release, the main clock oscillator is stopped and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the Oscillation Stop Detection Function Enable bit (OSTDCR.OSTDE) after the specified oscillation stabilization time elapses.

The oscillation stop detection function detects when the main clock oscillator is stopped by an external cause. This means that the oscillation stop detection function must be disabled before the main clock oscillator is stopped by software or before entering Software Standby or Deep Software Standby mode.

The oscillation stop detection function switches the following clocks to the MOCO clock (when the system clock is MOSC) or to the PLL free-running clock (when the system clock is PLL):

- All clocks that can be selected as the MOSC clock or PLL except CLKOUT
- The system clock (ICLK) frequency during MOCO operation (when the system clock is MOSC) or PLL free-running operation (when the system clock is PLL) is specified in the MOCO oscillation frequency and the division ratio set in the System Clock Select bits (SCKDIVCR.ICK[2:0]).

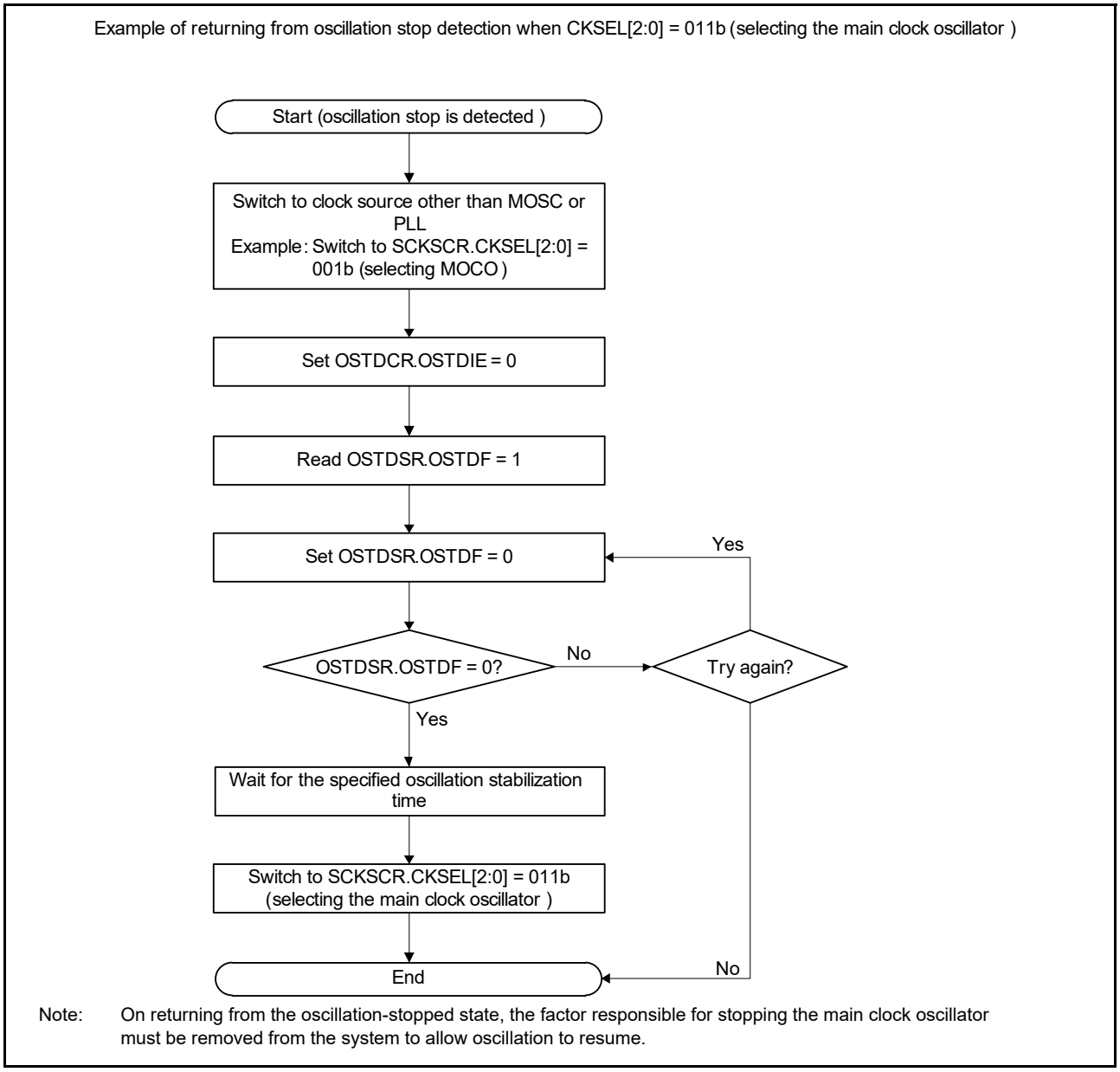


Figure 9.12 Flow of recovery on detection of oscillator stop

9.5.2 Oscillation Stop Detection Interrupts

An oscillation stop detection interrupt (MOSC_STOP) is generated when the Oscillation Stop Detection flag (OSTDSR.OSTDF) is 1 and the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE) is 1 (enabled). The Port Output Enable for GPT (POEG) is notified of the main clock oscillator stop. On receiving the notification, the POEG sets the Oscillation Stop Detection Flag in the POEG Group n Setting Register (POEGGn.OSTPF) to 1 (n = A, B).

After the oscillation stop is detected, wait at least 10 PCLKB cycles before writing to the POEGGn.OSTPF flag. When the OSTDSR.OSTDF flag requires clearing, do so after clearing the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE). Wait for at least 2 PCLKB clock cycles before setting the OSTDCR.OSTDIE bit to 1 again. A longer PCLKB wait time might be required, depending on the number of cycles required to read a given I/O register.

The oscillation stop detection interrupt is a non-maskable interrupt. Because non-maskable interrupts are disabled in the initial state after a reset release, enable non-maskable interrupts through software before using oscillation stop detection interrupts. For details, see section 13, Interrupt Controller Unit (ICU).

9.6 PLL Circuit

The PLL circuit provides a function for multiplying the frequency from the oscillator.

9.7 Internal Clock

Clock sources for the internal clock signals include:

- Main clock oscillator
- Sub-clock oscillator
- HOCO clock
- MOCO clock
- LOCO clock
- PLL clock
- Dedicated clock for the IWDT
- External clock for JTAG.

The following internal clocks are produced from these sources:

- Operating clock for the CPU, DMAC, DTC, flash memory, and SRAM — system clock (ICLK)
- Operating clocks for peripheral modules — PCLKA, PCLKB, PCLKC, and PCLKD
- Operating clock for the flash interface — FCLK
- Operating clock for the CAN — CANMCLK
- Operating clock for the CAC — CACCLK
- Operating clock for the IWDT — IWDTCLK
- Operating clock for the AGT LOCO clock — AGTLCLK
- Operating clock for the AGT sub-clock — AGTSCLK
- Operating clock for the SysTick timer — SYSTICCLK
- Clock for external pin output — CLKOUT
- Operating clock for the JTAG — JTAGTCK.

For details on the registers used to set the frequencies of the internal clocks, see section 9.7.1, System Clock (ICLK) to section 9.7.10, JTAG Clock (JTAGTCK).

If the value of any of these bits is changed, subsequent operation is at the frequency determined by the new value.

9.7.1 System Clock (ICLK)

The system clock, ICLK, is the operating clock for the CPU, DMAC, DTC, flash memory, and SRAM.

The ICLK frequency is specified in the following bits:

- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ[1:0] bits in OFS1.

When the ICLK clock source is switched, the duration of the ICLK clock cycle becomes longer during the clock source transition period. See Figure 9.13 and Figure 9.14.

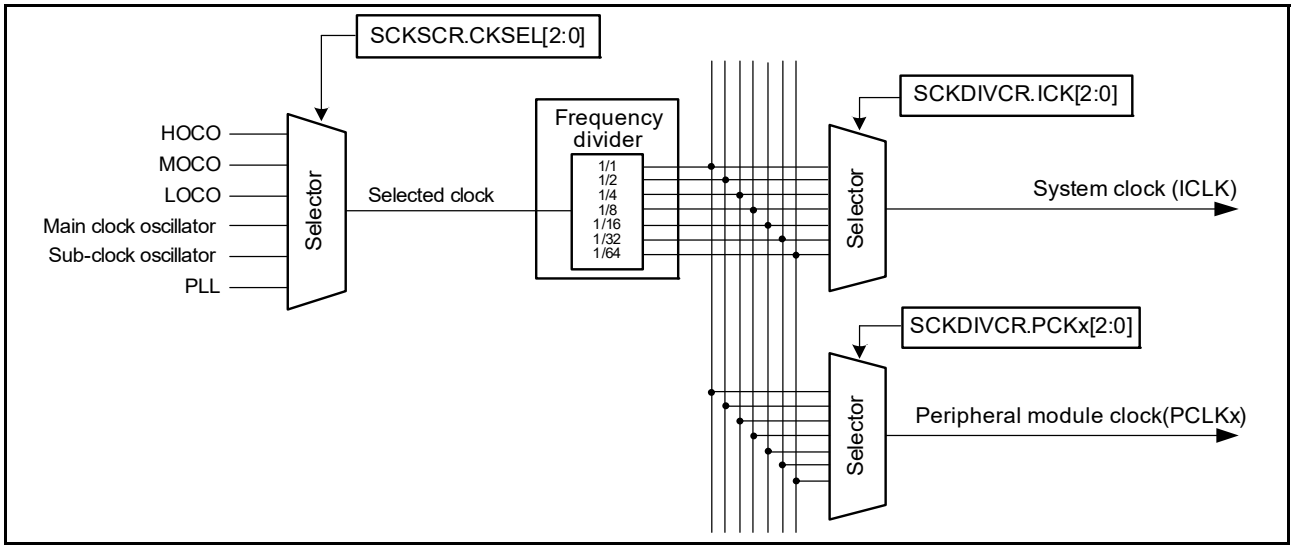


Figure 9.13 Clock source selector block diagram

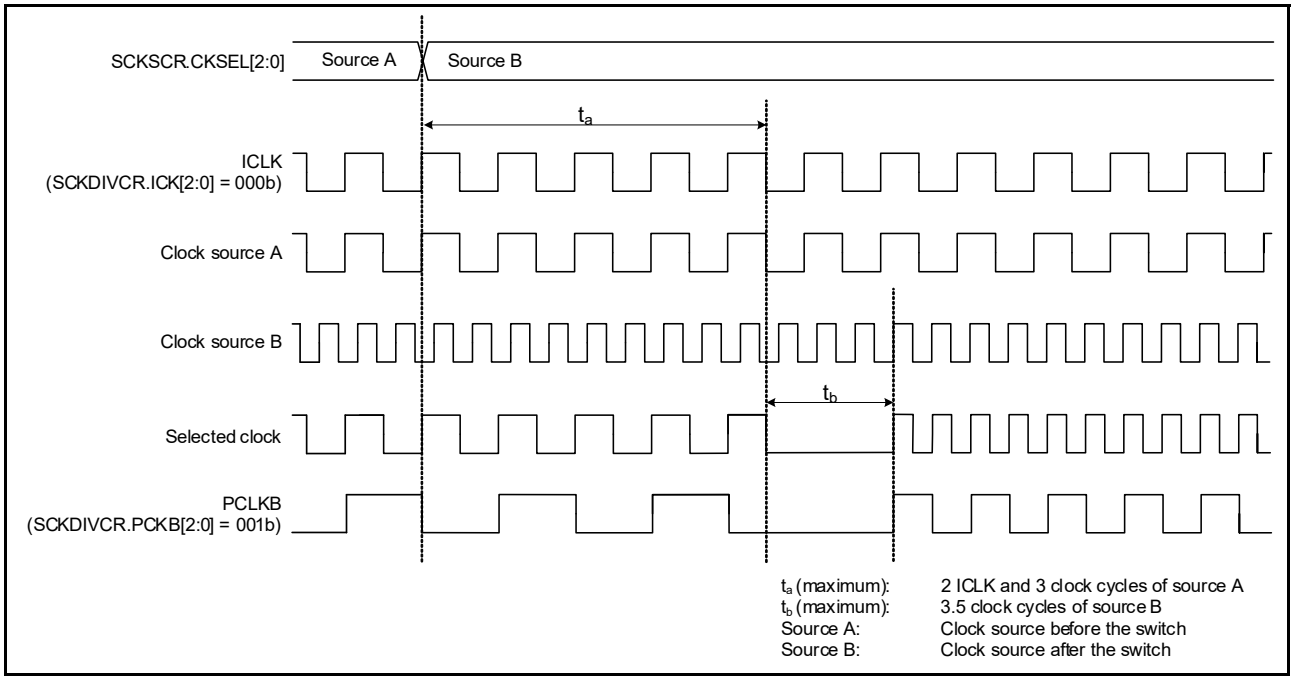


Figure 9.14 Clock source switching timing diagram

9.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

The peripheral module clocks, PCLKA, PCLKB, PCLKC, and PCLKD, are the operating clocks for the peripheral modules.

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ[1:0] bits in OFS1.

When the clock source of the peripheral module clock is switched, the duration of the peripheral module clock cycle becomes longer during the clock source transition period. See Figure 9.13 and Figure 9.14.

9.7.3 Flash Interface Clock (FCLK)

The flash interface clock, FCLK, is the operating clock for the flash memory interface. In addition to reading from the data flash, FCLK is used for the programming and erasure of the code flash and data flash.

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ[1:0] bits in OFS1.

9.7.4 CAN Clock (CANMCLK)

The CAN clock, CANMCLK, is the operating clock for the CAN module. CANMCLK is generated by the main clock oscillator.

9.7.5 CAC Clock (CACCLK)

The CAC clock, CACCLK, is the operating clock for the CAC. CACCLK is generated by the following oscillators:

- Main clock oscillator
- Sub-clock oscillator
- High-speed clock oscillator (HOCO)
- Middle-speed clock oscillator (MOCO)
- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator.

9.7.6 IWDT-Dedicated Clock (IWDTCLK)

The IWDT-dedicated clock, IWDTCLK, is the operating clock for the IWDT. IWDTCLK is internally generated by the IWDT-dedicated on-chip oscillator.

9.7.7 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

The AGT-dedicated clocks, AGTSCLK and AGTLCLK, are the operating clocks for the AGT. AGTSCLK is generated by the sub-clock oscillator and AGTLCLK is generated by the LOCO clock.

9.7.8 SysTick Timer-Dedicated Clock (SYSTICCLK)

The SysTick timer-dedicated clock, SYSTICCLK, is the operating clock for the SYSTICCLK. SYSTICCLK is generated by the LOCO clock.

9.7.9 Clock/Buzzer Output Clock (CLKOUT)

The CLKOUT is output externally from the CLKOUT pin for the clock or buzzer output. CLKOUT is output to the CLKOUT pin when CKOCR.CKOEN is set to 1. Only change the value in the CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR when the CKOCR.CKOEN bit is 0.

The CLKOUT frequency is specified in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR
- HOCOFRQ[1:0] bits in OFS1.

9.7.10 JTAG Clock (JTAGTCK)

The JTAG-dedicated clock, JTAGTCK, is the operating clock for the JTAG. JTAGTCK is generated by the external clock for JTAG (TCK).

9.8 Usage Notes

9.8.1 Notes on Clock Generation Circuit

The frequencies of the system clock (ICLK), peripheral module clock (PCLKA to PCLKD), and flash interface clock (FCLK) supplied to each module change according to the settings in SCKDIVCR. Each frequency must meet the following conditions:

- Each frequency must be selected within the operation-guaranteed range of the clock cycle time (t_{cyc}) specified in the AC electrical characteristics, see section 43, Electrical Characteristics
- The frequencies must not exceed the ranges listed in Table 9.2
- The peripheral modules operate on PCLKB and PCLKA. The operating speed of modules such as the timer and SCI varies before and after the frequency is changed.
- The system clock (ICLK), peripheral module clock (PCLKA to PCLKD), and flash interface clock (FCLK) must be set according to Table 9.2.

To ensure correct processing after the clock frequency changes, first write to the relevant Clock Control Register to change the frequency, then read the value from the register, and finally perform the subsequent processing.

9.8.2 Notes on Resonator

Because various resonator characteristics relate closely to your board design, adequate evaluation is required before use. See the resonator connection example in Figure 9.9. The circuit constants for the resonator depend on the resonator to be used and the stray capacitance of the mounting circuit. Therefore, consult the resonator manufacturer when determining the circuit constants. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

9.8.3 Notes on Board Design

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Route other signal lines away from the oscillation circuit as shown in Figure 9.15, to prevent electromagnetic induction from interfering with correct oscillation.

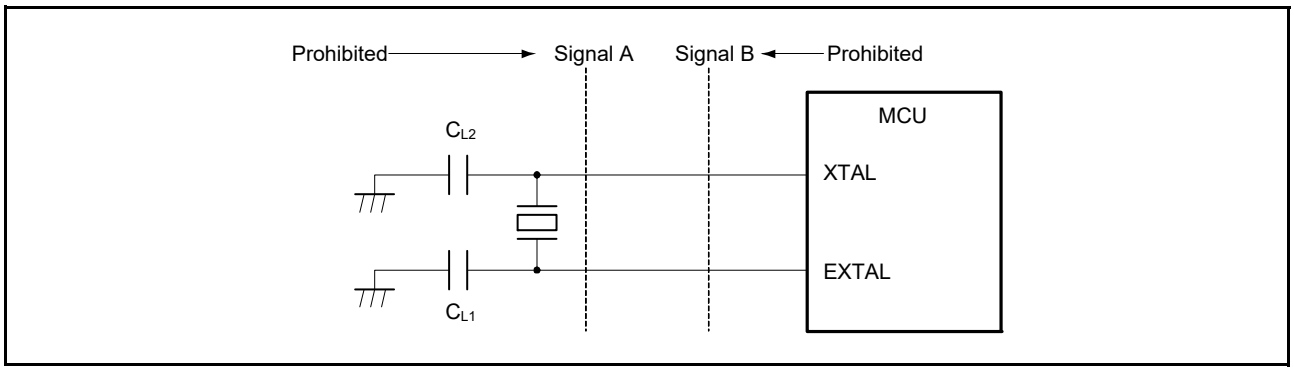


Figure 9.15 Signal routing in board design for oscillation circuit (applies to the sub-clock oscillator for the main clock oscillator)

9.8.4 Notes on the Resonator Connect Pin

When the main clock oscillator is not used, the EXTAL and XTAL pins can be used as general ports P212 and P213. When these pins are used as general ports, the main clock oscillator must be stopped (MOSCCR.MOSTP must be set to 1).

9.8.5 Notes on the Main Clock Oscillator Drive Capability Auto Switching Function

The drive capability of the auto switching function automatically lowers the drive capability of the main clock oscillator, after the main clock oscillator starts and suppresses the associated EMI.

To enable the drive capability of auto switching, set MOMCR.AUTODRVEN to 1 when the main clock oscillator is stopped (MOSCCR.MOSTP = 1). Regardless of the MOMCR.AUTODRVEN setting, the Drive Capability Switching

Register (MOMCR.MODRV0[1:0]) must be set properly according to the selected oscillator. Next, enable the main clock oscillator (MOSCCR.MOSTP = 0). After the Oscillation Stabilization flag (OSCSF.MOSCSF) becomes 1, the main clock can be used.

EMI suppression is gained in return for an extension in the oscillation stabilization wait time. For more information, see section 9.2.16, Main Clock Oscillator Wait Control Register (MOSCWTCR).

10. Clock Frequency Accuracy Measurement Circuit (CAC)

10.1 Overview

The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as a measurement reference (measurement reference clock). It determines the accuracy depending on whether the number of pulses is within the allowable range.

The reference clock can be provided externally through an I/O port pin or internally from various on-chip oscillators. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. This feature is useful in implementing a fail-safe mechanism for home and industrial automation applications.

Table 10.1 lists the CAC specifications, Figure 10.1 shows a block diagram, and Table 10.2 shows the I/O pins.

Table 10.1 CAC specifications

Parameter	Specifications
Measurement target clocks	Frequency can be measured for: • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB).
Measurement reference clocks	Frequency can be referenced to: • External clock input to the CACREF pin • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB).
Selectable function	Digital filter
Interrupt sources	• Measurement end • Frequency error • Overflow.
Module-stop function	Module-stop state can be set to reduce power consumption

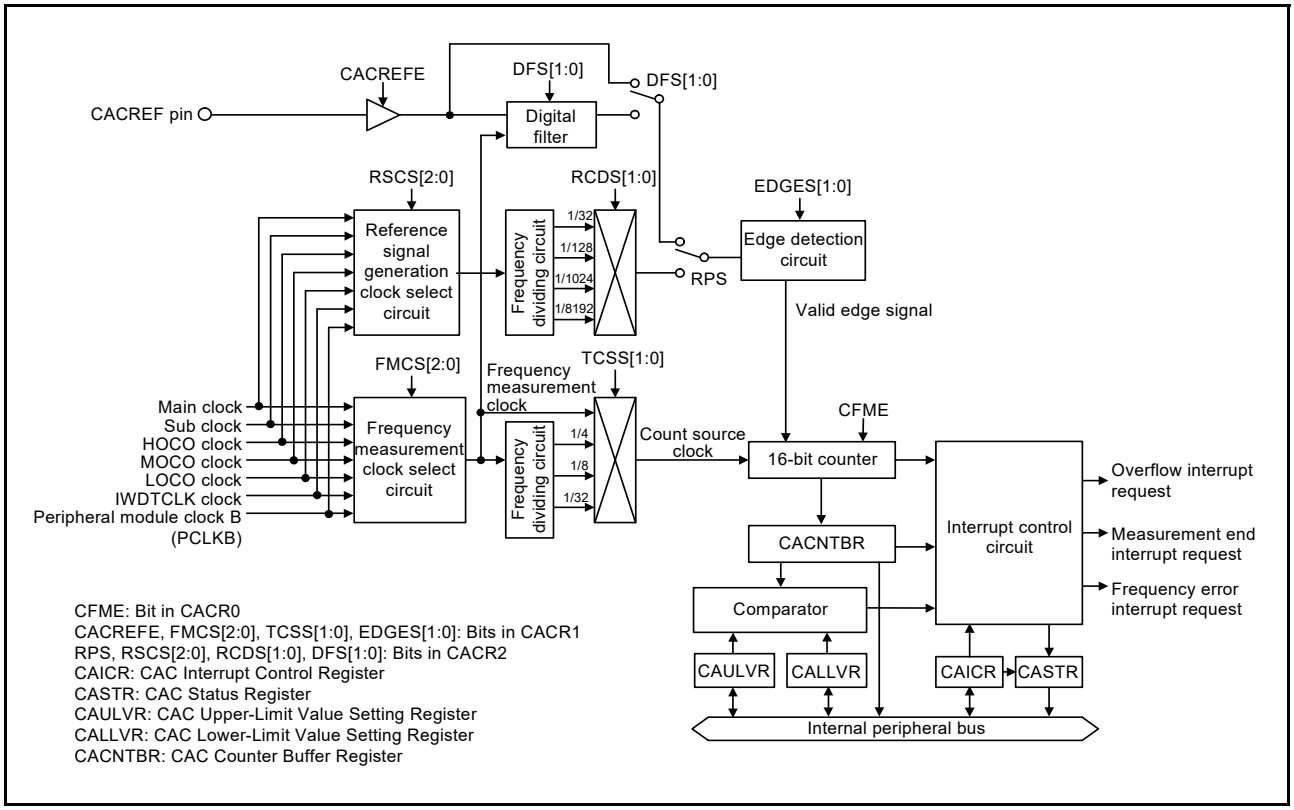


Figure 10.1 CAC block diagram

Table 10.2 CAC I/O pin

Pin name	I/O	Function
CACREF	Input	Measurement reference clock input pin

10.2 Register Descriptions

10.2.1 CAC Control Register 0 (CACR0)

Address(es): CAC.CACR0 4004 4600h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CFME
Value after reset:	0	0	0	0	0	0	0	0

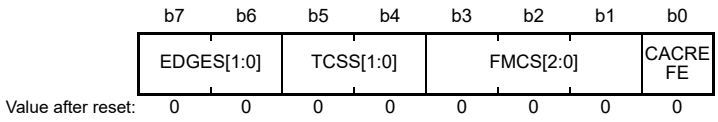
Bit	Symbol	Bit name	Description	R/W
b0	CFME	Clock Frequency Measurement Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CFME bit (Clock Frequency Measurement Enable)

The CFME bit enables the clock frequency measurement. Read the CFME bit to confirm that the bit value has changed. Additional write accesses are ignored before the change is complete.

10.2.2 CAC Control Register 1 (CACR1)

Address(es): CAC.CACR1 4004 4601h



Bit	Symbol	Bit name	Description	R/W
b0	CACREFE	CACREF Pin Input Enable	0: Disable 1: Enable.	R/W
b3 to b1	FMCS[2:0]	Measurement Target Clock Select	b3 b1 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock (PCLKB) 1 1 0: IWDTCLK clock 1 1 1: Setting prohibited.	R/W
b5, b4	TCSS[1:0]	Measurement Target Clock Frequency Division Ratio Select	b5 b4 0 0: No division 0 1: ×1/4 clock 1 0: ×1/8 clock 1 1: ×1/32 clock.	R/W
b7, b6	EDGES[1:0]	Valid Edge Select	b7 b6 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited.	R/W

Note: Set the CACR1 register when the CACR0.CFME bit is 0.

CACREFE bit (CACREF Pin Input Enable)

The CACREFE bit enables the CACREF pin input.

FMCS[2:0] bits (Measurement Target Clock Select)

The FMCS[2:0] bits select the measurement target clock whose frequency is to be measured.

TCSS[1:0] bits (Measurement Target Clock Frequency Division Ratio Select)

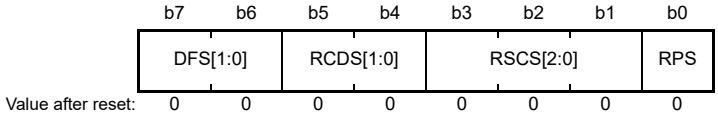
The TCSS[1:0] bits select the division ratio of the measurement target clock.

EDGES[1:0] bits (Valid Edge Select)

The EDGES[1:0] bits select the valid edge for the reference signal.

10.2.3 CAC Control Register 2 (CACR2)

Address(es): CAC.CACR2 4004 4602h



Bit	Symbol	Bit name	Description	R/W
b0	RPS	Reference Signal Select	0: CACREF pin input 1: Internal clock (internally generated signal).	R/W
b3 to b1	RSCS[2:0]	Measurement Reference Clock Select	b3 b1 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock (PCLKB) 1 1 0: IWDTCLK clock 1 1 1: Setting prohibited.	R/W
b5, b4	RCDS[1:0]	Measurement Reference Clock Frequency Division Ratio Select	b5 b4 0 0: ×1/32 clock 0 1: ×1/128 clock 1 0: ×1/1024 clock 1 1: ×1/8192 clock.	R/W
b7, b6	DFS[1:0]	Digital Filter Select	b7 b6 0 0: Disable digital filtering 0 1: Use sampling clock for the digital filter as the frequency measuring clock 1 0: Use sampling clock for the digital filter as the frequency measuring clock divided by 4 1 1: Use sampling clock for the digital filter as the frequency measuring clock divided by 16.	R/W

Note: Set the CACR2 register when the CACR0.CFME bit is 0.

RPS bit (Reference Signal Select)

The RPS bit selects whether to use the CACREF pin input or an internal clock (internally generated signal) as the reference signal.

RSCS[2:0] bits (Measurement Reference Clock Select)

The RSCS[2:0] bits select the reference clock for measurement.

RCDS[1:0] bits (Measurement Reference Clock Frequency Division Ratio Select)

The RCDS[1:0] bits select the frequency division ratio of the measurement reference clock when an internal reference clock is selected (RPS = 1). When RPS = 0 (CACREF pin is used as the reference clock source), the reference clock is not divided.

DFS[1:0] bits (Digital Filter Select)

The DFS[1:0] bits enable or disable the digital filter and select its sampling clock.

10.2.4 CAC Interrupt Control Register (CAICR)

Address(es): CAC.CAICR 4004 4603h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FERRIE	Frequency Error Interrupt Request Enable	0: Frequency error interrupt request is disabled 1: Frequency error interrupt request is enabled.	R/W
b1	MENDIE	Measurement End Interrupt Request Enable	0: Measurement end interrupt request is disabled 1: Measurement end interrupt request is enabled.	R/W
b2	OVFIE	Overflow Interrupt Request Enable	0: Overflow interrupt request is disabled 1: Overflow interrupt request is enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	FERRFCL	FERRF Clear	When 1 is written to this bit, the FERRF flag is cleared. This bit is read as 0.	R/W
b5	MENDFCL	MENDF Clear	When 1 is written to this bit, the MENDF flag is cleared. This bit is read as 0.	R/W
b6	OVFFCL	OVFF Clear	When 1 is written to this bit, the OVFF flag is cleared. This bit is read as 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

FERRIE bit (Frequency Error Interrupt Request Enable)

The FERRIE bit enables the frequency error interrupt request.

MENDIE bit (Measurement End Interrupt Request Enable)

The MENDIE bit enables the measurement end interrupt request.

OVFIE bit (Overflow Interrupt Request Enable)

The OVFIE bit enables the overflow interrupt request.

FERRFCL bit (FERRF Clear)

Setting the FERRFCL bit to 1 clears the CASTR.FERRF flag.

MENDFCL bit (MENDF Clear)

Setting the MENDFCL bit to 1 clears the CASTR.MENDF flag.

OVFFCL bit (OVFF Clear)

Setting the OVFFCL bit to 1 clears the CASTR.OVFF flag.

10.2.5 CAC Status Register (CASTR)

Address(es): CAC.CASTR 4004 4604h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OVFF	MENDF	FERRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FERRF	Frequency Error Flag	0: Clock frequency is within the allowable range 1: Clock frequency has deviated beyond the allowable range (frequency error).	R
b1	MENDF	Measurement End Flag	0: Measurement is in progress 1: Measurement ended.	R
b2	OVFF	Overflow Flag	0: Counter has not overflowed 1: Counter overflowed.	R
b7 to b3	—	Reserved	These bits are read as 0	R

FERRF flag (Frequency Error Flag)

The FERRF flag indicates a deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- The clock frequency is outside the allowable range defined in the CAULVR and CALLVR registers.

[Clearing condition]

- 1 is written to the FERRFCL bit.

MENDF flag (Measurement End Flag)

The MENDF flag indicates the end of measurement.

[Setting condition]

- Measurement ends.

[Clearing condition]

- 1 is written to the MENDFCL bit.

OVFF flag (Overflow Flag)

The OVFF flag indicates that the counter overflowed.

[Setting condition]

- The counter overflows.

[Clearing condition]

- 1 is written to the OVFFCL bit.

10.2.6 CAC Upper-Limit Value Setting Register (CAULVR)

Address(es): CAC.CAULVR 4004 4606h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAULVR is a 16-bit read/write register that specifies the upper value of the allowable range. When the counter value exceeds the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0.

The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.

10.2.7 CAC Lower-Limit Value Setting Register (CALLVR)

Address(es): CAC.CALLVR 4004 4608h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CALLVR is a 16-bit read/write register that specifies the lower value of the allowable range. When the counter value falls below the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0.

The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.

10.2.8 CAC Counter Buffer Register (CACNTBR)

Address(es): CAC.CACNTBR 4004 460Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CACNTBR is a 16-bit read-only register that stores the measurement result.

10.3 Operation

10.3.1 Measuring Clock Frequency

The CAC measures the clock frequency using the CACREF pin input or the internal clock as a reference. Figure 10.2 shows an operating example of the CAC.

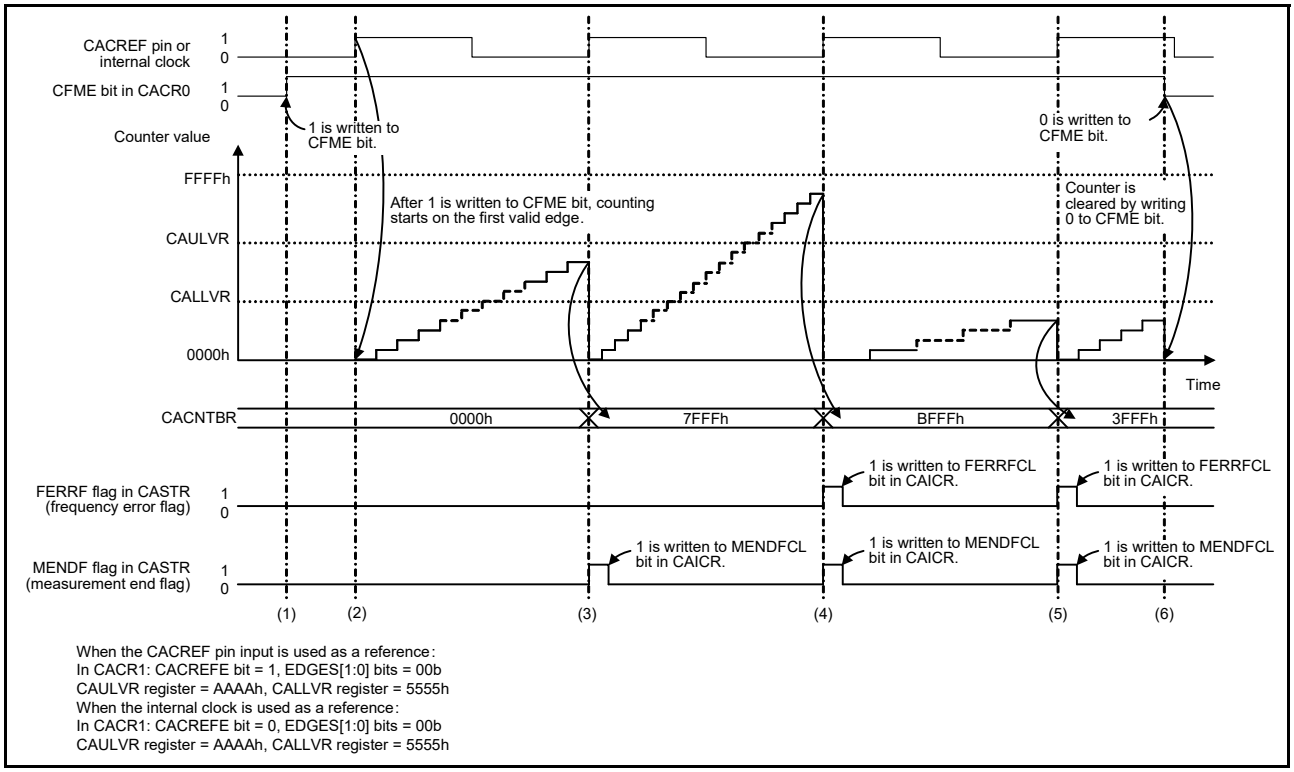


Figure 10.2 CAC operating example

In Figure 10.2:

1. Before writing 1 to CACR0.CFME, set CACR1 and CACR2 to define the measurement target clock and measurement reference clock. Writing 1 to the CACR0.CFME bit enables clock frequency measurement.
2. The timer starts counting up if the valid edge selected in the CACR1.EDGES[1:0] bits is input from the measurement reference clock. In Figure 10.2, the valid edge is a rising edge (CACR1.EDGES[1:0] = 00b).
3. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are true, only the MENDF flag in CASTR is set to 1, because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
4. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
5. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
6. When the CFME bit in CACR0 is 1, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops up-counting.

10.3.2 Digital Filtering of Signals on CACREF Pin

The CACREF pin has a digital filter, and levels on the CACREF pin are transmitted to the internal circuitry after three consecutive matches in the selected sampling interval. The same level continues to be transmitted internally until the level on the pin has three consecutive matches again. Enabling or disabling of the digital filter and its sampling clock are selectable.

The counter value transferred to CACNTBR might be in error by up to 1 cycle of the sampling clock because of the difference between the phases of the digital filter and the signal input to the CACREF pin. When a frequency dividing clock is selected as a count source clock, the counter value error is obtained using the following formula:

Counter value error = (1 cycle of the count source clock) / (1 cycle of the sampling clock)

10.4 Interrupt Requests

The CAC generates three types of interrupt requests:

- Frequency error interrupt
- Measurement end interrupt
- Overflow interrupt.

When an interrupt source is generated, the associated status flag becomes 1. Table 10.3 provides information on the CAC interrupt requests.

Table 10.3 CAC interrupt requests

Interrupt request	Interrupt enable bit	Status flag	Interrupt sources
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	The result of comparing CACNTBR with CAULVR and CALLVR is either CACNTBR > CAULVR or CACNTBR < CALLVR
Measurement end interrupt	CAICR.MENDIE	CASTR.MENDF	• Valid edge is input from the CACREF pin or internal clock • Measurement end interrupt does not occur at the first valid edge after writing 1 to the CACR0.CFME bit.
Overflow interrupt	CAICR.OVFIE	CASTR.OVFF	The counter overflows

10.5 Usage Notes

10.5.1 Settings for the Module-Stop Function

The Module Stop Control Register C (MSTPCRC) can enable or disable CAC operation. The CAC module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

11. Low Power Modes

11.1 Overview

The MCU provides several functions for reducing power consumption, such as setting clock dividers, stopping modules, selecting power control mode in normal mode, and transitioning to low power modes.

Table 11.1 lists the specifications of the low power mode functions. Table 11.2 lists the conditions to transition to low power modes, the states of the CPU and peripheral modules, and the method for canceling each mode. After a reset, the MCU enters the program execution state, but only the DMAC, DTC, and SRAM operate.

Table 11.1 Specifications of the low power mode functions

Parameter	Specifications
Reducing power consumption by switching clock signals	The frequency division ratio can be selected independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), and flash interface clock (FCLK)*1
Module-stop state	Peripheral module functions can be stopped independently
Low power modes	• Sleep mode • Software Standby mode • Snooze mode • Deep Software Standby mode.
Power control modes	Power consumption can be reduced in Normal, Sleep, and Snooze modes by selecting an appropriate operating power control mode according to the operating frequency and voltage. Three operating power control modes are available: • High-speed mode • Low-speed mode • Subosc-speed mode.

Note 1. For details, see section 9, Clock Generation Circuit.

Table 11.2 Operating conditions of each low power mode (1 of 2)

Parameter	Sleep mode	Software Standby mode	Snooze mode*1	Deep Software Standby mode
Transition condition	WFI instruction while SBYCR.SSBY = 0	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0	Snooze request in Software Standby mode. SNZCR.SNZE = 1	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1
Canceling method	All interrupts. Any reset available in the mode.	Interrupts shown in Table 11.3. Any reset available in the mode.	Interrupts shown in Table 11.3. Any reset available in the mode.	Interrupts shown in Table 11.3. Any reset available in the mode.
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Reset state
State after cancellation by a reset	Reset state	Reset state	Reset state	Reset state
Main clock oscillator	Selectable	Stop	Selectable*2	Stop
Sub-clock oscillator	Selectable	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Middle-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Low-speed on-chip oscillator	Selectable	Selectable	Selectable	Selectable*3
IWDT-dedicated on-chip oscillator	Selectable*5	Selectable*5	Selectable*5	Stop
PLL	Selectable	Stop	Selectable*2	Stop
Oscillation stop detection function	Selectable	Operation prohibited	Operation prohibited	Operation prohibited
Clock/buzzer output function	Selectable	Selectable*4	Selectable	Stop (Undefined)

Table 11.2 Operating conditions of each low power mode (2 of 2)

Parameter	Sleep mode	Software Standby mode	Snooze mode*1	Deep Software Standby mode
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)	Stop (Undefined)
SRAMHS	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Flash memory	Operating	Stop (Retained)	Stop (Retained)	Stop (Retained)
DMA Controller (DMAC)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
Data Transfer Controller (DTC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Watchdog Timer (WDT)	Selectable*5	Stop (Retained)	Stop (Retained)	Stop (Undefined)
Independent Watchdog Timer (IWDT)	Selectable*5	Selectable*5	Selectable *5	Stop (Undefined)
Low Power Asynchronous General Purpose Timer (AGTn, n = 0, 1)	Selectable	Selectable*6	Selectable*6	Selectable*6
12-bit A/D Converter (ADC12)	Selectable	Stop (Retained)	Selectable*15	Stop (Undefined)
Programmable Gain Amplifiers (PGAs)	Selectable*16	Selectable*16	Selectable*16	Stop (Undefined)
12-bit D/A Converter (DAC12)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Data Operation Circuit (DOC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Serial Communications Interface (SCI0)	Selectable	Stop (Retained)	Selectable (RXD0 falling edge is available to enter Snooze mode) (only in asynchronous mode).*11	Stop (Undefined)
Serial Communications Interface (SCIn, n = 1 to 4, 8, 9)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I^2C Bus Interface (IIC0)	Selectable	Selectable*10	Selectable*10	Stop (Undefined)
I^2C Bus Interface (IIC1)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
Event Link Controller (ELC)	Selectable	Stop (Retained)	Selectable*7	Stop (Undefined)
High-Speed Analog Comparator (ACMPHS0)	Selectable	Selectable*9	Selectable. VCOUT function only.*9	Stop (Undefined)
High-Speed Analog Comparator (ACMPHSn, n = 1 to 5)	Selectable	Selectable*8	Selectable. VCOUT function only.*8	Stop (Undefined)
IRQn (n = 0 to 13) pin interrupt	Selectable	Selectable	Selectable	Stop (Undefined)
NMI, IRQn-DS (n = 0, 1, 4 to 12) pin interrupt	Selectable	Selectable	Selectable	Selectable
Key Interrupt Function (KINT)	Selectable	Selectable	Selectable	Stop (Undefined)
Low voltage detection (LVD)	Selectable	Selectable	Selectable	Selectable*12
Power-on reset circuit	Operating	Operating	Operating	Operating*13
Other peripheral modules	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I/O ports	Operating	Retained*14	Operating	Retained*14

Note: Selectable means that operating or not operating can be selected in the control registers.
Stop (Retained) means that the contents of the internal registers are retained but the operations are suspended.
Operation prohibited means that the function must be stopped before entering Software Standby mode.

Stop (Undefined) means that the contents of the internal registers are undefined and power to the internal circuit is cut off.

Note 1. All modules whose module-stop bits are 0 start as soon as PCLKs are supplied after entering Snooze mode. To avoid an increase in power consumption in Snooze mode, set the module-stop bit of modules that are not required in Snooze mode to 1 before entering Software Standby mode.

Note 2. When using SCI0 in Snooze mode, MOSCCR.MOSTP and PLLCR.PLLSTP bits must be 1.

Note 3. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, the oscillator status is the same as before entering Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, the oscillator stops when the MCU enters Deep Software Standby mode.

Note 4. Stopped when the Clock Output Source Select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO) and 100b (SOSC).

Note 5. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in Option Function Select Register 0 (OFS0) in WDT auto start mode.

Note 6. AGT0 operation is possible when 100b (AGTLCLK) or 110b (AGTSCLK) is selected in the AGT0.AGTMR1.TCK[2:0] bits. AGT1 operation is possible when 100b (AGTLCLK), 110b (AGTSCLK), or 101b (underflow event signal from AGT0) is selected in the AGT1.AGTMR1.TCK[2:0] bits.
When 100b (AGTLCLK) is selected in AGTn.AGTMR1.TCK[2:0] bits (n = 0, 1), the DPSBYCR.DEEPCUT[1:0] bits must be set to 00b before entering Deep Software Standby mode.

Note 7. Event lists the restrictions described in section 11.10.13, ELC Events in Snooze Mode.

Note 8. Only VCOUT function is permitted. The VCOUT pin operates when ACMPHS uses no digital filter.
For details on digital filter, see section 38, High-Speed Analog Comparator (ACMPHS).

Note 9. When CMPCTL0.CSTEN bit is 1, canceling Software Standby Mode or entering Snooze mode by the comparator detection is available.

Note 10. IIC0 wakeup interrupt is available.

Note 11. Serial communication mode of SCI0 is asynchronous mode.

Note 12. When using LVD in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] bits must be 00b or 01b before entering Deep Software Standby mode.

Note 13. When the MCU enters Deep Software Standby mode with the DPSBYCR.DEEPCUT[1:0] bits set to 11b, the LVD circuit stops and the low power function of the power-on reset circuit is enabled.

Note 14. For the address bus and bus control signals (for SRAM: CS0, CS1, CS4 to CS7, RD, WR0, and ALE), keeping the output state or changing to the high-impedance state can be selected in the SBYCR.OPE bit.

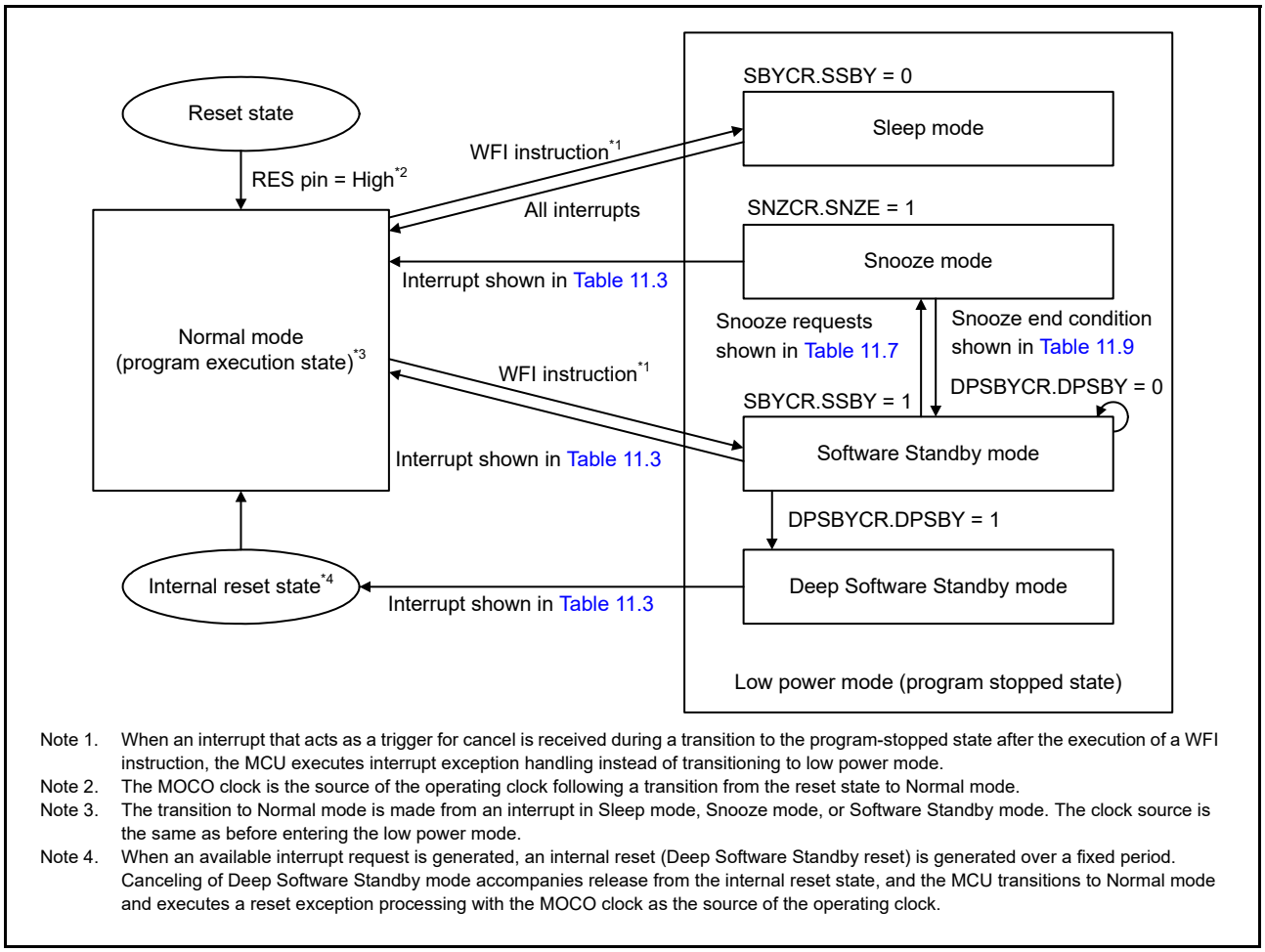
Note 15. When using the 12-bit A/D Converter in Snooze mode, the ADCMPCR.CMPAE and ADCMPCR.CMPBE bits must be 1.

Note 16. When using the Programmable Gain Amplifiers, MSTPDn (n = 15, 16) must be set to 0. For details, see section 35.3.12, Programmable Gain Amplifiers.

Table 11.3 Interrupt sources for canceling Snooze, Software Standby, and Deep Software Standby modes

Interrupt source	Name	Software Standby mode	Snooze mode	Deep Software Standby mode
NMI		Yes	Yes	Yes
Port	PORT_IRQn (n = 0 to 13)	Yes	Yes	No
	PORT_IRQn-DS (n = 0, 1, 4 to 12)	Yes	Yes	Yes
LVD	LVD_LVD1	Yes	Yes	Yes
	LVD_LVD2	Yes	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes	No
KINT	KEY_INTKR	Yes	Yes	No
AGT1	AGT1_AGTI	Yes	Yes*3	Yes
	AGT1_AGTCMAI	Yes	Yes	No
	AGT1_AGTCMBI	Yes	Yes	No
ACMPHS	ACMP_HS0	Yes	Yes	No
IIC0	IIC0_WUI	Yes	Yes	No
ADC12n (n = 0, 1)	ADC12n_WCMPM	No	Yes with SELSR0*1,*3	No
	ADC12n_WCMPUM	No	Yes with SELSR0*1,*3	No
SCI0	SCI0_AM	No	Yes with SELSR0*1,*2	No
	SCI0_RXI_OR_ERI	No	Yes with SELSR0*1,*2	No
DTC	DTC_COMPLETE	No	Yes with SELSR0*1,*3	No
DOC	DOC_DOPCI	No	Yes with SELSR0*1	No

Note 1. To use the interrupt request as a trigger for exiting Snooze mode, the request must be selected in SELSR0. See section 13, Interrupt Controller Unit (ICU). When a trigger selected in SELSR0 occurs after executing a WFI instruction and during transition from Normal to Software Standby mode, whether the request can be accepted depends on the timing of the occurrence.
Note 2. Only one of either SCI0_AM or SCI0_RXI_OR_ERI can be selected.
Note 3. The event that is enabled by the SNZEDCR register must not be used.



Note 1. When an interrupt that acts as a trigger for cancel is received during a transition to the program-stopped state after the execution of a WFI instruction, the MCU executes interrupt exception handling instead of transitioning to low power mode.
Note 2. The MOCO clock is the source of the operating clock following a transition from the reset state to Normal mode.
Note 3. The transition to Normal mode is made from an interrupt in Sleep mode, Snooze mode, or Software Standby mode. The clock source is the same as before entering the low power mode.
Note 4. When an available interrupt request is generated, an internal reset (Deep Software Standby reset) is generated over a fixed period. Canceling of Deep Software Standby mode accompanies release from the internal reset state, and the MCU transitions to Normal mode and executes a reset exception processing with the MOCO clock as the source of the operating clock.

Figure 11.1 Mode transitions

11.2 Register Descriptions

11.2.1 Standby Control Register (SBYCR)

Address(es): SYSTEM.SBYCR 4001 E00Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSBY	OPE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b14	OPE	Output Port Enable	0: In Software Standby or Deep Software Standby mode, set the address bus and bus control signals to the high-impedance state. In Snooze mode, the status of the address bus and bus control signals are the same as before entering Software Standby mode. 1: In Software Standby or Deep Software Standby mode, retain the output state of the address bus and bus control signals.	R/W
b15	SSBY	Software Standby	0: Sleep mode 1: Software Standby mode when DPSBYCR.DPSBY = 0 and Deep Software Standby mode when DPSBYCR.DPSBY = 1.	R/W

OPE bit (Output Port Enable)

The OPE bit specifies whether to set to the high-impedance state or to retain the output of the address bus and bus control signals (for SRAM: CS0, CS1, CS4 to CS7, RD, WR0, and ALE) in Software Standby mode or Deep Software Standby mode.

SSBY bit (Software Standby)

The SSBY bit specifies the transition destination after a WFI instruction is executed.

When the SSBY bit is set to 1, the MCU enters Software Standby mode after executing a WFI instruction. When the MCU cancels Software Standby mode by an interrupt, the SSBY bit remains 1. The SSBY bit can be cleared by writing 0 to it.

When the OSTDCR.OSTDE bit is 1, the setting of SSBY bit is ignored. Even if the SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

When the FENTRYR.FENTRYi bit (i = 0 to 3) is 1 or the FENTRYR.FENTRYD bit is 1, the setting of SSBY bit is ignored. Even if the SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction. See Table 11.6 for details.

When using the HOCO clock to enter Software Standby mode, STCONR.STCON[1:0] must be set to 00b and HOCOWTCR.HSTS[2:0] must be set to 110b. However, when using SCI0 in Snooze mode, HOCOWTCR.HSTS[2:0] must be set to 010b.

11.2.2 Module Stop Control Register A (MSTPCRA)

Address(es): SYSTEM.MSTPCRA 4001 E01Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	MSTPA5	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	The write value should be 1.	R/W
b4 to b1	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	MSTPA5	High-Speed SRAM Module Stop	Target module: high-speed SRAM 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b7, b6	—	Reserved	The write value should be 1.	R/W
b21 to b8	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b22	MSTPA22	DMA Controller/Data Transfer Controller Module Stop*2	Target modules: DMAC, DTC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Bit	Symbol	Bit name	Description	R/W
b31 to b23	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. Bit [0] and bit [6] settings must be the same.
Note 2. When rewriting the MSTPA22 bit from 0 to 1, disable the DMAC and DTC before setting the MSTPA22 bit.

11.2.3 Module Stop Control Register B (MSTPCRB)

Address(es): MSTP.MSTPCRB 4004 7000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPB31	MSTPB30	MSTPB29	MSTPB28	MSTPB27	—	—	—	MSTPB23	MSTPB22	—	—	MSTPB19	MSTPB18	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MSTPB9	MSTPB8	—	—	MSTPB5	—	—	MSTPB2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b2	MSTPB2	Controller Area Network 0 Module Stop*1	Target module: CAN0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b4, b3	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	MSTPB5	IrDA Module Stop	Target module: IrDA 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b7, b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b8	MSTPB8	I2C Bus Interface 1 Module Stop	Target module: IIC1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b9	MSTPB9	I2C Bus Interface 0 Module Stop	Target module: IIC0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b17 to b10	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b18	MSTPB18	Serial Peripheral Interface 1 Module Stop	Target module: SPI1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b19	MSTPB19	Serial Peripheral Interface 0 Module Stop	Target module: SPI0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b21, b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b22	MSTPB22	Serial Communication Interface 9 Module Stop	Target module: SCI9 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b23	MSTPB23	Serial Communication Interface 8 Module Stop	Target module: SCI8 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b26 to b24	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b27	MSTPB27	Serial Communication Interface 4 Module Stop	Target module: SCI4 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Bit	Symbol	Bit name	Description	R/W
b28	MSTPB28	Serial Communication Interface 3 Module Stop	Target module: SCI3 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b29	MSTPB29	Serial Communication Interface 2 Module Stop	Target module: SCI2 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b30	MSTPB30	Serial Communication Interface 1 Module Stop	Target module: SCI1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b31	MSTPB31	Serial Communication Interface 0 Module Stop	Target module: SCI0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Note 1. The MSTPBi bit must be written while the oscillation of the clock controlled by this bit is stable. To enter Software Standby mode after writing to this bit, wait for 2 CAN clock (CANMCLK) cycles after writing, then execute a WFI instruction (i = 1, 2).

11.2.4 Module Stop Control Register C (MSTPCRC)

Address(es): MSTP.MSTPCRC 4004 7004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPC31	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MSTPC14	MSTPC13	—	—	—	—	—	—	—	—	—	—	—	MSTPC1	MSTPC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	MSTPC0*1	Clock Frequency Accuracy Measurement Circuit Module Stop	Target module: CAC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b1	MSTPC1	Cyclic Redundancy Check Calculator Module Stop	Target module: CRC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b12 to b2	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b13	MSTPC13	Data Operation Circuit Module Stop	Target module: DOC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b14	MSTPC14	Event Link Controller Module Stop	Target module: ELC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b30 to b15	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b31	MSTPC31	SCE7 Module Stop	Target module: SCE7 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Note 1. The MSTPC0 bit must be written while the oscillation of the clock controlled by this bit is stable. To enter Software Standby mode after writing to this bit, wait for 2 cycles of the slowest clock from the clocks output by the oscillators, then execute a WFI instruction.

11.2.5 Module Stop Control Register D (MSTPCRD)

Address(es): MSTP.MSTPCRD 4004 7008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	MSTPD28	MSTPD27	MSTPD26	MSTPD25	MSTPD24	MSTPD23	MSTPD22	—	MSTPD20	—	—	—	MSTPD16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPD15	MSTPD14	—	—	—	—	—	—	—	MSTPD6	MSTPD5	—	MSTPD3	MSTPD2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b2	MSTPD2	Low Power Asynchronous General Purpose Timer 1 Module Stop*1	Target module: AGT1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b3	MSTPD3	Low Power Asynchronous General Purpose Timer 0 Module Stop*2	Target module: AGT0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b4	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b5	MSTPD5	General PWM Timer 32EH0 to 32EH3, 32E4 to 32E7, and PWM Delay Generation Circuit Module Stop	Target modules: GPT32EHx (x = 0 to 3), GPT32Ey (y = 4 to 7), and PWM Delay Generation Circuit 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b6	MSTPD6	General PWM Timer 328 to 3212 Module Stop	Target modules: GPT32x (x = 8 to 12) 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b13 to b7	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b14	MSTPD14	Port Output Enable for GPT Module Stop	Target module: POEG 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b15	MSTPD15	12-bit A/D Converter 1 Module Stop	Target module: ADC121 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b16	MSTPD16	12-bit A/D Converter 0 Module Stop	Target module: ADC120 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b19 to b17	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b20	MSTPD20	12-bit D/A Converter Module Stop	Target module: DAC12 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b21	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b22	MSTPD22	Temperature Sensor Module Stop	Target module: TSN 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b23	MSTPD23	High-Speed Analog Comparator 5 Module Stop	Target module: ACMPHS5 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b24	MSTPD24	High-Speed Analog Comparator 4 Module Stop	Target module: ACMPHS4 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b25	MSTPD25	High-Speed Analog Comparator 3 Module Stop	Target module: ACMPHS3 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Bit	Symbol	Bit name	Description	R/W
b26	MSTPD26	High-Speed Analog Comparator 2 Module Stop	Target module: ACMPHS2 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b27	MSTPD27	High-Speed Analog Comparator 1 Module Stop	Target module: ACMPHS1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b28	MSTPD28	High-Speed Analog Comparator 0 Module Stop	Target module: ACMPHS0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b31 to b29	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. When the count source is sub-clock oscillator or LOCO, AGT1 counting does not stop even if MSTPD2 bit is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT1 registers.
Note 2. When the count source is sub-clock oscillator or LOCO, AGT0 counting does not stop even if MSTPD3 bit is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT0 registers.

11.2.6 Operating Power Control Register (OPCCR)

Address(es): SYSTEM.OPCCR 4001 E0A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	OPCM[1:0]	Operating Power Control Mode Select	b1 b0 0 0: High-speed mode 1 1: Low-speed mode. Other settings are prohibited.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	OPCMTSF	Operating Power Control Mode Transition Status Flag	• Read 0: Transition completed 1: Transition in progress. • Write The write value should be 0.	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The OPCCR register is used to reduce power consumption in Normal mode and Sleep mode by specifying a lower operating frequency and operating voltage. For the procedure to change the operating power control modes, see section 11.5, Function for Lower Operating Power Consumption.

When transitioning from Software Standby mode to Normal or Snooze mode, the settings in the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits are as follows, regardless of their settings before entering Software Standby mode:

- OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0b (not Subosc-speed mode).

If Software Standby mode is canceled before the transition to Software Standby completes, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits retain their settings from before the WFI instruction is executed. If this causes a problem, set the MCU to High-speed mode during the exception handling procedure when canceling Software Standby mode.

OPCM[1:0] bits (Operating Power Control Mode Select)

The OPCM[1:0] bits select the operating power control mode in Normal mode and Sleep mode. Table 11.4 shows the relationship between the operating power control modes, the OPCM[1:0], and SOPCM bit settings.

OPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The OPCMTSF flag indicates the switching control state when the operating power control mode is switched. This flag

becomes 1 when the OPCM[1:0] bits are written, and 0 when the mode transition completes. Read this flag and confirm that it is 0 before proceeding.

11.2.7 Sub Operating Power Control Register (SOPCCR)

Address(es): SYSTEM.SOPCCR 4001 E0AAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SOPCMTSF	—	—	—	SOPCM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SOPCM	Sub Operating Power Control Mode Select	0: Not Subosc-speed mode 1: Subosc-speed mode.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SOPCMTSF	Sub Operating Power Control Mode Transition Status Flag	0: Transition completed 1: Transition in progress.	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SOPCCR register is used to reduce power consumption in Normal and Sleep modes by initiating entry to and exit from Subosc-speed mode. Subosc-speed mode is only available when using the sub-clock oscillator or LOCO without dividing the frequency.

The flash cache function should be set to disabled by setting FCACHEE.FCACHEEN to 0 before switching the operating power control mode. For details, see section 41, Flash Memory.

For the procedure to change operating power control modes, see section 11.5, Function for Lower Operating Power Consumption.

SOPCM bit (Sub Operating Power Control Mode Select)

The SOPCM bit selects the operating power control mode in Normal mode and Sleep mode. Setting this bit to 1 allows transition to Subosc-speed mode. Setting this bit to 0 allows a return to the operating mode (set in OPCCR.OPCM[1:0]) before the transition to Subosc-speed mode.

When transitioning from Software Standby mode to Normal mode or Snooze mode, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM settings are as follows, regardless of their settings before entering Software Standby mode:

- OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0b (not Subosc-speed mode).

If Software Standby mode is canceled before the transition to Software Standby completes, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits retain their settings from before the WFI instruction is executed. If this causes a problem, set the MCU to High-speed mode during the exception handling procedure when canceling Software Standby mode.

Table 11.4 shows the relationship between the operating power control modes, the OPCM[1:0], and SOPCM bit settings.

SOPCMTSF flag (Sub Operating Power Control Mode Transition Status Flag)

The SOPCMTSF flag indicates the switching control state when the operating power control mode is switched from or to Subosc-speed mode. This flag becomes 1 when the SOPCM bit is written, and 0 when mode transition completes. Read this flag and confirm that it is 0 before proceeding.

Table 11.4 shows the operating power control modes.

Table 11.4 Relationship between the operating power control modes, and the OPCM[1:0] and SOPCM bits

Operating power control mode	OPCM[1:0] bits	SOPCM bit	Power consumption
High-speed mode	00b	0	High ↓ Low
Low-speed mode	11b	0	
Subosc-speed mode	00b, 11b	1	

Note: See section 43, Electrical Characteristics for the operating frequency range and voltage range.

High-speed operating mode

After a reset cancellation, the MCU is activated in this mode.

Low-speed mode

The following constraints apply in low-speed mode:

- Programming and erasure operations for the flash memory are prohibited
- Using the PLL is prohibited. See section 11.10.1, Register Access.

In low-speed mode, lower power consumption is possible than in High-speed mode when the same operation is performed under the same conditions, such as operating frequency and operating voltage.

Subosc-speed mode

The following constraints apply in Subosc-speed mode:

- Programming and erasure operations for the flash memory are prohibited
- Reading of the data flash is prohibited
- Using MOSC, PLL, MOCO, or HOCO is prohibited. See section 11.10.1, Register Access.
- Using the divided clock for ICK or FCK is prohibited. See section 11.10.1, Register Access.
- Using the oscillation stop detection function of the main clock oscillator is prohibited.

11.2.8 Snooze Control Register (SNZCR)

Address(es): SYSTEM.SNZCR 4001 E092h

	b7	b6	b5	b4	b3	b2	b1	b0
	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RXDREQEN	RXD0 Snooze Request Enable	0: Ignore RXD0 falling edge in Software Standby mode 1: Detect RXD0 falling edge in Software Standby mode.	R/W
b1	SNZDTCEN	DTC Enable in Snooze mode	0: Disable DTC operation in Snooze mode 1: Enable DTC operation in Snooze mode.	R/W
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SNZE	Snooze Mode Enable	0: Disable Snooze mode 1: Enable Snooze mode.	R/W

RXDREQEN bit (RXD0 Snooze Request Enable)

The RXDREQEN bit specifies whether to detect a falling edge of the RXD0 pin in Software Standby mode. This bit is only available when SCI0 operates in asynchronous mode. To detect a falling edge of the RXD0 pin, set this bit before entering Software Standby mode. When this bit is set to 1, a falling edge of the RXD0 pin in Software Standby mode causes the MCU to enter Snooze mode.

SNZDTCEN bit (DTC Enable in Snooze mode)

The SNZDTCEN bit specifies whether to use the DTC and SRAM in Snooze mode. To use the DTC and SRAM in Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, the DTC can be activated by setting IELSRn (ICU Event Link Setting Register n).

SNZE bit (Snooze Mode Enable)

The SNZE bit enables or disables a transition from Software Standby to Snooze mode. To use Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, a trigger as shown in Table 11.7 in Software Standby mode causes the MCU to enter Snooze mode. After the MCU transitions from Software Standby mode or Snooze mode to Normal mode, clear the SNZE bit once then set it before re-entering Software Standby mode. For details, see section 11.8, Snooze Mode.

11.2.9 Snooze End Control Register (SNZEDCR)

Address(es): SYSTEM.SNZEDCR 4001 E094h

	b7	b6	b5	b4	b3	b2	b1	b0
	SCI0UMTED	AD1UMTED	AD1MATED	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	AGTUNFED	AGT1 Underflow Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b1	DTCZRED	Last DTC Transmission Completion Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b2	DTCNZRED	Not Last DTC Transmission Completion Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b3	AD0MATED	AD Compare Match 0 Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b4	AD0UMTED	AD Compare Mismatch 0 Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b5	AD1MATED	AD Compare Match 1 Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b6	AD1UMTED	AD Compare Mismatch 1 Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b7	SCI0UMTED	SCI0 Address Mismatch Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W

To use a trigger shown in Table 11.8 as a condition to switch from Snooze mode to Software Standby mode, set the associated bit in the SNZEDCR register to 1.

The event that is used to return to Normal mode from Snooze mode listed in Table 11.3 must not be enabled in the SNZEDCR register.

AGTUNFED bit (AGT1 Underflow Snooze End Enable)

The AGTUNFED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AGT1 underflow. For details on the trigger conditions, see section 24, Low Power Asynchronous General-Purpose Timer (AGT).

DTCZRED bit (Last DTC Transmission Completion Snooze End Enable)

The DTCZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of the last DTC transmission, that is, when CRA or CRB register in the DTC is 0. For details on the trigger conditions, see section 17, Data Transfer Controller (DTC).

DTCNZRED bit (Not Last DTC Transmission Completion Snooze End Enable)

The DTCNZRED bit specifies whether to enable a transition from Snooze to Software Standby mode on completion of each DTC transmission, that is, when CRA or CRB register in the DTC is not 0. For details on the trigger conditions, see section 17, Data Transfer Controller (DTC).

AD0MATED bit (AD Compare Match 0 Snooze End Enable)

The AD0MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AD0 event when a conversion result matches the expected data. For details on the trigger conditions, see section 35, 12-Bit A/D Converter (ADC12).

AD0UMTED bit (AD Compare Mismatch 0 Snooze End Enable)

The AD0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AD0 event when the conversion result does not match the expected data. For details on the trigger conditions, see section 35, 12-Bit A/D Converter (ADC12).

AD1MATED bit (AD Compare Match 1 Snooze End Enable)

The AD1MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AD1 event when the conversion result matches the expected data. For details on the trigger conditions, see section 35, 12-Bit A/D Converter (ADC12).

AD1UMTED bit (AD Compare Mismatch 1 Snooze End Enable)

The AD1UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AD1 event when the conversion result does not match the expected data. For details on the trigger conditions, see section 35, 12-Bit A/D Converter (ADC12).

SCI0UMTED bit (SCI0 Address Mismatch Snooze End Enable)

The SCI0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an SCI0 event when an address received in Software Standby mode does not match the expected data. For details on the trigger conditions, see section 27, Serial Communications Interface (SCI). Only set this bit to 1 when SCI0 operates in asynchronous mode.

11.2.10 Snooze Request Control Register (SNZREQCR)

Address(es): SYSTEM.SNZREQCR 4001 E098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	—	—	—	SNZREQEN22	—	—	—	—	SNZREQEN17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SNZREQEN13	SNZREQEN12	SNZREQEN11	SNZREQEN10	SNZREQEN9	SNZREQEN8	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SNZREQEN0	Snooze Request Enable 0	Enable IRQ0 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b1	SNZREQEN1	Snooze Request Enable 1	Enable IRQ1 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b2	SNZREQEN2	Snooze Request Enable 2	Enable IRQ2 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W

Bit	Symbol	Bit name	Description	R/W
b3	SNZREQEN3	Snooze Request Enable 3	Enable IRQ3 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b4	SNZREQEN4	Snooze Request Enable 4	Enable IRQ4 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b5	SNZREQEN5	Snooze Request Enable 5	Enable IRQ5 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b6	SNZREQEN6	Snooze Request Enable 6	Enable IRQ6 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b7	SNZREQEN7	Snooze Request Enable 7	Enable IRQ7 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b8	SNZREQEN8	Snooze Request Enable 8	Enable IRQ8 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b9	SNZREQEN9	Snooze Request Enable 9	Enable IRQ9 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b10	SNZREQEN10	Snooze Request Enable 10	Enable IRQ10 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b11	SNZREQEN11	Snooze Request Enable 11	Enable IRQ11 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b12	SNZREQEN12	Snooze Request Enable 12	Enable IRQ12 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b13	SNZREQEN13	Snooze Request Enable 13	Enable IRQ13 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b16 to b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17	SNZREQEN17	Snooze Request Enable 17	Enable Key Interrupt snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b21 to b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b22	SNZREQEN22	Snooze Request Enable 22	Enable ACMPHS0 snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b27 to b23	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	SNZREQEN28	Snooze Request Enable 28	Enable AGT1 underflow snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b29	SNZREQEN29	Snooze Request Enable 29	Enable AGT1 compare match A snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b30	SNZREQEN30	Snooze Request Enable 30	Enable AGT1 compare match B snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The SNZREQCR register controls which trigger causes the MCU to switch from Software Standby mode to Snooze mode. If a trigger is selected as a request to cancel Software Standby mode by setting the WUPEN register, see section 13, Interrupt Controller Unit (ICU), the MCU enters Normal mode when the trigger is generated while the associated bit of the SNZREQCR is 1. The setting of the WUPEN register always has a higher priority than the SNZREQCR register settings. For details, see section 11.8, Snooze Mode and section 13, Interrupt Controller Unit (ICU).

11.2.11 Deep Software Standby Control Register (DPSBYCR)

Address(es): SYSTEM.DPSBYCR 4001 E400h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSBY	IOKEEP	—	—	—	—	DEEPCUT[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	DEEPCUT[1:0]	Power-Supply Control	b1 b0 0 0: Supply power to the low-speed on-chip oscillator and AGTn in Deep Software Standby mode 0 1: Do not supply power to the low-speed on-chip oscillator and AGTn in Deep Software Standby mode 1 0: Setting prohibited 1 1: Do not supply power to the low-speed on-chip oscillator and AGTn in Deep Software Standby mode. In addition, disable the LVD and enable the low power function of the power-on reset circuit.	R/W
b5 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	IOKEEP	I/O Port Retention	0: When Deep Software Standby mode is canceled, clear the I/O ports to the reset state 1: When Deep Software Standby mode is canceled, keep the I/O ports in the same state as in Deep Software Standby mode.	R/W
b7	DPSBY	Deep Software Standby	0: Sleep mode (SBYCR.SSBY = 0) or Software Standby mode (SBYCR.SSBY = 1) 1: Sleep mode (SBYCR.SSBY = 0) or Deep Software Standby mode (SBYCR.SSBY = 1).	R/W

The DPSBYCR register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

DEEPCUT[1:0] bits (Power-Supply Control)

The DEEPCUT[1:0] bits control the internal power supply to the low-speed on-chip oscillator and AGTn in Deep Software Standby mode. In addition, these bits control the state of the LVD and power-on reset circuit in Deep Software Standby mode. When an LVD interrupt is used in Deep Software Standby mode, the DEEPCUT[1:0] bits must be set to 00b or 01b.

For lower power consumption, set the DEEPCUT[1:0] bits to 11b so that the LVD is stopped and the low power mode function of the power-on reset circuit is enabled. The internal power supply of the SRAM stops in Deep Software Standby mode regardless of the DEEPCUT[1:0] bit settings.

IOKEEP bit (I/O Port Retention)

In Deep Software Standby mode, the I/O ports keep the same states as in Software Standby mode. The IOKEEP bit specifies whether to reset the state of the I/O ports when Deep Software Standby mode is canceled.

DPSBY bit (Deep Software Standby)

The DPSBY bit controls transitions to Deep Software Standby mode. See Table 11.6 for details.

When the WFI instruction is executed while the SBYCR.SSBY and DPSBYCR.DPSBY bits are both 1, the MCU enters Deep Software Standby mode through Software Standby mode.

The DPSBY bit remains 1 when Deep Software Standby mode is canceled by certain pins that are the sources of external pin interrupts (NMI, IRQ0-DS, IRQ1-DS, and IRQ4-DS to IRQ12-DS) or by a peripheral interrupt (voltage monitor 1 or voltage monitor 2). Write 0 to this bit to clear it.

The DPSBY setting is invalid when the OFS0.IWDTSTPCTL bit is 0 (counting continues), regardless of the setting in the OFS0.IWDTSTRT bit. When the SBYCR.SSBY and DPSBY bits are 1, the MCU transitions to Software Standby mode on execution of a WFI instruction.

The DPSBY setting is invalid when the voltage monitor 1 reset is enabled (LVD1CR0.RI = 1) or when the voltage

monitor 2 reset is enabled (LVD2CR0.RI = 1). When the SBYCR.SSBY and the DPSBY bits are 1, the MCU transitions to Software Standby mode on execution of a WFI instruction.

11.2.12 Deep Software Standby Interrupt Enable Register 0 (DPSIER0)

Address(es): SYSTEM.DPSIER0 4001 E402h

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7E	DIRQ6E	DIRQ5E	DIRQ4E	—	—	DIRQ1E	DIRQ0E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ0E	IRQ0-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ0-DS pin: 0: Disable 1: Enable.	R/W
b1	DIRQ1E	IRQ1-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ1-DS pin: 0: Disable 1: Enable.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DIRQ4E	IRQ4-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ4-DS pin: 0: Disable 1: Enable.	R/W
b5	DIRQ5E	IRQ5-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ5-DS pin: 0: Disable 1: Enable.	R/W
b6	DIRQ6E	IRQ6-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ6-DS pin: 0: Disable 1: Enable.	R/W
b7	DIRQ7E	IRQ7-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ7-DS pin: 0: Disable 1: Enable.	R/W

The DPSIER0 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source. After a setting in DPSIER0 is changed, an edge can be internally generated depending on the associated pin state, resulting in the associated DPSIFR0 bit being set to 1. Clear DPSIFR0 to 0 before entering Deep Software Standby mode.

11.2.13 Deep Software Standby Interrupt Enable Register 1 (DPSIER1)

Address(es): SYSTEM.DPSIER1 4001 E403h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DIRQ12E	DIRQ11E	DIRQ10E	DIRQ9E	DIRQ8E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ8E	IRQ8-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ8-DS pin: 0: Disable 1: Enable.	R/W
b1	DIRQ9E	IRQ9-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ9-DS pin: 0: Disable 1: Enable.	R/W

Bit	Symbol	Bit name	Description	R/W
b2	DIRQ10E	IRQ10-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ10-DS pin: 0: Disable 1: Enable.	R/W
b3	DIRQ11E	IRQ11-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ11-DS pin: 0: Disable 1: Enable.	R/W
b4	DIRQ12E	IRQ12-DS Pin Enable	Enable canceling of Deep Software Standby mode by the IRQ12-DS pin: 0: Disable 1: Enable.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DPSIER1 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source. After a setting in DPSIER1 is changed, an edge can be internally generated depending on the associated pin state, resulting in the associated DPSIFR1 bit being set to 1. Clear DPSIFR1 to 0 before entering Deep Software Standby mode.

11.2.14 Deep Software Standby Interrupt Enable Register 2 (DPSIER2)

Address(es): SYSTEM.DPSIER2 4001 E404h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIE	—	—	DLVD2IE	DLVD1IE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLVD1IE	LVD1 Deep Software Standby Cancel Signal Enable	Enable canceling of Deep Software Standby mode by the voltage monitor 1 signal: 0: Disable 1: Enable.	R/W
b1	DLVD2IE	LVD2 Deep Software Standby Cancel Signal Enable	Enable canceling of Deep Software Standby mode by the voltage monitor 2 signal: 0: Disable 1: Enable.	R/W
b3 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DNMIE	NMI Pin Enable	Enable canceling of Deep Software Standby mode by the NMI pin: 0: Disable 1: Enable.	R/W*1
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. 1 can be written only once. After 1 is written to this bit, subsequent write accesses are disabled.

The DPSIER2 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source. After a setting in DPSIER2 is changed, an edge can be internally generated depending on the associated pin state, resulting in the associated DPSIFR2 bit being set to 1. Clear DPSIFR2 to 0 before entering Deep Software Standby mode.

11.2.15 Deep Software Standby Interrupt Enable Register 3 (DPSIER3)

Address(es): SYSTEM.DPSIER3 4001 E405h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAGT1IE	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	DAGT1IE	AGT1 Underflow Deep Software Standby Cancel Signal Enable	Enable canceling of Deep Software Standby mode by an AGT1 underflow: 0: Disable 1: Enable.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DPSIER3 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source. After a setting in DPSIER3 is changed, an edge can be internally generated depending on the associated pin state, resulting in the associated DPSIFR3 bit being set to 1. Clear DPSIFR3 to 0 before entering Deep Software Standby mode.

11.2.16 Deep Software Standby Interrupt Flag Register 0 (DPSIFR0)

Address(es): SYSTEM.DPSIFR0 4001 E406h

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7F	DIRQ6F	DIRQ5F	DIRQ4F	—	—	DIRQ1F	DIRQ0F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ0F	IRQ0-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ0-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b1	DIRQ1F	IRQ1-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ1-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R(/W) *1
b4	DIRQ4F	IRQ4-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ4-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b5	DIRQ5F	IRQ5-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ5-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b6	DIRQ6F	IRQ6-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ6-DS pin: 0: No request generated 1: Request generated.	R(/W) *1

Bit	Symbol	Bit name	Description	R/W
b7	DIRQ7F	IRQ7-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ7-DS pin: 0: No request generated 1: Request generated.	R(/W) *1

Note 1. Only 0 can be written to clear the flag.

The flags in the DPSIFR0 register is set to 1 when the associated cancel request specified in DPSIEGR0 is generated. Each flag can be set to 1 when a cancel request is generated in any mode, not only in Deep Software Standby mode, or when the setting in DPSIER0 is changed. Clear DPSIFR0 to 00h before entering Deep Software Standby mode.

To clear DPSIFR0 to 00h after modifying DPSIER0, wait for at least 6 PCLKB cycles, read DPSIFR0, and then write 0 to DPSIFR0. Six or more PCLKB cycles can be secured, for example, by reading DPSIER0. DPSIFR0 is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

DIRQnF flag (IRQn-DS Deep Software Standby Cancel Flag) (n = 0, 1, 4 to 7)

The DIRQnF flag indicates that a cancel request is generated by the IRQn-DS pin.

[Setting condition]

- A cancel request generated by an IRQn-DS pin specified in DPSIEGR0.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

11.2.17 Deep Software Standby Interrupt Flag Register 1 (DPSIFR1)

Address(es): SYSTEM.DPSIFR1 4001 E407h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DIRQ12F	DIRQ11F	DIRQ10F	DIRQ9F	DIRQ8F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ8F	IRQ8-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ8-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b1	DIRQ9F	IRQ9-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ9-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b2	DIRQ10F	IRQ10-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ10-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b3	DIRQ11F	IRQ11-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ11-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b4	DIRQ12F	IRQ12-DS Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the IRQ12-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R(/W)*1

Note 1. Only 0 can be written to clear the flag.

The flags in the DPSIFR1 register are set to 1 when the associated cancel request specified in DPSIEGR1 is generated. Each flag can be set to 1 when a cancel request is generated in any mode, not only in Deep Software Standby mode, or when the setting in DPSIER1 is changed. Clear DPSIFR1 to 00h before entering Deep Software Standby mode.

To clear DPSIFR1 to 00h after modifying DPSIER1, wait for at least 6 PCLKB cycles, read DPSIFR1, and then write 0 to DPSIFR1. Six or more PCLKB cycles can be secured, for example, by reading DPSIER1. DPSIFR1 is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

DIRQnF flag (IRQn-DS Deep Software Standby Cancel Flag) (n = 8 to 12)

The DIRQnF flag indicates that a cancel request is generated by the IRQn-DS pin.

[Setting condition]

- A cancel request generated by the IRQn-DS pin specified in DPSIEGR1.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

11.2.18 Deep Software Standby Interrupt Flag Register 2 (DPSIFR2)

Address(es): SYSTEM.DPSIFR2 4001 E408h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIF	—	—	DLVD2IF	DLVD1IF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLVD1IF	LVD1 Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the voltage monitor 1 signal: 0: No request generated 1: Request generated.	R(/W)*1
b1	DLVD2IF	LVD2 Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the voltage monitor 2 signal: 0: No request generated 1: Request generated.	R(/W)*1
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DNMIF	NMI Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by the NMI pin: 0: No request generated 1: Request generated.	R(/W)*1
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the flag.

The flags in the DPSIFR2 register are set to 1 when the associated cancel request specified in DPSIEGR2 is generated. Each flag can be set to 1 when a cancel request is generated in any mode, not only in Deep Software Standby mode, or when the setting in DPSIER2 is changed. Clear DPSIFR2 to 00h before entering Deep Software Standby mode.

To clear DPSIFR2 to 00h after modifying DPSIER2, wait for at least 6 PCLKB cycles, read DPSIFR2, and then write 0 to DPSIFR2. Six or more PCLKB cycles can be secured, for example, by reading DPSIER2. DPSIFR2 is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

DLVDmIF flag (LVDm Deep Software Standby Cancel Flag) (m = 1 or 2)

The DLVDmIF flag indicates that a cancel request is generated by the voltage monitor m signal.

[Setting condition]

- A cancel request generated by the voltage monitor m signal specified in DPSIEGR2.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

DNMIF flag (NMI Deep Software Standby Cancel Flag)

The DNMIF flag indicates that a cancel request is generated by the NMI pin.

[Setting condition]

- A cancel request generated by the NMI pin specified in DPSIEGR2.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

11.2.19 Deep Software Standby Interrupt Flag Register 3 (DPSIFR3)

Address(es): SYSTEM.DPSIFR3 4001 E409h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAGT1IF	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	DAGT1IF	AGT1 Underflow Deep Software Standby Cancel Flag	Indicate Deep Software Standby cancel request by an AGT1 underflow: 0: No request generated 1: Request generated.	R(/W)*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the flag.

The flags in the DPSIFR3 register are set to 1 when the associated cancel request is generated. Each flag can be set to 1 when a cancel request is generated in any mode, not only in Deep Software Standby mode, or when the setting in DPSIER3 is changed. Clear DPSIFR3 to 00h before entering Deep Software Standby mode.

To clear DPSIFR3 to 00h after modifying DPSIER3, wait for at least 6 PCLKB cycles, read DPSIFR3, and then write 0 to DPSIFR3. Six or more PCLKB cycles can be secured, for example, by reading DPSIER3. DPSIFR3 is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see section 6, Resets.

DAGT1IF flag (AGT1 Underflow Deep Software Standby Cancel Flag)

The DAGT1IF flag indicates that a cancel request is generated by an AGT1 underflow.

[Setting condition]

- A cancel request generated by the AGT1 underflow.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

11.2.20 Deep Software Standby Interrupt Edge Register 0 (DPSIEGR0)

Address(es): SYSTEM.DPSIEGR0 4001 E40Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7EG	DIRQ6EG	DIRQ5EG	DIRQ4EG	—	—	DIRQ1EG	DIRQ0EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ0EG	IRQ0-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b1	DIRQ1EG	IRQ1-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DIRQ4EG	IRQ4-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b5	DIRQ5EG	IRQ5-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b6	DIRQ6EG	IRQ6-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b7	DIRQ7EG	IRQ7-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W

The DPSIEGR0 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

11.2.21 Deep Software Standby Interrupt Edge Register 1 (DPSIEGR1)

Address(es): SYSTEM.DPSIEGR1 4001 E40Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DIRQ12EG	DIRQ11EG	DIRQ10EG	DIRQ9EG	DIRQ8EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ8EG	IRQ8-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b1	DIRQ9EG	IRQ9-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b2	DIRQ10EG	IRQ10-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b3	DIRQ11EG	IRQ11-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b4	DIRQ12EG	IRQ12-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DPSIEGR1 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

11.2.22 Deep Software Standby Interrupt Edge Register 2 (DPSIEGR2)

Address(es): SYSTEM.DPSIEGR2 4001 E40Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIEG	—	—	DLVD2EG	DLVD1EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLVD1EG	LVD1 Edge Select	0: Generate cancel request when VCC < V_{det1} (fall) is detected 1: Generate cancel request when VCC ≥ V_{det1} (rise) is detected.	R/W
b1	DLVD2EG	LVD2 Edge Select	0: Generate cancel request when VCC < V_{det2} (fall) is detected 1: Generate cancel request when VCC ≥ V_{det2} (rise) is detected.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DNMIEG	NMI Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DPSIEGR2 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

11.2.23 System Control OCD Control Register (SYOCDCR)

Address(es): SYSTEM.SYOCDCR 4001 E40Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	DBGEN	—	—	—	—	—	—	DOCDF
Value after reset:	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	DOCDF	Deep Software Standby OCD Flag	Indicate cancel request by the DBIRQ: 0: DBIRQ is not generated 1: DBIRQ is generated.	R/(W)*1
b6 to b1	—	Reserved	These bits are read as 0. The write value must be 0.	R/W
b7	DBGEN	Debugger Enable Bit	0: Disable on-chip debugger 1: Enable on-chip debugger. Set to 1 first in On-Chip Debug (OCD) mode.	R/W

Note 1. Writing 0 clears the flag. Writing 1 is ignored.

SYOCDCR is not initialized by the internal reset signal that cancels Deep Software Standby mode.

DOCDF flag (Deep Software Standby OCD Flag)

The DOCDF flag indicates that a Deep Software Standby cancel request is generated by the MCUCTRL.DBIRQ bit. The flag is set to 1 when the cancel request is generated. The flag can be set to 1 when a cancel request is generated in any mode, not only in Deep Software Standby mode. Clear the DOCDF flag to 0 before entering Deep Software Standby mode.

[Setting condition]

- A cancel request generated by the MCUCTRL.DBIRQ bit.

[Clearing condition]

- Writing 0 to the flag after reading it as 1

- When the DBGEN bit is 0.

DBGEN bit (Debugger Enable Bit)

The DBGEN bit enables the OCD mode. This bit must be set to 1 first in OCD mode.

[Setting condition]

- Writing 1 to the bit when the debugger is connected.

[Clearing condition]

- Power-on reset is generated
- Writing 0 to the bit.

11.2.24 Standby Condition Register (STCONR)

Address(es): SYSTEM.STCONR 4001 E40Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	STCON[1:0]	
Value after reset:	1	1	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b1 to b0	STCON[1:0]	SSTBY Condition Bit	b1 b0 0 0: Set this value to transition to Software Standby mode when using HOCO 1 1: Set this value to transition to Software Standby mode when not using HOCO.	R/W
b5 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7 to b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

STCON[1:0] bits (SSTBY Condition Bit)

The STCON[1:0] bits must always be set to 00b when using HOCO to enter Software Standby mode.

11.3 Reducing Power Consumption by Switching Clock Signals

The clock frequency changes when the following bits are set:

- SCKDIVCR.FCK[2:0]
- ICK[2:0]
- PCKA[2:0]
- PCKB[2:0]
- PCKC[2:0]
- PCKD[2:0].

The module and clock associations are as follows:

- The CPU, DMAC, DTC, flash, and SRAM use the operating clock specified in the ICK[2:0] bits
- Peripheral modules use the operating clocks specified in the PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits
- The flash memory interface uses the operating clock specified in the FCK[2:0] bits.

For details, see section 9, Clock Generation Circuit.

11.4 Module-Stop Function

The module-stop function can be set for each on-chip peripheral module.

When the MSTPmi bit (m = A to D, i = 31 to 0) in MSTPCRA to MSTPCRD is set to 1, the specified module stops operating and enters the module-stop state, but the CPU continues to operate independently. Clearing the MSTPmi bit to 0 cancels the module-stop state, allowing the module to resume operation at the end of the bus cycle. The internal states of the modules are retained in the module-stop state.

After a reset is canceled, all modules other than the DMAC, DTC, and SRAM modules are placed in the module-stop state. Do not access the module while the associated MSTPmi bit is 1, otherwise the read/write data or the operation of the module is not guaranteed. Also, do not set the MSTPmi bit to 1 while the associated module is accessed.

When the PLL is selected as the clock source, MSTPmi bits must only be changed one bit at a time. In this case, wait at least 250 ns after changing each MSTPmi bit before starting subsequent processing if you change any of the following bits:

- MSTPA22 (DMAC, DTC)
- MSTPC31 (SCE7)
- MSTPD5 (GPT32EH, GPT32E).

The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

11.5 Function for Lower Operating Power Consumption

By selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage, power consumption can be reduced in Normal mode and Sleep mode.

11.5.1 Setting the Operating Power Control Mode

Make sure that the operating conditions such as the voltage and frequency ranges, are always within the specified ranges before and after switching the operating power control modes. This section provides example procedures for switching operating power control modes.

Table 11.5 Available oscillators in each mode

Mode	Oscillator						
	PLL	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	Main clock oscillator	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available	Available
Low-speed	N/A	Available	Available	Available	Available	Available	Available
Subosc-speed	N/A	N/A	N/A	Available	N/A	Available	Available

(1) Switching from a higher to a lower power mode

Example 1: From High-speed mode to Low-speed mode

Operation begins in High-speed mode.

1. Change the oscillator to that used in Low-speed mode. Set the frequency of each clock lower than the maximum operating frequency in Low-speed mode.
2. Turn off the oscillator that is not required in Low-speed mode.
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Set the OPCCR.OPCM[1:0] bits to 11b (Low-speed mode).
5. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).

Operation is now in Low-speed mode.

Example 2: From High-speed mode to Subosc-speed mode

Operation begins in High-speed mode.

1. Switch the clock source to the sub-clock oscillator.
2. Turn off HOCO, MOCO, LOCO, main oscillator, and PLL.
3. Confirm that all clock sources other than the sub-clock oscillator are stopped.
4. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
5. Set the SOPCCR.SOPCM bit to 1 (Subosc-speed mode).
6. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).

Operation is now in Subosc-speed mode.

(2) Switching from a lower to a higher power mode

Example 1: From Subosc-speed mode to High-speed mode

Operation begins in Subosc-speed mode.

1. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
2. Set the SOPCCR.SOPCM bit to 0 (High-speed mode).
3. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
4. Turn on the required oscillator in High-speed mode.
5. Set the frequency of each clock lower than the maximum operating frequency for High-speed mode.

Operation is now in High-speed mode.

Example 2: From Low-speed mode to High-speed mode

Operation begins in Low-speed mode.

1. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
2. Set the OPCCR.OPCM[1:0] bits to 00b (High-speed mode).
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Turn on any required oscillator in High-speed mode.
5. Set the frequency of each clock to lower than the maximum operating frequency for High-speed mode.

Operation is now in High-speed mode.

11.6 Sleep Mode

11.6.1 Transitioning to Sleep Mode

When a WFI instruction is executed while the SBYCR.SSBY bit is 0, the MCU enters Sleep mode. In Sleep mode, the CPU stops operating, but the contents of its internal registers are retained. Other peripheral functions do not stop. Available resets or interrupts in Sleep mode cause the MCU to cancel Sleep mode. All interrupt sources are available. If using an interrupt to cancel Sleep mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 13, Interrupt Controller Unit (ICU).

Counting by the IWDT stops when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep mode, Software Standby mode, or Snooze mode).

Counting by the IWDT continues when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby mode, or Snooze mode).

Counting by the WDT stops when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 1 (WDT stops in Sleep mode). Similarly, counting by the WDT stops when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 1 (WDT stops in Sleep mode).

Counting by the WDT continues when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.

WDTSTPCTL bit is 0 (WDT does not stop in Sleep mode). Similarly, counting by the WDT continues when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 0 (WDT does not stop in Sleep mode).

11.6.2 Canceling Sleep Mode

Sleep mode is canceled by:

- An interrupt
- A RES pin reset
- A power-on reset
- A voltage monitor reset
- An SRAM parity error reset
- A bus master MPU error reset
- A bus slave MPU error reset
- A reset caused by an IWDT or WDT underflow.

The operations are as follows:

1. Canceling by an interrupt
   When an available interrupt request (see Table 11.3) is generated, Sleep mode is canceled and the MCU starts the interrupt handling.
2. Canceling by RES pin reset
   When the RES pin is driven low, the MCU enters the reset state. Be sure to keep the RES pin low for the time period specified in section 43, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by IWDT reset
   Sleep mode is canceled by an internal reset generated by an IWDT underflow, and the MCU starts the reset exception handling. However, IWDT stops in Sleep mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
4. Canceling by WDT reset
   Sleep mode is canceled by an internal reset generated by an WDT underflow and the MCU starts the reset exception handling. However, WDT stops in Sleep mode even when counting in Normal mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.WDTSTRT = 0 (auto start mode) and OFS0.WDTSTPCTL = 1
   - OFS0.WDTSTRT = 1 (register start mode) and WDTCSTPR.SLCSTP = 1.
5. Canceling by other resets available in Sleep mode
   Sleep mode is canceled by other resets and the MCU starts the reset exception handling.

Note: For details on proper setting of the interrupts, see section 13, Interrupt Controller Unit (ICU).

11.7 Software Standby Mode

11.7.1 Transitioning to Software Standby Mode

When a WFI instruction is executed while the SBYCR.SSBY bit is 1 and the DPSBYCR.DPSBY bit is 0, the MCU enters Software Standby mode. In this mode, the CPU, most of the on-chip peripheral functions, and the oscillators stop. However, the contents of the CPU internal registers and SRAM data, the states of the on-chip peripheral functions, and the I/O port states are retained. Software Standby mode allows a significant reduction in power consumption because most of the oscillators stop in this mode. Table 11.2 shows the status of the on-chip peripheral functions and oscillators. Available resets or interrupts in Software Standby mode cause the MCU to cancel Software Standby mode. See Table 11.3 for available interrupt sources and section 13.2.9, Wake Up Interrupt Enable Register (WUPEN) for information on waking up the MCU from Software Standby mode. If using an interrupt to cancel Software Standby mode, you must set

the associated IELSRn register before executing a WFI instruction. For details, see section 13, Interrupt Controller Unit (ICU).

The status of the address bus and bus control signals in Software Standby mode can be selected with the SBYCR.OPE bit.

Clear the DMAST.DMST and DTCST.DTCST bits to 0 before executing a WFI instruction, except when using the DTC in Snooze mode. If the DTC is required in Snooze mode, set the DTCST.DTCST bit to 1 before executing a WFI instruction.

Counting by the IWDT stops when the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep, Software Standby, or Snooze mode).

Counting by the IWDT continues when the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby mode, or Snooze mode). The WDT stops counting when the MCU enters Software Standby mode.

Do not enter Software Standby mode while OSTDCR.OSTDE is 1 (oscillation stop detection function enabled). To enter Software Standby mode, execute a WFI instruction after disabling the oscillation stop detection function (OSTDCR.OSTDE is 0). If executing a WFI instruction while OSTDCR.OSTDE is 1, the MCU enters Sleep mode even when SBYCR.SSBY is 1. In addition, do not enter Software Standby mode while the flash memory performs a programming or erasing procedure. To enter Software Standby mode, execute a WFI instruction after the programming or erasing procedure completes.

When the PLL is selected as the clock source, set the following modules to the module-stop state before executing a WFI instruction:

- SCE7
- GPT32EH
- GPT32E.

You must also insert a wait time of at least 750 ns before executing the WFI instruction. The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

Table 11.6 shows the setting of the related control bits and the modes entered when executing a WFI instruction.

Figure 11.2 shows an example flow for transitioning to Software Standby mode or Deep Software Standby mode.

Table 11.6 Bit settings that affect modes when executing a WFI instruction

Other bit settings		SBYCR.SSBY and DPSBYCR.DPSBY bit settings			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
OSTDCR.OSTDE	0	Sleep mode	Sleep mode	Software Standby mode	Deep Software Standby mode
	1			Sleep mode	Sleep mode
FENTRYR.FENTRYi	0	Sleep mode	Sleep mode	Software Standby mode	Deep Software Standby mode
	1			Sleep mode	Sleep mode
OFS0.IWDTSTPCTL	0	Sleep mode	Sleep mode	Software Standby mode	Software Standby mode
	1				Deep Software Standby mode
LVD1CR0.RI	0	Sleep mode	Sleep mode	Software Standby mode	Deep Software Standby mode
	1				Software Standby mode
LVD2CR0.RI	0	Sleep mode	Sleep mode	Software Standby mode	Deep Software Standby mode
	1				Software Standby mode

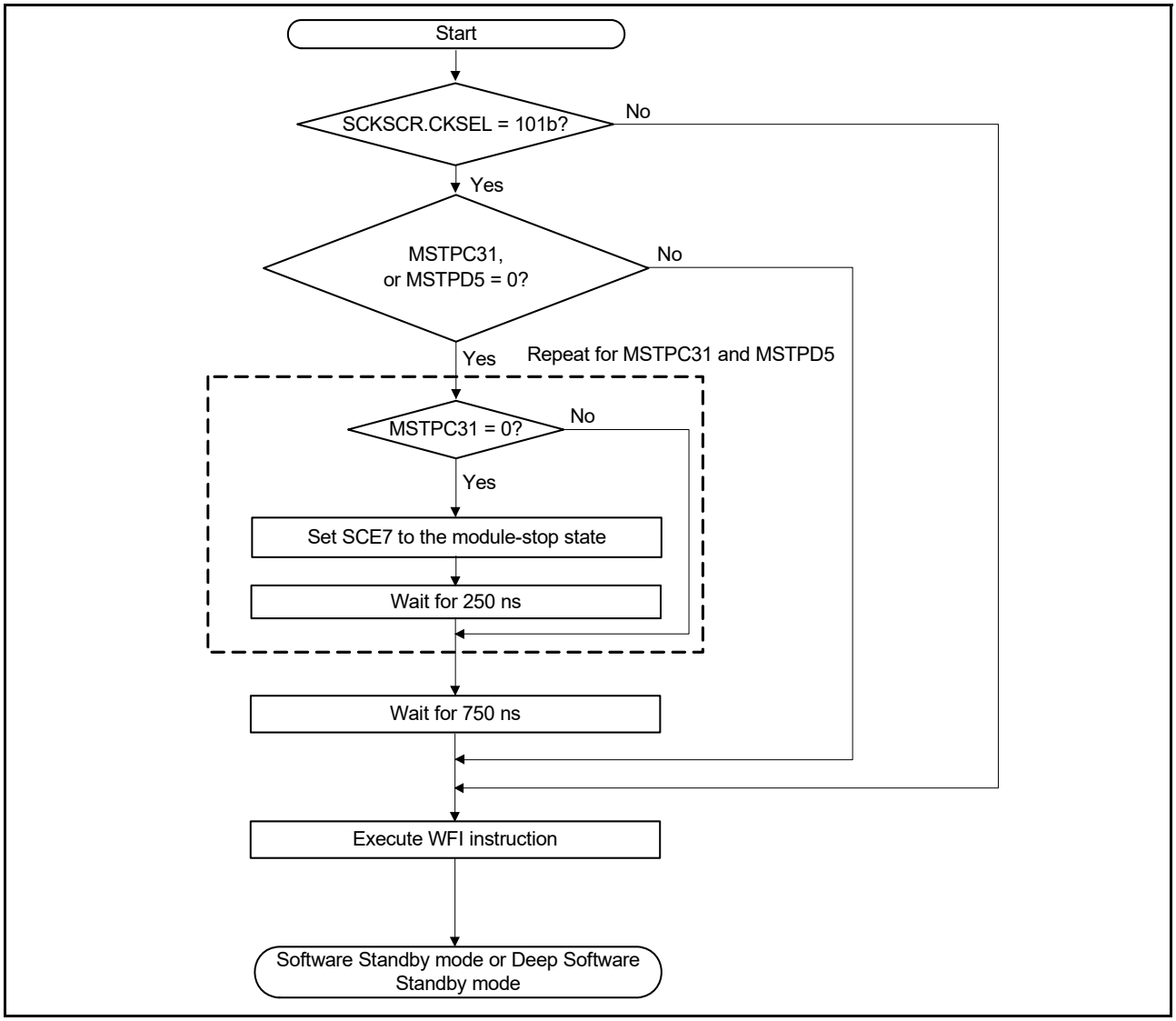


Figure 11.2 Example flow for transition to Software Standby mode or Deep Software Standby mode

11.7.2 Canceling Software Standby Mode

Software Standby mode is canceled by:

- An available interrupt shown in Table 11.3
- A RES pin reset
- A power-on reset
- A voltage monitor reset
- A reset caused by an IWDT underflow.

On exiting Software Standby mode, the oscillators that operate before transitioning to the mode restart. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode. See section 13.2.9, Wake Up Interrupt Enable Register (WUPEN), for information on waking up the MCU from Software Standby mode.

You can cancel Software Standby mode in any of the following ways:

- Canceling by an interrupt
  When an available interrupt request (see Table 11.3) is generated, an oscillator that operates before the transition to Software Standby mode restarts. After all the oscillators are stabilized, the MCU cancels Software Standby mode and starts the interrupt handling. When the PLL is selected as the clock source, you must insert a wait time of at least 250 ns at the beginning of the interrupt handling. The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses. Figure 11.3 shows an example flow for canceling Software Standby mode by an interrupt.
- Canceling by a RES pin reset
  When the RES pin is driven low, the MCU enters the reset state, and the oscillators whose default status is operating, start the oscillation. Be sure to keep the RES pin low for the time period specified in section 43, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
- Canceling by an IWDT reset
  Software Standby mode is canceled by an internal reset generated by an IWDT underflow, and the MCU starts reset exception handling. However, IWDT stops in Software Standby mode and an internal reset for canceling Software Standby mode is not generated in the following conditions:
  - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
- Canceling by other resets available in Software Standby mode
  Software Standby mode is canceled by other resets, and the MCU starts the reset exception handling.

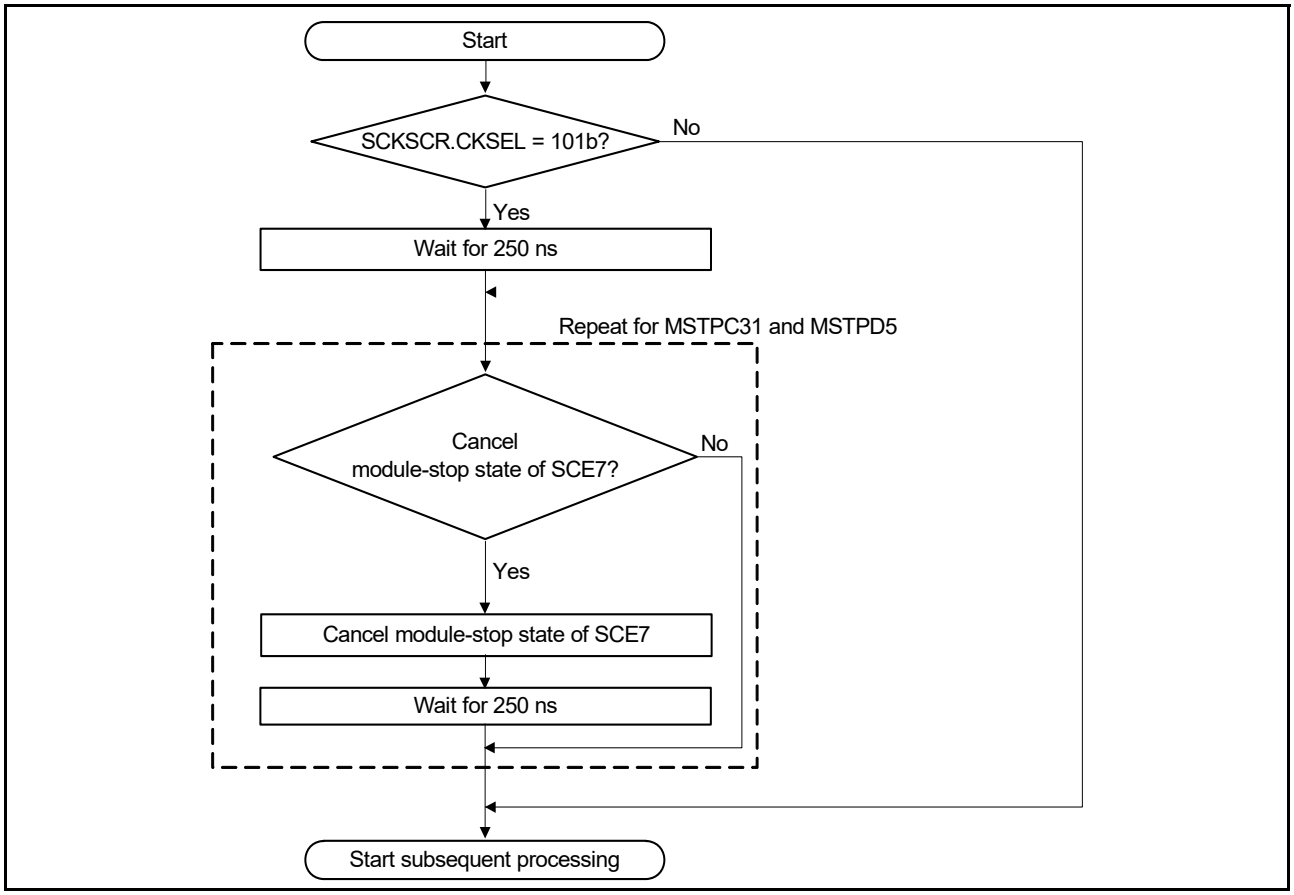


Figure 11.3 Example flow for canceling Software Standby mode

11.7.3 Example of Software Standby Mode Application

Figure 11.4 shows an example of entry to Software Standby mode on detection of a falling edge of the IRQn pin, and exit from Software Standby mode on a rising edge of the IRQn pin.

In this example, an IRQn pin interrupt is accepted when the IRQCRi.IRQMD[1:0] bits of the ICU are set to 01b (falling edge) in Normal mode, and the IRQCRi.IRQMD[1:0] bits set to 10b (rising edge). Next, the SBYCR.SSBY bit is set to 1 and a WFI instruction is executed. As a result, entry to Software Standby mode completes, and exit from Software Standby mode is initiated by a rising edge of the IRQn pin.

Setting the ICU is also required to exit Software Standby mode. For details, see section 13, Interrupt Controller Unit (ICU). The oscillation stabilization time in Figure 11.4 is specified in section 43, Electrical Characteristics.

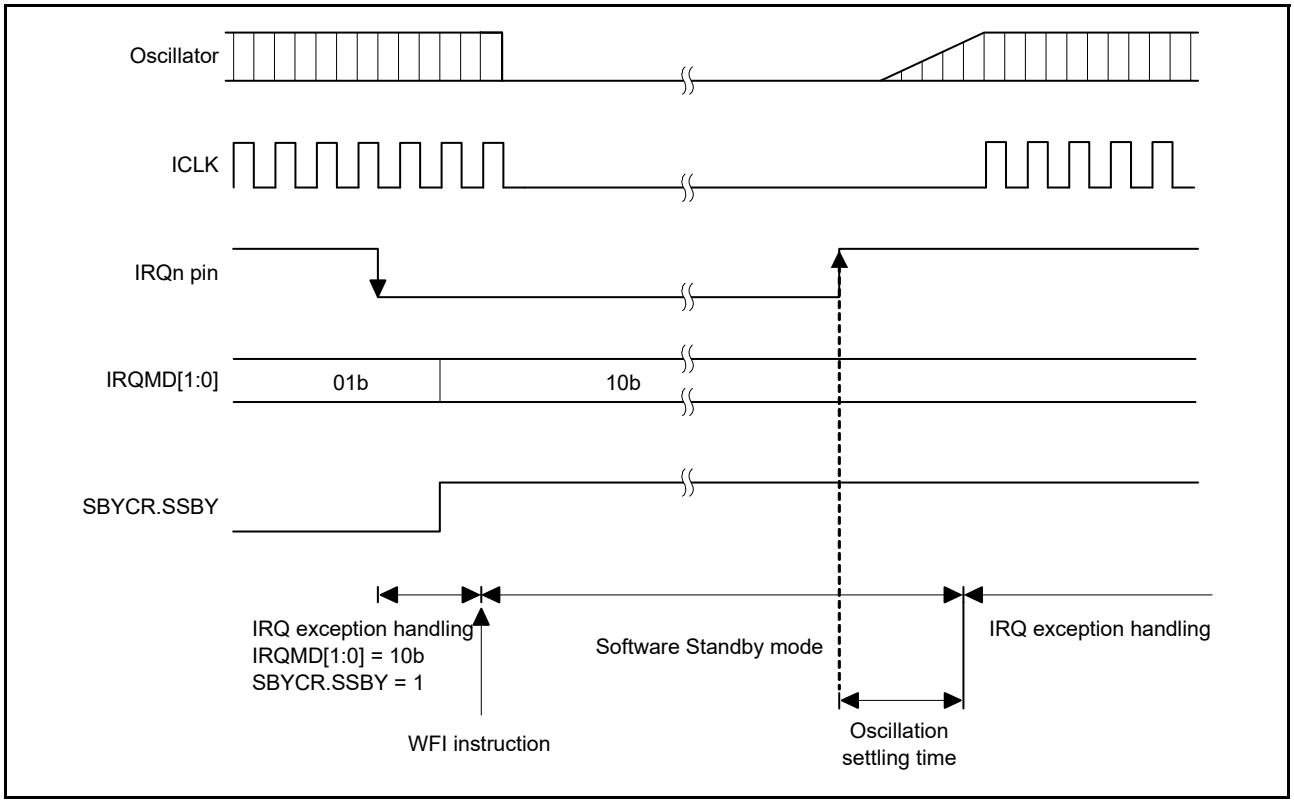


Figure 11.4 Example of Software Standby mode application

11.8 Snooze Mode

11.8.1 Transitioning to Snooze Mode

Figure 11.5 shows snooze mode entry configuration. When the snooze control circuit receives a snooze request in Software Standby mode, the MCU transitions to Snooze mode. In this mode, some peripheral modules operate without waking up the CPU. Table 11.2 shows the peripheral modules that can operate in Snooze mode. Also, DTC operation can be selected in Snooze mode by setting the SNZCR.SNZDTCEN bit.

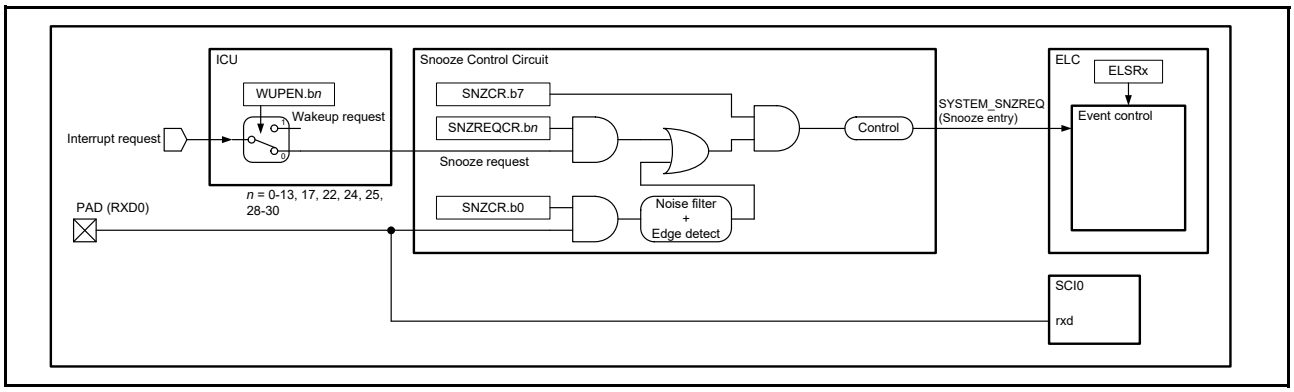


Figure 11.5 Snooze entry configuration

Table 11.7 shows the snooze requests to switch the MCU from Software Standby mode to Snooze mode. To use a listed snooze requests as a trigger to switch to Snooze mode, you must set the associated SNZREQENn bit of the SNZREQCR register or RXDREQEN bit of the SNZCR register before entering Software Standby mode.

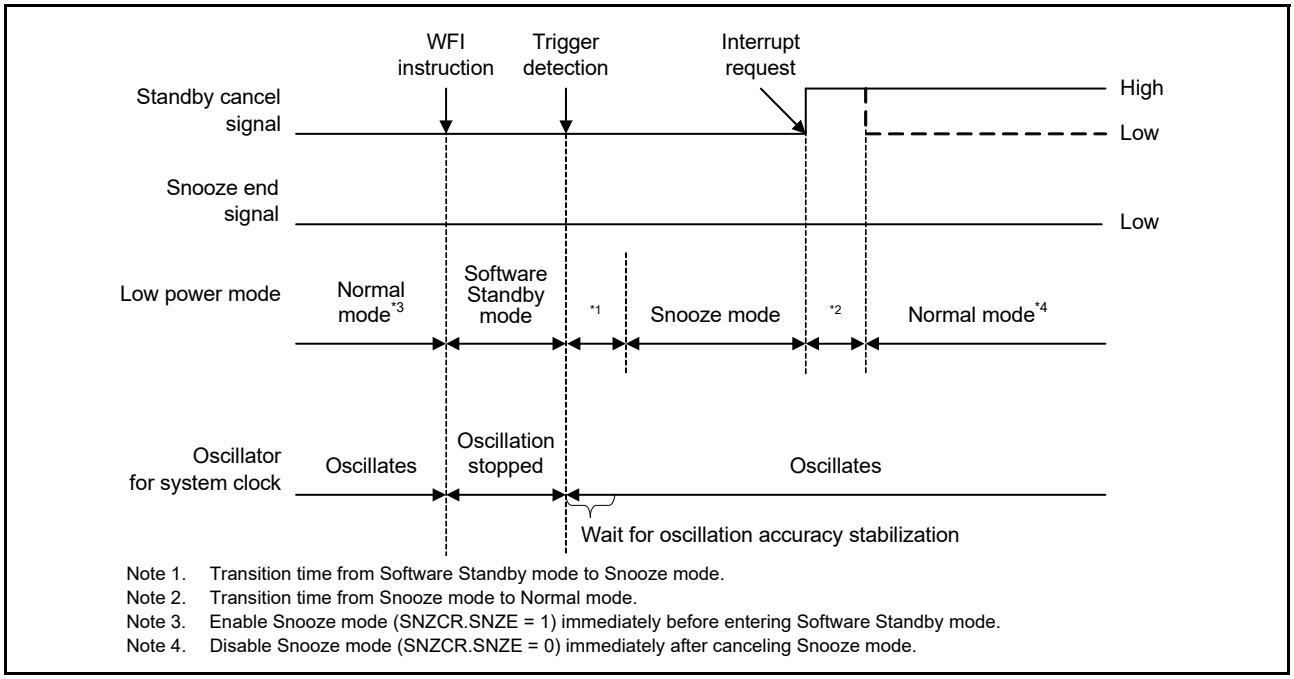
Table 11.7 Available snooze requests to switch to Snooze mode

Snooze request	Control Register	
	Register	Bit*1
PORT_IRQn (n = 0 to 13)	SNZREQCR	SNZREQENn (n = 0 to 13)
KEY_INTKR	SNZREQCR	SNZREQEN17
ACMP_HS0	SNZREQCR	SNZREQEN22
AGT1_AGTI	SNZREQCR	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR	SNZREQEN30
RXD0 falling edge	SNZCR	RXDREQEN*2

Note 1. Do not enable multiple snooze requests at the same time.
Note 2. Do not set the RXDREQEN bit to 1 except in asynchronous mode.

11.8.2 Canceling Snooze Mode

Snooze mode is canceled by an interrupt request that is available in Software Standby mode or a reset. Table 11.3 shows the requests that can be used to exit each mode. After canceling the Snooze mode, the MCU enters Normal mode and proceeds with exception processing for the given interrupt or reset. The action triggered by the interrupt requests selected in SELSR0, cancels Snooze mode. Interrupt canceling Snooze mode must be selected in IELSRn (n = 0 to 96) to link to the NVIC for the associated interrupt handling. See section 13, Interrupt Controller Unit (ICU), for information on SELSR0 and IELSRn registers.



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Transition time from Snooze mode to Normal mode.
Note 3. Enable Snooze mode (SNZCR.SNZE = 1) immediately before entering Software Standby mode.
Note 4. Disable Snooze mode (SNZCR.SNZE = 0) immediately after canceling Snooze mode.

Figure 11.6 Canceling of Snooze mode when an interrupt request signal is generated

11.8.3 Returning to Software Standby Mode

Table 11.8 shows the snooze end requests that can be used as triggers to return to Software Standby mode. The snooze end requests are available only in Snooze mode. If the requests are generated when the MCU is not in Snooze mode, they are ignored. When multiple requests are selected, each one of the requests invokes transition to Software Standby mode from Snooze mode.

Table 11.9 shows the snooze end conditions that consist of the snooze end requests and the conditions of the peripheral modules. The SCI0, ADC120, ADC121, and DTC modules can keep the MCU in Snooze mode until they complete their

operation. However, an AGT1 underflow as a trigger to return to Software Standby mode cancels Snooze mode without waiting for the completion of the SCI0 operation.

Figure 11.7 shows the timing diagram for the transition from Snooze mode to Software Standby mode. This mode transition occurs according to which snooze end requests are set in the SNZEDCR register. A snooze request is cleared automatically after returning to Software Standby mode.

Table 11.8 Available snooze end requests (triggers to return to Software Standby mode)

	Enable/disable control	
Snooze end request	**Register**	**Bit**
AGT1 unterflow or measurement complete (AGT1_AGTI)	SNZEDCR	b0
DTC transfer complete (DTC_COMPLETE)	SNZEDCR	b1
DTC transfer not complete (DTC_TRANSFER)	SNZEDCR	b2
ADC120 window A/B compare match (ADC120_WCMPM)	SNZEDCR	b3
ADC120 window A/B compare mismatch (ADC120_WCMPUM)	SNZEDCR	b4
ADC121 window A/B compare match (ADC121_WCMPM)	SNZEDCR	b5
ADC121 window A/B compare mismatch (ADC121_WCMPUM)	SNZEDCR	b6
SCI0 address mismatch (SCI0_DCUF)	SNZEDCR	b7

Table 11.9 Snooze end conditions

Operating module when a snooze end request occurs	**Snooze end request**	
	AGT1 underflow	**Other than AGT1 underflow**
DTC	The MCU transitions to Software Standby mode after all of the modules listed in this table complete operation	The MCU transitions to Software Standby mode after all of the modules listed to the left of this column complete operation
ADC120		
ADC121		
SCI0	The MCU transitions to Software Standby mode immediately after a snooze end request is generated	
All other modules	The MCU transitions to Software Standby mode immediately after a snooze end request is generated	

Note: If the DTC is used to activate the ADC120, ADC121, or SCI, the MCU transitions to Software Standby mode immediately after a snooze end request is generated.

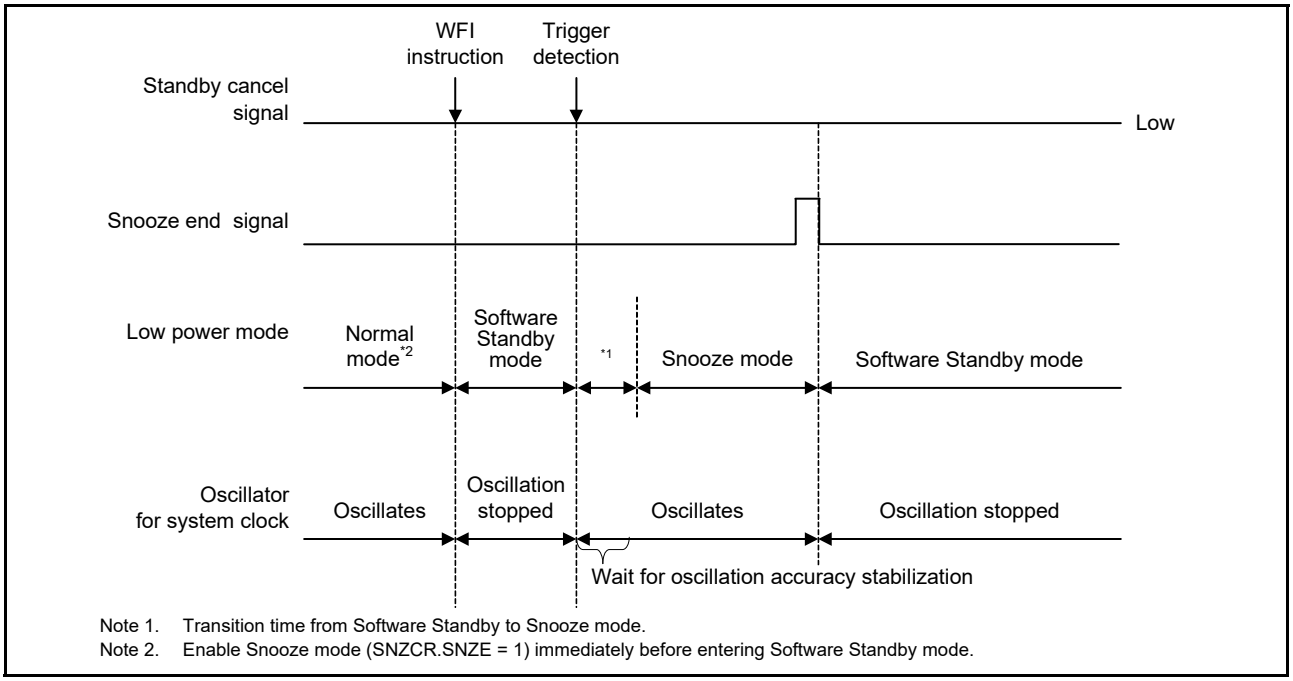


Figure 11.7 Canceling of Snooze mode when an interrupt request signal is not generated

11.8.4 Snooze Operation Example

Figure 11.8 shows an example setting for using ELC in Snooze mode.

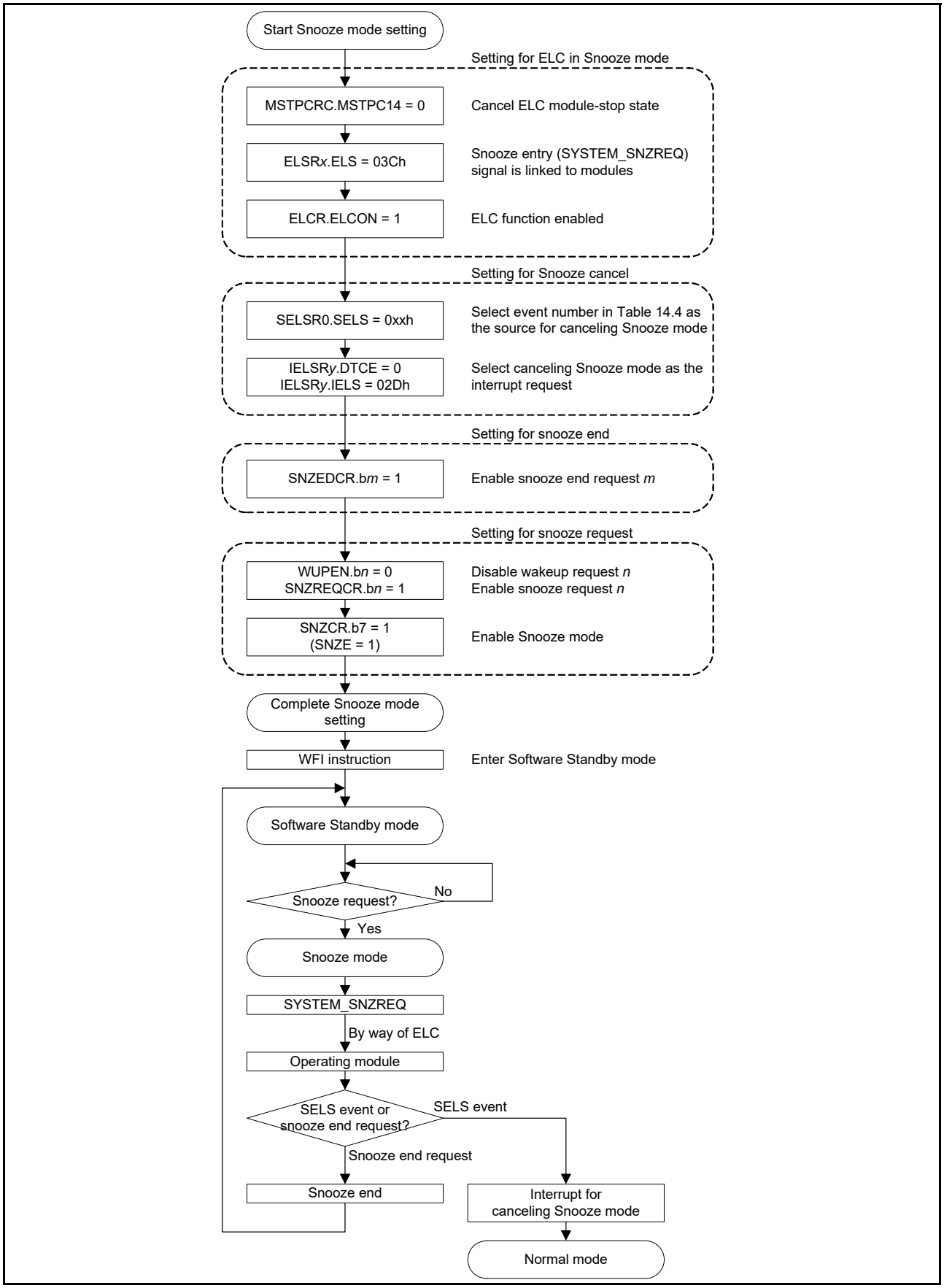


Figure 11.8 Setting example of using ELC in Snooze mode

The MCU can transmit and receive data in SCI0 asynchronous mode without CPU intervention. When using the SCI0 in Snooze mode, use either High-speed mode or Low-speed mode.

Do not use Subosc-speed mode. Table 11.10 shows the maximum transfer rate of SCI0 in Snooze mode.

Table 11.10 HOCO: ± 1.4% (Ta = -20 to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and TRCLK	HOCO frequency					
	LOCO is not operating			LOCO is operating		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			4800		
2						
4						
8						
16						
32	1200			2400		
64						

Figure 11.9 shows an example setting for using SCI0 in Snooze mode entry.

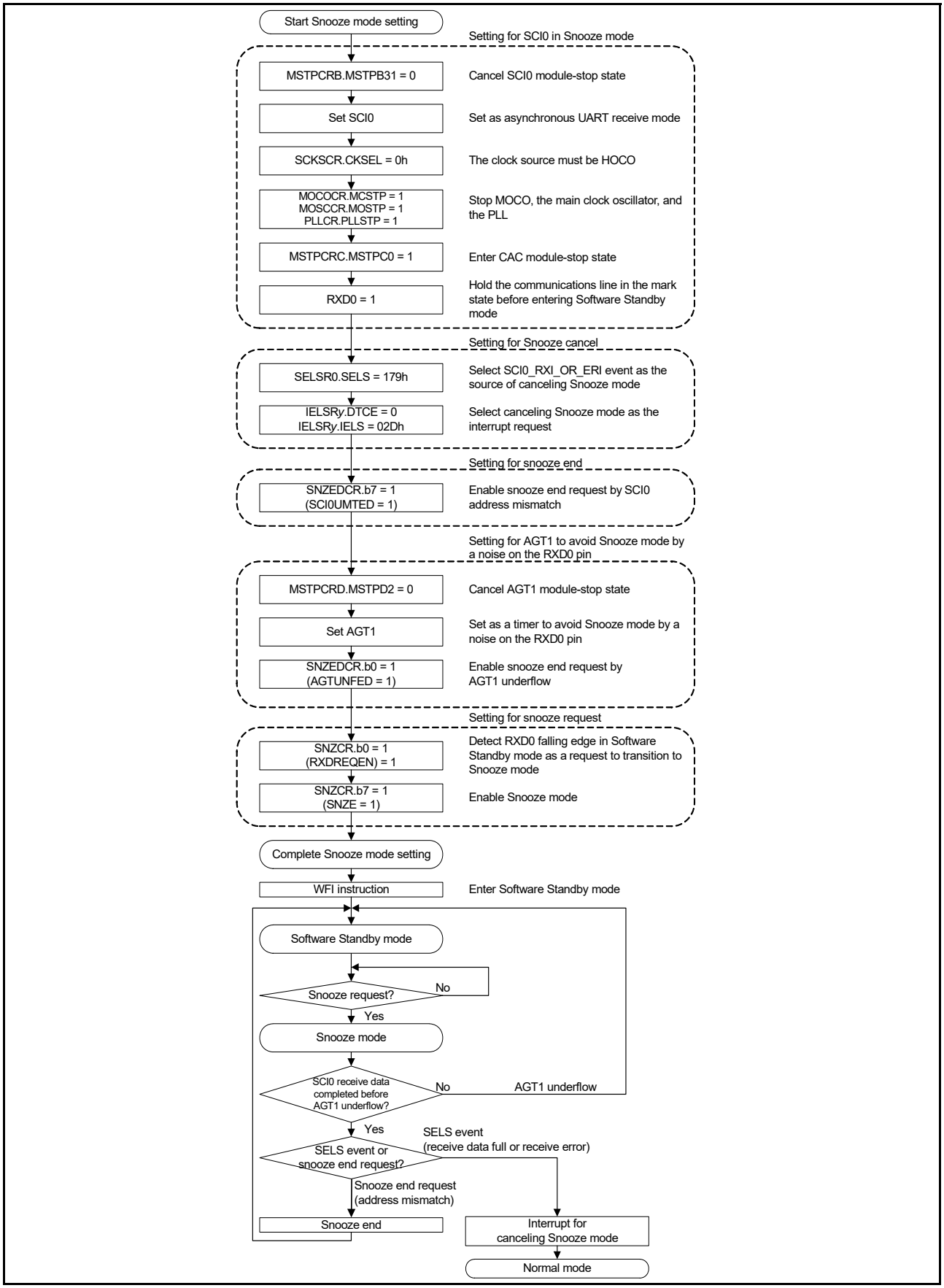


Figure 11.9 Setting example of using SCI0 in Snooze mode entry

11.9 Deep Software Standby Mode

11.9.1 Transitioning to Deep Software Standby Mode

The MCU enters Deep Software Standby mode when a WFI instruction is executed with the SBYCR.SSBY bit set to 1 and the DPSBYCR.DPSBY bit set to 1. See Table 11.6 for the settings of the related control bits.

In Deep Software Standby mode, the following modules are stopped:

- The CPU
- The on-chip peripheral functions
- The SRAM
- All oscillators, except for the sub-clock and low-speed on-chip oscillators.

Power consumption is reduced because the internal power supply to these modules is stopped. The contents of all CPU registers and internal peripheral modules become undefined.

If the setting in the DEEPCUT[1:0] bits is 11b, the internal power supply to the LVD is stopped, and the low power mode function of the power-on reset circuit is enabled. Therefore, power consumption is further reduced. For details, see section 43, Electrical Characteristics.

When the MCU enters Deep Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1, power supply to the IWDT-dedicated clock and the IWDT is cut off. Counting by the IWDT also stops.

When the OFS0.IWDTSTPCTL bit is 0, the MCU enters Software Standby mode instead of Deep Software Standby mode, regardless of the setting in the OFS0.IWDTSTRT or DPSBYCR.DPSBY bit. When the OFS0.IWDTSTPCTL bit is 0 while the OFS0.IWDTSTRT bit is 0 (auto start mode), the IWDT-dedicated clock and IWDT continue operation.

When the LVD1CR0.RI bit is 1 (voltage monitor 1 reset selected) or the LVD2CR0.RI bit is 1 (voltage monitor 2 reset selected), the MCU enters Software Standby mode instead of Deep Software Standby mode. The I/O port states are the same as in Software Standby mode.

When the PLL is selected as the clock source, set the following modules to the module-stop state before executing a WFI instruction:

- SCE7
- GPT32EH
- GPT32E.

In this case, you must also insert a wait time of at least 750 ns before executing the WFI instruction. The recommended method to measure the wait time is through software. Consider the worst-case conditions to ensure that the required wait time elapses.

Figure 11.2 shows an example flow for transitioning to Software Standby mode or Deep Software Standby mode.

Note 1. Conditions on the DTC, DMAC, and IWDT for transitioning to Software Standby mode must be met before the WFI instruction is executed. For details, see section 11.7, Software Standby Mode.

11.9.2 Canceling Deep Software Standby Mode

Deep Software Standby mode is canceled by:

- An interrupt shown in Table 11.3
- A RES pin reset
- A power-on reset
- A voltage monitor 0 reset.

The operations are as follows:

1. Canceling by an interrupt
   Canceling by interrupts is controlled by DPSIERn (n = 0 to 3) and DPSIFRn (n = 0 to 3). When an available

interrupt request is generated, the associated flag in DPSIFRn is set to 1. If the interrupt is enabled in DPSIERn, Deep Software Standby mode is canceled. Rising or falling edge detection can be selected in DPSIEGRn (n = 0 to 2). The detection edge can be selected for the NMI, IRQ0-DS, IRQ1-DS, IRQ4-DS to IRQ12-DS, voltage monitor 1, and voltage monitor 2 interrupts. When a Deep Software Standby mode canceling request occurs, internal power is supplied, the MOCO clock starts to oscillate, and an internal reset (deep software standby reset) is generated for the entire MCU. The stable MOCO clock is supplied to the entire MCU and deep software standby reset is canceled. The MCU starts reset exception handling.
When Deep Software Standby mode is canceled by an external interrupt pin or internal interrupt signal, the RSTSR0.DPSRSTF flag is set to 1.

2. Canceling by a RES pin reset
When the RES pin is driven low, the MCU cancels Deep Software Standby mode and enters a reset state. Make sure to keep the RES pin low for the time period specified in section 43, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts reset exception handling.

3. Canceling by a power-on reset
Deep Software Standby mode is canceled by a power-on reset, and the MCU starts reset exception handling.

4. Canceling by a voltage monitor 0 reset
Deep Software Standby mode is canceled by a voltage monitor 0 reset from the voltage detection circuit, and the MCU starts reset exception handling.

11.9.3 Pin States when Deep Software Standby Mode is Canceled

In Deep Software Standby mode, the I/O ports retain the same states from Software Standby mode. The MCU is initialized by an internal reset generated when Deep Software Standby mode is canceled, and reset exception handling starts immediately. The DPSBYCR.IOKEEP bit setting determines whether to initialize the I/O ports or to retain the I/O ports states for Software Standby mode. The following is the state of the I/O ports for each bit setting:

- When the DPSBYCR.IOKEEP bit = 0
The I/O ports are initialized by an internal reset generated when Deep Software Standby mode is canceled.
- When the DPSBYCR.IOKEEP bit = 1
Although the MCU is initialized by an internal reset generated when Deep Software Standby mode is canceled, the I/O ports retain their states from Software Standby mode regardless of the MCU internal state. The I/O ports states remain unchanged from Software Standby mode even when settings are made to the I/O ports or peripheral modules. The retained I/O ports states are released by clearing the DPSBYCR.IOKEEP bit to 0, and the MCU operates according to the internal state. The DPSBYCR.IOKEEP bit is not initialized by any internal reset generated when Deep Software Standby mode is canceled.

11.9.4 Example of Deep Software Standby Mode Application

(1) Entering and exiting Deep Software Standby mode

Figure 11.10 shows an example transition to Deep Software Standby mode on the falling edge of the IRQn-DS pin, and an exit from Deep Software Standby mode on the rising edge of the IRQn-DS pin. In this example, an IRQn interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 01b (falling edge). After the DPSIEGRy.DIRQnEG bit (y = 0, 1 and n = 0, 1, 4 to 12) is set to 1 (rising edge) and the SBYCR.SSBY and DPSBYCR.DPSBY bits are both set to 1, the WFI instruction is executed. As a result, the MCU transitions to Deep Software Standby mode. Deep Software Standby mode is then canceled on the rising edge of the IRQn-DS pin.

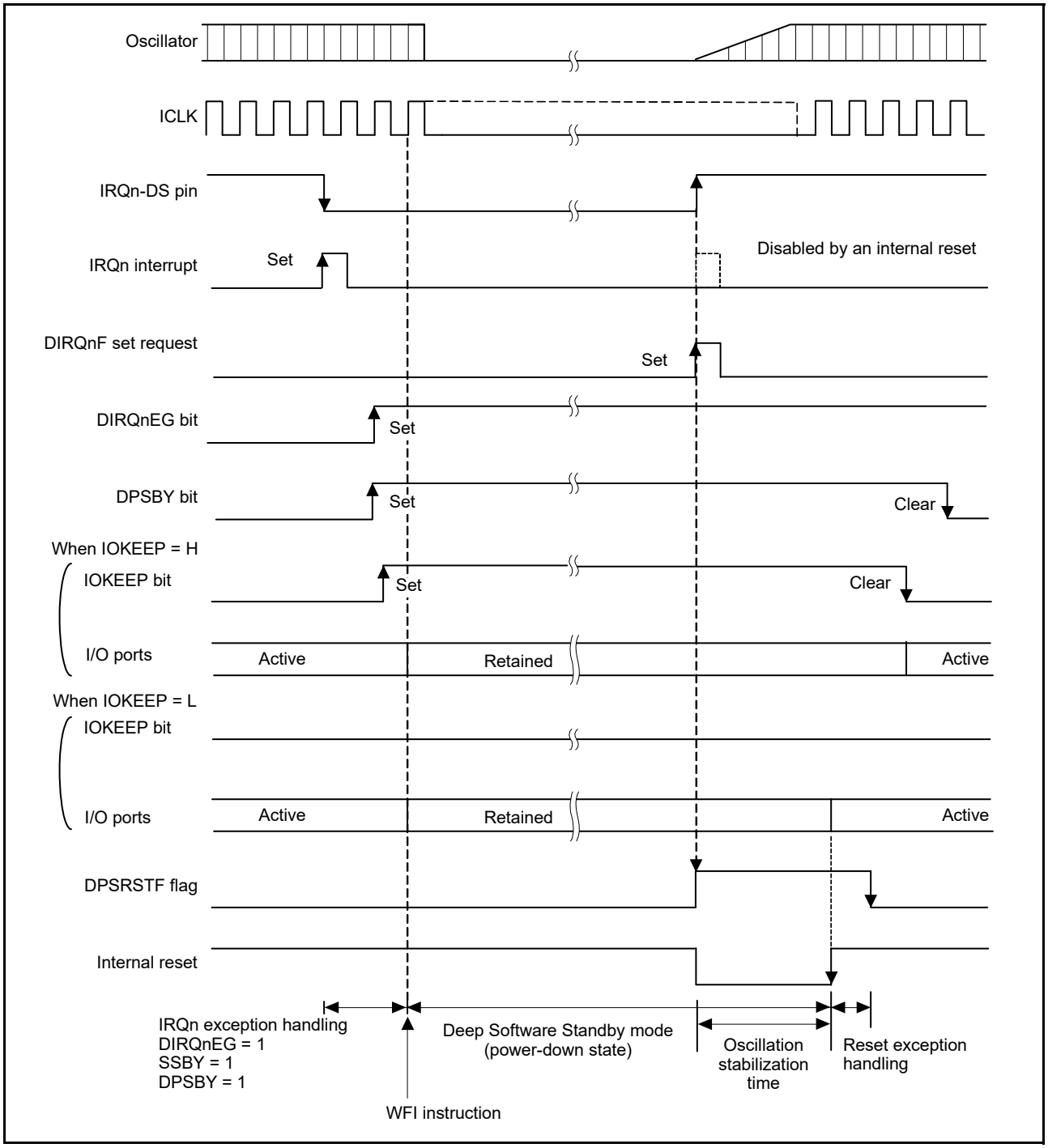


Figure 11.10 Example of Deep Software Standby mode application

11.9.5 Usage Flow for Deep Software Standby Mode

Figure 11.11 shows an example flow for using Deep Software Standby mode. In this example, the RSTSR0.DPSRSTF flag of the reset function is read after reset exception handling to determine whether the reset is generated by the RES pin or by the cancellation of Deep Software Standby mode. For a reset by the RES pin, the MCU transitions to Deep Software Standby mode after the required register settings are made. For a reset by cancellation of Deep Software Standby mode, the DPSBYCR.IOKEEP bit is set to 0 after the I/O port settings are made.

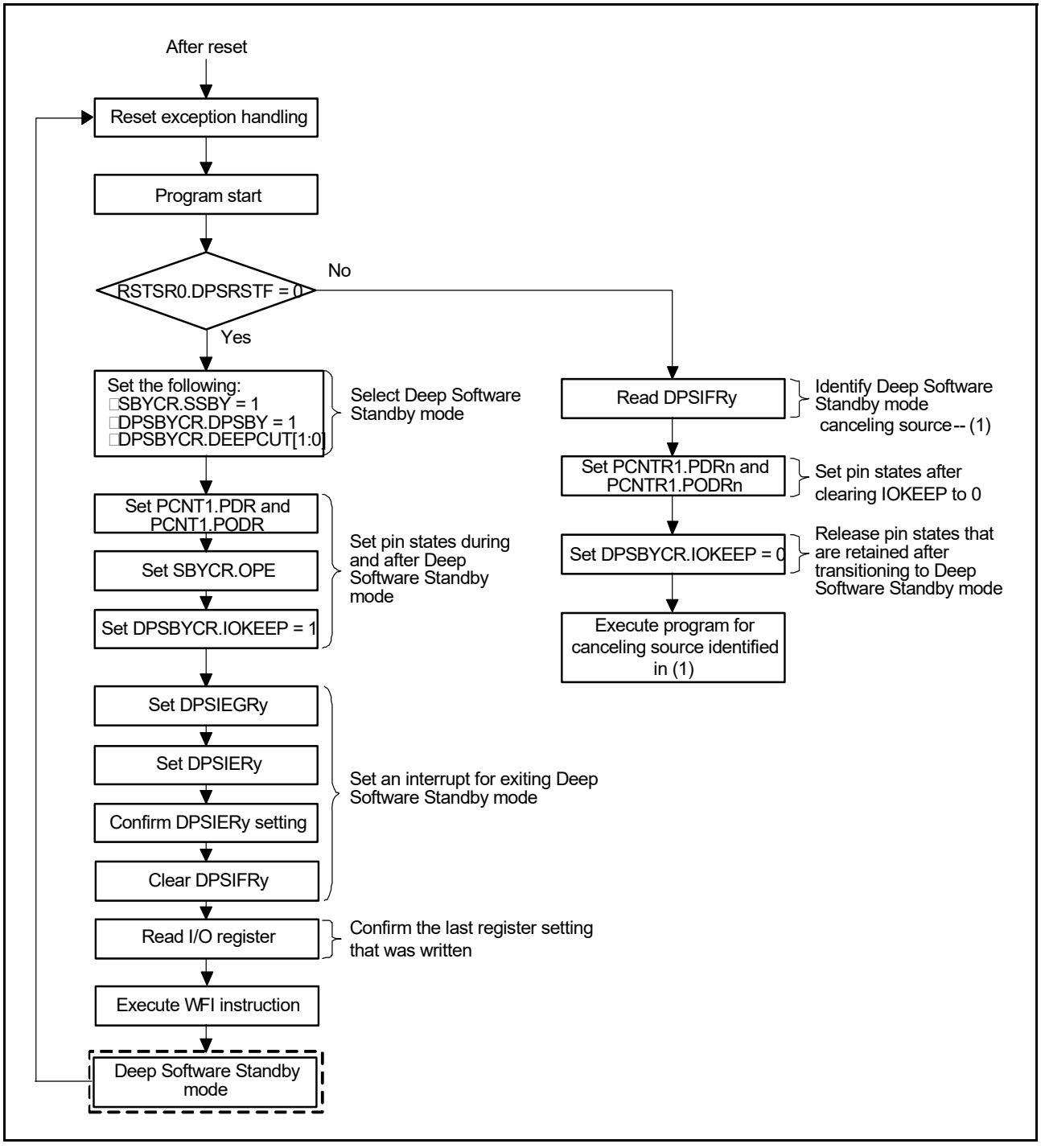


Figure 11.11 Example flow for using Deep Software Standby mode

11.10 Usage Notes

11.10.1 Register Access

(1) Invalid register write accesses during specific modes or transitions

Do not write to registers under any of the conditions listed in this section.

[Registers]

- All registers with a peripheral name of SYSTEM.

[Conditions]

- OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of the operating power control mode)
- During the time period from executing a WFI instruction to returning to Normal mode
- When FENTRYR.FENTRYi = 1 (i = 0 to 3) (flash P/E mode) or FENTRYR.FENTRYD = 1 (data flash P/E mode).

(2) Valid settings for the clock-related registers

Table 11.11 and Table 11.12 show the valid settings of the clock-related registers in each operating power control mode. Do not write any value other than the valid setting. Any other written value is ignored. Each register has certain prohibited settings under conditions other than those related to the operating power control modes. See section 9, Clock Generation Circuit, for these other conditions for each register.

Table 11.11 Valid settings for the clock-related registers (1)

Mode	Valid settings							
	SCKSCR.CKSEL[2:0], CKOCR.CKOSEL[2:0]	SCKDIVCR.FCK[2:0], ICK[2:0]	PLLCR.PLLSTP	HOCOCR. HCSTP	MOCOCR. MCSTP	LOCOCR. LCSTP	MOSCCR. MOSTP	SOSCCR. SOSTP
High-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub-clock) 101b (PLL)*1	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stop)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub-clock)		1 (stopped)					
Subosc-speed	010b (LOCO) 100b (Sub-clock)	000b (1/1)	1 (stopped)	1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)

Note 1. SCKSCR.CKSEL[2:0] only.

Table 11.12 Valid settings for the clock related registers (2)

Operating oscillator	Valid settings	
	OPCCR.OPCM[1:0]	SOPCCR.SOPCM
PLL	00b	0
High-speed on-chip oscillator	00b, 11b	0
Middle-speed on-chip oscillator		
Main clock oscillator		
Low-speed on-chip oscillator	00b, 11b	0, 1
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) Invalid register write accesses in subosc-speed mode

Do not write to registers under the listed condition in this section.

[Registers]

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(4) Invalid register write accesses by the DTC or DMAC

Do not write to registers listed in this section by the DTC or DMAC.

[Register]

- MSTPCRA.

(5) Invalid register write accesses in Snooze mode

Do not write to registers listed in this section in Snooze mode. They must be set before entering Software Standby mode.

[Registers]

- SNZCR, SNZEDCR, SNZREQCR.

(6) Invalid write access to FLWT.FLWT[2:0]

Do not write any value other than 000b to the FLWT.FLWT[2:0] bits under the listed condition.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode)

(7) Invalid write access when PRCR.PRC1 is 0

Do not write to registers listed in this section when the PRCR.PRC1 bit is 0.

[Registers]

- SBYCR, SNZCR, SNZEDCR, SNZREQCR, OPCCR, SOPCCR, DPSBYCR, DPSIERn (n = 0 to 3), DPSIFRn (n = 0 to 3), DPSIEGRn (n = 0 to 2), and SYOCDCR.

11.10.2 I/O Port States

The I/O port states in Software Standby, Deep Software Standby, and Snooze modes (except when modifying in Snooze mode) are the same before entering the modes. Therefore, power consumption is not reduced while the output signals are held high.

11.10.3 Module-Stop State of DMAC and DTC

Before writing 1 to MSTPCRA.MSTPA22, clear the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC to 0.

11.10.4 Internal Interrupt Sources

Interrupts do not operate in the module-stop state. If the module-stop bit is set when an interrupt request is generated, a CPU interrupt source or a DMAC or DTC startup source cannot be cleared. Always disable the associated interrupts before setting the module-stop bits.

11.10.5 Input Buffer Control by the DIRQnE Bit (n = 0, 1, 4 to 12)

Setting the DPSIERy.DIRQnE bit (y = 0, 1 and n = 0, 1, 4 to 12) to 1 enables the associated input buffer of the IRQ0-DS, IRQ1-DS, and IRQ4-DS to IRQ12-DS pins. Although inputs to these pins are sent to the DPSIFRy.DIRQnF bits (y = 0, 1 and n = 0, 1, 4 to 12), they are not sent to the ICU, peripheral modules, or I/O ports.

11.10.6 Transitioning to Low Power Modes

Because the MCU does not support wakeup by events, do not enter the low power modes (Sleep, Software Standby, or Deep Software Standby mode) by executing a WFE instruction. Also, do not set the SLEEPDEEP bit of the System Control Register in the Cortex®-M4 core, because the MCU does not support low power modes by SLEEPDEEP.

11.10.7 Timing of WFI Instruction

It is possible for the WFI instruction to be executed before I/O register writes are complete, in which case operation might not proceed as intended. This can happen if the WFI is placed immediately after a write to an I/O register. To avoid this problem, read back the register that was written to confirm that the write completed.

11.10.8 Writing to the WDT and IWDT Registers by the DMAC or DTC in Sleep Mode or Snooze Mode

Do not write to the WDT or IWDT registers by the DMAC or DTC while the WDT or IWDT is stopped after entering Sleep mode or Snooze mode.

11.10.9 Oscillators in Snooze Mode

Oscillators that stop on entering Software Standby mode automatically restart when a trigger for switching to Snooze mode is generated. The MCU does not enter Snooze mode until all of the oscillators stabilize. In Snooze mode, you must disable oscillators that are not required in Snooze mode before entering Software Standby mode. Otherwise, the transition from Software Standby mode to Snooze mode takes longer.

11.10.10 Snooze Mode Entry by RXD0 Falling Edge

When the SNZCR.RXDREQEN bit is 1, noise on the RXD0 pin might cause the MCU transition from Software Standby mode to Snooze mode. Any subsequent RXD0 data can be received in Snooze mode by noise on the RXD0 pin. If the MCU does not receive any RXD0 data after the noise, interrupts such as SCI0_ERI or SCI0_RXI, and address mismatch events are not generated, and the MCU stays in Snooze mode. To avoid this, an AGT1 underflow interrupt must be used to return to Software Standby mode or Normal mode when using SCI0 in Snooze mode. However, set AGT1 underflow not to be a source to return to Software Standby mode during an SCI communication. This makes the SCI0 stop the operation in a half-finished state.

11.10.11 Using SCI0 in Snooze Mode

When using SCI0 in Snooze mode, the AGT1 underflow must be used for the interrupt request or snooze end request. Do not use any other trigger.

When using SCI0 in Snooze mode, the following conditions must be satisfied:

- The clock source must be HOCO
- MOCO, the main clock oscillator, and the PLL must be stopped before entering Software Standby mode
- The RXD0 pin must be kept at the high level before entering Software Standby mode
- A transition to Software Standby mode must not occur during an SCI communication
- The MSTPCRC.MSTPC0 bit must be 1 before entering Software Standby mode.

11.10.12 Conditions of A/D Conversion Start in Snooze Mode

The ADC12 can only be triggered by the ELC in Snooze mode. Do not use a software trigger or ADTRGn pin.

11.10.13 ELC Events in Snooze Mode

Only the ELC events listed in this section are available in Snooze mode. Do not use any other events. If starting peripheral modules for the first time after entering Snooze mode, the Event Link Setting Register (ELSRn) must set a Snooze mode entry event (SYSTEM_SNZREQ) as the trigger.

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC12n Window A/B compare match (ADC12n_WCMPM) (n = 0, 1)
- ADC12n Window A/B compare mismatch (ADC12n_WCMPUM) (n = 0, 1)
- Data operation circuit interrupt (DOC_DOPCI).

12. Register Write Protection

12.1 Overview

The register write protection function protects important registers from being overwritten because of software errors. The registers to be protected are set with the Protect Register (PRCR).

Table 12.1 lists the association between the PRCR bits and the registers to be protected.

Table 12.1 Association between PRCR bits and registers to be protected

PRCR bit	Registers to be protected
PRC0	• Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, FLLCR1, FLLCR2.
PRC1	• Registers related to the low power modes: SBYCR, SNZCR, SNZEDCR, SNZREQCR, OPCCR, SOPCCR, DPSBYCR, DPSIER0-3, DPSIFR0-3, DPSIEGR0-2, SYOCDCR, STCONR • Registers related to the AGT function: VBTICTLR.
PRC3	• Registers related to the LVD: LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVCMPCR, LVDLVLR, LVD1CR0, LVD2CR0.

12.2 Register Descriptions

12.2.1 Protect Register (PRCR)

Address(es): SYSTEM.PRCR 4001 E3FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	PRC3	—	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Function	R/W
b0	PRC0	Protect Bit 0	Enable writing to the registers related to the clock generation circuit: 0: Disable writes 1: Enable writes.	R/W
b1	PRC1	Protect Bit 1	Enable writing to the registers related to the low power modes and the AGT function: 0: Disable writes 1: Enable writes.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	PRC3	Protect Bit 3	Enable writing to the registers related to the LVD: 0: Disable writes 1: Enable writes.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	PRC Key Code	These bits control write access to the PRCR register. To modify the PRCR register, write A5h to the upper 8 bits and the target value to the lower 8 bits as a 16-bit unit.	W*1

Note 1. Write data is not saved. Always reads 00h.

PRCn bits (Protect Bit n) (n = 0, 1, 3)

The PRCn bits enable or disable writing to the protected registers listed in Table 12.1. Setting PRCn to 1 or 0 enables or disables writing, respectively.

13. Interrupt Controller Unit (ICU)

13.1 Overview

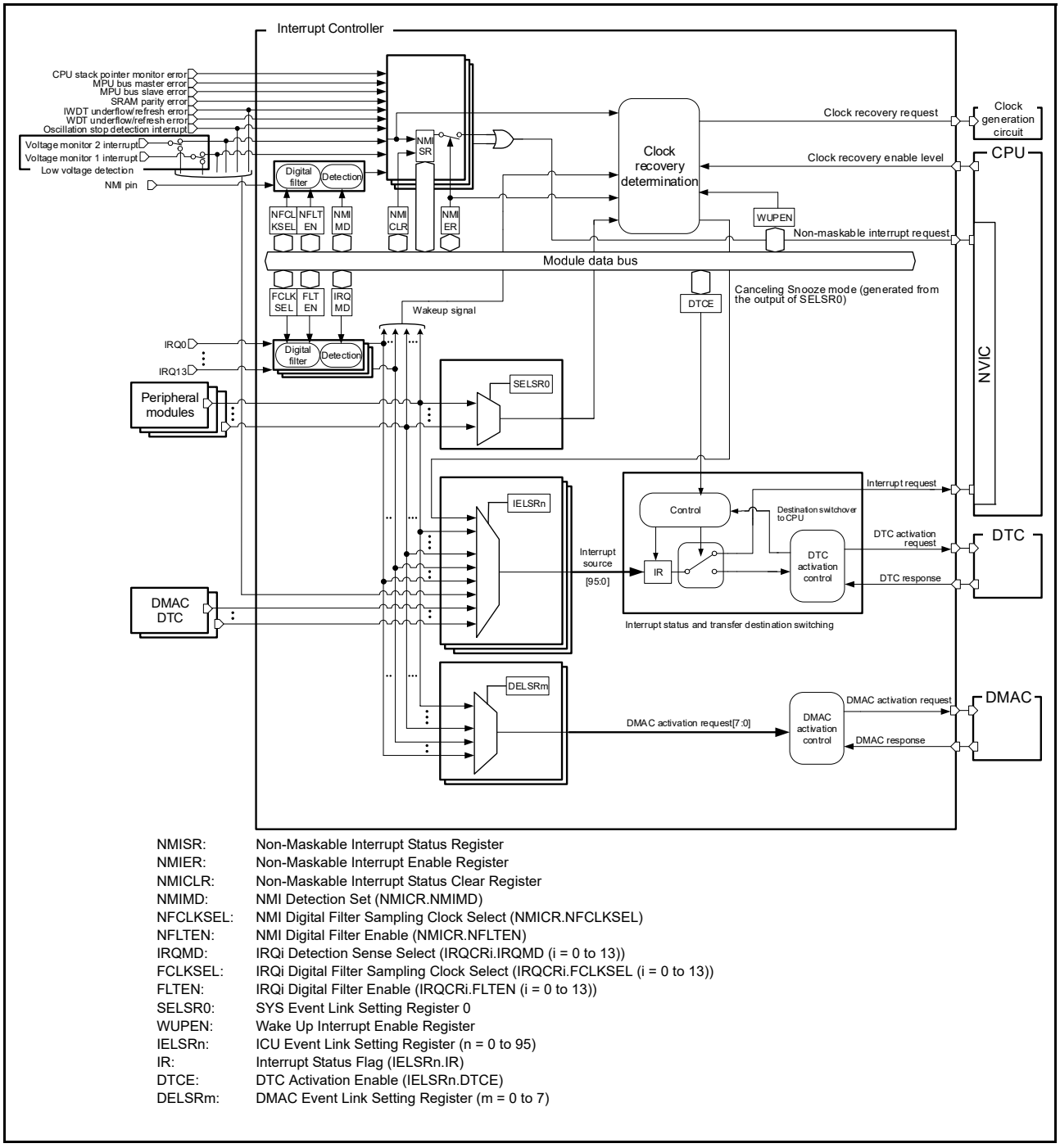
The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.

Table 13.1 lists the ICU specifications, Figure 13.1 shows a block diagram, and Table 13.2 lists the I/O pins.

Table 13.1 ICU specifications

Parameter		Specifications
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules Number of sources: 268 (select factors within event list numbers 64 to 511)
	External pin interrupts	• Interrupt detection on low level, falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source. • Digital filter function supported • 14 sources, with interrupts from IRQ0 to IRQ13 pins.
	DTC and DMAC control	The DTC and DMAC can be activated using interrupt sources*1
	Interrupt sources for NVIC	96 sources
Non-maskable interrupts*2	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge • Digital filter function supported.
	Oscillation stop detection interrupt*3	Interrupt on detecting that the main oscillator has stopped
	WDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	IWDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Voltage monitor 1 interrupt*3	Voltage monitor interrupt of low voltage detection detector 1 (LVD1)
	Voltage monitor 2 interrupt*3	Voltage monitor interrupt of low voltage detection detector 2 (LVD2)
	RPEST	Interrupt on SRAM parity error
	BUSSST	Interrupt on MPU bus slave error
	BUSMST	Interrupt on MPU bus master error
	SPEST	Interrupt on CPU stack pointer monitor
Return from low power mode*4		• Sleep mode: return is initiated by non-maskable interrupts or any other interrupt source • Software Standby mode: return is initiated by non-maskable interrupts. Interrupts can be selected in the WUPEN register*5. • Snooze mode: return is initiated by non-maskable interrupts. Interrupts can be selected in the SELSR0 and WUPEN registers*5.

Note 1. For the DTC and DMAC activation sources, see Table 13.4, Event table.
Note 2. Non-maskable interrupts can be enabled only once after a reset release.
Note 3. These non-maskable interrupts can also be used as event signals. When used as interrupts, do not change the value of the NMIER register from the reset state. To enable voltage monitor 1 and voltage monitor 2 interrupts, set the LVD1CR1.IRQSEL and LVD2CR1.IRQSEL bits to 1.
Note 4. For return from Deep Software Standby mode, see section 11.9, Deep Software Standby Mode.
Note 5. See section 13.2.8, SYS Event Link Setting Register (SELSR0), and section 13.2.9, Wake Up Interrupt Enable Register (WUPEN).



NMISR: Non-Maskable Interrupt Status Register
NMIER: Non-Maskable Interrupt Enable Register
NMICLR: Non-Maskable Interrupt Status Clear Register
NMIMD: NMI Detection Set (NMICR.NMIMD)
NFCLKSEL: NMI Digital Filter Sampling Clock Select (NMICR.NFCLKSEL)
NFLTEN: NMI Digital Filter Enable (NMICR.NFLTEN)
IRQMD: IRQi Detection Sense Select (IRQCRi.IRQMD (i = 0 to 13))
FCLKSEL: IRQi Digital Filter Sampling Clock Select (IRQCRi.FCLKSEL (i = 0 to 13))
FLTEN: IRQi Digital Filter Enable (IRQCRi.FLTEN (i = 0 to 13))
SELSR0: SYS Event Link Setting Register 0
WUPEN: Wake Up Interrupt Enable Register
IELSRn: ICU Event Link Setting Register (n = 0 to 95)
IR: Interrupt Status Flag (IELSRn.IR)
DTCE: DTC Activation Enable (IELSRn.DTCE)
DELSRm: DMAC Event Link Setting Register (m = 0 to 7)

Figure 13.1 ICU block diagram

Table 13.2 lists the ICU input/output pins.

Table 13.2 ICU I/O pins

Pin name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQ0 to IRQ13	Input	External interrupt request pins

13.2 Register Descriptions

This chapter does not describe the Arm® NVIC internal registers. For information on these registers, see the *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D).

13.2.1 IRQ Control Register i (IRQCRi) (i = 0 to 13)

Address(es): ICU.IRQCR0 4000 6000h, ICU.IRQCR1 4000 6001h, ICU.IRQCR2 4000 6002h, ICU.IRQCR3 4000 6003h, ICU.IRQCR4 4000 6004h, ICU.IRQCR5 4000 6005h, ICU.IRQCR6 4000 6006h, ICU.IRQCR7 4000 6007h ICU.IRQCR8 4000 6008h, ICU.IRQCR9 4000 6009h, ICU.IRQCR10 4000 600Ah, ICU.IRQCR11 4000 600Bh, ICU.IRQCR12 4000 600Ch, ICU.IRQCR13 4000 600Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	IRQMD[1:0]	IRQi Detection Sense Select	b1 b0 0 0: Falling edge 0 1: Rising edge 1 0: Rising and falling edges 1 1: Low level.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	FCLKSEL[1:0]	IRQi Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	FLTEN	IRQi Digital Filter Enable	0: Disable 1: Enable.	R/W

IRQCRi register changes must satisfy the following conditions:

- For a CPU interrupt or DTC trigger:
  Change the IRQCRi register setting before setting the target IELSRn register (n = 0 to 95).
  You can only change the register values when the target IELSRn register is 0000h.
- For a DMAC trigger:
  Change the IRQCRi register setting before setting the target DELSRn register (n = 0 to 7).
  You can change the register values only when the DELSRn.DELS[8:0] bits are 000h.
- For a wakeup enable signal:
  Change the IRQCRi register setting before setting the target WUPEN.IRQWUPEN[n] (n = 0 to 13).
  You can change the register values only when the target WUPEN.IRQWUPEN[n] is 000h.

IRQMD[1:0] bits (IRQi Detection Sense Select)

The IRQMD[1:0] bits set the detection sensing method for the IRQi external pin interrupt sources. For more information on the settings, see section 13.4.4, External Pin Interrupts.

FCLKSEL[1:0] bits (IRQi Digital Filter Sampling Clock Select)

The FCLKSEL[1:0] bits select the digital filter sampling clock for the external pin interrupt request IRQi, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

For details on the digital filter, see section 13.4.3, Digital Filter.

FLTEN bit (IRQi Digital Filter Enable)

The FLTEN bit enables the digital filter used for the IRQi external pin interrupt sources. The filter is enabled when FLTEN is 1 and disabled when FLTEN is 0. The IRQi pin level is sampled at the clock cycle specified in the FCLKSEL[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes. For details on the digital filter, see section 13.4.3, Digital Filter.

13.2.2 Non-Maskable Interrupt Status Register (NMISR)

Address(es): ICU.NMISR 4000 6140h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEST	BUSMST	BUSSST	—	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTST	IWDT Underflow/Refresh Error Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b1	WDTST	WDT Underflow/Refresh Error Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b2	LVD1ST	Voltage Monitor 1 Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b3	LVD2ST	Voltage Monitor 2 Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b5, b4	—	Reserved	These bits are read as 0.	R
b6	OSTST	Oscillation Stop Detection Interrupt Status Flag	0: Interrupt not requested for main oscillation stop 1: Interrupt requested for main oscillation stop.	R
b7	NMIST	NMI Status Flag	0: NMI pin interrupt not requested 1: NMI pin interrupt requested.	R
b8	RPEST	SRAM Parity Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b9	—	Reserved	This bit is read as 0.	R
b10	BUSSST	MPU Bus Slave Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b11	BUSMST	MPU Bus Master Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b12	SPEST	CPU Stack Pointer Monitor Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b15 to b13	—	Reserved	These bits are read as 0.	R

The NMISR register monitors the status of non-maskable interrupt sources. Writes to the NMISR register are ignored. The setting in the Non-Maskable Interrupt Enable Register (NMIER) does not affect the status flags in this register. Before the end of the non-maskable interrupt handler, check that all of the bits in this register are set to 0 to confirm that no other NMI requests have occurred during handler processing.

IWDTST flag (IWDT Underflow/Refresh Error Status Flag)

The IWDTST flag indicates an IWDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.IWDTCLR bit.

[Setting condition]

- When an IWDT underflow/refresh error interrupt occurs and this interrupt source is enabled.

[Clearing condition]

- When 1 is written to the NMICLR.IWDTCLR bit.

WDTST flag (WDT Underflow/Refresh Error Status Flag)

The WDTST flag indicates a WDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.WDTCLR bit.

[Setting condition]

- When a WDT underflow/refresh error interrupt occurs.

[Clearing condition]

- When 1 is written to the NMICLR.WDTCLR bit.

LVD1ST flag (Voltage Monitor 1 Interrupt Status Flag)

The LVD1ST flag indicates a request for voltage monitor 1 interrupt. It is read-only and cleared by the NMICLR.LVD1CLR bit.

[Setting condition]

- When a voltage monitor 1 interrupt occurs and this interrupt source is enabled.

[Clearing condition]

- When 1 is written to the NMICLR.LVD1CLR bit.

LVD2ST flag (Voltage Monitor 2 Interrupt Status Flag)

The LVD2ST flag indicates a request for voltage monitor 2 interrupt. It is read-only and cleared by the NMICLR.LVD2CLR bit.

[Setting condition]

- When a voltage monitor 2 interrupt occurs and this interrupt source is enabled.

[Clearing condition]

- When 1 is written to the NMICLR.LVD2CLR bit.

OSTST flag (Oscillation Stop Detection Interrupt Status Flag)

The OSTST flag indicates a main oscillation stop detection interrupt request. It is read-only and cleared by the NMICLR.OSTCLR bit.

[Setting condition]

- When an oscillation stop detection interrupt occurs.

[Clearing condition]

- When 1 is written to the NMICLR.OSTCLR bit.

NMIST flag (NMI Status Flag)

The NMIST flag indicates an NMI pin interrupt request. It is read-only and cleared by the NMICLR.NMICLR bit.

[Setting condition]

- When an edge specified in the NMICR.NMIMD bit is input to the NMI pin.

[Clearing condition]

- When 1 is written to the NMICLR.NMICLR bit.

RPEST flag (SRAM Parity Error Interrupt Status Flag)

The RPEST flag indicates an SRAM parity error interrupt request.

[Setting condition]

- When an interrupt occurs in response to an SRAM parity error.

[Clearing condition]

- When 1 is written to the NMICLR.RPECLR bit.

BUSSST flag (MPU Bus Slave Error Interrupt Status Flag)

The BUSSST flag indicates a bus slave error interrupt request.

[Setting condition]

- When an interrupt occurs in response to a bus slave error.

[Clearing condition]

- When 1 is written to the NMICLR.BUSSCLR bit.

BUSMST flag (MPU Bus Master Error Interrupt Status Flag)

The BUSMST flag indicates a bus master error interrupt request.

[Setting condition]

- When an interrupt occurs in response to a bus master error.

[Clearing condition]

- When 1 is written to the NMICLR.BUSMCLR bit.

SPEST flag (CPU Stack Pointer Monitor Interrupt Status Flag)

The SPEST flag indicates a CPU stack pointer monitor interrupt request.

[Setting condition]

- When an interrupt occurs in response to a CPU stack pointer monitor error.

[Clearing condition]

- When 1 is written to the NMICLR.SPECLR bit.

13.2.3 Non-Maskable Interrupt Enable Register (NMIER)

Address(es): ICU.NMIER 4000 6120h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEEN	BUSMEN	BUSSEN	—	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTEN	IWDT Underflow/Refresh Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b1	WDTEN	WDT Underflow/Refresh Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b2	LVD1EN	Voltage Monitor 1 Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b3	LVD2EN	Voltage Monitor 2 Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	OSTEN	Oscillation Stop Detection Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b7	NMIEN	NMI Pin Interrupt Enable	0: Disable 1: Enable.	R/(W) *1
b8	RPEEN	SRAM Parity Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b10	BUSSEN	MPU Bus Slave Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b11	BUSMEN	MPU Bus Master Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b12	SPEEN	CPU Stack Pointer Monitor Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. You can write 1 to this bit only once after reset. Subsequent write accesses are invalid. Writing 0 to this bit is invalid.
Note 2. Do not write 1 to this bit when the source is used as an event signal.

IWDTEN bit (IWDT Underflow/Refresh Error Interrupt Enable)

The IWDTEN bit enables IWDT underflow/refresh error interrupts as an NMI trigger.

WDTEN bit (WDT Underflow/Refresh Error Interrupt Enable)

The WDTEN bit enables WDT underflow/refresh error interrupts as an NMI trigger.

LVD1EN bit (Voltage Monitor 1 Interrupt Enable)

The LVD1EN bit enables voltage monitor 1 interrupts as an NMI trigger.

LVD2EN bit (Voltage Monitor 2 Interrupt Enable)

The LVD2EN bit enables voltage monitor 2 interrupts as an NMI trigger.

OSTEN bit (Oscillation Stop Detection Interrupt Enable)

The OSTEN bit enables main oscillation stop detection interrupt as an NMI trigger.

NMIEN bit (NMI Pin Interrupt Enable)

The NMIEN bit enables NMI pin interrupt as an NMI trigger.

RPEEN bit (SRAM Parity Error Interrupt Enable)

The RPEEN bit enables SRAM parity error interrupt as an NMI trigger.

BUSSEN bit (MPU Bus Slave Error Interrupt Enable)

The BUSSEN bit enables bus slave error interrupt as an NMI trigger.

BUSMEN bit (MPU Bus Master Error Interrupt Enable)

The BUSMEN bit enables bus master error interrupt as an NMI trigger.

SPEEN bit (CPU Stack Pointer Monitor Interrupt Enable)

The SPEEN bit enables CPU stack pointer monitor interrupt as an NMI trigger.

13.2.4 Non-Maskable Interrupt Status Clear Register (NMICLR)

Address(es): ICU.NMICLR 4000 6130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPECLR	BUSMCLR	BUSSCLR	—	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTCLR	IWDT Clear	0: No effect 1: Clear the NMISR.IWDTST flag.	R/(W)*1

Bit	Symbol	Bit name	Description	R/W
b1	WDTCLR	WDT Clear	0: No effect 1: Clear the NMISR.WDTST flag.	R/(W)*1
b2	LVD1CLR	LVD1 Clear	0: No effect 1: Clear the NMISR.LVD1ST flag.	R/(W)*1
b3	LVD2CLR	LVD2 Clear	0: No effect 1: Clear the NMISR.LVD2ST flag.	R/(W)*1
b5, b4	—	Reserved	The write value should be 0.	R/(W)
b6	OSTCLR	OST Clear	0: No effect 1: Clear the NMISR.OSTST flag.	R/(W)*1
b7	NMICLR	NMI Clear	0: No effect 1: Clear the NMISR.NMIST flag.	R/(W)*1
b8	RPECLR	SRAM Parity Error Clear	0: No effect 1: Clear the NMISR.RPEST flag.	R/(W)*1
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	BUSSCLR	Bus Slave Error Clear	0: No effect 1: Clear the NMISR.BUSSST flag.	R/(W)*1
b11	BUSMCLR	Bus Master Error Clear	0: No effect 1: Clear the NMISR.BUSMST flag.	R/(W)*1
b12	SPECLR	SPEST Clear	0: No effect 1: Clear the NMISR.SPEST flag.	R/(W)*1
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/(W)

Note 1. Only write 1 to this bit.

IWDTCLR bit (IWDT Clear)

Writing 1 to the IWDTCLR bit clears the NMISR.IWDTST flag. This bit is read as 0.

WDTCLR bit (WDT Clear)

Writing 1 to the WDTCLR bit clears the NMISR.WDTST flag. This bit is read as 0.

LVD1CLR bit (LVD1 Clear)

Writing 1 to the LVD1CLR bit clears the NMISR.LVD1ST flag. This bit is read as 0.

LVD2CLR bit (LVD2 Clear)

Writing 1 to the LVD2CLR bit clears the NMISR.LVD2ST flag. This bit is read as 0.

OSTCLR bit (OST Clear)

Writing 1 to the OSTCLR bit clears the NMISR.OSTST flag. This bit is read as 0.

NMICLR bit (NMI Clear)

Writing 1 to the NMICLR bit clears the NMISR.NMIST flag. This bit is read as 0.

RPECLR bit (SRAM Parity Error Clear)

Writing 1 to the RPECLR bit clears the NMISR.RPEST flag. This bit is read as 0.

BUSSCLR bit (Bus Slave Error Clear)

Writing 1 to the BUSSCLR bit clears the NMISR.BUSSST flag. This bit is read as 0.

BUSMCLR bit (Bus Master Error Clear)

Writing 1 to the BUSMCLR bit clears the NMISR.BUSMSST flag. This bit is read as 0.

SPECLR bit (SPEST Clear)

Writing 1 to the SPECLR bit clears the NMISR.SPEST flag. This bit is read as 0.

13.2.5 NMI Pin Interrupt Control Register (NMICR)

Address(es): ICU.NMICR 4000 6100h

	b7	b6	b5	b4	b3	b2	b1	b0
	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	NFLTEN	NMI Digital Filter Enable	0: Disable 1: Enable.	R/W

Change the NMICR register settings before enabling NMI pin interrupts, that is, before setting NMIER.NMIEN to 1.

NMIMD bit (NMI Detection Set)

The NMIMD bit selects the detection sensing method for the NMI pin interrupts.

NFCLKSEL[1:0] bits (NMI Digital Filter Sampling Clock Select)

The NFCLKSEL[1:0] bits select the digital filter sampling clock for the NMI pin interrupts, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

For details of the digital filter, see section 13.4.3, Digital Filter.

NFLTEN bit (NMI Digital Filter Enable)

The NFLTEN bit enables the digital filter used for NMI pin interrupts. The filter is enabled when NFLTEN is 1, and disabled when NFLTEN is 0. The NMI pin level is sampled at the clock cycle specified in NMIFLTC.NFCLKSEL[1:0]. When the sampled level matches three times, the output level from the digital filter changes. For details of the digital filter, see section 13.4.3, Digital Filter.

13.2.6 ICU Event Link Setting Register n (IELSRn) (n = 0 to 95)

Address(es): ICU.IELSR0 4000 6300h, ICU.IELSR1 4000 6304h, ICU.IELSR2 4000 6308h, ICU.IELSR3 4000 630Ch.....
.....ICU.IELSR92 4000 6470h, ICU.IELSR93 4000 6474h, ICU.IELSR94 4000 6478h, ICU.IELSR95 4000 647Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	IELS[8:0]	ICU Event Link Select	b8 b0 000000000:Disable interrupts to the associated NVIC or DTC module 000000001 to 111111111:Event signal number to be linked. For details, see Table 13.4.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	IR	Interrupt Status Flag	0: No interrupt request occurred 1: Interrupt request occurred.	R/(W)*1
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	DTCE	DTC Activation Enable	0: Disable 1: Enable.	R/W
b31 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This register requires halfword or word access.
Note 1. Writing 1 to the IR flag is prohibited.

The IELSRn register selects the IRQ source used by the NVIC. For details, see Table 13.4. IELSRn corresponds to the NVIC IRQ input source number, where n = 0 to 95.

IELS[8:0] bits (ICU Event Link Select)

The IELS[8:0] bits link an event signal to the associated NVIC or DTC module. All IELS[8:0] bits must be written to simultaneously.

IR flag (Interrupt Status Flag)

The IR flag indicates an individual interrupt request from the event specified in IELS[8:0].

[Setting condition]

- When an interrupt request is received from the associated peripheral module or IRQi pin.

[Clearing conditions]

- When 0 is written to the flag. DTCE must be set to 0 before writing 0 to the IR flag.

To clear the IR flag:

1. Negate the input interrupt signal.
2. Read access the peripheral once and wait for 2 clock cycles of the target module clock.
3. Clear the IR flag by writing 0.

DTCE bit (DTC Activation Enable)

When the DTCE bit is set to 1, the associated event is selected as the source for DTC activation.

[Setting condition]

- When 1 is written to the DTCE bit.

[Clearing conditions]

- When the specified number of transfers is complete. For chain transfers, when the specified number of transfers for the last chain transfer is complete
- When 0 is written to the bit.

13.2.7 DMAC Event Link Setting Register n (DELSRn) (n = 0 to 7)

Address(es): ICU.DELSR0 4000 6280h, ICU.DELSR1 4000 6284h, ICU.DELSR2 4000 6288h, ICU.DELSR3 4000 628Ch, ICU.DELSR4 4000 6290h, ICU.DELSR5 4000 6294h, ICU.DELSR6 4000 6298h, ICU.DELSR7 4000 629Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	DELS[8:0]	DMAC Event Link Select	b8 b0 000000000:Disable DMA start requests to the associated DMAC module 000000001 to 111111111:Event signal number to be linked. For details, see Table 13.4.	R/W*1
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	IR	Interrupt Status Flag for DMAC	0: No interrupt request is generated 1: An interrupt request is generated.	R/(W)*2
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This register requires halfword or word access.
Note 2. Writing 1 to the IR flag is prohibited.

DELS[8:0] bits (DMAC Event Link Select)

The DELS[8:0] bits link an event signal to the DMAC module. All DELS[8:0] bits must be written to simultaneously.

IR flag (Interrupt Status Flag for DMAC)

The IR flag is the status flag of an individual DMA transfer request. This flag corresponds to DELS[8:0] bits of the same register.

[Setting condition]

- The flag is set to 1 when a DMA transfer request is generated from the corresponding peripheral module or IRQi pin.

[Clearing conditions]

- When 0 is written to the flag
- At the start of a DMA transfer after the DMA transfer request is issued.

13.2.8 SYS Event Link Setting Register (SELSR0)

Address(es): ICU.SELSR0 4000 6200h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	SELS[8:0]	SYS Event Link Select	b8 b0 000000000:Disable event output to the associated low-power mode module 000000001 to 111111111:Event signal number to be linked. For details, see Table 13.4.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This register requires halfword access.

The SELSR0 register selects the events that wake up the CPU from Snooze mode. You can only use the events listed in Table 13.4 checked for Canceling Snooze using SELSR0. Events specified in this register are defined as ICU_SNZCANCEL (02Dh) in Table 13.4. When 02Dh is set in IELSRn.IELS, the SELSR0 event interrupt occurs.

SELS[8:0] bits (SYS Event Link Select)

All SELS[8:0] bits must be written to simultaneously.

13.2.9 Wake Up Interrupt Enable Register (WUPEN)

Address(es): ICU.WUPEN 4000 61A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	—	—	—	—	—	ACMPHS0WUPEN	—	—	LVD2WUPEN	LVD1WUPEN	KEYWUPEN	IWDTWUPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IRQWUPEN[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	IRQWUPEN[13:0]	IRQ Interrupt Software Standby Returns Enable	0: Disable software standby returns by IRQ interrupt 1: Enable software standby returns by IRQ interrupt.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	IWDTWUPEN	IWDT Interrupt Software Standby Returns Enable	0: Disable software standby returns by IWDT interrupt 1: Enable software standby returns by IWDT interrupt.	R/W
b17	KEYWUPEN	Key Interrupt Software Standby Returns Enable	0: Disable software standby returns by KEY interrupt 1: Enable software standby returns by KEY interrupt.	R/W
b18	LVD1WUPEN	LVD1 Interrupt Software Standby Returns Enable	0: Disable software standby returns by LVD1 interrupt 1: Enable software standby returns by LVD1 interrupt.	R/W
b19	LVD2WUPEN	LVD2 Interrupt Software Standby Returns Enable	0: Disable software standby returns by LVD2 interrupt 1: Enable software standby returns by LVD2 interrupt.	R/W
b21, b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b22	ACMPHS0WUPEN	ACMPHS0 Interrupt Software Standby Returns Enable	0: Disable software standby returns by ACMPHS0 interrupt 1: Enable software standby returns by ACMPHS0 interrupt.	R/W
b27 to b23	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	AGT1UDWUPEN	AGT1 Underflow Interrupt Software Standby Returns Enable	0: Disable software standby returns by AGT1 underflow interrupt 1: Enable software standby returns by AGT1 underflow interrupt.	R/W
b29	AGT1CAWUPEN	AGT1 Compare Match A Interrupt Software Standby Returns Enable	0: Disable software standby returns by AGT1 compare match A interrupt 1: Enable software standby returns by AGT1 compare match A interrupt.	R/W
b30	AGT1CBWUPEN	AGT1 Compare Match B Interrupt Software Standby Returns Enable	0: Disable software standby returns by AGT1 compare match B interrupt 1: Enable software standby returns by AGT1 compare match B interrupt.	R/W
b31	IIC0WUPEN	IIC0 Address Match Interrupt Software Standby Returns Enable	0: Disable software standby returns by IIC0 address match interrupt 1: Enable software standby returns by IIC0 address match interrupt	R/W

The bits in this register control whether the associated interrupt can wake up the CPU from Software Standby mode.

IRQWUPEN[13:0] bits (IRQ Interrupt Software Standby Returns Enable)

The IRQWUPEN[13:0] bits enable the use of IRQn interrupts to cancel Software Standby mode.

IWDTWUPEN bit (IWDT Interrupt Software Standby Returns Enable)

The IWDTWUPEN bit enables the use of IWDT interrupts to cancel Software Standby mode.

KEYWUPEN bit (Key Interrupt Software Standby Returns Enable)

The KEYWUPEN bit enables the use of key interrupts to cancel Software Standby mode.

LVD1WUPEN bit (LVD1 Interrupt Software Standby Returns Enable)

The LVD1WUPEN bit enables the use of LVD1 interrupts to cancel Software Standby mode.

LVD2WUPEN bit (LVD2 Interrupt Software Standby Returns Enable)

The LVD2WUPEN bit enables the use of LVD2 interrupts to cancel Software Standby mode.

ACMPHS0WUPEN bit (ACMPHS0 Interrupt Software Standby Returns Enable)

The ACMPHS0WUPEN bit enables the use of ACMPHS0 interrupts to cancel Software Standby mode.

AGT1UDWUPEN bit (AGT1 Underflow Interrupt Software Standby Returns Enable)

The AGT1UDWUPEN bit enables the use of AGT1 underflow interrupts to cancel Software Standby mode.

AGT1CAWUPEN bit (AGT1 Compare Match A Interrupt Software Standby Returns Enable)

The AGT1CAWUPEN bit enables the use of AGT1 compare match A interrupts to cancel Software Standby mode.

AGT1CBWUPEN bit (AGT1 Compare Match B Interrupt Software Standby Returns Enable)

The AGT1CBWUPEN bit enables the use of AGT1 compare match B interrupts to cancel Software Standby mode.

IIC0WUPEN bit (IIC0 Address Match Interrupt Software Standby Returns Enable)

The IIC0WUPEN bit enables the use of IIC0 interrupts to cancel Software Standby mode.

13.3 Vector Table

The ICU detects maskable and non-maskable interrupts. Interrupt priorities are set up in the Arm NVIC. See the NVIC

chapter of the *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D).

13.3.1 Interrupt Vector Table

Table 13.3 describes the interrupt vectors. The interrupt vector addresses conform to the NVIC specifications.

Table 13.3 Interrupt vector table (1 of 3)

Exception number	IRQ number	Vector offset	Source	Description
0	-	000h	Arm	Initial stack pointer
1	-	004h	Arm	Initial program counter (reset vector)
2	-	008h	Arm	Non-maskable interrupt (NMI)
3	-	00Ch	Arm	Hard fault
4	-	010h	Arm	MemManage fault
5	-	014h	Arm	Bus fault
6	-	018h	Arm	Usage fault
7	-	01Ch	Arm	Reserved
8	-	020h	Arm	Reserved
9	-	024h	Arm	Reserved
10	-	028h	Arm	Reserved
11	-	02Ch	Arm	Supervisor call (SVCall)
12	-	030h	Arm	Debug Monitor
13	-	034h	Arm	Reserved
14	-	038h	Arm	Pendable request for system service (PendableSrvReq)
15	-	03Ch	Arm	System Tick timer (SysTick)
16	0	040h	ICU.IELSR0	Event selected in the ICU.IELSR0 register
17	1	044h	ICU.IELSR1	Event selected in the ICU.IELSR1 register
18	2	048h	ICU.IELSR2	Event selected in the ICU.IELSR2 register
19	3	04Ch	ICU.IELSR3	Event selected in the ICU.IELSR3 register
20	4	050h	ICU.IELSR4	Event selected in the ICU.IELSR4 register
21	5	054h	ICU.IELSR5	Event selected in the ICU.IELSR5 register
22	6	058h	ICU.IELSR6	Event selected in the ICU.IELSR6 register
23	7	05Ch	ICU.IELSR7	Event selected in the ICU.IELSR7 register
24	8	060h	ICU.IELSR8	Event selected in the ICU.IELSR8 register
25	9	064h	ICU.IELSR9	Event selected in the ICU.IELSR9 register
26	10	068h	ICU.IELSR10	Event selected in the ICU.IELSR10 register
27	11	06Ch	ICU.IELSR11	Event selected in the ICU.IELSR11 register
28	12	070h	ICU.IELSR12	Event selected in the ICU.IELSR12 register
29	13	074h	ICU.IELSR13	Event selected in the ICU.IELSR13 register
30	14	078h	ICU.IELSR14	Event selected in the ICU.IELSR14 register
31	15	07Ch	ICU.IELSR15	Event selected in the ICU.IELSR15 register
32	16	080h	ICU.IELSR16	Event selected in the ICU.IELSR16 register
33	17	084h	ICU.IELSR17	Event selected in the ICU.IELSR17 register
34	18	088h	ICU.IELSR18	Event selected in the ICU.IELSR18 register
35	19	08Ch	ICU.IELSR19	Event selected in the ICU.IELSR19 register
36	20	090h	ICU.IELSR20	Event selected in the ICU.IELSR20 register
37	21	094h	ICU.IELSR21	Event selected in the ICU.IELSR21 register
38	22	098h	ICU.IELSR22	Event selected in the ICU.IELSR22 register

Table 13.3 Interrupt vector table (2 of 3)

Exception number	IRQ number	Vector offset	Source	Description
39	23	09Ch	ICU.IELSR23	Event selected in the ICU.IELSR23 register
40	24	0A0h	ICU.IELSR24	Event selected in the ICU.IELSR24 register
41	25	0A4h	ICU.IELSR25	Event selected in the ICU.IELSR25 register
42	26	0A8h	ICU.IELSR26	Event selected in the ICU.IELSR26 register
43	27	0ACh	ICU.IELSR27	Event selected in the ICU.IELSR27 register
44	28	0B0h	ICU.IELSR28	Event selected in the ICU.IELSR28 register
45	29	0B4h	ICU.IELSR29	Event selected in the ICU.IELSR29 register
46	30	0B8h	ICU.IELSR30	Event selected in the ICU.IELSR30 register
47	31	0BCh	ICU.IELSR31	Event selected in the ICU.IELSR31 register
48	32	0C0h	ICU.IELSR32	Event selected in the ICU.IELSR32 register
49	33	0C4h	ICU.IELSR33	Event selected in the ICU.IELSR33 register
50	34	0C8h	ICU.IELSR34	Event selected in the ICU.IELSR34 register
51	35	0CCh	ICU.IELSR35	Event selected in the ICU.IELSR35 register
52	36	0D0h	ICU.IELSR36	Event selected in the ICU.IELSR36 register
53	37	0D4h	ICU.IELSR37	Event selected in the ICU.IELSR37 register
54	38	0D8h	ICU.IELSR38	Event selected in the ICU.IELSR38 register
55	39	0DCh	ICU.IELSR39	Event selected in the ICU.IELSR39 register
56	40	0E0h	ICU.IELSR40	Event selected in the ICU.IELSR40 register
57	41	0E4h	ICU.IELSR41	Event selected in the ICU.IELSR41 register
58	42	0E8h	ICU.IELSR42	Event selected in the ICU.IELSR42 register
59	43	0ECh	ICU.IELSR43	Event selected in the ICU.IELSR43 register
60	44	0F0h	ICU.IELSR44	Event selected in the ICU.IELSR44 register
61	45	0F4h	ICU.IELSR45	Event selected in the ICU.IELSR45 register
62	46	0F8h	ICU.IELSR46	Event selected in the ICU.IELSR46 register
63	47	0FCh	ICU.IELSR47	Event selected in the ICU.IELSR47 register
64	48	100h	ICU.IELSR48	Event selected in the ICU.IELSR48 register
65	49	104h	ICU.IELSR49	Event selected in the ICU.IELSR49 register
66	50	108h	ICU.IELSR50	Event selected in the ICU.IELSR50 register
67	51	10Ch	ICU.IELSR51	Event selected in the ICU.IELSR51 register
68	52	110h	ICU.IELSR52	Event selected in the ICU.IELSR52 register
69	53	114h	ICU.IELSR53	Event selected in the ICU.IELSR53 register
70	54	118h	ICU.IELSR54	Event selected in the ICU.IELSR54 register
71	55	11Ch	ICU.IELSR55	Event selected in the ICU.IELSR55 register
72	56	120h	ICU.IELSR56	Event selected in the ICU.IELSR56 register
73	57	124h	ICU.IELSR57	Event selected in the ICU.IELSR57 register
74	58	128h	ICU.IELSR58	Event selected in the ICU.IELSR58 register
75	59	12Ch	ICU.IELSR59	Event selected in the ICU.IELSR59 register
76	60	130h	ICU.IELSR60	Event selected in the ICU.IELSR60 register
77	61	134h	ICU.IELSR61	Event selected in the ICU.IELSR61 register
78	62	138h	ICU.IELSR62	Event selected in the ICU.IELSR62 register
79	63	13Ch	ICU.IELSR63	Event selected in the ICU.IELSR63 register
80	64	140h	ICU.IELSR64	Event selected in the ICU.IELSR64 register
81	65	144h	ICU.IELSR65	Event selected in the ICU.IELSR65 register
82	66	148h	ICU.IELSR66	Event selected in the ICU.IELSR66 register
83	67	14Ch	ICU.IELSR67	Event selected in the ICU.IELSR67 register

Table 13.3 Interrupt vector table (3 of 3)

Exception number	IRQ number	Vector offset	Source	Description
84	68	150h	ICU.IELSR68	Event selected in the ICU.IELSR68 register
85	69	154h	ICU.IELSR69	Event selected in the ICU.IELSR69 register
86	70	158h	ICU.IELSR70	Event selected in the ICU.IELSR70 register
87	71	15Ch	ICU.IELSR71	Event selected in the ICU.IELSR71 register
88	72	160h	ICU.IELSR72	Event selected in the ICU.IELSR72 register
89	73	164h	ICU.IELSR73	Event selected in the ICU.IELSR73 register
90	74	168h	ICU.IELSR74	Event selected in the ICU.IELSR74 register
91	75	16Ch	ICU.IELSR75	Event selected in the ICU.IELSR75 register
92	76	170h	ICU.IELSR76	Event selected in the ICU.IELSR76 register
93	77	174h	ICU.IELSR77	Event selected in the ICU.IELSR77 register
94	78	178h	ICU.IELSR78	Event selected in the ICU.IELSR78 register
95	79	17Ch	ICU.IELSR79	Event selected in the ICU.IELSR79 register
96	80	180h	ICU.IELSR80	Event selected in the ICU.IELSR80 register
97	81	184h	ICU.IELSR81	Event selected in the ICU.IELSR81 register
98	82	188h	ICU.IELSR82	Event selected in the ICU.IELSR82 register
99	83	18Ch	ICU.IELSR83	Event selected in the ICU.IELSR83 register
100	84	190h	ICU.IELSR84	Event selected in the ICU.IELSR84 register
101	85	194h	ICU.IELSR85	Event selected in the ICU.IELSR85 register
102	86	198h	ICU.IELSR86	Event selected in the ICU.IELSR86 register
103	87	19Ch	ICU.IELSR87	Event selected in the ICU.IELSR87 register
104	88	1A0h	ICU.IELSR88	Event selected in the ICU.IELSR88 register
105	89	1A4h	ICU.IELSR89	Event selected in the ICU.IELSR89 register
106	90	1A8h	ICU.IELSR90	Event selected in the ICU.IELSR90 register
107	91	1ACh	ICU.IELSR91	Event selected in the ICU.IELSR91 register
108	92	1B0h	ICU.IELSR92	Event selected in the ICU.IELSR92 register
109	93	1B4h	ICU.IELSR93	Event selected in the ICU.IELSR93 register
110	94	1B8h	ICU.IELSR94	Event selected in the ICU.IELSR94 register
111	95	1BCh	ICU.IELSR95	Event selected in the ICU.IELSR95 register

13.3.2 Event Numbers

The following table lists heading details for Table 13.4, which describes each event number.

Heading	Description
Interrupt request source	Name of the source generating the interrupt request
Name	Name of the interrupt
Connect to NVIC	"✓" indicates the interrupt can be used as a CPU interrupt (IELSRn setting)
Invoke DTC	"✓" indicates the interrupt can be used to request DTC activation (IELSRn setting)
Invoke DMAC	"✓" indicates the interrupt can be used to request DMAC activation (DELSRn setting)
Canceling Snooze mode	"✓" indicates the interrupt can be used to request a return from Snooze mode using SELSR0. Otherwise, "✓" indicates it can be used directly
Canceling Software Standby mode	"✓" indicates the interrupt can be used to request a return from Software Standby mode
Canceling Deep Software Standby mode	"✓" indicates the interrupt can be used to request a return from Deep Software Standby mode

Table 13.4 Event table (1 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
001h	Port	PORT_IRQ0	✓	✓	✓	✓	✓	✓
002h		PORT_IRQ1	✓	✓	✓	✓	✓	✓
003h		PORT_IRQ2	✓	✓	✓	✓	✓	✓
004h		PORT_IRQ3	✓	✓	✓	✓	✓	✓
005h		PORT_IRQ4	✓	✓	✓	✓	✓	✓
006h		PORT_IRQ5	✓	✓	✓	✓	✓	✓
007h		PORT_IRQ6	✓	✓	✓	✓	✓	✓
008h		PORT_IRQ7	✓	✓	✓	✓	✓	✓
009h		PORT_IRQ8	✓	✓	✓	✓	✓	✓
00Ah		PORT_IRQ9	✓	✓	✓	✓	✓	✓
00Bh		PORT_IRQ10	✓	✓	✓	✓	✓	✓
00Ch		PORT_IRQ11	✓	✓	✓	✓	✓	✓
00Dh		PORT_IRQ12	✓	✓	✓	✓	✓	✓
00Eh		PORT_IRQ13	✓	✓	✓	✓	✓	✓
020h	DMAC0	DMAC0_INT	✓	✓	-	-	-	-
021h	DMAC1	DMAC1_INT	✓	✓	-	-	-	-
022h	DMAC2	DMAC2_INT	✓	✓	-	-	-	-
023h	DMAC3	DMAC3_INT	✓	✓	-	-	-	-
024h	DMAC4	DMAC4_INT	✓	✓	-	-	-	-
025h	DMAC5	DMAC5_INT	✓	✓	-	-	-	-
026h	DMAC6	DMAC6_INT	✓	✓	-	-	-	-
027h	DMAC7	DMAC7_INT	✓	✓	-	-	-	-
029h	DTC	DTC_COMPLETE	✓	-	-	✓*5	-	-
02Dh	ICU	ICU_SNZCANCEL	✓	-	-	✓	-	-
030h	FCU	FCU_FIFERR	✓	-	-	-	-	-
031h		FCU_FRDYI	✓	-	-	-	-	-
038h	LVD	LVD_LVD1	✓	-	-	✓	✓	✓
039h		LVD_LVD2	✓	-	-	✓	✓	✓
03Bh	MOSC	MOSC_STOP	✓	-	-	-	-	-
03Ch	Low power mode	SYSTEM_SNZREQ	-	✓	-	-	-	-
040h	AGT0	AGT0_AGTI	✓	✓	✓	-	-	-
041h		AGT0_AGTCMAI	✓	✓	✓	-	-	-
042h		AGT0_AGTCMBI	✓	✓	✓	-	-	-
043h	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓	✓
044h		AGT1_AGTCMAI	✓	✓	✓	✓	✓	-
045h		AGT1_AGTCMBI	✓	✓	✓	✓	✓	-
046h	IWDT	IWDT_NMIUNDF	✓	-	-	✓	✓	-
047h	WDT	WDT_NMIUNDF	✓	-	-	-	-	-
04Bh	ADC120	ADC120_ADI	✓	✓	✓	-	-	-
04Ch		ADC120_GBADI	✓	✓	✓	-	-	-
04Dh		ADC120_CMPAI	✓	-	-	-	-	-
04Eh		ADC120_CMPBI	✓	-	-	-	-	-
04Fh		ADC120_WCMPM	-	✓	✓	✓*5	-	-
050h		ADC120_WCMPUM	-	✓	✓	✓*5	-	-

Table 13.4 Event table (2 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
051h	ADC121	ADC121_ADI	✓	✓	✓	-	-	-
052h		ADC121_GBADI	✓	✓	✓	-	-	-
053h		ADC121_CMPAI	✓	-	-	-	-	-
054h		ADC121_CMPBI	✓	-	-	-	-	-
055h		ADC121_WCMPM	-	✓	✓	✓*5	-	-
056h		ADC121_WCMPUM	-	✓	✓	✓*5	-	-
057h	ACMPHS	ACMP_HS0	✓	-	-	✓*1	✓*1	-
058h		ACMP_HS1	✓	-	-	-	-	-
059h		ACMP_HS2	✓	-	-	-	-	-
05Ah		ACMP_HS3	✓	-	-	-	-	-
05Bh		ACMP_HS4	✓	-	-	-	-	-
05Ch		ACMP_HS5	✓	-	-	-	-	-
063h	IIC0	IIC0_RXI	✓	✓	✓	-	-	-
064h		IIC0_TXI	✓	✓	✓	-	-	-
065h		IIC0_TEI	✓	-	-	-	-	-
066h		IIC0_EEI	✓	-	-	-	-	-
067h		IIC0_WUI	✓	-	-	✓	✓	-
068h	IIC1	IIC1_RXI	✓	✓	✓	-	-	-
069h		IIC1_TXI	✓	✓	✓	-	-	-
06Ah		IIC1_TEI	✓	-	-	-	-	-
06Bh		IIC1_EEI	✓	-	-	-	-	-
085h	KINT	KEY_INTKR	✓	-	-	✓*2	✓*2	-
086h	DOC	DOC_DOPCI	✓	-	-	✓*5	-	-
087h	CAC	CAC_FERRI	✓	-	-	-	-	-
088h		CAC_MENDI	✓	-	-	-	-	-
089h		CAC_OVFI	✓	-	-	-	-	-
08Ah	CAN0	CAN0_ERS	✓	-	-	-	-	-
08Bh		CAN0_RXF	✓	-	-	-	-	-
08Ch		CAN0_TXF	✓	-	-	-	-	-
08Dh		CAN0_RXM	✓	-	-	-	-	-
08Eh		CAN0_TXM	✓	-	-	-	-	-
094h	I/O port	IOPORT_GROUP1	✓	✓*3	✓*3	-	-	-
095h		IOPORT_GROUP2	✓	✓*3	✓*3	-	-	-
096h		IOPORT_GROUP3	✓	✓*3	✓*3	-	-	-
097h		IOPORT_GROUP4	✓	✓*3	✓*3	-	-	-
098h	ELC	ELC_SWEVT0	✓*4	✓	-	-	-	-
099h		ELC_SWEVT1	✓*4	✓	-	-	-	-
09Ah	POEG	POEG_GROUP0	✓	-	-	-	-	-
09Bh		POEG_GROUP1	✓	-	-	-	-	-
09Ch		POEG_GROUP2	✓	-	-	-	-	-
09Dh		POEG_GROUP3	✓	-	-	-	-	-

Table 13.4 Event table (3 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0B0h	GPT32EH0	GPT0_CCMPA	✓	✓	✓	-	-	-
0B1h		GPT0_CCMPB	✓	✓	✓	-	-	-
0B2h		GPT0_CMPC	✓	✓	✓	-	-	-
0B3h		GPT0_CMPD	✓	✓	✓	-	-	-
0B4h		GPT0_CMPE	✓	✓	✓	-	-	-
0B5h		GPT0_CMPF	✓	✓	✓	-	-	-
0B6h		GPT0_OVF	✓	✓	✓	-	-	-
0B7h		GPT0_UDF	✓	✓	✓	-	-	-
0B8h		GPT0_ADTRGA	✓	✓	✓	-	-	-
0B9h		GPT0_ADTRGB	✓	✓	✓	-	-	-
0BAh	GPT32EH1	GPT1_CCMPA	✓	✓	✓	-	-	-
0BBh		GPT1_CCMPB	✓	✓	✓	-	-	-
0BCh		GPT1_CMPC	✓	✓	✓	-	-	-
0BDh		GPT1_CMPD	✓	✓	✓	-	-	-
0BEh		GPT1_CMPE	✓	✓	✓	-	-	-
0BFh		GPT1_CMPF	✓	✓	✓	-	-	-
0C0h		GPT1_OVF	✓	✓	✓	-	-	-
0C1h		GPT1_UDF	✓	✓	✓	-	-	-
0C2h		GPT1_ADTRGA	✓	✓	✓	-	-	-
0C3h		GPT1_ADTRGB	✓	✓	✓	-	-	-
0C4h	GPT32EH2	GPT2_CCMPA	✓	✓	✓	-	-	-
0C5h		GPT2_CCMPB	✓	✓	✓	-	-	-
0C6h		GPT2_CMPC	✓	✓	✓	-	-	-
0C7h		GPT2_CMPD	✓	✓	✓	-	-	-
0C8h		GPT2_CMPE	✓	✓	✓	-	-	-
0C9h		GPT2_CMPF	✓	✓	✓	-	-	-
0CAh		GPT2_OVF	✓	✓	✓	-	-	-
0CBh		GPT2_UDF	✓	✓	✓	-	-	-
0CCh		GPT2_ADTRGA	✓	✓	✓	-	-	-
0CDh		GPT2_ADTRGB	✓	✓	✓	-	-	-
0CEh	GPT32EH3	GPT3_CCMPA	✓	✓	✓	-	-	-
0CFh		GPT3_CCMPB	✓	✓	✓	-	-	-
0D0h		GPT3_CMPC	✓	✓	✓	-	-	-
0D1h		GPT3_CMPD	✓	✓	✓	-	-	-
0D2h		GPT3_CMPE	✓	✓	✓	-	-	-
0D3h		GPT3_CMPF	✓	✓	✓	-	-	-
0D4h		GPT3_OVF	✓	✓	✓	-	-	-
0D5h		GPT3_UDF	✓	✓	✓	-	-	-
0D6h		GPT3_ADTRGA	✓	✓	✓	-	-	-
0D7h		GPT3_ADTRGB	✓	✓	✓	-	-	-

Table 13.4 Event table (4 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0D8h	GPT32E4	GPT4_CCMPA	✓	✓	✓	-	-	-
0D9h		GPT4_CCMPB	✓	✓	✓	-	-	-
0DAh		GPT4_CMPC	✓	✓	✓	-	-	-
0DBh		GPT4_CMPD	✓	✓	✓	-	-	-
0DCh		GPT4_CMPE	✓	✓	✓	-	-	-
0DDh		GPT4_CMPF	✓	✓	✓	-	-	-
0DEh		GPT4_OVF	✓	✓	✓	-	-	-
0DFh		GPT4_UDF	✓	✓	✓	-	-	-
0E0h		GPT4_ADTRGA	✓	✓	✓	-	-	-
0E1h		GPT4_ADTRGB	✓	✓	✓	-	-	-
0E2h	GPT32E5	GPT5_CCMPA	✓	✓	✓	-	-	-
0E3h		GPT5_CCMPB	✓	✓	✓	-	-	-
0E4h		GPT5_CMPC	✓	✓	✓	-	-	-
0E5h		GPT5_CMPD	✓	✓	✓	-	-	-
0E6h		GPT5_CMPE	✓	✓	✓	-	-	-
0E7h		GPT5_CMPF	✓	✓	✓	-	-	-
0E8h		GPT5_OVF	✓	✓	✓	-	-	-
0E9h		GPT5_UDF	✓	✓	✓	-	-	-
0EAh		GPT5_ADTRGA	✓	✓	✓	-	-	-
0EBh		GPT5_ADTRGB	✓	✓	✓	-	-	-
0ECh	GPT32E6	GPT6_CCMPA	✓	✓	✓	-	-	-
0EDh		GPT6_CCMPB	✓	✓	✓	-	-	-
0EEh		GPT6_CMPC	✓	✓	✓	-	-	-
0EFh		GPT6_CMPD	✓	✓	✓	-	-	-
0F0h		GPT6_CMPE	✓	✓	✓	-	-	-
0F1h		GPT6_CMPF	✓	✓	✓	-	-	-
0F2h		GPT6_OVF	✓	✓	✓	-	-	-
0F3h		GPT6_UDF	✓	✓	✓	-	-	-
0F4h		GPT6_ADTRGA	✓	✓	✓	-	-	-
0F5h		GPT6_ADTRGB	✓	✓	✓	-	-	-
0F6h	GPT32E7	GPT7_CCMPA	✓	✓	✓	-	-	-
0F7h		GPT7_CCMPB	✓	✓	✓	-	-	-
0F8h		GPT7_CMPC	✓	✓	✓	-	-	-
0F9h		GPT7_CMPD	✓	✓	✓	-	-	-
0FAh		GPT7_CMPE	✓	✓	✓	-	-	-
0FBh		GPT7_CMPF	✓	✓	✓	-	-	-
0FCh		GPT7_OVF	✓	✓	✓	-	-	-
0FDh		GPT7_UDF	✓	✓	✓	-	-	-
0FEh		GPT7_ADTRGA	✓	✓	✓	-	-	-
0FFh		GPT7_ADTRGB	✓	✓	✓	-	-	-

Table 13.4 Event table (5 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
100h	GPT328	GPT8_CCMPA	✓	✓	✓	-	-	-
101h		GPT8_CCMPB	✓	✓	✓	-	-	-
102h		GPT8_CMPC	✓	✓	✓	-	-	-
103h		GPT8_CMPD	✓	✓	✓	-	-	-
104h		GPT8_CMPE	✓	✓	✓	-	-	-
105h		GPT8_CMPF	✓	✓	✓	-	-	-
106h		GPT8_OVF	✓	✓	✓	-	-	-
107h		GPT8_UDF	✓	✓	✓	-	-	-
10Ah	GPT329	GPT9_CCMPA	✓	✓	✓	-	-	-
10Bh		GPT9_CCMPB	✓	✓	✓	-	-	-
10Ch		GPT9_CMPC	✓	✓	✓	-	-	-
10Dh		GPT9_CMPD	✓	✓	✓	-	-	-
10Eh		GPT9_CMPE	✓	✓	✓	-	-	-
10Fh		GPT9_CMPF	✓	✓	✓	-	-	-
110h		GPT9_OVF	✓	✓	✓	-	-	-
111h		GPT9_UDF	✓	✓	✓	-	-	-
114h	GPT3210	GPT10_CCMPA	✓	✓	✓	-	-	-
115h		GPT10_CCMPB	✓	✓	✓	-	-	-
116h		GPT10_CMPC	✓	✓	✓	-	-	-
117h		GPT10_CMPD	✓	✓	✓	-	-	-
118h		GPT10_CMPE	✓	✓	✓	-	-	-
119h		GPT10_CMPF	✓	✓	✓	-	-	-
11Ah		GPT10_OVF	✓	✓	✓	-	-	-
11Bh		GPT10_UDF	✓	✓	✓	-	-	-
11Eh	GPT3211	GPT11_CCMPA	✓	✓	✓	-	-	-
11Fh		GPT11_CCMPB	✓	✓	✓	-	-	-
120h		GPT11_CMPC	✓	✓	✓	-	-	-
121h		GPT11_CMPD	✓	✓	✓	-	-	-
122h		GPT11_CMPE	✓	✓	✓	-	-	-
123h		GPT11_CMPF	✓	✓	✓	-	-	-
124h		GPT11_OVF	✓	✓	✓	-	-	-
125h		GPT11_UDF	✓	✓	✓	-	-	-
128h	GPT3212	GPT12_CCMPA	✓	✓	✓	-	-	-
129h		GPT12_CCMPB	✓	✓	✓	-	-	-
12Ah		GPT12_CMPC	✓	✓	✓	-	-	-
12Bh		GPT12_CMPD	✓	✓	✓	-	-	-
12Ch		GPT12_CMPE	✓	✓	✓	-	-	-
12Dh		GPT12_CMPF	✓	✓	✓	-	-	-
12Eh		GPT12_OVF	✓	✓	✓	-	-	-
12Fh		GPT12_UDF	✓	✓	✓	-	-	-
150h	GPT	GPT_UVWEDGE	✓			-	-	-

Table 13.4 Event table (6 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
174h	SCI0	SCI0_RXI	✓	✓	✓	-	-	-
175h		SCI0_TXI	✓	✓	✓	-	-	-
176h		SCI0_TEI	✓	-	-	-	-	-
177h		SCI0_ERI	✓	-	-	-	-	-
178h		SCI0_AM	✓	-	-	✓*5	-	-
179h		SCI0_RXI_OR_ERI	-	-	-	✓*5	-	-
17Ah	SCI1	SCI1_RXI	✓	✓	✓	-	-	-
17Bh		SCI1_TXI	✓	✓	✓	-	-	-
17Ch		SCI1_TEI	✓	-	-	-	-	-
17Dh		SCI1_ERI	✓	-	-	-	-	-
17Eh		SCI1_AM	✓	-	-	-	-	-
180h	SCI2	SCI2_RXI	✓	✓	✓	-	-	-
181h		SCI2_TXI	✓	✓	✓	-	-	-
182h		SCI2_TEI	✓	-	-	-	-	-
183h		SCI2_ERI	✓	-	-	-	-	-
184h		SCI2_AM	✓	-	-	-	-	-
186h	SCI3	SCI3_RXI	✓	✓	✓	-	-	-
187h		SCI3_TXI	✓	✓	✓	-	-	-
188h		SCI3_TEI	✓	-	-	-	-	-
189h		SCI3_ERI	✓	-	-	-	-	-
18Ah		SCI3_AM	✓	-	-	-	-	-
18Ch	SCI4	SCI4_RXI	✓	✓	✓	-	-	-
18Dh		SCI4_TXI	✓	✓	✓	-	-	-
18Eh		SCI4_TEI	✓	-	-	-	-	-
18Fh		SCI4_ERI	✓	-	-	-	-	-
190h		SCI4_AM	✓	-	-	-	-	-
1A4h	SCI8	SCI8_RXI	✓	✓	✓	-	-	-
1A5h		SCI8_TXI	✓	✓	✓	-	-	-
1A6h		SCI8_TEI	✓	-	-	-	-	-
1A7h		SCI8_ERI	✓	-	-	-	-	-
1A8h		SCI8_AM	✓	-	-	-	-	-
1AAh	SCI9	SCI9_RXI	✓	✓	✓	-	-	-
1ABh		SCI9_TXI	✓	✓	✓	-	-	-
1ACh		SCI9_TEI	✓	-	-	-	-	-
1ADh		SCI9_ERI	✓	-	-	-	-	-
1AEh		SCI9_AM	✓	-	-	-	-	-
1BCh	SPI0	SPI0_SPRI	✓	✓	✓	-	-	-
1BDh		SPI0_SPTI	✓	✓	✓	-	-	-
1BEh		SPI0_SPII	✓	-	-	-	-	-
1BFh		SPI0_SPEI	✓	-	-	-	-	-
1C0h		SPI0_SPTEND	✓	-	-	-	-	-
1C1h	SPI1	SPI1_SPRI	✓	✓	✓	-	-	-
1C2h		SPI1_SPTI	✓	✓	✓	-	-	-
1C3h		SPI1_SPII	✓	-	-	-	-	-
1C4h		SPI1_SPEI	✓	-	-	-	-	-
1C5h		SPI1_SPTEND	✓	-	-	-	-	-

Note 1. Only supported when CMPCTL.CSTEN = 1.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.
Note 5. Using SELSR0.

13.4 Interrupt Operation

The ICU performs the following functions:

- Detecting interrupts
- Enabling and disabling interrupts
- Selecting interrupt request destinations such as CPU interrupt, DTC activation, and DMAC activation.

13.4.1 Detecting Interrupts

External pin interrupt requests are detected by either:

- Edges (falling edge, rising edge, or rising and falling edges) of the interrupt signal
- Level (low level) of the interrupt signal.

Set the IRQMD[1:0] bits in the IRQCRi register to select the detection mode for the IRQi pins. For interrupt sources associated with peripheral modules, see section 13.3.2, Event Numbers. Events must be accepted by the NVIC before an interrupt occurs and is accepted by the CPU.

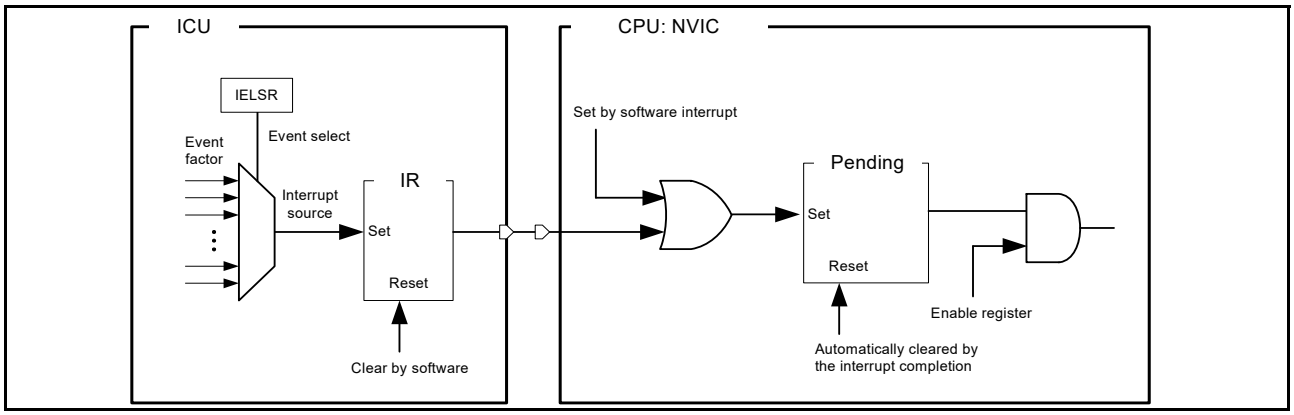


Figure 13.2 Interrupt path of the ICU and CPU: NVIC

Use the following procedures for detecting interrupts.

General operations during an interrupt:

- When a non-software interrupt occurs:
  The IELSRn.IR flag and Interrupt Set/Clear-Pending register (NVIC) are set.
- When a software interrupt occurs:
  Set the Interrupt Set-Pending register.
- When an interrupt is complete:
  Clear the IELSRn.IR flag in the software.
  The Interrupt Set/Clear-Pending register clears automatically.

When interrupts are enabled:

1. Set the Interrupt Set-Enable register (NVIC).
2. Set the IELSRn.IELS[8:0] bits as the interrupt source.
3. Specify the operation settings for the event source.

When interrupts are disabled:

1. Disable the settings for the event source.

2. Clear the IELSRn.IELS[8:0] bits (IELSRn.IELS[8:0] = 0000h). Clear the IELSRn.IR flag as required.
3. Clear the Interrupt Clear-Enable register. Clear the Interrupt Clear-Pending register as required.

When polling for interrupts:

1. Set the Interrupt Clear-Enable register (disabling interrupts).
2. Set the IELSRn.IELS[8:0] bits (selecting the source).
3. Specify the operation settings for the event source.
4. Poll the Interrupt Set-Pending register.
5. When polling is no longer required, follow the procedure for clearing an interrupt when it is complete. Clear the IELSRn.IR flag through software.

13.4.2 Selecting Interrupt Request Destinations

The interrupt output destination, CPU, DTC, or DMAC, can be independently selected for each interrupt source. The available destinations are fixed for each interrupt, as described in Table 13.4.

Note: Use an interrupt request destination setting that is indicated by a "✓" in the event list (see Table 13.4).

If you select the CPU or DTC in one IELSRn register, setting the same interrupt factor in any other IELSRn register is prohibited. Similarly, if you select the DMAC in one DELSRn register, setting the same interrupt factor in any other DELSRn register is prohibited.

Note: Setting the same interrupt factor for IELSRn and DELSRn is prohibited.

If the DMAC or DTC is selected as the destination for requests from an IRQi pin, you must set the IRQMD[1:0] bits in IRQCRi for that interrupt to select edge detection.

13.4.2.1 CPU interrupt request

When IELSRn.DTCE = 0, the event specified in the IELSRn register is output to the NVIC. Set the IELSRn.IELS bits to the target event and the IELSRn.DTCE bit to 0.

13.4.2.2 DTC activation

When IELSRn.DTCE = 1, the event specified in the IELSRn register is output to the DTC. After DTC transmission completes, the associated interrupt occurs. Use the following procedure:

1. Set the IELSRn.IELS bits to the target event and the IELSRn.DTCE bit to 1.
2. Set the DTC Module Start bit (DTCST.DTCST) to 1.

Table 13.5 shows operation when the DTC is the request destination.

Table 13.5 Operations when the DTC is activated

Interrupt request destination	DISEL*1	Remaining transfer operations	Operations per request	IR*2	Interrupt request destination after transfer
DTC*3	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The IELSRn.DTCE bit is cleared and the CPU becomes the destination
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after DTC transfer data is read	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The IELSRn.DTCE bit is cleared and the CPU becomes the destination

Note 1. Set the interrupt request mode for the DTC in the DTC.MRB.DISEL bit.
Note 2. When the IELSRn.IR flag is 1, an interrupt request (DTC activation request) that occurs again is ignored.
Note 3. For chain transfers, DTC transfer continues until the last chain transfer ends. At this point, the DISEL bit state and the remaining transfer count determine whether a CPU interrupt occurs, the IELSRn.IR flag clear timing, and the interrupt request destination after transfer. See Table 17.3, Chain transfer conditions, in section 17, Data Transfer Controller (DTC).

13.4.2.3 DMAC activation

Events specified in the DELSRn registers are output to the DMAC. When using interrupts, you must select the DMAC as the interrupt source in the IELSRn.IELS[8:0] bits and enable DMAC output by setting IELSRn.DTCE to 1. When IELSRn.DTCE is 0, the events specified in the IELSRn registers are output to the NVIC. Use the following procedure:

1. Set the DELSRn.DELS[8:0] bits to the target event.
2. When using interrupts, set the IELSRn.IELS bit to DMAC interrupts as the source, and set the IELSRn.DTCE bit to 1.
3. Set the activation source for the target DMAC channel (DMACm.DMTMD.DCTG[1:0]) to 01b (interrupt module detection).
4. Set the DMAC transfer enable bit for the target DMAC channel (DMACm.DMCNT.DTE) to 1.
5. Set the DMAC operation enable bit (DMACm.DMAST.DMST) to 1.

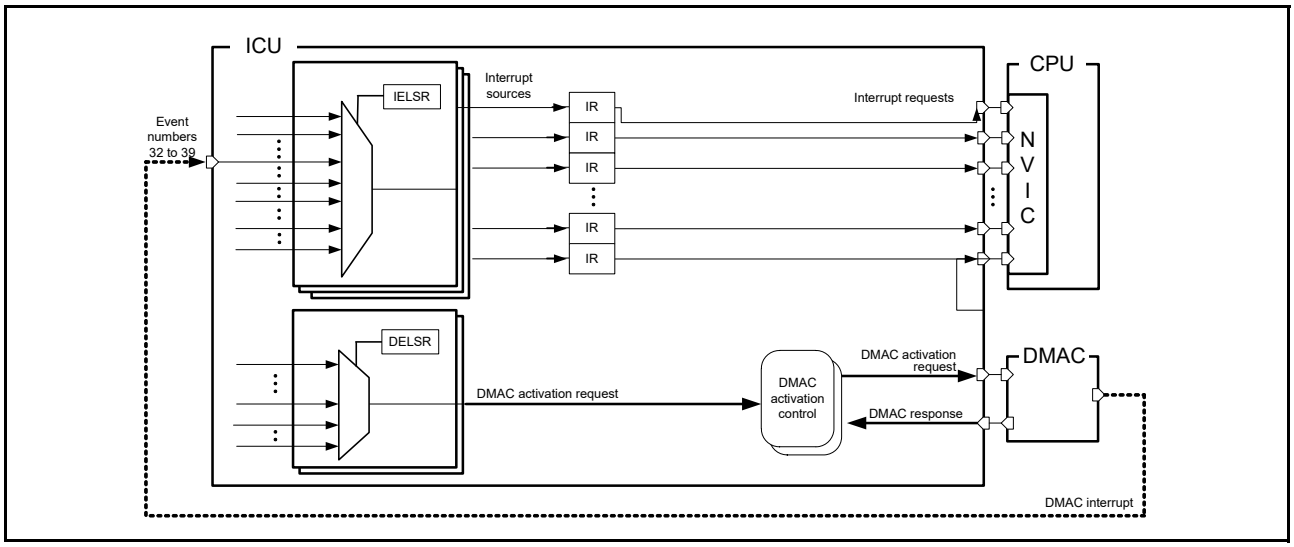


Figure 13.3 DMAC request trigger and interrupt path

13.4.3 Digital Filter

A digital filter function is provided for the external interrupt request pins IRQi, (i = 0 to 13) and NMI pin interrupt. It samples input signals on the filter PCLKB sampling clock, and removes any signal with a pulse width less than 3 sampling cycles.

To use the digital filter for an IRQi pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the IRQCRi.FCLKSEL[1:0] bits.
2. Set the IRQCRi.FLTEN bit to 1 (digital filter enabled).

To use the digital filter for the NMI pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the NMICR.NFCLKSEL[1:0] bits.
2. Set the NMICR.NFLTEN bit to 1 (digital filter enabled).

Figure 13.4 shows an example of digital filter operation.

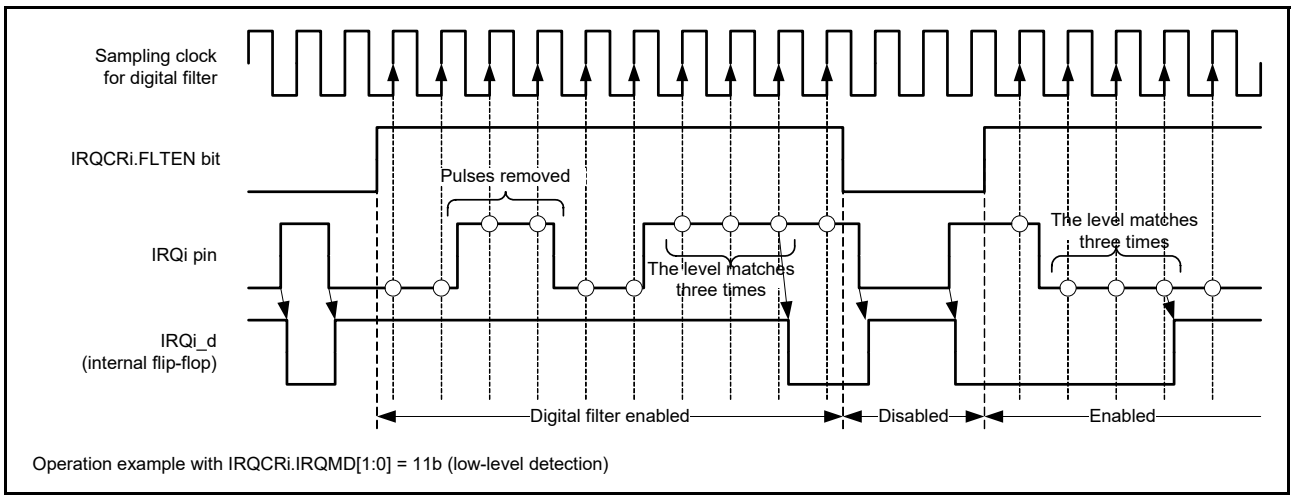


Figure 13.4 Digital filter operation example

Before entering Software Standby mode, disable the digital filters by clearing the IRQCRi.FLTEN and NMICR.NFLTEN bits. The clock for the ICU stops in Software Standby mode. On exiting Software Standby, the circuit detects the edge by comparing the state before standby to the state after standby release. If the input changes during Software Standby, an incorrect edge might be detected. You can enable the digital filters again after exiting Software Standby mode.

13.4.4 External Pin Interrupts

To use external pin interrupts:

1. Clear the IRQCRi.FLTEN bit (i = 0 to 13) to 0 (digital filter disabled).
2. Set or confirm the I/O port settings.
3. Set the IRQMD[1:0] bits, FCLKSEL[1:0] bits, and FLTEN bit of the IRQCRi register.
4. Select the IRQ pin as follows:
   - If the IRQ pin is to be used for CPU interrupt requests, set the IELSRn.IELS bits and set the IELSRn.DTCE bit to 0
   - If the IRQ pin is to be used for DTC activation, set the IELSRn.IELS bits and set the IELSRn.DTCE bit to 1
   - If the IRQ pin is to be used for DMAC activation, set the DELSRn.DELS bits.

13.5 Non-Maskable Interrupt Operation

The following sources can trigger a non-maskable interrupt:

- NMI pin interrupt
- Oscillation stop detection interrupt
- WDT underflow/refresh error interrupt
- IWDT underflow/refresh error interrupt
- Voltage monitor 1 interrupt
- Voltage monitor 2 interrupt
- SRAM parity error interrupt
- MPU bus master error interrupt
- MPU bus slave error interrupt
- CPU stack pointer monitor interrupt.

Non-maskable interrupts can only be used with the CPU, not to activate the DTC or DMAC. Non-maskable interrupts take precedence over all other interrupts. The non-maskable interrupt states can be verified in the Non-Maskable Interrupt Status Register (NMISR). Confirm that all bits in the NMISR are 0 before returning from the NMI handler.

Non-maskable interrupts are disabled by default. To use non-maskable interrupts:

1. Clear the NMICR.NFLTEN bit to 0 (digital filter disabled) to use the NMI pin.
2. Set the NMIMD bit, NFCLKSEL[1:0] bits, and NFLTEN bit of NMICR register to use the NMI pin.
3. Write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0 to use the NMI pin.
4. Enable the non-maskable interrupt by writing 1 to the associated bit in the Non-Maskable Interrupt Enable Register (NMIER).

After 1 is written to the NMIER register, subsequent write access to the NMIEN bit in NMIER is ignored. An NMI interrupt cannot be disabled when enabled, except by a reset.

13.6 Return from Low Power Modes

Table 13.4 lists the interrupt sources you can use to exit Sleep or Software Standby mode. For more information, see section 11, Low Power Modes. Sections 13.6.1 to 13.6.3 describe how to use interrupts to return from Sleep, Software Standby, and Snooze modes. For Deep Software Standby mode, see section 11.9, Deep Software Standby Mode.

13.6.1 Return from Sleep Mode

To return from Sleep mode in response to an interrupt:

1. Select the CPU as the interrupt request destination.
2. Enable the interrupt in the NVIC.

To return from Sleep mode in response to a non-maskable interrupt, use the NMIER register to enable the target interrupt request.

13.6.2 Return from Software Standby Mode

The ICU can return from Software Standby mode using a non-maskable interrupt or an interrupt selected in the WUPEN register. See section 13.2.9, Wake Up Interrupt Enable Register (WUPEN).

To return from Software Standby mode:

1. Select the interrupt source that enables return from Software Standby:
   - For non-maskable interrupts, use the NMIER register to enable the target interrupt request
   - For maskable interrupts, use the WUPEN register to enable the target interrupt request.

2. Select the CPU as the interrupt request destination.
3. Enable the interrupt in the NVIC.

Interrupt requests through the IRQ pins that do not satisfy these conditions are not detected while the clock is stopped in Software Standby mode.

13.6.3 Return from Snooze Mode

The ICU can return to Normal mode from Snooze mode using the interrupts provided for this mode.

To return to Normal mode from Snooze mode:

1. Use either of the following methods to select the event that you want to trigger a return to Normal mode from Snooze mode:
   - Set the event that you want to trigger a return to Normal mode from Snooze mode in SELSR0.SELS[8:0] and set the value 02Dh (ICU_SNZCANCEL) in IELSRn.IELS[8:0]
   - Set the event that you want to trigger a return to Normal mode from Snooze mode in IELSRn.IELS[8:0].
2. Select the CPU as the interrupt request destination.
3. Enable the interrupt in the NVIC.

Note: In Snooze mode, a clock is supplied to the ICU. If an event selected in IELSRn is detected, the CPU can acknowledge the interrupt after returning to Normal mode from Software Standby mode. If an event selected in DELSRn is detected, the DMAC can acknowledge the interrupt after returning to Normal mode from Software Standby mode.

13.7 Using the WFI Instruction with Non-Maskable Interrupts

Whenever a WFI instruction is executed, confirm that all status flags in the NMISR register are 0.

13.8 Reference

ARM® Cortex®-M4 Processor Technical Reference Manual (ARM DDI 0439D).

14. Buses

14.1 Overview

Table 14.1 lists the bus specifications, Figure 14.1 shows the bus configuration, and Table 14.2 lists the addresses assigned for each bus.

This bus interface can also be used to connect LCD Intel 8080 and Motorola 6800 interfaces.

Table 14.1 Bus specifications

Bus type		Specifications
Main bus	ICode bus (CPU)	• Connected to the CPU • Connected to the on-chip memory (code flash memory, SRAMHS).
	DCode bus (CPU)	• Connected to the CPU • Connected to the on-chip memory (code flash memory, SRAMHS).
	System bus (CPU)	• Connected to the CPU • Connected to the on-chip memory and internal peripheral buses.
	DMA bus	• Connected to the DMAC and DTC • Connected to the on-chip memory and internal peripheral buses.
Slave interface	Memory bus 1	• Connected to code flash memory
	Memory bus 2	• Connected to SRAMHS
	Memory bus 3	• Connected to code flash memory and SRAMHS through the DMA bus
	Internal peripheral bus 1	• Connected to system control related to peripheral modules
	Internal peripheral bus 3	• Connected to peripheral modules (CAC, ELC, I/O ports, POEG, WDT, IWDT, IIC, CAN, ADC12, DAC12, TSN, and DOC)
	Internal peripheral bus 4	• Connected to peripheral modules (GPT, SCI, IrDA, SPI, and CRC)
	Internal peripheral bus 5	• Connected to peripheral modules (KINT, AGT, and ACMPHS)
	Internal peripheral bus 7	• Connected to Secure IPs (SCE7)
	Internal peripheral bus 9	• Connected to flash memory (in P/E)*1, data flash memory, and TSN

Note 1. P/E: Programming and erasure.

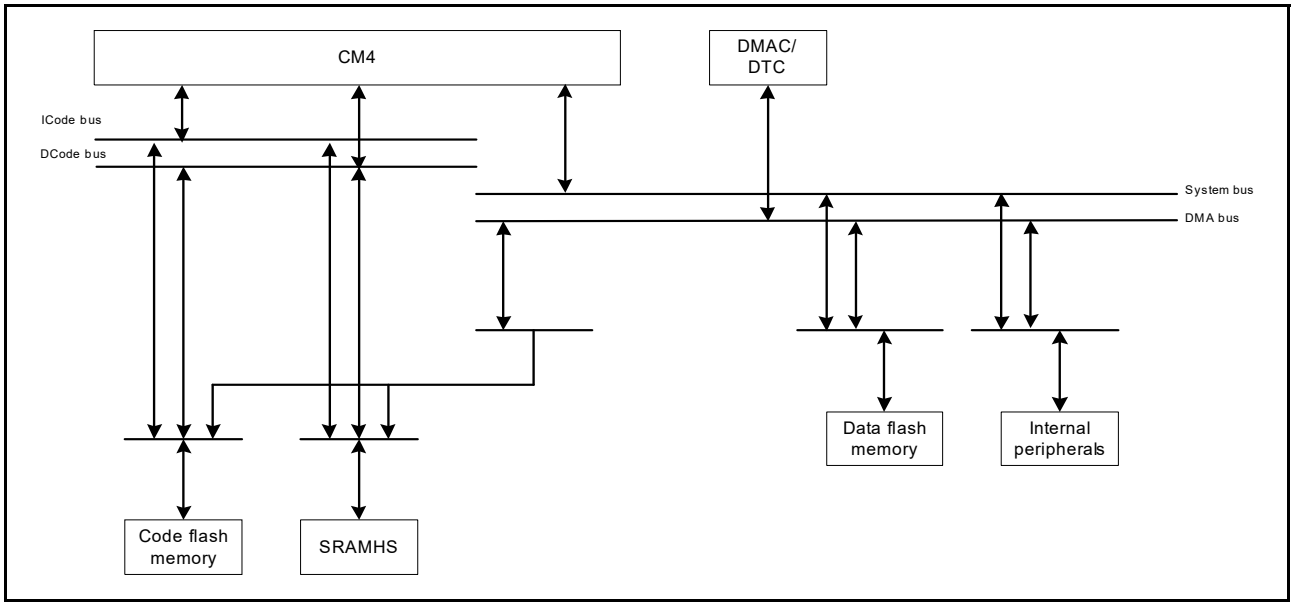


Figure 14.1 Bus configuration

Table 14.2 Addresses assigned to each bus

Addresses	Bus	Area
0000 0000h to 01FF FFFFh	Memory bus 1, 3	Code flash memory
1FFE 0000h to 1FFE FFFFh	Memory bus 2, 3	SRAMHS
4000 0000h to 4001 FFFFh	Internal peripheral bus 1	Peripheral I/O registers
4004 0000h to 4005 FFFFh	Internal peripheral bus 3	
4006 0000h to 4007 FFFFh	Internal peripheral bus 4	
4008 0000h to 4009 FFFFh	Internal peripheral bus 5	
400C 0000h to 400D FFFFh	Internal peripheral bus 7	Secure IPs
4010 0000h to 407F FFFFh	Internal peripheral bus 9	Flash memory (in P/E*1), data flash memory, and TSN

Note 1. P/E: Programming and erasure.

14.2 Description of Buses

14.2.1 Main Buses

The main buses for the CPU consist of the ICode bus, DCode bus, and system bus:

- The ICode and DCode buses are connected to the code flash memory and SRAMHS. The ICode bus is used for instruction access to the CPU, and the DCode bus is used for data access to the CPU.
- The system bus is connected to the data flash memory and internal peripheral buses. It is used for instruction and data accesses to the CPU.

The main bus for modules other than the CPU consists of the DMA bus:

- The DMA bus is connected to the code flash memory, SRAMHS, and data flash memory.

Different master and slave transfer combinations can proceed simultaneously.

Arbitration between the DMAC and DTC for the mastership of the DMA bus occurs in the DMAC and DTC. The following fixed-priority order is used:

DMAC0 > DMAC1 > DMAC2 > DMAC3 > DMAC4 > DMAC5 > DMAC6 > DMAC7 > DTC.

Only one DTC channel and DMAC channel that have accepted the activation requests can issue the bus mastership request. In addition, requests for bus access from masters other than the DTC are not accepted during reads of transfer control information for the DTC.

The arbitration protocol is selectable as either fixed-priority or round-robin. For more information, see section 14.3.2, Slave Bus Control Register (BUSSCNT<slave>).

14.2.2 Slave Interface

Products using the Cortex®-M4 core contain ICode and DCode bus areas and a system bus area.

To create the ICode and DCode bus areas, a bus matrix connects the ICode bus, DCode bus, and memory bus 3 from the main bus to the slave interfaces of the code flash memory and SRAMHS. Bus access to the slave interfaces is arbitrated between the three buses. The arbitration protocol is selectable as either fixed-priority or round-robin. For more information, see section 14.3.2, Slave Bus Control Register (BUSSCNT<slave>).

To create the system bus area, a bus matrix connects the system bus, and DMA bus from the main bus to the slave interfaces of the data flash memory and internal peripherals. Bus access to the slave interfaces is arbitrated between the three buses. The arbitration protocol is selectable as either fixed-priority or round-robin. For more information, see section 14.3.2, Slave Bus Control Register (BUSSCNT<slave>).

For connections from the main bus to the slave interfaces, see the slave interfaces in Table 14.1.

Different master and slave transfer combinations can proceed simultaneously.

14.2.3 Parallel Operations

Parallel operations are possible when different bus masters request access to different slave modules. For example, if the CPU fetches an instruction from the flash and an operand from the SRAM, the DMAC can handle transfers between a peripheral bus and the data flash at the same time.

An example of parallel operations is shown in Figure 14.2. In this example, the CPU uses the instruction and operand buses for simultaneous access to the flash and SRAM, respectively. Additionally, the DMAC/DTC simultaneously use the DMA bus (DMAC/DTC) for access to a peripheral bus or data flash during access to the flash memory and SRAM by the CPU.

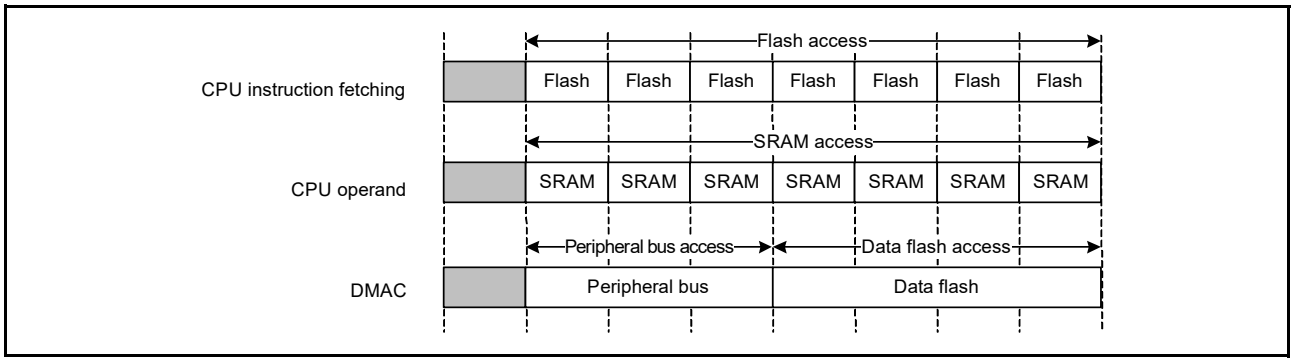


Figure 14.2 Example of parallel operations

14.2.4 Restrictions on Endianness

Memory space must be little-endian to execute code on the Cortex®-M4 core.

14.3 Register Descriptions

14.3.1 Master Bus Control Register (BUSMCNT<master>)

Address(es): BUS.BUSMCNTM4I 4000 4000h, BUS.BUSMCNTM4D 4000 4004h, BUS.BUSMCNTSYS 4000 4008h, BUS.BUSMCNTDMA 4000 400Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IERES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	IERES	Ignore Error Responses	0: Report bus errors 1: Do not report bus errors.	R/W

Note: Changing reserved bits from the initial value of 0 is prohibited. Operation during the change is not guaranteed.

Table 14.3 shows the registers associated with each bus type.

Table 14.3 Associations between bus types and registers

Bus type	Master Bus Control Register	Slave Bus Control Register	Bus Error Address Register	Bus Error Status Register
ICode bus (CPU)	BUSMCNTM4I	-	BUS1ERRADD	BUS1ERRSTAT
DCode bus (CPU)	BUSMCNTM4D	-	BUS2ERRADD	BUS2ERRSTAT
System bus (CPU)	BUSMCNTSYS	-	BUS3ERRADD	BUS3ERRSTAT
DMA bus	BUSMCNTDMA	-	BUS4ERRADD	BUS4ERRSTAT
Memory bus 1	-	BUSSCNTFLI	-	-
Memory bus 2	-	BUSSCNTRAMH	-	-
Memory bus 3	-	BUSSCNTMBIU	-	-
Internal peripheral bus 1, 3, 4, 5, 7	-	BUSSCNTPnB (n = 0, 2, 3, 4, 6)	-	-
Internal peripheral bus 9	-	BUSSCNTFBU	-	-

IERES bit (Ignore Error Responses)

The IERES bit, when set, disables the AHB-Lite protocol error response.

14.3.2 Slave Bus Control Register (BUSSCNT<slave>)

Address(es): BUS.BUSSCNTFLI 4000 4100h, BUS.BUSSCNTRAMH 4000 4104h, BUS.BUSSCNTMBIU 4000 4108h, BUS.BUSSCNTP0B 4000 4114h,BUS.BUSSCNTP2B 4000 4118h, BUS.BUSSCNTP3B 4000 411Ch, BUS.BUSSCNTP4B 4000 4120h, BUS.BUSSCNTP6B 4000 4128h, BUS.BUSSCNTFBU 4000 4130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EWRES	—	—	ARBMET[1:0]		—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	ARBMET[1:0]	Arbitration Method	Specifies the group priorities. b5 b4 0 0: Fixed priority 0 1: Round-robin 1 0: Setting prohibited 1 1: Setting prohibited.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	EWRES	Early Write Response	0: Disable early write response 1: Enable early write response.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Changing reserved bits from the initial value of 0 is prohibited. Operation during the change is not guaranteed.

Table 14.3 lists the registers associated with each bus type.

ARBMET[1:0] bits (Arbitration Method)

The ARBMET[1:0] bits specify the arbitration protocol, with priority defined for all bus masters. For fixed priority, see Table 14.4. For round-robin, see Table 14.5.

EWRES bit (Early Write Response)

The EWRES bit indicates whether the next write request is accepted before the response for the current write transaction occurs. When the value is 1, the next write request is accepted and high-speed transfer is possible, but AHB-Lite error responses are not detected. Bus errors are returned to the requesting master IP using the error response protocol for AHB-Lite. For details on errors that occur on each bus, see section 14.4, Bus Error Monitoring. Only use the BUSSCNTMBIU,

BUSSCNTP0B, and BUSSCNTEXT registers.

Table 14.4 Bus priorities with fixed-priority arbitration (ARBMET[1:0] = 00b)

Slave Bus Control Register	Slave interface	Priority order
BUSSCNTFLI	Memory bus 1	Memory bus 3 > DCode bus (CPU) > ICode bus (CPU)
BUSSCNTRAMH	Memory bus 2	Memory bus 3 > DCode bus (CPU) > ICode bus (CPU)
BUSSCNTPnB (n = 0, 2, 3, 4, 6)	Internal peripheral bus 1, 3, 4, 5, 7	DMA bus > system bus (CPU)
BUSSCNTFBU	Internal peripheral bus 9	DMA bus > system bus (CPU)

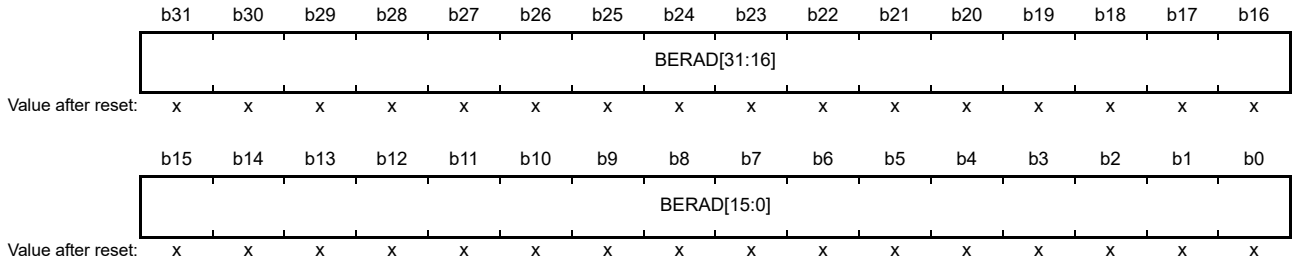
Table 14.5 Bus priorities with round-robin priority arbitration (ARBMET[1:0] = 01b)

Slave Bus Control Register	Slave interface	Priority order*1
BUSSCNTFLI	Memory bus 1	Memory bus 3 <=> DCode bus (CPU) <=> ICode bus (CPU)
BUSSCNTRAMH	Memory bus 2	Memory bus 3 <=> DCode bus (CPU) <=> ICode bus (CPU)
BUSSCNTPnB (n = 0, 2, 3, 4, 6)	Internal peripheral bus 1, 3, 4, 5, 7	DMA bus <=> system bus (CPU)
BUSSCNTFBU	Internal peripheral bus 9	DMA bus <=> system bus (CPU)

Note 1. Round-robin priority is denoted by <=>.

14.3.3 Bus Error Address Register (BUSnERRADD) (n = 1 to 4)

Address(es): BUS.BUS1ERRADD 4000 4800h, BUS.BUS2ERRADD 4000 4810h, BUS.BUS3ERRADD 4000 4820h, BUS.BUS4ERRADD 4000 4830h



x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	BERAD[31:0]	Bus Error Address	When a bus error occurs, these bits store the error address	R

Note: This register is cleared only by a reset that is not an MPU-related reset. For more information, see section 6, Resets, and section 15, Memory Protection Unit (MPU).

Table 14.3 lists the registers associated with each bus type.

BERAD[31:0] bits (Bus Error Address)

When a bus error occurs, the BERAD[31:0] bits store the access address. For more information, see the BUSnERRSTAT.ERRSTAT bit description and section 14.4, Bus Error Monitoring.

A value of BUSnERRADD.BERAD[31:0] (n = 1 to 4) is only valid when BUSnERRSTAT.ERRSTAT (n = 1 to 4) is set to 1.

14.3.4 Bus Error Status Register (BUSnERRSTAT) (n = 1 to 4)

Address(es): BUS.BUS1ERRSTAT 4000 4804h, BUS.BUS2ERRSTAT 4000 4814h, BUS.BUS3ERRSTAT 4000 4824h, BUS.BUS4ERRSTAT 4000 4834h

	b7	b6	b5	b4	b3	b2	b1	b0
	ERRSTAT	—	—	—	—	—	—	ACCSTAT
Value after reset:	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	ACCSTAT	Error Access Status	Access status when the error occurred: 1: Write access 0: Read access.	R
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ERRSTAT	Bus Error Status	0: No bus error occurred 1: Bus error occurred.	R

Note: This register is cleared only by a reset that is not an MPU-related reset. For more information, see section 6, Resets, and section 15, Memory Protection Unit (MPU).

Table 14.3 lists the registers associated with each bus type.

ACCSTAT bit (Error Access Status)

The ACCSTAT bit indicates the access status, write access or read access, when an error occurs on the associated bus. For more information, see the BUSnERRSTAT.ERRSTAT bit description and section 14.4, Bus Error Monitoring.

The value is only valid when BUSnERRSTAT.ERRSTAT (n = 1 to 4) is set to 1.

ERRSTAT bit (Bus Error Status)

The ERRSTAT bit indicates whether a bus error occurred. When an error occurs on the associated bus, the access address and status of write or read access are stored. BUSnERRSTATn.ERRSTAT (n = 1 to 4) is set to 1.

The following types of errors can occur on each bus:

- Illegal address access
- Bus master MPU error
- Bus slave MPU error
- Time out.

When detecting bus master MPU errors or bus slave MPU errors, and reset is selected in the respective OAD bit, BUSnERRSTAT.ERRSTAT (n = 1 to 4) is not set to 1 if the bus access that caused the MPU error completes later than the internal reset signal being generated, which may occur depending on the wait setting.

When detecting bus master MPU errors or bus slave MPU errors, and NMI is selected in the respective OAD bit, BUSnERRSTAT.ERRSTAT (n = 1 to 4) is set to 1 when the bus access that caused the MPU error completes.

For more information on errors that occur on each bus, see section 14.4, Bus Error Monitoring, and section 15, Memory Protection Unit (MPU).

14.4 Bus Error Monitoring

The bus error monitoring system monitors each individual area, and whenever an error is detected, it returns the error to the requesting master IP using the AHB-Lite error response protocol.

14.4.1 Bus Error Types

The following types of errors can occur on each bus:

- Illegal address access
- Bus master MPU error
- Bus slave MPU error
- Timeout.

Table 14.6 lists the address ranges where access leads to illegal address access errors. The reserved area in the slave does not trigger an illegal address access error. For more information on the bus master MPU and bus slave MPU, see section 15, Memory Protection Unit (MPU).

14.4.2 Operation when a Bus Error Occurs

When a bus error occurs, operation is not guaranteed and the error is returned to the requesting master IP. The bus errors that occur for each master are stored in the BUSnERRADD and BUSnERRSTAT registers. These registers must only be cleared by a reset. For more information, see section 14.3.3, Bus Error Address Register (BUSnERRADD) (n = 1 to 4) and section 14.3.4, Bus Error Status Register (BUSnERRSTAT) (n = 1 to 4).

Note: The DMAC and DTC do not receive bus errors. If the DMAC or DTC accesses the bus, the transfer continues.

14.4.3 Conditions Leading to Illegal Address Access Errors

Table 14.6 lists the address spaces for each bus that trigger illegal address access errors.

Table 14.6 Conditions leading to illegal address access errors

Address	Slave bus name	Master bus	
		CPU (ICode, DCode, System)	DMA
0000 0000h to 01FF FFFFh	Memory bus 1 Memory bus 3	-	-
0200 0000h to 027F FFFFh	Memory mapping area	*1	E
0280 0000h to 1FFD FFFFh	Reserved	E	E
1FFE 0000h to 1FFF FFFFh	Memory bus 2 Memory bus 3	-	-
2000 0000h to 200F FFFFh	Reserved	-	-
2010 0000h to 3FFF FFFFh	Reserved	E	E
4000 0000h to 4001 FFFFh	Peripheral bus 1	-	-
4002 0000h to 4003 FFFFh	Reserved	E	E
4004 0000h to 4005 FFFFh	Peripheral bus 3	-	-
4006 0000h to 4007 FFFFh	Peripheral bus 4	-	-
4008 0000h to 4009 FFFFh	Peripheral bus 5	-	-
400A 0000h to 400B FFFFh	Reserved	-	-
400C 0000h to 400D FFFFh	Peripheral bus 7	-	-
400E 0000h to 400F FFFFh	Reserved	E	E
4010 0000h to 407F FFFFh	Peripheral bus 9	-	-
4080 0000h to 5FFF FFFFh	Reserved	E	E
6000 0000h to 67FF FFFFh	Reserved	-	-
6800 0000h to 7FFF FFFFh	Reserved	E	E
8000 0000h to 97FF FFFFh	Reserved	-	-
9800 0000h to DFFF FFFFh	Reserved	E	E
E000 0000h to FFFF FFFFh	System for Cortex®-M4	-	E

E: Path where an illegal address access error occurs.

Note 1. The bus module does not detect whether the Memory Mirror Function (MMF) switched the address. Therefore, if the MMF is enabled and the CPU accesses 0200 0000h, no error occurs. This depends on the switched address.

If the MMF is disabled and the CPU accesses 0200 0000h, the bus module can detect the error.

The bus module detects an access error resulting from access to a reserved area, for example if no area is assigned to the slave:

- 0200 0000h to 1FFD FFFFh: access error detection
- 0000 0000h to 01FF FFFFh: memory bus 1 no access error detection.

14.4.4 Timeout

For some peripheral modules, a timeout error occurs with the module-stop function. When there is no response from the slave for a certain period of time, a timeout error is detected and is returned to the requesting master IP using the AHB-Lite error response protocol.

14.5 Notes on using Flash Cache

When using the flash cache through access from the CPU, the Arm MPU should also be set to cacheable. See references 1. and 2. for more information.

14.6 References

1. *ARM®v7-M Architecture Reference Manual* (ARM DDI 0403D)
2. *ARM® Cortex®-M4 Devices Generic User Guide* (ARM DUI 0553A).

15. Memory Protection Unit (MPU)

15.1 Overview

The MCU has four Memory Protection Units (MPUs) and a CPU stack pointer monitor function. Table 15.1 lists the MPU specifications and Table 15.2 shows the behavior on detection of each MPU error.

Table 15.1 MPU specifications

Classification	Module/Function	Specifications
Illegal memory access	Arm® Cortex®-M4 CPU	• Arm CPU has a default memory map. If the CPU makes an illegal access, an exception interrupt occurs. • The MPU can change a default memory map.
	CPU stack pointer monitor	2 regions: • Main Stack Pointer (MSP) • Process Stack Pointer (PSP).
Memory protection	Arm MPU	Memory protection function for the CPU: • 8 MPU regions with subregions and background region.
	Bus master MPU	Memory protection function for each bus master except for the CPU: • Bus master MPU group A: 32 regions.
	Bus slave MPU	Memory protection function for each bus slave
Security	Security MPU	Protect accesses from non-secure programs to the following secure regions: • 2 regions (PC) • 4 regions (code flash, SRAM, two secure functions).

Table 15.2 Behavior on MPU error detection

MPU type	Notification type	Bus access on error detection	Storing of error access information
CPU stack pointer monitor	Reset or non-maskable interrupt	Don't care	Not stored
Arm MPU	Hard fault	• Does not correctly have write access • Does not correctly have read access.	Stored in the Cortex-M4 processor
Bus master MPU	Reset or non-maskable interrupt	• Write access to the protection region • Read access to the protection region.	Stored
Bus slave MPU	• Reset or non-maskable interrupt • Hard fault.	• Write access ignored • Read access read as 0.	Stored
Security MPU	Not notified	• Does not correctly have write access • Does not correctly have read access.	Not stored

For information on error access for the Arm MPU, see section 15.7. For information on error access for other MPUs, see section 14.3.3, Bus Error Address Register (BUSnERRADD) (n = 1 to 4) and section 14.3.4, Bus Error Status Register (BUSnERRSTAT) (n = 1 to 4) in section 14, Buses.

15.2 CPU Stack Pointer Monitor

The CPU stack pointer monitor detects underflows and overflows of the stack pointer. Because the Arm CPU has two stack pointers, a Main Stack Pointer (MSP) and a Process Stack Pointer (PSP), it supports two CPU stack pointer monitors. If a stack pointer underflow or overflow is detected, the CPU stack pointer monitor generates a reset or a non-maskable interrupt.

The CPU stack pointer monitor is enabled by setting the Stack Pointer Monitor Enable bit in the Stack Pointer Monitor Access Control Register (MSPMPUCTL, PSPMPUCTL) to 1.

Table 15.3 lists the specifications of the CPU stack pointer monitor, Figure 15.1 shows a block diagram, and Figure 15.2 shows the register setting flow.

Table 15.3 CPU stack pointer monitor specifications

Parameter	Description
SRAM region	Region to be covered by memory protection
Number of regions	2 regions: • Main Stack Pointer (MSP) • Process Stack Pointer (PSP).
Address specification for individual regions	Region start and end addresses configurable
Stack pointer monitor enable or disable setting for individual regions	Stack pointer monitor for individual regions can be enabled or disabled
Operation on error detection	Reset or non-maskable interrupts can be generated
Register protection	Registers can be protected from illegal writes

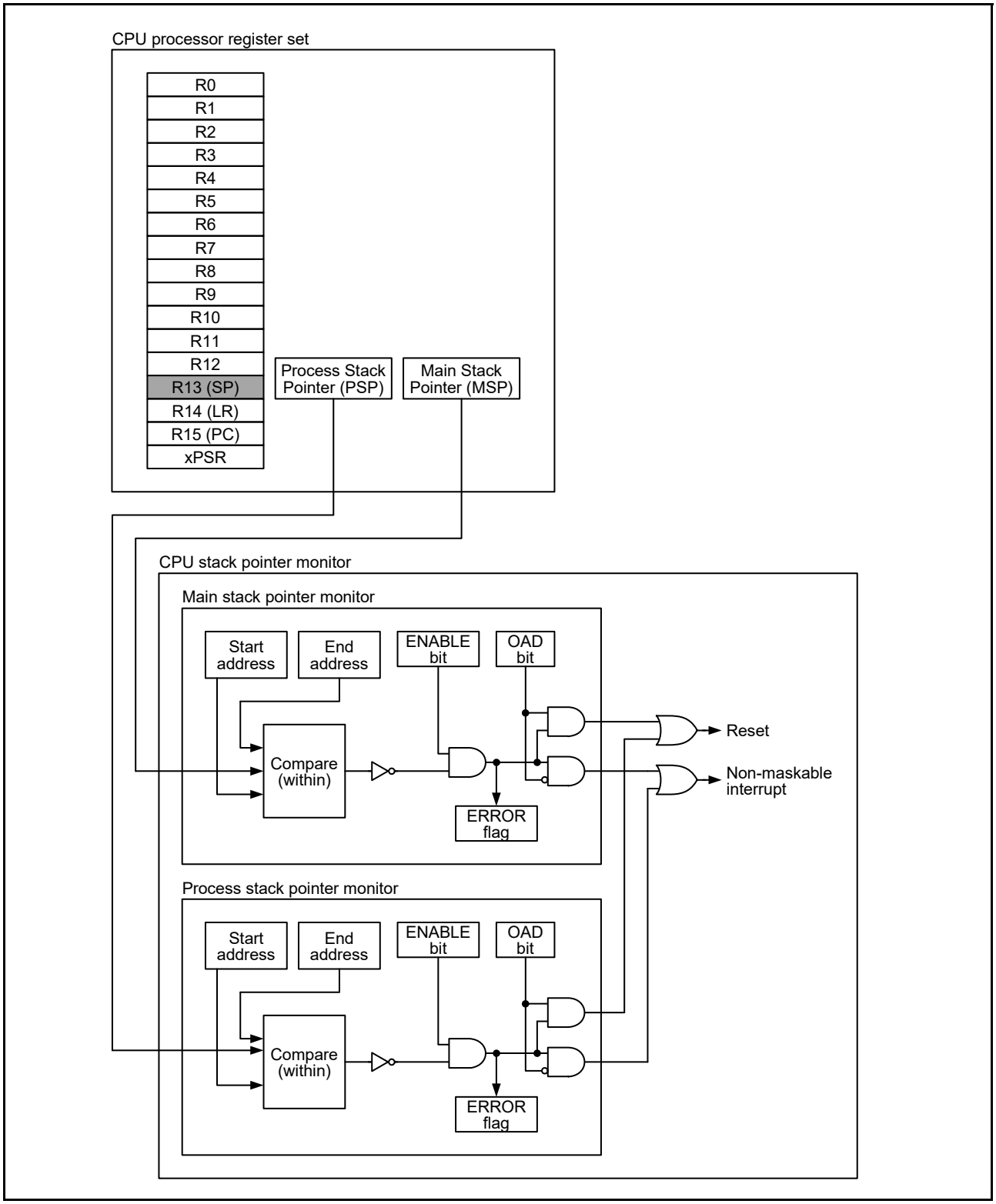


Figure 15.1 CPU stack pointer monitor block diagram

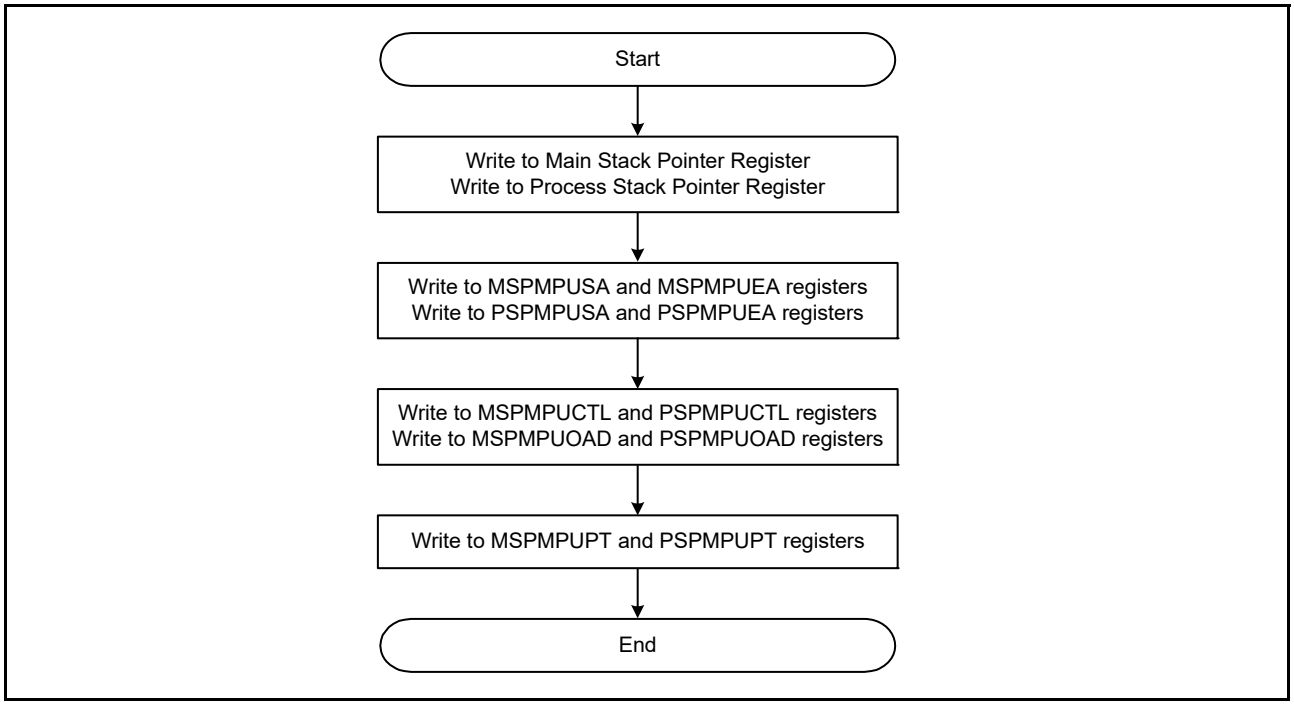


Figure 15.2 Register setting flow

15.2.1 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

15.2.1.1 Main Stack Pointer Monitor Start Address Register (MSPMPUSA)

Address(es): SPMON.MSPMPUSA 4000 0D08h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MSPMPUSA[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits should be 0. The value range is from 1FF0 0000h to 1FFE FFFCh, excluding reserved areas.	R/W

The MSPMPUSA and MSPMPUEA registers specify the CPU stack region in the SRAM (1FF0 0000h to 1FFE FFFFh, excluding reserved areas). For SRAM area to be covered, see Figure 4.1, Memory map.

15.2.1.2 Main Stack Pointer Monitor End Address Register (MSPMPUEA)

Address(es): SPMON.MSPMPUEA 4000 0D0Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MSPMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1. The value range is from 1FF0 0003h to 1FFE FFFFh, excluding reserved areas.	R/W

15.2.1.3 Process Stack Pointer Monitor Start Address Register (PSPMPUSA)

Address(es): SPMON.PSPMPUSA 4000 0D18h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	PSPMPUSA[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits should be 0. The value range is from 1FF0 0000h to 1FFE FFFCh, excluding reserved areas.	R/W

The PSPMPUSA and PSPMPUEA registers specify the CPU stack region in the SRAM (1FF0 0000h to 1FFE FFFFh, excluding reserved areas). For SRAM area to be covered, see Figure 4.1, Memory map.

15.2.1.4 Process Stack Pointer Monitor End Address Register (PSPMPUEA)

Address(es): SPMON.PSPMPUEA 4000 0D1Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	PSPMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1. The value range is from 1FF0 0003h to1FFE FFFFh, excluding reserved areas.	R/W

15.2.1.5 Stack Pointer Monitor Operation After Detection Register (MSPMPUOAD, PSPMPUOAD)

Address(es): SPMON.MSPMPUOAD 4000 0D00h, SPMON.PSPMPUOAD 4000 0D10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation after Detection	0: Non-maskable interrupt 1: Reset.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD bit	R/(W)*1

Note 1. Write data is not saved.

OAD bit (Operation after Detection)

The OAD bit selects either a reset or a non-maskable interrupt when a stack pointer underflow or overflow is detected by the CPU stack pointer monitor.

The main and the process stack pointer monitors each uses an OAD bit to determine which signal is generated when a stack pointer underflow or overflow is detected. When writing to the OAD bit, write A5h simultaneously to the KEY[7:0] bits using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the OAD bit. When writing to the OAD bit, write A5h simultaneously to the KEY[7:0] bits. When values other than A5h are written to the KEY[7:0] bits, the OAD bit is not updated. The KEY[7:0] bits are always read as 00h.

15.2.1.6 Stack Pointer Monitor Access Control Register (MSPMPUCTL, PSPMPUCTL)

Address(es): SPMON.MSPMPUCTL 4000 0D04h, SPMON.PSPMPUCTL 4000 0D14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ERROR	—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0/1*1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Stack Pointer Monitor Enable	0: Disable stack pointer monitor 1: Enable stack pointer monitor.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	ERROR	Stack Pointer Monitor Error Flag	0: No stack pointer overflow or underflow occurred 1: Stack pointer overflow or underflow occurred.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The initial value depends on the reset generation source.

ENABLE bit (Stack Pointer Monitor Enable)

The ENABLE bit enables or disables the stack pointer monitor function, independently set for the main stack pointer monitor and the process stack pointer monitor.

When the MSPMPUCTL.ENABLE bit is set to 1, the following registers are available:

- MSPMPUSA
- MSPMPUEA
- MSPMPUOAD.

When the PSPMPUCTL.ENABLE bit is set to 1, the following registers are available:

- PSPMPUSA
- PSPMPUEA
- PSPMPUOAD.

ERROR bit (Stack Pointer Monitor Error Flag)

The ERROR bit indicates the status of the stack pointer monitor. Each stack pointer monitor has an independent ERROR bit.

[Setting condition]

- Overflow or underflow of the stack pointer.

[Clearing condition]

- 0 is written to this bit
- A reset other than the bus master MPU error reset, bus slave MPU error reset, and stack pointer error reset.

Note: Only 0 can be written to the ERROR bit.

15.2.1.7 Stack Pointer Monitor Protection Register (MSPMPUPT, PSPMPUPT)

Address(es): SPMON.MSPMPUPT 4000 0D06h, SPMON.PSPMPUPT 4000 0D16h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PROTECT	Protection of Register	0: Stack pointer monitor register writes are permitted 1: Stack pointer monitor register writes are protected. Reads are permitted.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the PROTECT bit.	R/(W)*1

Note 1. Write data is not saved.

PROTECT bit (Protection of Register)

The PROTECT bit enables or disables writes to the associated registers to be protected, independently set for the main stack pointer monitor and the process stack pointer monitor.

MSPMPUPT.PROTECT controls the following main stack pointer protection registers:

- MSPMPUCTL
- MSPMPUSA
- MSPMPUEA.

PSPMPUT.PROTECT controls the following process stack pointer protection registers:

- PSPMPUCTL
- PSPMPUSA
- PSPMPUEA.

When writing to the PROTECT bit, simultaneously write A5h to the KEY[7:0] bits, using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, simultaneously write A5h to the KEY[7:0] bits. When other values are written, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 00h.

15.2.2 Operation

15.2.2.1 Protecting the registers

To protect registers related to the CPU stack pointer monitor, set the associated PROTECT bit.

15.2.2.2 Overflow and underflow errors

The CPU stack pointer monitor generates an error if an overflow or underflow error is detected. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or reset. The non-maskable interrupt status is indicated in ICU.NMISR.SPEST, see section 13, Interrupt Controller Unit (ICU). Reset status is indicated in SYSTEM.RSTSR1.SPERF, see section 6, Resets.

When ICU.NMISR.SPEST indicates that a CPU stack pointer monitor interrupt occurred, confirm it by checking the ERROR bit in MSPMPUCTL and PSPMPUCTL to determine whether the error is a main stack pointer monitor error or process stack pointer monitor error.

A non-maskable interrupt remains set when a stack pointer overflows or underflows. To clear the error, clear the non-maskable interrupt flag by writing 1 to ICU.NMICLR.SPECLR. Write 0 to clear the ERROR bit in MSPMPUCTL or PSPMPUCTL.

15.3 Arm MPU

The Arm MPU provides full support for:

- 8 protected regions
- Overlapping protected regions, with ascending priority:
  7 = highest priority
  0 = lowest priority.
- Access permissions
- Export of memory attributes to the system.

Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (HardFault) handler. For details, see section 15.7.

15.4 Bus Master MPU

The bus master MPU monitors the addresses accessed by the bus masters in the entire address space (0000 0000h to FFFF FFFFh). The access control information, consisting of read and write permissions, can be independently set for up to 32 regions. The bus master MPU monitors access to each region based on these settings. If access to a protected region is detected, the bus master MPU generates a reset or a non-maskable interrupt. For details on error access, see section 14.3.3 and section 14.3.4 in section 14, Buses.

Table 15.4 lists the specifications of the bus master MPU and Figure 15.3 shows a block diagram. Figure 15.4 shows bus master MPU group A.

Table 15.4 Bus master MPU specifications

Parameter	Specifications
Protected master groups	Bus master MPU group A: DMA bus.
Protected region	0000 0000h to FFFF FFFFh
Number of regions	Bus master MPU group A: 32 regions.
Address specification for individual regions	Region start and end addresses configurable
Enable/disable setting for memory protection in individual regions	Settings enabled or disabled for the associated region
Access-control settings for individual regions	Permission to read and write
Operation on error detection	Reset or non-maskable interrupt
Register protection	Register can be protected from illegal writes

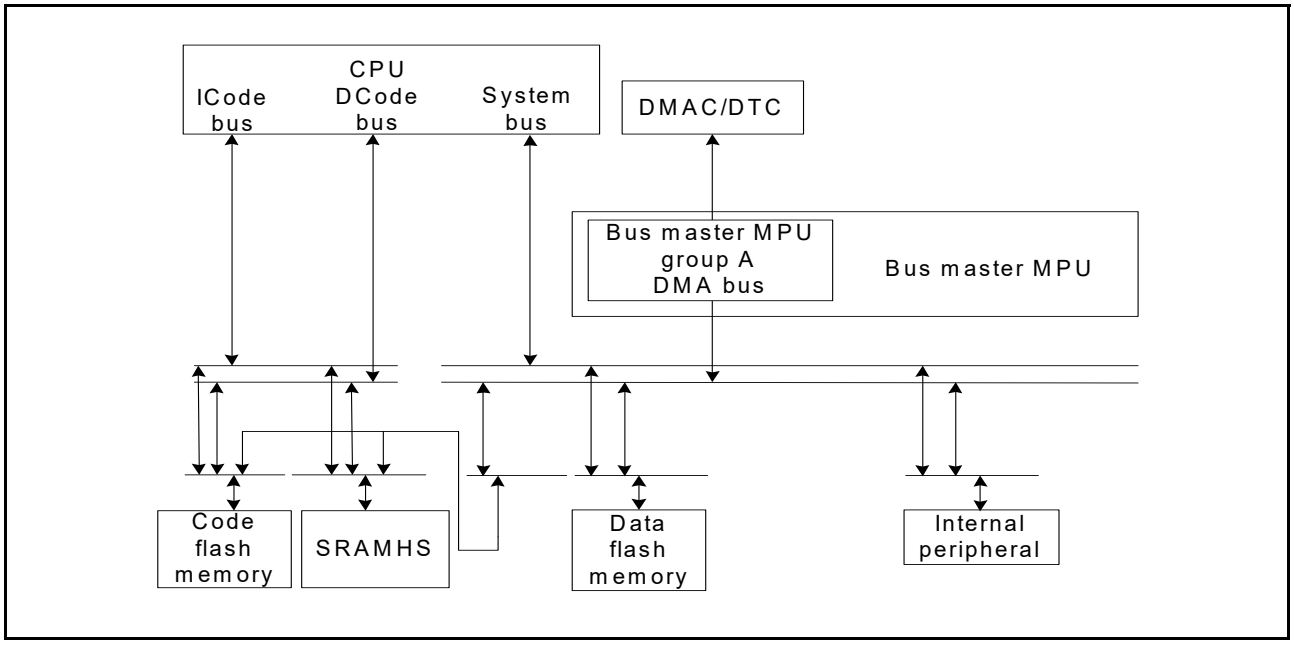


Figure 15.3 MPU bus master block diagram

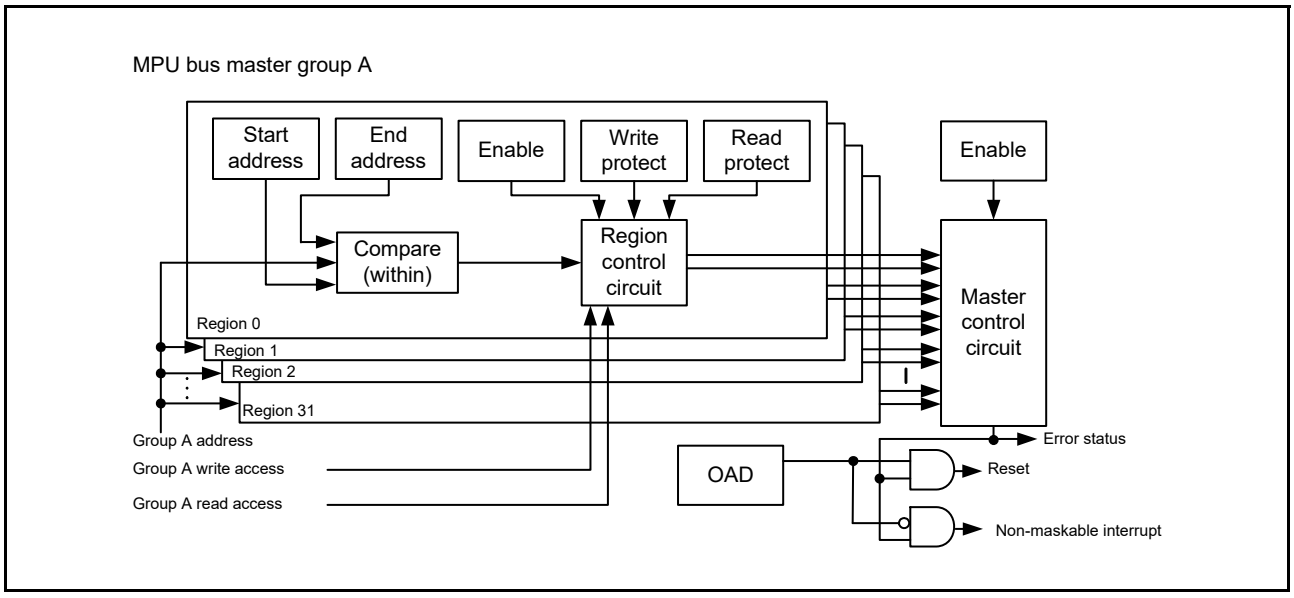


Figure 15.4 MPU bus master group A

15.4.1 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

15.4.1.1 Group A Region n Start Address Register (MMPUSAn) (n = 0 to 31)

Address(es): MMPU.MMPUSA0 4000 0204h, MMPU.MMPUSA1 4000 0214h, MMPU.MMPUSA2 4000 0224h, MMPU.MMPUSA3 4000 0234h, MMPU.MMPUSA4 4000 0244h, MMPU.MMPUSA5 4000 0254h, MMPU.MMPUSA6 4000 0264h, MMPU.MMPUSA7 4000 0274h, MMPU.MMPUSA8 4000 0284h, MMPU.MMPUSA9 4000 0294h, MMPU.MMPUSA10 4000 02A4h, MMPU.MMPUSA11 4000 02B4h, MMPU.MMPUSA12 4000 02C4h, MMPU.MMPUSA13 4000 02D4h, MMPU.MMPUSA14 4000 02E4h, MMPU.MMPUSA15 4000 02F4h, MMPU.MMPUSA16 4000 0304h, MMPU.MMPUSA17 4000 0314h, MMPU.MMPUSA18 4000 0324h, MMPU.MMPUSA19 4000 0334h, MMPU.MMPUSA20 4000 0344h, MMPU.MMPUSA21 4000 0354h, MMPU.MMPUSA22 4000 0364h, MMPU.MMPUSA23 4000 0374h, MMPU.MMPUSA24 4000 0384h, MMPU.MMPUSA25 4000 0394h, MMPU.MMPUSA26 4000 03A4h, MMPU.MMPUSA27 4000 03B4h, MMPU.MMPUSA28 4000 03C4h, MMPU.MMPUSA29 4000 03D4h, MMPU.MMPUSA30 4000 03E4h, MMPU.MMPUSA31 4000 03F4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MMPUSA[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits should be 0.	R/W

15.4.1.2 Group A Region n End Address Register (MMPUEAn) (n = 0 to 31)

Address(es): MMPU.MMPUEA0 4000 0208h, MMPU.MMPUEA1 4000 0218h, MMPU.MMPUEA2 4000 0228h, MMPU.MMPUEA3 4000 0238h, MMPU.MMPUEA4 4000 0248h, MMPU.MMPUEA5 4000 0258h, MMPU.MMPUEA6 4000 0268h, MMPU.MMPUEA7 4000 0278h, MMPU.MMPUEA8 4000 0288h, MMPU.MMPUEA9 4000 0298h, MMPU.MMPUEA10 4000 02A8h, MMPU.MMPUEA11 4000 02B8h, MMPU.MMPUEA12 4000 02C8h, MMPU.MMPUEA13 4000 02D8h, MMPU.MMPUEA14 4000 02E8h, MMPU.MMPUEA15 4000 02F8h, MMPU.MMPUEA16 4000 0308h, MMPU.MMPUEA17 4000 0318h, MMPU.MMPUEA18 4000 0328h, MMPU.MMPUEA19 4000 0338h, MMPU.MMPUEA20 4000 0348h, MMPU.MMPUEA21 4000 0358h, MMPU.MMPUEA22 4000 0368h, MMPU.MMPUEA23 4000 0378h, MMPU.MMPUEA24 4000 0388h, MMPU.MMPUEA25 4000 0398h, MMPU.MMPUEA26 4000 03A8h, MMPU.MMPUEA27 4000 03B8h, MMPU.MMPUEA28 4000 03C8h, MMPU.MMPUEA29 4000 03D8h, MMPU.MMPUEA30 4000 03E8h, MMPU.MMPUEA31 4000 03F8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1.	R/W

15.4.1.3 Group A Region n Access Control Register (MMPUACAn) (n = 0 to 31)

Address(es): MMPU.MMPUACA0 4000 0200h, MMPU.MMPUACA1 4000 0210h, MMPU.MMPUACA2 4000 0220h, MMPU.MMPUACA3 4000 0230h, MMPU.MMPUACA4 4000 0240h, MMPU.MMPUACA5 4000 0250h, MMPU.MMPUACA6 4000 0260h, MMPU.MMPUACA7 4000 0270h, MMPU.MMPUACA8 4000 0280h, MMPU.MMPUACA9 4000 0290h, MMPU.MMPUACA10 4000 02A0h, MMPU.MMPUACA11 4000 02B0h, MMPU.MMPUACA12 4000 02C0h, MMPU.MMPUACA13 4000 02D0h, MMPU.MMPUACA14 4000 02E0h, MMPU.MMPUACA15 4000 02F0h, MMPU.MMPUACA16 4000 0300h, MMPU.MMPUACA17 4000 0310h, MMPU.MMPUACA18 4000 0320h, MMPU.MMPUACA19 4000 0330h, MMPU.MMPUACA20 4000 0340h, MMPU.MMPUACA21 4000 0350h, MMPU.MMPUACA22 4000 0360h, MMPU.MMPUACA23 4000 0370h, MMPU.MMPUACA24 4000 0380h, MMPU.MMPUACA25 4000 0390h, MMPU.MMPUACA26 4000 03A0h, MMPU.MMPUACA27 4000 03B0h, MMPU.MMPUACA28 4000 03C0h, MMPU.MMPUACA29 4000 03D0h, MMPU.MMPUACA30 4000 03E0h, MMPU.MMPUACA31 4000 03F0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Region Enable	0: Group A region n unit disabled 1: Group A region n unit enabled.	R/W
b1	RP	Read Protection	0: Read access permitted 1: Read access protected.	R/W
b2	WP	Write Protection	0: Write access permitted 1: Write access protected.	R/W
b15 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ENABLE, RP, and WP bits are individually configurable for each group A region n unit.

ENABLE bit (Region Enable)

The ENABLE bit enables or disables the group A region n unit. When the ENABLE bit is set to 1, the RP and WP bits can be set to permit or protect access to the region that is set in MMPUSAn and MMPUEAn. When the ENABLE bit is set to 0, no region is specified for group A region n access.

RP bit (Read Protection)

The RP bit enables or disables read protection for group A region n. The RP bit is available when the ENABLE bit is set to 1.

WP bit (Write Protection)

The WP bit enables or disables write protection for group A region n. The WP bit is available when the ENABLE bit is set to 1.

Table 15.5 Function of region control circuit

MMPUACAn.ENABLE*1	MMPUACAn.RP*1	MMPUACAn.WP*1	Access	Region	Output of group A region n unit*1
0	-	-	Read	-	Outside of region
			Write	-	Outside of region
1	0	0	Read	Inside	Permitted region
				Outside	Outside of region
			Write	Inside	Permitted region
				Outside	Outside of region
	0	1	Read	Inside	Permitted region
				Outside	Outside of region
			Write	Inside	Protected region
				Outside	Outside of region
	1	0	Read	Inside	Protected region
				Outside	Outside of region
			Write	Inside	Permitted region
				Outside	Outside of region
	1	1	Read	Inside	Protected region
				Outside	Outside of region
			Write	Inside	Protected region
				Outside	Outside of region

Note 1. n = 0 to 31.

Table 15.6 Function of master control circuit

MMPUCTLA.ENABLE	Output of group A region 0 unit	Output of group A region 1 unit	Output of Group A Region 2 to 31 unit	Function of group A
1	Protected region	Don't care	Don't care	Generate error
1	Don't care	Protected region	Don't care	Generate error
1	Don't care	Don't care	Protected region	Generate error
1	Outside of region	Outside of region	Outside of region	Generate error
Other case				No error

A master MPU error occurs on the following conditions:

- MMPUCTLA.ENABLE = 1, and output of one or more region n units is to a protected region
- MMPUCTLA.ENABLE = 1, and output of all region n units is outside of region.

Other cases are handled as permitted regions.

15.4.1.4 Bus Master MPU Control Register (MMPUCTLA)

Address(es): MMPU.MMPUCTLA 4000 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	OAD	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Master Group Enable	0: Master group A disabled 1: Master group A enabled.	R/W

Bit	Symbol	Bit name	Description	R/W
b1	OAD	Operation After Detection	0: Non-maskable interrupt 1: Reset.	R/W
b7 to b2	—	Reserved	These bits are read as 0.The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD and ENABLE bits.	R/(W)*1

Note 1. Write data is not saved.

ENABLE bit (Master Group Enable)

The ENABLE bit enables or disables the bus master MPU function of master group A. When this bit is set to 1, MMPUACAn is available. When this bit is set to 0, MMPUACAn is unavailable, including permission for all regions. When writing to the ENABLE bit, simultaneously write A5h to the KEY[7:0] bits using halfword access.

OAD bit (Operation After Detection)

The OAD bit generates either a reset or a non-maskable interrupt when access to the protected region is detected by the bus master MPU. When writing to the OAD bit, simultaneously write A5h to the KEY[7:0] bits using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the ENABLE and OAD bits. When writing to the ENABLE and OAD bits, simultaneously write A5h to the KEY[7:0] bits. When other values are written, the ENABLE and OAD bits are not updated. The KEY[7:0] bits are always read as 00h.

15.4.1.5 Group A Protection of Register (MMPUPTA)

Address(es): MMPU.MMPUPTA 4000 0102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PROTECT	Protection of Register	0: All bus master MPU group A register writes are permitted 1: All bus master MPU group A register writes are protected. Reads are possible.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the PROTECT bit.	R/(W)*1

Note 1. Write data is not saved.

PROTECT bit (Protection of Register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPUTA.PROTECT controls the bus master MPU group A protection registers. The following registers are protected by MMPUPTA.PROTECT:

- MMPUSAn
- MMPUEAn
- MMPUACAn
- MMPUCTLA.

When writing to the PROTECT bit, simultaneously write A5h to the KEY[7:0] bits using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, simultaneously

write A5h to the KEY[7:0] bits. When values other than A5h are written to the KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 00h.

15.4.2 Operation

15.4.2.1 Memory protection

The bus master MPU monitors memory access using control settings made individually for the access control regions. If access to a protected region is detected, the bus master MPU generates a memory protection error.

The bus master MPU can be configured for up to 32 protected regions. Protected regions include those with overlapping permitted and protected regions, and those with two overlapping permitted regions.

The bus master MPU provides group A. The memory protection function checks the address of the bus for a unified master group, and all master group accesses are protected. The bus master MPU sets the permission for all of the regions after reset. Setting MMPUCTLA.ENABLE to 1 protects all of the regions. A permitted region is set up within the protected region for each region. If access to a protected region is detected, the bus master MPU generates an error.

Figure 15.5 shows the use case of a bus master MPU.

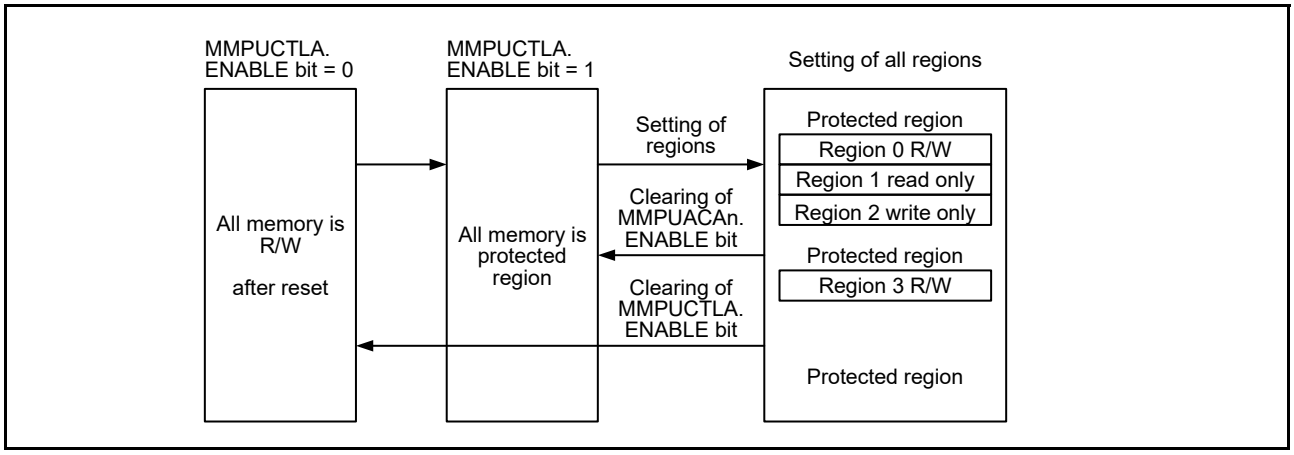


Figure 15.5 Use case of bus master MPU

Figure 15.6 shows the access permission or protection for overlapping bus master MPU regions. Access control for overlapping regions is as follows:

- The region is handled as a protected region when output of one or more region units is a protected region
- The region is handled as a protected region when output of all region units is outside of the regions
- Other cases are handled as permitted regions.

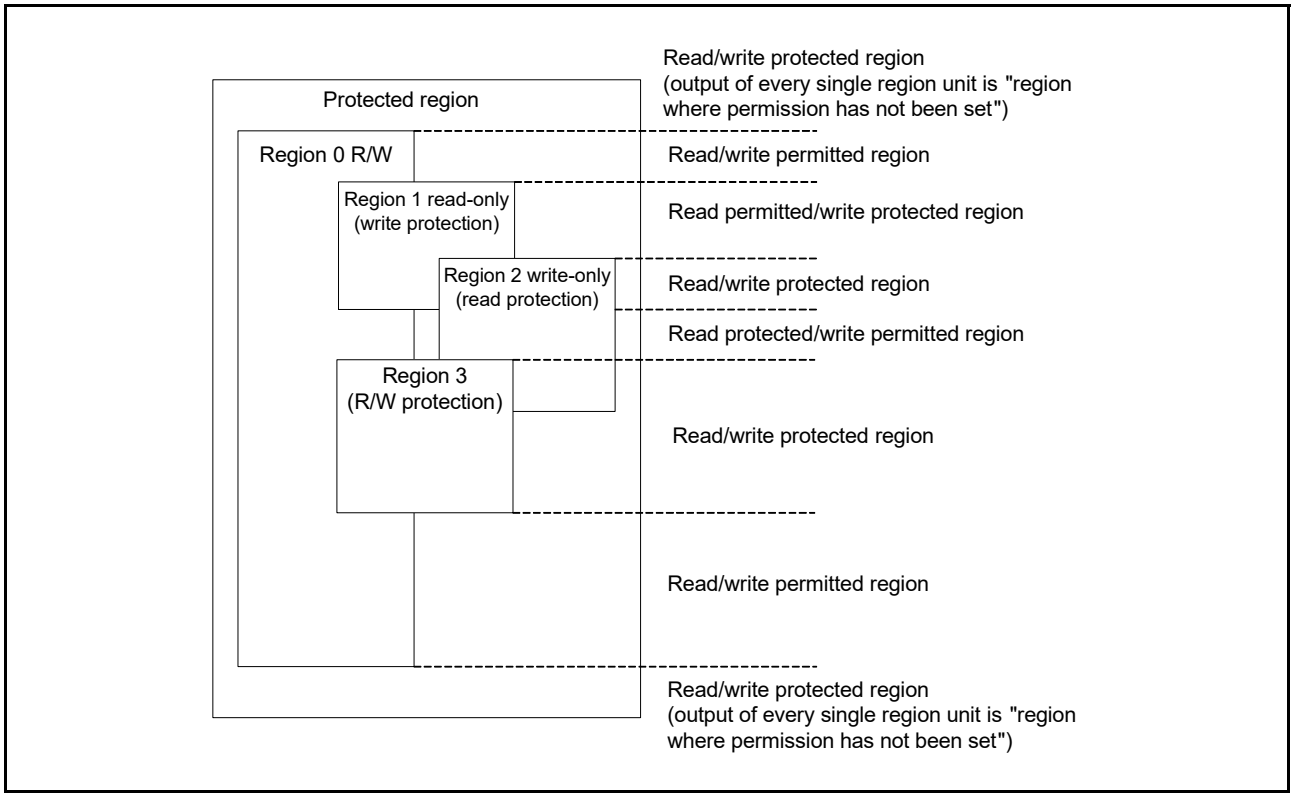


Figure 15.6 Access permission or protection by overlap of the bus master MPU regions

Figure 15.7 shows the register setting flow after reset. During this register setting, stop all the masters except the CPU.

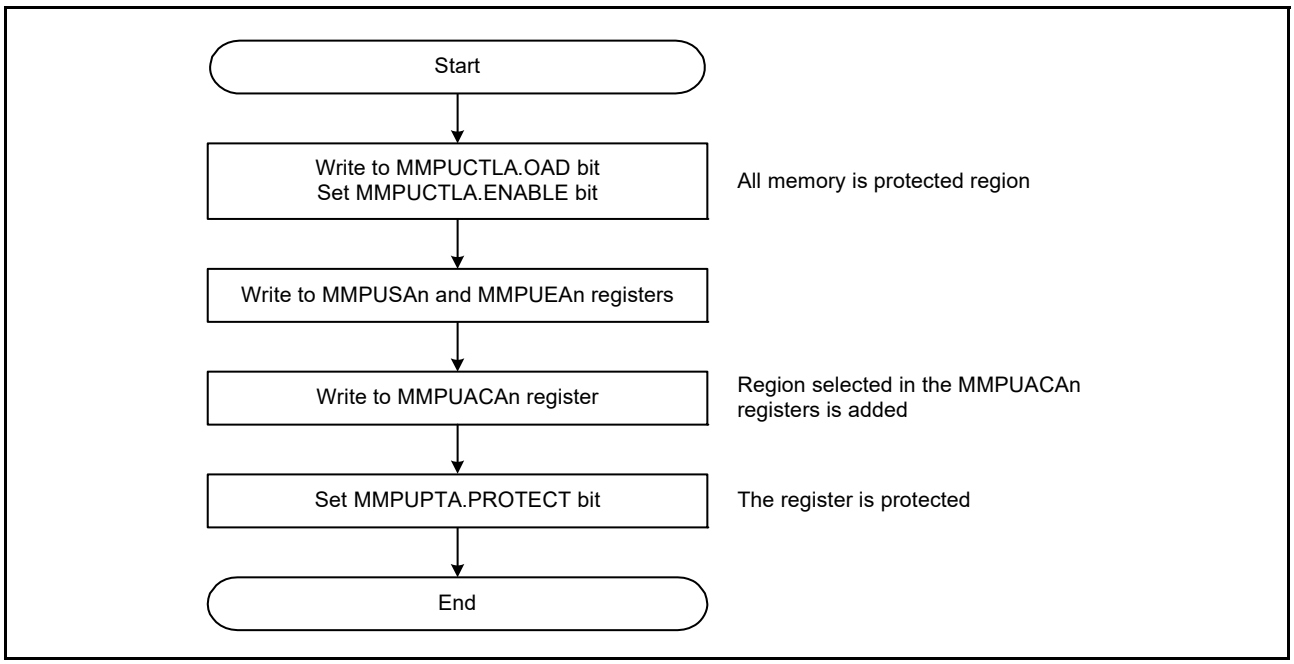


Figure 15.7 Register setting flow after reset

Figure 15.8 shows the register setting flow for adding regions. During this register setting, stop all masters except the CPU.

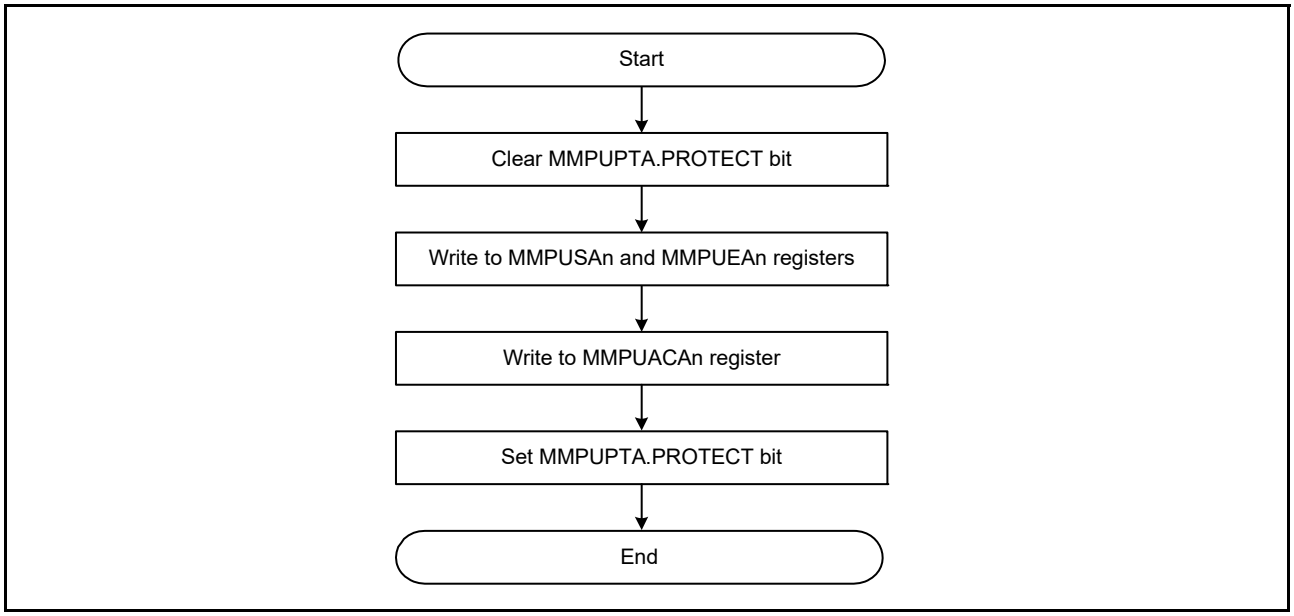


Figure 15.8 Register setting flow for region addition

15.4.2.2 Protecting the registers

To protect the registers related to the bus master MPU, set the PROTECT bit in the associated MMPUPTA register.

15.4.2.3 Memory protection error

If access to a protected region is detected, the bus master MPU generates an error. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or a reset. The non-maskable interrupt status is indicated in ICU.NMISR.BUSMST. For details, see section 13, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSMRF. For details, see section 6, Resets.

15.5 Bus Slave MPU

The bus slave MPU monitors access to the bus slave functions, such as flash or SRAM. The function can be accessed from two bus masters, the CPU, and the bus master MPU group A. The bus slave MPU has a separate protection register for each of the two bus masters, with individual access protection control, consisting of read and write permissions. If access to a protected region is detected, the bus slave MPU generates a reset or a non-maskable interrupt, and stores the bus error address, bus error status, and error access status. For details, see 14.3.3 and 14.3.4 in section 14, Buses.

Table 15.7 lists the specifications of the bus slave MPU and Figure 15.9 shows a block diagram.

Table 15.7 Specifications of bus slave MPU

Specifications	Description
Protected bus master	Bus master MPU group A: DMA bus.
Protected slave functions	• Memory bus 3: Code flash memory, SRAMHS • Internal peripheral bus 1: Connected to peripheral modules (DTC, DMAC, interrupt controller, flash registers, MPU, SRAM registers, system controller, and bus controller) • Internal peripheral bus 3, 4, 5: Connected to other peripherals • Internal peripheral bus 7: Connected to Secure IP (SCE7) • Internal peripheral bus 9: Flash memory (in P/E), data flash memory, and TSN.
‘	Permission to read and write
Operation on error detection	Reset, non-maskable interrupt, or exception
Protection of register	Register can be protected from illegal writes

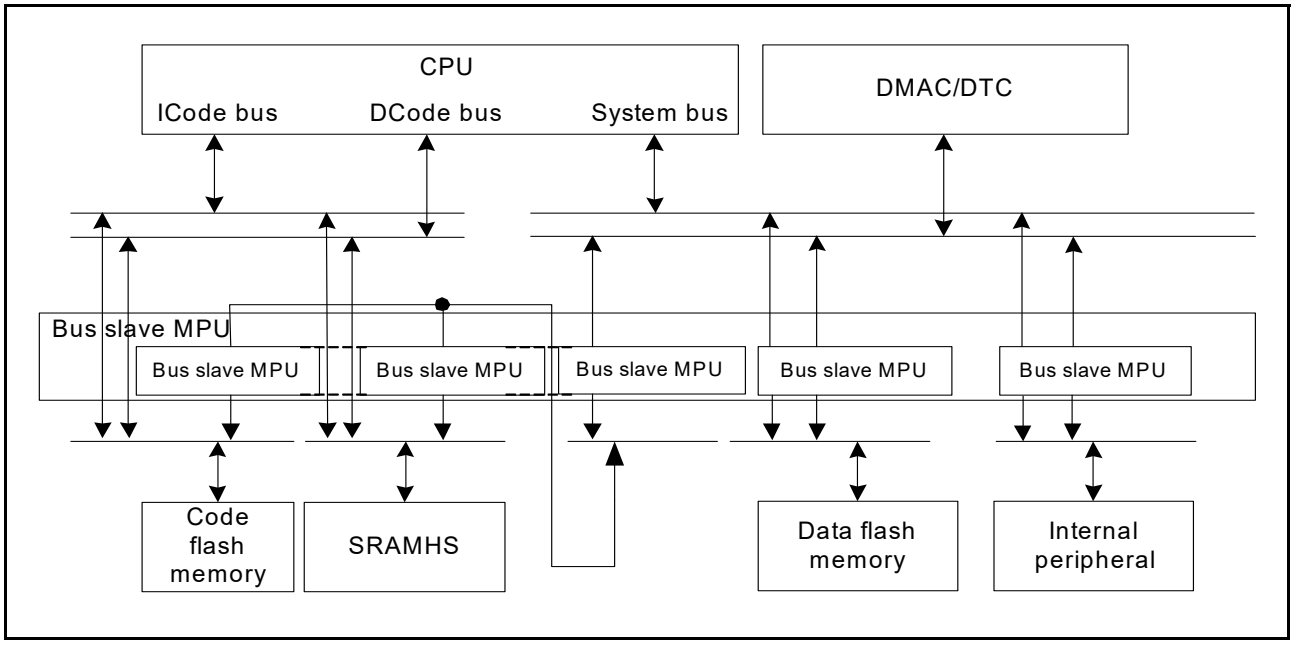


Figure 15.9 Bus slave MPU block diagram

15.5.1 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

15.5.1.1 Access Control Register for Memory Bus 3 (SMPUMBIU)

Address(es): SMPU.SMPUMBIU 4000 0C10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WPSRAMHS	RPSRAMHS	WPFLI	RPFLI	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	—	—
Value after reset:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b11 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	RPFLI	Code Flash Memory Read Protection	0: Memory protection for code flash memory reads from master group A disabled 1: Memory protection for code flash memory reads from master group A enabled.	R/W
b13	WPFLI	Code Flash Memory Write Protection	0: Memory protection for code flash memory writes from master group A disabled 1: Memory protection for code flash memory writes from master group A enabled. This bit is read as 1. The write value should be 1.	R/W
b14	RPSRAMHS	SRAMHS Read Protection	0: Memory protection for SRAMHS reads from master group A disabled 1: Memory protection for SRAMHS reads from master group A enabled.	R/W

Bit	Symbol	Bit name	Description	R/W
b15	WPSRAMHS	SRAMHS Write Protection	0: Memory protection for SRAMHS writes from master group A disabled 1: Memory protection for SRAMHS writes from master group A enabled.	R/W

The SMPUMBIU register enables memory protection for the specified master and slave for access from master group A to code flash memory and SRAMHS.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on memory bus 3.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on memory bus 3.

RPFLI bit (Code Flash Memory Read Protection)

The RPFLI bit enables or disables memory protection for reads by master group A on the code flash memory.

WPFLI bit (Code Flash Memory Write Protection)

The WPFLI bit enables memory protection for writes by master group A on the code flash memory.

RPSRAMHS bit (SRAMHS Read Protection)

The RPSRAMHS bit enables or disables memory protection for reads by master group A on the SRAMHS.

WPSRAMHS bit (SRAMHS Write Protection)

The WPSRAMHS bit enables or disables memory protection for writes by master group A on the SRAMHS.

15.5.1.2 Access Control Register for Internal Peripheral Bus 9 (SMPUFBIU)

Address(es): SMPU.SMPUFBIU 4000 0C14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on internal peripheral bus 9.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on internal peripheral bus 9.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on internal peripheral bus 9.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on internal peripheral bus 9.

15.5.1.3 Access Control Register for Internal Peripheral Bus 1 (SMPUP0BIU)

Address(es): SMPU.SMPUP0BIU 4000 0C20h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b5, b4	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on internal peripheral bus 1.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on internal peripheral bus 1.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on internal peripheral bus 1.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on internal peripheral bus 1.

15.5.1.4 Access Control Register for Internal Peripheral Bus 3 (SMPUP2BIU)

Address(es): SMPU.SMPUP2BIU 4000 0C24h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W

Bit	Symbol	Bit name	Description	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b5, b4	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on internal peripheral buses 3, 4, and 5.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on internal peripheral buses 3, 4, and 5.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on internal peripheral buses 3, 4, and 5.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on internal peripheral buses 3, 4, and 5.

15.5.1.5 Access Control Register for Internal Peripheral Bus 7 (SMPUP6BIU)

Address(es): SMPU.SMPUP6BIU 4000 0C28h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b5, b4	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on internal peripheral bus 7.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on internal peripheral bus 7.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on internal peripheral bus 7.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on internal peripheral bus 7.

15.5.1.6 Slave MPU Control Register (SMPUCTL)

Address(es): SMPU.SMPUCTL 4000 0C00h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	PROTECT	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation After Detection	0: Non-maskable interrupt 1: Reset.	R/W
b1	PROTECT	Protection of Register	0: All bus slave MPU register writes are permitted 1: All bus slave MPU register writes are protected. Reads are permitted.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD and PROTECT bits	R/(W)*1

Note 1. Write data is not saved.

OAD bit (Operation After Detection)

The OAD bit generates either a reset or non-maskable interrupt when access to the protected region is detected by the bus slave MPU. When writing to the OAD bit, simultaneously write A5h to the KEY[7:0] bits using halfword access.

PROTECT bit (Protection of Register)

The PROTECT bit enables or disables writes to the associated registers to be protected. SMPUCTL.PROTECT controls the following registers:

- SMPUMBIU
- SMPUFBIU
- SMPUP0BIU
- SMPUP2BIU
- SMPUP6BIU.

When writing to the PROTECT bit, simultaneously write A5h to the KEY[7:0] bits using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the OAD and PROTECT bits. When writing to the OAD and PROTECT bits, simultaneously write A5h to the KEY[7:0] bits. When other values are written, the OAD and PROTECT bits are not updated. The KEY[7:0] bits are always read as 00h.

15.5.2 Operation

15.5.2.1 Memory protection

The bus slave MPU monitoring uses access control information that is set for the individual access control registers. If access to a protected region is detected, the bus slave MPU generates a memory protection error.

The bus slave MPU is enabled by writing 1 to the Write Protect (WPCPU or WPGRPA) bit or the Read Protect (RPCPU or RPGRPA) bit in the access control registers (SMPUMBIU, SMPUFBIU, SMPUP0BIU, SMPUP2BIU, and SMPUP6BIU).

15.5.2.2 Protecting the registers

Registers related to the bus slave MPU can be protected with the PROTECT bit in the SMPUCTL register.

15.5.2.3 Memory protection error

If access to a protected region is detected, the bus slave MPU generates a memory protection error. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or a reset.

The non-maskable interrupt status is indicated in ICU.NMISR.BUSSST. For details, see section 13, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSSRF. For details, see section 6, Resets.

15.6 Security MPU

The MCU incorporates a security MPU with four secure regions that include the code flash, SRAM, and two security functions. The secure regions can be protected from non-secure program accesses. A non-secure program cannot access a protected region.

Table 15.8 lists the specifications of the security MPU and Figure 15.10 shows a block diagram.

Table 15.8 Security MPU specifications

Specifications	Description
Secure regions	Code flash, SRAM, two security functions
Protected regions	0000 0000h to FFFF FFFFh
Number of regions	Program Counter: 2 regions Data access: 4 regions
Address specification for individual regions	Region start and end addresses configurable
Enable/disable setting for memory protection in individual regions	Settings enabled or disabled for the associated region

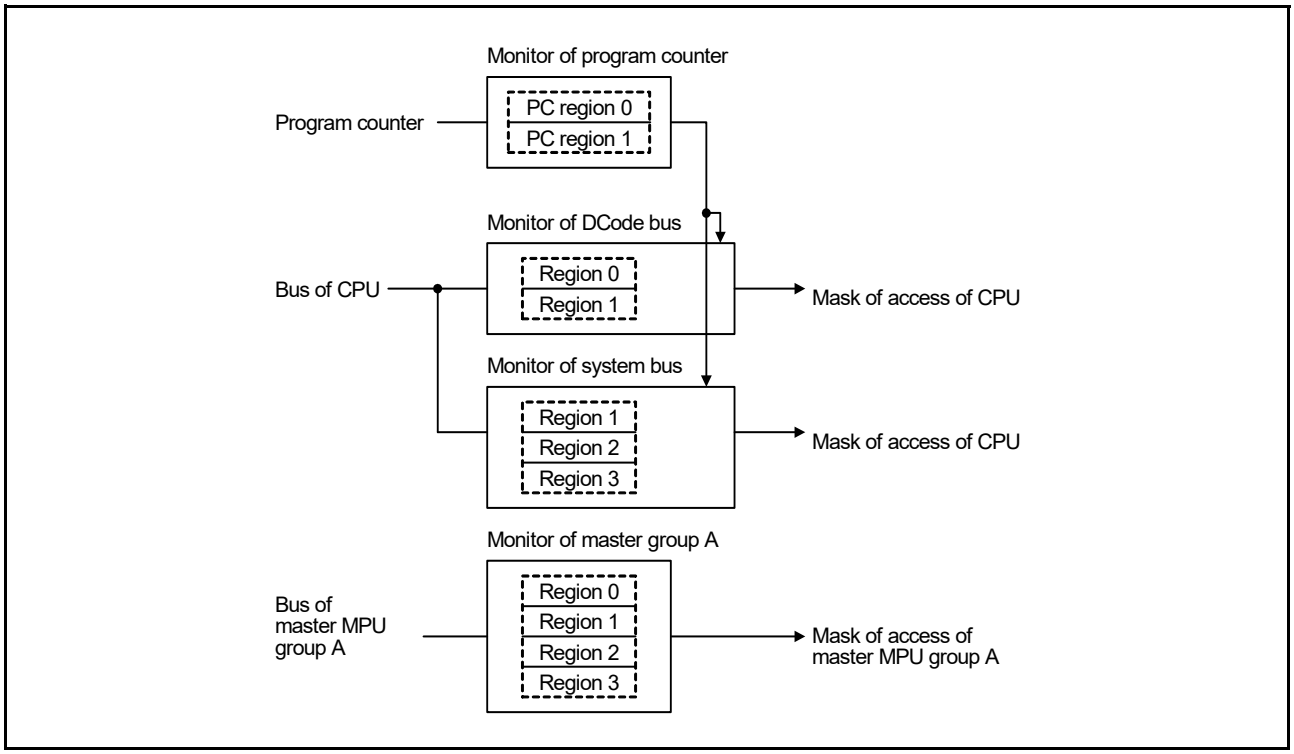


Figure 15.10 Security MPU block diagram

15.6.1 Register Descriptions (Option-Setting memory)

All security MPU registers are option-setting memory. Option-setting memory refers to a set of registers that are provided for selecting the state of the microcontroller after a reset. The option-setting memory is allocated in the code flash.

15.6.1.1 Security MPU Program Counter Start Address Register (SECMPUPCSn) (n = 0, 1)

Address(es): SECMPUPCS0 0000 0408h, SECMPUPCS1 0000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUPCS[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUPCS[15:2]														—	—
Value after reset:	The value set by user														0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should always be 0.	R
b31 to b2	SECMPUPCS[31:2]	Region Start Address	Address where the region starts, for use in region determination	R

The SECMPUPCSn and SECMPUPCEn registers specify the security fetch region for the code flash or SRAM (0000 0000h to FFFF FFFFh). The secure program is executed in the memory space defined by the SECMPUPCSn and SECMPUPCEn registers, and can access the secure data specified in the SECMPUSm and SECMPUEm registers (m = 0 to 3).

The SECMPUPCSn register specifies the address where the region starts. Setting of the memory mirror space (0200 0000h to 027F FFFFh) for MMF is prohibited.

An address space of greater than 12 bytes is required between the last instruction of the non-secure program and the first instruction of the secure program.

15.6.1.2 Security MPU Program Counter End Address Register (SECMPUPCEn) (n = 0, 1)

Address(es): SECMPUPCE0 0000 040Ch, SECMPUPCE1 0000 0414h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUPCE[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUPCE[15:2]														—	—
Value after reset:	The value set by user														1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	R
b31 to b2	SECMPUPCE[31:2]	Region End Address	Address where the region ends, for use in region determination.	R

The SECMPUPCSn and SECMPUPCEn registers specify the security fetch region of the code flash or SRAM (0000 0000h to FFFF FFFFh).

The SECMPUPCEn register specifies the address where the region ends.

15.6.1.3 Security MPU Region 0 Start Address Register (SECMPUS0)

Address(es): SECMPUS0 0000 0418h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	SECMPUS0[23:16]							
Value after reset:	0	0	0	0	0	0	0	0	The value set by user							

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS0[15:2]														—	—
Value after reset:	The value set by user														0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should always be 0.	R
b23 to b2	SECMPUS0[23:2]	Region Start Address	Address where the region starts, for use in region determination.	R
b31 to b24	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should always be 0.	R

The SECMPUS0 and SECMPUE0 registers specify the secure region of the code flash (0000 0000 to 00FF FFFFh). The memory space defined in the SECMPUS0 and SECMPUE0 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUS0 register specifies the address where the region starts. Setting of the vector table area is prohibited.

15.6.1.4 Security MPU Region 0 End Address Register (SECMPUE0)

Address(es): SECMPUE0 0000 041Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	SECMPUE0[23:16]							
Value after reset:	0	0	0	0	0	0	0	0	The value set by user							

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE0[15:2]														—	—
Value after reset:	The value set by user														1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. When programming to the code flash, the write value should always be 1.	R
b23 to b2	SECMPUE0[23:2]	Region End Address	Address where the region end, for use in region determination.	R
b31 to b24	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should always be 0.	R

The SECMPUS0 and SECMPUE0 registers specify the secure region of the flash (0000 0000 to 00FF FFFFh). The memory space defined in the SECMPUS0 and SECMPUE0 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUE0 register specifies the address where the region ends.

15.6.1.5 Security MPU Region 1 Start Address Register (SECMPUS1)

Address(es): SECMPUS1 0000 0420h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
SECMPUS1[31:16]															
Value after reset:	The value set by user														

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
SECMPUS1[15:2]														—	—
Value after reset:	The value set by user													0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R
b19 to b2	SECMPUS1[19:2]	Region Start Address	Address where the region starts, for use in region determination	R
b31 to b20	SECMPUS1[31:20]	Region Start Address	Address where the region starts, for use in region determination. The write value should always be 1FFh.	R

The SECMPUS1 and SECMPUE1 registers specify the secure region of the SRAM (1FF0 0000h to 1FFE FFFFh). The memory space defined in the SECMPUS1 and SECMPUE1 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUS1 register specifies the start address where the region starts. Setting of the stack area and the vector table are prohibited.

15.6.1.6 Security MPU Region 1 End Address Register (SECMPUE1)

Address(es): SECMPUE1 0000 0424h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
SECMPUE1[31:16]															
Value after reset:	The value set by user														

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
SECMPUE1[15:2]														—	—
Value after reset:	The value set by user													1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	R
b19 to b2	SECMPUE1[19:2]	Region End Address	Address where the region ends, for use in region determination	R
b31 to b20	SECMPUE1[31:20]	Region End Address	Address where the region ends, for use in region determination. The write value should always be 1FFh.	R

The SECMPUS1 and SECMPUE1 registers specify the secure region of the SRAM (1FF0 0000h to 1FFE FFFFh). The memory space defined in the SECMPUS1 and SECMPUE1 registers can only be accessed from the secure program set in up the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUE1 register specifies the address where the region ends.

15.6.1.7 Security MPU Region 2 Start Address Register (SECMPUS2)

Address(es): SECMPUS2 0000 0428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUS2[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS2[15:2]														—	—
Value after reset:	The value set by user														0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should always be 0.	R
b22 to b2	SECMPUS2[22:2]	Region Start Address	Address where the region starts, for use in region determination	R
b29 to b23	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should always be 0.	R
b30	—	Reserved	This bit is read as 1. When programming to the code flash, the write value should always be 1.	R
b31	—	Reserved	This bit is read as 0. When programming to the code flash, the write value should always be 0.	R

The SECMPUS2 and SECMPUE2 registers specify the secure region of security function 1 (400C 0000h to 400D FFFFh and 4010 0000h to 407F FFFFh). The memory space defined in the SECMPUS2 and SECMPUE2 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUS2 register specifies the address where the region starts.

15.6.1.8 Security MPU Region 2 End Address Register (SECMPUE2)

Address(es): SECMPUE2 0000 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUE2[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE2[15:2]														—	—
Value after reset:	The value set by user														1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. When programming to the code flash, the write value should always be 1.	R
b22 to b2	SECMPUE2[22:2]	Region End Address	Address where the region ends, for use in region determination	R
b29 to b23	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should always be 0.	R
b30	—	Reserved	This bit is read as 1. When programming to the code flash, the write value should always be 1.	R

Bit	Symbol	Bit name	Description	R/W
b31	—	Reserved	This bit is read as 0. When programming to the code flash, the write value should always be 0.	R

The SECMPUS2 and SECMPUE2 registers specify the secure region of security function 1 (400C 0000h to 400D FFFFh and 4010 0000h to 407F FFFFh). The memory space defined in the SECMPUS2 and SECMPUE2 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUE2 register specifies the address where the region ends.

15.6.1.9 Security MPU Region 3 Start Address Register (SECMPUS3)

Address(es): SECMPUS3 0000 0430h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUS3[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS3[15:2]														—	—
Value after reset:	The value set by user														0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should always be 0.	R
b22 to b2	SECMPUS3[22:2]	Region Start Address	Address where the region starts, for use in region determination.	R
b29 to b23	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should always be 0.	R
b30	—	Reserved	This bit is read as 1. When programming to the code flash, the write value should always be 1.	R
b31	—	Reserved	This bit is read as 0. When programming to the code flash, the write value should always be 0.	R

The SECMPUS3 and SECMPUE3 registers specify the secure region of security function 2 (400C 0000h to 400D FFFFh and 4010 0000h to 407F FFFFh). The memory space defined in the SECMPUS3 and SECMPUE3 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUS3 register specifies the address where the region starts.

15.6.1.10 Security MPU Region 3 End Address Register (SECMPUE3)

Address(es): SECMPUE3 0000 0434h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUE3[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE3[15:2]														—	—
Value after reset:	The value set by user														1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	R
b22 to b2	SECMPUE3[22:2]	Region End Address	Address where the region ends, for use in region determination.	R
b29 to b23	—	Reserved	These bits are read as 0. When programming to the code flash, the write value should always be 0.	R
b30	—	Reserved	This bit is read as 1. When programming to the code flash, the write value should always be 1.	R
b31	—	Reserved	This bit is read as 0. When programming to the code flash, the write value should always be 0.	R

The SECMPUS3 and SECMPUE3 registers specify the secure region of security function 2 (400C 0000h to 400D FFFFh and 4010 0000h to 407F FFFFh). The memory space defined in the SECMPUS3 and SECMPUE3 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUE3 register specifies the address where the region ends.

15.6.1.11 Security MPU Access Control Register (SECMPUAC)

Address(es): SECMPUAC 0000 0438h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DISPC1	DISPC0	—	—	—	—	DIS3	DIS2	DIS1	DIS0
Value after reset:	1	1	1	1	1	1	The value set by user		1	1	1	1	The value set by user			

Bit	Symbol	Bit name	Description	R/W
b0	DIS0	Region 0 Disable	0: Security MPU region 0 enabled 1: Security MPU region 0 disabled.	R
b1	DIS1	Region 1 Disable	0: Security MPU region 1 enabled 1: Security MPU region 1 disabled.	R
b2	DIS2	Region 2 Disable	0: Security MPU region 2 enabled 1: Security MPU region 2 disabled.	R
b3	DIS3	Region 3 Disable	0: Security MPU region 3 enabled 1: Security MPU region 3 disabled.	R
b7 to b4	—	Reserved	These bits are read as 1. When programming to the code flash, the write value should always be 1.	R
b8	DISPC0	PC Region 0 Disable	0: Security MPU PC region 0 enabled 1: Security MPU PC region 0 disabled.	R

Bit	Symbol	Bit name	Description	R/W
b9	DISPC1	PC Region 1 Disable	0: Security MPU PC region 1 enabled 1: Security MPU PC region 1 disabled.	R
b15 to b10	—	Reserved	These bits are read as 1. When programming to the code flash, the write value should always be 1.	R

Note: When flash memory is erased, the security MPU is disabled.
Note: To enable or disable the security MPU, see section 15.6.2, Memory Protection.

DIS0 bit (Region 0 Disable)

The DIS0 bit enables or disables the security MPU region 0. If security MPU region 0 is enabled, the code flash region within the limits set up by SECMPUS0 and SECMPUE0 is secure data.

DIS1 bit (Region 1 Disable)

The DIS1 bit enables or disables the security MPU region 1. If security MPU region 1 is enabled, the SRAM region within the limits set up by SECMPUS1 and SECMPUE1 is secure data.

DIS2 bit (Region 2 Disable)

The DIS2 bit enables or disables the security MPU region 2. If security MPU region 2 is enabled, the region within the limits set up by SECMPUS2 and SECMPUE2 is secure data.

DIS3 bit (Region 3 Disable)

The DIS3 bit enables or disables the security MPU region 3. If security MPU region 3 is enabled, the region within the limits set up by SECMPUS3 and SECMPUE3 is secure data.

DISPC0 bit (PC Region 0 Disable)

The DISPC0 bit enables or disables the security MPU PC region 0. If security MPU PC region 0 is enabled, the code flash or the SRAM region within the limits set up by SECMPUPCS0 and SECMPUPCE0 contains a secure program.

DISPC1 bit (PC Region 1 Disable)

The DISPC1 bit enables or disables the security MPU PC region 1. If security MPU PC region 1 is enabled, the code flash or the SRAM region within the limits set up by SECMPUPCS1 and SECMPUPCE1 contains a secure program.

15.6.2 Memory Protection

The security MPU protects the regions (the code flash, the SRAM, and two security function regions) from being accessed by non-secure programs. If access to a protected region is detected, the access becomes invalid.

When the security MPU is enabled, DISPC0 or DISPC1 in the Security MPU Access Control Register (SECMPUAC), and DIS0, DIS1, DIS2, or DIS3 in the Security MPU Access Control Register (SECMPUAC) must be set to 0.

When the security MPU is disabled, all bits in DISPC0, DISPC1, DIS0, DIS1, DIS2, and DIS3 in the Security MPU Access Control Register (SECMPUAC) must be set to 1. Other settings in the Security MPU Access Control Register (SECMPUAC) are prohibited.

The security MPU provides access protection in the following conditions:

- Secure data is accessed from a non-secure program
- Secure data is accessed from other than the CPU (DMAC, DTC)
- Secure data is accessed from the debugger.

Secure data is accessible only from a secure program.

Note: Secure program: Code flash or SRAM region within the limits set up by SECMPUPCS0 and SECMPUPCE0, code flash or SRAM region within the limits set up by SECMPUPCS1 and SECMPUPCE1.
Non-secure program: All regions outside the secure program.
Secure data: Code flash region within the limits set up by SECMPUS0 and SECMPUE0,
SRAM region within the limits set up by SECMPUS1 and SECMPUE1,
security function region within the limits set up by SECMPUS2 and SECMPUE2,
security Function region within the limits set up by SECMPUS3 and SECMPUE3.

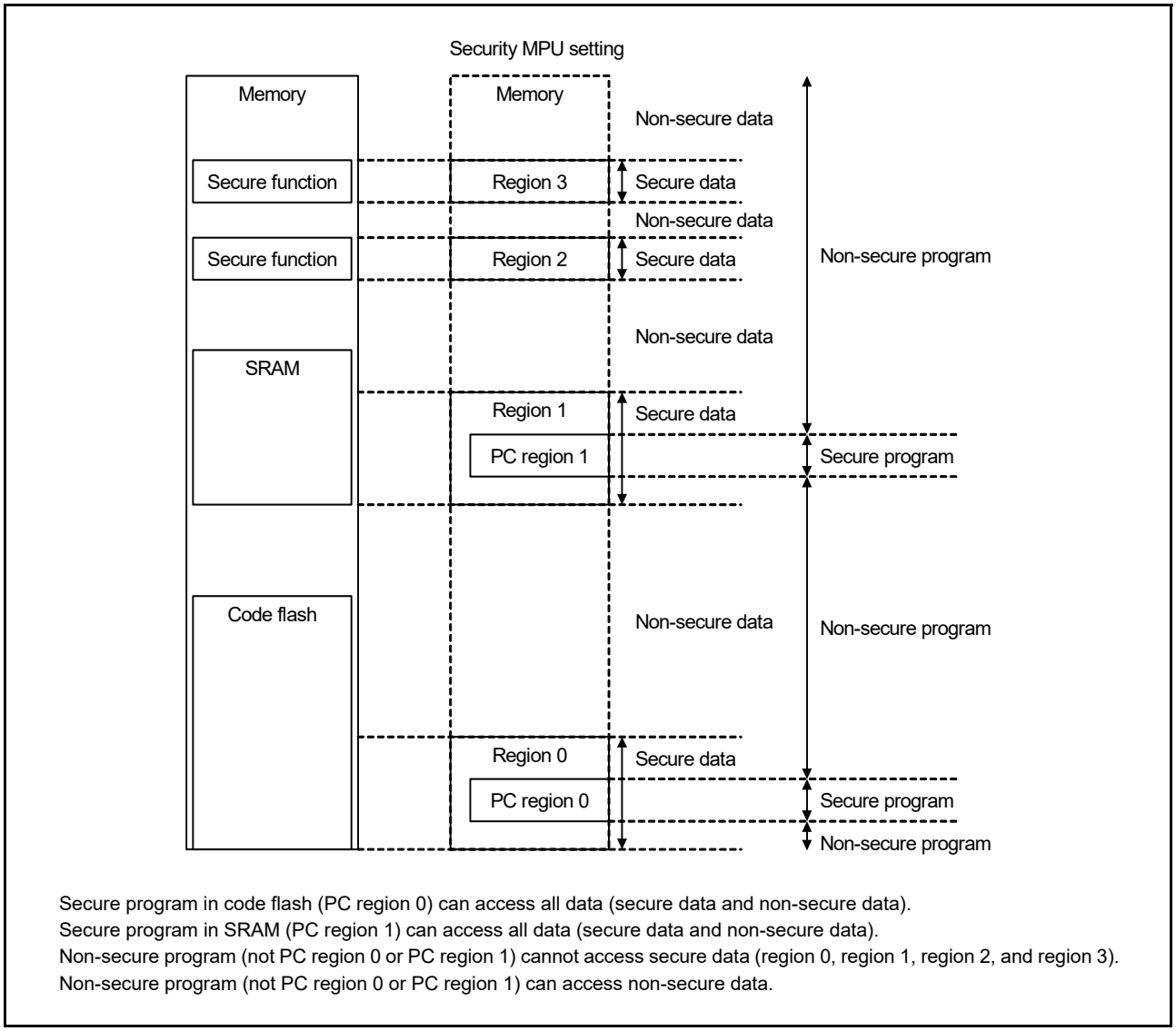


Figure 15.11 Use case of security MPU

15.6.3 Usage Notes

The protected memory cannot be debugged if the security MPU is enabled. Disable the security MPU when debugging a secure program.

15.7 References

1. *ARM®v7-M Architecture Reference Manual* (ARM DDI 0403D)
2. *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D)
3. *ARM® Cortex®-M4 Devices Generic User Guide* (ARM DUI 0553A).

16. DMA Controller (DMAC)

16.1 Overview

The MCU includes an 8-channel DMA Controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 16.1 lists the DMAC specifications and Figure 16.1 shows a block diagram.

Table 16.1 DMAC specifications

Parameter		Specifications
Number of channels		8 channels (DMACm, m = 0 to 7)
Transfer space		4 GB (0000 0000h to FFFF FFFFh, excluding reserved areas)
Maximum transfer volume		64M data units (maximum number of transfers in block transfer mode: 1,024 data units × 65,536 blocks)
DMA activation source		Selectable for each channel: • Software trigger • Interrupt requests from peripheral modules or trigger from external interrupt input pins.*1
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3... > Channel 7 (Channel 0: highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024
Transfer mode	Normal transfer mode	• One data transfer by one DMA transfer request • Selectable free running mode (total number of data transfers is not specified).
	Repeat transfer mode	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination • Maximum settable repeat size: 1,024.
	Block transfer mode	• One data block transfer by one DMA transfer request • Maximum settable block size: 1,024 data.
Selective functions	Extended repeat area function	• Allow data to be transferred by repeating the address values in the specified range, with the upper bit values in the transfer address register remaining fixed • Area of 2 bytes to 128 MB individually selectable as the extended repeat area for transfer source and destination.
Interrupt request (DMACm_INT)	Transfer end interrupt	Generated on completion of transferring data volume specified in the transfer counter
	Transfer escape end interrupt	Generated when: • The repeat size of data transfer is complete • The source address of the extended repeat area overflows • The destination address of the extended repeat area overflows.
Event link activation (DMACm_INT)		An event link request is generated after each data transfer (for block transfer, after each block is transferred)
Module-stop function		Module-stop state can be set to reduce power consumption

Note 1. For details on DMAC activation sources, see Table 13.3, Interrupt vector table in section 13, Interrupt Controller Unit (ICU).

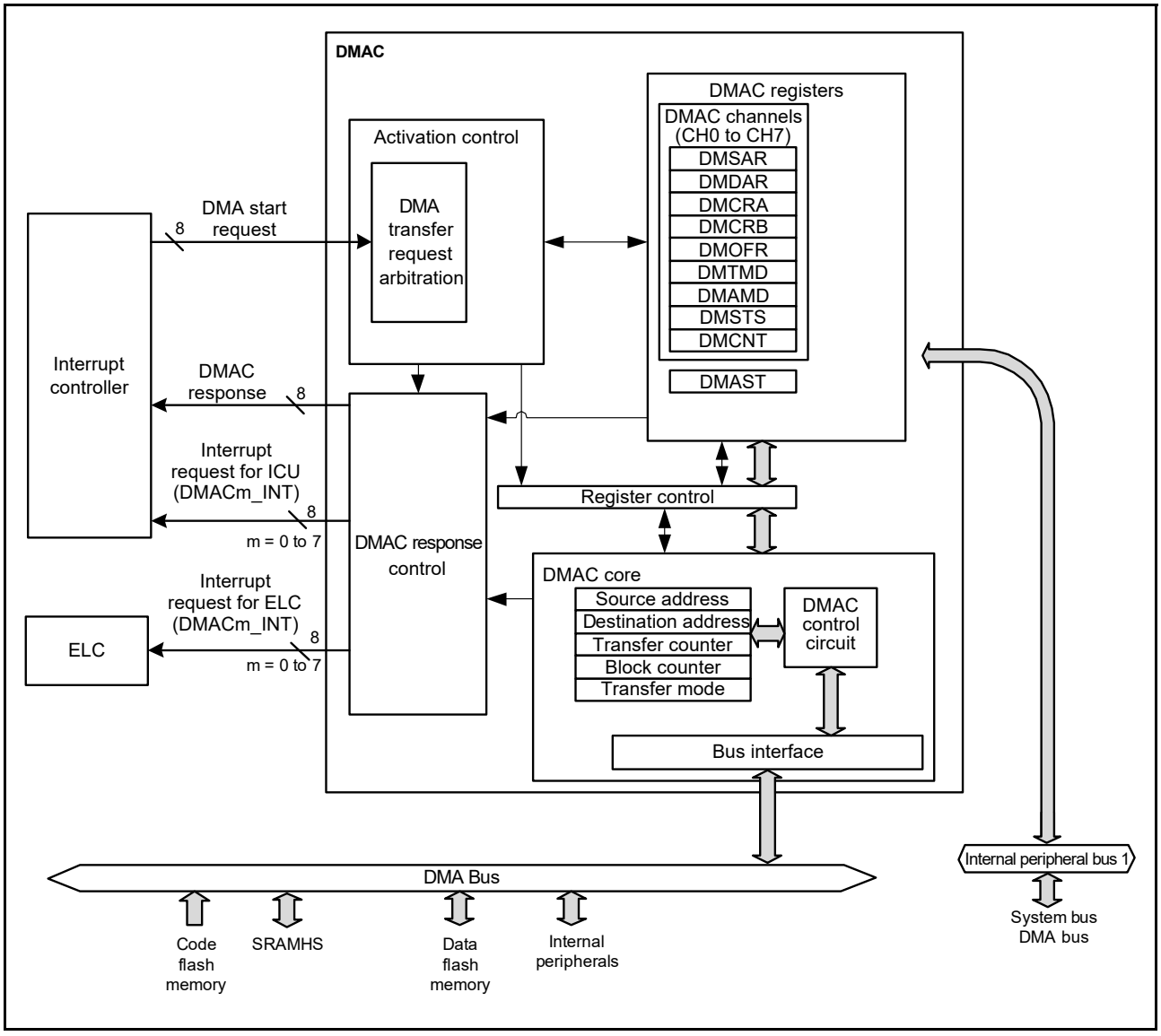


Figure 16.1 DMAC block diagram

16.2 Register Descriptions

16.2.1 DMA Source Address Register (DMSAR)

Address(es): DMAC0.DMSAR 4000 5000h, DMAC1.DMSAR 4000 5040h, DMAC2.DMSAR 4000 5080h, DMAC3.DMSAR 4000 50C0h, DMAC4.DMSAR 4000 5100h, DMAC5.DMSAR 4000 5140h, DMAC6.DMSAR 4000 5180h, DMAC7.DMSAR 4000 51C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b31 to b0	Specifies the transfer source start address	0000 0000h to FFFF FFFFh (4 GB)	R/W

Set DMSAR while DMAC activation is disabled (the DMST bit in DMAST = 0) or DMA transfer is disabled (the DTE bit in DMCNT = 0).

Note: Address alignment in this register must match the transfer data size value selected in the SZ bit in DMTMD.

16.2.2 DMA Destination Address Register (DMDAR)

Address(es): DMAC0.DMDAR 4000 5004h, DMAC1.DMDAR 4000 5044h, DMAC2.DMDAR 4000 5084h, DMAC3.DMDAR 4000 50C4h, DMAC4.DMDAR 4000 5104h, DMAC5.DMDAR 4000 5144h, DMAC6.DMDAR 4000 5184h, DMAC7.DMDAR 4000 51C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b31 to b0	Specifies the transfer destination start address	0000 0000h to FFFF FFFFh (4 GB)	R/W

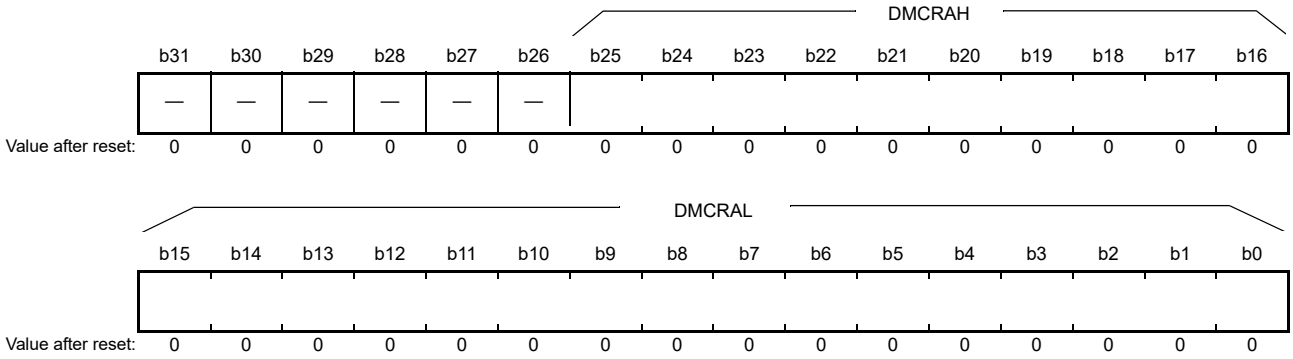
Set DMDAR while DMAC activation is disabled (the DMST bit in DMAST = 0) or DMA transfer is disabled (the DTE bit in DMCNT = 0).

Note: Address alignment in this register must match the transfer data size value selected in the SZ bit in DMTMD.

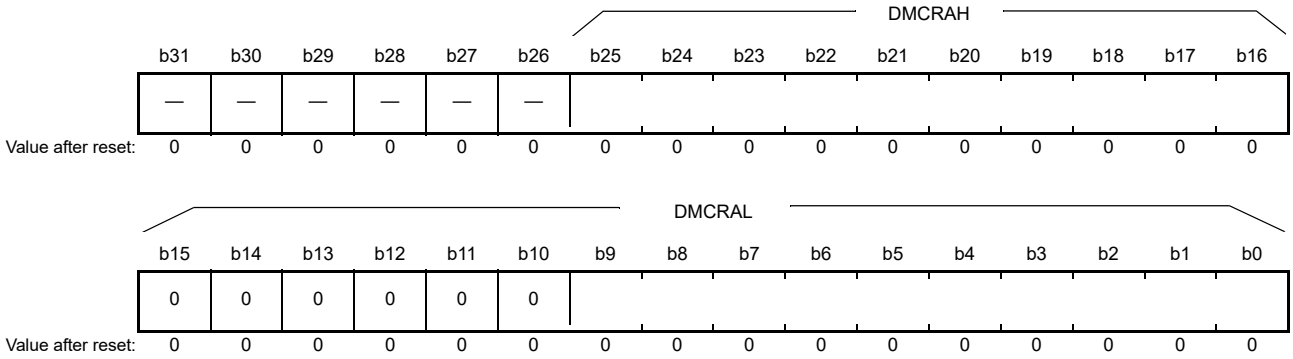
16.2.3 DMA Transfer Count Register (DMCRA)

Address(es): DMAC0.DMCRA 4000 5008h, DMAC1.DMCRA 4000 5048h, DMAC2.DMCRA 4000 5088h, DMAC3.DMCRA 4000 50C8h
DMAC4.DMCRA 4000 5108h, DMAC5.DMCRA 4000 5148h, DMAC6.DMCRA 4000 5188h, DMAC7.DMCRA 4000 51C8h

- Normal transfer mode



- Repeat transfer mode, block transfer mode



Symbol	Bit name	Description	R/W
DMCRAL	Lower bits of transfer count	Specifies the number of transfer operations	R/W
DMCRAH	Upper bits of transfer count		R/W

Note: In repeat and block transfer modes, set the same value for DMCRAH and DMCRAL.

(1) Normal transfer mode (MD[1:0] bits in DMACm.DMTMD = 00b)

In normal transfer mode, DMCRAL functions as a 16-bit transfer counter. The number of transfer operations is one when the setting is 0001h, and 65535 when it is FFFFh. The value is decremented by 1 each time data is transferred. A setting of 0000h indicates an unspecified number of transfer operations. Data transfer is performed with the transfer counter stopped, that is, in free running mode.

Do not use DMCRAH in normal transfer mode. Write 0000h to DMCRAH.

(2) Repeat transfer mode (MD[1:0] bits in DMACm.DMTMD = 01b)

In repeat transfer mode, DMCRAH specifies the repeat size and DMCRAL functions as a 10-bit transfer counter. The number of transfer operations is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In this mode, a value in the range of 000h to 3FFh (1 to 1024) can be set for DMCRAH and DMCRAL.

Setting bits [15:10] in DMCRAL is invalid. Write 0 to these bits. The value in DMCRAL is decremented by 1 each time data is transferred until it reaches 000h, at which time the value in DMCRAH is loaded into DMCRAL.

(3) Block transfer mode (MD[1:0] bits in DMACm.DMTMD = 10b)

In block transfer mode, DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter. The block size is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In this mode, a value in the

range of 000h to 3FFh can be set for DMCRAH and DMCRAL.

Setting bits [15:10] in DMCRAL is invalid. Write 0 to these bits. The value in DMCRAL is decremented by 1 each time data is transferred until it reaches 000h, at which time the value in DMCRAH is loaded into DMCRAL.

16.2.4 DMA Block Transfer Count Register (DMCRB)

Address(es): DMAC0.DMCRB 4000 500Ch, DMAC1.DMCRB 4000 504Ch, DMAC2.DMCRB 4000 508Ch, DMAC3.DMCRB 4000 50CCh, DMAC4.DMCRB 4000 510Ch, DMAC5.DMCRB 4000 514Ch, DMAC6.DMCRB 4000 518Ch, DMAC7.DMCRB 4000 51CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b15 to b0	Specifies the number of block or repeat transfer operations	0001h to FFFFh (1 to 65535) 0000h (65536).	R/W

DMCRB specifies the number of operations in block and repeat transfer modes. The number of transfer operations is one when the setting is 0001h, 65535 when it is FFFFh, and 65536 when it is 0000h.

In repeat transfer mode, the value is decremented by 1 when the final data of one repeat size is transferred. In block transfer mode, the value is decremented by 1 when the final data of one block size is transferred. Do not use DMCRB in normal transfer mode as the setting is invalid.

16.2.5 DMA Transfer Mode Register (DMTMD)

Address(es): DMAC0.DMTMD 4000 5010h, DMAC1.DMTMD 4000 5050h, DMAC2.DMTMD 4000 5090h, DMAC3.DMTMD 4000 50D0h, DMAC4.DMTMD 4000 5110h, DMAC5.DMTMD 4000 5150h, DMAC6.DMTMD 4000 5190h, DMAC7.DMTMD 4000 51D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		DTS[1:0]		—	—	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DCTG[1:0]	Transfer Request Source Select	b1 b0 0 0: Software 0 1: Interrupts*1 from peripheral modules or external interrupt input pins 1 0: Setting prohibited 1 1: Setting prohibited.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SZ[1:0]	Transfer Data Size Select	b9 b8 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: Setting prohibited.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	DTS[1:0]	Repeat Area Select	b13 b12 0 0: Specify destination as the repeat area or block area 0 1: Specify source as the repeat area or block area 1 0: Do not specify repeat area or block area 1 1: Setting prohibited.	R/W
b15, b14	MD[1:0]	Transfer Mode Select	b15 b14 0 0: Normal transfer 0 1: Repeat transfer 1 0: Block transfer 1 1: Setting prohibited.	R/W

Note 1. To select the DMAC activation source, use the DELSRn registers of the ICU. For details on DMAC activation sources, see Table 13.4, Event table in section 13, Interrupt Controller Unit (ICU).

DTS[1:0] bits (Repeat Area Select)

The DTS[1:0] bits select either the source or destination as the repeat area in repeat transfer mode and the block area in block transfer mode. In normal transfer mode, these bit settings are invalid.

16.2.6 DMA Interrupt Setting Register (DMINT)

Address(es): DMAC0.DMINT 4000 5013h, DMAC1.DMINT 4000 5053h, DMAC2.DMINT 4000 5093h, DMAC3.DMINT 4000 50D3h, DMAC4.DMINT 4000 5113h, DMAC5.DMINT 4000 5153h, DMAC6.DMINT 4000 5193h, DMAC7.DMINT 4000 51D3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DARIE	Destination Address Extended Repeat Area Overflow Interrupt Enable	0: Disabled 1: Enabled.	R/W
b1	SARIE	Source Address Extended Repeat Area Overflow Interrupt Enable	0: Disabled 1: Enabled.	R/W
b2	RPTIE	Repeat Size End Interrupt Enable	0: Disabled 1: Enabled.	R/W
b3	ESIE	Transfer Escape End Interrupt Enable	0: Disabled 1: Enabled.	R/W
b4	DTIE	Transfer End Interrupt Enable	0: Disabled 1: Enabled.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DARIE bit (Destination Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow occurs on the destination address when the DARIE bit is set to 1, the DTE bit in DMCNT is set to 0. At the same time, the ESIF flag in DMSTS is set to 1 to indicate an interrupt request triggered by an extended repeat area overflow on the destination address.

When block transfer mode is used with the extended repeat area function, an interrupt occurs after completion of a 1-block size transfer. When the DTE bit is set to 1 in DMACm.DMCNT of the channel associated with the stopped transfer, the transfer resumes from the state it was in when the transfer stopped. If the extended repeat area is not specified for the destination address, this bit is ignored.

SARIE bit (Source Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow occurs on the source address when the SARIE bit is set to 1, the DTE bit in DMCNT is set to 0. At the same time, the ESIF flag in DMSTS is set to 1 to indicate an interrupt request triggered by an extended repeat area overflow on the source address.

When block transfer mode is used with the extended repeat area function, an interrupt occurs after completion of a 1-block size transfer. When the DTE bit is set to 1 in DMACm.DMCNT of the channel associated with the stopped transfer, the transfer resumes from the state it was in when the transfer stopped. When the extended repeat area is not specified for the source address, this bit is ignored.

RPTIE bit (Repeat Size End Interrupt Enable)

When the RPTIE bit is set to 1 in repeat transfer mode, the DTE bit in DMCNT clears to 0 after completion of a 1-repeat size data transfer. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that the repeat size end interrupt request occurred. The repeat size end interrupt request can be generated even when the DTS[1:0] bits in DMTMD are 10b (repeat area or block area is not specified).

When the RPTIE bit is set to 1 in block transfer mode, the DTE bit in DMCNT sets to 0 after completion of a 1-block

data transfer in the same way as repeat transfer mode. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that the repeat size end interrupt request occurred. The repeat size end interrupt request can be generated even when the DTS[1:0] bits in DMTMD are 10b (repeat area or block area is not specified).

ESIE bit (Transfer Escape End Interrupt Enable)

The ESIE bit enables the transfer escape end interrupt requests (repeat size end interrupt request and extended repeat area overflow interrupt request) that occur during DMA transfer. The interrupt occurs when this bit is 1 and the ESIF flag in DMSTS is set to 1. To clear the transfer escape end interrupt, clear this bit or the ESIF flag in DMSTS to 0.

DTIE bit (Transfer End Interrupt Enable)

The DTIE bit enables the transfer end interrupt request that occurs on completion of a specified number of data transfers. The interrupt occurs when this bit is 1 and the DTIF flag in DMSTS is set to 1. To clear the transfer end interrupt, clear this bit or the DTIF flag in DMSTS to 0.

16.2.7 DMA Address Mode Register (DMAMD)

Address(es): DMAC0.DMAMD 4000 5014h, DMAC1.DMAMD 4000 5054h, DMAC2.DMAMD 4000 5094h, DMAC3.DMAMD 4000 50D4h, DMAC4.DMAMD 4000 5114h, DMAC5.DMAMD 4000 5154h, DMAC6.DMAMD 4000 5194h, DMAC7.DMAMD 4000 51D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SM[1:0]		—	SARA[4:0]					DM[1:0]		—	DARA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DARA[4:0]	Destination Address Extended Repeat Area	Specifies the extended repeat area on the destination address. For details on the settings, see Table 16.2.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	DM[1:0]	Destination Address Update Mode	b7 b6 0 0: Fixed address 0 1: Offset addition 1 0: Incremented address 1 1: Decremented address.	R/W
b12 to b8	SARA[4:0]	Source Address Extended Repeat Area	Specifies the extended repeat area on the source address. For details on the settings, see Table 16.2.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15, b14	SM[1:0]	Source Address Update Mode	b15 b14 0 0: Fixed address 0 1: Offset addition 1 0: Incremented address 1 1: Decremented address.	R/W

DARA[4:0] bits (Destination Address Extended Repeat Area)

The DARA[4:0] bits specify the extended repeat area on the destination address. The extended repeat area function is realized through an update of the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of 2 between 2 bytes and 128 MB. The start address of the extended repeat area is set when the lower address overflows the extended repeat area on an address increment. Similarly, the end address of the extended repeat area is set when the lower address underflows the extended repeat area on an address decrement.

Do not specify the extended repeat area on the destination address when a repeat or block area is specified as the transfer destination. When repeat or block transfer is selected, and when DMACm.DMTMD.DTS[1:0] = 00b (the transfer destination is specified as the repeat or block area), write 00000b in the DARA[4:0] bits.

To request an interrupt when an overflow or underflow occurs in the extended repeat area, set the DARIE bit in DMINT to 1. Table 16.2 lists the extended repeat areas associated with each setting.

DM[1:0] bits (Destination Address Update Mode)

The DM[1:0] bits select the update mode for the destination address.

- When increment is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the destination address is incremented by 1, 2, and 4, respectively
- When decrement is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the destination address is decremented by 1, 2, and 4, respectively
- When offset addition is selected, the offset specified in the DMACm.DMOFR register is added to the address.

SARA[4:0] bits (Source Address Extended Repeat Area)

The SARA[4:0] bits specify the extended repeat area on the source address. The extended repeat area function is realized through an update of the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of 2 between 2 bytes and 128 MB. The start address of the extended repeat area is set when the lower address overflows the extended repeat area on an address increment. Similarly, the end address of the extended repeat area is set when the lower address underflows the extended repeat area on an address decrement.

Do not specify the extended repeat area on the source address when a repeat or block area is specified as the transfer source. When repeat or block transfer is selected, and when DMACm.DMTMD.DTS[1:0] = 01b (the transfer source is specified as the repeat or block area), write 00000b in the SARA[4:0] bits.

To request an interrupt when an overflow or underflow occurs in the extended repeat area, set the SARIE bit in DMINT to 1. Table 16.2 lists the extended repeat areas associated with each setting.

SM[1:0] bits (Source Address Update Mode)

The SM[1:0] bits select the update mode for the source address:

- When increment is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the source address is incremented by 1, 2, and 4, respectively
- When decrement is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the source address is decremented by 1, 2, and 4, respectively
- When offset addition is selected, the offset specified in the DMACm.DMOFR register is added to the address.

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Table 16.2 SARA[4:0] or DARA[4:0] settings and corresponding repeat areas (1 of 2)

SARA[4:0] or DARA[4:0]	Extended repeat area
00000b	Not specified
00001b	2 bytes specified as extended repeat area by the lower 1 bit of the address
00010b	4 bytes specified as extended repeat area by the lower 2 bits of the address
00011b	8 bytes specified as extended repeat area by the lower 3 bits of the address
00100b	16 bytes specified as extended repeat area by the lower 4 bits of the address
00101b	32 bytes specified as extended repeat area by the lower 5 bits of the address
00110b	64 bytes specified as extended repeat area by the lower 6 bits of the address
00111b	128 bytes specified as extended repeat area by the lower 7 bits of the address
01000b	256 bytes specified as extended repeat area by the lower 8 bits of the address
01001b	512 bytes specified as extended repeat area by the lower 9 bits of the address
01010b	1 KB specified as extended repeat area by the lower 10 bits of the address
01011b	2 KB specified as extended repeat area by the lower 11 bits of the address
01100b	4 KB specified as extended repeat area by the lower 12 bits of the address
01101b	8 KB specified as extended repeat area by the lower 13 bits of the address
01110b	16 KB specified as extended repeat area by the lower 14 bits of the address
01111b	32 KB specified as extended repeat area by the lower 15 bits of the address
10000b	64 KB specified as extended repeat area by the lower 16 bits of the address
10001b	128 KB specified as extended repeat area by the lower 17 bits of the address
10010b	256 KB specified as extended repeat area by the lower 18 bits of the address
10011b	512 KB specified as extended repeat area by the lower 19 bits of the address

Table 16.2 SARA[4:0] or DARA[4:0] settings and corresponding repeat areas (2 of 2)

SARA[4:0] or DARA[4:0]	Extended repeat area
10100b	1 MB specified as extended repeat area by the lower 20 bits of the address
10101b	2 MB specified as extended repeat area by the lower 21 bits of the address
10110b	4 MB specified as extended repeat area by the lower 22 bits of the address
10111b	8 MB specified as extended repeat area by the lower 23 bits of the address
11000b	16 MB specified as extended repeat area by the lower 24 bits of the address
11001b	32 MB specified as extended repeat area by the lower 25 bits of the address
11010b	64 MB specified as extended repeat area by the lower 26 bits of the address
11011b	128 MB specified as extended repeat area by the lower 27 bits of the address
11100b to 11111b	Setting prohibited

16.2.8 DMA Offset Register (DMOFR)

Address(es): DMAC0.DMOFR 4000 5018h, DMAC1.DMOFR 4000 5058h, DMAC2.DMOFR 4000 5098h, DMAC3.DMOFR 4000 50D8h, DMAC4.DMOFR 4000 5118h, DMAC5.DMOFR 4000 5158h, DMAC6.DMOFR 4000 5198h, DMAC7.DMOFR 4000 51D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b31 to b0	Specifies the offset when offset addition is selected as the address update mode for transfer source or destination	0000 0000h to 00FF FFFFh (0 byte to (16 MB - 1 byte)) FF00 0000h to FFFF FFFFh (-16 MB to -1 byte)	R/W

Only write to this register while DMAC operation is stopped or DMA transfer is disabled, not during data transfer. Setting bits [31:25] is invalid. The value in bit [24] is extended to bits [31:25]. Reading DMOFR returns the extended value.

16.2.9 DMA Transfer Enable Register (DMCNT)

Address(es): DMAC0.DMCNT 4000 501Ch, DMAC1.DMCNT 4000 505Ch, DMAC2.DMCNT 4000 509Ch, DMAC3.DMCNT 4000 50DCh, DMAC4.DMCNT 4000 511Ch, DMAC5.DMCNT 4000 515Ch, DMAC6.DMCNT 4000 519Ch, DMAC7.DMCNT 4000 51DCh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DTE	DMA Transfer Enable	0: Disabled 1: Enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTE bit (DMA Transfer Enable)

The DTE bit enables DMA transfer. To enable DMA transfer, set the DMST bit in DMAST to 1 to enable DMAC activation, then set the DTE bit to 1 to enable DMA transfer for the associated channel.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When 0 is written to this bit
- When the specified volume of data transfer is complete
- When DMA transfer is stopped by a repeat size end interrupt
- When DMA transfer is stopped by an extended repeat area overflow interrupt.

16.2.10 DMA Software Start Register (DMREQ)

Address(es): DMAC0.DMREQ 4000 501Dh, DMAC1.DMREQ 4000 505Dh, DMAC2.DMREQ 4000 509Dh, DMAC3.DMREQ 4000 50DDh, DMAC4.DMREQ 4000 511Dh, DMAC5.DMREQ 4000 515Dh, DMAC6.DMREQ 4000 519Dh, DMAC7.DMREQ 4000 51DDh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CLRS	—	—	—	SWREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SWREQ	DMA Software Start	0: DMA transfer is not requested 1: DMA transfer is requested.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	CLRS	DMA Software Start Bit Auto Clear Select	0: SWREQ bit is cleared after DMA transfer is started by software 1: SWREQ bit is not cleared after DMA transfer is started by software.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SWREQ bit (DMA Software Start)

Writing 1 to the SWREQ bit generates a DMA transfer request. After DMA transfer starts, SWREQ sets to 0 if the CLRS bit is 0. SWREQ does not clear if CLRS bit is 1. The DMA transfer request can be issued again after the transfer is complete.

Note: Setting this bit is valid and DMA transfer by software is enabled only when the DCTG[1:0] bits in DMTMD are set to 00b, specifying software as the DMA activation source. Setting this bit is invalid when the DCTG[1:0] bits in DMTMD are set to any value other than 00b.

To start DMA transfer by software with the CLRS bit set to 0, ensure that the SWREQ bit is 0, then write 1 to the SWREQ bit.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When a DMA transfer request by software is accepted and DMA transfer is started with the CLRS bit set to 0 (the SWREQ bit is cleared after DMA transfer is started by software)
- When 0 is written to this bit.

CLRS bit (DMA Software Start Bit Auto Clear Select)

When an SWREQ setting of 1 triggers a transfer request, the CLRS bit specifies whether to clear the SWREQ bit to 0 after DMA transfer starts. When the CLRS bit is set to 0, SWREQ sets to 0 after DMA transfer starts. When the CLRS bit is set to 1, SWREQ is not set to 0. A DMA transfer request can be issued again after the transfer is complete.

16.2.11 DMA Status Register (DMSTS)

Address(es): DMAC0.DMSTS 4000 501Eh, DMAC1.DMSTS 4000 505Eh, DMAC2.DMSTS 4000 509Eh, DMAC3.DMSTS 4000 50DEh, DMAC4.DMSTS 4000 511Eh, DMAC5.DMSTS 4000 515Eh, DMAC6.DMSTS 4000 519Eh, DMAC7.DMSTS 4000 51DEh

	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	DTIF	—	—	—	ESIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ESIF	Transfer Escape End Interrupt Flag	0: No interrupt occurred 1: Interrupt occurred.	R/W*1
b3 to b1	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b4	DTIF	Transfer End Interrupt Flag	0: No interrupt occurred 1: Interrupt occurred.	R/W*1
b6, b5	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7	ACT	DMA Active Flag	0: DMAC operation suspended 1: DMAC operating.	R

Note 1. Only 0 can be written to clear the flag.

ESIF flag (Transfer Escape End Interrupt Flag)

The ESIF flag indicates that a transfer escape end interrupt occurred.

[Setting conditions]

- In repeat transfer mode, when one repeat size data transfer completes with the RPTIE bit in DMINT set to 1
- In block transfer mode, when one block data transfer completes with the RPTIE bit in DMINT set to 1
- When an extended repeat area overflow on the source address occurs with the SARIE bit in DMINT set to 1, and the SARA[4:0] bits in DMAMD set to any value other than 00000b (extended repeat area is specified on the transfer source address)
- When an extended repeat area overflow on the destination address occurs with the DARIE bit in DMINT set to 1, and the DARA[4:0] bits in DMAMD set to any value other than 00000b (extended repeat area is specified on the transfer destination address).

[Clearing conditions]

- When 0 is written to this flag
- When 1 is written to the DTE bit in DMCNT.

DTIF flag (Transfer End Interrupt Flag)

The DTIF flag indicates that a transfer end interrupt occurred.

[Setting conditions]

- In normal transfer mode, when the specified number of unit transfers completes (the value of DMCRAL becomes 0 on completion of transfer)
- In repeat transfer mode, when the specified number of repeat transfer operations completes (the value of DMCRB becomes 0 on completion of transfer)
- In block transfer mode, when the specified number of blocks is transferred (the value of DMCRB becomes 0 on completion of transfer).

[Clearing conditions]

- When 0 is written to this flag
- When 1 is written to the DTE bit in DMCNT.

ACT flag (DMA Active Flag)

The ACT flag indicates whether the DMAC is in the idle or active state.

[Setting condition]

- When the DMAC starts a data transfer.

[Clearing condition]

- When the data transfer in response to one transfer request completes.

16.2.12 DMAC Module Activation Register (DMAST)

Address(es): DMA.DMAST 4000 5200h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DMST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DMST	DMAC Operation Enable	0: Disabled 1: Enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DMST bit (DMAC Operation Enable)

Setting the DMST bit to 1 enables DMAC activation for all channels. When the DMST bit is set to 1 (DMAC activation is enabled), and 1 is written to the DMACm.DMCNT.DTE bit (DMA transfer is enabled) for multiple channels, all of the associated channels can be placed in the transfer request ready state at the same time.

When the DMST bit sets to 0 during DMA transfer, DMA transfer is suspended after the current data transfer associated with a single transfer request completes. To resume DMA transfer, set the DMST bit to 1 again.

[Setting condition]

- When 1 is written to this bit.

[Clearing condition]

- When 0 is written to this bit.

16.3 Operation

16.3.1 Transfer Mode

(1) Normal transfer mode

In normal transfer mode, one data unit is transferred for one transfer request. You can specify the number of transfer operations, up to a maximum of 65535, in DMACm.DMCRAL. When these bits are set to 0000h, no number of operations is specified and data transfer is performed with the transfer counter stopped (free running mode). A transfer end interrupt request can be generated after completion of the specified number of transfer operations, except when in free running mode. Setting DMACm.DMCRB is invalid in normal transfer mode.

Table 16.3 summarizes the register update operation in normal transfer mode.

Table 16.3 Register update operation in normal transfer mode (1 of 2)

Register	Function	Update operation after completion of a transfer for one transfer request
DMACm.DMSAR	Transfer source address	Increment, decrement, fixed, or offset addition
DMACm.DMDAR	Transfer destination address	Increment, decrement, fixed, or offset addition

Table 16.3 Register update operation in normal transfer mode (2 of 2)

Register	Function	Update operation after completion of a transfer for one transfer request
DMACm.DMCRAL	Transfer count	Decremented by 1 or not updated (in free running mode)
DMACm.DMCRAH	-	Not updated (not used in normal transfer mode)
DMACm.DMCRB	-	Not updated (not used in normal transfer mode)

Figure 16.2 shows the operation in normal transfer mode.

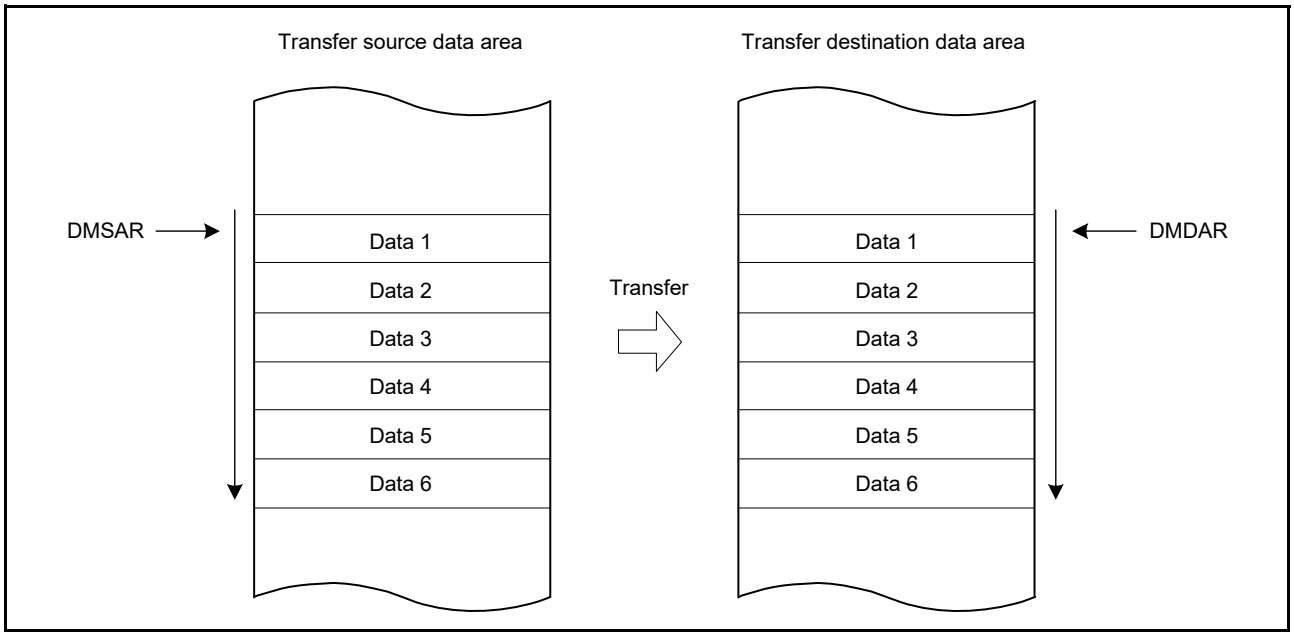


Figure 16.2 Operation in normal transfer mode

(2) Repeat transfer mode

In repeat transfer mode, one data unit is transferred for one transfer request. The repeat transfer size, up to a maximum of 1K data units, is set in DMACm.DMCRA. The number of repeat transfers, up to a maximum of 64K, is set in DMACm.DMCRB. The total data transfer size can be set to a maximum of 64M data units (1K data units × 64K repeat transfer operations).

You can specify either the transfer source or destination as a repeat area. When transfer of the repeat size data is complete, the address of the specified repeat area (DMSAR or DMDAR in DMACm) returns to the transfer start address. In this mode, when all data of the specified repeat size is transferred, DMA transfer can be stopped and a repeat size end interrupt can be requested. To resume DMA transfer, write 1 to the DTE bit in DMACm.DMCNT during repeat size end interrupt handling.

A transfer end interrupt request can be generated after completion of the specified number of repeat transfers.

Table 16.4 summarizes the register update operation in repeat transfer mode, and Figure 16.3 shows the operation in repeat transfer mode.

Table 16.4 Register update operation in repeat transfer mode (1 of 2)

		Update operation after completion of a transfer for one transfer request	
Register	Function	When DMACm.DMCRAL is not 1	When DMACm.DMCRAL is 1 (transfer of the last repeat size data unit)
DMACm.DMSAR	Transfer source address	Increment, decrement, fixed, or offset addition	• DMACm.DMTMD.DTS[1:0] = 00b Increment, decrement, fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 01b Initial value of DMACm.DMSAR • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition.

Table 16.4 Register update operation in repeat transfer mode (2 of 2)

Register	Function	Update operation after completion of a transfer for one transfer request	
		When DMACm.DMCRAL is not 1	When DMACm.DMCRAL is 1 (transfer of the last repeat size data unit)
DMACm.DMDAR	Transfer destination address	Increment, decrement, fixed, or offset addition	• DMACm.DMTMD.DTS[1:0] = 00b Initial value of DMACm.DMDAR • DMACm.DMTMD.DTS[1:0] = 01b Increment, decrement, fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition.
DMACm.DMCRAH	Repeat size	Not updated	Not updated
DMACm.DMCRAL	Transfer count	Decremented by 1	DMACm.DMCRAH
DMACm.DMCRB	Count of repeat transfer operations	Not updated	Decremented by 1

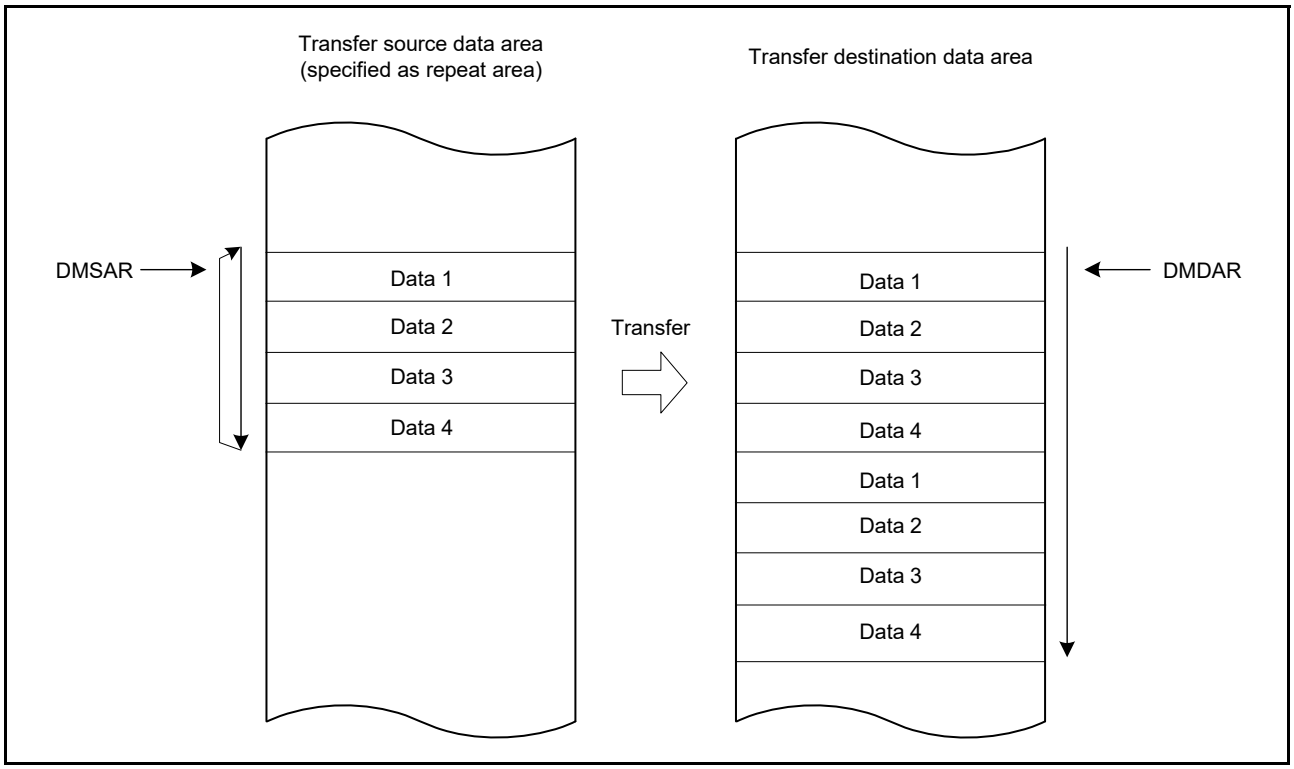


Figure 16.3 Operation in repeat transfer mode

(3) Block transfer mode

In block transfer mode, a single data block is transferred for one transfer request. The block size, up to a maximum of 1K data units, is set in DMACm.DMCRA. The number of block transfers, up to a maximum of 64K, is set in DMACm.DMCRB. A total data transfer size up to a maximum of 64M data units (1K data units × 64K block transfer operations) can be set.

You can specify either the transfer source or destination as a block area. When transfer of a single data block is complete, the address of the specified block area (DMSAR or DMDAR in DMACm) returns to the transfer start address. In this mode, when all data in a single block is transferred, DMA transfer can be stopped and a repeat size end interrupt can be requested. To resume DMA transfer, write 1 to the DTE bit in DMACm.DMCNT during repeat size end interrupt handling.

A transfer end interrupt request can be generated after completion of the specified number of block transfers.

Table 16.5 summarizes the register update operation in block transfer mode, and Figure 16.4 shows the operation in block transfer mode.

Table 16.5 Register update operation in block transfer mode

Register	Function	Update operation after completion of single-block transfer for one transfer request
DMACm.DMSAR	Transfer source address	• DMACm.DMTMD.DTS[1:0] = 00b Increment, decrement, fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 01b Initial value of DMACm.DMSAR • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition.
DMACm.DMDAR	Transfer destination address	• DMACm.DMTMD.DTS[1:0] = 00b Initial value of DMACm.DMDAR • DMACm.DMTMD.DTS[1:0] = 01b Increment, decrement, fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition.
DMACm.DMCRAH	Block size	Not updated
DMACm.DMCRAL	Transfer count	DMACm.DMCRAH
DMACm.DMCRB	Count of block transfer operations	Decremented by 1

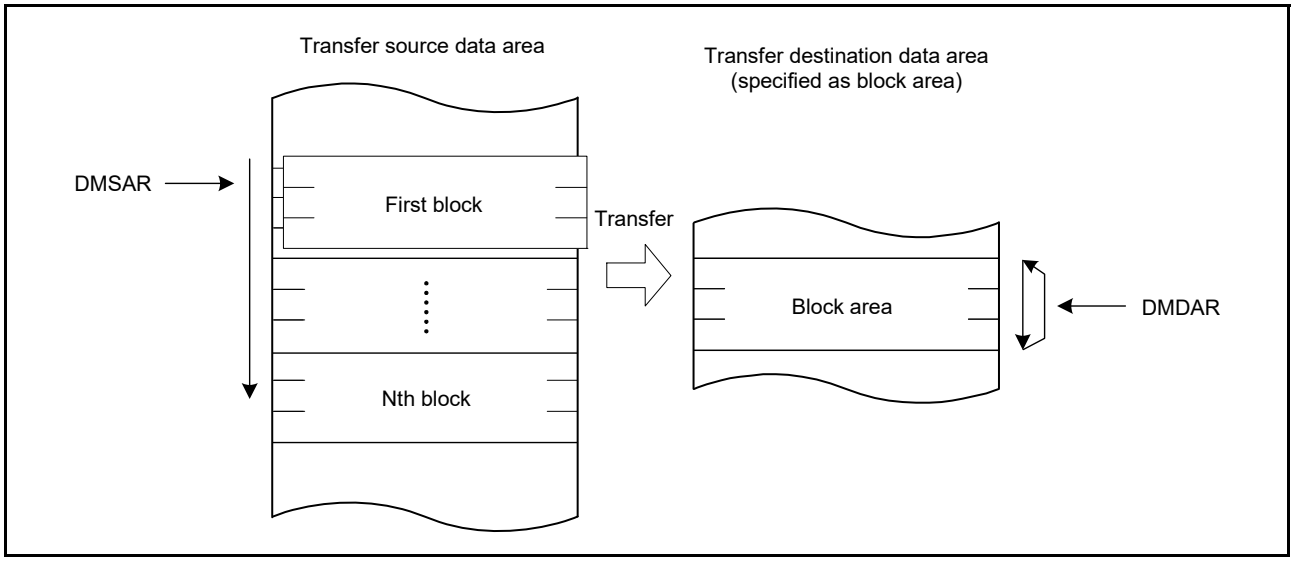


Figure 16.4 Operation in block transfer mode

16.3.2 Extended Repeat Area Function

The DMAC supports extended repeat areas on the transfer source and destination addresses, specified separately in the transfer source address register (DMSAR) and transfer destination address register (DMDAR) of DMACm. When this function is set, the address registers repeatedly indicate the addresses of the specified extended repeat areas.

The extended repeat area on the source address is specified in the SARA[4:0] bits in DMACm.DMAMD. The extended repeat area on the destination address is specified in the DARA[4:0] bits in DMACm.DMAMD. You can specify different sizes for the source and destination. However, you must not specify a transfer source or destination that is set as the repeat or block area as the extended repeat area.

When the address register value reaches the end address of the extended repeat area and the extended repeat area overflows, DMA transfer is stopped and an extended repeat area overflow interrupt can be requested. When an overflow occurs in the extended repeat area on the transfer source while the SARIE bit in DMACm.DMINT is set to 1, the ESIF flag in DMACm.DMSTS is set to 1 and the DTE bit in DMACm.DMCNT sets to 0 to stop DMA transfer. At this point, if the ESIE bit in DMACm.DMINT is set to 1, an extended repeat area overflow interrupt is requested. When the DARIE bit in DMACm.DMINT is set to 1, the destination address register becomes a target for the function. To resume DMA transfer, write 1 to the DTE bit in DMACm.DMCNT during interrupt handling.

Figure 16.5 shows an example of the extended repeat area operation.

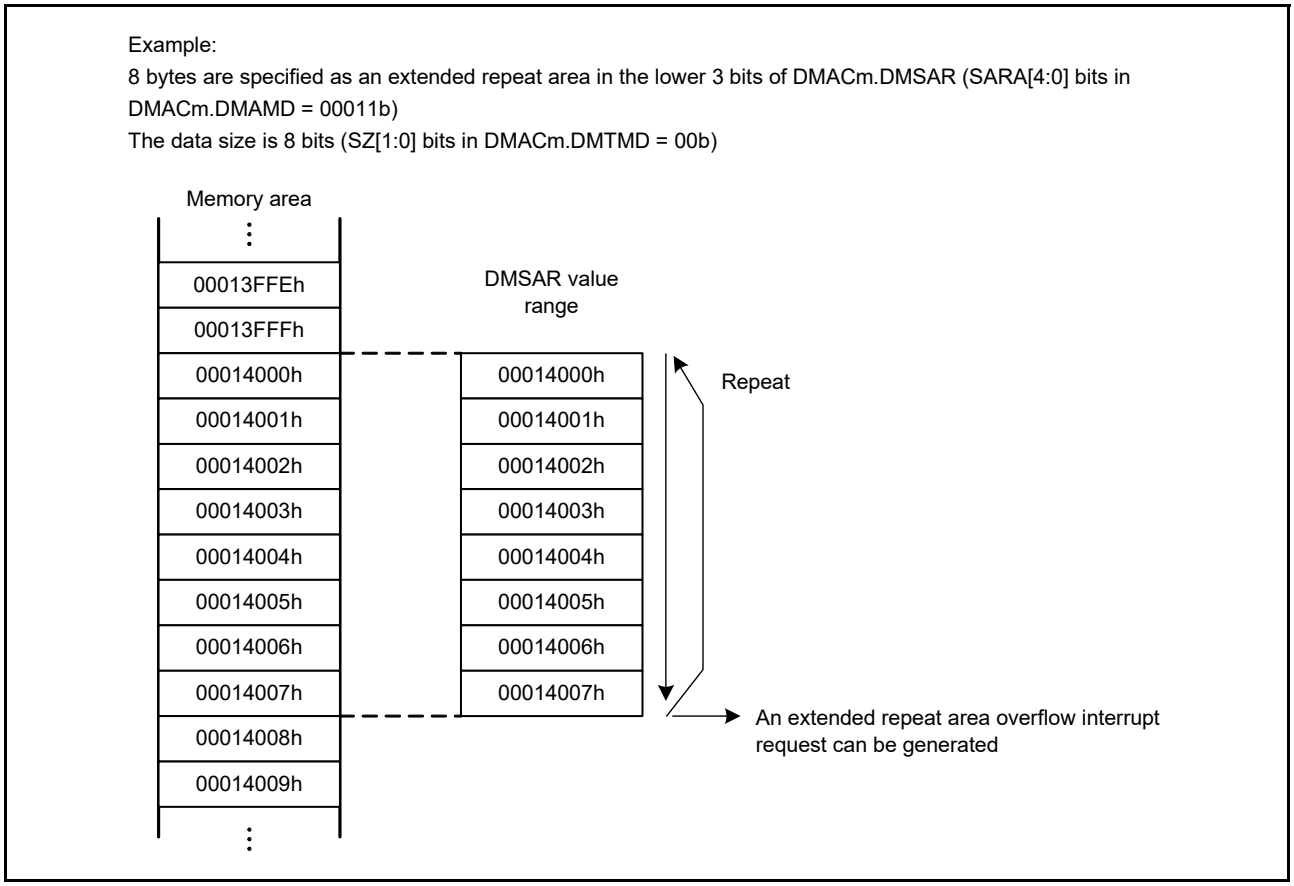


Figure 16.5 Example of extended repeat area operation

When using extended repeat area overflow interrupts in block transfer mode, consider the following points:

- When a transfer is stopped by an extended repeat area overflow interrupt, the address register must be set so that the block size is a power of 2 or the block size boundary is aligned with the extended repeat area boundary. When an overflow on the extended repeat area occurs during a transfer of one block, the overflow interrupt is suspended until transfer of the block is complete, and the transfer overruns.

Figure 16.6 shows an example of using the extended repeat area function in block transfer mode.

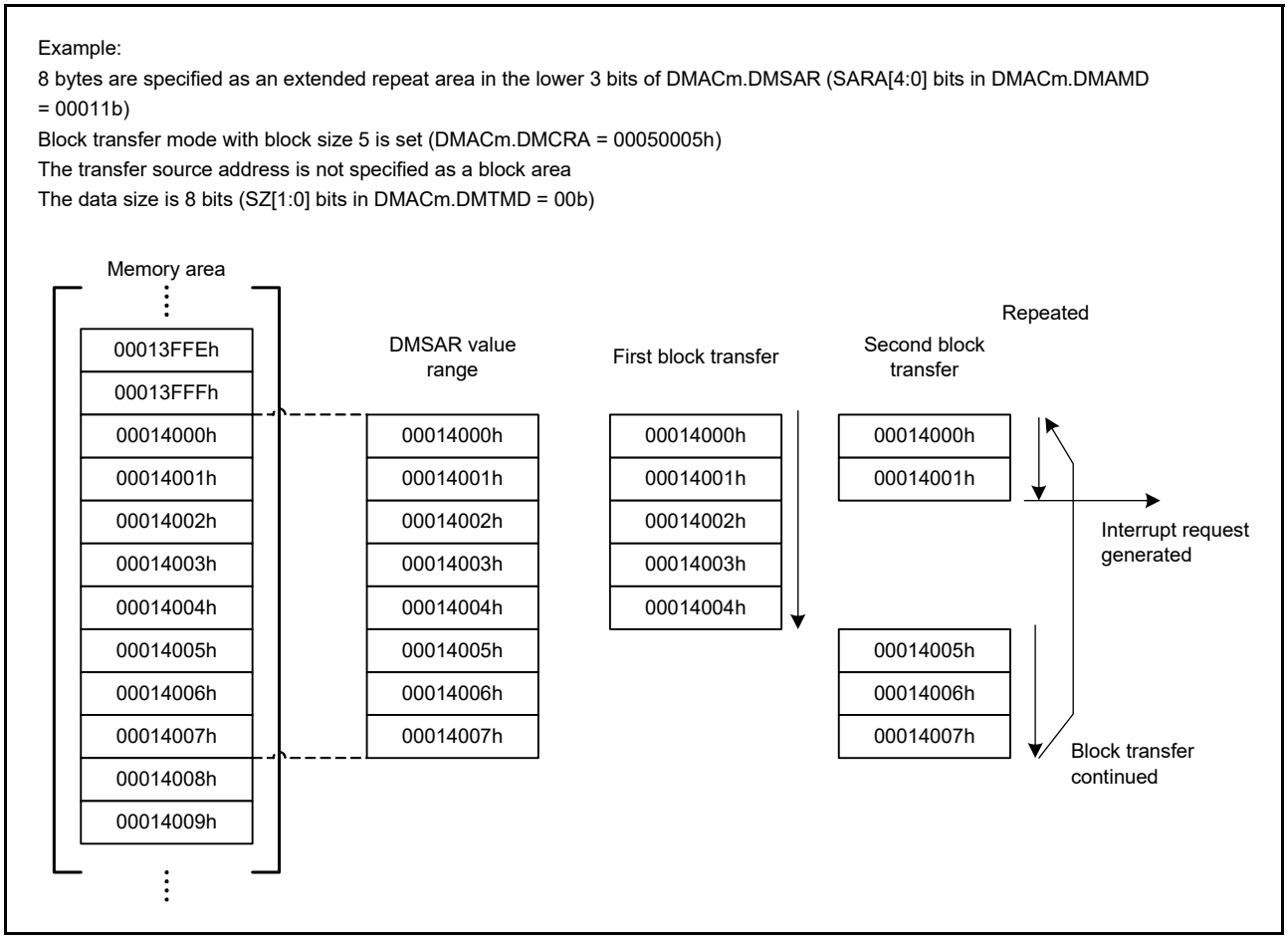


Figure 16.6 Example of extended repeat area function in block transfer mode

16.3.3 Address Update Function Using Offset

The source and destination addresses can be updated by fixing, incrementing, decrementing, or adding an offset. When offset addition is selected, the offset specified in the DMA Offset Register (DMACm.DMOFR) is added to the address every time the DMAC performs one data transfer. You can also subtract an offset by setting a negative value in DMACm.DMOFR. The negative value must be in two's complement.

Table 16.6 shows the address update method in each address update mode.

Table 16.6 Address update method in each address update mode

Address update mode	Settings of DMACm.DMAMD.SM[1:0] and DMACm.DMAMD.DM[1:0] for address update modes	Address update method for different SZ[1:0] settings in DMACm.DMTMD		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
Address fixed	00b	Fixed		
Offset addition	01b	+DMACm.DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	-1	-2	-4

Note 1. When setting a negative value in the DMA Offset Register, the value must be in two's complement, obtained by the following formula:
Two's complement of a negative offset value = ~ (offset) + 1 (~ = bit inversion)

(1) Basic transfer using offset addition

Figure 16.7 shows an example of address updating using offset addition.

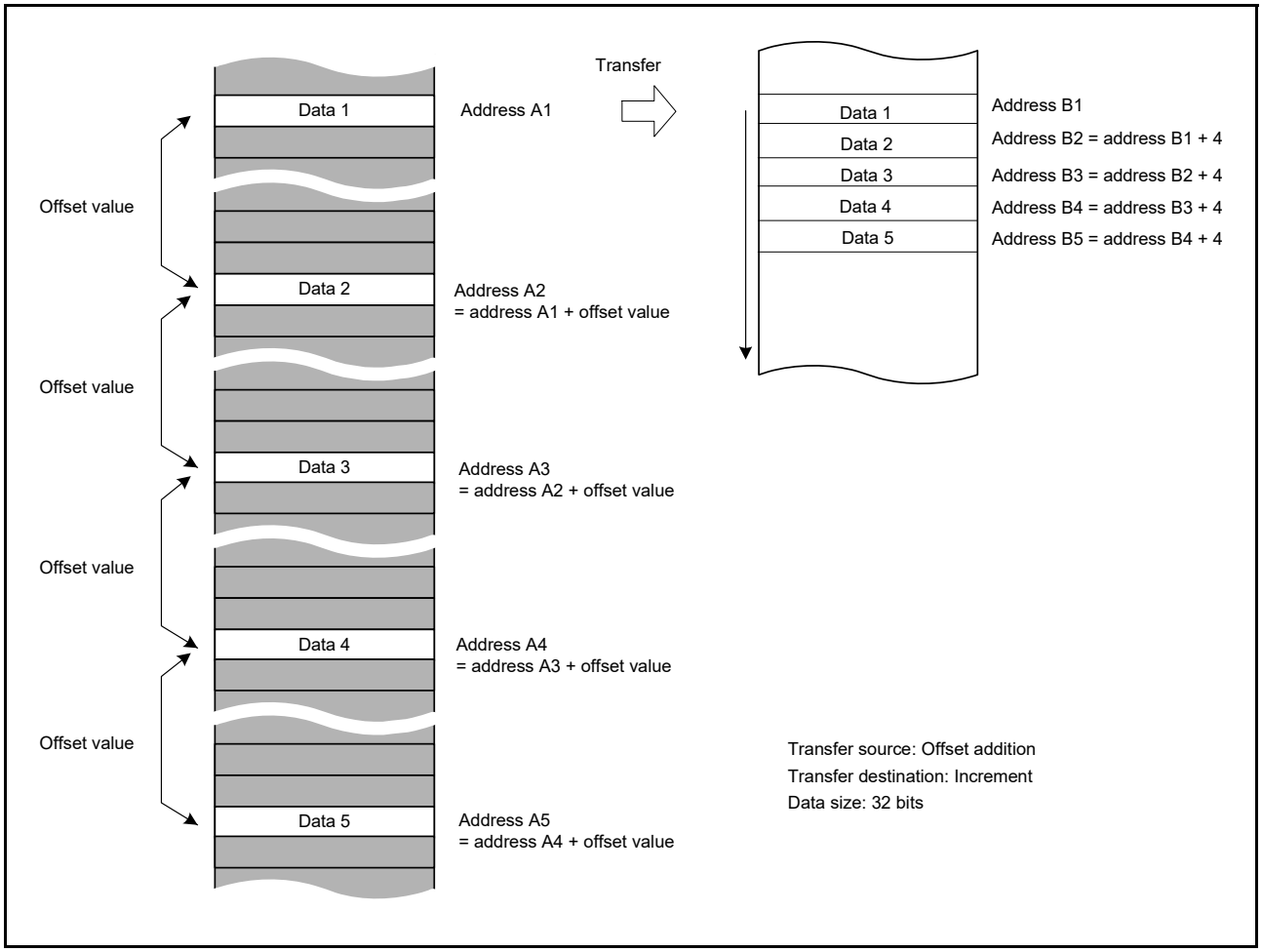


Figure 16.7 Example of address updating through offset addition

In Figure 16.7:

- The transfer data is 32 bits long
- Offset addition is set as the transfer source address update mode
- Increment is set as the transfer destination address update mode.

The second and subsequent data units are each read from the source address obtained by adding the offset value to the previous address. The data read from the addresses at the specified intervals is written to continuous locations on the destination.

(2) Example of XY conversion using offset addition

Figure 16.8 shows XY conversion using offset addition in repeat transfer mode. The settings are as follows:

- DMAC0.DMAMD — Transfer source address update mode: offset addition
- DMAC0.DMAMD — Transfer destination address update mode: destination address is incremented
- DMAC0.DMTMD — Transfer data size select: 32 bits
- DMAC0.DMTMD — Transfer mode select: repeat transfer
- DMAC0.DMTMD — Repeat area select: the source is specified as the repeat area
- DMAC0.DMOFR — Offset address: 10h
- DMAC0.DMCRA — Repeat size: 4h
- DMAC0.DMINT — The repeat size end interrupt is enabled.

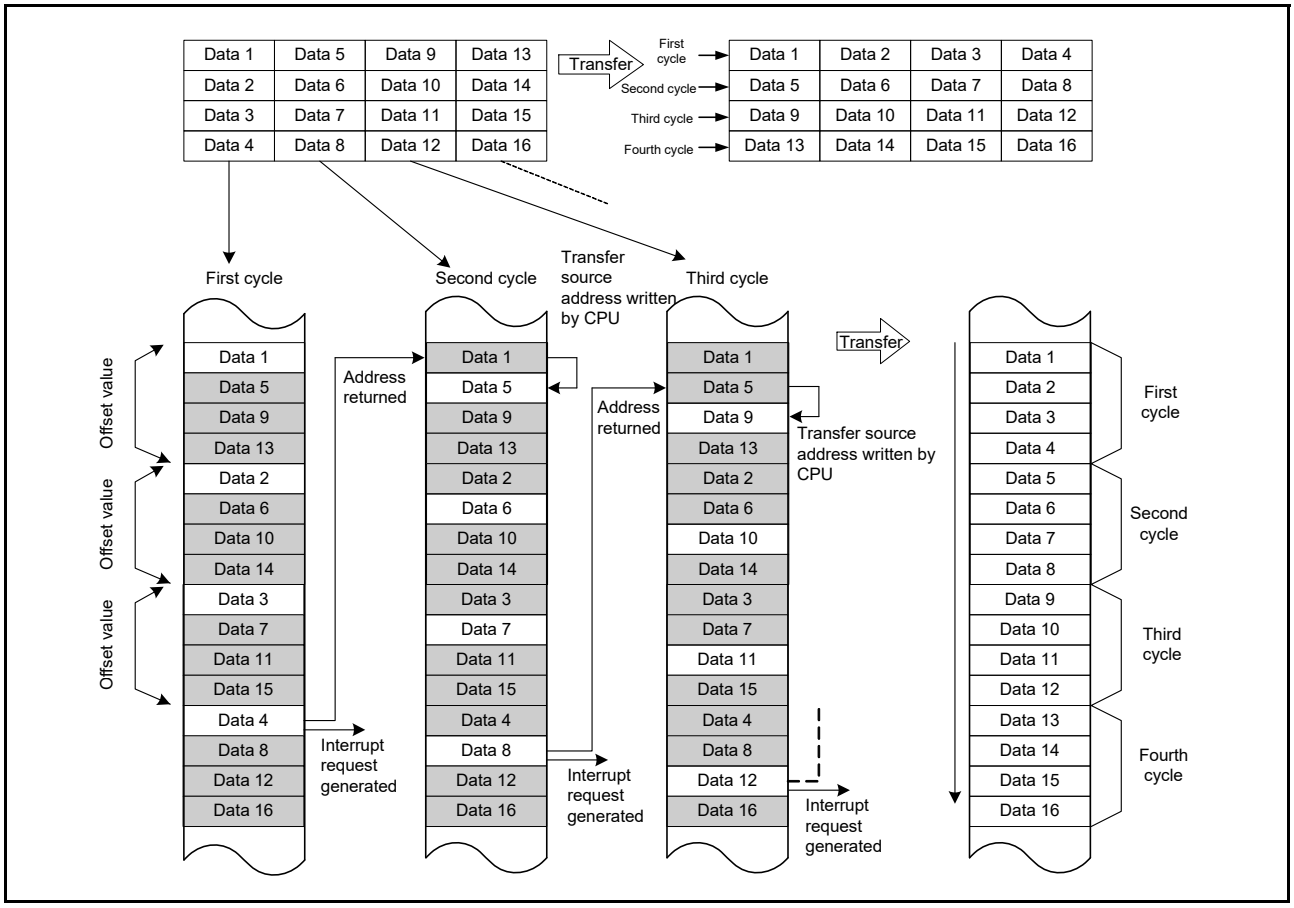


Figure 16.8 XY conversion operation using offset addition in repeat transfer mode

When a transfer starts, the offset value is added to the transfer source address every time data is transferred. The transfer data is written to continuous destination addresses. When data 4 is transferred:

- The repeat size of the transfers is complete
- The transfer source address returns to the transfer start address (the address of data 1 on the transfer source)
- A repeat size end interrupt is requested.

During the time this interrupt pauses the transfer, perform the following:

- DMAC0.DMSAR — Rewrite the DMA transfer source address to the address of data 5 (in this example, the data 1 address + 4)
- DMAC0.DMCNT — Set the DTE bit to 1.

The DMA transfer resumes from the state when the DMA transfer was stopped. The same operations are repeated until the transfer source data is transposed to the destination area (XY conversion).

Figure 16.9 shows a flow of the XY conversion.

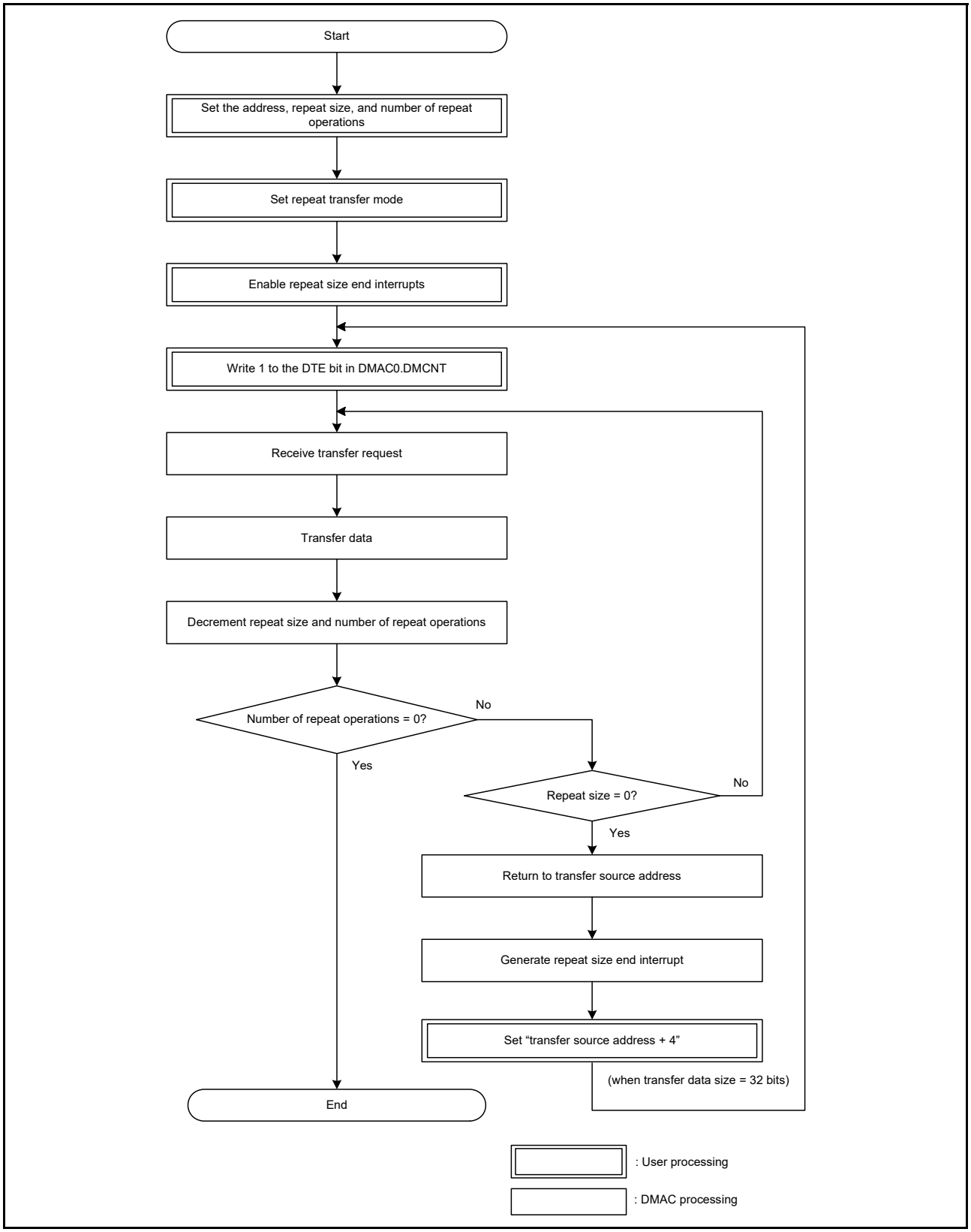


Figure 16.9 XY conversion flow using offset addition in repeat transfer mode

16.3.4 Activation Sources

Software, interrupt requests from the peripheral modules, and external interrupt requests can all be specified as DMAC activation sources. Set the DCTG[1:0] bits in DMACm.DMTMD to select the activation source.

(1) DMAC activation through software

To start DMA transfer through software:

1. Set the DCTG[1:0] bits in DMACm.DMTMD to 00b.
2. Set the DTE bit in DMACm.DMCNT to 1 (enable DMA transfer).
3. Set the DMST bit in DMAST to 1 (enable DMAC activation).
4. Set the SWREQ bit in DMACm.DMREQ to 1 (request DMA).

When the DMAC is activated by software while the CLRS bit in DMACm.DMREQ is 0, the SWREQ bit in DMACm.DMREQ sets to 0 after data transfer starts in response to a DMA transfer request.

When the DMAC is activated by software while the CLRS bit is 1, SWREQ does not clear to 0 after data transfer starts. A DMA transfer request is issued again after completion of a transfer.

(2) DMAC activation through interrupt requests from on-chip peripheral modules or external interrupt requests

You can specify interrupt requests from on-chip peripheral modules and external interrupt requests as DMAC activation sources. The activation source can be individually selected for each channel in ICU.DELSRn.DELS[8:0] (n = 0 to 7).

To start DMAC transfer through an interrupt request from an on-chip peripheral module or an external interrupt request:

1. Set the DCTG[1:0] bits in DMACm.DMTMD to 01b (select interrupts from the peripheral modules and the external interrupt pins).
2. Set the DTE bit in DMACm.DMCNT to 1 (enable DMA transfer).
3. Set ICU.DELSRn.DSEL to the event number (select the DMAC event link).
4. Set the DMST bit in DMAST to 1 (enable DMAC activation).

For interrupt requests specified as DMAC activation sources, see Table 13.3, Interrupt vector table in section 13, Interrupt Controller Unit (ICU).

16.3.5 Operation Timing

The following timing diagrams show the minimum number of execution cycles.

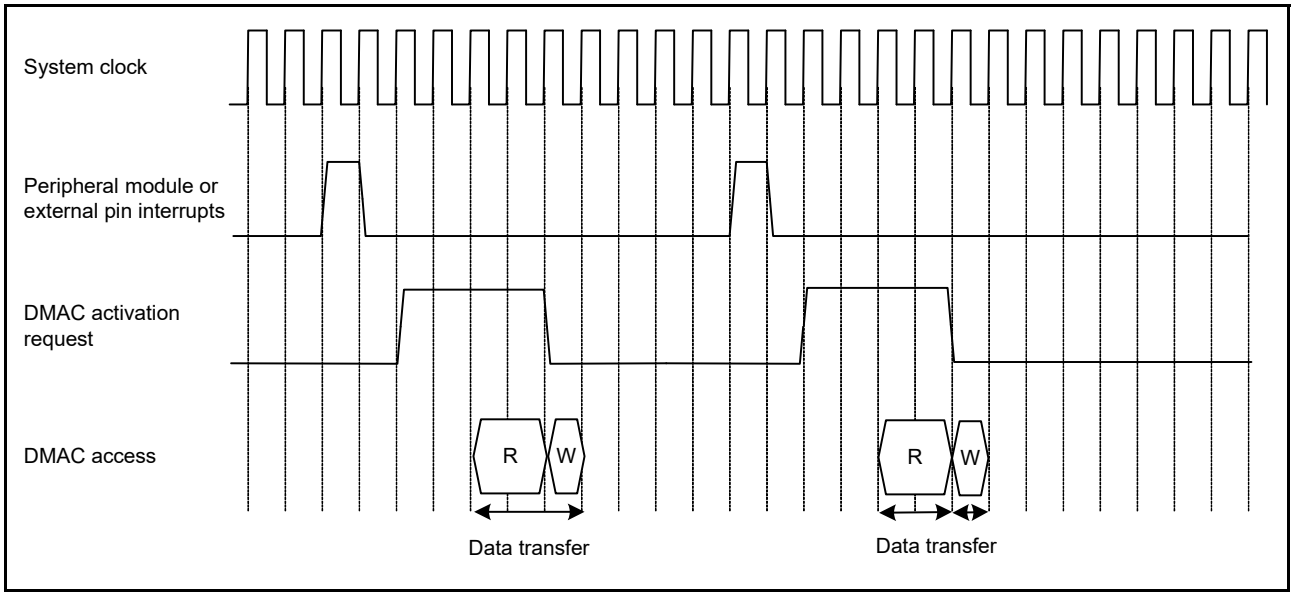


Figure 16.10 DMAC operation timing example 1 with DMA activation by interrupt from peripheral module or external interrupt input pin, in normal transfer mode or repeat transfer mode

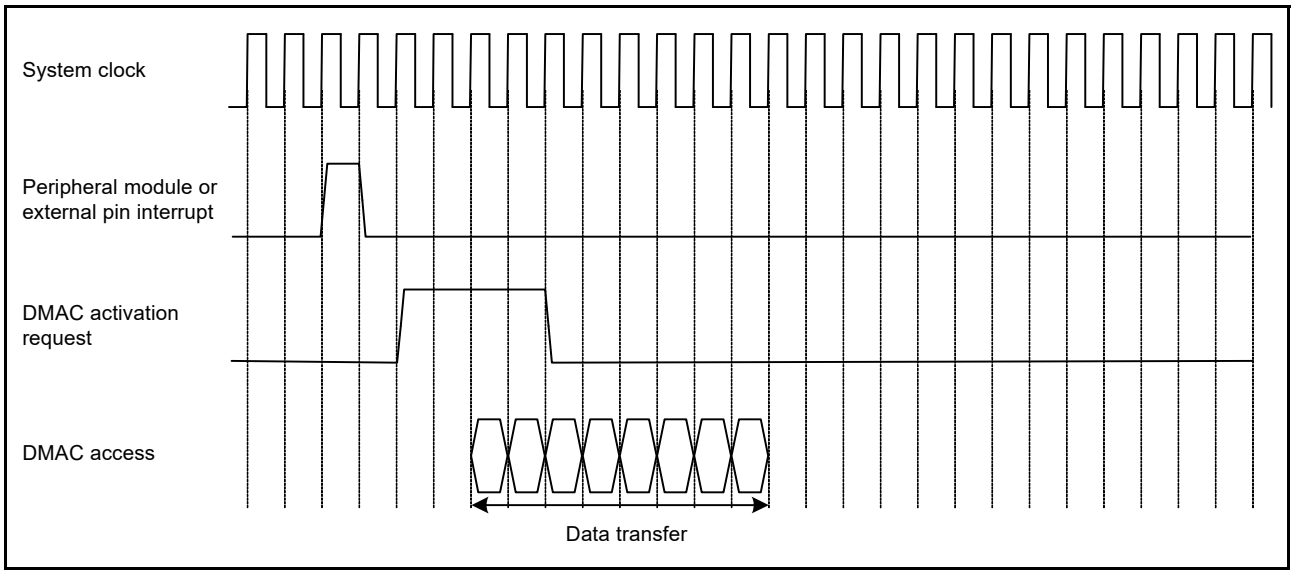


Figure 16.11 DMAC operation timing example 2 with DMA activation by interrupt from peripheral module or external interrupt input pin, in block transfer mode with block size = 4

16.3.6 Execution Cycles of DMAC

Table 16.7 lists the execution cycles in one DMAC data transfer operation.

Table 16.7 DMAC execution cycles

Transfer mode	Data transfer (read)	Data transfer (write)
Normal	Cr+Cs+1	Cw+Cs
Repeat	Cr+Cs+1	Cw+Cs
Block*1	P × (Cr+Cs)	P × (Cw+Cs)

Note: P = Block size (DMCRAH register setting).
Cr = Data read destination access cycle.
Cw = Data write destination access cycle.

Cs = When accessing SRAMHS and peripheral modules related to system control: 2 cycles.
When accessing elsewhere: 0 cycles.
When a slave bus changes by a read/write data transfer, add 1 more cycle.

Note 1. This is the case when the block size is 2 or more. When the block size is 1, normal transfer cycle applies.

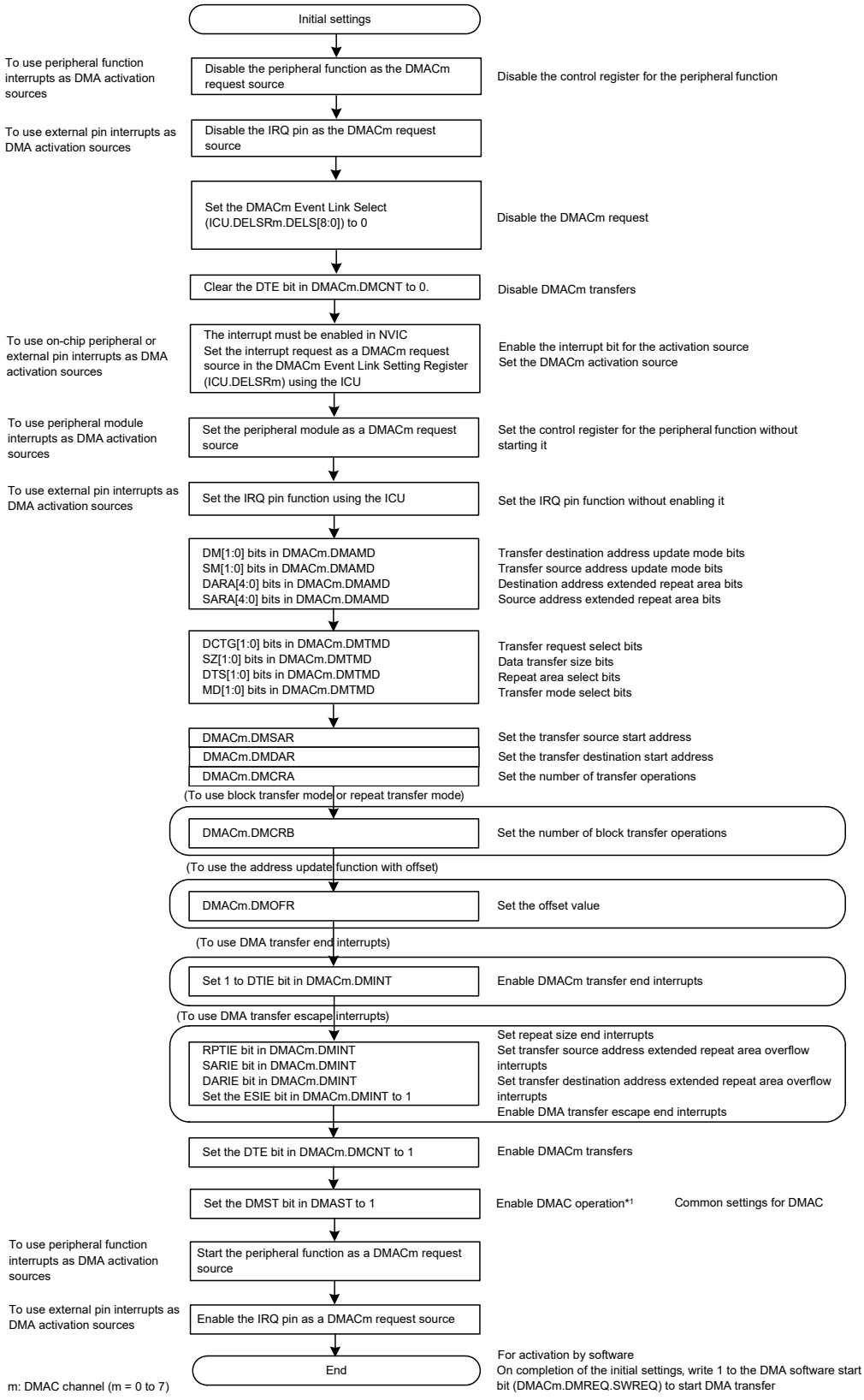
Cr and Cw depend on the access destination. For the number of cycles of each access destination, see section 40, SRAM and section 41, Flash Memory. The frequency ratio of the system clock and the peripheral clock is also taken into consideration.

The unit for +1 in the data transfer (read) column is 1 system clock cycle, ICLK. For the operation example, see section 16.3.5, Operation Timing.

The DMAC response time is the time from when the DMAC activation source is detected until the DMAC transfer starts. Table 16.7 does not include the time until the DMAC data transfer starts after the DMAC activation source becomes active.

16.3.7 Activating the DMAC

Figure 16.12 shows the register setting procedure.



Note 1. Setting of the DMAST.DMST bit does not necessarily have to follow the settings for the individual activation sources.

Figure 16.12 Register setting procedure

16.3.8 Starting DMA Transfer

To enable a DMA transfer of channel m, set the DTE bit in DMACm.DMCNT to 1 (DMA transfer enabled) and set the DMST bit in DMAST to 1 (DMAC activation enabled). New activation requests are not accepted during the transfer of another DMAC channel or DTC. When the proceeding transfer is complete, channel arbitration selects the DMA transfer request of the highest priority channel, and DMA transfer of that channel starts. When DMA transfer starts, the ACT flag in DMACm.DMSTS is set to 1 (the DMAC is in the active state).

16.3.9 Registers during DMA Transfer

The DMAC registers are updated by a DMA transfer. The value to be updated differs according to the other settings and the transfer state. The registers that are updated are DMSAR, DMDAR, DMCRA, DMCRB, DMCNT, and DMACm.DMSTS, described in the following sections. For details on register update operations in each transfer mode, see Table 16.3 to Table 16.5.

(1) DMA Source Address Register (DMACm.DMSAR)

After the data for one transfer request is transferred, the contents of DMSAR are updated to the address to be accessed by the next transfer request.

(2) DMA Destination Address Register (DMACm.DMDAR)

After the data for one transfer request is transferred, the contents of DMDAR are updated to the address to be accessed by the next transfer request.

(3) DMA Transfer Count Register (DMACm.DMCRA)

After the data for one transfer request is transferred, the count value is updated. The update operation depends on the transfer mode selected.

(4) DMA Block Transfer Count Register (DMACm.DMCRB)

After the data for one transfer request is transferred, the count value is updated. The update operation depends on the transfer mode selected.

(5) DMA Transfer Enable bit (DMACm.DMCNT.DTE)

The DMACm.DMCNT.DTE bit enables or disables data transfer through register write access. It is automatically cleared to 0 by the DMAC based on the DMA transfer state.

The conditions for clearing this bit by the DMAC are as follows:

- When the specified total volume of data transfer is complete
- When DMA transfer is stopped by a repeat size end interrupt
- When DMA transfer is stopped by an extended repeat area overflow interrupt.

Writing to the registers for channels whose associated DMACm.DMCNT.DTE bit is set to 1 is prohibited except for DMACm.DMCNT. Writes are only possible after the bit sets to 0.

(6) DMA Active flag (DMACm.DMSTS.ACT)

The ACT flag in DMSTS of DMACm indicates whether the DMACm is in the idle or active state. This flag is set to 1 when the DMAC starts data transfer, and sets to 0 when data transfer for one transfer request is complete. Even when DMA transfer is stopped by a write of 0 to the DTE bit in DMACm.DMCNT, this flag remains 1 until DMA transfer is complete.

(7) Transfer End Interrupt Flag (DMACm.DMSTS.DTIF)

The DTIF flag in DMACm.DMSTS is set to 1 after DMA transfer of the total transfer size is complete. When both this flag and the DTIE bit in DMACm.DMINT are 1, a transfer end interrupt is requested. This flag is set to 1 when the DMA transfer bus cycle is complete and the ACT flag in DMACm.DMSTS sets to 0, indicating the DMA transfer end. The flag automatically sets to 0 when the DTE bit in DMACm.DMCNT is set to 1 during interrupt handling.

(8) Transfer Escape End Interrupt Flag (DMACm.DMSTS.ESIF)

The ESIF flag in DMACm.DMSTS is set to 1 when a repeat size end interrupt or extended repeat area overflow interrupt

is requested. When this bit and the ESIE bit in DMACm.DMINT are 1, a transfer escape end interrupt is requested. This flag is set to 1 when the bus cycle of the DMA transfer that caused the interrupt request is complete and the ACT flag in DMACm.DMSTS sets to 0, indicating the DMA transfer end. The flag automatically sets to 0 when the DTE bit in DMACm.DMCNT is set to 1 during interrupt handling.

You must set the interrupt control register before sending an interrupt request from the DMAC to the CPU or the DTC. For more information, see section 13, Interrupt Controller Unit (ICU).

16.3.10 Channel Priority

When multiple DMA transfer requests occur, the DMAC determines the priority of channels that have DMA transfer requests.

The priority is fixed as channel 0 > channel 1 > channel 2 > channel 3 > channel 4 > channel 5 > channel 6 > channel 7. (channel 0 is the highest.)

When a DMA transfer request occurs during data transfer, channel arbitration starts after the final data unit is transferred, and DMA transfer of the highest-priority channel starts.

16.4 Ending DMA Transfer

The operation for ending a DMA transfer depends on the transfer end conditions. When a DMA transfer ends, the DTE bit in DMCNT and the ACT flag in DMACm.DMSTS change from 1 to 0.

16.4.1 Transfer End by Completion of Specified Total Number of Transfer Operations

(1) In normal transfer mode (DMACm.DMTMD.MD[1:0] = 00b)

When the value of DMACm.DMCRAL changes from 1 to 0, DMA transfer ends on the associated channel, the DTE bit in DMACm.DMCNT is set to 0, and the DTIF flag in DMACm.DMSTS is set to 1. If the DTIE bit in DMACm.DMINT is 1 at this time, a transfer end interrupt request is sent to the CPU or the DTC.

(2) In repeat transfer mode (DMACm.DMTMD.MD[1:0] = 01b)

When the value of DMACm.DMCRB changes from 1 to 0, DMA transfer ends on the associated channel, the DTE bit in DMACm.DMCNT is set to 0, and the DTIF flag in DMACm.DMSTS is set to 1. If the DTIE bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC.

(3) In block transfer mode (DMACm.DMTMD.MD[1:0] = 10b)

When the value of DMACm.DMCRB changes from 1 to 0, DMA transfer ends on the associated channel, the DTE bit in DMACm.DMCNT is set to 0, and the DTIF flag in DMACm.DMSTS is set to 1. If the DTIE bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC.

You must set the interrupt control register before sending an interrupt request from the DMAC to the CPU or the DTC. For more information, see section 13, Interrupt Controller Unit (ICU).

16.4.2 Transfer End by Repeat Size End Interrupt

In repeat transfer mode, if the RPTIE bit in DMACm.DMINT is 1, a repeat size end interrupt is requested when transfer of a single repeat size of data is complete. The DTE bit in DMACm.DMCNT is set to 0 and the ESIF flag in DMACm.DMSTS is set to 1. If the ESIE bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC. To resume the transfer, write 1 to the DTE bit in DMACm.DMCNT.

A repeat size end interrupt can also be requested in block transfer mode. When transfer of a single block size of data is complete, the interrupt is requested in the same way as in repeat transfer mode.

You must set the interrupt control register before sending an interrupt request from the DMAC to the CPU or the DTC. For more information, see section 13, Interrupt Controller Unit (ICU).

16.4.3 Transfer End by Interrupt on Extended Repeat Area Overflow

When an overflow on the extended repeat area occurs while the extended repeat area is specified and the SARIE or DARIE bit in DMACm.DMINT is 1, an extended repeat area overflow interrupt is requested. The DMA transfer is terminated, the DTE bit in DMACm.DMCNT is set to 0, and the ESIF flag in DMACm.DMSTS is set to 1. If the ESIE

bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC.

If this interrupt is requested during a read cycle, the subsequent write cycle is performed. In block transfer mode, if the interrupt is requested during a 1-block transfer, the remaining data in the block is transferred before transfer stops.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For more information, see section 13, Interrupt Controller Unit (ICU).

16.4.4 Precautions for the End of DMA Transfer

A DMA activation request source might occur in the next request after a DMA transfer completes. If this happens, the DMA transfer starts and the DMA activation request is held in DMAC. To prevent this, stop the DMA activation requests by clearing the DELSRn.DSELS[8:0] bits in the ICU to 0.

When the DMA activation request occurs after the last round of the DMA transfer is generated, clear the DMA activation request by setting ICU.DELSRm.IR bit to 0.

16.5 Interrupts

Each DMAC channel can output an interrupt request (DMACm_INT) to the CPU or DTC after transfer for one request is complete.

Table 16.8 lists the interrupt sources and their associated status flags and enable bits. Figure 16.13 shows the schematic logic diagram of the interrupt outputs (DMAC0 to DMAC7). Figure 16.14 shows the DMAC interrupt handling routine for resuming and terminating DMA transfers.

Table 16.8 Association between interrupt sources, interrupt status flags, and interrupt enable bits

Interrupt sources		Interrupt enable bits	Interrupt status flags	Request output enable bits
Transfer end		—	DMACm.DMSTS.DTIF	DMACm.DMINT.DTIE
Escape transfer end	Repeat size end	DMACm.DMINT.RPTIE	DMACm.DMSTS.ESIF	DMACm.DMINT.ESIE
	Source address extended repeat area overflow	DMACm.DMINT.SARIE		
	Destination address extended repeat area overflow	DMACm.DMINT.DARIE		

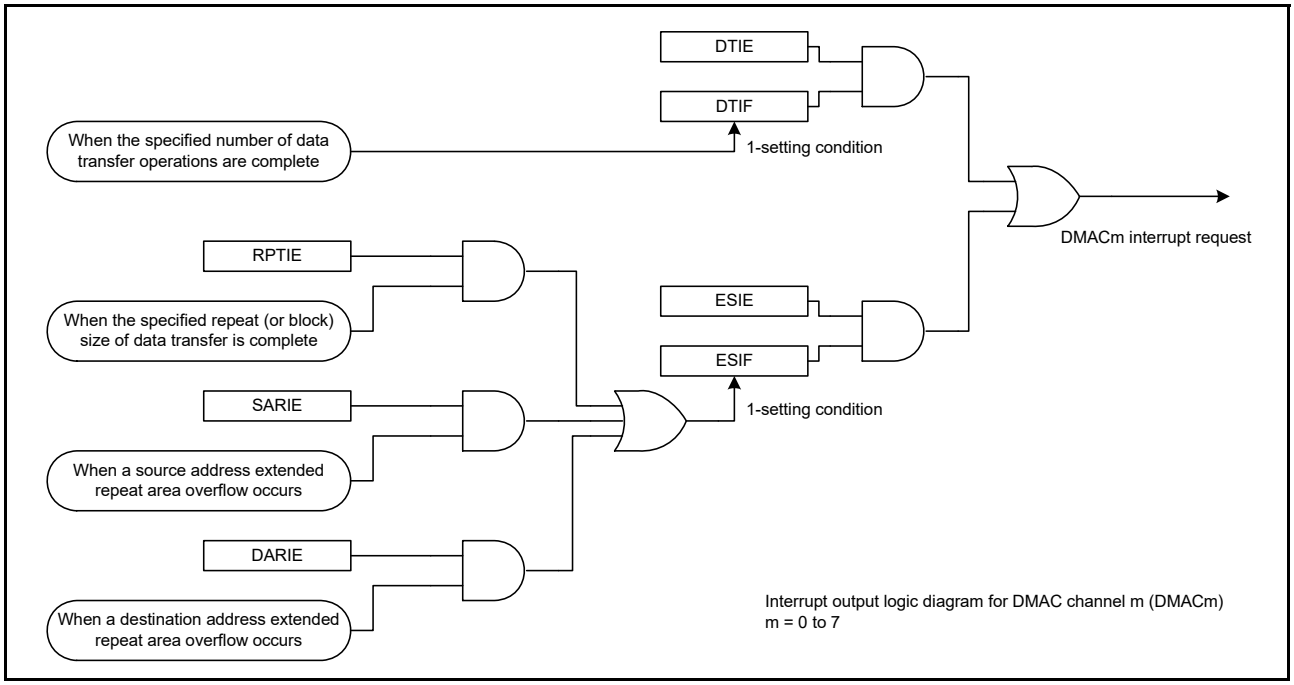


Figure 16.13 Schematic logic diagram of interrupt outputs for DMAC0 to DMAC7

Different procedures are used for canceling an interrupt to restart a DMA transfer as in the following cases:

- When terminating a DMA transfer
- When continuing a DMA transfer.

(1) When terminating a DMA transfer

Write 0 to the DTIF flag in DMACm.DMSTS to clear a transfer end interrupt, and to the ESIF flag in DMACm.DMSTS to clear a repeat size interrupt or an extended repeat area overflow interrupt. DMACm remains in the stopped state. When starting another DMA transfer, set the appropriate registers and set the DTE bit in DMACm.DMCNT to 1 (DMA transfer enabled).

(2) When continuing a DMA transfer

Write 1 to the DTE bit in DMACm.DMCNT. The ESIF flag in DMSTS of DMACm automatically sets to 0 (interrupt source cleared), and the DMA transfer resumes.

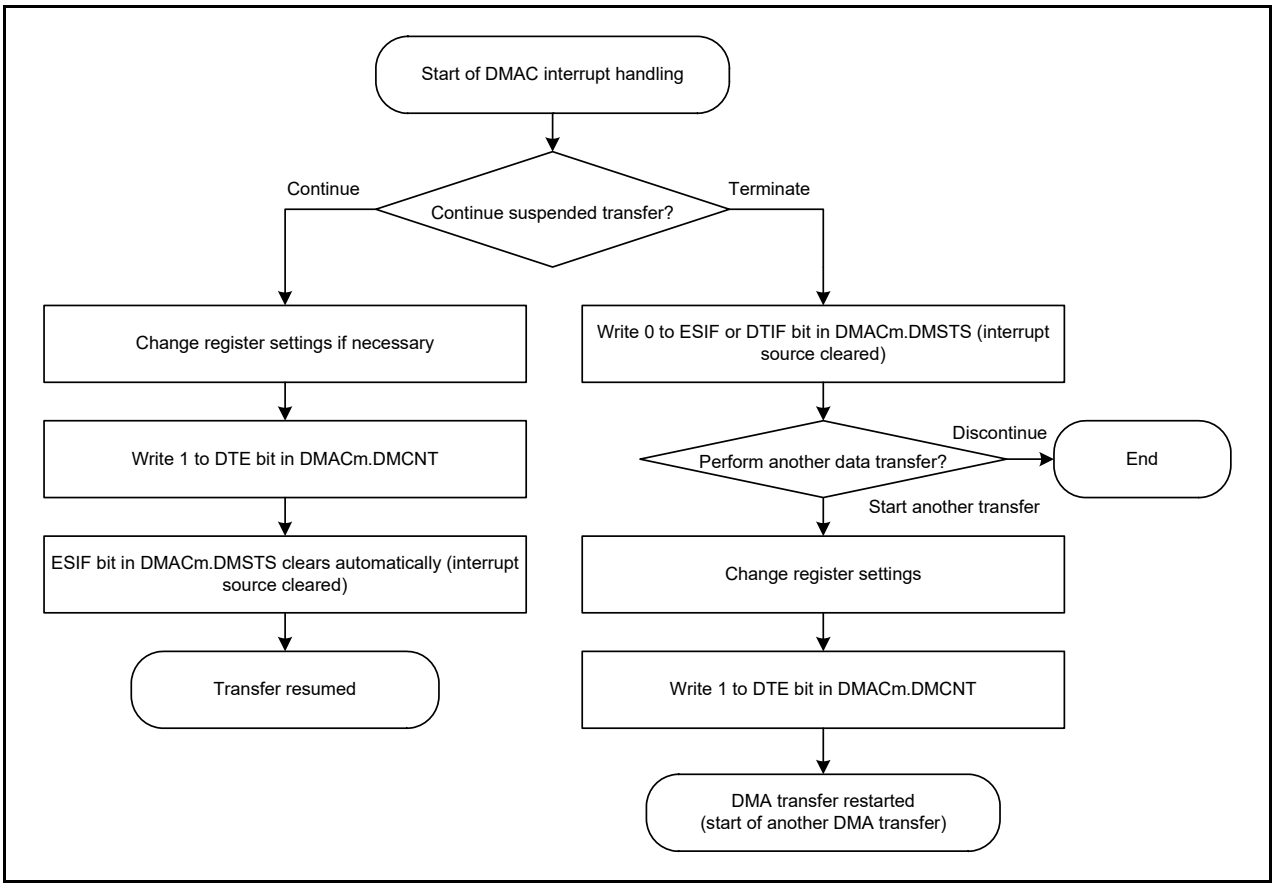


Figure 16.14 DMAC interrupt handling routine to resume or terminate a DMA transfer

16.6 Event Link

Each DMAC channel outputs an event link request signal (DMACm_INT) every time it completes a data transfer, or a block transfer in block transfer mode. For more information, see section 18, Event Link Controller (ELC).

16.7 Low Power Consumption Function

Before entering the module-stop state, Software Standby mode, or Deep Software Standby mode, you must first set the DMST bit in DMAST to 0 (DMAC suspended) and use the settings in the sections that follow.

(1) Module-stop function

Writing 1 to the MSTPA22 bit in MSTPCRA enables the module-stop function of the DMAC. If a DMA transfer is in progress when 1 is written to MSTPA22, the transition to the module-stop state continues after DMA transfer ends.

Access to the DMAC registers is prohibited while MSTPA22 is 1. Writing 0 to the MSTPA22 bit releases the DMAC from the module-stop state.

(2) Software Standby and Deep Software Standby modes

Use the settings described in section 11.7.1, Transitioning to Software Standby Mode and section 11.9.1, Transitioning to Deep Software Standby Mode.

If DMA transfer operations are in progress when the WFI instruction is executed, the DMA transfer completes before the transition to Software Standby mode or Deep Software Standby mode.

(3) Notes on low power consumption function

For information on the WFI instruction and register settings, see section 11.10.7, Timing of WFI Instruction.

To perform a DMA transfer after returning from a low power consumption mode, set the DMST bit in DMAST to 1 again. To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DMAC startup request, specify the CPU as the interrupt request destination, as described in section 13.4.2, Selecting Interrupt Request Destinations, then execute the WFI instruction.

16.8 Usage Notes

16.8.1 Access to Registers during DMA Transfer

Do not write to the following registers of DMACm while the ACT flag in DMSTS of the associated channel is set to 1 (DMAC active state) or the DTE bit in DMCNT of the associated channel is set to 1 (DMA transfer enabled):

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT
- DMAMD
- DMOFR.

16.8.2 DMA Transfer to Reserved Areas

DMA transfer to reserved areas is prohibited. If such an access is made, transfer results are not guaranteed. For details on reserved areas, see section 4, Address Space.

16.8.3 Setting the DMAC Event Link Setting Register of the Interrupt Controller Unit (ICU.DELSRn)

Before setting the DMAC Event Link Setting Register (ICU.DELSRn), make sure the DMA Transfer Enable bit (DMACm.DMCNT.DTE) is set to 0, to disable DMA transfer. Additionally, ensure that the DTC Activation Enable bit (ICU.IELSRn.DTCE) associated with the event number set in the ICU.DELSRn register is not set to 1. For details on ICU.IELSRn.DTCE and ICU.DELSRn, see section 13, Interrupt Controller Unit (ICU).

16.8.4 Suspending or Restarting DMA Activation

To suspend a DMA activation request, write 0 to the DMAC Event Link Select bits (ICU.DELSRn.DELS[8:0]). To restart the DMA transfer, write the event number to the ICU.DELSRn.DELS[8:0] bits with the settings shown in section 16.3.7, Activating the DMAC.

17. Data Transfer Controller (DTC)

17.1 Overview

The MCU includes a Data Transfer Controller (DTC) that performs data transfers when activated by an interrupt request. Table 17.1 lists the DTC specifications and Figure 17.1 shows a block diagram.

Table 17.1 DTC specifications

Parameter	Specifications
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the start address after the number of data transfers reaches the specified repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits (1024 bytes). • Block transfer mode A single activation leads to a single block transfer. The maximum block size is 256 × 32 bits = 1024 bytes.
Transfer channel	• Channel transfer can be associated with the interrupt source (transferred by a DTC activation request from the ICU) • Multiple data units can be transferred on a single activation source (chain transfer) • Chain transfers can be set to either execute when the counter is 0, or always execute.
Transfer space	• 4 GB (0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 halfword (16 bits), or 1 word (32 bits) • Single block size: 1 to 256 data units.
CPU interrupt source	• An interrupt request can be generated to the CPU on a DTC activation interrupt • An interrupt request can be generated to the CPU after a single data transfer • An interrupt request can be generated to the CPU after a data transfer of a specified volume.
Event link function	An event link request is generated after one data transfer (for block, after one block transfer)
Read skip	Read of transfer information can be skipped
Write-back skip	When the transfer source or destination address is specified as fixed, a write-back of transfer information can be skipped
Module-stop function	Module-stop state can be set to reduce power consumption

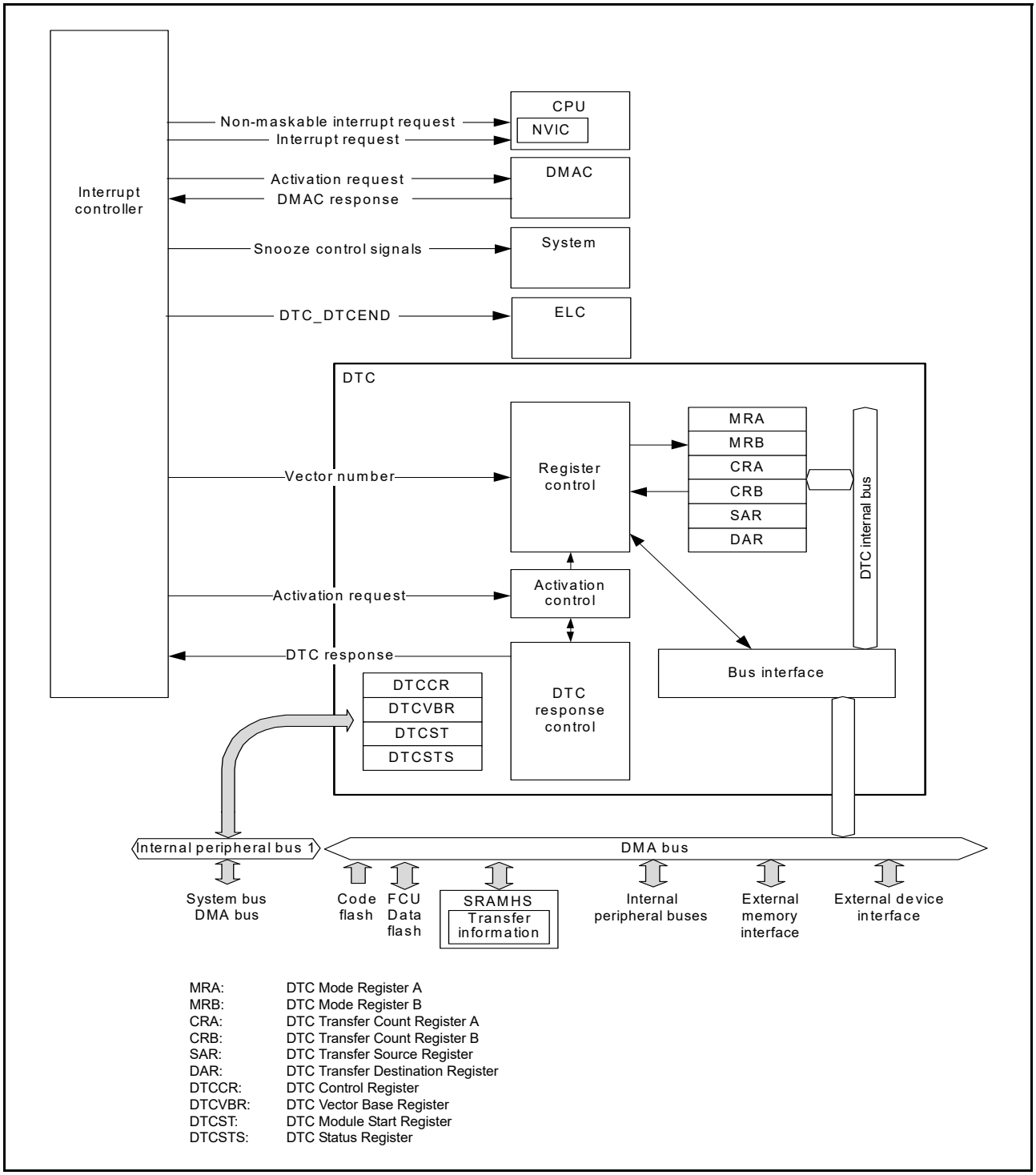


Figure 17.1 DTC block diagram

See 13.1 Overview, in section 13, Interrupt Controller Unit (ICU), for the connections between the DTC and NVIC in the CPU.

17.2 Register Descriptions

MRA, MRB, SAR, DAR, CRA, and CRB are all DTC internal registers that cannot be directly accessed from the CPU. Values to be set in these DTC internal registers are placed in the SRAM area as transfer information. When an activation request is generated, the DTC reads the transfer information from the SRAM area and sets it in its internal registers. After the data transfer ends, the internal register contents are written back to the SRAM area as transfer information.

17.2.1 DTC Mode Register A (MRA)

Address(es): (Inaccessible directly from the CPU. See section 17.3.1.)

	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as undefined. The write value should be 0.	—
b3, b2	SM[1:0]	Transfer Source Address Addressing Mode	b3 b2 0 0: Address in the SAR register is fixed (write-back to SAR) is skipped 0 1: Address in the SAR register is fixed (write-back to SAR is skipped) 1 0: SAR value is incremented after data transfer: +1 when SZ[1:0] = 00b +2 when SZ[1:0] = 01b +4 when SZ[1:0] = 10b. 1 1: SAR value is decremented after data transfer: -1 when SZ[1:0] = 00b -2 when SZ[1:0] = 01b -4 when SZ[1:0] = 10b.	—
b5, b4	SZ[1:0]	DTC Data Transfer Size	b5 b4 0 0: Byte (8-bit) transfer 0 1: Halfword (16-bit) transfer 1 0: Word (32-bit) transfer 1 1: Setting prohibited.	—
b7, b6	MD[1:0]	DTC Transfer Mode Select	b7 b6 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited.	—

The MRA register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 03h) and the DTC automatically transfers the MRA transfer information to and from the MRA register. See section 17.3.1, Allocating Transfer Information and the DTC Vector Table.

17.2.2 DTC Mode Register B (MRB)

Address(es): (Inaccessible directly from the CPU. See section 17.3.1.)

	b7	b6	b5	b4	b3	b2	b1	b0
	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as undefined. The write value should be 0.	—
b3, b2	DM[1:0]	Transfer Destination Address Addressing Mode	b3 b2 0 0: Address in the DAR register is fixed (write-back to DAR is skipped) 0 1: Address in the DAR register is fixed (write-back to DAR is skipped) 1 0: DAR value is incremented after data transfer: +1 when MRA.SZ[1:0] = 00b +2 when MRA.SZ[1:0] = 01b +4 when MRA.SZ[1:0] = 10b. 1 1: DAR value is decremented after data transfer: -1 when MRA.SZ[1:0] = 00b -2 when MRA.SZ[1:0] = 01b -4 when MRA.SZ[1:0] = 10b.	—
b4	DTS	DTC Transfer Mode Select	0: Select transfer destination as repeat or block area 1: Select transfer source as repeat or block area.	—
b5	DISEL	DTC Interrupt Select	0: Generate an interrupt request to the CPU when specified data transfer is complete 1: Generate an interrupt request to the CPU each time DTC data transfer is performed.	—
b6	CHNS	DTC Chain Transfer Select	0: Select continuous chain transfer 1: Select chain transfer to occur only when the transfer counter is changed from 1 to 0 or 1 to CRAH.	—
b7	CHNE	DTC Chain Transfer Enable	0: Chain transfer disabled 1: Chain transfer enabled.	—

The MRB register cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 02h) and the DTC automatically transfers the MRB transfer information to and from the MRB register. See section 17.3.1, Allocating Transfer Information and the DTC Vector Table.

DTS bit (DTC Transfer Mode Select)

The DTS bit selects either the transfer source or transfer destination as the repeat area or block area in repeat or block transfer mode.

CHNS bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition. When CHNE is 0, the CHNS setting is ignored. For details on the conditions for chain transfer, see Table 17.3, Chain transfer conditions.

When the next transfer is a chain transfer, completion of the specified number of transfers is not determined, the activation source flag is not cleared, and an interrupt request to the CPU is not generated.

CHNE bit (DTC Chain Transfer Enable)

The CHNE bit enables chain transfer. The chain transfer condition is selected in the CHNS bit. For details on chain transfer, see section 17.4.6, Chain Transfer.

17.2.3 DTC Transfer Source Register (SAR)

Address(es): (Inaccessible directly from the CPU. See section 17.3.1.)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The SAR register sets the transfer source start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 04h) and the DTC automatically transfers the SAR transfer information to and from the SAR register. See section 17.3.1, Allocating Transfer Information and the DTC Vector Table.

Note: Misalignment is prohibited for DTC transfers. Bit [0] must be 0 when MRA.SZ[1:0] = 01b. Bits [1] and [0] must be 0 when MRA.SZ[1:0] = 10b.

17.2.4 DTC Transfer Destination Register (DAR)

Address(es): (inaccessible directly from the CPU. See section 17.3.1.)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

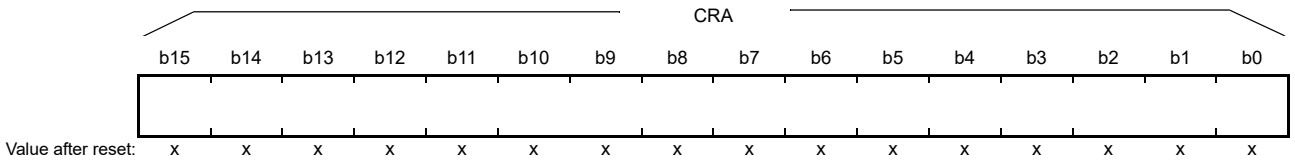
The DAR register sets the transfer destination start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 08h) and the DTC automatically transfers the DAR transfer information to and from the DAR register. See section 17.3.1, Allocating Transfer Information and the DTC Vector Table.

Note: Misalignment is prohibited for DTC transfers. Bit [0] must be 0 when MRA.SZ[1:0] = 01b. Bits [1] and [0] must be 0 when MRA.SZ[1:0] = 10b.

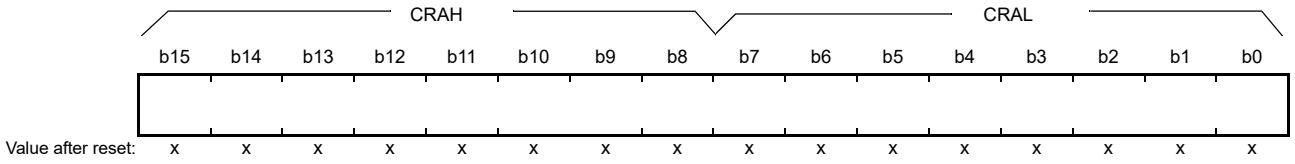
17.2.5 DTC Transfer Count Register A (CRA)

Address(es): (inaccessible directly from the CPU. See section 17.3.1.)

- Normal transfer mode



- Repeat transfer mode/block transfer mode



x: Undefined

Symbol	Register name	Description	R/W
CRAL	Transfer Counter A Lower Register	Specify the transfer count	—
CRAH	Transfer Counter A Upper Register		—

Note: The function depends on the transfer mode.
Note: Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

The CRA register cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0Eh) and the DTC automatically transfers the CRA transfer information to and from the CRA register. See section 17.3.1, Allocating Transfer Information and the DTC Vector Table.

(1) Normal transfer mode (MRA.MD[1:0] = 00b)

In normal transfer mode, CRA functions as a 16-bit transfer counter. The transfer count is 1, 65535, and 65536 when the set value is 0001h, FFFFh, and 0000h, respectively. The CRA value is decremented (-1) on each data transfer.

(2) Repeat transfer mode (MRA.MD[1:0] = 01b)

In repeat transfer mode, the CRAH register holds the transfer count and the CRAL register functions as an 8-bit transfer counter. The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively. The CRAL value is decremented (-1) on each data transfer. When it reaches 00h, the CRAH value is transferred to CRAL.

(3) Block transfer mode (MRA.MD[1:0] = 10b)

In block transfer mode, the CRAH register holds the transfer count and the CRAL register functions as an 8-bit block size counter. The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively. The CRAL value is decremented (-1) at each data transfer. When it reaches 00h, the CRAH value is transferred to CRAL.

17.2.6 DTC Transfer Count Register B (CRB)

Address(es): (Inaccessible directly from the CPU. See section 17.3.1.)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The CRB register sets the block transfer count for block transfer mode. The transfer count is 1, 65535, and 65536 when the set value is 0001h, FFFFh, and 0000h, respectively. The CRB value is decremented (-1) when the final data of a single block size is transferred. When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.

CRB cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0Ch) and the DTC automatically transfers the CRB transfer information to and from the CRB register. See section 17.3.1, Allocating Transfer Information and the DTC Vector Table.

17.2.7 DTC Control Register (DTCCR)

Address(es): DTC.DTCCR 4000 5400h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	RRS	DTC Transfer Information Read Skip Enable	0: Transfer information read is not skipped 1: Transfer information read is skipped when vector numbers match.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RRS bit (DTC Transfer Information Read Skip Enable)

The RRS bit enables skipping of transfer information reads when the vector numbers match. The DTC vector number is compared with the vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the transfer information. However, when the previous transfer is a chain transfer, the transfer information is read regardless of the value in the RRS bit.

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit value.

17.2.8 DTC Vector Base Register (DTCVBR)

Address(es): DTC.DTCVBR 4000 5404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit name	Description	R/W
b31 to b0	DTC Vector Base Address	Set the DTC vector base address. The lower 10 bits should be 0.	R/W

The DTCVBR register sets the base address to calculate the DTC vector table address, which can be set in the range of 0000 0000h to FFFF FFFFh (4 GB) in 1-KB units.

17.2.9 DTC Module Start Register (DTCST)

Address(es): DTC.DTCST 4000 540Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DTCST	DTC Module Start	0: DTC module stopped 1: DTC module started.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCST bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When the DTCST bit is set to 0, transfer requests are no longer accepted. If this bit is set to 0 during a data transfer, the accepted transfer request is active until processing is complete.

DTCST must be set to 0 before transitioning to any of the following state or mode:

- Module-stop state
- Software Standby mode without Snooze mode transition
- Deep Software Standby mode.

For details on these transitions, see section 17.10, Module-Stop Function, and section 11, Low Power Modes.

17.2.10 DTC Status Register (DTCSTS)

Address(es): DTC.DTCSTS 4000 540Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	VECN[7:0]	DTC-Activating Vector Number Monitoring	These bits indicate the vector number for the activation source when a DTC transfer is in progress. The value is only valid if a DTC transfer is in progress (ACT flag is 1).	R
b14 to b8	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b15	ACT	DTC Active Flag	0: DTC transfer operation is not in progress 1: DTC transfer operation is in progress.	R

VECN[7:0] bits (DTC-Activating Vector Number Monitoring)

While transfer by the DTC is in progress, the VECN[7:0] bits indicate the vector number associated with the activation source for the transfer. The value read from the VECN[7:0] bits is valid if the ACT flag is 1, indicating that a DTC transfer is in progress, and invalid if the ACT flag is 0, indicating that no DTC transfer is in progress.

ACT flag (DTC Active Flag)

The ACT flag indicates the state of the DTC transfer operation.

[Setting condition]

- When the DTC is activated by a transfer request.

[Clearing condition]

- When transfer by the DTC, in response to a transfer request, is complete.

17.3 Activation Sources

The DTC is activated by an interrupt request. Setting the ICU.IELSRn.DTCE bit to 1 enables activation of the DTC by the associated interrupt. The selector output *n* number set in ICU.IELSRn is defined as the interrupt vector number, where n = 0 to 95. For an enabled interrupt, the specific DTC interrupt source associated with each interrupt vector number n is selected in ICU.IELSRn.IELS[8:0] where n = 0 to 95, as listed in Table 13.4, Event table, in section 13, Interrupt Controller Unit (ICU). For activation by software, see section 18.2.2, Event Link Software Event Generation Register n (ELSEGRn) (n = 0, 1).

The interrupt vector number is equivalent to the DTC vector table number. After the DTC accepted an activation request, it does not accept another activation request until transfer for that single request is complete, regardless of the priority of the requests. When multiple activation requests are generated during a DMAC or DTC transfer, a highest priority request is accepted on completion of the transfer. When multiple activation requests are generated while the DTC Module Start bit (DTCST.DTCST) is 0, the DTC accepts the highest-priority request when DTCST.DTCST is subsequently set to 1. The smaller interrupt vector number has higher priority.

The DTC performs the following operations at the start of a single data transfer or for a chain transfer, after the last of the consecutive transfers:

- On completion of a specified round of data transfer, the ICU.IELSRn.DTCE bit is set to 0, and an interrupt request is sent to the CPU
- If the MRB.DISEL bit is 1, an interrupt request is sent to the CPU on completion of a data transfer
- For other transfers, the ICU.IELSRn.IR bit of the activation source is set to 0 at the start of the data transfer.

17.3.1 Allocating Transfer Information and the DTC Vector Table

The DTC reads the start address of the transfer information associated with each activation source from the vector table and reads the transfer information starting at that address.

The vector table must be located so that the lower 10 bits of the base address (start address) are 0. Use the DTC Vector Base Register (DTCVBR) to set the base address of the DTC vector table. Transfer information is allocated in the SRAM area. In the SRAM area, the start address of the transfer information *n* with vector number *n* must be 4n added to the base address in the vector table.

Figure 17.2 shows the relationship between the DTC vector table and transfer information. Figure 17.3 shows the allocation of transfer information in the SRAM area.

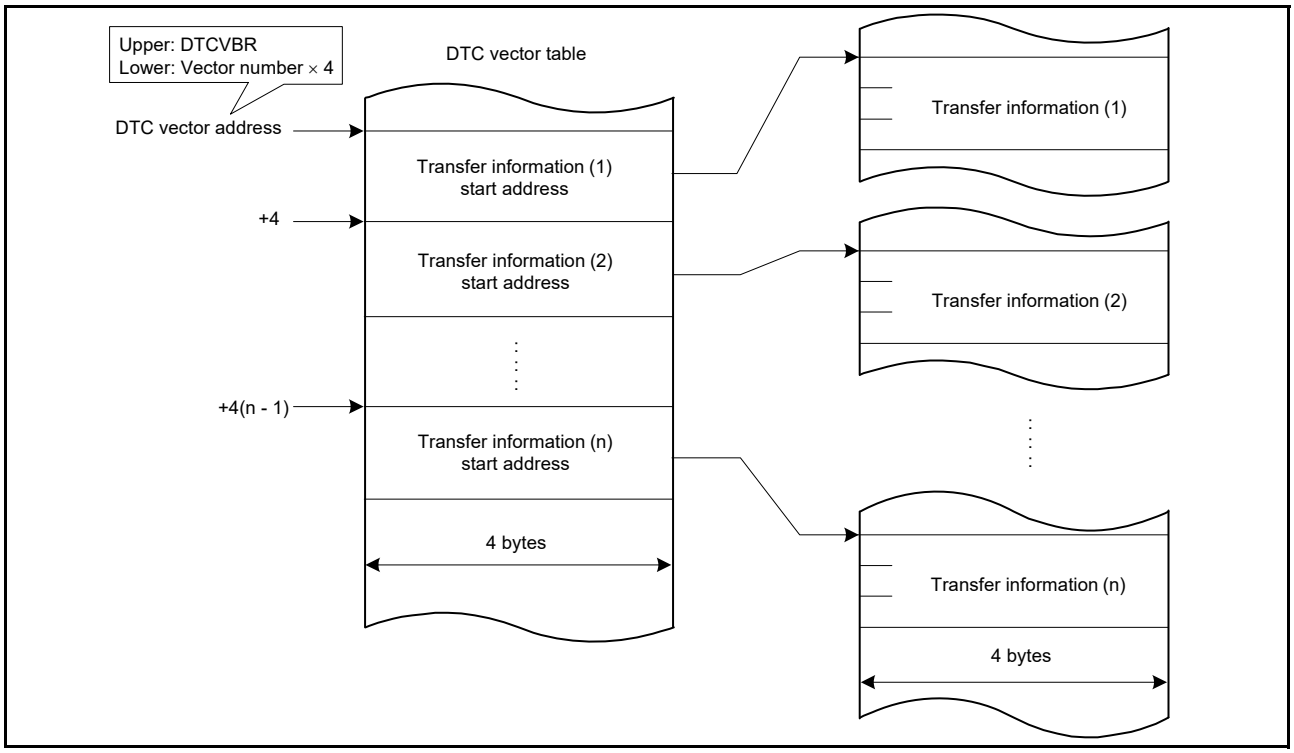


Figure 17.2 DTC vector table and transfer information

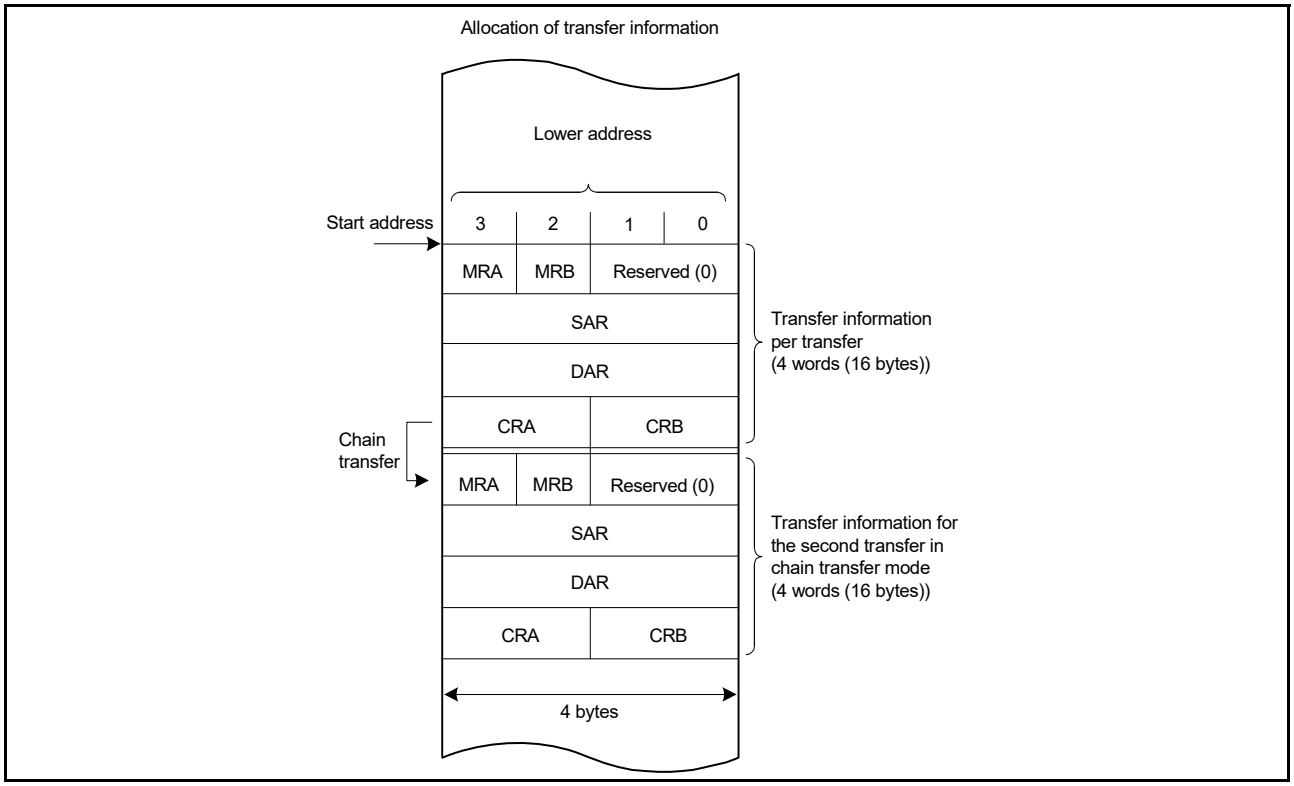


Figure 17.3 Allocation of transfer information in the SRAM area

17.4 Operation

The DTC transfers data according to the transfer information. Storage of the transfer information in the SRAM area is required before a DTC operation. When the DTC is activated, it reads the DTC vector associated with the vector number. The DTC then reads the transfer information from the transfer information store address referenced by the DTC vector and transfers the data. After the data transfer, the DTC writes back the transfer information. Storing the transfer information in the SRAM area allows data transfer of any number of channels.

The transfer modes include:

- Normal transfer mode
- Repeat transfer mode
- Block transfer mode.

The DTC specifies a transfer source address in the SAR register and a transfer destination address in the DAR register. The values in these registers are incremented, decremented, or address-fixed independently after the data transfer.

Table 17.2 describes the DTC transfer modes.

Table 17.2 DTC transfer modes

Transfer mode	Data size transferred on single transfer request	Increment or decrement of memory address	Settable transfer count
Normal transfer mode	1 byte (8 bits), 1 halfword (16 bits), or 1 word (32 bits)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65536
Repeat transfer mode*1	1 byte (8 bits), 1 halfword (16 bits), or 1 word (32 bits)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes))	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65536

Note 1. Set the transfer source or destination as the repeat area.

Note 2. Set the transfer source or destination as the block area.
Note 3. After a data transfer of the specified count, the initial state is restored and operation restarts.

Setting the MRB.CHNE bit to 1 allows multiple transfers or a chain transfer on a single activation source. It also enables a chain transfer when the specified data transfer is complete.

Figure 17.4 shows the operation flow of the DTC. Table 17.3 lists the chain transfer conditions. The combination of control information for the second and subsequent transfers are omitted in this table.

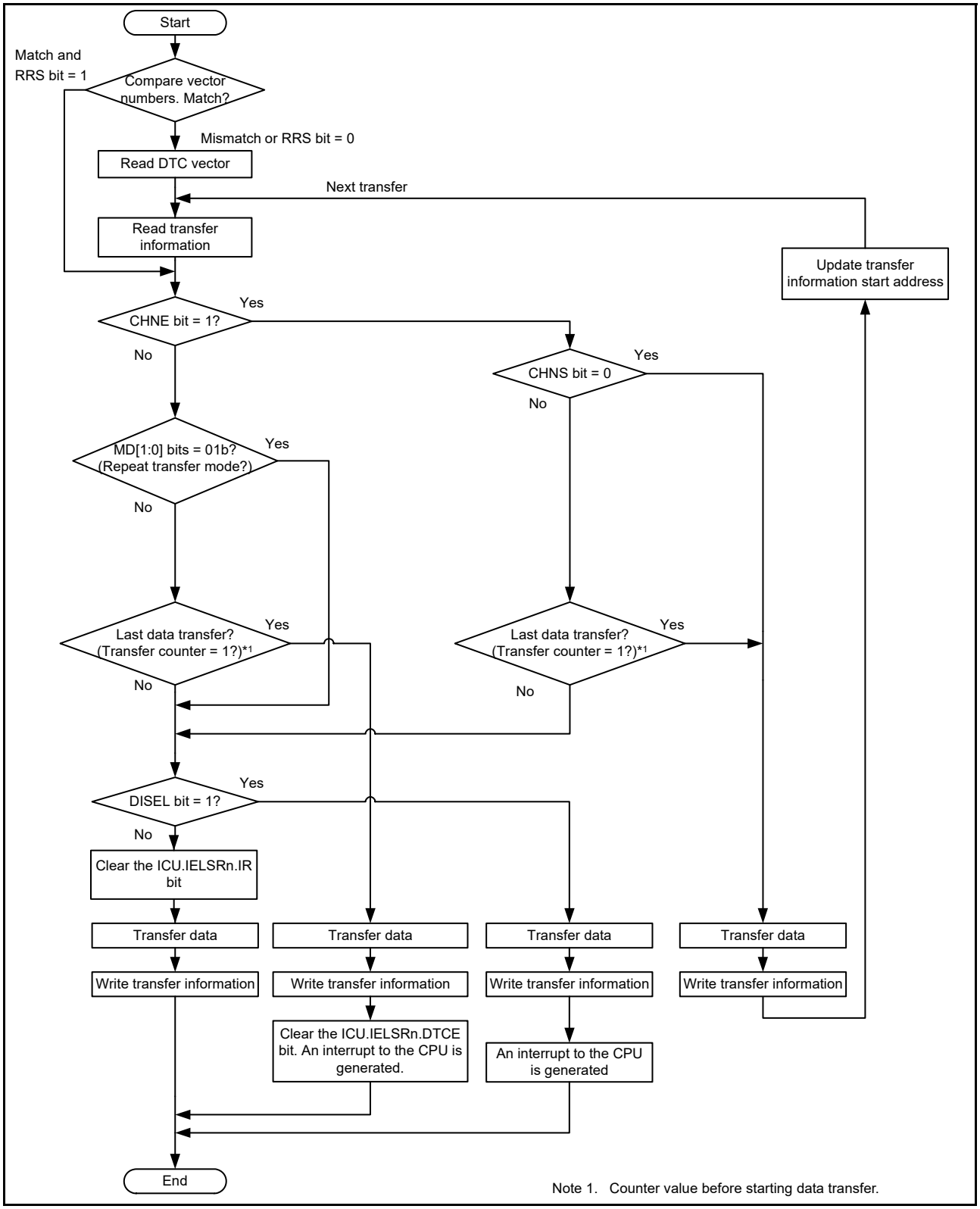


Figure 17.4 DTC operation flow

Table 17.3 Chain transfer conditions

First transfer				Second transfer*3				
CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	DTC transfer
0	-	0	Other than (1 → 0)	-	-	-	-	Ends after the first transfer
0	-	0	(1 → 0)	-	-	-	-	Ends after the first transfer with an interrupt request to the CPU
0	-	1	-	-	-	-	-	
1	0	-	-	0	-	0	Other than (1 → 0)	Ends after the second transfer
				0	-	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	-	1	-	
1	1	0	Other than (1 → *)	-	-	-	-	Ends after the first transfer
1	1	-	(1 → *)	0	-	0	Other than (1 → 0)	Ends after the second transfer
				0	-	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	-	1	-	
1	1	1	Other than (1 → *)	-	-	-	-	Ends after the first transfer with an interrupt request to the CPU

Note 1. The transfer counter used depends on the transfer modes as follows:
Normal transfer mode — CRA register
Repeat transfer mode — CRAL register
Block transfer mode — CRB register

Note 2. On completion of a data transfer, the counters operate as follows:
1 → 0 in normal and block transfer modes
1 → CRAH in repeat transfer mode
(1 → *) in the table indicates both of these two operations, depending on the mode.

Note 3. Chain transfer can be selected for the second or subsequent transfers. The conditions for the combination of the second transfer and CHNE bit = 1 is omitted.

17.4.1 Transfer Information Read Skip Function

Reading of vector addresses and transfer information can be skipped by setting the DTCCR.RRS bit. When a DTC activation request is generated, the current DTC vector number is compared to the DTC vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, the DTC data transfer is performed without reading the vector address and transfer information. However, when the previous transfer is a chain transfer, the vector address and transfer information are read. Additionally, when the transfer counter (CRA register) becomes 0 during the previous normal transfer, or when the transfer counter (CRB register) becomes 0 during the previous block transfer, transfer information is read regardless of the RRS bit. Figure 17.12 shows an example of a transfer information read skip.

To update the vector table and transfer information:

1. Set the RRS bit to 0.
2. Update the vector table and transfer information.
3. Set the RRS bit to 1.

The stored vector number is discarded by setting the RRS bit to 0. The updated DTC vector table and transfer information are read in the next activation process.

17.4.2 Transfer Information Write-Back Skip Function

When the MRA.SM[1:0] bits or the MRB.DM[1:0] bits are set to *address fixed*, a part of the transfer information is not written back. Table 17.4 lists the transfer information write-back skip conditions and the associated registers. The CRA and CRB registers are written back, and the write-back of the MRA and MRB registers is skipped.

Table 17.4 Transfer information write-back skip conditions and applicable registers

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	**SAR register**	**DAR register**
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

17.4.3 Normal Transfer Mode

Normal transfer mode allows a 1-byte (8-bit), 1-halfword (16-bit), or 1-word (32-bit) data transfer on a single activation source. The transfer count can be set from 1 to 65536. Transfer source and destination addresses can be independently set to increment, decrement, or remain fixed. This mode enables an interrupt request to the CPU to be generated at the end of a specified-count transfer.

Table 17.5 lists the register functions in normal transfer mode, and Figure 17.5 shows the memory map of normal transfer mode.

Table 17.5 Register functions in normal transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	Increment, decrement, or fixed*1
DAR	Transfer destination address	Increment, decrement, or fixed*1
CRA	Transfer counter A	CRA - 1
CRB	Transfer counter B	Not updated

Note 1. Write-back operation is skipped in address-fixed mode.

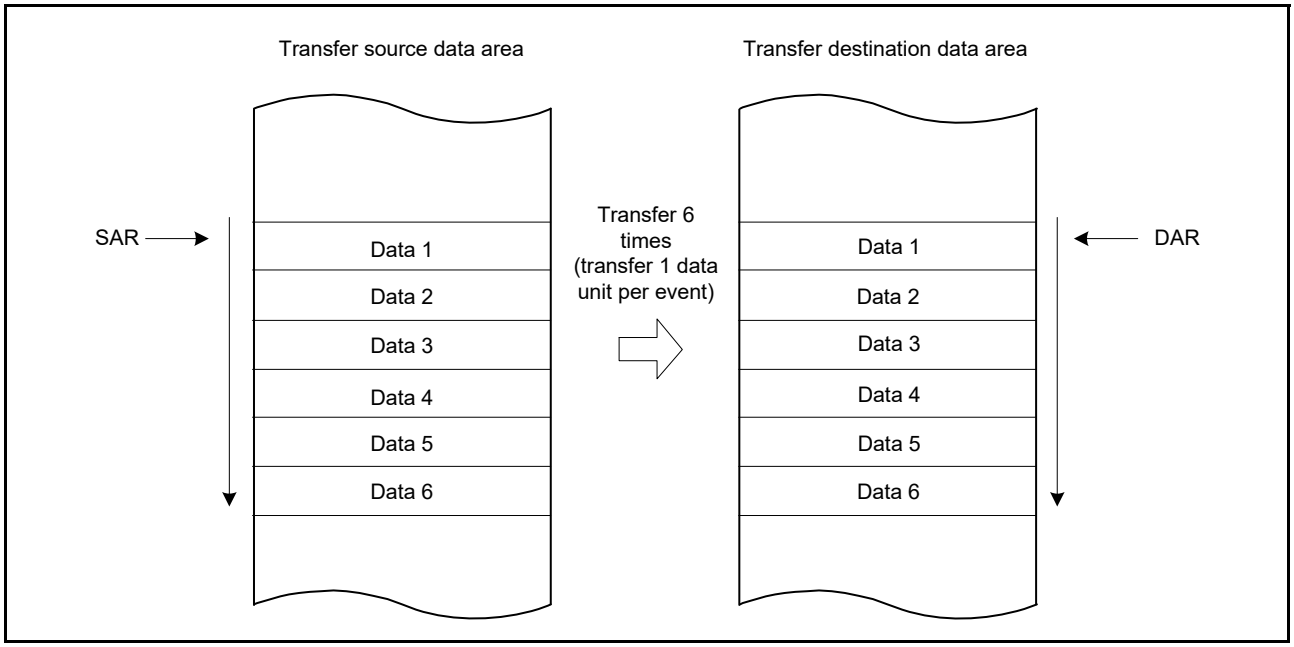


Figure 17.5 Memory map of normal transfer mode (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRA = 0006h)

17.4.4 Repeat Transfer Mode

Repeat transfer mode allows a 1-byte (8-bit), 1-halfword (16-bit), or 1-word (32-bit) data transfer on a single activation source. Specify either transfer source or transfer destination for the repeat area in the MRB.DTS bit. The transfer count can be set from 1 to 256. When the specified transfer count is complete, the initial value of the address register specified in the repeat area is restored, the initial value of the transfer counter is restored, and transfer is repeated. The other address register is incremented or decremented continuously or remains unchanged.

When the transfer counter CRAL decrements to 00h in repeat transfer mode, the CRAL value is updated to the value set in the CRAH register. As a result, the transfer counter does not clear to 00h, which disables interrupt requests to the CPU when the MRB.DISEL bit is set to 0. An interrupt request to the CPU is generated when the specified data transfer is complete.

Table 17.6 lists the register functions in repeat transfer mode, and Figure 17.6 shows the memory map of repeat transfer mode.

Table 17.6 Register functions in repeat transfer mode

Register	Description	Value written back by writing transfer information	
		When CRAL is not 1	When CRAL is 1
SAR	Transfer source address	Increment, decrement, or fixed*1	• When the MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When the MRB.DTS bit is 1 SAR register initial value.
DAR	Transfer destination address	Increment, decrement, or fixed*1	• When the MRB.DTS bit is 0 DAR register initial value • When the MRB.DTS bit is 1 Increment, decrement, or fixed.*1
CRAH	Holds transfer counter	CRAH	CRAH
CRAL	Transfer counter A	CRAL - 1	CRAH
CRB	Transfer counter B	Not updated	Not updated

Note 1. Write-back is skipped in address-fixed mode.

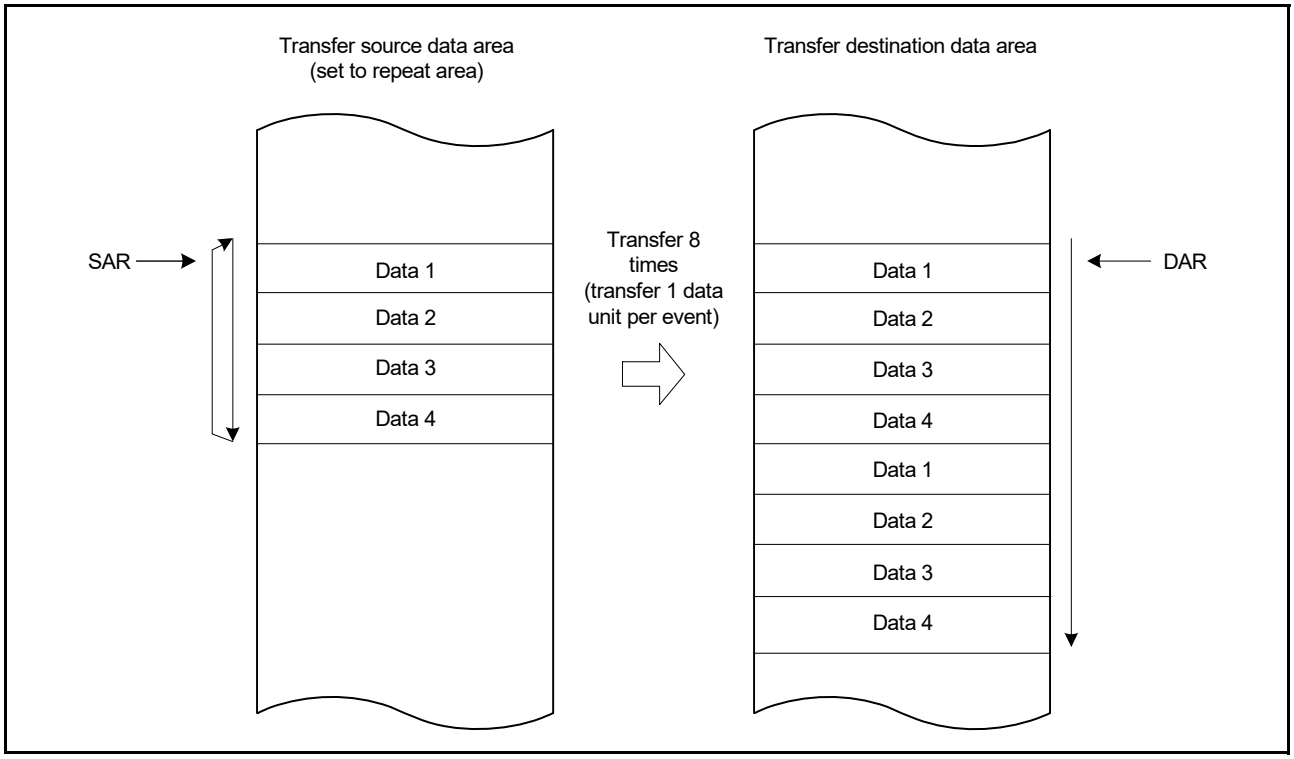


Figure 17.6 Memory map of repeat transfer mode when transfer source is a repeat area (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRAH = 04h)

17.4.5 Block Transfer Mode

Block transfer mode allows single-block data transfer on a single activation source. Transfer source or transfer destination for the block area must be specified in the MRB.DTS bit. The block size can be set from 1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes). When transfer of the specified block completes, the initial values of the block size counter CRAL and the address register (the SAR register when the MRB.DTS bit = 1 or the DAR register when the DTS bit = 0) specified in the block area are restored. The other address register is incremented or decremented continuously or remains unchanged.

The transfer count (block count) can be set from 1 to 65536. This mode enables an interrupt request to the CPU to be generated at the end of the specified-count block transfer.

Table 17.7 lists register functions in block transfer mode, and Figure 17.7 shows the memory map for block transfer mode.

Table 17.7 Register functions in block transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	• When MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When MRB.DTS bit is 1 SAR register initial value.
DAR	Transfer destination address	• When MRB.DTS bit is 0 DAR register initial value • When MRB.DTS bit is 1 Increment, decrement, or fixed.*1
CRAH	Holds the block size	CRAH
CRAL	Block size counter	CRAH
CRB	Block transfer counter	CRB - 1

Note 1. Write-back is skipped in address-fixed mode.

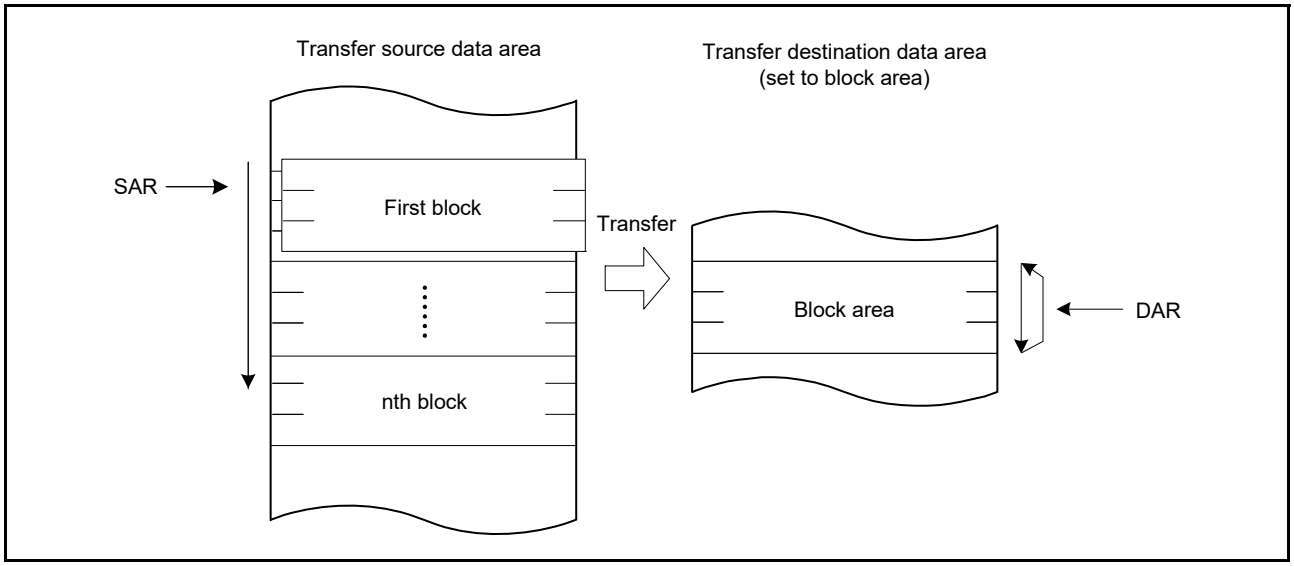


Figure 17.7 Memory map of block transfer mode

17.4.6 Chain Transfer

Setting the MRB.CHNE bit to 1 allows chain transfer to be performed continuously on a single activation source. If MRB.CHNE is set to 1 and CHNS to 0, an interrupt request to the CPU is not generated on completion of the specified number of transfer rounds or by setting the MRB.DISEL bit to 1. An interrupt request is sent to the CPU each time DTC data transfer is performed. Data transfer has no effect on the ICU.IELSRn.IR bit of the activation source.

The SAR, DAR, CRA, CRB, MRA, and MRB registers can be set independently of each other to define the data transfer. Figure 17.8 shows a chain transfer operation.

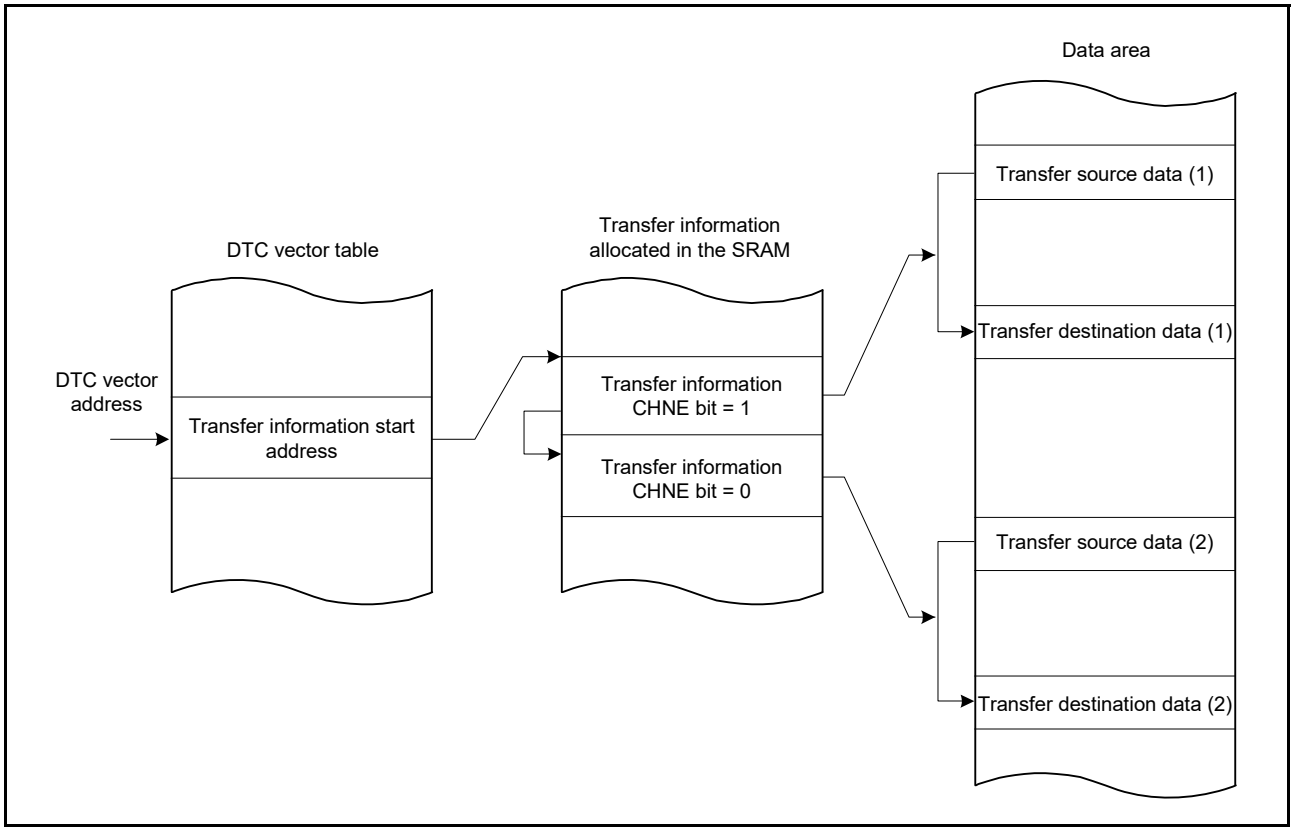


Figure 17.8 Chain transfer operation

Writing 1 to the MRB.CHNE and CHNS bits enables chain transfer to be performed only after completion of the specified data transfer. In repeat transfer mode, chain transfer is performed after completion of the specified data transfer. For details on chain transfer conditions, see Table 17.3, Chain transfer conditions.

17.4.7 Operation Timing

Figure 17.9 to Figure 17.12 are timing diagrams that show the minimum number of execution cycles.

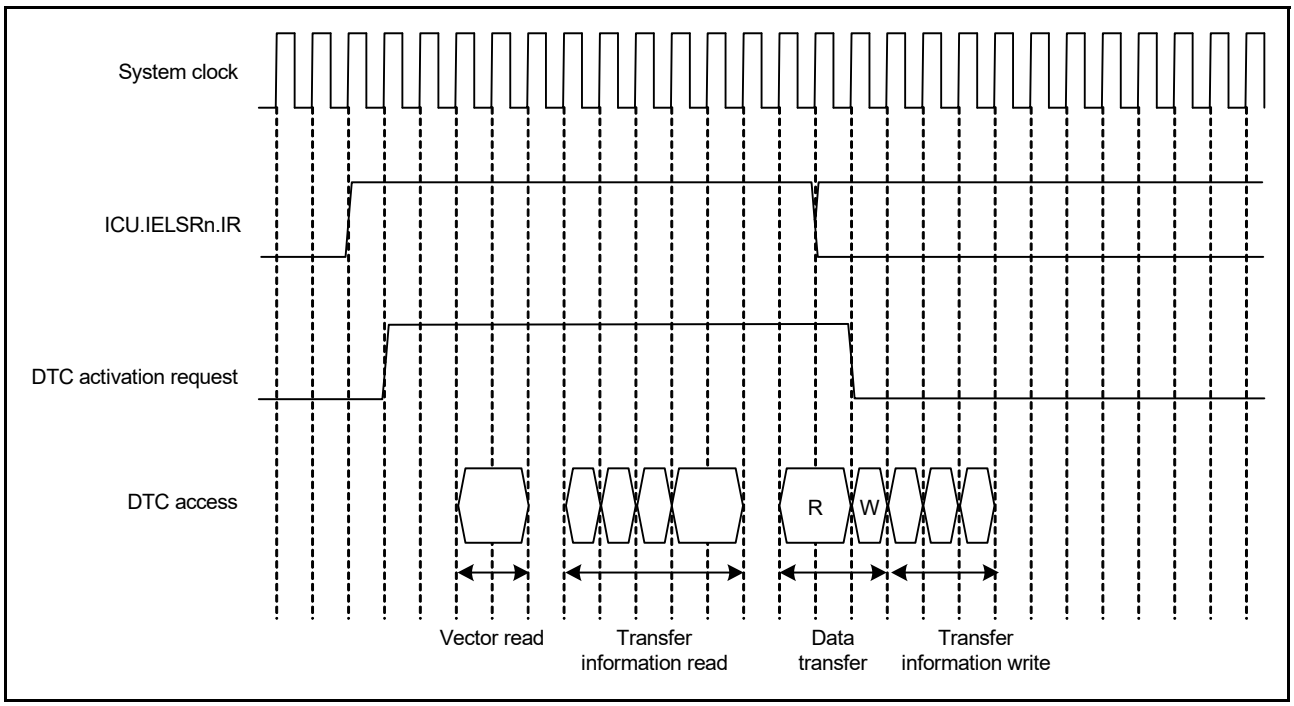


Figure 17.9 Example 1 of DTC operation timing in normal transfer and repeat transfer modes

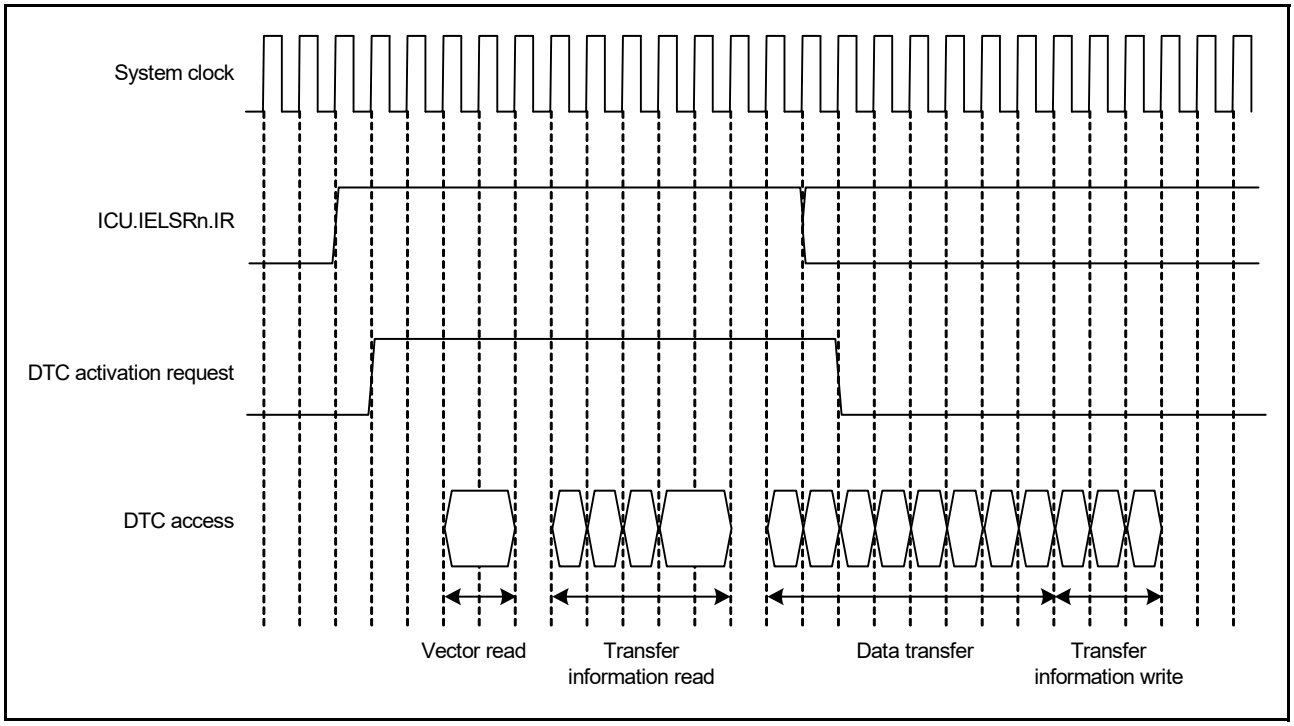


Figure 17.10 Example 2 of DTC operation timing in block transfer mode when the block size = 4

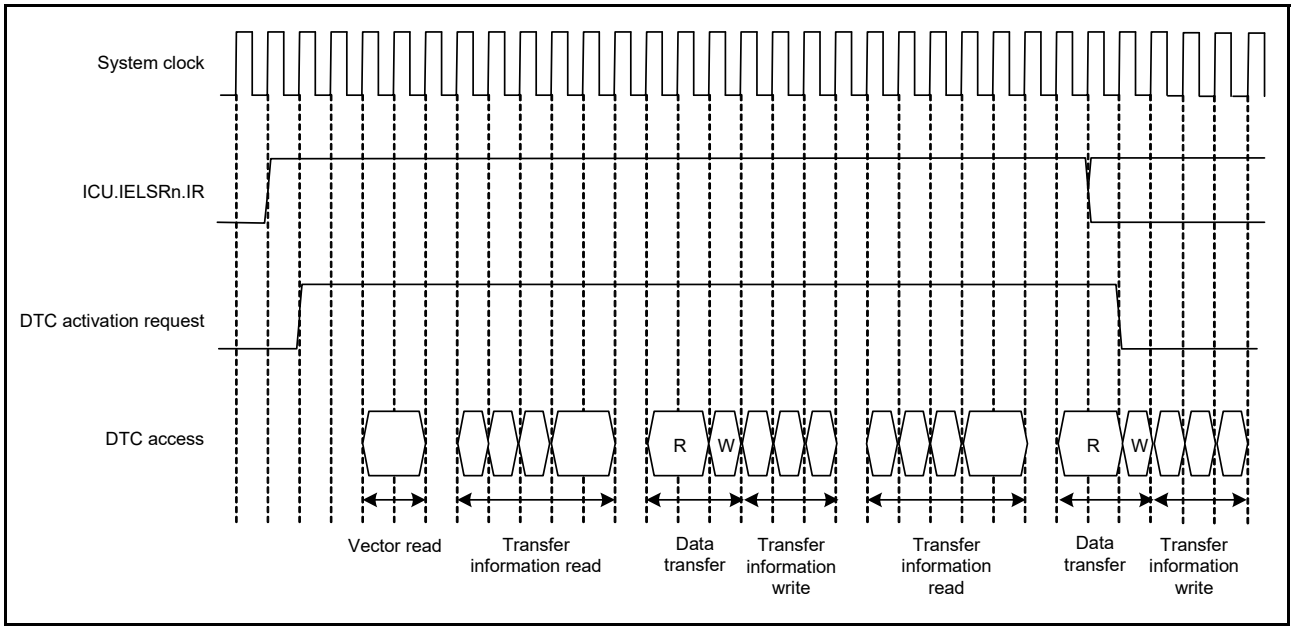
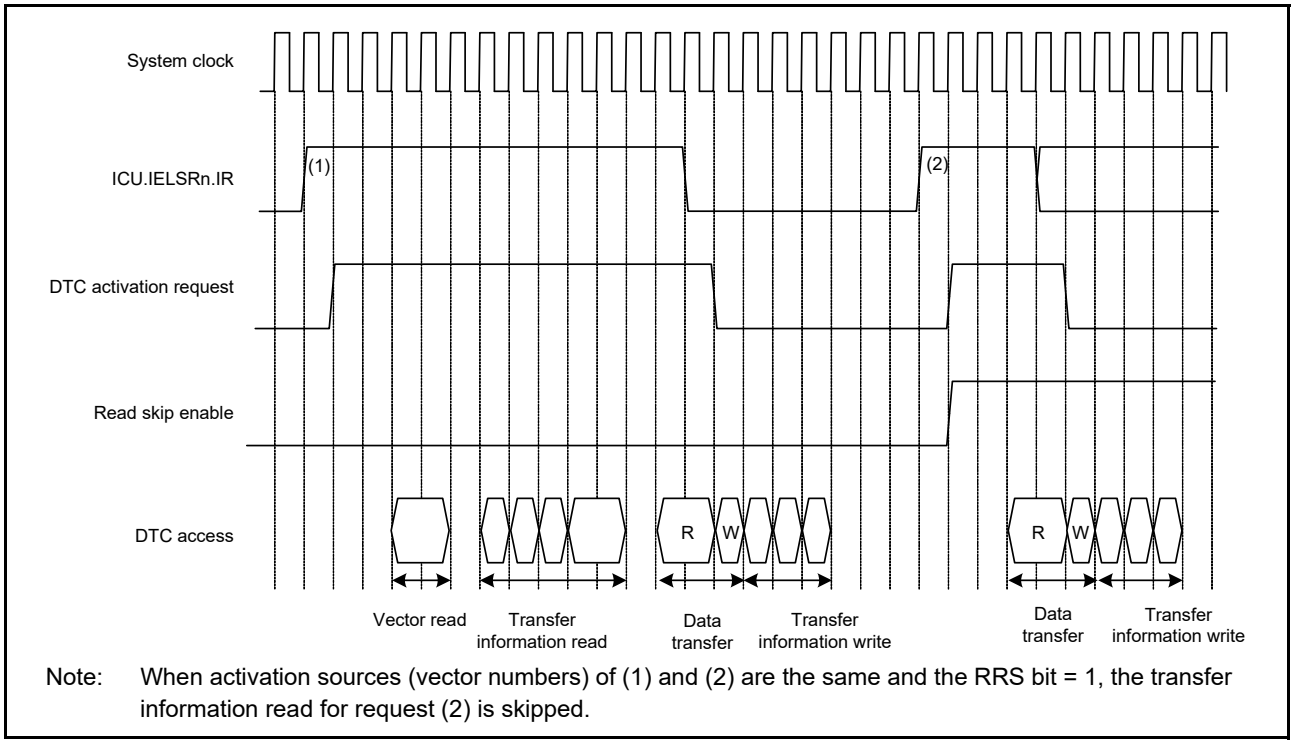


Figure 17.11 Example 3 of DTC operation timing for chain transfer



Note: When activation sources (vector numbers) of (1) and (2) are the same and the RRS bit = 1, the transfer information read for request (2) is skipped.

Figure 17.12 Example of operation when a transfer information read is skipped, with the vector, transfer information, and transfer destination data on the SRAM, and the transfer source data on the peripheral module

17.4.8 Execution Cycles of DTC

Table 17.8 lists the execution cycles of single data transfer of the DTC.

For the order of the execution states, see section 17.4.7, Operation Timing.

Table 17.8 Execution cycles of DTC

Transfer mode	Vector read		Transfer information read		Transfer information write			Data transfer		Internal operation	
								Read	Write		
Normal	Cv + Cs1 + 1	0*1	4 × (Ci + Cs1) + 1	0*1	3 × (Ci + Cs1) + 1*2	2 × (Ci + Cs1) + 1*3	(Ci + Cs1)*4	Cr + Cs2 + 1	Cw + Cs2 + 1	2	0*1
Repeat								Cr + Cs2 + 1	Cw + Cs2 + 1		
Block*5								P × (Cr + Cs2)	P × (Cw + Cs2)		

Note 1. When transfer information read is skipped.
Note 2. When neither SAR nor DAR is set to address-fixed mode.
Note 3. When SAR or DAR is set to address-fixed mode.
Note 4. When SAR and DAR are set to address-fixed mode.
Note 5. When the block size is 2 or more. If the block size is 1, the cycle number for normal transfer is applied.

P: Block size (initial settings of CRAH and CRAL)
Cv: Cycles for access to vector transfer information storage destination
Ci: Cycles for access to transfer information storage destination address
Cr: Cycles for access to data read destination
Cw: Cycles for access to data write destination
Cs1: When accessing SRAMHS: 2 cycles.
When accessing elsewhere: 0 cycle.
When a slave bus change by a read/write data transfer, add 1 more cycle.
Cs2: When accessing SRAMHS and peripheral modules related to system control: 2 cycles.
When accessing elsewhere: 0 cycle.
When a slave bus change by a read/write data transfer, add 1 more cycle.
The unit is system clock (ICLK) for + 1 in the Vector read, Transfer information read, and Data transfer read columns and 2 in the Internal operation column.
Cv, Ci, Cr, and Cw vary depending on the corresponding access destination. For the number of cycles for respective access destinations, see section 40, SRAM and section 41, Flash Memory.
The frequency ratio of the system clock and peripheral clock is also taken into consideration.
The DTC response time is the time from when the DTC activation source is detected until DTC transfer starts.
This table does not include the time until DTC data transfer starts after the DTC activation source becomes active.

17.4.9 DTC Bus Mastership Release Timing

The DTC does not release bus mastership during transfer information reads. Before the transfer information is read or written, the bus is arbitrated according to the priority determined by the bus master arbitrator. For bus arbitration, see section 14, Buses.

17.5 DTC Setting Procedure

Before using the DTC, set the DTC Vector Base Register (DTCVBR). Figure 17.13 shows the procedure for setting the DTC.

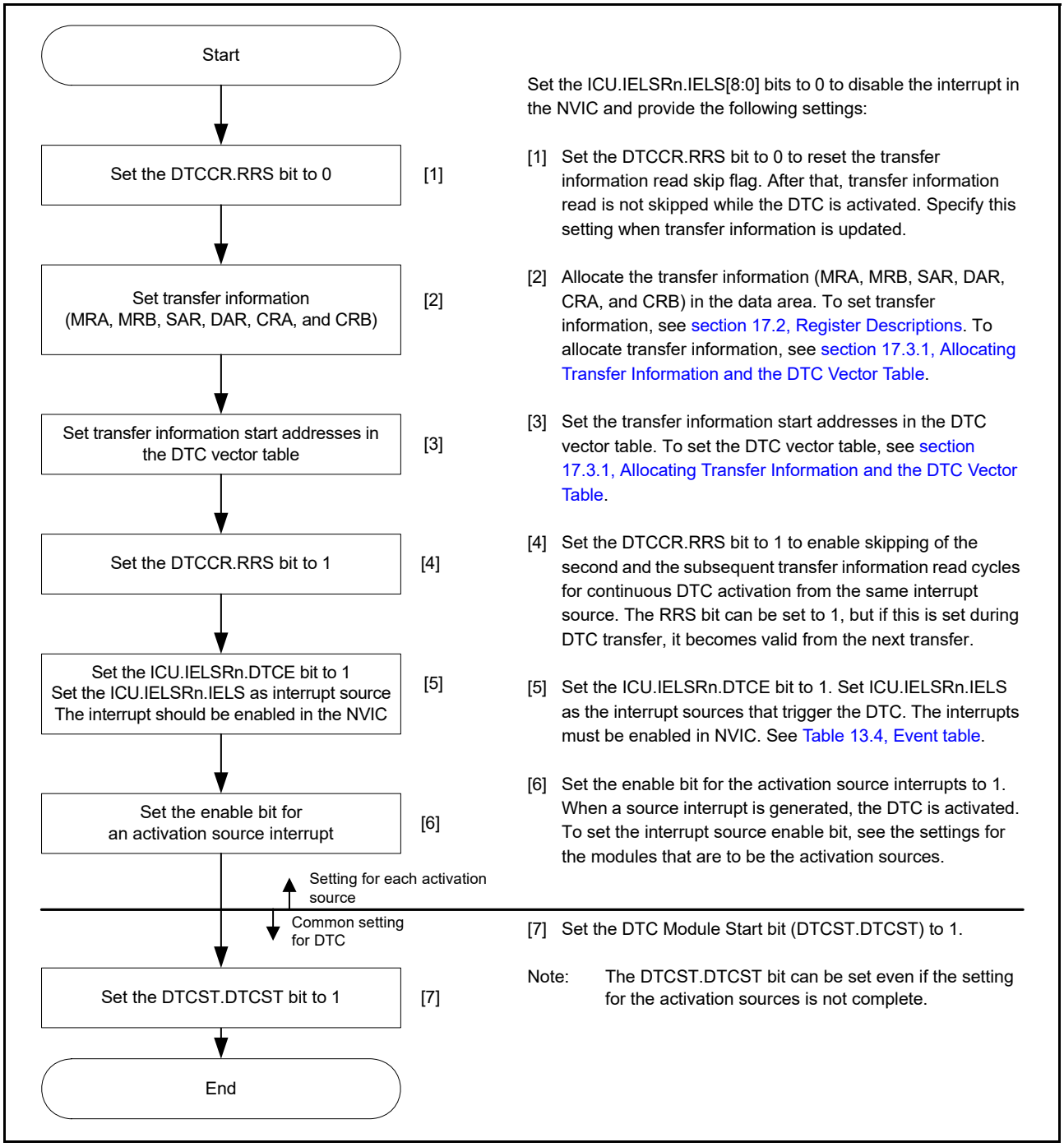


Figure 17.13 DTC setting procedure

17.6 Examples of DTC Usage

17.6.1 Normal Transfer

This section provides an example of DTC usage and its application when receiving 128 bytes of data from an SCI.

(1) Transfer information settings

In the MRA register, select a fixed source address (MRA.SM[1:0] = 00b), normal transfer mode (MRA.MD[1:0] = 00b), and byte-sized transfer (MRA.SZ[1:0] = 00b). In the MRB register, specify incrementation of the destination address (MRB.DM[1:0] = 10b) and single data transfer by a single interrupt (MRB.CHNE = 0 and MRB.DISEL = 0). The MRB.DTS bit can be set to any value. Set the RDR register address of the SCI in the SAR register, the start address of the SRAM area for data storage in the DAR register, and 128 (0080h) in the CRA register. The CRB register can be set to any value.

(2) DTC vector table settings

The start address of the transfer information for the RXI interrupt is set in the vector table for the DTC.

(3) ICU settings and DTC module activation

Set the ICU.IELSRn.DTCE bit to 1 and set ICU.IELSRn.IELS as the SCI interrupt. The interrupt must be enabled in the NVIC. Set the DTCST.DTCST bit to 1.

(4) SCI settings

Enable the RXI interrupt by setting the SCR.RIE bit in the SCI to 1. If a reception error occurs during the SCI receive operation, reception stops. To manage this, use settings that allow the CPU to accept receive error interrupts.

(5) DTC transfer

Each time a reception of 1 byte by the SCI is complete, an RXI interrupt is generated to activate the DTC. The DTC transfers the received byte from the RDR of the SCI to the SRAM, after which the DAR register is incremented and the CRA register is decremented.

(6) Interrupt handling

After 128 rounds of data transfer are complete and the value in the CRA register becomes 0, an RXI interrupt request is generated for the CPU. Complete the process in the handling routine for this interrupt.

17.6.2 Chain Transfer

This section provides an example of chain transfer by the DTC and describes its use in the output of pulses by the General PWM Timer (GPT). You can use chain transfer to transfer PWM timer compare data and change the period of the PWM timer for GPT.

For the first of the chain transfers, normal transfer mode is specified for transfer to the GPT32m.GTCCRC register (m = EH0 to EH3, E4 to E7, 8 to 12). For the second transfer, normal transfer mode is specified for transfer to the GPT32m.GTCCRE register. For the third transfer, normal transfer mode is specified for transfer to the GPT32m.GTPBR register. This is because clearing of the activation source and generation of an interrupt on completion of the specified number of transfers are restricted to the third of the chain transfers, that is, transfer while MRB.CHNE = 0.

The following example shows how to use the counter overflow interrupt with a GPT32EH0.GTPR register as an activating source for the DTC.

(1) First transfer information settings

Set up transfer to the GPT32EH0.GTCCRC register:

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1 and MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT32EH0.GTCCRC register.

6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(2) Second transfer information settings

Set up transfer to the GPT32EH0.GTCCRE register:

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1 and MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT32EH0.GTCCRE register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(3) Third transfer information settings

Set up transfer to the GPT32EH0.GTPBR register:

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up single data transfer per interrupt (MRB.CHNE = 0, MRB.DISEL = 0). The MRB.DTS bit can be set to any value.
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT32EH0.GTPBR register.
6. Set the CRA register to the size of the data table. The CRB register can be set to any value.

(4) Transfer information assignment

Place the transfer information for use in the transfer to GPT32EH0.GTPBR immediately after the transfer control information for use in the GPT32EH0.GTCCRC and GPT32EH0.GTCCRE registers.

(5) DTC vector table

In the DTC vector table, set the address where the transfer control information for use in transfer to the GPT32EH0.GTCCRC and GPT32EH0.GTCCRE registers starts.

(6) ICU setting and DTC module activation

1. Set the ICU.IELSRn.DTCE bit associated with the GPT32EH0 counter overflow interrupt.
2. Set the ICU.IELSRn.IELS[8:0] bits to 182 (B6h) for the GPT32EH0 counter overflow.
3. Set the DTCST.DTCST bit to 1.

(7) GPT settings

1. Set the GPT32EH0.GTIOR register so that the GTCCRA and GTCCRB registers operate as output compare registers.
2. Set the default PWM timer compare values in the GPT32EH0.GTCCRA and GPT32EH0.GTCCRB registers and the next PWM timer compare values in the GPT32EH0.GTCCRC and GPT32EH0.GTCCRE registers.
3. Set the default PWM timer period values in the GPT32EH0.GTPR register and the next PWM timer period values in the GPT32EH0.GTPBR register.
4. Set 1 to the output bit in PmnPFS.PDR, and set 00011b to the Peripheral Select bits in PmnPFS.PSEL[4:0].

(8) GPT activation

Set the GPT32EH0.GTSTR.CSTRT bits to 1 to start the GPT32EH0.GTCNT counter.

(9) DTC transfer

Each time a GPT32EH0 counter overflow is generated with the GPT32EH0.GTPR register, the next PWM timer compare values are transferred to the GPT32EH0.GTCCRC and GPT32EH0.GTCCRE registers. The setting for the next PWM timer period is transferred to the GPT32EH0.GTPBR register.

(10) Interrupt handling

After the specified rounds of data transfer are complete, for example when the value in the CRA register for GPT transfer becomes 0, a GPT counter overflow interrupt request is issued for the CPU. Complete the process for this interrupt in the handling routine.

17.6.3 Chain Transfer when Counter = 0

The second data transfer is performed only when the transfer counter is set to 0 in the first data transfer, and the first data transfer information is repeatedly changed in the second transfer. Chain transfer enables transfers to be repeated 256 times or more.

The following procedure shows an example of configuring a 128-KB input buffer, where the input buffer is set so that its lower address starts with 0000h. Figure 17.14 shows a chain transfer when the counter = 0.

1. Set the normal transfer mode to input data for the first data transfer. Set the following:
   a. Transfer source address = fixed.
   b. CRA register = 0000h (65536) times.
   c. MRB.CHNE bit = 1 (chain transfer is enabled).
   d. MRB.CHNS bit = 1 (chain transfer is performed only when the transfer counter is 0).
   e. MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
2. Prepare the upper 8-bit address of the start address at every 65536 times of the transfer destination address for the first data transfer in different area such as the flash. For example, when setting the input buffer to 20 0000h to 21 FFFFh, prepare 21h and 20h.
3. For the second data transfer:
   a. Set the repeat transfer mode (with the source as the repeat area) to reset the transfer destination address of the first data transfer.
   b. Specify the upper 8 bits of the DAR register in the first transfer information area for the transfer destination.
   c. Set the MRB.CHNE bit = 0 (chain transfer is disabled).
   d. Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   e. When setting the input buffer to 20 0000h to 21 FFFFh, also set the transfer counter to 2.
4. The first data transfer is performed by an interrupt 65536 times. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 21h. The lower 16 bits of the transfer destination address and the transfer counter of the first data transfer becomes 0000h.
5. In succession, the first data transfer is performed by an interrupt 65536 times as specified for the first data transfer. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 20h. The lower 16 bits of the transfer destination address and the transfer counter of the first data transfer becomes 0000h.
6. Steps 4 and 5 are repeated indefinitely. Because the second data transfer is in repeat transfer mode, no interrupt request to the CPU is generated.

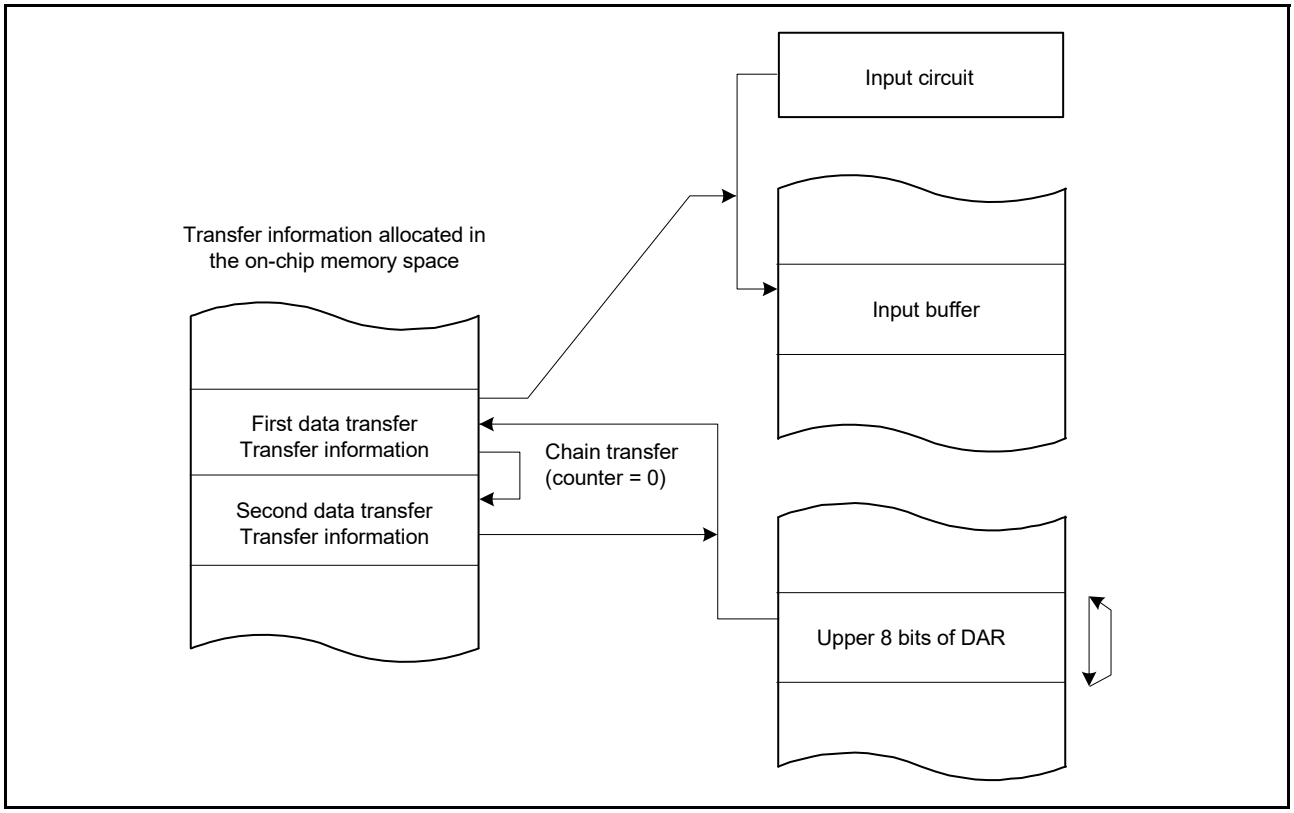


Figure 17.14 Chain transfer when counter = 0

17.7 Interrupt Sources

When the DTC completes data transfer of the specified count or when data transfer with MRB.DISEL set to 1 is complete, a DTC activation source generates an interrupt to the CPU. Interrupts to the CPU are controlled according to the settings in the NVIC and ICU.IELSRn.IELS[8:0] bits. See section 13, Interrupt Controller Unit (ICU).

The DTC prioritizes activation sources by granting the smaller interrupt vector numbers higher priority. The priority of interrupts to the CPU is determined by the NVIC priority.

17.8 Event Link

The DTC can produce an event link request on completion of one transfer request.

17.9 Snooze Control Interface

To return to Software Standby mode from Snooze mode through the DTC, set SYSTEM.SNZEDCR.DTCZRED or SYSTEM.SNZEDCR.DTCNZRED to 1. See section 11.8.3, Returning to Software Standby Mode.

SYSTEM.SNZEDCR.DTCZRED enables or disables a snooze end request on completion of the last DTC transmission, detected on DTC transmission completion when CRA and CRB are 0.

SYSTEM.SNZEDCR.DTCNZRED enables or disables a snooze end request on a not last DTC transmission completion (CRA and CRB are not 0), detected on DTC transmission completion when CRA and CRB are not 0.

17.10 Module-Stop Function

Before transitioning to the module-stop function, Software Standby mode without a Snooze mode transition, or Deep Software Standby mode, set the DTCST.DTCST bit to 0, then perform the operations described in the following sections. The DTC is available in Snooze mode by setting LPW.SNZCR.SNZDTCEN to 1. See section 11, Low Power Modes.

(1) Module-stop function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DTC. If the DTC transfer is in progress at the time 1 is written to the MSTPCRA.MSTPA22 bit, the transition to the module-stop state proceeds after

DTC transfer ends. When the MSTPCRA.MSTPA22 bit is 1, accessing the DTC registers is prohibited. Writing 0 to the MSTPCRA.MSTPA22 bit releases the DTC from the module-stop state.

(2) Software Standby and Deep Software Standby modes

Use the settings described in section 11.7.1, Transitioning to Software Standby Mode, or section 11.9.1, Transitioning to Deep Software Standby Mode.

If DTC transfer operations are in progress when the WFI instruction is executed, the transition to Software Standby mode or Deep Software Standby mode follows the completion of the DTC transfer.

When the snooze control circuit receives a snooze request in Software Standby mode, the MCU transfers to Snooze mode. See section 11.8.1, Transitioning to Snooze Mode. DTC operation in Snooze mode can be selected in the SYSTEM.SNZCR.SNZDTCEN bit. If DTC operation is enabled in Snooze mode, before transitioning to Software Standby mode, set the DTCST.DTCST bit to 1. To return to Software Standby mode through the DTC, set SYSTEM.SNZEDCR.DTCZRED or SYSTEM.SNZEDCR.DTCNZRED to 1. See section 11.8.3, Returning to Software Standby Mode. The DTC activation request from the ICU is stopped during Software Standby mode but not during Snooze mode.

(3) Notes on the module-stop function

For the WFI instruction and the register setting procedure, see section 11, Low Power Modes.

To perform a DTC transfer after returning from a low power mode without a Snooze mode transition, set the DTCST.DTCST bit to 1 again.

To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DTC activation request, specify the CPU as the interrupt request destination as described in section 13.4.2, Selecting Interrupt Request Destinations, then execute a WFI instruction. If DTC operation is enabled in Snooze mode, do not use the module-stop function of the DTC.

17.11 Usage Notes

17.11.1 Transfer Information Start Address

You must set multiples of 4 for the transfer information start addresses in the vector table. Otherwise, such addresses are accessed with their lowest 2 bits regarded as 00b.

18. Event Link Controller (ELC)

18.1 Overview

The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 18.1 lists the ELC specifications and Figure 18.1 shows a block diagram.

Table 18.1 ELC specifications

Parameter	Specifications
Event link function	229 types of event signals can be directly connected to modules. The ELC can generate an ELC event signal, and events that activate the DTC.
Module-stop function	Module-stop state can be set

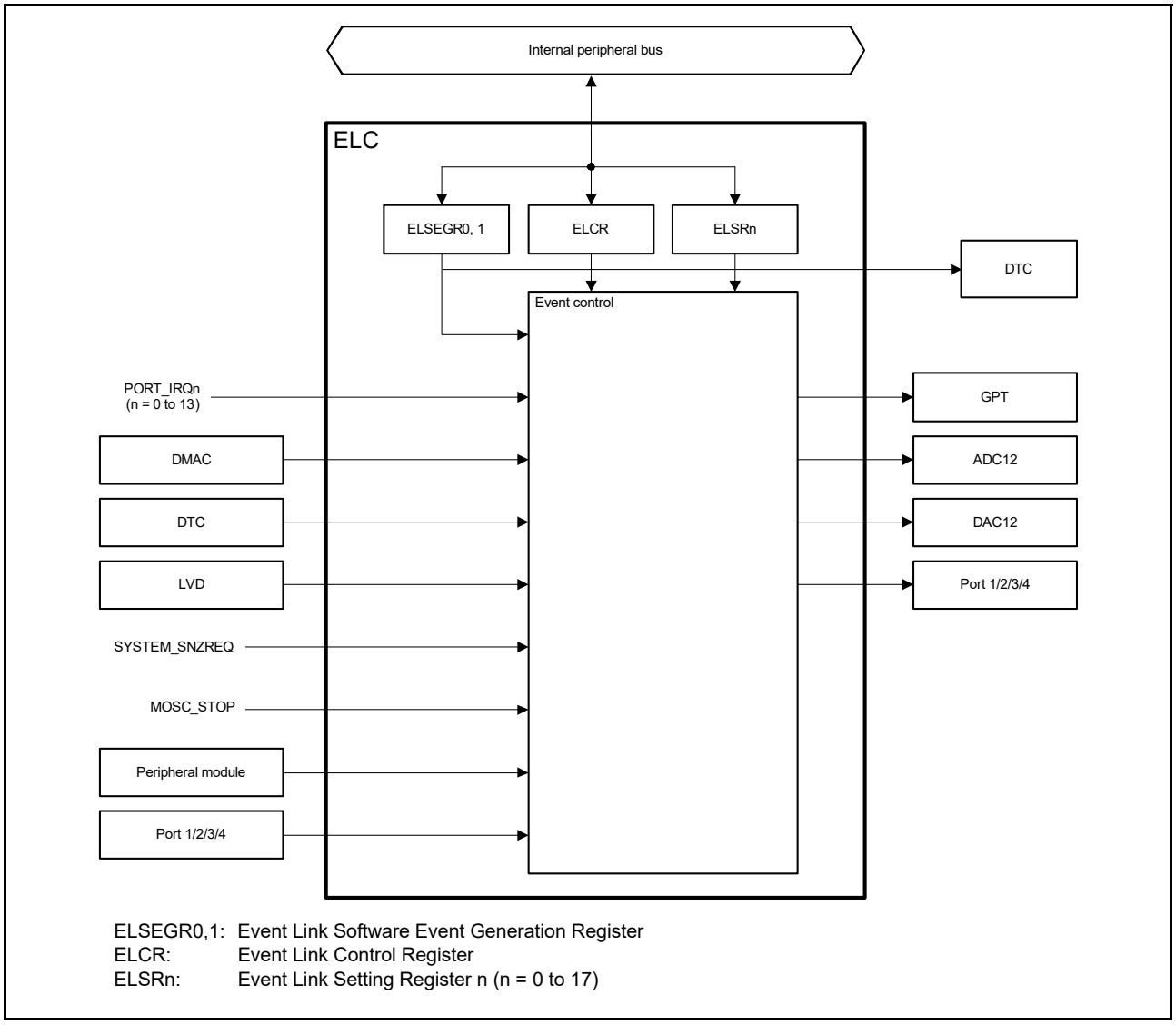


Figure 18.1 ELC block diagram

18.2 Register Descriptions

18.2.1 Event Link Controller Register (ELCR)

Address(es): ELC.ELCR 4004 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	ELCON	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ELCON	All Event Link Enable	0: ELC function disabled 1: ELC function enabled.	R/W

The ELCR register controls the ELC operation.

18.2.2 Event Link Software Event Generation Register n (ELSEGRn) (n = 0, 1)

Address(es): ELC.ELSEGR0 4004 1002h, ELC.ELSEGR1 4004 1004h

	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	—	—	—	—	—	SEG
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SEG	Software Event Generation	0: Normal operation 1: Software event is generated.	W
b5 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	WE	SEG Bit Write Enable	0: Writes to SEG bit disabled 1: Writes to SEG bit enabled.	R/W
b7	WI	ELSEGR Register Write Disable	0: Writes to ELSEGR register enabled 1: Writes to ELSEGR register disabled.	W

SEG bit (Software Event Generation)

When 1 is written to the SEG bit while the WE bit is 1, a software event is generated. This bit is read as 0. Even when 1 is written to this bit, data is not stored. The WE bit must be set to 1 before writing to this bit.

A software event can trigger a linked DTC event.

WE bit (SEG Bit Write Enable)

The SEG bit can only be written to when the WE bit is 1. Clear the WI bit to 0 before writing to this bit.

[Setting condition]

- If 1 is written to this bit while the WI bit is 0, this bit becomes 1.

[Clearing condition]

- If 0 is written to this bit while the WI bit is 0, this bit becomes 0.

WI bit (ELSEGR Register Write Disable)

The ELSEGR register can only be written to when the write value to the WI bit is 0. This bit is read as 1. Before setting the WE or SEG bit, the WI bit must be set to 0.

18.2.3 Event Link Setting Register n (ELSRn) (n = 0 to 17)

Address(es): ELC.ELSR0 4004 1010h, ELC.ELSR1 4004 1014h, ELC.ELSR2 4004 1018h, ELC.ELSR3 4004 101Ch, ELC.ELSR4 4004 1020h, ELC.ELSR5 4004 1024h, ELC.ELSR6 4004 1028h, ELC.ELSR7 4004 102Ch, ELC.ELSR8 4004 1030h, ELC.ELSR9 4004 1034h, ELC.ELSR10 4004 1038h, ELC.ELSR11 4004 103Ch, ELC.ELSR12 4004 1040h, ELC.ELSR13 4004 1044h, ELC.ELSR14 4004 1048h, ELC.ELSR15 4004 104Ch, ELC.ELSR16 4004 1050h, ELC.ELSR17 4004 1054h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	ELS[8:0]	Event Link Select	b8 b0 000000000: Event output disabled for the associated peripheral module 000000001 to 111000101b: Number setting for the event signal to be linked. Other settings are prohibited.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ELSRn register specifies an event signal to be linked to each peripheral module. Table 18.2 shows the association between the ELSRn registers and the peripheral modules. Table 18.3 shows the association between the event signal names set in the ELSRn registers and the signal numbers.

Table 18.2 Association between the ELSRn registers and peripheral functions

Register name	Peripheral function (module)	Event name
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR8	ADC12A0	ELC_AD00
ELSR9	ADC12B0	ELC_AD01
ELSR10	ADC12A1	ELC_AD10
ELSR11	ADC12B1	ELC_AD11
ELSR12	DAC12 channel 0	ELC_DA0
ELSR13	DAC12 channel 1	ELC_DA1
ELSR14	PORT 1	ELC_PORT1
ELSR15	PORT 2	ELC_PORT2
ELSR16	PORT 3	ELC_PORT3
ELSR17	PORT 4	ELC_PORT4

Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (1 of 6)

Event number	Interrupt request source	Name	Description
001h	Port	PORT_IRQ0*1	External pin interrupt 0
002h		PORT_IRQ1*1	External pin interrupt 1
003h		PORT_IRQ2*1	External pin interrupt 2
004h		PORT_IRQ3*1	External pin interrupt 3
005h		PORT_IRQ4*1	External pin interrupt 4
006h		PORT_IRQ5*1	External pin interrupt 5
007h		PORT_IRQ6*1	External pin interrupt 6
008h		PORT_IRQ7*1	External pin interrupt 7
009h		PORT_IRQ8*1	External pin interrupt 8
00Ah		PORT_IRQ9*1	External pin interrupt 9
00Bh		PORT_IRQ10*1	External pin interrupt 10
00Ch		PORT_IRQ11*1	External pin interrupt 11
00Dh		PORT_IRQ12*1	External pin interrupt 12
00Eh		PORT_IRQ13*1	External pin interrupt 13
020h	DMAC0	DMAC0_INT	DMAC transfer end 0
021h	DMAC1	DMAC1_INT	DMAC transfer end 1
022h	DMAC2	DMAC2_INT	DMAC transfer end 2
023h	DMAC3	DMAC3_INT	DMAC transfer end 3
024h	DMAC4	DMAC4_INT	DMAC transfer end 4
025h	DMAC5	DMAC5_INT	DMAC transfer end 5
026h	DMAC6	DMAC6_INT	DMAC transfer end 6
027h	DMAC7	DMAC7_INT	DMAC transfer end 7
02Ah	DTC	DTC_DTCEND*3	DTC transfer end
038h	LVD	LVD_LVD1	Voltage monitor 1 interrupt
039h		LVD_LVD2	Voltage monitor 2 interrupt
03Bh	MOSC	MOSC_STOP	Main clock oscillation stop
03Ch	Low power mode	SYSTEM_SNZREQ*2, *3	Snooze entry
040h	AGT0	AGT0_AGTI	AGT interrupt
041h		AGT0_AGTCMAI	Compare match A
042h		AGT0_AGTCMBI	Compare match B
043h	AGT1	AGT1_AGTI	AGT interrupt
044h		AGT1_AGTCMAI	Compare match A
045h		AGT1_AGTCMBI	Compare match B
046h	IWDT	IWDT_NMIUNDF	IWDT underflow
047h	WDT	WDT_NMIUNDF	WDT underflow
04Bh	ADC120	ADC120_ADI	A/D scan end interrupt
04Fh		ADC120_WCMPM*3	Compare match
050h		ADC120_WCMPUM*3	Compare mismatch
051h	ADC121	ADC121_ADI	A/D scan end interrupt
055h		ADC121_WCMPM*3	Compare match
056h		ADC121_WCMPUM*3	Compare mismatch

Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (2 of 6)

Event number	Interrupt request source	Name	Description
057h	ACMPHS	ACMP_HS0*1	High-Speed Analog Comparator interrupt 0
058h		ACMP_HS1*1	High-Speed Analog Comparator interrupt 1
059h		ACMP_HS2*1	High-Speed Analog Comparator interrupt 2
05Ah		ACMP_HS3*1	High-Speed Analog Comparator interrupt 3
05Bh		ACMP_HS4*1	High-Speed Analog Comparator interrupt 4
05Ch		ACMP_HS5*1	High-Speed Analog Comparator interrupt 5
063h	IIC0	IIC0_RXI	Receive data full
064h		IIC0_TXI	Transmit data empty
065h		IIC0_TEI	Transmit end
066h		IIC0_EEI	Transfer error
068h	IIC1	IIC1_RXI	Receive data full
069h		IIC1_TXI	Transmit data empty
06Ah		IIC1_TEI	Transmit end
06Bh		IIC1_EEI	Transfer error
086h	DOC	DOC_DOPCI*3	Data Operation Circuit interrupt
094h	I/O port	IOPORT_GROUP1	Port 1 event
095h		IOPORT_GROUP2	Port 2 event
096h		IOPORT_GROUP3	Port 3 event
097h		IOPORT_GROUP4	Port 4 event
098h	ELC	ELC_SWEVT0	Software event 0
099h		ELC_SWEVT1	Software event 1
0B0h	GPT32EH0	GPT0_CCMPA	Compare match A
0B1h		GPT0_CCMPB	Compare match B
0B2h		GPT0_CMPC	Compare match C
0B3h		GPT0_CMPD	Compare match D
0B4h		GPT0_CMPE	Compare match E
0B5h		GPT0_CMPF	Compare match F
0B6h		GPT0_OVF	Overflow
0B7h		GPT0_UDF	Underflow
0B8h		GPT0_ADTRGA	A/D converter start request A
0B9h		GPT0_ADTRGB	A/D converter start request B
0BAh	GPT32EH1	GPT1_CCMPA	Compare match A
0BBh		GPT1_CCMPB	Compare match B
0BCh		GPT1_CMPC	Compare match C
0BDh		GPT1_CMPD	Compare match D
0BEh		GPT1_CMPE	Compare match E
0BFh		GPT1_CMPF	Compare match F
0C0h		GPT1_OVF	Overflow
0C1h		GPT1_UDF	Underflow
0C2h		GPT1_ADTRGA	A/D converter start request A
0C3h		GPT1_ADTRGB	A/D converter start request B

Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (3 of 6)

Event number	Interrupt request source	Name	Description
0C4h	GPT32EH2	GPT2_CCMPA	Compare match A
0C5h		GPT2_CCMPB	Compare match B
0C6h		GPT2_CMPC	Compare match C
0C7h		GPT2_CMPD	Compare match D
0C8h		GPT2_CMPE	Compare match E
0C9h		GPT2_CMPF	Compare match F
0CAh		GPT2_OVF	Overflow
0CBh		GPT2_UDF	Underflow
0CCh		GPT2_ADTRGA	A/D converter start request A
0CDh		GPT2_ADTRGB	A/D converter start request B
0CEh	GPT32EH3	GPT3_CCMPA	Compare match A
0CFh		GPT3_CCMPB	Compare match B
0D0h		GPT3_CMPC	Compare match C
0D1h		GPT3_CMPD	Compare match D
0D2h		GPT3_CMPE	Compare match E
0D3h		GPT3_CMPF	Compare match F
0D4h		GPT3_OVF	Overflow
0D5h		GPT3_UDF	Underflow
0D6h		GPT3_ADTRGA	A/D converter start request A
0D7h		GPT3_ADTRGB	A/D converter start request B
0D8h	GPT32E4	GPT4_CCMPA	Compare match A
0D9h		GPT4_CCMPB	Compare match B
0DAh		GPT4_CMPC	Compare match C
0DBh		GPT4_CMPD	Compare match D
0DCh		GPT4_CMPE	Compare match E
0DDh		GPT4_CMPF	Compare match F
0DEh		GPT4_OVF	Overflow
0DFh		GPT4_UDF	Underflow
0E0h		GPT4_ADTRGA	A/D converter start request A
0E1h		GPT4_ADTRGB	A/D converter start request B
0E2h	GPT32E5	GPT5_CCMPA	Compare match A
0E3h		GPT5_CCMPB	Compare match B
0E4h		GPT5_CMPC	Compare match C
0E5h		GPT5_CMPD	Compare match D
0E6h		GPT5_CMPE	Compare match E
0E7h		GPT5_CMPF	Compare match F
0E8h		GPT5_OVF	Overflow
0E9h		GPT5_UDF	Underflow
0EAh		GPT5_ADTRGA	A/D converter start request A
0EBh		GPT5_ADTRGB	A/D converter start request B

Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (4 of 6)

Event number	Interrupt request source	Name	Description
0ECh	GPT32E6	GPT6_CCMPA	Compare match A
0EDh		GPT6_CCMPB	Compare match B
0EEh		GPT6_CMPC	Compare match C
0EFh		GPT6_CMPD	Compare match D
0F0h		GPT6_CMPE	Compare match E
0F1h		GPT6_CMPF	Compare match F
0F2h		GPT6_OVF	Overflow
0F3h		GPT6_UDF	Underflow
0F4h		GPT6_ADTRGA	A/D converter start request A
0F5h		GPT6_ADTRGB	A/D converter start request B
0F6h	GPT32E7	GPT7_CCMPA	Compare match A
0F7h		GPT7_CCMPB	Compare match B
0F8h		GPT7_CMPC	Compare match C
0F9h		GPT7_CMPD	Compare match D
0FAh		GPT7_CMPE	Compare match E
0FBh		GPT7_CMPF	Compare match F
0FCh		GPT7_OVF	Overflow
0FDh		GPT7_UDF	Underflow
0FEh		GPT7_ADTRGA	A/D converter start request A
0FFh		GPT7_ADTRGB	A/D converter start request B
100h	GPT328	GPT8_CCMPA	Compare match A
101h		GPT8_CCMPB	Compare match B
102h		GPT8_CMPC	Compare match C
103h		GPT8_CMPD	Compare match D
104h		GPT8_CMPE	Compare match E
105h		GPT8_CMPF	Compare match F
106h		GPT8_OVF	Overflow
107h		GPT8_UDF	Underflow
10Ah	GPT329	GPT9_CCMPA	Compare match A
10Bh		GPT9_CCMPB	Compare match B
10Ch		GPT9_CMPC	Compare match C
10Dh		GPT9_CMPD	Compare match D
10Eh		GPT9_CMPE	Compare match E
10Fh		GPT9_CMPF	Compare match F
110h		GPT9_OVF	Overflow
111h		GPT9_UDF	Underflow
114h	GPT3210	GPT10_CCMPA	Compare match A
115h		GPT10_CCMPB	Compare match B
116h		GPT10_CMPC	Compare match C
117h		GPT10_CMPD	Compare match D
118h		GPT10_CMPE	Compare match E
119h		GPT10_CMPF	Compare match F
11Ah		GPT10_OVF	Overflow
11Bh		GPT10_UDF	Underflow

Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (5 of 6)

Event number	Interrupt request source	Name	Description
11Eh	GPT3211	GPT11_CCMPA	Compare match A
11Fh		GPT11_CCMPB	Compare match B
120h		GPT11_CMPC	Compare match C
121h		GPT11_CMPD	Compare match D
122h		GPT11_CMPE	Compare match E
123h		GPT11_CMPF	Compare match F
124h		GPT11_OVF	Overflow
125h		GPT11_UDF	Underflow
128h	GPT3212	GPT12_CCMPA	Compare match A
129h		GPT12_CCMPB	Compare match B
12Ah		GPT12_CMPC	Compare match C
12Bh		GPT12_CMPD	Compare match D
12Ch		GPT12_CMPE	Compare match E
12Dh		GPT12_CMPF	Compare match F
12Eh		GPT12_OVF	Overflow
12Fh		GPT12_UDF	Underflow
150h	GPT	GPT_UVWEDGE	UVW edge event
174h	SCI0	SCI0_RXI *4	Receive data full
175h		SCI0_TXI *4	Transmit data empty
176h		SCI0_TEI	Transmit end
177h		SCI0_ERI *4	Receive error
178h		SCI0_AM	Address match event
17Ah	SCI1	SCI1_RXI *4	Receive data full
17Bh		SCI1_TXI *4	Transmit data empty
17Ch		SCI1_TEI	Transmit end
17Dh		SCI1_ERI *4	Receive error
17Eh		SCI1_AM	Address match event
180h	SCI2	SCI2_RXI *4	Receive data full
181h		SCI2_TXI *4	Transmit data empty
182h		SCI2_TEI	Transmit end
183h		SCI2_ERI *4	Receive error
184h		SCI2_AM	Address match event
186h	SCI3	SCI3_RXI *4	Receive data full
187h		SCI3_TXI *4	Transmit data empty
188h		SCI3_TEI	Transmit end
189h		SCI3_ERI *4	Receive error
18Ah		SCI3_AM	Address match event
18Ch	SCI4	SCI4_RXI *4	Receive data full
18Dh		SCI4_TXI *4	Transmit data empty
18Eh		SCI4_TEI	Transmit end
18Fh		SCI4_ERI *4	Receive error
190h		SCI4_AM	Address match event

Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (6 of 6)

Event number	Interrupt request source	Name	Description
1A4h	SCI8	SCI8_RXI *4	Receive data full
1A5h		SCI8_TXI *4	Transmit data empty
1A6h		SCI8_TEI	Transmit end
1A7h		SCI8_ERI *4	Receive error
1A8h		SCI8_AM	Address match event
1AAh	SCI9	SCI9_RXI *4	Receive data full
1ABh		SCI9_TXI *4	Transmit data empty
1ACh		SCI9_TEI	Transmit end
1ADh		SCI9_ERI *4	Receive error
1AEh		SCI9_AM	Address match event
1BCh	SPI0	SPI0_SPRI	Receive data full
1BDh		SPI0_SPTI	Transmit data empty
1BEh		SPI0_SPII	Idle
1BFh		SPI0_SPEI	Receive error
1C0h		SPI0_SPTEND	Transmit end
1C1h	SPI1	SPI1_SPRI	Receive data full
1C2h		SPI1_SPTI	Transmit data empty
1C3h		SPI1_SPII	Idle
1C4h		SPI1_SPEI	Receive error
1C5h		SPI1_SPTEND	Transmit end

Note 1. Only pulse (edge detection) is supported.
Note 2. ELSR8 to ELSR11, and ELSR14 to ELSR17 can select this event.
Note 3. This event can occur in Snooze mode.
Note 4. This event is not supported in FIFO mode.

18.3 Operation

18.3.1 Relation between Interrupt Handling and Event Linking

Event number for an event link is the same as that for the associated interrupt source. For information on generating event signals, see the explanation in the chapter for each event source module.

18.3.2 Linking Events

When an event occurs and that event is already set as a trigger in the Event Link Setting Register (ELSRn), the associated module is activated. The operation of the module must be set up in advance. Table 18.4 lists the operations of modules when an event occurs.

Table 18.4 Module operations when event occurs (1 of 2)

Module	Operations when event occurs
GPT	• Start counting • Stop counting • Clear counting • Up counting • Down counting • Input capture.
ADC12	Start A/D conversion
DAC12	Start D/A conversion

Table 18.4 Module operations when event occurs (2 of 2)

Module	Operations when event occurs
I/O ports	• Change pin output based on the EORR (reset) or EOSR (set) • Latch pin state to EIDR • The following ports can be used for the ELC: PORT 1 PORT 2 PORT 3 PORT 4.
DTC	Start DTC data transfer

18.3.3 Example Procedure for Linking Events

To link events:

1. Set the operation of the module for which an event is to be linked.
2. Set the appropriate ELSRn register for the module to be linked.
3. Set the ELCR.ELCON bit to 1 to enable linkage of all events.
4. Configure the module from which an event is output and activate the module. The link between the two modules is now active.
5. To stop event linkage of modules individually, set 000000000b in the ELSRn.ELS[8:0] bits associated with the modules. To stop linkage of all events, set the ELCR.ELCON bit to 0.

18.4 Usage Notes

18.4.1 Linking DMAC or DTC Transfer End Signals as Events

When linking the DMAC or DTC transfer end signals as events, do not set the same peripheral module as the DMAC or DTC transfer destination and event link destination. If set, the peripheral module might be started before DMAC or DTC transfer to the peripheral module is complete.

18.4.2 Setting the Clocks

To link events, you must enable the ELC and the related modules. The modules cannot operate if the related modules are in the module-stop state or in the specific low power mode in which the module is stopped (Software Standby mode or Deep Software Standby mode). Some modules can perform in Snooze mode. For more information, see Table 18.3 and section 11, Low Power Modes.

18.4.3 Setting the Module-Stop Function

The Module Stop Control Register C (MSTPCRC) can enable or disable ELC operation. The ELC is initially stopped after reset. Releasing the module-stop state enables access to the registers. The ELCON bit must be set to 0 before disabling ELC operation using the Module Stop Control Register. For more information, see Table 18.3 and section 11, Low Power Modes.

18.4.4 ELC delay time

In Figure 18.2, module A accesses module B through the ELC. There is a delay time in the ELC between module A and module B. The ELC delay time is shown in Table 18.5.

If the clock domains on both modules A and B are the same, the delay time is 0. But, if the clock domains on modules A and B are different, the ELC module has some delay. The time delay is defined by the slower clock frequency between module A and module B.

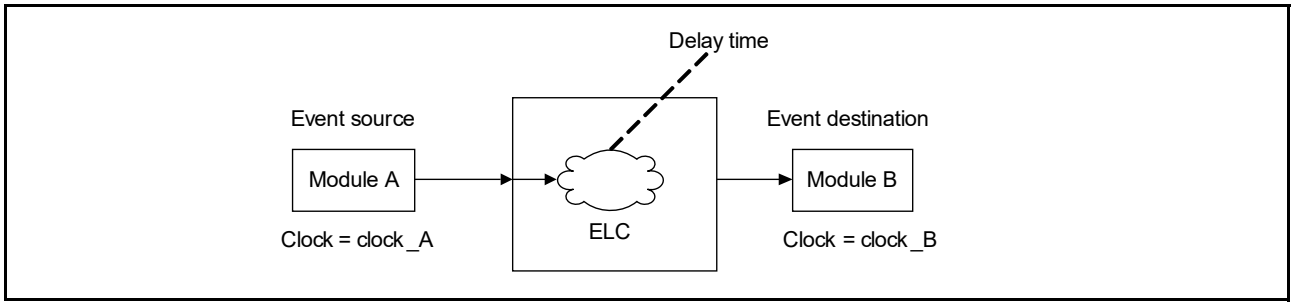


Figure 18.2 ELC delay time

Table 18.5 ELC delay time

Clock domain	Clock frequency	ELC delay time
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1 cycle to 2 cycle
	clock_A > clock_B	1 cycle to 2 cycle of B
	clock_A < clock_B	1 cycle to 2 cycle of A

19. I/O Ports

19.1 Overview

The I/O port pins operate as general I/O port pins, I/O pins for peripheral modules, interrupt input pins, analog I/O, or port group function for the ELC. All pins operate as input pins immediately after a reset, and pin functions are switched by register settings. The I/O ports and peripheral modules for each pin are specified in the associated registers.

Figure 19.1 shows a connection diagram for the I/O port registers. The configuration of the I/O ports differs depending on the package. Table 19.1 lists the I/O port specifications by package, and Table 19.2 lists the port functions.

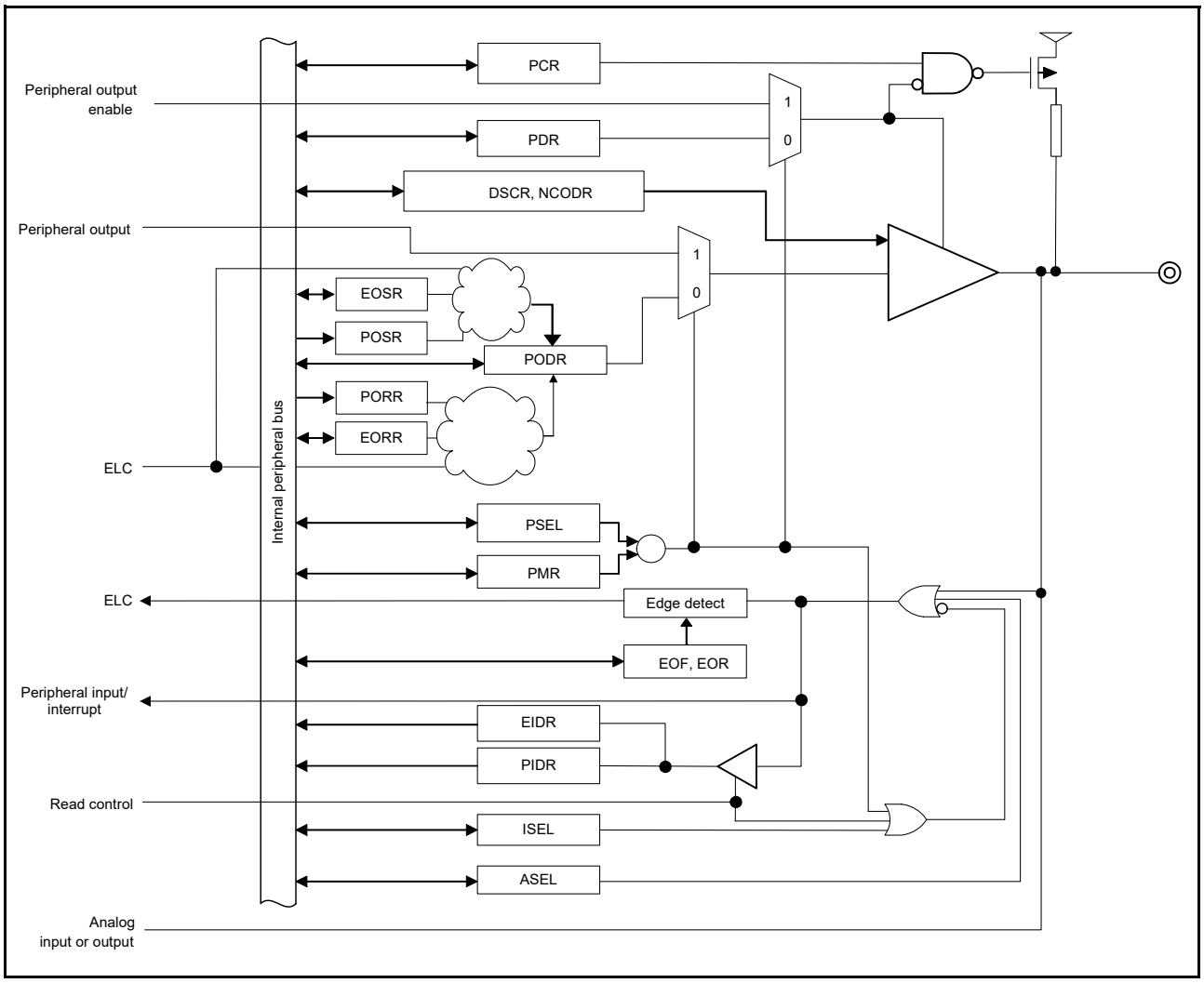


Figure 19.1 Connection diagram for I/O port registers

Note: Figure 19.1 shows a basic port configuration. The configuration differs depending on the ports.

Table 19.1 I/O port specifications

Port	Package		Package	
	100 pins	Number of pins	64 pins	Number of pins
PORT0	P000 to P008, P014, P015	11	P000 to P003, P014, P015	6
PORT1	P100 to P115	16	P100 to P112	13
PORT2	P200, P201, P205 to P214	12	P200, P201, P205 to P207, P210, P212, P213	8
PORT3	P300 to P307	8	P300 to P302	3
PORT4	P400 to P415	16	P400 to P402, P407 to P411	8
PORT5	P500 to P504, P508	6	P500, P501	2
PORT6	P600 to P602, P608 to P610	6	N/A	0
PORT7	P708	1	N/A	0
	Total pins	76	Total pins	40

Table 19.2 I/O port functions

Port	Port name	Input pull-up	Open-drain output	Drive capacity switching	5 V tolerant
PORT0	P000 to P007	-	-	-	-
	P008, P014, P015	✓	✓	-	-
PORT1	P100 to P115	✓	✓	Low, middle, high	-
PORT2	P200	✓	-	-	-
	P201	✓	✓	-	-
	P205, P206	✓	✓	Low, middle, high	✓
	P207 to P214	✓	✓	Low, middle, high	-
PORT3	P300 to P307	✓	✓	Low, middle, high	-
PORT4	P400, P401, P407 to P415	✓	✓	Low, middle, high	✓
	P402 to P406	✓	✓	Low, middle, high	-
PORT5	P500 to P504, P508	✓	✓	Low, middle, high	-
PORT6	P600 to P602, P608 to P610	✓	✓	Low, middle, high	-
PORT7	P708	✓	✓	Low, middle, high	✓

✓: Available

19.2 Register Descriptions

19.2.1 Port Control Register 1 (PCNTR1/PODR/PDR)

Address(es): PORT0.PCNTR1 4004 0000h, PORT1.PCNTR1 4004 0020h, PORT2.PCNTR1 4004 0040h, PORT3.PCNTR1 4004 0060h, PORT4.PCNTR1 4004 0080h, PORT5.PCNTR1 4004 00A0h, PORT6.PCNTR1 4004 00C0h, PORT7.PCNTR1 4004 00E0h

PORT0.PODR 4004 0000h, PORT1.PODR 4004 0020h, PORT2.PODR 4004 0040h, PORT3.PODR 4004 0060h, PORT4.PODR 4004 0080h, PORT5.PODR 4004 00A0h, PORT6.PODR 4004 00C0h, PORT7.PODR 4004 00E0h

PORT0.PDR 4004 0002h, PORT1.PDR 4004 0022h, PORT2.PDR 4004 0042h, PORT3.PDR 4004 0062h, PORT4.PDR 4004 0082h, PORT5.PDR 4004 00A2h, PORT6.PDR 4004 00C2h, PORT7.PDR 4004 00E2h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PODR 15	PODR 14	PODR 13	PODR 12	PODR 11	PODR 10	PODR 09	PODR 08	PODR 07	PODR 06	PODR 05	PODR 04	PODR 03	PODR 02	PODR 01	PODR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PDRn	Pmn Direction	0: Input (functions as an input pin) 1: Output (functions as an output pin).	R/W
b31 to b16	PODRn	Pmn Output Data	0: Low output 1: High output.	R/W

m = 0 to 7
n = 00 to 15

The Port Control Register 1 (PCNTR1/PODR/PDR) is a 32-bit and 16-bit read/write register that controls the port direction and port output data.

The PCNTR1 specifies the port direction and output data, and is accessed in 32-bit units. The PDRn (bits [15:0] in PCNTR1) and PODRn (bits [31:16] in PCNTR1) respectively, are accessed in 16-bit units.

The PDRn bits select the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on port m is associated with a PORTm.PCNTR1.PDRn bit. The I/O direction can be specified in 1-bit units. Bits associated with non-existent pins are reserved. The write value should always be 0. P000 to P007 and P200 are input only, so PORT0.PCNTR1.PDR00-PDR07 and PORT2.PCNTR1.PDR00 are reserved. The PDRn bit in the PORTm.PCNTR1 register serves the same function as the PDR bit in the PFS.PmnPFS register.

The PODRn bits hold data to be output from the general I/O pins. Bits associated with non-existent pins are reserved. The write value should be 0. P000 to P007 and P200 are input only, so PORT0.PCNTR1.PODR00-PODR07 and PORT2.PCNTR1.PODR00 are reserved. Writes to P000 to P007 and P200 have no effect. The PODRn bit in the PORTm.PCNTR1 register serves the same function as the PODR bit in the PFS.PmnPFS register.

19.2.2 Port Control Register 2 (PCNTR2/EIDR/PIDR)

Address(es): PORT0.PCNTR2 4004 0004h, PORT1.PCNTR2 4004 0024h, PORT2.PCNTR2 4004 0044h, PORT3.PCNTR2 4004 0064h, PORT4.PCNTR2 4004 0084h, PORT5.PCNTR2 4004 00A4h, PORT6.PCNTR2 4004 00C4h, PORT7.PCNTR2 4004 00E4h

PORT0.EIDR 4004 0004h, PORT1.EIDR 4004 0024h, PORT2.EIDR 4004 0044h, PORT3.EIDR 4004 0064h, PORT4.EIDR 4004 0084h, PORT5.EIDR 4004 00A4h, PORT6.EIDR 4004 00C4h, PORT7.EIDR 4004 00E4h

PORT0.PIDR 4004 0006h, PORT1.PIDR 4004 0026h, PORT2.PIDR 4004 0046h, PORT3.PIDR 4004 0066h, PORT4.PIDR 4004 0086h, PORT5.PIDR 4004 00A6h, PORT6.PIDR 4004 00C6h, PORT7.PIDR 4004 00E6h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PIDRn	Pmn State	0: Low level 1: High level.	R
b31 to b16	EIDRn	Port Event Input Data*1	When an ELC_PORTx occurs: 0: Low input 1: High input.	R

m = 0 to 7
n = 00 to 15
x = 1 to 4

Note 1. Supported for PORT1 to PORT4.

The Port Control Register 2 (PCNTR2/EIDR/PIDR) allows read access to the Pmn state and the port event input data using 32-bit or 16-bit access.

The PCNTR2 specifies the Pmn state and port event input data, and is accessed in 32-bit units. The PIDRn (bits [15:0] in PCNTR2) and EIDRn (bits [31:16] in PCNTR2) respectively, are accessed in 16-bit units. Bits associated with non-existent pins are reserved. Reserved bits are read as undefined.

The PIDRn bits reflect the individual pin states of the port, regardless of the values set in PmnPFS.PMR and PORTm.PCNTR1.PDRn. The PIDRn bit in the PORTm.PCNTR2 register serves the same function as the PIDR bit in the PFS.PmnPFS register.

A pin state cannot be reflected in PIDRn when one of the following functions is enabled:

- Main clock oscillator (MOSC)
- Analog function (ASEL = 1).

The EIDRn bits latch a pin state when an ELC_PORTx signal occurs. Pin states can only be input to EIDRn when PmnPFS.PMR and PORTm.PCNTR1.PDRn are 0. When the PmnPFS.ASEL bit is set to 1, the associated pin state is not reflected in EIDRn.

19.2.3 Port Control Register 3 (PCNTR3/PORR/POSR)

Address(es): PORT0.PCNTR3 4004 0008h, PORT1.PCNTR3 4004 0028h, PORT2.PCNTR3 4004 0048h, PORT3.PCNTR3 4004 0068h, PORT4.PCNTR3 4004 0088h, PORT5.PCNTR3 4004 00A8h, PORT6.PCNTR3 4004 00C8h, PORT7.PCNTR3 4004 00E8h

PORT0.PORR 4004 0008h, PORT1.PORR 4004 0028h, PORT2.PORR 4004 0048h, PORT3.PORR 4004 0068h, PORT4.PORR 4004 0088h, PORT5.PORR 4004 00A8h, PORT6.PORR 4004 00C8h, PORT7.PORR 4004 00E8h

PORT0.POSR 4004 000Ah, PORT1.POSR 4004 002Ah, PORT2.POSR 4004 004Ah, PORT3.POSR 4004 006Ah, PORT4.POSR 4004 008Ah, PORT5.POSR 4004 00AAh, PORT6.POSR 4004 00CAh, PORT7.POSR 4004 00EAh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PORR 15	PORR 14	PORR 13	PORR 12	PORR 11	PORR 10	PORR 09	PORR 08	PORR 07	PORR 06	PORR 05	PORR 04	PORR 03	PORR 02	PORR 01	PORR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	POSR 15	POSR 14	POSR 13	POSR 12	POSR 11	POSR 10	POSR 09	POSR 08	POSR 07	POSR 06	POSR 05	POSR 04	POSR 03	POSR 02	POSR 01	POSR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	POSRn	Pmn Output Set	0: No effect on output 1: High output.	W
b31 to b16	PORRn	Pmn Output Reset	0: No effect on output 1: Low output.	W

m = 0 to 7
n = 00 to 15

The Port Control Register 3 (PCNTR3/PORR/POSR) is a 32-bit and 16-bit write register that controls the setting or resetting of the port output data.

The PCNTR3 controls the setting or resetting of the port output data, and is accessed in 32-bit units. The POSRn (bits [15:0] in PCNTR3) and PORRn (bits [31:16] in PCNTR3) respectively, are accessed in 16-bit units.

POSR changes PODR when set by a software write. For example, for P100, when PORT1.PCNTR3.POSR00 is 1, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. P000 to P007 and P200 are input only, so PORT0.PCNTR3.POSR00-07 and PORT2.PCNTR3.POSR00 are reserved.

PORR changes PODR when reset by a software write. For example, for P100, when PORT1.PCNTR3.PORR00 is 1, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. P000 to P007 and P200 are input only, so PORT0.PCNTR3.PORR00-07 and PORT2.PCNTR3.PORR00 are reserved.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.
Note: PORRn and POSRn should not be set at the same time.

19.2.4 Port Control Register 4 (PCNTR4/EORR/EOSR)

Address(es): PORT1.PCNTR4 4004 002Ch, PORT2.PCNTR4 4004 004Ch, PORT3.PCNTR4 4004 006Ch, PORT4.PCNTR4 4004 008Ch
PORT1.EORR 4004 002Ch, PORT2.EORR 4004 004Ch, PORT3.EORR 4004 006Ch, PORT4.EORR 4004 008Ch
PORT1.EOSR 4004 002Eh, PORT2.EOSR 4004 004Eh, PORT3.EOSR 4004 006Eh, PORT4.EOSR 4004 008Eh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EORR 15	EORR 14	EORR 13	EORR 12	EORR 11	EORR 10	EORR 09	EORR 08	EORR 07	EORR 06	EORR 05	EORR 04	EORR 03	EORR 02	EORR 01	EORR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EOSR 15	EOSR 14	EOSR 13	EOSR 12	EOSR 11	EOSR 10	EOSR 09	EOSR 08	EOSR 07	EOSR 06	EOSR 05	EOSR 04	EOSR 03	EOSR 02	EOSR 01	EOSR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	EOSRn	Pmn Event Output Set	When an ELC_PORTx occurs: 0: No effect on output 1: High output.	R/W
b31 to b16	EORRn	Pmn Event Output Reset	When an ELC_PORTx occurs: 0: No effect on output 1: Low output.	R/W

m = 1 to 4
n = 00 to 15
x = 1 to 4

The Port Control Register 4 (PCNTR4/EORR/EOSR) is a 32-bit and 16-bit read/write register that controls the setting or resetting of the port output data by an event input from the ELC.

The PCNTR4 controls the setting or resetting of the port output data by an event input from the ELC, and is accessed in 32-bit units. The EOSRn (bits [15:0] in PCNTR4) and EORRn (bits [31:16] in PCNTR4) respectively, are accessed in 16-bit units.

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100, if PORT1.PCNTR4.EOSR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. P200 is input only, so PORT2.PCNTR4.EOSR00 is reserved.

EORR changes PODR when reset because an ELC_PORTx signal occurs. For example, for P100, if PORT1.PCNTR4.EORR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. P200 is input only, so PORT2.PCNTR4.EORR00 is reserved.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.
Note: EORRn and EOSRn should not be set at the same time.

19.2.5 Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 7; n = 00 to 15)

Address(es): PFS.P000PFS 4004 0800h to PFS.P015PFS 4004 083Ch, PFS.P100PFS 4004 0840h to PFS.P115PFS 4004 087Ch, PFS.P200PFS 4004 0880h to PFS.P214PFS 4004 08B8h, PFS.P300PFS 4004 08C0h to PFS.P307PFS 4004 08DCh, PFS.P400PFS 4004 0900h to PFS.P415PFS 4004 093Ch, PFS.P500PFS 4004 0940h to PFS.P508PFS 4004 0960h, PFS.P600PFS 4004 0980h to PFS.P610PFS 4004 09A8h, PFS.P708PFS 4004 09E0h

PFS.P000PFS_HA 4004 0802h to PFS.P015PFS_HA 4004 083Eh, PFS.P100PFS_HA 4004 0842h to PFS.P115PFS_HA 4004 087Eh, PFS.P200PFS_HA 4004 0882h to PFS.P214PFS_HA 4004 08BAh, PFS.P300PFS_HA 4004 08C2h to PFS.P307PFS_HA 4004 08DEh, PFS.P400PFS_HA 4004 0902h to PFS.P415PFS_HA 4004 093Eh, PFS.P500PFS_HA 4004 0942h to PFS.P508PFS_HA 4004 0962h, PFS.P600PFS_HA 4004 0982h to PFS.P610PFS_HA 4004 09AAh, PFS.P708PFS_HA 4004 09E2h

PFS.P000PFS_BY 4004 0803h to PFS.P015PFS_BY 4004 083Fh, PFS.P100PFS_BY 4004 0843h to PFS.P115PFS_BY 4004 087Fh, PFS.P200PFS_BY 4004 0883h to PFS.P214PFS_BY 4004 08BBh, PFS.P300PFS_BY 4004 08C3h to PFS.P307PFS_BY 4004 08DFh, PFS.P400PFS_BY 4004 0903h to PFS.P415PFS_BY 4004 093Fh, PFS.P500PFS_BY 4004 0943h to PFS.P508PFS_BY 4004 0963h, PFS.P600PFS_BY 4004 0983h to PFS.P610PFS_BY 4004 09ABh, PFS.P708PFS_BY 4004 09E3h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*2

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	EOF	EOR	DSCR[1:0]		—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
Value after reset:	0*2	0	0	0	0	0*2	0	0	0	0	0	0*2	0	0	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	PODR	Port Output Data	0: Low output 1: High output.	R/W
b1	PIDR	Pmn State	0: Low level 1: High level.	R
b2	PDR	Port Direction	0: Input (functions as an input pin) 1: Output (functions as an output pin).	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	PCR	Pull-up Control	0: Disable input pull-up 1: Enable input pull-up.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	NCODR	N-Channel Open-Drain Control	0: CMOS output 1: NMOS open-drain output.	R/W
b9 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11, b10	DSCR[1:0]	Port Drive Capability	b11 b10 0 0: Low drive 0 1: Middle drive 1 0: Setting prohibited 1 1: High drive.	R/W
b13, b12	EOF/EOR	Event on Falling/Event on Rising*1	b13 b12 0 0: Don't care 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges.	R/W
b14	ISEL	IRQ Input Enable	0: Not used as an IRQn input pin 1: Used as an IRQn input pin.	R/W
b15	ASEL	Analog Input Enable	0: Not used as analog pin 1: Used as analog pin.	R/W
b16	PMR	Port Mode Control	0: Used as a general I/O pin 1: Used as an I/O port for peripheral functions.	R/W
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28 to b24	PSEL[4:0]	Peripheral Select	These bits select the peripheral function. For individual pin functions, see the associated tables in this chapter.	R/W

Bit	Symbol	Bit name	Description	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: P009PFS to P013PFS, P202PFS to P204PFS, P505PFS to P507PFS and P603PFS to P607PFS for 32-bit, 16-bit, and 8-bit access are not available.
Note 1. Supported for PORT1 to PORT4.
Note 2. The initial value of P000 to P007, P108, P109, P110, P201 and P300 is not 0000_0000h.
P000 to P007 is 0000_8000h, P108 is 0001_0410h, P109 is 0001_0400h, P110 is 0001_0010h, P201 is 0000_0010h, and P300 is 0001_0010h.

The Port mn Pin Function Select register (PmnPFS/PmnPFS_HA/PmnPFS_BY) is a 32-bit, 16-bit, and 8-bit read/write control register that selects the port mn pin function, and is accessed in 32-bit units. PmnPFS_HA (bits [15:0] in PmnPFS) is accessed in 16-bit units. PmnPFS_BY (bits [7:0]) is accessed in 8-bit units.

The PDR/PIDR/PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

The PCR bit enables or disables an input pull-up resistor on the individual port pins. When a pin is in the input state with the associated bit in PmnPFS.PCR set to 1, the pull-up resistor connected to the pin is enabled. When a pin is set as a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the PCR setting. The pull-up resistor is also disabled in the reset state. Bits associated with non-existent pins are reserved. The write value should be 0.

The NCODR bit specifies the output type for the port pins. Bits associated with non-existent pins are reserved. The write value should be 0.

The DSCR bit switches the drive capacity of the port. If the drive capacity of a pin is fixed, the associated bit is a read/write bit, but the drive capacity cannot be changed. Bits associated with non-existent pins are reserved. The write value should be 0.

The EOR and EOF bits select the edge detection method for the port group input signal. These bits support rising, falling, or both edge detections. When the EOR and EOF bits are set to 01b, 10b, or 11b, the input enable of the I/O cell is asserted. Following that, the event pulse is input from the external pin, and the GPIO outputs the event pulse to the ELC. Bits associated with non-existent pins are reserved. The write value should be 0.

The ISEL bit specifies IRQ input pins. This setting can be used in combination with the peripheral functions, although an IRQn (external pin interrupt) of the same number must only be enabled for one pin.

The ASEL bit specifies analog pins. When a pin is set as an analog pin by this bit:

1. Specify it as a general I/O port with the Port Mode Control bit (PmnPFS.PMR).
2. Disable the Pull-up register with the Pull-up Control bit (PmnPFS.PCR).
3. Specify the input with the Port Direction bit (PmnPFS.PDR). The pin state cannot be read at this point. The PmnPFS register is protected by the Write-Protect Register (PWPR). Release write-protect before modifying the register.

The ISEL bit for an unspecified IRQn is reserved. The ASEL bit for an unspecified analog input/output pin is reserved.

The PMR bit specifies the port pin function. Bits associated with non-existent pins are reserved. The write value should be 0.

The PSEL[4:0] bits assign the peripheral function.

For details on the peripheral settings for each product, see section 19.6, Peripheral Select Settings for each Product.

19.2.6 Write-Protect Register (PWPR)

Address(es): PMISC.PWPR 4004 0D03h

	b7	b6	b5	b4	b3	b2	b1	b0
	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	PFSWE	PmnPFS Register Write Enable	0: Writing to the PmnPFS register is disabled 1: Writing to the PmnPFS register is enabled.	R/W
b7	B0WI	PFSWE Bit Write Disable	0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled.	R/W

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register is enabled only when the PFSWE bit is set to 1. You must first write 0 to the B0WI bit before setting PFSWE to 1.

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

19.2.7 AGT Input Control Register (VBTICTLR)

Address(es): SYSTEM.VBTICTLR 4001 E4BBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	VCH2INEN	VCH1INEN	VCH0INEN
Value after reset:	0	0	0	0	0	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	VCH0INEN	AGT Input Enable (P402)	0: Disable 1: Enable.	R/W
b1	VCH1INEN	AGT Input Enable (P403)	0: Disable 1: Enable.	R/W
b2	VCH2INEN	Reserved	The read value is undefined. The write value should be 0.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The VBTICTLR register selects the AGTIO (P402, P403) direction as input.

VCHnINEN bit (AGT Input Enable) (n= 0 to 1)

The VCHnINEN bit enables the input direction on the associated AGTIO (P402, P403). Bits associated with non-existent pins are reserved. The write value should be 0.

For more information on the associated function of CH0 and CH1, see section 19.5.5, I/O Buffer Specification.

19.3 Operation

19.3.1 General I/O Ports

All pins except P000 to P007, P108 to P110, and P300 operate as general I/O ports after reset. General I/O ports are organized as 16 bits per port and can be accessed by port with the Port Control Registers (PCNTRn, where n = 1 to 4), or

by individual pins with the Port mn Pin Function Select register. For details on these registers, see section 19, Register Descriptions.

Each port has the following bits:

- Port Direction bit (PDRn), which selects input or output direction
- Port Output Data bit (PODRn), which holds data for output
- Port Input Data bit (PIDRn), which indicates the pin state
- Event Input Data bit (EIDRn), which indicates the pin state when an ELC_PORT1, 2, 3, or 4 signal occurs
- Port Output Set bit (POSRn), which indicates the output value when a software write occurs
- Port Output Reset bit (PORRn), which indicates the output value when a software write occurs
- Event Output Set bit (EOSRn), which indicates the output value when an ELC_PORT1, 2, 3 or 4 signal occurs
- Event Output Reset bit (EORRn), which indicates the output value when an ELC_PORT1, 2, 3 or 4 signal occurs.

19.3.2 Port Function Select

The following port functions are available for configuring each pin:

- I/O configuration: Complementary or open-drain output, pull-up control, and drive strength
- General I/O port: Port direction, output data setting, and reading input data
- Alternate function: Configured function mapping to the pin.

Each pin is associated with a Port mn Pin Function Select register (PmnPFS), which includes the associated PODR, PIDR, and PDR bits. In addition, the PmnPFS register includes:

- PCR: Pull-up resistor control bit that turns the input pull-up MOS on or off
- NCODR: N-channel open-drain control bit that selects the output type for each pin
- DSCR: Drive capacity control bit that selects the drive capacity
- EOR: Event on rising bit used to detect rising edges on the port input
- EOF: Event on falling bit used to detect falling edges on the port input
- ISEL: IRQ input enable bit to specify an IRQ input pin
- ASEL: Analog input enable bit to specify an analog pin
- PMR: Port mode control bit to specify the pin function of each port
- PSEL[4:0]: Port function select bits to select the associated peripheral function.

These configurations can be made by a single-register access to the Port mn Pin Function Select register. For details, see section 19, Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 7; n = 00 to 15).

19.3.3 Port Group Function for the ELC

In the MCU, PORT1 to PORT4 are assigned for the port group function.

19.3.3.1 Behavior when ELC_PORT1, 2, 3, or 4 is input from the ELC

The MCU supports the two functions described in this section when an ELC_PORT1, 2, 3, or 4 signal comes from the ELC.

(1) Input to EIDR

For the GPI function (PDR = 0 and PMR = 0 in the PmnPFS register), when an ELC_PORT1, 2, 3, or 4 signal comes from the ELC, the input enable of the I/O cell is asserted, and data from the external pins are read into the EIDR bit. See Figure 19.2.

For the GPO function (PDR = 1) or the peripheral mode (PMR = 1), 0 is input into the EIDR bit from the external pins.

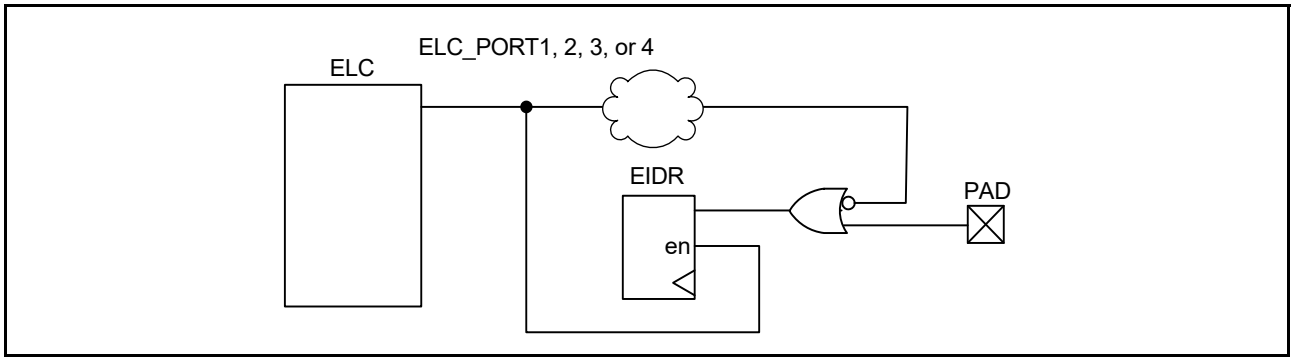


Figure 19.2 Event ports input data

(2) Output from PODR by EOSR/EORR

When an ELC_PORT1, 2, 3, or 4 signal occurs, the data is output from the PODR to the external pin based on the EOSR/EORR bit settings as follows:

- If EOSR is set to 1, when an ELC_PORT1, 2, 3, or 4 signal occurs, the PODR register outputs 1 to the external pin. Otherwise, when EOSR = 0, the PODR value is kept.
- If EORR is set to 1, when an ELC_PORT1, 2, 3, or 4 signal occurs, the PODR register outputs 0 to the external pin. Otherwise, when EORR = 0, the PODR value is kept.

See Figure 19.3.

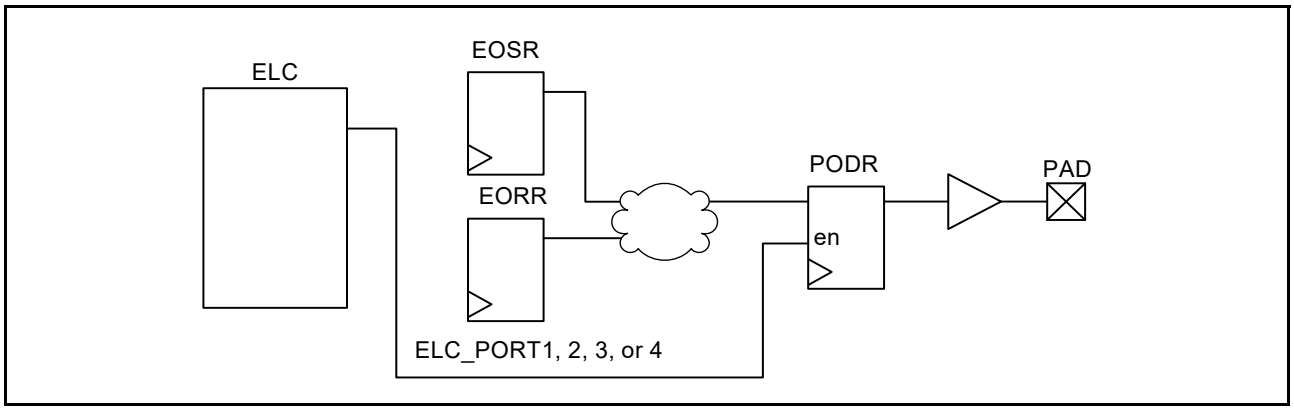


Figure 19.3 Event ports output data

19.3.3.2 Behavior when an event pulse is output to the ELC

To output the event pulse from the external pins to the ELC, set the EOR/EOF bits in the PmnPFS register. For details, see section 19.2.5, Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 7; n = 00 to 15). When the EOR/EOF bits are set, the input enable of the I/O cell is asserted.

Data from the external pin is the input. For example, for PORT1, when the data is input from P100 to P115, the data of those 16 pins is organized by OR logic. This data is formed into a one-shot pulse that goes to the ELC. The operation of PORT2 to PORT4 is the same. See Figure 19.4.

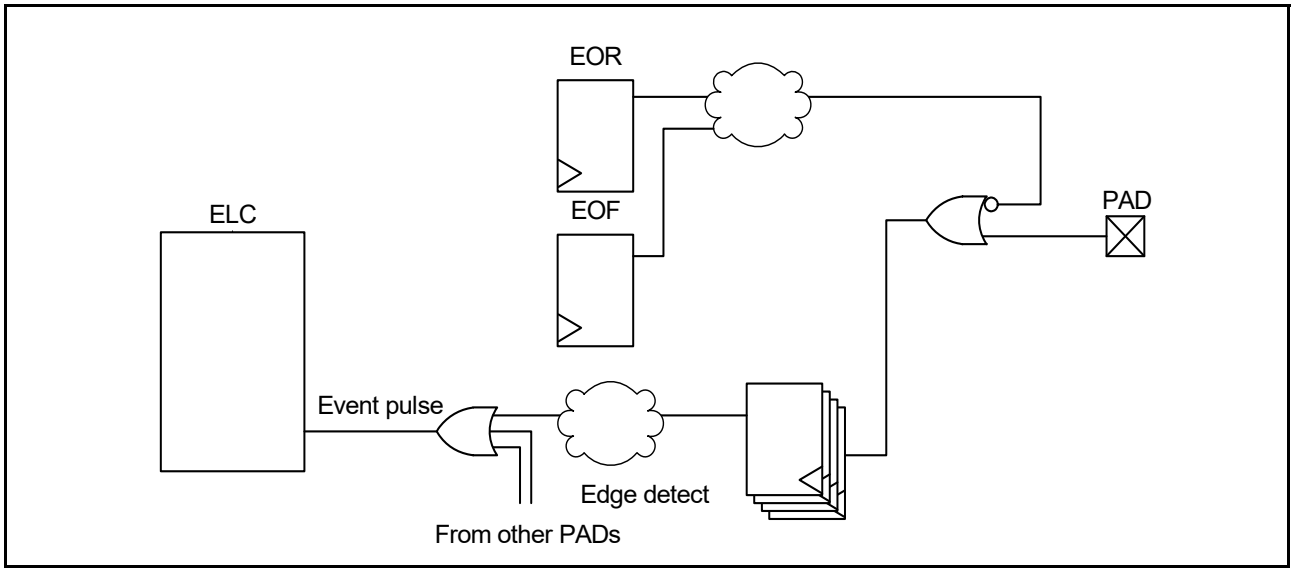


Figure 19.4 Generation of event pulse

19.4 Handling of Unused Pins

Table 19.3 shows how to handle unused pins.

Table 19.3 Handling of unused pins

Pin name	Handling when unused
MD	Use as a mode pin
RES	Connect to VCC through a resistor (pulling up)
P200/NMI	Connect to VCC through a resistor (pulling up)
EXTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P212). When this pin is not used as port P212, configure it in the same way as ports 1 to 7.
XTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P213). When the external clock is input to the EXTAL pin, the XTAL pin functions as P213. When this pin is not used as port P213, configure it in the same way as ports 1 to 7.
XCIN	Connect to VSS through a resistor (pulling down)
XCOUT	Keep pin open
P000 to P007	Connect to AVCC0 (pulled up) through a resistor or to AVSS0 (pulled down) through a resistor*1, *4
P008, P014, P015	• If the direction is set to input (PCNTR1.PDRn = 0), connect the associated pin to AVCC0 (pulled up) through a resistor or to AVSS0 (pulled down) through a resistor*1 • If the direction is set to output (PCNTR1.PDRn = 1), release the pin*1.
P1x to P7x	• If the direction is set to input (PCNTR1.PDRn = 0), connect the associated pin to VCC (pulled up) through a resistor or to VSS (pulled down) through a resistor*1, *2 • If the direction is set to output (PCNTR1.PDRn = 1), release the pin*1, *3.
VREFH0, VREFH	Connect to AVCC0
VREFL0, VREFL	Connect to AVSS0

Note 1. Clear the PmnPFS.PMR, PmnPFS.ISEL, PmnPFS.PCR, and PmnPFS.ASEL bits to 0.
Note 2. P108, P110, P300 are recommended for pull up VCC (pulled up) through a resistor, because these pins are input pull-up enabled from the initial value (PmnPFS.PCR = 1).
Note 3. P109 is recommended to be set as an output (PCNTR1.PDRn = 1), because this pin is output from the initial value.
Note 4. To reduce input leakage current of P003 and P007, set the P003PFS.ASEL and P007PFS.ASEL bits to 0.
When using 64-pin product, set P007PFS.ASEL bit to 0.

19.5 Usage Notes

19.5.1 Procedure for Specifying the Pin Functions

To specify the I/O pin functions:

1. Clear the B0WI bit in the PWPR register. This enables writing to the PFSWE bit in the PWPR register.
2. Set 1 to the PFSWE bit in the PWPR register. This enables writing to the PmnPFS register.
3. Clear the Port Mode Control bit in the PMR for the target pin to select the general I/O port.
4. Specify the I/O function for the pin through the PSEL[4:0] bit settings in the PmnPFS register.
5. Set the PMR bit to 1 as required to switch to the selected I/O function for the pin.
6. Clear the PFSWE bit in the PWPR register. This disables writing to the PmnPFS register.
7. Set 1 to the B0WI bit in the PWPR register. This disables writing to the PFSWE bit in the PWPR register.

19.5.2 Procedure for Using Port Group Input

To use the port group input (PORT1 to PORT4):

1. Set the ELSRx.ELS[8:0] bits to 0000 0000b to ignore unexpected pulses. For more information, see section 18, Event Link Controller (ELC).
2. Set the EOF/EOR bit of the PmnPFS register to specify the rising, falling, or both edge detections.
3. Execute a dummy read or wait for a short time, for example 100 ns. Ignoring of unexpected pulses depends on the initial value of the external pin.
4. Set the ELSRx.ELS[8:0] bits to enable the event signals.

19.5.3 Port Output Data Register (PODR) Summary

This register outputs data as follows:

1. Output 0 if PCNTR4.EORRn is set to 1 when an ELC_PORT1, 2, 3, or 4 signal occurs.
2. Output 1 if PCNTR4.EOSRn is set to 1 when an ELC_PORT1, 2, 3, or 4 signal occurs.
3. Output 0 if PCNTR3.PORRn is set to 1.
4. Output 1 if PCNTR3.POSRn is set to 1.
5. Output 0 or 1 because PCNTR1.PODRn is set.
6. Output 0 or 1 because PmnPFS.PODRn is set.

Numbers in this list correspond to the priority for writing to the PODR. For example, if 1. and 3. from the list occur at the same time, the higher priority event 1. is executed.

19.5.4 Notes on Using Analog Functions

To use an analog function, set the Port Mode Control bit (PMR) and Port Direction bit (PDR) to 0 so that the pin acts as a general input port. Next, set the Analog Input Enable bit (ASEL) in the Port mn Pin Function Select register (PmnPFS.ASEL) to 1.

19.5.5 I/O Buffer Specification

The P402, P403, and P404 can be used as AGT input and other peripheral functions.

Table 19.4 lists the P402, P403, P404 specifications.

Table 19.4 P402, P403, P404 specifications

	Functions			
I/O port	**AGT**		**Other peripheral**	
	AGT input enable register	AGT	Other peripheral enable register	CAC, GPT, CAN, and interrupt
P402	VBTICTLR .VCH0INEN	AGTIO0 AGTIO1	P402PFS.PSEL and PMR	For details, see Table 19.12 Register settings for I/O pin functions on PORT4
P403	VBTICTLR .VCH1INEN	AGTIO0 AGTIO1	P403PFS.PSEL and PMR	
P404	VBTICTLR .VCH2INEN	—	P404PFS.PSEL and PMR	

These AGT inputs are controlled by the VBTICTLR register, which has the highest priority for selecting the AGT input functions. See Figure 19.5.

The VBTICTLR register is not initialized on reset. Therefore, when not using the AGT inputs, the associated bit of the VBTICTLR register must be set to 0 after reset. Set VBTICTLR.VCH2INEN bit to 0 after reset. When using 64-pin product, also set VBTICTLR.VCH1INEN bit to 0.

For more information on the VBTICTLR register, see section 19.2.7, AGT Input Control Register (VBTICTLR).

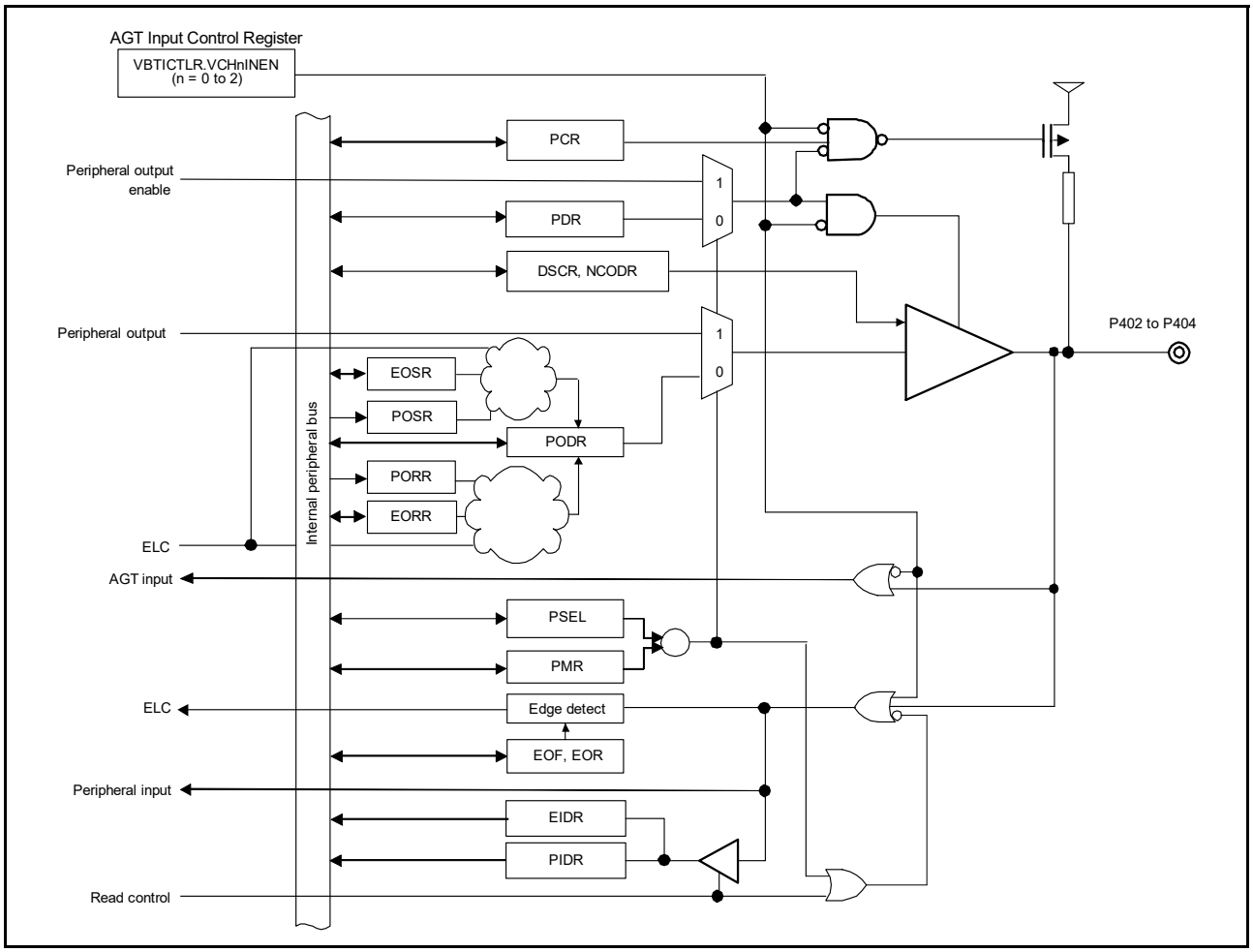


Figure 19.5 P402, P403, P404 diagram

19.6 Peripheral Select Settings for each Product

This section describes the pin function select configuration by the PmnPFS register. Some pin names have added _A and _B suffixes. When assigning IIC and SPI functionality, select the functional pins having the same suffix. The other pins can be selected regardless of the suffix. Assigning the same function to two or more pins simultaneously is prohibited.

19.7 Notes on the PmnPFS Register Setting

(1) In the Port mn Pin Function Select register (PmnPFS), the PSEL bits must be set when the PMR bit of the target pin is 0. If the PSEL bits are set when the PMR bit is 1, unexpected edges might be input for the input function or unexpected pulses might be output to the external pin for the output function.

(2) Only the allowed values (functions) should be specified in the PSEL bits of PmnPFS. If a value that is not allowed for the register is specified, the correct operation is not guaranteed.

(3) A single function should not be assigned to multiple pins by the PmnPFS register.

(4) PORT0 and PORT5 have the analog functions such as A/D converter and D/A converter. When these pins are used as an analog function, to avoid loss of resolution, the PMR and PDR bits should be set to 0. After that, the ASEL bit should be set to 1.

(5) The initial value of the ASEL bit for P003 and P007 is 1. When these pins are not used as an analog function, to reduce the input leakage current, the ASEL bit should be set to 0. When using 64-pin product, clear the P007PFS.ASEL bit to 0.

Table 19.5 Register settings for I/O pin functions (PORT0)

PSEL[4:0] settings	Function	Pin							
		P000	P001	P002	P003	P004	P005	P006	P007
00000b (value after reset)	Hi-z/JTAG/SWD	Hi-Z							
ASEL bit		AN000/ IVCMP2	AN001/ IVCMP2	AN002/ IVCMP2	PGAVSS000/ AN007	AN100/ IVCMP2	AN101/ IVCMP2	AN102/ IVCMP2	PGAVSS100/ AN107
ISEL bit		IRQ6-DS	IRQ7-DS	IRQ8-DS		IRQ9-DS	IRQ10-DS	IRQ11-DS	
DSCR[1:0] bits	Drive capacity control	—	—	—	—	—	—	—	—
NCODR bit	N-ch open-drain	—	—	—	—	—	—	—	—
PCR bit	Pull-up	—	—	—	—	—	—	—	—
Number of pins	100 pins	✓	✓	✓	✓	✓	✓	✓	✓
	64 pins	✓	✓	✓	✓	—	—	—	—

✓: Available

Table 19.6 Register settings for I/O pin functions (PORT0)

PSEL[4:0] settings	Function	Pin		
		P008	P014	P015
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z		
ASEL bit		AN003	AN005/ AN105/ DA0/ IVREF3	AN006/ AN106/ DA1/ IVCMP1
ISEL bit		IRQ12-DS		IRQ13
DSCR[1:0] bits	Drive capacity control	*1	*1	*1
NCODR bit	N-ch open-drain	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓
Number of pins	100 pins	✓	✓	✓
	64 pins	—	✓	✓

✓: Available
—: Setting prohibited

Note 1. The drive strength of this port cannot be controlled by PmnPFS.DSCR[1:0] bits.

Table 19.7 Register settings for I/O pin functions (PORT1)

PSEL[4:0] settings	Function	Pin							
		P100	P101	P102	P103	P104	P105	P106	P107
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	AGTIO0	AGTEE0	AGTO0	—	—	—	AGTOB0	AGTOA0
00010b	GPT	GTETRGA	GTETRGB	GTOWLO	GTOWUP	GTETRGB	GTETRGA	—	—
00011b	GPT*2	GTIOC5B	GTIOC5A	GTIOC2B_A	GTIOC2A_A	GTIOC1B	GTIOC1A	GTIOC8B	GTIOC8A
00100b	SCI	RXD0/MISO0/ SCL0	TXD0/MOSI0/ SDA0	SCK0	CTS0_RTS0/ SS0	RXD8/MISO8/ SCL8	TXD8/MOSI8/ SDA8	SCK8	CTS8_RTS8/ SS8
00101b	SCI	SCK1	CTS1_RTS1/ SS1	—	—	—	—	—	—
00110b	SPI*1	MISOA_A	MOSIA_A	RSPCKA_A	SSLA0_A	SSLA1_A	SSLA2_A	SSLA3_A	—
00111b	IIC*1	SCL1_B	SDA1_B	—	—	—	—	—	—
01000b	KINT	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07
01010b	CAC/ADC12	—	—	ADTRG0	—	—	—	—	—
10000b	CAN	—	—	CRX0	CTX0	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—
ISEL bit		IRQ2	IRQ1	—	—	IRQ1	IRQ0	—	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	100 pins	✓	✓	✓	✓	✓	✓	✓	✓
	64 pins	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 19.8 Register settings for I/O pin functions (PORT1)

PSEL[4:0] settings	Function	Pin							
		P108	P109	P110	P111	P112	P113	P114	P115
00000b (value after reset)	Hi-Z/JTAG/SWD	TMS/SWDIO	TDO/SWO	TDI	Hi-Z				
00010b	GPT	GTOULO	GTOVUP	GTOVLO	—	—	—	—	—
00011b	GPT*2	GTIOC0B_A	GTIOC1A_A	GTIOC1B_A	GTIOC3A_A	GTIOC3B_A	GTIOC2A	GTIOC2B	GTIOC4A
00100b	SCI	—	—	CTS2_RTS2/ SS2	SCK2	TXD2/MOSI2/ SDA2	RXD2/MISO2/ SCL2	—	—
00101b	SCI	CTS9_RTS9/ SS9	TXD9/MOSI9/ SDA9	RXD9/MISO9/ SCL9	SCK9	SCK1	—	—	—
00110b	SPI*1	SSLB0_B	MOSIB_B	MISOB_B	RSPCKB_B	SSLB0_B	—	—	—
01001b	CLKOUT/ACMPHS	—	CLKOUT	VCOUT	—	—	—	—	—
10000b	CAN	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—
ISEL bit		—	—	IRQ3	IRQ4	—	—	—	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	100 pins	✓	✓	✓	✓	✓	✓	✓	✓
	64 pins	✓	✓	✓	✓	✓	—	—	—

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 19.9 Register settings for I/O pin functions (PORT2)

PSEL[4:0] settings	Function	Pin				
		P200	P201	P205	P206	P207
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
00001b	AGT	—	—	AGTO1	—	—
00010b	GPT	—	—	GTIV	GTIU	—
00011b	GPT*2	—	—	GTIOC4A	—	—
00100b	SCI	—	—	TXD4/MOSI4/ SDA4	RXD4/MISO4/ SCL4	—
00101b	SCI	—	—	CTS9_RTS9/ SS9	—	—
00111b	IIC*1	—	—	SCL1_A	SDA1_A	—
01001b	CLKOUT/ACMPHS	—	—	CLKOUT	—	—
10000b	CAN	—	—	—	—	—
ASEL bit		—	—	—	—	—
ISEL bit		NMI	—	IRQ1-DS	IRQ0-DS	—
DSCR[1:0] bits	Drive capacity control	—	*3	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	—	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓
Number of pins	100 pins	✓	✓	✓	✓	✓
	64 pins	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).
Note 3. The drive strength of this port cannot be controlled by PmnPFS.DSCR[1:0] bits.

Table 19.10 Register settings for I/O pin functions (PORT2)

PSEL[4:0] settings	Function	Pin						
		P208	P209	P210	P211	P212	P213	P214
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z						
00001b	AGT	—	—	—	—	AGTEE1	—	—
00010b	GPT	GTOVL0	GTOVUP	GTIW	GTIV	GTETRGD	GTETRGC	GTIU
00011b	GPT*1	—	—	—	—	GTIOC0B	GTIOC0A	—
00101b	SCI	—	—	—	—	RXD1/MISO1/ SCL1	TXD1/MOSI1/ SDA1	—
01010b	CAC/ADC12	—	—	—	—	—	ADTRG1	—
11010b	Trace (Debug)	TDATA3	TDATA2	TDATA1	TDATA0	—	—	TCLK
ASEL bit		—	—	—	—	—	—	—
ISEL bit		—	—	—	—	IRQ3	IRQ2	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓
Number of pins	100 pins	✓	✓	✓	✓	✓	✓	✓
	64 pins	—	—	✓	—	✓	✓	—

✓: Available
—: Setting prohibited

Note 1. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 19.11 Register settings for I/O pin functions (PORT3)

PSEL[4:0] settings	Function	Pin							
		P300	P301	P302	P303	P304	P305	P306	P307
00000b (value after reset)	Hi-Z/JTAG/SWD	TCK/SWCLK	Hi-Z						
00001b	AGT	—	AGTIO0	—	—	—	—	—	—
00010b	GPT	—	GTOULO	GTOUUP	—	GTOWLO	GTOWUP	GTOULO	GTOUUP
00011b	GPT*2	GTIOC0A_A	GTIOC4B	GTIOC4A	GTIOC7B	GTIOC7A	—	—	—
00100b	SCI	—	RXD2/MISO2/ SCL2	TXD2/MOSI2/ SDA2	—	—	—	—	—
00101b	SCI	—	CTS9_RTS9/ SS9	—	—	—	—	—	—
00110b	SPI*1	SSLB1_B	SSLB2_B	SSLB3_B	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—
ISEL bit		—	IRQ6	IRQ5	—	IRQ9	IRQ8	—	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	100 pins	✓	✓	✓	✓	✓	✓	✓	✓
	64 pins	✓	✓	✓	—	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 19.12 Register settings for I/O pin functions (PORT4)

PSEL[4:0] settings	Function	Pin							
		P400	P401	P402	P403	P404	P405	P406	P407
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	AGTIO1	—	—	—	—	—	—	AGTIO0
00010b	GPT	—	GTETRGA	—	—	—	—	—	—
00011b	GPT*3	GTIOC6A	GTIOC6B	—	GTIOC3A	GTIOC3B	GTIOC1A	GTIOC1B	—
00100b	SCI	SCK4	CTS4_RTS4/ SS4	—	—	—	—	—	CTS4_RTS4/ SS4
00111b	IIC*2	SCL0_A	SDA0_A	—	—	—	—	—	SDA0_B
01001b	CLKOUT/ACMPHS	—	—	—	—	—	—	—	—
01010b	CAC/ADC12	ADTRG1	—	CACREF	—	—	—	—	ADTRG0
10000b	CAN	—	CTX0	CRX0	—	—	—	—	—
Don't-care	AGT	—	—	AGTIO0*1/ AGTIO1*1	AGTIO0*1/ AGTIO1*1	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—
ISEL bit		IRQ0	IRQ5-DS	IRQ4-DS	—	—	—	—	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	100 pins	✓	✓	✓	✓	✓	✓	✓	✓
	64 pins	✓	✓	✓	—	—	—	—	✓

✓: Available
—: Setting prohibited

Note 1. To use this pin function, set the associated pin as a general input (set the PmnPFS.PDR and PmnPFS.PMR bits to 0).
Note 2. Renesas recommends using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 19.13 Register settings for I/O pin functions (PORT4)

PSEL[4:0] settings	Function	Pin							
		P408	P409	P410	P411	P412	P413	P414	P415
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	AGTOB1	AGTOA1	AGTEE1	—	—	—
00010b	GPT	GTOWLO	GTOWUP	GTOVLO	GTOVUP	GTOULO	GTOUUP	—	—
00011b	GPT*2	GTIOC10B	GTIOC10A	GTIOC9B	GTIOC9A	—	—	GTIOC0B	GTIOC0A
00100b	SCI	—	—	RXD0/MISO0/ SCL0	TXD0/MOSI0/ SDA0	SCK0	CTS0_RTS0/ SS0	—	—
00101b	SCI	RXD3/MISO3/ SCL3	TXD3/MOSI3/ SDA3	SCK3	CTS3_RTS3/ SS3	—	—	—	—
00110b	SPI*1	—	—	MISOA_B	MOSIA_B	RSPCKA_B	SSLA0_B	SSLA1_B	SSLA2_B
00111b	IIC*1	SCL0_B	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—
ISEL bit		IRQ7	IRQ6	IRQ5	IRQ4	—	—	IRQ9	IRQ8
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	100 pins	✓	✓	✓	✓	✓	✓	✓	✓
	64 pins	✓	✓	✓	✓	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 19.14 Register settings for I/O pin functions (PORT5)

PSEL[4:0] settings	Function	Pin					
		P500	P501	P502	P503	P504	P508
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z					
00001b	AGT	AGTOA0	AGTOB0	—	—	—	—
00010b	GPT	GTIU	GTIV	GTIW	GTETRGC	GTETRGD	—
00011b	GPT*1	GTIOC11A	GTIOC11B	GTIOC12A	GTIOC12B	—	—
ASEL bit		AN016/ IVREF0	AN116/ IVREF1	AN017/ IVCMP0	AN117	AN018	AN020
ISEL bit		—	IRQ11	IRQ12	—	—	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓
Number of pins	100 pins	✓	✓	✓	✓	✓	✓
	64 pins	✓	✓	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 19.15 Register settings for I/O pin functions (PORT6)

PSEL[4:0] settings	Function	Pin					
		P600	P601	P602	P608	P609	P610
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z					
00011b	GPT*1	GTIOC6B	GTIOC6A	GTIOC7B	GTIOC4B	GTIOC5A	GTIOC5B
00101b	SCI	SCK9	RXD9	TXD9	—	—	—
01001b	CLKOUT/ACMPHS	CLKOUT	—	—	—	—	—
01010b	CAC/ADC12	CACREF	—	—	—	—	—
10000b	CAN	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—
ISEL bit		—	—	—	—	—	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓
Number of pins	100 pins	✓	✓	✓	✓	✓	✓
	64 pins	—	—	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 19.16 Register settings for I/O pin functions (PORT7)

PSEL[4:0] settings	Function	Pin
		P708
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z
00101b	SCI	RXD1/MISO1/ SCL1
00110b	SPI*1	SSLA3_B
01010b	CAC/ADC12	CACREF
ASEL bit		—
ISEL bit		IRQ11
DSCR[1:0] bits	Drive capacity control	L/M/H
NCODR bit	N-ch open-drain	✓
PCR bit	Pull-up	✓
Number of pins	100 pins	✓
	64 pins	—

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

20. Key Interrupt Function (KINT)

20.1 Overview

A key interrupt (KEY_INTKR) can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins, KR00 to KR07.

Table 20.1 shows the pin assignment for key interrupt detection, Table 20.2 shows the function configuration, and Figure 20.1 shows a block diagram.

Table 20.1 Assignment of key interrupt detection pins

Key interrupt mode control n (n = 0 to 7)	Description
KRM0	Controls KR00 signal in 1-bit units
KRM1	Controls KR01 signal in 1-bit units
KRM2	Controls KR02 signal in 1-bit units
KRM3	Controls KR03 signal in 1-bit units
KRM4	Controls KR04 signal in 1-bit units
KRM5	Controls KR05 signal in 1-bit units
KRM6	Controls KR06 signal in 1-bit units
KRM7	Controls KR07 signal in 1-bit units

Table 20.2 Configuration of key interrupt function

Parameter	Configuration
Input	KR00 to KR07
Control registers	Key Return Control Register (KRCTL) Key Return Mode Register (KRM) Key Return Flag Register (KRF)

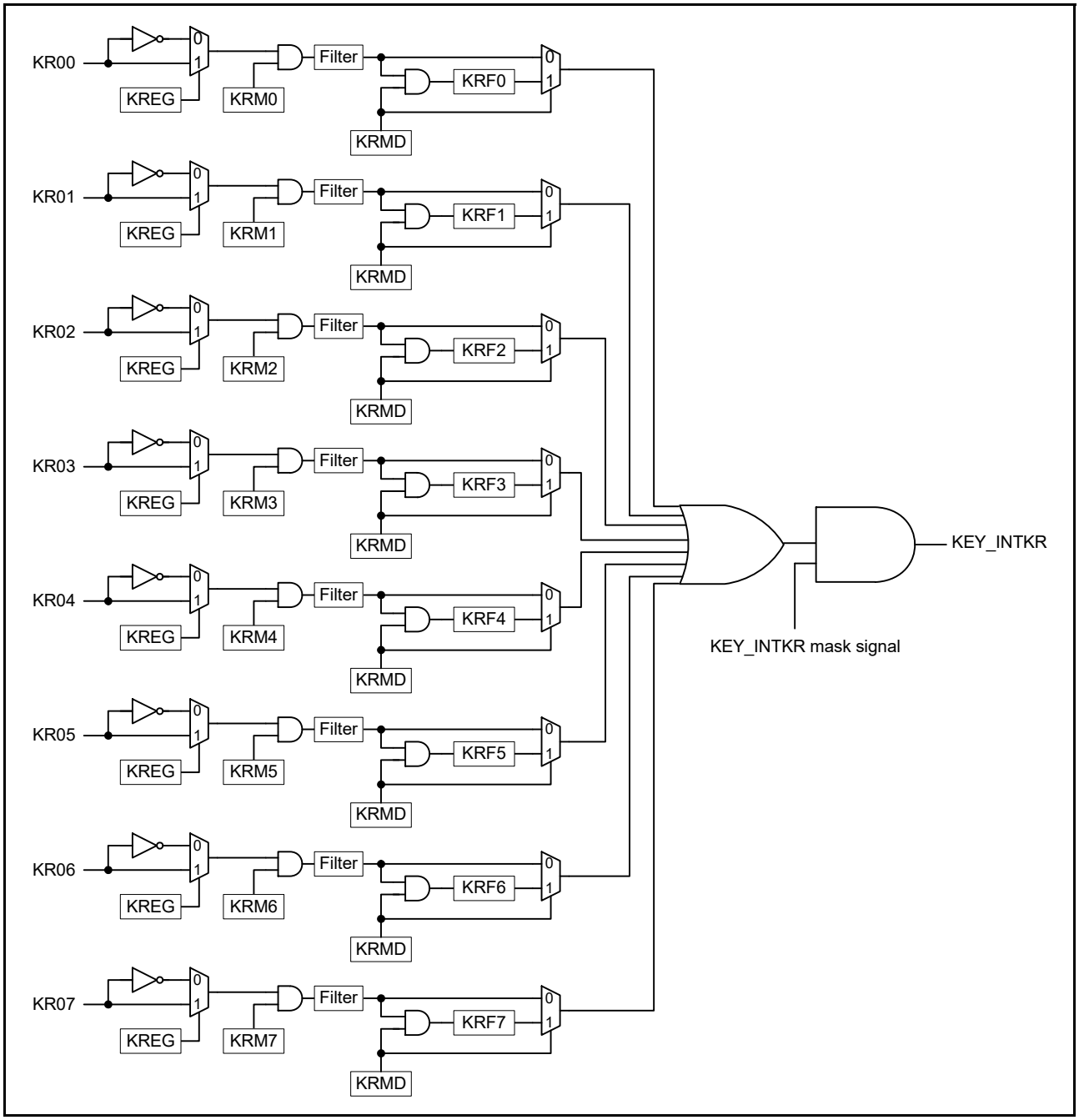


Figure 20.1 Key interrupt function block diagram

Note: In Figure 20.1, all key return factors are merged by an OR gate, and the key interrupt (KEY_INTKR) is the output of the AND gate to mask the merged key return factor by the KEY_INTKR mask signal. When using KRFn (KRMD = 1), the KEY_INTKR mask signal is used as the output mask that is asserted by clearing KRFn.

20.2 Register Descriptions

20.2.1 Key Return Control Register (KRCTL)

Address(es): KINT.KRCTL 4008 0000h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRMD	—	—	—	—	—	—	KREG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	KREG	Detection Edge Selection (KR00 to KR07)	0: Falling edge 1: Rising edge.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	KRMD	Usage of Key Interrupt Flags (KRF0 to KRF7)	0: Do not use key interrupt flags 1: Use key interrupt flags.	R/W

The KRCTL register controls the usage of the key interrupt flags, KRF0 to KRF7, and sets the detection edge.

20.2.2 Key Return Flag Register (KRF)

Address(es): KINT.KRF 4008 0004h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRF7	KRF6	KRF5	KRF4	KRF3	KRF2	KRF1	KRF0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	KRFn	Key Interrupt Flag n	0: No key interrupt detected 1: Key interrupt detected.	R/W

n = 0 to 7

Note: When KRMD = 0, setting the KRFn bit to 1 is prohibited.
When setting the KRFn bit to 1, the KRFn value does not change. To clear the KRFn bit, confirm the target bit is 1 before writing 0 to the bit, then write 1 to the other bits.

The KRF register controls the key interrupt flags, KRF0 to KRF7.

20.2.3 Key Return Mode Register (KRM)

Address(es): KINT.KRM 4008 0008h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	KRMn	Key Interrupt Mode Control n	0:No key interrupt signal detected 1:Key interrupt signal detected.	R/W

n = 0 to 7

Note: The on-chip pull-up resistors can be applied by setting the associated key interrupt input pin in the pull-up function. For more information, see section 19, I/O Ports.
Key interrupts can be assigned in the PmnPFS.PSEL[4:0] bits. For details, see section 19, I/O Ports.
An interrupt is generated when the target bit in the KRM register is set while a low level (KREG = 0) or a high level (KREG = 1) is being input to the key interrupt input pin. To ignore this interrupt, set the KRM register after disabling the interrupt handling.

The KRM register sets the key interrupt mode.

20.3 Operation

20.3.1 Operation When Not Using Key Interrupt Flag (KRMD = 0)

A key interrupt (KEY_INTKR) is generated when the valid edge specified in the KREG bit is input to a key interrupt pin, KR00 to KR07. To identify the channel to which the valid edge is input, read the port register and check the port level after the key interrupt (KEY_INTKR) is generated.

The KEY_INTKR signal changes based on the input level of the key interrupt input pin, KR00 to KR07.

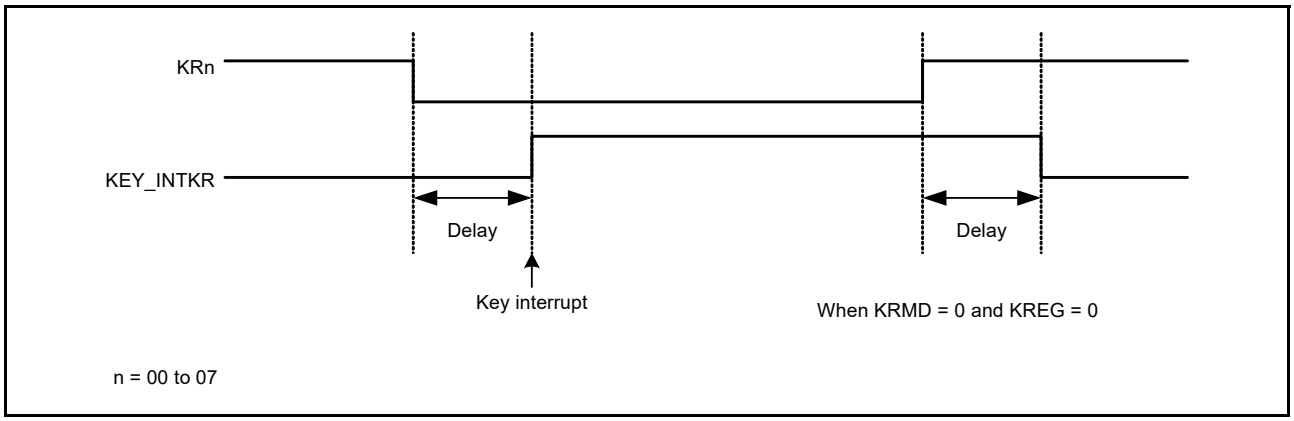


Figure 20.2 Operation of KEY_INTKR signal when a key interrupt is input to a single channel

Figure 20.3 shows the operation when a valid edge is input to multiple key interrupt input pins. The KEY_INTKR signal is set while a low level is being input to one pin (when KREG is 0). Therefore, even if a falling edge is input to another pin in this period, a key interrupt (KEY_INTKR) is not generated again. See [1] in Figure 20.3.

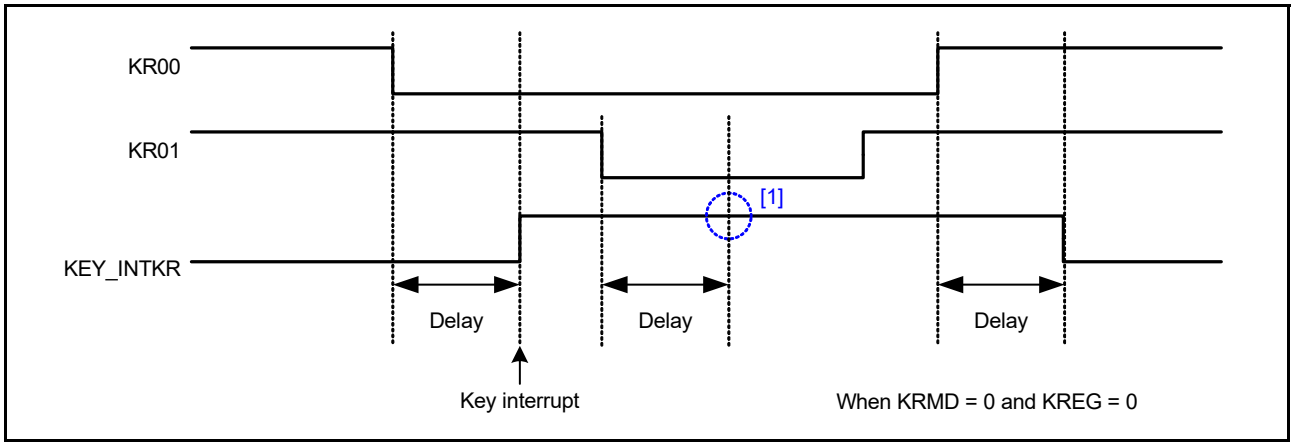


Figure 20.3 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

20.3.2 Operation When Using the Key Interrupt Flags (KRMD = 1)

A key interrupt (KEY_INTKR) is generated when the valid edge specified in the KREG bit is input to a key interrupt pin, KR00 to KR07. To identify the channels to which the valid edge is input, read the Key Return Flag Register (KRF) after the key interrupt (KEY_INTKR) is generated. If the KRMD bit is set to 1, clear the KEY_INTKR signal by clearing the associated bit in the KRF register.

As Figure 20.4 shows, only one interrupt is generated each time a falling edge is input to one channel, that is, when KREG = 0, regardless of whether the KRFn bit is cleared before or after a rising edge is input.

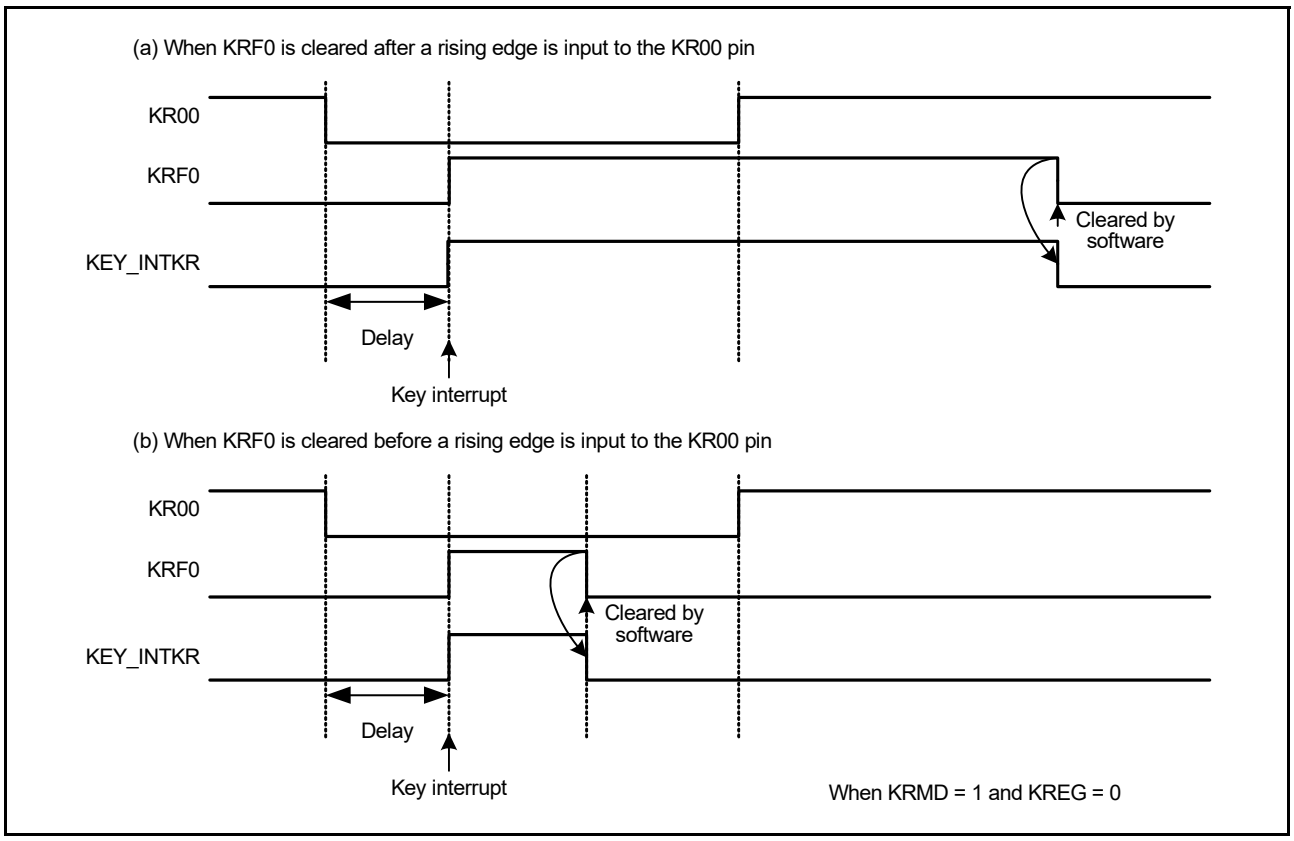


Figure 20.4 Basic operation of KEY_INTKR signal when key interrupt flag is used

Figure 20.5 shows the operation when a valid edge is input to multiple key interrupt input pins. A falling edge is also input to the KR01 and KR05 pins after a falling edge is input to the KR00 pin (when KREG is 0). The KRF1 bit is set when the KRF0 bit is cleared. A key interrupt is generated 1 PCLKB clock cycle, after the KRF0 bit is cleared. See [1] in Figure 20.5. Also, after a falling edge is input to the KR05 pin, the KRF5 bit is set. The KRF1 bit is cleared at time [2] in the figure. A key interrupt is generated 1 PCLKB clock cycle, after the KRF1 bit is cleared. See [3] in the figure. It is therefore possible to generate a key interrupt when a valid edge is input to multiple channels.

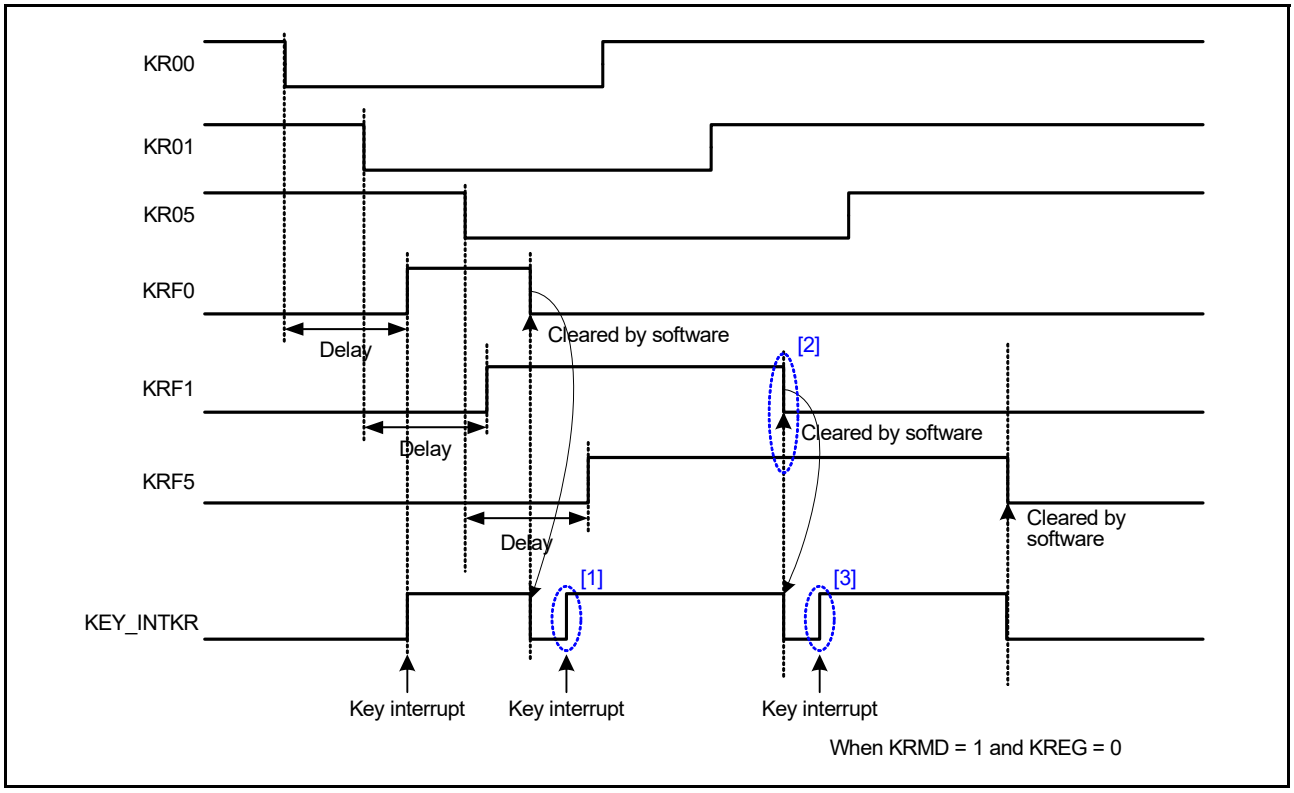


Figure 20.5 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

20.4 Usage Notes

- If KEY_INTKR is used as the snooze request, the KRMD bit must be set to 0.
- If KEY_INTKR is used as the interrupt source for returning to Normal mode from Snooze mode and Software Standby mode, the KRMD bit must be set to 1.
- When the Key Interrupt function (KINT) is assigned to a pin, this pin input is always enabled in Software Standby mode, and if the pin level changes, the associated KRFn flag can be set. Therefore, a key interrupt might occur on canceling Software Standby mode.

To ignore changes to the key interrupt pin during a software standby, clear the associated KRM bit before entering Software Standby mode. After canceling Software Standby mode, you must clear KRFn before the associated KRM bit can be set.

21. Port Output Enable for GPT (POEG)

21.1 Overview

The Port Output Enable for GPT (POEG) function can place the General PWM Timer (GPT) output pins in the output-disable state in one of the following ways:

- Input level detection of the GTETRGn (n = A, B, C, D) pins
- Output-disable request from the GPT
- Comparator interrupt request detection
- Oscillation stop detection of the clock generation circuit
- Register settings.

The GTETRGn (n = A, B, C, D) pins can also be used as GPT external trigger input pins.

Table 21.1 lists the POEG specifications, Figure 21.1 shows a block diagram, and Table 21.2 lists the input pins.

Table 21.1 POEG specifications

Parameter	Specifications
Output-disable control through input level detection	The GPT output pins can be disabled when a GTETRGn rising edge or high level is sampled after polarity and filter selection
Output-disable request from the GPT	• When the GTIOCA and the GTIOCB pins are driven to an active level simultaneously, the GPT generates an output-disable request to the POEG.Through reception of these requests, the POEG can control whether the GTIOCA and GTIOCB pins are output-disabled. • GPT output pins can be disabled when the GPT output pins detect a dead time error.
Output-disable control through comparator (ACMPHS) interrupt detection	The GPT output pins can be disabled when an interrupt request is generated by a change in the output results of any of the comparators
Output-disable control through oscillation stop detection	The GPT output pins can be disabled when oscillation of the clock generation circuit stops
Output-disable control by software (registers)	The GPT output pins can be disabled by modifying the register settings
Interrupts	• Allows output-disable control by the input level detection • Allows output-disable requests from the GPT or ACMPHS.
External trigger output to the GPT (count start, count stop, count clear, up-count, down-count, or input capture function)	The GTETRGn signals can be output to the GPT after polarity and filter selection
Noise filtering	• Three times sampling for every PCLKB/1, PCLKB/8, PCLKB/32, or PCLKB/128 can be set for any of the input pins GTETRGn • Positive or negative polarity can be selected for any of the input pins GTETRGn • Signal state after polarity and filter selection can be monitored.

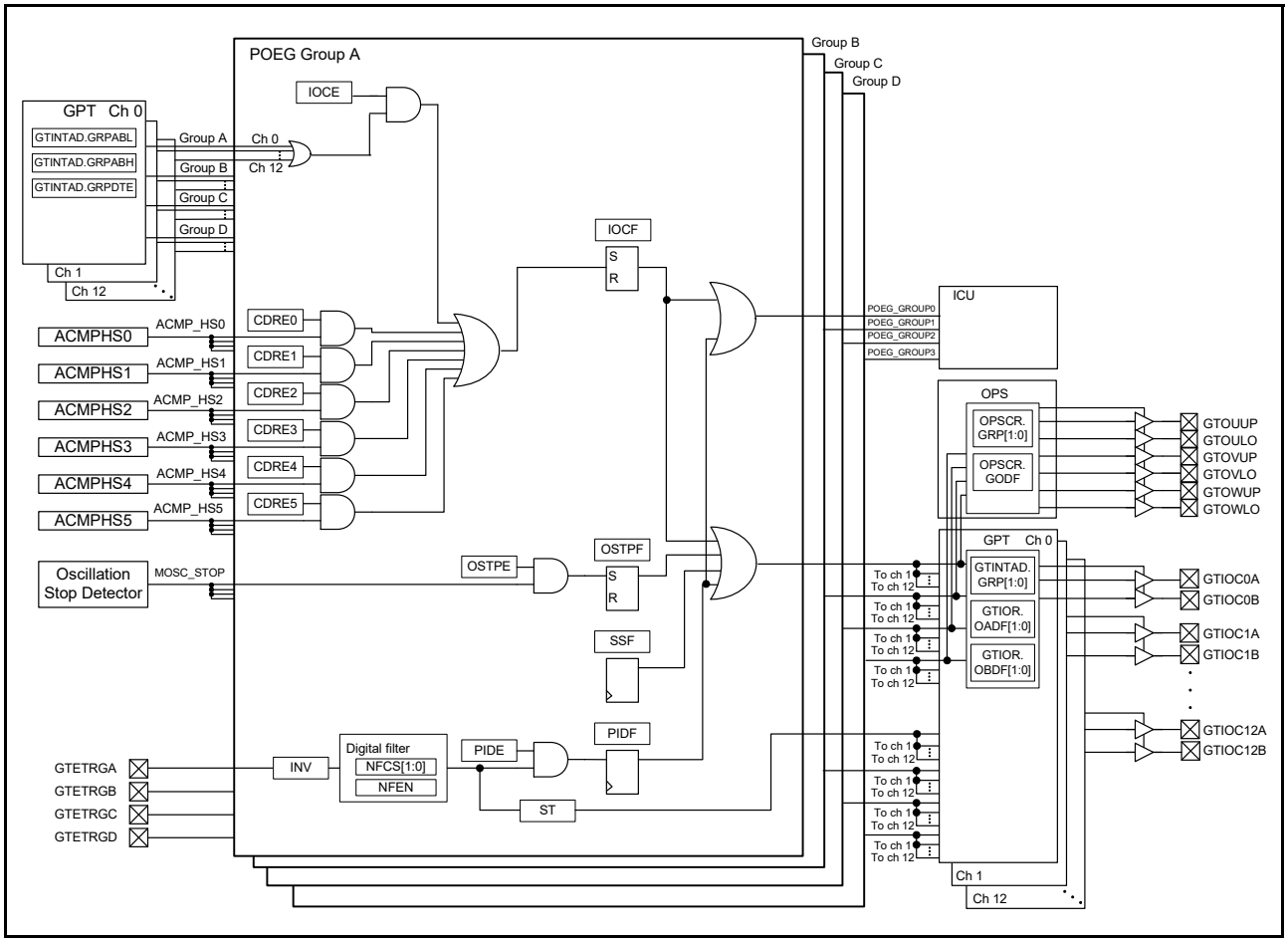


Figure 21.1 POEG block diagram

Table 21.2 POEG input pins

Pin name	I/O	Description
GTETRGA	Input	GPT output pin output-disable request signal and GPT external trigger input pin A
GTETRGB	Input	GPT output pin output-disable request signal and GPT external trigger input pin B
GTETRGC	Input	GPT output pin output-disable request signal and GPT external trigger input pin C
GTETRGD	Input	GPT output pin output-disable request signal and GPT external trigger input pin D

21.2 Register Descriptions

21.2.1 POEG Group n Setting Register (POEGGn) (n = A to D)

Address(es): POEG.POEGGA 4004 2000h, POEG.POEGGB 4004 2100h, POEG.POEGGC 4004 2200h, POEG.POEGGD 4004 2300h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CDRE5	CDRE4	CDRE3	CDRE2	CDRE1	CDRE0	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIDF	Port Input Detection Flag	0: No output-disable request from the GTETRGn pin occurred 1: Output-disable request from the GTETRGn pin occurred.	R(/W)*1
b1	IOCF	Detection Flag for GPT or ACMPHS Output-Disable Request	0: No output-disable request from the GPT disable request or the ACMPHS occurred 1: Output-disable request from the GPT disable request or the ACMPHS occurred.	R(/W)*1
b2	OSTPF	Oscillation Stop Detection Flag	0: No output-disable request from the oscillation stop detection occurred 1: Output-disable request from the oscillation stop detection occurred.	R(/W)*1
b3	SSF	Software Stop Flag	0: No output-disable request from software occurred 1: Output-disable request from software occurred.	R/W
b4	PIDE	Port Input Detection Enable	0: Output-disable requests from the GTETRGn pins disabled 1: Output-disable requests from the GTETRGn pins enabled.	R/W*2
b5	IOCE	Enable for GPT Output-Disable Request	0: Output-disable requests from the GPT disable request disabled 1: Output-disable requests from the GPT disable request enabled.	R/W*2
b6	OSTPE	Oscillation Stop Detection Enable	0: Output-disable requests from the oscillation stop detection disabled 1: Output-disable requests from the oscillation stop detection enabled.	R/W*2
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	CDRE0	ACMP_HS0 Enable	0: Comparator 0 disable requests disabled 1: Comparator 0 disable requests enabled.	R/W*2
b9	CDRE1	ACMP_HS1 Enable	0: Comparator 1 disable requests disabled 1: Comparator 1 disable requests enabled.	R/W*2
b10	CDRE2	ACMP_HS2 Enable	0: Comparator 2 disable requests disabled 1: Comparator 2 disable requests enabled.	R/W*2
b11	CDRE3	ACMP_HS3 Enable	0: Comparator 3 disable requests disabled 1: Comparator 3 disable requests enabled.	R/W*2
b12	CDRE4	ACMP_HS4 Enable	0: Comparator 4 disable requests disabled 1: Comparator 4 disable requests enabled.	R/W*2
b13	CDRE5	ACMP_HS5 Enable	0: Comparator 5 disable requests disabled 1: Comparator 5 disable requests enabled.	R/W*2
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	ST	GTETRGn Input Status Flag	0: GTETRGn input after filtering is 0 1: GTETRGn input after filtering is 1.	R
b27 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b28	INV	GTETRGn Input Reverse	0: Input GTETRGn as-is 1: Input GTETRGn reversed.	R/W
b29	NFEN	Noise Filter Enable	0: Noise filtering disabled 1: Noise filtering enabled.	R/W
b31, b30	NFCS[1:0]	Noise Filter Clock Select	b1 b0 0 0: GTETRGn pin input level sampled three times every PCLKB 0 1: GTETRGn pin input level sampled three times every PCLKB/8 1 0: GTETRGn pin input level sampled three times every PCLKB/32 1 1: GTETRGn pin input level sampled three times every PCLKB/128.	R/W

Note 1. Only 0 can be written to clear the flag.
Note 2. Can be modified only once after a reset.

The POEGGA to POEGGD registers control the output-disable state of the GPT pins, interrupts, and the external trigger input to the GPT. In the descriptions, POEGGn represents all of the POEGGA to POEGGD registers.

21.3 Output-Disable Control Operation

If any of the following conditions is satisfied, the GTIOCxA, GTIOCxB, and the 3-phase PWM output for BLDC motor control pins can be set to output-disable:

- Input level or edge detection of the GTETRGn pins
  When POEGGn.PIDE is 1, the POEGGn.PIDF flag is set to 1.
- Output-disable request from the GPT
  When POEGGn.IOCE is 1, the POEGGn.IOCF flag is set to 1 if the disable request is enabled in the GTINTAD register. The GTINTAD.GRPDTE, GTINTAD.GRPABH, and GTINTAD.GRPABL settings apply to the group selected in the GPT registers GTINTAD.GRP[1:0] and OPSCR.GRP[1:0].
- Comparator (ACMPHS) interrupt request detection
  Comparator interrupt detection is activated when any of the POEGGn.CDRE[5:0] registers is 1. When the associated comparator interrupt is generated, the GPT output pins are disabled. POEGGn.IOCF indicates the detection status.
- Oscillation stop detection for the clock generation circuit
  When POEGGn.OSTPE is 1, the POEGGn.OSTPF flag is set to 1.
- SSF bit setting
  When POEGGn.SSF is set to 1, the PWM output is disabled.

The output-disable state is controlled in the GPT. The output-disable of the GTIOCxA and GTIOCxB pins is set in the GTINTAD.GRP[1:0], GTIOR.OADF[1:0], and GTIOR.OBDF[1:0] bits in GPTx. The output-disable of the 3-phase PWM output for the BLDC motor control pins is set in the OPSCR.GRP[1:0] bits and OPSCR.GODF bit in GPT_OPS.

21.3.1 Pin Input Level Detection Operation

If the input conditions set in POEGGn.PIDE, POEGGn.NFCS[1:0], POEGGn.NFEN, and POEGGn.INV occur on the GTETRGn pins, the GPT output pins are output-disabled.

21.3.1.1 Digital filter

Figure 21.2 shows high level detection by the digital filter. When a high level associated with the POEGGn.INV polarity setting is detected three times consecutively with the sampling clock selected in POEGGn.NFCS[1:0] and POEGGn.NFEN, the detected level is recognized as high, and the GPT output pins are output-disabled. If even one low level is detected during this interval, the detected level is not recognized as high. In addition, in an interval where the sampling clock is not output, changes of the levels on the GTETRGn pins are ignored.

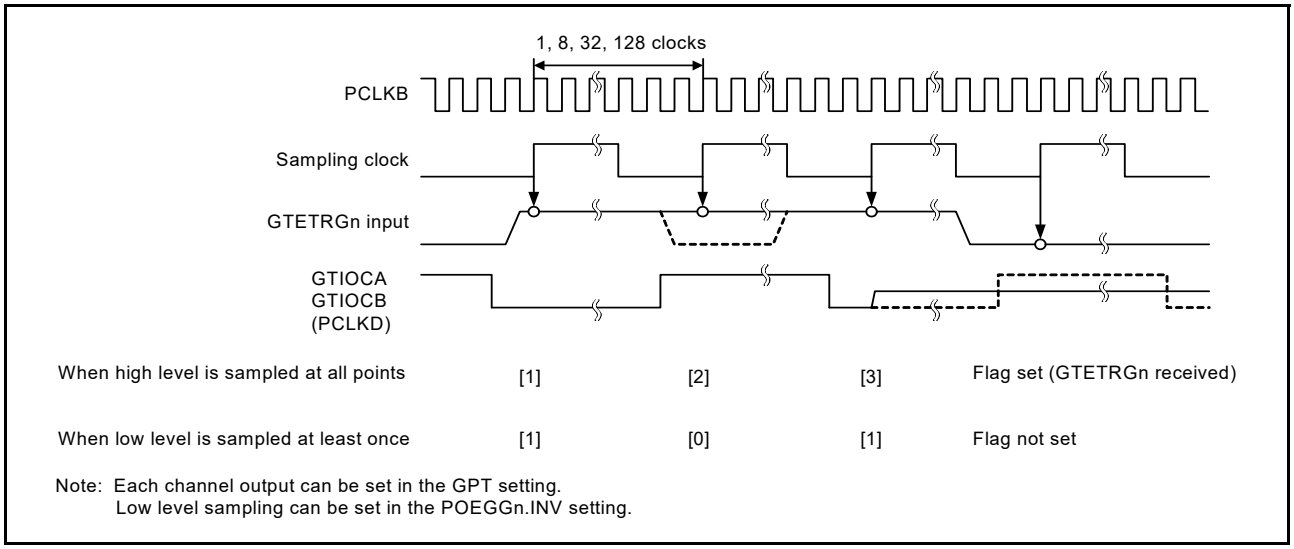


Figure 21.2 Example of digital filter operation

21.3.2 Output-Disable Requests from the GPT

For details on the operation, see the description for GTIOC Pin Output Negate Control in section 22, General PWM Timer (GPT).

21.3.3 Comparator Interrupt Detection

If POEGGn.CDRE[5:0] is 1 when the associated comparator interrupt request is generated, the GPT output pins are output-disabled for each group. The status flag is POEGGn.IOCF, which is shared with GPT output-disable detection.

21.3.4 Output-Disable Control Using Detection of Stopped Oscillation

When the oscillation stop detection function in the clock generation circuit detects stopped oscillation while POEGGn.OSTPE is 1, the GPT output pins are output-disabled for each group.

21.3.5 Output-Disable Control Using Registers

The GPT output pins can be directly controlled by writing to the Software Stop flag, POEGGn.SSF.

21.3.6 Release from Output-Disable

To release the GPT output pins in the output-disabled state, either return them to their initial state with a reset or clear all of the following flags:

- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF.

Writing 0 to the POEGGn.PIDF flag is ignored (the flag is not cleared) if the external input pins, GTETRGn, are not disabled and the POEGGn.ST bit is not set to 0.

Writing 0 to the POEGGn.IOCF flag is valid (the flag is cleared) only if all of the GTST.DTEF, GTST.OABHF, and GTST.OABLF flags in the GPT are set to 0.

Writing 0 to the POEGGn.OSTPF flag is ignored (the flag is not cleared) if the OSTDSR.OSTDF flag in the clock generation circuit is not set to 0. In addition, when the flag set and release occur at the same time, the flag set takes precedence.

Figure 21.3 shows the release timing for output-disable. The output-disable is released at the beginning of the next count cycle of the GPT after the flag is cleared.

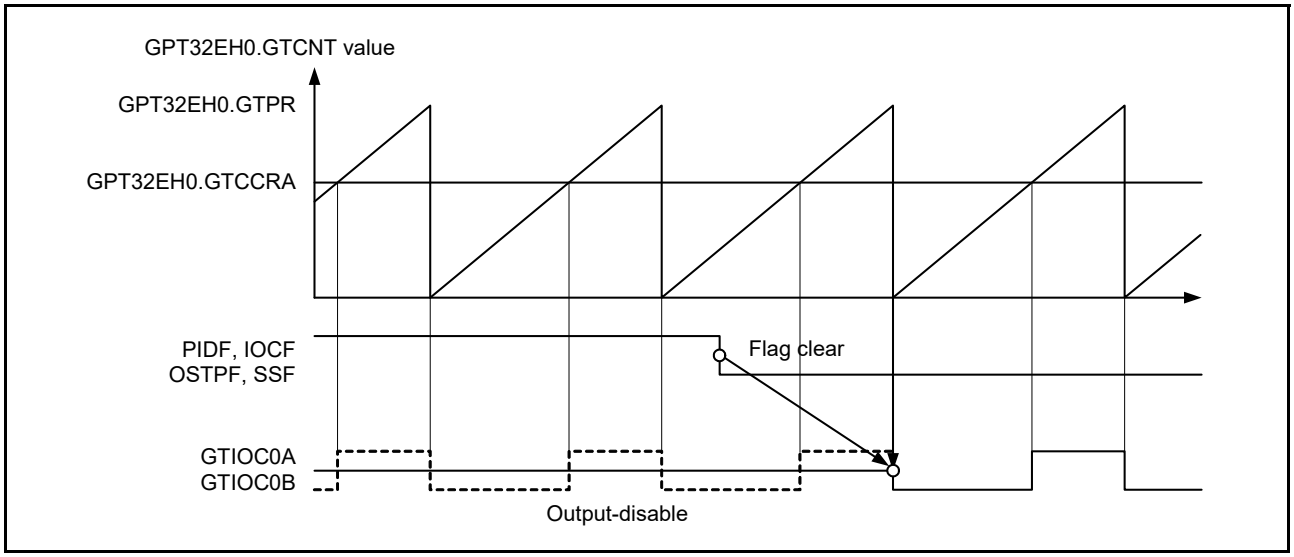


Figure 21.3 Output-disable release timing for the GPT pin outputs

21.4 Interrupt Sources

The POEG generates an interrupt request when triggered by these sources:

- Output-disable control by the input level detection
- Output-disable request from the GPT
- Output-disable request from the comparator interrupt request detection.

Table 21.3 lists the conditions for interrupt requests.

Table 21.3 Interrupt sources and conditions

Interrupt source	Symbol	Associated flag	Trigger conditions
POEG group A interrupt	POEG_GROUP0	POEGGA.IOCF	An output-disable request from a GPT disable request occurred
			An output-disable request from a comparator interrupt request occurred
		POEGGA.PIDF	An output-disable request from the GTETRGA pin occurred
POEG group B interrupt	POEG_GROUP1	POEGGB.IOCF	An output-disable request from a GPT disable request occurred
			An output-disable request from a comparator interrupt request occurred
		POEGGB.PIDF	An output-disable request from the GTETRGB pin occurred
POEG group C interrupt	POEG_GROUP2	POEGGC.IOCF	An output-disable request from a GPT disable request occurred
			An output-disable request from a comparator interrupt request occurred
		POEGGC.PIDF	An output-disable request from the GTETRGC pin occurred
POEG group D interrupt	POEG_GROUP3	POEGGD.IOCF	An output-disable request from a GPT disable request occurred
			An output-disable request from a comparator interrupt request occurred
		POEGGD.PIDF	An output-disable request from the GTETRGD pin occurred

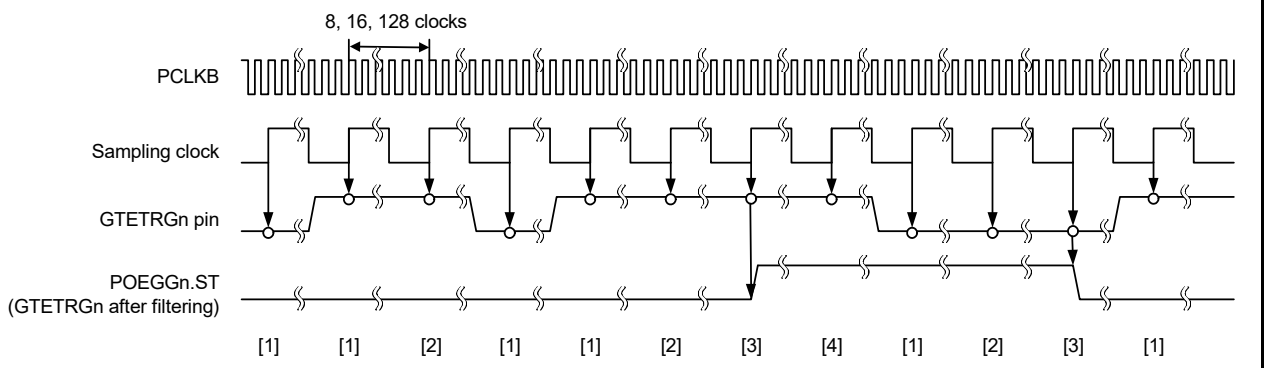
21.5 External Trigger Output to the GPT

The POEG outputs the GTETRGn signals as the GPT operation trigger signal for the following:

- Count start
- Count stop
- Count clear
- Up-count
- Down-count
- Input capture.

For the POEGGn.INV polarity setting signal, when the same level is input three times continuously with the sampling clock selected in POEGGn.NFCS[1:0] and POEGGn.NFEN, that value is output. Set the control registers the same as for the input level detection operation described in section 21.3.1, Pin Input Level Detection Operation. The state after filtering can be monitored in POEGGn.ST.

Figure 21.4 shows the output timing of an external trigger to the GPT.



Note: Each channel output can be set in the GPT settings.
Polarity can be reversed in the POEGGn.INV setting.

Figure 21.4 Output timing of external trigger to the GPT

21.6 Usage Notes

21.6.1 Transition to Software Standby Mode

When using the POEG, do not invoke Software Standby mode. In this mode, the POEG stops and therefore output-disable of the pins cannot be controlled.

21.6.2 Specifying Pins Associated with the GPT

The POEG controls output-disable only when a pin is associated with the GPT in the PmnPFS.PMR and PmnPFS.PSEL[4:0] settings. When the pin is specified as a general I/O pin, the POEG does not perform output-disable control.

22. General PWM Timer (GPT)

22.1 Overview

The General PWM Timer (GPT) is a 32-bit timer with four GPT32EH channels, four GPT32E channels, and five GPT32 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.

Table 22.1 lists the GPT specifications, Table 22.2 shows the GPT functions, and Figure 22.1 shows a block diagram.

Table 22.1 GPT specifications

Parameter	Specifications
Functions	• 32 bits × 13 channels • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms • Registers for setting up frame cycles in each channel with capability for generating interrupts at overflow or underflow • Generation of dead times in PWM operation • Synchronous starting, stopping, and clearing counters for arbitrary channels • Starting, stopping, and clearing up/down counters in response to a maximum of eight ELC events • Starting, stopping, and clearing up/down counters in response to input level comparison • Starting, stopping, and clearing up/down counters in response to a maximum of four external triggers • Output pin disable function by dead time error and detected short-circuits between output pins • A/D converter start triggers can be generated • PWM waveform for controlling brushless DC motors can be generated • Compare match A to F event, overflow/underflow event, and input UVW edge event can be output to the ELC • Enables the noise filter for input capture and input UVW • Bus clock: PCLKA • Core clock: PCLKD • Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64).

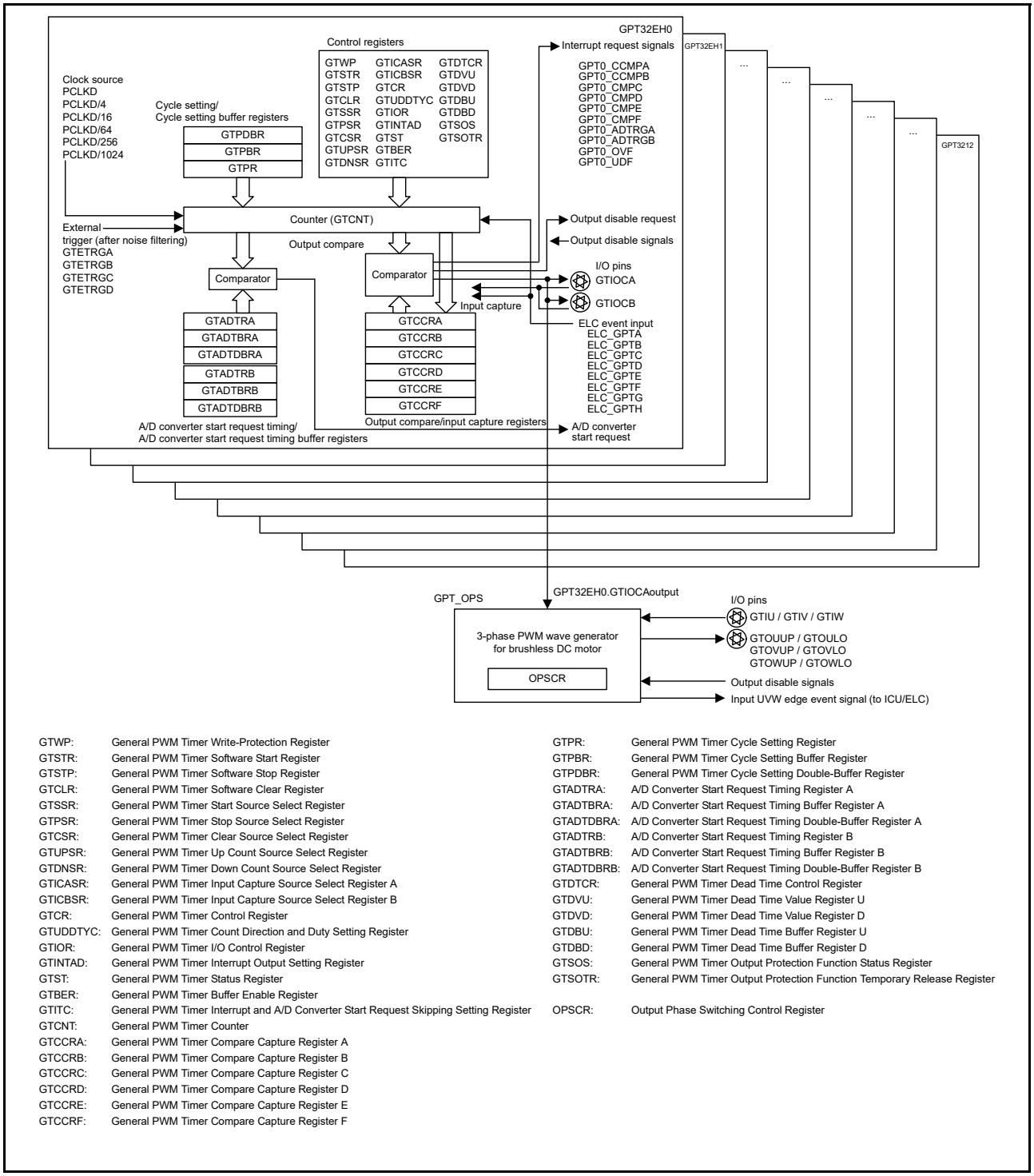
Table 22.2 GPT functions (1 of 2)

Parameter	GPT32EH, GPT32E	GPT32
Count clock	PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024	PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024
Output compare/input capture registers (GTCCR)	GTCCRA GTCCRB	GTCCRA GTCCRB
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register	GTPR	GTPR
Cycle setting buffer registers	GTPBR GTPDBR	GTPBR
I/O pins	GTIOCA GTIOCB	GTIOCA GTIOCB

Table 22.2 GPT functions (2 of 2)

Parameter		GPT32EH, GPT32E	GPT32
External trigger input pin*1		GTETRGA GTETRGB GTETRGC GTETRGD	GTETRGA GTETRGB GTETRGC GTETRGD
Counter clear sources		GTPR register compare match, input capture, input pin status, ELC event input, and GTETRGn (n = A, B, C, D) pin input	GTPR register compare match, input capture, input pin status, ELC event input, and GTETRGn (n = A, B, C, D) pin input
Compare match output	Low output	Available	Available
	High output	Available	Available
	Toggle output	Available	Available
Input capture function		Available	Available
Automatic addition of dead time		Available	Available (no dead time buffer)
PWM mode		Available	Available
Phase count function		Available	Available
Buffer operation		Double buffer	Double buffer
One-shot operation		Available	Available
DTC activation		All the interrupt sources	All the interrupt sources
A/D converter start trigger		Compare match of GTADTRA or GTADTRB	-
Brushless DC motor control function		Available	Available
Interrupt sources		10 sources • GTCCRA compare match/input capture (GPTn_CCMPA) • GTCCRB compare match/input capture (GPTn_CCMPB) • GTCCRC compare match (GPTn_CMPC) • GTCCRD compare match (GPTn_CMPD) • GTCCRE compare match (GPTn_CMPCE) • GTCCRF compare match (GPTn_CMPF) • GTADTRA compare match (GPTn_ADTRGA) • GTADTRB compare match (GPTn_ADTRGB) • GTCNT overflow (GTPR compare match) (GPTn_OVF) • GTCNT underflow (GPTn_UDF)	8 sources • GTCCRA compare match/input capture (GPTn_CCMPA) • GTCCRB compare match/input capture (GPTn_CCMPB) • GTCCRC compare match (GPTn_CMPC) • GTCCRD compare match (GPTn_CMPD) • GTCCRE compare match (GPTn_CMPE) • GTCCRF compare match (GPTn_CMPF) • GTCNT overflow (GTPR compare match) (GPTn_OVF) • GTCNT underflow (GPTn_UDF)
Interrupt skipping function		Skips GTCNT overflows (GTPR compare match) (GPTn_OVF)/ GTCNT underflow (GPTn_UDF) interrupts (with interlocking function for other interrupts or A/D conversion requests)	-
Event linking (ELC) function		Available	Available
Noise filtering function		Available	Available

Note 1. GTRETRGn connects to GPT through the POEG module. Therefore, to use the GPT function, supply the POEG clock by clearing the MSTPD14 bit.



GTWP: General PWM Timer Write-Protection Register
GTSTR: General PWM Timer Software Start Register
GTSTP: General PWM Timer Software Stop Register
GTCLR: General PWM Timer Software Clear Register
GTSSR: General PWM Timer Start Source Select Register
GTPSR: General PWM Timer Stop Source Select Register
GTCSR: General PWM Timer Clear Source Select Register
GTUPSR: General PWM Timer Up Count Source Select Register
GTDNSR: General PWM Timer Down Count Source Select Register
GTICASR: General PWM Timer Input Capture Source Select Register A
GTICBSR: General PWM Timer Input Capture Source Select Register B
GTCR: General PWM Timer Control Register
GTUDDTYC: General PWM Timer Count Direction and Duty Setting Register
GTIOR: General PWM Timer I/O Control Register
GTINTAD: General PWM Timer Interrupt Output Setting Register
GTST: General PWM Timer Status Register
GTBER: General PWM Timer Buffer Enable Register
GTITC: General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register
GTCNT: General PWM Timer Counter
GTCCRA: General PWM Timer Compare Capture Register A
GTCCRB: General PWM Timer Compare Capture Register B
GTCCRC: General PWM Timer Compare Capture Register C
GTCCRD: General PWM Timer Compare Capture Register D
GTCCRE: General PWM Timer Compare Capture Register E
GTCCRF: General PWM Timer Compare Capture Register F

GTPR: General PWM Timer Cycle Setting Register
GTPBR: General PWM Timer Cycle Setting Buffer Register
GTPDBR: General PWM Timer Cycle Setting Double-Buffer Register
GTADTRA: A/D Converter Start Request Timing Register A
GTADTBRA: A/D Converter Start Request Timing Buffer Register A
GTADTDBRA: A/D Converter Start Request Timing Double-Buffer Register A
GTADTRB: A/D Converter Start Request Timing Register B
GTADTBRB: A/D Converter Start Request Timing Buffer Register B
GTADTDBRB: A/D Converter Start Request Timing Double-Buffer Register B
GTDTCR: General PWM Timer Dead Time Control Register
GTDVU: General PWM Timer Dead Time Value Register U
GTDVD: General PWM Timer Dead Time Value Register D
GTDBU: General PWM Timer Dead Time Buffer Register U
GTDBD: General PWM Timer Dead Time Buffer Register D
GTSOS: General PWM Timer Output Protection Function Status Register
GTSOTR: General PWM Timer Output Protection Function Temporary Release Register

OPSCR: Output Phase Switching Control Register

Figure 22.1 GPT block diagram

Figure 22.2 shows an example using multiple GPTs.

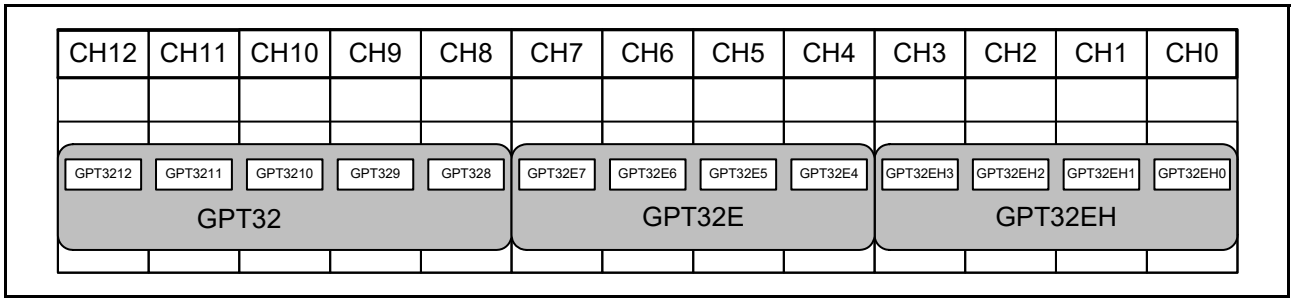


Figure 22.2 Association between GPT channels and module names

Table 22.3 lists the I/O pins.

Table 22.3 GPT I/O pins (1 of 2)

Channel	Pin name	I/O	Function
Shared	GTETRGA	Input	External trigger input pin A (after noise filtering)
	GTETRGB	Input	External trigger input pin B (after noise filtering)
	GTETRGC	Input	External trigger input pin C (after noise filtering)
	GTETRGD	Input	External trigger input pin D (after noise filtering)
GPT32EH0	GTIOC0A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC0B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32EH1	GTIOC1A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC1B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32EH2	GTIOC2A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC2B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32EH3	GTIOC3A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC3B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32E4	GTIOC4A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC4B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32E5	GTIOC5A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC5B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32E6	GTIOC6A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC6B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32E7	GTIOC7A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC7B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT328	GTIOC8A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC8B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT329	GTIOC9A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC9B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT3210	GTIOC10A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC10B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT3211	GTIOC11A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC11B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT3212	GTIOC12A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC12B	I/O	GTCCRB register input capture input/output compare output/PWM output pin

Table 22.3 GPT I/O pins (2 of 2)

Channel	Pin name	I/O	Function
GPT_OPS	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)

22.2 Register Descriptions

Table 22.4 lists the registers in the GPT.

Table 22.4 GPT registers (1 of 2)

Module symbol	Register name	Register symbol	Reset value	Address (m = 0 to 12)	Access size	GPT32EH/ GPT32E	GPT32
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7) GPT32m (m = 8 to 12)	General PWM Timer Write Protection Register	GTWP	0000 0000h	4007 8000h + 0100h × m	32	✓	✓
	General PWM Timer Software Start Register	GTSTR	0000 0000h	4007 8004h + 0100h × m	32	✓	✓
	General PWM Timer Software Stop Register	GTSTP	FFFF FFFFh	4007 8008h + 0100h × m	32	✓	✓
	General PWM Timer Software Clear Register	GTCLR	0000 0000h	4007 800Ch + 0100h × m	32	✓	✓
	General PWM Timer Start Source Select Register	GTSSR	0000 0000h	4007 8010h + 0100h × m	32	✓	✓
	General PWM Timer Stop Source Select Register	GTPSR	0000 0000h	4007 8014h + 0100h × m	32	✓	✓
	General PWM Timer Clear Source Select Register	GTCSR	0000 0000h	4007 8018h + 0100h × m	32	✓	✓
	General PWM Timer Up Count Source Select Register	GTUPSR	0000 0000h	4007 801Ch + 0100h × m	32	✓	✓
	General PWM Timer Down Count Source Select Register	GTDNSR	0000 0000h	4007 8020h + 0100h × m	32	✓	✓
	General PWM Timer Input Capture Source Select Register A	GTICASR	0000 0000h	4007 8024h + 0100h × m	32	✓	✓
	General PWM Timer Input Capture Source Select Register B	GTICBSR	0000 0000h	4007 8028h + 0100h × m	32	✓	✓
	General PWM Timer Control Register	GTCR	0000 0000h	4007 802Ch + 0100h × m	32	✓	✓
	General PWM Timer Count Direction and Duty Setting Register	GTUDDTYC	0000 0001h	4007 8030h + 0100h × m	32	✓	✓
	General PWM Timer I/O Control Register	GTIOR	0000 0000h	4007 8034h + 0100h × m	32	✓	✓
	General PWM Timer Interrupt Output Setting Register	GTINTAD	0000 0000h	4007 8038h + 0100h × m	32	✓	(✓)*1
	General PWM Timer Status Register	GTST	0000 8000h	4007 803Ch + 0100h × m	32	✓	(✓)*1
	General PWM Timer Buffer Enable Register	GTBER	0000 0000h	4007 8040h + 0100h × m	32	✓	(✓)*1
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7)	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	0000 0000h	4007 8044h + 0100h × m	32	✓	-

Table 22.4 GPT registers (2 of 2)

Module symbol	Register name	Register symbol	Reset value	Address (m = 0 to 12)	Access size	GPT32EH/ GPT32E	GPT32
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7) GPT32m (m = 8 to 12)	General PWM Timer Counter	GTCNT	0000 0000h	4007 8048h + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register A	GTCCRA	FFFF FFFFh	4007 804Ch + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register B	GTCCRB	FFFF FFFFh	4007 8050h + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register C	GTCCRC	FFFF FFFFh	4007 8054h + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register E	GTCCRE	FFFF FFFFh	4007 8058h + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register D	GTCCRD	FFFF FFFFh	4007 805Ch + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register F	GTCCRF	FFFF FFFFh	4007 8060h + 0100h × m	32	✓	✓
	General PWM Timer Cycle Setting Register	GTPR	FFFF FFFFh	4007 8064h + 0100h × m	32	✓	✓
	General PWM Timer Cycle Setting Buffer Register	GTPBR	FFFF FFFFh	4007 8068h + 0100h × m	32	✓	✓
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7)	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	FFFF FFFFh	4007 806Ch + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Register A	GTADTRA	FFFF FFFFh	4007 8070h + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	FFFF FFFFh	4007 8074h + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	FFFF FFFFh	4007 8078h + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Register B	GTADTRB	FFFF FFFFh	4007 807Ch + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	FFFF FFFFh	4007 8080h + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	FFFF FFFFh	4007 8084h + 0100h × m	32	✓	-
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7) GPT32m (m = 8 to 12)	General PWM Timer Dead Time Control Register	GTDTCR	0000 0000h	4007 8088h + 0100h × m	32	✓	(✓)*1
	General PWM Timer Dead Time Value Register U	GTDVU	FFFF FFFFh	4007 808Ch + 0100h × m	32	✓	✓
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7)	General PWM Timer Dead Time Value Register D	GTDVD	FFFF FFFFh	4007 8090h + 0100h × m	32	✓	-
	General PWM Timer Dead Time Buffer Register U	GTDBU	FFFF FFFFh	4007 8094h + 0100h × m	32	✓	-
	General PWM Timer Dead Time Buffer Register D	GTDBD	FFFF FFFFh	4007 8098h + 0100h × m	32	✓	-
	General PWM Timer Output Protection Function Status Register	GTSOS	0000 0000h	4007 809Ch + 0100h × m	32	✓	-
	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	0000 0000h	4007 80A0h + 0100h × m	32	✓	-
GPT_OPS	Output Phase Switching Control Register	OPSCR	0000 0000h	4007 8FF0h	32	✓	✓

Note 1. Some functions are reduced from GPT32EH/GPT32E.

22.2.1 General PWM Timer Write Protection Register (GTWP)

Address(es): GPT32EHm.GTWP 4007 8000h + 0100h × m (m = 0 to 3)
GPT32Em.GTWP 4007 8000h + 0100h × m (m = 4 to 7)
GPT32m.GTWP 4007 8000h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	—	—	—	WP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	WP	Register Write Disable	0: Write to the register enabled 1: Write to the register disabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	GTWP Key Code	When A5h is written to these bits, writes to the WP bit are permitted. These bits are read as 0.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

To prevent accidental modification, the GTWP register enables or disables writing to following registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR.

22.2.2 General PWM Timer Software Start Register (GTSTR)

Address(es): GPT32EHm.GTSTR 4007 8004h + 0100h × m (m = 0 to 3)
GPT32Em.GTSTR 4007 8004h + 0100h × m (m = 4 to 7)
GPT32m.GTSTR 4007 8004h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CSTRT 12	CSTRT 11	CSTRT 10	CSTRT 9	CSTRT 8	CSTRT 7	CSTRT 6	CSTRT 5	CSTRT 4	CSTRT 3	CSTRT 2	CSTRT 1	CSTRT 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The GTSTR starts the GTCNT counter operation for each channel n, where n = 0 to 12.

The GTSTR bit number represents the channel number. The GTSTR register is shared by all of the channels. The GTCNT counter starts for the channel associated with the GTSTR bit where 1 is written. Writing 0 has no effect on the status of the GTCNT counter and the value of GTSTR register.

For the association between the GTSTR bit number and a channel number, see Figure 22.2.

CSTRT[12:0] bits (Channel n GTCNT Count Start) (n = 0 to 12)

The CSTRT[12:0] bits start channel n of the GTCNT counter operation. Writing to the GTSTR.CSTRTn bit (n = 0 to 12) has no effect unless the GPTm.GTSSR.CSTRT bit is set to 1 (for GPT32EH, m = 0 to 3, for GPT32E, m = 4 to 7, for GPT32, m = 8 to 12). The read data shows the counter status of each channel (GTCR.CST bit). Zero means the counter is stopped and 1 means the counter is running.

22.2.3 General PWM Timer Software Stop Register (GTSTP)

Address(es): GPT32EHm.GTSTP 4007 8008h + 0100h × m (m = 0 to 3)
GPT32Em.GTSTP 4007 8008h + 0100h × m (m = 4 to 7)
GPT32m.GTSTP 4007 8008h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CSTOP 12	CSTOP 11	CSTOP 10	CSTOP 9	CSTOP 8	CSTOP 7	CSTOP 6	CSTOP 5	CSTOP 4	CSTOP 3	CSTOP 2	CSTOP 1	CSTOP 0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The GTSTP stops the GTCNT counter operation for each channel n, where n = 0 to 12.

The GTSTP bit number represents the channel number. The GTSTP register is shared by all of the channels. The GTCNT counter stops for the channel associated with the GTSTP bit where 1 is written. Writing 0 has no effect on the status of GTCNT counter and the value of GTSTP register. For the association between the GTSTP bit number and a channel number, see Figure 22.2.

CSTOPn bit (channel n GTCNT Count Stop) (n = 0 to 12)

The CSTOPn bit stops channel n of the GTCNT counter operation. Writing to the GTSTP.CSTOPn bit (n = 0 to 12) has no effect unless the GPTm.GTPSR.CSTOP bit is set to 1 (for GPT32EH, m = 0 to 3, for GPT32E, m = 4 to 7, for GPT32, m = 8 to 12).

Read data shows the counter status of each channel (invert of the GTCR.CST bit). Zero means the counter is running and 1 means the counter stops.

22.2.4 General PWM Timer Software Clear Register (GTCLR)

Address(es): GPT32EHm.GTCLR 4007 800Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCLR 4007 800Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCLR 4007 800Ch + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CCLR 12	CCLR 11	CCLR 10	CCLR 9	CCLR 8	CCLR 7	CCLR 6	CCLR 5	CCLR 4	CCLR 3	CCLR 2	CCLR 1	CCLR 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The GTCLR is a write-only register that clears the GTCNT counter operation for each channel n, where n = 0 to 12.

The GTCLR bit number represents the channel number. The GTCLR register is shared by all of the channels. The GTCNT counter is cleared for the channel associated with the GTCLR bit number where 1 is written. Writing 0 has no effect on the status of the GTCNT counter.

For the association between the GTCLR bit number and a channel number, see Figure 22.2.

CCLR[12:0] bits (Channel n GTCNT Count Clear) (n = 0 to 12)

Channel n of the GTCNT counter value is cleared on writing 1 to the CCLRn bit. This bit is read as 0.

22.2.5 General PWM Timer Start Source Select Register (GTSSR)

Address(es): GPT32EHm.GTSSR 4007 8010h + 0100h × m (m = 0 to 3)
GPT32Em.GTSSR 4007 8010h + 0100h × m (m = 4 to 7)
GPT32m.GTSSR 4007 8010h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	SSGTRGDF	SSGTRGDR	SSGTRGCF	SSGTRGCR	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSGTRGAR	GTETRGA Pin Rising Input Source Counter Start Enable	0: Counter start disabled on the rising edge of GTETRGA input 1: Counter start enabled on the rising edge of GTETRGA input.	R/W
b1	SSGTRGAF	GTETRGA Pin Falling Input Source Counter Start Enable	0: Counter start disabled on the falling edge of GTETRGA input 1: Counter start enabled on the falling edge of GTETRGA input.	R/W
b2	SSGTRGBR	GTETRGB Pin Rising Input Source Counter Start Enable	0: Counter start disabled on the rising edge of GTETRGB input 1: Counter start enabled on the rising edge of GTETRGB input.	R/W
b3	SSGTRGBF	GTETRGB Pin Falling Input Source Counter Start Enable	0: Counter start disabled on the falling edge of GTETRGB input 1: Counter start enabled on the falling edge of GTETRGB input.	R/W
b4	SSGTRGCR	GTETRGC Pin Rising Input Source Counter Start Enable	0: Counter start disabled on the rising edge of GTETRGC input 1: Counter start enabled on the rising edge of GTETRGC input.	R/W
b5	SSGTRGCF	GTETRGC Pin Falling Input Source Counter Start Enable	0: Counter start disabled on the falling edge of GTETRGC input 1: Counter start enabled on the falling edge of GTETRGC input	R/W
b6	SSGTRGDR	GTETRGD Pin Rising Input Source Counter Start Enable	0: Counter start disabled on the rising edge of GTETRGD input 1: Counter start enabled on the rising edge of GTETRGD input.	R/W
b7	SSGTRGDF	GTETRGD Pin Falling Input Source Counter Start Enable	0: Counter start disabled on the falling edge of GTETRGD input 1: Counter start enabled on the falling edge of GTETRGD input.	R/W
b8	SSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Start Enable	0: Counter start disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: Counter start enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	SSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Start Enable	0: Counter start disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: Counter start enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	SSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Start Enable	0: Counter start disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: Counter start enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b11	SSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Start Enable	0: Counter start disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: Counter start enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	SSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Start Enable	0: Counter start disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: Counter start enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	SSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Start Enable	0: Counter start disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: Counter start enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	SSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Start Enable	0: Counter start disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Counter start enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	SSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Start Enable	0: Counter start disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter start enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	SSELCA	ELC_GPTA Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTA event input 1: Counter start enabled at the ELC_GPTA event input.	R/W
b17	SSELCB	ELC_GPTB Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTB event input 1: Counter start enabled at the ELC_GPTB event input.	R/W
b18	SSELCC	ELC_GPTC Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTC event input 1: Counter start enabled at the ELC_GPTC event input.	R/W
b19	SSELCD	ELC_GPTD Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTD event input 1: Counter start enabled at the ELC_GPTD event input.	R/W
b20	SSELCE	ELC_GPTE Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTE event input 1: Counter start enabled at the ELC_GPTE event input.	R/W
b21	SSELCF	ELC_GPTF Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTF event input 1: Counter start enabled at the ELC_GPTF event input.	R/W
b22	SSELCG	ELC_GPTG Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTG event input 1: Counter start enabled at the ELC_GPTG event input.	R/W
b23	SSELCH	ELC_GPTH Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTH event input 1: Counter start enabled at the ELC_GPTH event input.	R/W
b30 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CSTRT	Software Source Counter Start Enable	0: Counter start disabled by the GTSTR register 1: Counter start enabled by the GTSTR register.	R/W

The GTSSR sets the source to start the GTCNT counter.

SSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Start Enable)

The SSGTRGAR bit enables or disables the GTCNT counter start on the rising edge of GTETRGA pin input.

SSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Start Enable)

The SSGTRGAF bit enables or disables the GTCNT counter start on the falling edge of GTETRGA pin input.

SSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Start Enable)

The SSGTRGBR bit enables or disables the GTCNT counter start on the rising edge of GTETRGB pin input.

SSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Start Enable)

The SSGTRGBF bit enables or disables the GTCNT counter start on the falling edge of GTETRGB pin input.

SSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Start Enable)

The SSGTRGCR bit enables or disables the GTCNT counter start on the rising edge of GTETRGC pin input.

SSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Start Enable)

The SSGTRGCF bit enables or disables the GTCNT counter start on the falling edge of GTETRGC pin input.

SSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Start Enable)

The SSGTRGDR bit enables or disables the GTCNT counter start on the rising edge of GTETRGD pin input.

SSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Start Enable)

The SSGTRGDF bit enables or disables the GTCNT counter start on the falling edge of GTETRGD pin input.

SSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Start Enable)

The SSCARBL bit enables or disables the GTCNT counter start on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

SSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Start Enable)

The SSCARBH bit enables or disables the GTCNT counter start on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

SSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Start Enable)

The SSCAFBL bit enables or disables the GTCNT counter start on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

SSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Start Enable)

The SSCAFBH bit enables or disables the GTCNT counter start on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

SSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Start Enable)

The SSCBRAL bit enables or disables the GTCNT counter start on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

SSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Start Enable)

The SSCBRAH bit enables or disables the GTCNT counter start on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

SSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Start Enable)

The SSCBFAL bit enables or disables the GTCNT counter start on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

SSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Start Enable)

The SSCBFAH bit enables or disables the GTCNT counter start on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

SSELCm bit (ELC_GPTm Event Source Counter Start Enable) (m = A to H)

The SSELCm bit enables or disables the GTCNT counter start at the ELC_GPTm event input.

CSTRT bit (Software Source Counter Start Enable)

The CSTRT bit enables or disables the GTCNT counter start by the GTSTR register.

22.2.6 General PWM Timer Stop Source Select Register (GTPSR)

Address(es): GPT32EHm.GTPSR 4007 8014h + 0100h × m (m = 0 to 3)
GPT32Em.GTPSR 4007 8014h + 0100h × m (m = 4 to 7)
GPT32m.GTPSR 4007 8014h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	PSGTRGDF	PSGTRGDR	PSGTRGCF	PSGTRGCR	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PSGTRGAR	GTETRGA Pin Rising Input Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTETRGA input 1: Counter stop enabled on the rising edge of GTETRGA input.	R/W
b1	PSGTRGAF	GTETRGA Pin Falling Input Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTETRGA input 1: Counter stop enabled on the falling edge of GTETRGA input.	R/W
b2	PSGTRGBR	GTETRGB Pin Rising Input Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTETRGB input 1: Counter stop enabled on the rising edge of GTETRGB input.	R/W
b3	PSGTRGBF	GTETRGB Pin Falling Input Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTETRGB input 1: Counter stop enabled on the falling edge of GTETRGB input.	R/W
b4	PSGTRGCR	GTETRGC Pin Rising Input Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTETRGC input 1: Counter stop enabled on the rising edge of GTETRGC input.	R/W
b5	PSGTRGCF	GTETRGC Pin Falling Input Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTETRGC input 1: Counter stop enabled on the falling edge of GTETRGC input.	R/W
b6	PSGTRGDR	GTETRGD Pin Rising Input Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTETRGD input 1: Counter stop enabled on the rising edge of GTETRGD input.	R/W
b7	PSGTRGDF	GTETRGD Pin Falling Input Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTETRGD input 1: Counter stop enabled on the falling edge of GTETRGD input.	R/W
b8	PSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: Counter stop enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	PSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: Counter stop enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	PSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: Counter stop enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b11	PSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: Counter stop enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	PSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: Counter stop enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	PSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: Counter stop enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	PSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Counter stop enabled on the falling edge of GTIOCB input when GTIOCA input is 0	R/W
b15	PSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter stop enabled on the falling edge of GTIOCB input when GTIOCA input is 1	R/W
b16	PSELCA	ELC_GPTA Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTA event input 1: Counter stop enabled at the ELC_GPTA event input.	R/W
b17	PSELCB	ELC_GPTB Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTB event input 1: Counter stop enabled at the ELC_GPTB event input.	R/W
b18	PSELCC	ELC_GPTC Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTC event input 1: Counter stop enabled at the ELC_GPTC event input.	R/W
b19	PSELCD	ELC_GPTD Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTD event input 1: Counter stop enabled at the ELC_GPTD event input.	R/W
b20	PSELCE	ELC_GPTE Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTE event input 1: Counter stop enabled at the ELC_GPTE event input.	R/W
b21	PSELCF	ELC_GPTF Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTF event input 1: Counter stop enabled at the ELC_GPTF event input.	R/W
b22	PSELCG	ELC_GPTG Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTG event input 1: Counter stop enabled at the ELC_GPTG event input.	R/W
b23	PSELCH	ELC_GPTH Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTH event input 1: Counter stop enabled at the ELC_GPTH event input.	R/W
b30 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CSTOP	Software Source Counter Stop Enable	0: Counter stop disabled by the GTSTP register 1: Counter stop enabled by the GTSTP register.	R/W

The GTPSR sets the source to stop the GTCNT counter.

PSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Stop Enable)

The PSGTRGAR bit enables or disables the GTCNT counter stop on the rising edge of GTETRGA pin input.

PSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Stop Enable)

The PSGTRGAF bit enables or disables the GTCNT counter stop on the falling edge of GTETRGA pin input.

PSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Stop Enable)

The PSGTRGBR bit enables or disables the GTCNT counter stop on the rising edge of GTETRGB pin input.

PSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Stop Enable)

The PSGTRGBF bit enables or disables the GTCNT counter stop on the falling edge of GTETRGB pin input.

PSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Stop Enable)

The PSGTRGCR bit enables or disables the GTCNT counter stop on the rising edge of GTETRGC pin input.

PSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Stop Enable)

The PSGTRGCF bit enables or disables the GTCNT counter stop on the falling edge of GTETRGC pin input.

PSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Stop Enable)

The PSGTRGDR bit enables or disables the GTCNT counter stop on the rising edge of GTETRGD pin input.

PSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Stop Enable)

The PSGTRGDF bit enables or disables the GTCNT counter stop on the falling edge of GTETRGD pin input.

PSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Stop Enable)

The PSCARBL bit enables or disables the GTCNT counter stop on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

PSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Stop Enable)

The PSCARBH bit enables or disables the GTCNT counter stop on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

PSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Stop Enable)

The PSCAFBL bit enables or disables the GTCNT counter stop on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

PSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Stop Enable)

The PSCAFBH bit enables or disables the GTCNT counter stop on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

PSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Stop Enable)

The PSCBRAL bit enables or disables the GTCNT counter stop on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

PSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Stop Enable)

The PSCBRAH bit enables or disables the GTCNT counter stop on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

PSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Stop Enable)

The PSCBFAL bit enables or disables the GTCNT counter stop on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

PSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Stop Enable)

The PSCBFAH bit enables or disables the GTCNT counter stop on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

PSELCm bit (ELC_GPTm Event Source Counter Stop Enable) (m = A to H)

The PSELCm bit enables or disables the GTCNT counter stop at the ELC_GPTm event input.

CSTOP bit (Software Source Counter Stop Enable)

The CSTOP bit enables or disables the GTCNT counter stop by the GTSTP register.

22.2.7 General PWM Timer Clear Source Select Register (GTCSR)

Address(es): GPT32EHm.GTCSR 4007 8018h + 0100h × m (m = 0 to 3)
GPT32Em.GTCSR 4007 8018h + 0100h × m (m = 4 to 7)
GPT32m.GTCSR 4007 8018h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CCLR	—	—	—	—	—	—	—	CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	CSGTRGDF	CSGTRGDR	CSGTRGCF	CSGTRGCR	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CSGTRGAR	GTETRGA Pin Rising Input Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTETRGA input 1: Counter clear enabled on the rising edge of GTETRGA input.	R/W
b1	CSGTRGAF	GTETRGA Pin Falling Input Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTETRGA input 1: Counter clear enabled on the falling edge of GTETRGA input.	R/W
b2	CSGTRGBR	GTETRGB Pin Rising Input Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTETRGB input 1: Counter clear enabled on the rising edge of GTETRGB input.	R/W
b3	CSGTRGBF	GTETRGB Pin Falling Input Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTETRGB input 1: Counter clear enabled on the falling edge of GTETRGB input.	R/W
b4	CSGTRGCR	GTETRGC Pin Rising Input Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTETRGC input 1: Counter clear enabled on the rising edge of GTETRGC input.	R/W
b5	CSGTRGCF	GTETRGC Pin Falling Input Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTETRGC input 1: Counter clear enabled on the falling edge of GTETRGC input.	R/W
b6	CSGTRGDR	GTETRGD Pin Rising Input Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTETRGD input 1: Counter clear enabled on the rising edge of GTETRGD input.	R/W
b7	CSGTRGDF	GTETRGD Pin Falling Input Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTETRGD input 1: Counter clear enabled on the falling edge of GTETRGD input.	R/W
b8	CSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: Counter clear enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	CSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: Counter clear enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	CSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: Counter clear enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b11	CSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: Counter clear enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	CSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: Counter clear enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	CSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: Counter clear enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	CSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Counter clear enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	CSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter clear enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	CSELCA	ELC_GPTA Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTA event input 1: Counter clear enabled at ELC_GPTA event input.	R/W
b17	CSELCB	ELC_GPTB Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTB event input 1: Counter clear enabled at the ELC_GPTB event input.	R/W
b18	CSELCC	ELC_GPTC Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTC event input 1: Counter clear enabled at the ELC_GPTC event input.	R/W
b19	CSELCD	ELC_GPTD Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTD event input 1: Counter clear enabled at the ELC_GPTD event input.	R/W
b20	CSELCE	ELC_GPTE Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTE event input 1: Counter clear enabled at the ELC_GPTE event input.	R/W
b21	CSELCF	ELC_GPTF Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTF event input 1: Counter clear enabled at the ELC_GPTF event input.	R/W
b22	CSELCG	ELC_GPTG Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTG event input 1: Counter clear enabled at the ELC_GPTG event input.	R/W
b23	CSELCH	ELC_GPTH Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTH event input 1: Counter clear enabled at the ELC_GPTH event input.	R/W
b30 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CCLR	Software Source Counter Clear Enable	0: Counter clear disabled by the GTCLR register 1: Counter clear enabled by the GTCLR register.	R/W

The GTCSR sets the source to clear the GTCNT counter.

CSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Clear Enable)

The CSGTRGAR bit enables or disables the GTCNT counter clear on the rising edge of GTETRGA pin input.

CSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Clear Enable)

The CSGTRGAF bit enables or disables the GTCNT counter clear on the falling edge of GTETRGA pin input.

CSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Clear Enable)

The CSGTRGBR bit enables or disables the GTCNT counter clear on the rising edge of GTETRGB pin input.

CSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Clear Enable)

The CSGTRGBF bit enables or disables the GTCNT counter clear on the falling edge of GTETRGB pin input.

CSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Clear Enable)

The CSGTRGCR bit enables or disables the GTCNT counter clear on the rising edge of GTETRGC pin input.

CSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Clear Enable)

The CSGTRGCF bit enables or disables the GTCNT counter clear on the falling edge of GTETRGC pin input.

CSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Clear Enable)

The CSGTRGDR bit enables or disables the GTCNT counter clear on the rising edge of GTETRGD pin input.

CSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Clear Enable)

The CSGTRGDF bit enables or disables the GTCNT counter clear on the falling edge of GTETRGD pin input.

CSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Clear Enable)

The CSCARBL bit enables or disables the GTCNT counter clear on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

CSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Clear Enable)

The CSCARBH bit enables or disables the GTCNT counter clear on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

CSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Clear Enable)

The CSCAFBL bit enables or disables the GTCNT counter clear on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

CSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Clear Enable)

The CSCAFBH bit enables or disables the GTCNT counter clear on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

CSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Clear Enable)

The CSCBRAL bit enables or disables the GTCNT counter clear on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

CSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Clear Enable)

The CSCBRAH bit enables or disables the GTCNT counter clear on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

CSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Clear Enable)

The CSCBFAL bit enables or disables the GTCNT counter clear on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

CSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Clear Enable)

The CSCBFAH bit enables or disables the GTCNT counter clear on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

CSELCm bit (ELC_GPTm Event Source Counter Clear Enable) (m = A to H)

The CSELCm bit enables or disables the GTCNT counter clear at the ELC_GPTm event input.

CCLR bit (Software Source Counter Clear Enable)

The CCLR bit enables or disables the GTCNT counter clear by the GTCLR register.

22.2.8 General PWM Timer Up Count Source Select Register (GTUPSR)

Address(es): GPT32EHm.GTUPSR 4007 801Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTUPSR 4007 801Ch + 0100h × m (m = 4 to 7)
GPT32m.GTUPSR 4007 801Ch + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	USGTRGDF	USGTRGDR	USGTRGCF	USGTRGCR	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	USGTRGAR	GTETRGA Pin Rising Input Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTETRGA input 1: Counter count up enabled on the rising edge of GTETRGA input.	R/W
b1	USGTRGAF	GTETRGA Pin Falling Input Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTETRGA input 1: Counter count up enabled on the falling edge of GTETRGA input.	R/W
b2	USGTRGBR	GTETRGB Pin Rising Input Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTETRGB input 1: Counter count up enabled on the rising edge of GTETRGB input.	R/W
b3	USGTRGBF	GTETRGB Pin Falling Input Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTETRGB input 1: Counter count up enabled on the falling edge of GTETRGB input.	R/W
b4	USGTRGCR	GTETRGC Pin Rising Input Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTETRGC input 1: Counter count up enabled on the rising edge of GTETRGC input.	R/W
b5	USGTRGCF	GTETRGC Pin Falling Input Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTETRGC input 1: Counter count up enabled on the falling edge of GTETRGC input.	R/W
b6	USGTRGDR	GTETRGD Pin Rising Input Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTETRGD input 1: Counter count up enabled on the rising edge of GTETRGD input.	R/W
b7	USGTRGDF	GTETRGD Pin Falling Input Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTETRGD input 1: Counter count up enabled on the falling edge of GTETRGD input.	R/W
b8	USCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: Counter count up enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	USCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: Counter count up enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	USCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: Counter count up enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b11	USCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: Counter count up enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	USCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: Counter count up enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	USCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: Counter count up enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	USCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Counter count up enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	USCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter count up enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	USELCA	ELC_GPTA Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTA event input 1: Counter count up enabled at the ELC_GPTA event input.	R/W
b17	USELCB	ELC_GPTB Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTB event input 1: Counter count up enabled at the ELC_GPTB event input.	R/W
b18	USELCC	ELC_GPTC Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTC event input 1: Counter count up enabled at the ELC_GPTC event input.	R/W
b19	USELCD	ELC_GPTD Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTD event input 1: Counter count up enabled at the ELC_GPTD event input.	R/W
b20	USELCE	ELC_GPTE Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTE event input 1: Counter count up enabled at the ELC_GPTE event input.	R/W
b21	USELCF	ELC_GPTF Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTF event input 1: Counter count up enabled at the ELC_GPTF event input.	R/W
b22	USELCG	ELC_GPTG Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTG event input 1: Counter count up enabled at the ELC_GPTG event input.	R/W
b23	USELCH	ELC_GPTH Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTH event input 1: Counter count up enabled at the ELC_GPTH event input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTUPSR sets the source to count up the GTCNT counter.

When at least one bit in the GTUPSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

USGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Up Enable)

The USGTRGAR bit enables or disables the GTCNT counter count up on the rising edge of GTETRGA pin input.

USGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Up Enable)

The USGTRGAF bit enables or disables the GTCNT counter count up on the falling edge of GTETRGA pin input.

USGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Up Enable)

The USGTRGBR bit enables or disables the GTCNT counter count up on the rising edge of GTETRGB pin input.

USGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Up Enable)

The USGTRGBF bit enables or disables the GTCNT counter count up on the falling edge of GTETRGB pin input.

USGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Up Enable)

The USGTRGCR bit enables or disables the GTCNT counter count up on the rising edge of GTETRGC pin input.

USGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Up Enable)

The USGTRGCF bit enables or disables the GTCNT counter count up on the falling edge of GTETRGC pin input.

USGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Up Enable)

The USGTRGDR bit enables or disables the GTCNT counter count up on the rising edge of GTETRGD pin input.

USGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Up Enable)

The USGTRGDF bit enables or disables the GTCNT counter count up on the falling edge of GTETRGD pin input.

USCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Up Enable)

The USCARBL bit enables or disables the GTCNT counter count up on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

USCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Up Enable)

The USCARBH bit enables or disables the GTCNT counter count up on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

USCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Up Enable)

The USCAFBL bit enables or disables the GTCNT counter count up on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

USCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Up Enable)

The USCAFBH bit enables or disables the GTCNT counter count up on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

USCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Up Enable)

The USCBRAL bit enables or disables the GTCNT counter count up on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

USCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Up Enable)

The USCBRAH bit enables or disables the GTCNT counter count up on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

USCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Up Enable)

The USCBFAL bit enables or disables the GTCNT counter count up on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

USCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Up Enable)

The USCBFAH bit enables or disables the GTCNT counter count up on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

USELCm bit (ELC_GPTm Event Source Counter Count Up Enable) (m = A to H)

The USELCm bit enables or disables the GTCNT counter count up at the ELC_GPTm event input.

22.2.9 General PWM Timer Down Count Source Select Register (GTDNSR)

Address(es): GPT32EHm.GTDNSR 4007 8020h + 0100h × m (m = 0 to 3)
GPT32Em.GTDNSR 4007 8020h + 0100h × m (m = 4 to 7)
GPT32m.GTDNSR 4007 8020h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	DSGTRGDF	DSGTRGDR	DSGTRGCF	DSGTRGCR	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DSGTRGAR	GTETRGA Pin Rising Input Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTETRGA input 1: Counter count down enabled on the rising edge of GTETRGA input.	R/W
b1	DSGTRGAF	GTETRGA Pin Falling Input Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTETRGA input 1: Counter count down enabled on the falling edge of GTETRGA input.	R/W
b2	DSGTRGBR	GTETRGB Pin Rising Input Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTETRGB input 1: Counter count down enabled on the rising edge of GTETRGB input.	R/W
b3	DSGTRGBF	GTETRGB Pin Falling Input Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTETRGB input 1: Counter count down enabled on the falling edge of GTETRGB input.	R/W
b4	DSGTRGCR	GTETRGC Pin Rising Input Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTETRGC input 1: Counter count down enabled on the rising edge of GTETRGC input.	R/W
b5	DSGTRGCF	GTETRGC Pin Falling Input Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTETRGC input 1: Counter count down enabled on the falling edge of GTETRGC input.	R/W
b6	DSGTRGDR	GTETRGD Pin Rising Input Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTETRGD input 1: Counter count down enabled on the rising edge of GTETRGD input.	R/W
b7	DSGTRGDF	GTETRGD Pin Falling Input Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTETRGD input 1: Counter count down enabled on the falling edge of GTETRGD input.	R/W
b8	DSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: Counter count down enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	DSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: Counter count down enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	DSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: Counter count down enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b11	DSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: Counter count down enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	DSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: Counter count down enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	DSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: Counter count down enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	DSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Counter count down enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	DSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter count down enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	DSELCA	ELC_GPTA Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTA event input 1: Counter count down enabled at the ELC_GPTA event input.	R/W
b17	DSELCB	ELC_GPTB Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTB event input 1: Counter count down enabled at the ELC_GPTB event input.	R/W
b18	DSELCC	ELC_GPTC Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTC event input 1: Counter count down enabled at the ELC_GPTC event input.	R/W
b19	DSELCD	ELC_GPTD Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTD event input 1: Counter count down enabled at the ELC_GPTD event input.	R/W
b20	DSELCE	ELC_GPTE Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTE event input 1: Counter count down enabled at the ELC_GPTE event input.	R/W
b21	DSELCF	ELC_GPTF Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTF event input 1: Counter count down enabled at the ELC_GPTF event input.	R/W
b22	DSELCG	ELC_GPTG Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTG event input 1: Counter count down enabled at the ELC_GPTG event input.	R/W
b23	DSELCH	ELC_GPTH Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTH event input 1: Counter count down enabled at the ELC_GPTH event input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDNSR sets the source to count down the GTCNT counter.

When at least one bit in the GTDNSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

DSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Down Enable)

The DSGTRGAR bit enables or disables the GTCNT counter count down on the rising edge of GTETRGA pin input.

DSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Down Enable)

The DSGTRGAF bit enables or disables the GTCNT counter count down on the falling edge of GTETRGA pin input.

DSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Down Enable)

The DSGTRGBR bit enables or disables the GTCNT counter count down on the rising edge of GTETRGB pin input.

DSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Down Enable)

The DSGTRGBF bit enables or disables the GTCNT counter count down on the falling edge of GTETRGB pin input.

DSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Down Enable)

The DSGTRGCR bit enables or disables the GTCNT counter count down on the rising edge of GTETRGC pin input.

DSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Down Enable)

The DSGTRGCF bit enables or disables the GTCNT counter count down on the falling edge of GTETRGC pin input.

DSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Down Enable)

The DSGTRGDR bit enables or disables the GTCNT counter count down on the rising edge of GTETRGD pin input.

DSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Down Enable)

The DSGTRGDF bit enables or disables the GTCNT counter count down on the falling edge of GTETRGD pin input.

DSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Down Enable)

The DSCARBL bit enables or disables the GTCNT counter count down on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

DSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Down Enable)

The DSCARBH bit enables or disables the GTCNT counter count down on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

DSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Down Enable)

The DSCAFBL bit enables or disables the GTCNT counter count down on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

DSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Down Enable)

The DSCAFBH bit enables or disables the GTCNT counter count down on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

DSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Down Enable)

The DSCBRAL bit enables or disables the GTCNT counter count down on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

DSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Down Enable)

The DSCBRAH bit enables or disables the GTCNT counter count down on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

DSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Down Enable)

The DSCBFAL bit enables or disables the GTCNT counter count down on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

DSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Down Enable)

The DSCBFAH bit enables or disables the GTCNT counter count down on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

DSELCm bit (ELC_GPTm Event Source Counter Count Down Enable) (m = A to H)

The DSELCm bit enables or disables the GTCNT counter count down at the ELC_GPTm event input.

22.2.10 General PWM Timer Input Capture Source Select Register A (GTICASR)

Address(es): GPT32EHm.GTICASR 4007 8024h + 0100h × m (m = 0 to 3)
GPT32Em.GTICASR 4007 8024h + 0100h × m (m = 4 to 7)
GPT32m.GTICASR 4007 8024h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	ASGTRGDF	ASGTRGDR	ASGTRGCF	ASGTRGCR	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ASGTRGAR	GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTETRGA input 1: GTCCRA input capture enabled on the rising edge of GTETRGA input.	R/W
b1	ASGTRGAF	GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTETRGA input 1: GTCCRA input capture enabled on the falling edge of GTETRGA input.	R/W
b2	ASGTRGBR	GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTETRGB input 1: GTCCRA input capture enabled on the rising edge of GTETRGB input.	R/W
b3	ASGTRGBF	GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTETRGB input 1: GTCCRA input capture enabled on the falling edge of GTETRGB input.	R/W
b4	ASGTRGCR	GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTETRGC input 1: GTCCRA input capture enabled on the rising edge of GTETRGC input.	R/W
b5	ASGTRGCF	GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTETRGC input 1: GTCCRA input capture enabled on the falling edge of GTETRGC input.	R/W
b6	ASGTRGDR	GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTETRGD input 1: GTCCRA input capture enabled on the rising edge of GTETRGD input.	R/W

Bit	Symbol	Bit name	Description	R/W
b7	ASGTRGDF	GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTETRGD input 1: GTCCRA input capture enabled on the falling edge of GTETRGD input.	R/W
b8	ASCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	ASCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	ASCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	ASCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	ASCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	ASCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	ASCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	ASCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	ASELCA	ELC_GPTA Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTA event input 1: GTCCRA input capture enabled at the ELC_GPTA event input.	R/W
b17	ASELCB	ELC_GPTB Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTB event input 1: GTCCRA input capture enabled at the ELC_GPTB event input.	R/W
b18	ASELCC	ELC_GPTC Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTC event input 1: GTCCRA input capture enabled at the ELC_GPTC event input.	R/W
b19	ASELCD	ELC_GPTD Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTD event input 1: GTCCRA input capture enabled at the ELC_GPTD event input.	R/W
b20	ASELCE	ELC_GPTE Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTE event input 1: GTCCRA input capture enabled at the ELC_GPTE event input.	R/W
b21	ASELCF	ELC_GPTF Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTF event input 1: GTCCRA input capture enabled at the ELC_GPTF event input.	R/W

Bit	Symbol	Bit name	Description	R/W
b22	ASELCG	ELC_GPTG Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTG event input 1: GTCCRA input capture enabled at the ELC_GPTG event input.	R/W
b23	ASELCH	ELC_GPTH Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTH event input 1: GTCCRA input capture enabled at the ELC_GPTH event input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTICASR sets the source of input capture for GTCCRA.

ASGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGAR bit enables or disables the input capture for GTCCRA on the rising edge of GTETRGA pin input.

ASGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGAF bit enables or disables the input capture for GTCCRA on the falling edge of GTETRGA pin input.

ASGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGBR bit enables or disables the input capture for GTCCRA on the rising edge of GTETRGB pin input.

ASGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGBF bit enables or disables the input capture for GTCCRA on the falling edge of GTETRGB pin input.

ASGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGCR bit enables or disables the input capture for GTCCRA on the rising edge of GTETRGC pin input.

ASGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGCF bit enables or disables the input capture for GTCCRA on the falling edge of GTETRGC pin input.

ASGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGDR bit enables or disables the input capture for GTCCRA on the rising edge of GTETRGD pin input.

ASGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGDF bit enables or disables the input capture for GTCCRA on the falling edge of GTETRGD pin input.

ASCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRA Input Capture Enable)

The ASCARBL bit enables or disables the input capture for GTCCRA on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

ASCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRA Input Capture Enable)

The ASCARBH bit enables or disables the input capture for GTCCRA on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

ASCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRA Input Capture Enable)

The ASCAFBL bit enables or disables the input capture for GTCCRA on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

ASCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRA Input Capture Enable)

The ASCAFBH bit enables or disables the input capture for GTCCRA on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

ASCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRA Input Capture Enable)

The ASCBRAL bit enables or disables the input capture for GTCCRA on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

ASCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRA Input Capture Enable)

The ASCBRAH bit enables or disables the input capture for GTCCRA on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

ASCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRA Input Capture Enable)

The ASCBFAL bit enables or disables the input capture for GTCCRA on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

ASCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRA Input Capture Enable)

The ASCBFAH bit enables or disables the input capture for GTCCRA on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

ASELCm bit (ELC_GPTm Event Source Counter GTCCRA Input Capture Enable) (m = A to H)

The ASELCm bit enables or disables the input capture for GTCCRA at the ELC_GPTm event input.

22.2.11 General PWM Timer Input Capture Source Select Register B (GTICBSR)

Address(es): GPT32EHm.GTICBSR 4007 8028h + 0100h × m (m = 0 to 3)
GPT32Em.GTICBSR 4007 8028h + 0100h × m (m = 4 to 7)
GPT32m.GTICBSR 4007 8028h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	BSGTRGDF	BSGTRGDR	BSGTRGCF	BSGTRGCR	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BSGTRGAR	GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTETRGA input 1: GTCCRB input capture enabled on the rising edge of GTETRGA input.	R/W
b1	BSGTRGAF	GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTETRGA input 1: GTCCRB input capture enabled on the falling edge of GTETRGA input.	R/W
b2	BSGTRGBR	GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTETRGB input 1: GTCCRB input capture enabled on the rising edge of GTETRGB input.	R/W
b3	BSGTRGBF	GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTETRGB input 1: GTCCRB input capture enabled on the falling edge of GTETRGB input.	R/W

Bit	Symbol	Bit name	Description	R/W
b4	BSGTRGCR	GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTETRGC input 1: GTCCRB input capture enabled on the rising edge of GTETRGC input.	R/W
b5	BSGTRGCF	GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTETRGC input 1: GTCCRB input capture enabled on the falling edge of GTETRGC input.	R/W
b6	BSGTRGDR	GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTETRGD input 1: GTCCRB input capture enabled on the rising edge of GTETRGD input.	R/W
b7	BSGTRGDF	GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTETRGD input 1: GTCCRB input capture enabled on the falling edge of GTETRGD input.	R/W
b8	BSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	BSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	BSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	BSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	BSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	BSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	BSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable GTCCRB input capture on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	BSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	BSELCA	ELC_GPTA Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTA event input 1: GTCCRB input capture enabled at the ELC_GPTA event input.	R/W
b17	BSELCB	ELC_GPTB Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTB event input 1: GTCCRB input capture enabled at the ELC_GPTB event input.	R/W
b18	BSELCC	ELC_GPTC Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTC event input 1: GTCCRB input capture enabled at the ELC_GPTC event input.	R/W

Bit	Symbol	Bit name	Description	R/W
b19	BSELCD	ELC_GPTD Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTD event input 1: GTCCRB input capture enabled at the ELC_GPTD event input.	R/W
b20	BSELCE	ELC_GPTE Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTE event input 1: GTCCRB input capture enabled at the ELC_GPTE event input.	R/W
b21	BSELCF	ELC_GPTF Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTF event input 1: GTCCRB input capture enabled at the ELC_GPTF event input.	R/W
b22	BSELCG	ELC_GPTG Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTG event input 1: GTCCRB input capture enabled at the ELC_GPTG event input.	R/W
b23	BSELCH	ELC_GPTH Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTH event input 1: GTCCRB input capture enabled at the ELC_GPTH event input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTICBSR sets the source of input capture for GTCCRB.

BSGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGAR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGA pin input.

BSGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGAF bit enables or disables the input capture for GTCCRB on the falling edge of GTETRGA pin input.

BSGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGBR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGB pin input.

BSGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGBF bit enables or disables the input capture for GTCCRB on the falling edge of GTETRGB pin input.

BSGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGCR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGC pin input.

BSGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGCF bit enables or disables the input capture for GTCCRB on the falling edge of GTETRGC pin input.

BSGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGDR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGD pin input.

BSGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGDF bit enables or disables the input capture for GTCCRB on the falling edge of GTETRGD pin input.

BSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRB Input Capture Enable)

The BSCARBL bit enables or disables the input capture for GTCCRB on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

BSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRB Input Capture Enable)

The BSCARBH bit enables or disables the input capture for GTCCRB on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

BSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRB Input Capture Enable)

The BSCAFBL bit enables or disables the input capture for GTCCRB on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

BSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRB Input Capture Enable)

The BSCAFBH bit enables or disables the input capture for GTCCRB on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

BSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRB Input Capture Enable)

The BSCBRAL bit enables or disables the input capture for GTCCRB on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

BSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRB Input Capture Enable)

The BSCBRAH bit enables or disables the input capture for GTCCRB on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

BSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRB Input Capture Enable)

The BSCBFAL bit enables or disables the input capture for GTCCRB on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

BSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRB Input Capture Enable)

The BSCBFAH bit enables or disables the input capture for GTCCRB on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

BSELCm bit (ELC_GPTm Event Source Counter GTCCRB Input Capture Enable) (m = A to H)

The BSELCm bit enables or disables the input capture for GTCCRB at the ELC_GPTm event input.

22.2.12 General PWM Timer Control Register (GTCR)

Address(es): GPT32EHm.GTCR 4007 802Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCR 4007 802Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCR 4007 802Ch + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	TPCS[2:0]			—	—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CST	Count Start	0: Count operation is stopped 1: Count operation is performed.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b18 to b16	MD[2:0]	Mode Select	b18 b16 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer is possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer is possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited.	R/W
b23 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b24	TPCS[2:0]	Timer Prescaler Select	b26 b24 0 0 0: PCLKD/1 0 0 1: PCLKD/4 0 1 0: PCLKD/16 0 1 1: PCLKD/64 1 0 0: PCLKD/256 1 0 1: PCLKD/1024.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTCR controls GTCNT.

CST bit (Count Start)

The CST bit controls the GTCNT counter start and stop.

[Setting conditions]

- The GTSTR value where the channel number associated with the bit number is set to 1 with the GTSSR.CSTRT bit at 1
- The ELC event input or the GTIOCA/GTIOCB/GTETRGn port input event enabled by GTSSR as the counter start source, occurs
- 1 is written by software directly.

[Clearing conditions]

- The GTSTP value where the channel number associated with the bit number is set to 1 with the GTSSR.CSTOP bit at 1.
- The ELC event input or the GTIOCA/GTIOCB/GTETRGn port input event enabled by GTSSR as the counter stop source, occurs
- 0 is written by software directly.

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

TPCS[2:0] bits (Timer Prescaler Select)

The TPCS[2:0] bits select the clock for GTCNT. A clock prescaler can be selected independently for each channel. The TPCS[2:0] bits must be set while the GTCNT operation is stopped.

22.2.13 General PWM Timer Count Direction and Duty Setting Register (GTUDDTYC)

Address(es): GPT32EHm.GTUDDTYC 4007 8030h + 0100h × m (m = 0 to 3)
GPT32Em.GTUDDTYC 4007 8030h + 0100h × m (m = 4 to 7)
GPT32m.GTUDDTYC 4007 8030h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	UD	Count Direction Setting	0: GTCNT counts down 1: GTCNT counts up.	R/W
b1	UDF	Forcible Count Direction Setting	0: Not forcibly set 1: Forcibly set.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17, 16	OADTY[1:0]	GTIOCA Output Duty Setting	b17 b16 0 x: GTIOCA pin duty depends on compare match 1 0: GTIOCA pin duty = 0% 1 1: GTIOCA pin duty = 100%.	R/W
b18	OADTYF	Forcible GTIOCA Output Duty Setting	0: Not forcibly set 1: Forcibly set.	R/W
b19	OADTYR	GTIOCA Output Value Selecting after Releasing 0%/100% Duty Setting	0: Apply output value set in 0%/100% duty to GTIOA[3:2] function after releasing 0%/100% duty setting 1: Apply masked compare match output value to GTIOA[3:2] function after releasing 0%/100% duty setting.	R/W
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	OBDTY[1:0]	GTIOCB Output Duty Setting	b25 b24 0 x: GTIOCB pin duty depends on compare match 1 0: GTIOCB pin duty = 0% 1 1: GTIOCB pin duty = 100%.	R/W
b26	OBDTYF	Forcible GTIOCB Output Duty Setting	0: Do not force setting 1: Force setting.	R/W
b27	OBDTYR	GTIOCB Output Value Selecting after Releasing 0%/100% Duty Setting	0: Apply output value set in 0%/100% duty to GTIOB[3:2] function after releasing 0%/100% duty setting 1: Apply masked compare match output value to GTIOB[3:2] function after releasing 0%/100% duty setting.	R/W
b31 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

x: Don't care

The GTUDDTYC sets the direction in which GTCNT counts (up-counting or down-counting) and sets the duty of the GTIOCA/GTIOCB pin output.

Count direction:

- In saw-wave mode.

When the UD value is set to 0 during up-counting, the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value is set to 1 during down-counting, the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).

When the UD value changes from 1 to 0 with the UDF bit being 0 and while counting is stopped, the counter starts up-counting and the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT

value becomes GTPR value). When the UD value changes from 0 to 1 with the UDF bit being 0 and while counting stops, the counter starts down-counting and the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).

When the UDF bit is set to 1 while counting stops, the UD bit value is reflected in the count direction when counting starts.

Count direction:

- In triangle-wave mode.

When the UD value changes during counting, the count direction does not change. When the UD value changes while the UDF bit is 0 and counting stops, the change is not reflected in the count direction when counting starts.

When the UDF bit is set to 1 while counting stops, the UD value is reflected in the count direction when counting starts.

UD bit (Count Direction Setting)

The UD bit sets the count direction (up-counting or down-counting) for GTCNT.

UDF bit (Forcible Count Direction Setting)

The UDF bit forcibly sets the count direction when GTCNT starts operation as the UD value. Only write 0 to this bit during counter operation. When 1 is written to the UDF bit while counting stops, return this bit to 0 before counting starts.

Output duty

- In saw-wave mode.

When the OADTY/OBDTY value changes during up-counting, the duty is reflected at an overflow (GTCNT = GTPR). When the OADTY/OBDTY value changes during down-counting, the duty is reflected at an underflow (GTCNT = 0).

When the OADTY/OBDTY value changes to 1 with the OADTYF/OBDTYF bit being 0 and while counting stops, the output duty is not reflected at the starting counter operation. When the count direction is up, the output duty is reflected at an overflow (GTCNT = GTPR). When the count direction is down, the output duty is reflected at an underflow (GTCNT = 0).

When the OADTY/OBDTY value changes to 0 with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at the starting counter operation.

Output duty

- In triangle-wave mode.

When the OADTY/OBDTY value changes during counting, the duty is reflected at an underflow. When the OADTY/OBDTY value changes to 1 with the OADTYF/OBDTYF bit being 0 and while counting stops, the output duty is not reflected at the starting counter operation. The output duty is reflected at an underflow.

When the OADTY/OBDTY value changes to 0 with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at the starting counter operation.

OmDTY[1:0] bits (GTIOCm Output Duty Setting) (m = A, B)

The OmDTY[1:0] bits set the output duty of the GTIOCm pin to either 0%, 100%, or compare match control.

OmDTYF bit (Forcible GTIOCm Output Duty Setting) (m = A, B)

The OmDTYF bit forcibly sets the output duty cycle to the OmDTY setting. Set this bit to 0 during counter operation. When OmDTYF bit is set to 1 while counting stops, return this bit to 0 until the first period ends after the counter starts.

OmDTYR bit (GTIOCm Output Value Selecting after Releasing 0%/100% Duty Setting) (m = A, B)

The OmDTYR bits select the value that is the object of output retained or toggled at cycle end, when the control changes from 0%/100% duty setting to compare match for the GTIOCm pin and GTIOR. The GTIOm[3:2] bits are set to 00b (output retained at cycle end) or the GTIOR.GTIOm[3:2] bits are set to 11b (output toggled at cycle end).

While the duty 0%/100% setting operation is running, the compare match operation continues inside the GPT32. When the OmDTYR bit is set to 1, the GTIOCm pin is in the output state selected by the GTIOR.GTIOm [3:2] bit at the end of

the cycle in the compare match operation.

22.2.14 General PWM Timer I/O Control Register (GTIOR)

Address(es): GPT32EHm.GTIOR 4007 8034h + 0100h × m (m = 0 to 3)
GPT32Em.GTIOR 4007 8034h + 0100h × m (m = 4 to 7)
GPT32m.GTIOR 4007 8034h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	GTIOA[4:0]	GTIOCA Pin Function Select	See Table 22.5.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	OADFLT	GTIOCA Pin Output Value Setting at the Count Stop	0: The GTIOCA pin outputs low when counting stops 1: The GTIOCA pin outputs high when counting stops.	R/W
b7	OAHLD	GTIOCA Pin Output Setting at the Start/Stop Count	0: The GTIOCA pin output level at the start or stop of counting depends on the register setting 1: The GTIOCA pin output level is retained at the start or stop of counting.	R/W
b8	OAE	GTIOCA Pin Output Enable	0: Output is disabled 1: Output is enabled.	R/W
b10, b9	OADF[1:0]	GTIOCA Pin Disable Value Setting	b10 b9 0 0: Output disable is prohibited 0 1: GTIOCA pin is set to Hi-Z on output disable 1 0: Set GTIOCA pin to 0 on output disable 1 1: Set GTIOCA pin to 1 on output disable.	R/W
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	NFAEN	Noise Filter A Enable	0: The noise filter for the GTIOCA pin is disabled 1: The noise filter for the GTIOCA pin is enabled.	R/W
b15, b14	NFCSA[1:0]	Noise Filter A Sampling Clock Select	b15 b14 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W
b20 to b16	GTIOB[4:0]	GTIOCB Pin Function Select	See Table 22.5.	R/W
b21	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b22	OBDFLT	GTIOCB Pin Output Value Setting at the Count Stop	0: The GTIOCB pin outputs low when counting stops 1: The GTIOCB pin outputs high when counting stops.	R/W
b23	OBHLD	GTIOCB Pin Output Setting at the Start/Stop Count	0: The GTIOCB pin output level at the start or stop of counting depends on the register setting 1: The GTIOCB pin output level is retained at the start or stop of counting.	R/W
b24	OBE	GTIOCB Pin Output Enable	0: Output is disabled 1: Output is enabled.	R/W
b26, b25	OBDF[1:0]	GTIOCB Pin Disable Value Setting	b26 b25 0 0: Output disable is prohibited 0 1: GTIOCB pin is set to Hi-Z on output disable 1 0: GTIOCB pin is set to 0 on output disable 1 1: GTIOCB pin is set to 1 on output disable.	R/W
b28, b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b29	NFBEN	Noise Filter B Enable	0: Noise filter for GTIOCB pin is disabled 1: Noise filter for GTIOCB pin is enabled.	R/W
b31, b30	NFCSB[1:0]	Noise Filter B Sampling Clock Select	b31 b30 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W

The GTIOR sets the functions of the GTIOCA and GTIOCB pins.

GTIOA[4:0] bits (GTIOCA Pin Function Select)

The GTIOA[4:0] bits select the GTIOCA pin function. For details, see Table 22.5.

OADFLT bit (GTIOCA Pin Output Value Setting at the Count Stop)

The OADFLT bit selects whether the GTIOCA pin outputs high or low when counting stops.

OAHLD bit (GTIOCA Pin Output Setting at the Start/Stop Count)

The OAHLD bit specifies whether the GTIOCA pin output level is retained or the level at the start/stop of counting depends on the register setting.

When the OAHLD bit is set to 0:

- The value specified in bit [4] of the GTIOA[4:0] bits is output when counting starts
- The value specified in the OADFLT bit is output when counting stops
- If the OADFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OAHLD bit is set to 1:

- The output is retained when counting starts or stops.

OAE bit (GTIOCA Pin Output Enable)

The OAE bit disables or enables the GTIOCA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of GTIOCA pin when an output disable request occurs.

NFAEN bit (Noise Filter A Enable)

The NFAEN bit disables or enables the noise filter for input from the GTIOCA pin. Because changing the value of the bit might lead to internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSA[1:0] bits (Noise Filter A Sampling Clock Select)

The NFCSA[1:0] bits set the sampling interval for the noise filter of the GTIOCA pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

GTIOB[4:0] bits (GTIOCB Pin Function Select)

The GTIOB[4:0] bits select the GTIOCB pin function. For details, see Table 22.5.

OBDFLT bit (GTIOCB Pin Output Value Setting at the Count Stop)

The OBDFLT bit sets whether the GTIOCB pin outputs high or low when counting stops.

OBHLD bit (GTIOCB Pin Output Setting at the Start/Stop Count)

The OBHLD bit specifies whether the GTIOCB pin output level is retained or the level at the start/stop of counting depends on the register setting.

When the OBHLD bit is set to 0:

- The value specified in bit [4] of the GTIOB[4:0] bits is output when counting starts
- The value specified in the OBDFLT bit is output when counting stops
- If the OBDFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OBHLD bit is set to 1:

- The output is retained when counting starts or stops.

OBE bit (GTIOCB Pin Output Enable)

The OBE bit disables or enables the GTIOCB pin output.

When GTCCRB register is used as the input capture register (at least one bit in GTICBSR register is set to 1), the GTIOCB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of GTIOCB pin when an output disable request occurs.

NFBEN bit (Noise Filter B Enable)

The NFBEN bit disables or enables the noise filter for input from the GTIOCB pin. Because changing the value of the bit might lead to internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSB[1:0] bits (Noise Filter B Sampling Clock Select)

The NFCSB[1:0] bits set the sampling interval for the noise filter of the GTIOCB pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

Table 22.5 Settings of GTIOA[4:0] and GTIOB[4:0] bits (1 of 2)

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2	b1, b0
0	0	0	0	0	Initial output is low	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	0	1	0			High output at GTCCRA/GTCCRB compare match
0	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	1	1	0			High output at GTCCRA/GTCCRB compare match
0	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	0	1	0			High output at GTCCRA/GTCCRB compare match
0	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	1	1	0			High output at GTCCRA/GTCCRB compare match
0	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match

Table 22.5 Settings of GTIOA[4:0] and GTIOB[4:0] bits (2 of 2)

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2	b1, b0
1	0	0	0	0	Set initial output high	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	0	1	0			High output at GTCCRA/GTCCRB compare match
1	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	1	0	0		Output low at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	1	1	0			High output at GTCCRA/GTCCRB compare match
1	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	0	0	0		Output high at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	0	1	0			High output at GTCCRA/GTCCRB compare match
1	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	1	1	0			High output at GTCCRA/GTCCRB compare match
1	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match

Note 1. The cycle end means an overflow (GTCNT changes from GTPR to 0 in up-counting) or underflow (GTCNT changes from 0 to GTPR in down-counting). The GTCNT counter is cleared for saw waves and for the trough (GTCNT changes from 0 to 1) for triangle waves.

Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, the b3 and b2 settings are given priority in saw-wave PWM mode, and the b1 and b0 settings are given priority in any other mode.

Note 3. In event count operation where at least one bit in GTUPSR or GTDNSR is set to 1, the setting of b3 and b2 is ignored.

22.2.15 General PWM Timer Interrupt Output Setting Register (GTINTAD)

Address(es): GPT32EHm.GTINTAD 4007 8038h + 0100h × m (m = 0 to 3)
GPT32Em.GTINTAD 4007 8038h + 0100h × m (m = 4 to 7)
GPT32m.GTINTAD 4007 8038h + 0100h × m (m = 8 to 12)

- GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	GRPABL	GRPABH	GRPDTE	—	—	GRP[1:0]		—	—	—	—	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	GRPABL	GRPABH	—	—	—	GRP[1:0]		—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	ADTRAUEN	GTADTRA Compare Match (Up-Counting) A/D Converter Start Request Enable	0: A/D converter start request disabled 1: A/D converter start request enabled.	R/W
b17	ADTRADEN	GTADTRA Compare Match (Down-Counting) A/D Converter Start Request Enable	0: A/D converter start request disabled 1: A/D converter start request enabled.	R/W
b18	ADTRBUEN	GTADTRB Compare Match (Up-Counting) A/D Converter Start Request Enable	0: A/D converter start request disabled 1: A/D converter start request enabled.	R/W
b19	ADTRBDEN	GTADTRB Compare Match (Down-Counting) A/D Converter Start Request Enable	0: A/D converter start request disabled 1: A/D converter start request enabled.	R/W
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	GRP[1:0]	Output Disable Source Select	b25 b24 0 0: Group A output disable request 0 1: Group B output disable request 1 0: Group C output disable request 1 1: Group D output disable request.	R/W
b27, b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	GRPDTE	Dead Time Error Output Disable Request Enable	0: Dead time error output disable request disabled 1: Dead time error output disable request enabled.	R/W
b29	GRPABH	Same Time Output Level High Disable Request Enable	0: Same time output level high disable request disabled 1: Same time output level high disable request enabled.	R/W
b30	GRPABL	Same Time Output Level Low Disable Request Enable	0: Same time output level low disable request disabled 1: Same time output level low disable request enabled.	R/W

Bit	Symbol	Bit name	Description	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The GTINTAD enables or disables interrupt requests, A/D converter start requests, and output disable requests.

ADTRAUEN bit (GTADTRA Compare Match (Up-Counting) A/D Converter Start Request Enable)

The ADTRAUEN bit enables or disables A/D converter start requests generated by GTADTRA compare matches during GTCNT up-counting. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

ADTRADEN bit (GTADTRA Compare Match (Down-Counting) A/D Converter Start Request Enable)

The ADTRADEN bit enables or disables A/D converter start requests generated by GTADTRA compare matches during GTCNT down-counting. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

ADTRBUEN bit (GTADTRB Compare Match (Up-Counting) A/D Converter Start Request Enable)

The ADTRBUEN bit enables or disables A/D converter start requests generated by GTADTRB compare matches during GTCNT up-counting. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

ADTRBDEN bit (GTADTRB Compare Match (Down-Counting) A/D Converter Start Request Enable)

The ADTRBDEN bit enables or disables A/D converter start requests generated by GTADTRB compare matches during GTCNT down-counting. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

GRP[1:0] bits (Output Disable Source Select)

The GRP[1:0] bits select the GTIOCA or GTIOCB pin output disable source.

The output disable request to POEG outputs to the group which is selected in the GRP[1:0] bits when dead time error, same time output level high, or same time output level low occurs based on the output disable request enable bit.

GTST.ODF shows the request of output disable source group that is selected in the GRP[1:0] bits. The GRP[1:0] bits should be set when both GTIOR.OAE and GTIOR.OBE are 0.

GRPDTE bit (Dead Time Error Output Disable Request Enable)

The GRPDTE bit enables or disables dead time error output disable request. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

GRPABH bit (Same Time Output Level High Disable Request Enable)

The GRPABH bit enables or disables output disable request when the GTIOCA and GTIOCB pins output 1 at the same time.

GRPABL bit (Same Time Output Level Low Disable Request Enable)

The GRPABL bit enables or disables output disable request when the GTIOCA and GTIOCB pins output 0 at the same time.

22.2.16 General PWM Timer Status Register (GTST)

Address(es): GPT32EHm.GTST 4007 803Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTST 4007 803Ch + 0100h × m (m = 4 to 7)
GPT32m.GTST 4007 803Ch + 0100h × m (m = 8 to 12)

- GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	OABLF	OABHF	DTEF	—	—	—	ODF	—	—	—	—	ADTRBDF	ADTRBUF	ADTRADF	ADTRAUF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	—	ITCNT[2:0]			TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	OABLF	OABHF	—	—	—	—	ODF	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	—	—	—	—	TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TCFA	Input Capture/Compare Match Flag A	0: No input capture/compare match of GTCCRA is generated 1: An input capture/compare match of GTCCRA is generated.	R/(W)*1
b1	TCFB	Input Capture/Compare Match Flag B	0: No input capture/compare match of GTCCRB is generated 1: An input capture/compare match of GTCCRB is generated.	R/(W)*1
b2	TCFC	Input Compare Match Flag C	0: No compare match of GTCCRC is generated 1: A compare match of GTCCRC is generated.	R/(W)*1
b3	TCFD	Input Compare Match Flag D	0: No compare match of GTCCRD is generated 1: A compare match of GTCCRD is generated.	R/(W)*1
b4	TCFE	Input Compare Match Flag E	0: No compare match of GTCCRE is generated 1: A compare match of GTCCRE is generated.	R/(W)*1
b5	TCFF	Input Compare Match Flag F	0: No compare match of GTCCRF is generated 1: A compare match of GTCCRF is generated.	R/(W)*1
b6	TCFPO	Overflow Flag	0: No overflow (crest) occurred 1: An overflow (crest) occurred.	R/(W)*1
b7	TCFPU	Underflow Flag	0: No underflow (trough) occurred 1: An underflow (trough) occurred.	R/(W)*1
b10 to b8	ITCNT[2:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Count Counter	Counter for counting the number of times a timer interrupt is skipped	R
b14 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	TUCF	Count Direction Flag	0: GTCNT counter counts downward 1: GTCNT counter counts upward.	R
b16	ADTRAUF	GTADTRA Compare Match (Up-Counting) A/D Converter Start Request Flag	0: No compare match of GTADTRA at up-counting occurred 1: A compare match of GTADTRA at up-counting occurred.	R/(W)*1
b17	ADTRADF	GTADTRA Compare Match (Down-Counting) A/D Converter Start Request Flag	0: No compare match of GTADTRA at down-counting occurred 1: A compare match of GTADTRA at down-counting occurred.	R/(W)*1

Bit	Symbol	Bit name	Description	R/W
b18	ADTRBUF	GTADTRB Compare Match (Up-Counting) A/D Converter Start Request Flag	0: No compare match of GTADTRB at up-counting occurred 1: A compare match of GTADTRB at up-counting occurred.	R/(W)*1
b19	ADTRBDF	GTADTRB Compare Match (Down-Counting) A/D Converter Start Request Flag	0: No compare match of GTADTRB at down-counting occurred 1: A compare match of GTADTRB at down-counting occurred.	R/(W)*1
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	ODF	Output Disable Flag	0: No output disable request is generated 1: An output disable request is generated.	R
b27 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	DTEF	Dead Time Error Flag	0: No dead time error occurred 1: Dead time error occurred.	R
b29	OABHF	Same Time Output Level High Flag	0: GTIOCA and GTIOCB pins do not output 1 at the same time 1: GTIOCA and GTIOCB pins output 1 at the same time.	R
b30	OABLF	Same Time Output Level Low Flag	0: GTIOCA and GTIOCB pins do not output 0 at the same time 1: GTIOCA and GTIOCB pins output 0 at the same time.	R
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit. Do not write 1.

The GTST register indicates the status of the GPT.

TCFA flag (Input Capture/Compare Match Flag A)

The TCFA flag indicates the status for the input capture or compare match of GTCCRA.

[Setting conditions]

- GTCNT = GTCCRA when the GTCCRA register functions as a compare match register
- GTCNT counter value is transferred to GTCCRA by the input capture signal when the GTCCRA register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFB flag (Input Capture/Compare Match Flag B)

The TCFB flag indicates the status for the input capture or compare match of GTCCRB.

[Setting conditions]

- GTCNT = GTCCRB when the GTCCRB register functions as a compare match register
- GTCNT counter value is transferred to GTCCRB by the input capture signal when the GTCCRB register function as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFC flag (Input Compare Match Flag C)

The TCFC flag indicates the status for the compare match of GTCCRC.

[Setting condition]

- GTCNT = GTCCRC

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)

- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (GTCCRC performs buffer operation).

TCFD flag (Input Compare Match Flag D)

The TCFD flag indicates the status for the compare match of GTCCRD.

[Setting condition]

- GTCNT = GTCCRD

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (GTCCRD performs buffer operation).

TCFE flag (Input Compare Match Flag E)

The TCFE flag indicates the status for the compare match of GTCCRE.

[Setting condition]

- GTCNT = GTCCRE

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (GTCCRE performs buffer operation).

TCFF flag (Input Compare Match Flag F)

The TCFF flag indicates the status for the compare match of GTCCRF.

[Setting condition]

- GTCNT = GTCCRF

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (GTCCRF performs buffer operation).

TCFPO flag (Overflow Flag)

The TCFPO flag indicates when an overflow or a crest has occurred.

[Setting conditions]

- In saw-wave mode, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred
- In triangle-wave mode, a crest (GTCNT changes from GTPR to GTPR - 1) has occurred
- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

TCFPU flag (Underflow Flag)

The TCFPU flag indicates when an underflow or a trough has occurred.

[Setting conditions]

- In saw-wave mode, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred
- In triangle-wave mode, a trough (GTCNT changes from 0 to 1) has occurred
- In counting by hardware sources, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

ITCNT[2:0] bits (GPTn_OVF/GPTn_UDF Interrupt Skipping Count Counter)

When the GPTn_OVF/GPTn_UDF (n = 0 to 7) interrupt skipping function is used (the GTITC.IVTC[1:0] bits are set to a value other than 00b), the counter in the ITCNT[2:0] bits increments by 1 every time the GPTn_OVF/GPTn_UDF interrupt source that is selected in GTITC.IVTC[1:0] is generated.

Only GPT32EH and GPT32E have these bits. GPT32 does not have these bits.

[Clearing conditions]

- The GPTn_OVF/GPTn_UDF interrupt skipping function is not used (GTITC.IVTT[2:0] is 000b when GTITC.IVTC[1:0] is 00b)
- The GPTn_OVF/GPTn_UDF interrupt skipping count matches the specified count (ITCNT[2:0] matches the skipping count specified in GTITC.IVTT[2:0]).

TUCF flag (Count Direction Flag)

The TUCF flag indicates the count direction of GTCNT. In event count operation, this flag is set to 1 in up-counting and to 0 in down-counting.

ADTRAUF flag (GTADTRA Compare Match (Up-Counting) A/D Converter Start Request Flag)

The ADTRAUF flag indicates the status for the compare match of GTADTRA at up-counting.

[Setting condition]

- GTCNT = GTADTRA at up-counting.

[Clearing condition]

- 0 is written to this flag.

ADTRADF flag (GTADTRA Compare Match (Down-Counting) A/D Converter Start Request Flag)

The ADTRADF flag indicates the status for the compare match of GTADTRA at down-counting.

[Setting condition]

- GTCNT = GTADTRA at down-counting.

[Clearing condition]

- 0 is written to this flag.

ADTRBUF flag (GTADTRB Compare Match (Up-Counting) A/D Converter Start Request Flag)

The ADTRBUF flag indicates the status for the compare match of GTADTRB at up-counting.

[Setting condition]

- GTCNT = GTADTRB at up-counting.

[Clearing condition]

- 0 is written to this flag.

ADTRBDF flag (GTADTRB Compare Match (Down-Counting) A/D Converter Start Request Flag)

The ADTRBDF flag indicates the status for the compare match of GTADTRB at down-counting.

[Setting condition]

- GTCNT = GTADTRB at down-counting.

[Clearing condition]

- 0 is written to this bit.

ODF flag (Output Disable Flag)

The ODF flag shows the request of the output disable source group that is selected in the GRP[1:0] bits. When output is disabled, an output disable control is not released within the same cycle in which an output disable request is negated. It is released in the next cycle.

DTEF flag (Dead Time Error Flag)

The DTEF flag indicates that the timer output toggle point after the automatic addition of dead time has exceeded the timer cycle.

This flag returns to 0 when the timer output toggle point after the automatic addition of dead time is within the timer cycle. This flag is read-only. Writing 0 to clear the flag is not allowed.

[Setting condition]

- The timer output toggle point after the automatic addition of dead time has exceeded the timer cycle.
  For triangle wave in up-counting: GTCCRA - GTDVU ≤ 0
  For triangle wave in down-counting: GTCCRA - GTDVD < 0
  For saw-wave one-shot pulse mode in up-counting:
  GTCCRA - GTDVU < 0 or GTCCRA + GTDVD > GTPR
  For saw-wave one-shot pulse mode in down-counting:
  GTCCRA + GTDVU > GTPR or GTCCRA - GTDVD < 0

[Clearing condition]

- The timer output toggle point after the automatic addition of dead time is within the timer cycle.
  Only GPT32EH and GPT32E have this flag. GPT32 does not have this flag.
  GPT32 has the automatic dead time setting function but it does not generate dead time error.

OABHF flag (Same Time Output Level High Flag)

The OABHF flag indicates that the GTIOCA and the GTIOCB pins output 1 at the same time.

When the GTIOCA or GTIOCB pin outputs 0, this flag returns to 0. This flag is read-only. Writing 0 to clear the flag is not allowed. When an interrupt by the OABHF flag is enabled (GTINTAD.GRPABH = 1), the OABHF flag is output to the POEG as an output disable request.

[Setting condition]

- GTIOCA and GTIOCB pins output 1 at the same time when both the OAE and OBE bits are set to 1.

[Clearing conditions]

- GTIOCA pin output value is different from GTIOCB pin output value when both the OAE and OBE bits are set to 1
- GTIOCA and GTIOCB pins output 0 at the same time when both the OAE and OBE bits are set to 1
- Either the OAE bit or OBE bit is set to 0.

OABLF flag (Same Time Output Level Low Flag)

The OABLF flag indicates that the GTIOCA and GTIOCB pins output 0 at the same time.

When the GTIOCA or GTIOCB pin outputs 1, this flag returns to 0. This flag is read-only. Writing 0 to clear the flag is not allowed. When an interrupt by the OABLF flag is enabled (GTINTAD.GRPABL = 1), the OABLF flag is output to

the POEG as an output disable request.

[Setting condition]

- The GTIOCA and GTIOCB pins output 0 at the same time when both the OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCA pin output value is different from GTIOCB pin output value when both the OAE and OBE bits are set to 1
- The GTIOCA and GTIOCB pins output 1 at the same time when both the OAE and OBE bits are set to 1
- Either the OAE bit or OBE bit is set to 0.

The compare-target signals to generate the OABHF/OABLF flag are the compare match outputs (PWM outputs) signals before they are masked by the output disable function. When the output disable state is active, a compare match is performed continuously in the GPT and the OABHF/OABLF flag is updated in association with the result of the compared value.

22.2.17 General PWM Timer Buffer Enable Register (GTBER)

Address(es): GPT32EHm.GTBER 4007 8040h + 0100h × m (m = 0 to 3)
GPT32Em.GTBER 4007 8040h + 0100h × m (m = 4 to 7)
GPT32m.GTBER 4007 8040h + 0100h × m (m = 8 to 12)

- GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	BD[3]	BD[2]	BD[1]	BD[0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—		—	—	—		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BD[1]	BD[0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BD[0]	GTCCR Buffer Operation Disable	0: Buffer operation is enabled 1: Buffer operation is disabled.	R/W
b1	BD[1]	GTPR Buffer Operation Disable		R/W
b2	BD[2]	GTADTR Buffer Operation Disable		R/W
b3	BD[3]	GTDV Buffer Operation Disable		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17, b16	CCRA[1:0]	GTCCRA Buffer Operation	b17 b16 0 0: No buffer operation 0 1: Single buffer operation (GTCCRA ↔ GTCCRC) 1 x: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD).	R/W

Bit	Symbol	Bit name	Description	R/W
b19, b18	CCRB[1:0]	GTCCRB Buffer Operation	b19 b18 0 0: No buffer operation 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) 1 x: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF).	R/W
b21, b20	PR[1:0]	GTPR Buffer Operation	b21 b20 0 0: No buffer operation 0 1: Single buffer operation (GTPBR → GTPR) 1 x: Double buffer operation (GTPDBR → GTPBR → GTPR).	R/W
b22	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation	Writing 1 to this bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0.	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b25, b24	ADTTA[1:0]	GTADTRA Buffer Transfer Timing Select	• Triangle waves b25 b24 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough. • Saw waves b25 b24 0 0: No transfer Values other than 0 0: Transfer on underflow (during down-counting) or on overflow (during up-counting).	R/W
b26	ADTDA	GTADTRA Double Buffer Operation	0: Single buffer operation (GTADTBRA → GTADTRA) 1: Double buffer operation (GTADTDBRA → GTADTBRA → GTADTDRA).	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b29, b28	ADTTB[1:0]	GTADTRB Buffer Transfer Timing Select	• Triangle waves b29 b28 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough. • Saw waves b29 b28 0 0: No transfer Values other than 0 0: Transfer on underflow (in down-counting) or on overflow (in up-counting).	R/W
b30	ADTDB	GTADTRB Double Buffer Operation	0: Single buffer operation (GTADTBRB → GTADTRB) 1: Double buffer operation (GTADTDBRB → GTADTBRB → GTADTDRB).	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The GTBER provides settings for the buffer operation and must be set while the GTCNT operation is stopped.

BD[0] bit (GTCCR Buffer Operation Disable)

The BD[0] bit disables buffer operation using GTCCRA, GTCCRC, and GTCCRD combined and the buffer operation using GTCCRB, GTCCRE, and GTCCRF combined.

When GTDTCR.TDE is 1 and when BD [0] is set to 0, GTCCRB does not perform buffer operation and the GTCCRB register is automatically set to a compare match value for a negative-phase waveform with dead time.

BD[1] bit (GTPR Buffer Operation Disable)

The BD[1] bit disables buffer operation using GTPR, GTPBR, and GTPDBR combined.

BD[2] bit (GTADTR Buffer Operation Disable)

The BD[2] bit disables buffer operation using GTADTRA, GTADTBRA, and GTADTDBRA combined and buffer operation using GTADTRB, GTADTBRB, and GTADTDBRB combined. In event count operation, this bit is not

available and the GTADTR buffer operation is not performed. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

BD[3] bit (GTDV Buffer Operation Disable)

The BD[3] bit disables buffer operation using GTDVU and GTDBU combined and buffer operation using GTDVD and GTDBD combined.

When the GTDTCR.TDFER bit is set to 1, even if BD[3] is set to 0, buffer operation is not performed and the GTDVD value is set as a value of GTDVU automatically. In event count operation, this bit is not available and the GTDV buffer operation is not performed. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

CCRA[1:0] bits (GTCCRA Buffer Operation)

The CCRA[1:0] bits set buffer operation using GTCCRA, GTCCRC, and GTCCRD combined. When buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

CCRB[1:0] bits (GTCCRB Buffer Operation)

The CCRB[1:0] bits set buffer operation using GTCCRB, GTCCRE, and GTCCRF combined. When buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

PR[1:0] bits (GTPR Buffer Operation)

The PR[1:0] bits set buffer operation using GTPR, GTPBR, and GTPDBR combined. GPT32 does not have the PR[1] bit. Only single buffer operation setting by PR[0] bit is available for GPT32.

CCRSWT bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0 and is only valid when counting is stopped with a specified compare match operation.

ADTTA[1:0] bits (GTADTRA Buffer Transfer Timing Select)

The ADTTA[1:0] bits set the transfer timing for buffer operation of GTADTRA, GTADTBRA, and GTADTDBRA. These bits are not available in event count operation. Only GPT32EH and GPT32E have these bits. GPT32 does not have these bits.

ADTDA bit (GTADTRA Double Buffer Operation)

The ADTDA bit sets buffer operation using GTADTRA, GTADTBRA, and GTADTDBRA combined. This bit is not available in event count operation. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

ADTTB[1:0] bits (GTADTRB Buffer Transfer Timing Select)

The ADTTB[1:0] bits set the transfer timing for buffer operation of GTADTRB, GTADTBRB, and GTADTDBRB. These bits are not available in event count operation. Only GPT32EH and GPT32E have these bits. GPT32 does not have these bits.

ADTDB bit (GTADTRB Double Buffer Operation)

The ADTDB bit sets buffer operation using GTADTRB, GTADTBRB, and GTADTDBRB combined. This bit is not available in event count operation. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

Note 1. The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough).

22.2.18 General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register (GTITC)

Address(es): GPT32EHm.GTITC 4007 8044h + 0100h × m (m = 0 to 3)
GPT32Em.GTITC 4007 8044h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ITLA	GTCCRA Compare Match/Input Capture Interrupt Link	0: GPTn_OVF/GPTn_UDF interrupt skipping function is not linked 1: GPTn_OVF/GPTn_UDF interrupt skipping function is linked	R/W
b1	ITLB	GTCCRB Compare Match/Input Capture Interrupt Link	0: GPTn_OVF/GPTn_UDF interrupt skipping function is not linked 1: GPTn_OVF/GPTn_UDF interrupt skipping function is linked.	R/W
b2	ITLC	GTCCRC Compare Match Interrupt Link	0: GPTn_OVF/GPTn_UDF interrupt skipping function is not linked 1: GPTn_OVF/GPTn_UDF interrupt skipping function is linked.	R/W
b3	ITLD	GTCCRD Compare Match Interrupt Link	0: GPTn_OVF/GPTn_UDF interrupt skipping function is not linked 1: GPTn_OVF/GPTn_UDF interrupt skipping function is linked.	R/W
b4	ITLE	GTCCRE Compare Match Interrupt Link	0: GPTn_OVF/GPTn_UDF interrupt skipping function is not linked 1: GPTn_OVF/GPTn_UDF interrupt skipping function is linked.	R/W
b5	ITLF	GTCCRF Compare Match Interrupt Link	0: GPTn_OVF/GPTn_UDF interrupt skipping function is not linked 1: GPTn_OVF/GPTn_UDF interrupt skipping function is linked.	R/W
b7, b6	IVTC[1:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Function Select	b7 b6 0 0: Do not perform skipping 0 1: Count and skip both overflow and underflow for saw waves and crest for triangle waves 1 0: Count and skip both overflow and underflow for saw waves and trough for triangle waves 1 1: Count and skip both overflow and underflow for saw waves and both crest and trough for triangle waves.	R/W
b10 to b8	IVTT[2:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Count Select	b10 b8 0 0 0: No skipping 0 0 1: Skipping count of 1 0 1 0: Skipping count of 2 0 1 1: Skipping count of 3 1 0 0: Skipping count of 4 1 0 1: Skipping count of 5 1 1 0: Skipping count of 6 1 1 1: Skipping count of 7.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b12	ADTAL	GTADTRA A/D Converter Start Request Link	0: GPTn_OVF/GPTn_UDF interrupt skipping function is not linked 1: GPTn_OVF/GPTn_UDF interrupt skipping function is linked.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	ADTBL	GTADTRB A/D Converter Start Request Link	0: GPTn_OVF/GPTn_UDF interrupt skipping function is not linked 1: GPTn_OVF/GPTn_UDF interrupt skipping function is linked.	R/W
b31 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTITC register sets the skipping function for the GTCNT counter overflow (GTPR compare match) interrupt (GPTn_OVF) and underflow interrupt (GPTn_UDF). It also specifies whether to link other interrupts and A/D converter start requests with the GPTn_OVF/GPTn_UDF interrupt skipping function. The output disable request to POEG cannot be linked with the GPTn_OVF/GPTn_UDF interrupt skipping function. This register is not available in event count operation. Only GPT32EH and GPT32E have this register. GPT32 does not have this register and it is read as 0.

ITLA bit (GTCCRA Compare Match/Input Capture Interrupt Link)

The ITLA bit specifies whether to link the GTCCRA compare match/input capture interrupt (GTCIA) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLB bit (GTCCRB Compare Match/Input Capture Interrupt Link)

The ITLB bit specifies whether to link the GTCCRB compare match/input capture interrupt (GTCIB) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLC bit (GTCCRC Compare Match Interrupt Link)

The ITLC bit specifies whether to link the GTCCRC compare match interrupt (GTCIC) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLD bit (GTCCRD Compare Match Interrupt Link)

The ITLD bit specifies whether to link the GTCCRD compare match interrupt (GTCID) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLE bit (GTCCRE Compare Match Interrupt Link)

The ITLE bit specifies whether to link the GTCCRE compare match interrupt (GTCIE) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLF bit (GTCCRF Compare Match Interrupt Link)

The ITLF bit specifies whether to link the GTCCRF compare match interrupt (GTCIF) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

IVTC[1:0] bits (GPTn_OVF/GPTn_UDF Interrupt Skipping Function Select)

The IVTC[1:0] bits set the skipping function for the GTPR compare match (GTCNT overflow) interrupt (GPTn_OVF) and GTCNT counter underflow interrupt (GPTn_UDF).

IVTT[2:0] bits (GPTn_OVF/GPTn_UDF Interrupt Skipping Count Select)

The IVTT[2:0] bits set the skipping count for the GTPR compare match (GTCNT overflow) interrupt (GPTn_OVF) and GTCNT counter underflow interrupt (GPTn_UDF). When modifying the IVTT[2:0] bits, first set the IVTC[1:0] bits to 00b.

ADTAL bit (GTADTRA A/D Converter Start Request Link)

The ADTAL bit specifies whether to link the GTADTRA A/D converter start request with GPTn_OVF/GPTn_UDF interrupt skipping function.

ADTBL bit (GTADTRB A/D Converter Start Request Link)

The ADTBL bit specifies whether to link the GTADTRB A/D converter start request with GPTn_OVF/GPTn_UDF interrupt skipping function.

22.2.19 General PWM Timer Counter (GTCNT)

Address(es): GPT32EHm.GTCNT 4007 8048h + 0100h × m (m = 0 to 3)
GPT32Em.GTCNT 4007 8048h + 0100h × m (m = 4 to 7)
GPT32m.GTCNT 4007 8048h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCNT is a 32-bit read/write counter and can only be written to after counting is stopped. GTCNT must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited. GTCNT must be set within the range of 0 ≤ GTCNT ≤ GTPR.

22.2.20 General PWM Timer Compare Capture Register n (GTCCRn) (n = A to F)

Address(es): GPT32EHm.GTCCRA 4007 804Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRA 4007 804Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCCRA 4007 804Ch + 0100h × m (m = 8 to 12)
GPT32EHm.GTCCRB 4007 8050h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRB 4007 8050h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRB 4007 8050h + 0100h × m (m = 8 to 12)
GPT32EHm.GTCCRC 4007 8054h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRC 4007 8054h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRC 4007 8054h + 0100h × m (m = 8 to 12)
GPT32EHm.GTCCRE 4007 8058h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRE 4007 8058h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRE 4007 8058h + 0100h × m (m = 8 to 12)
GPT32EHm.GTCCRD 4007 805Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRD 4007 805Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCCRD 4007 805Ch + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRF 4007 8060h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRF 4007 8060h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRF 4007 8060h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTCCRn registers are read/write registers.

GTCCRA and GTCCRB are registers used for both output compare and input capture.

GTCCRC and GTCCRE are compare match registers that can also function as buffer registers for GTCCRA and GTCCRB.

GTCCRD and GTCCRF are compare match registers that can also function as buffer registers for GTCCRC and GTCCRE (double-buffer registers for GTCCRA and GTCCRB).

22.2.21 General PWM Timer Cycle Setting Register (GTPR)

Address(es): GPT32EHm.GTPR 4007 8064h + 0100h × m (m = 0 to 3)
GPT32Em.GTPR 4007 8064h + 0100h × m (m = 4 to 7)
GPT32m.GTPR 4007 8064h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPR is a read/write register that sets the maximum count value of GTCNT. For saw waves, the value of (GTPR + 1) is the cycle. For triangle waves, the value of (GTPR value × 2) is the cycle.

22.2.22 General PWM Timer Cycle Setting Buffer Register (GTPBR)

Address(es): GPT32EHm.GTPBR 4007 8068h + 0100h × m (m = 0 to 3)
GPT32Em.GTPBR 4007 8068h + 0100h × m (m = 4 to 7)
GPT32m.GTPBR 4007 8068h + 0100h × m (m = 8 to 12)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPBR is a read/write register that functions as a buffer register for GTPR.

22.2.23 General PWM Timer Cycle Setting Double-Buffer Register (GTPDBR)

Address(es): GPT32EHm.GTPDBR 4007 806Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTPDBR 4007 806Ch + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPDBR is a 32-bit read/write register that functions as a buffer register for GTPBR (double-buffer register for GTPR). Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read with the value after reset.

22.2.24 A/D Converter Start Request Timing Register n (GTADTRn) (n = A, B)

Address(es): GPT32EHm.GTADTRA 4007 8070h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTRA 4007 8070h + 0100h × m (m = 4 to 7)

GPT32EHm.GTADTRB 4007 807Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTADTRB 4007 807Ch + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The GTADTRn registers are 32-bit read/write registers that set the timing of A/D converter start request generation. When the GTADTRn value matches the GTCNT counter value, an A/D converter start request is generated. GTADTRm must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited. Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read with the value after reset.

22.2.25 A/D Converter Start Request Timing Buffer Register n (GTADTBRn) (n = A, B)

Address(es): GPT32EHm.GTADTBRA 4007 8074h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTBRA 4007 8074h + 0100h × m (m = 4 to 7)

GPT32EHm.GTADTBRB 4007 8080h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTBRB 4007 8080h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The GTADTBRn registers are 32-bit read/write registers that function as buffer registers for GTADTRn. GTADTBRn must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited. Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read with the value after reset.

22.2.26 A/D Converter Start Request Timing Double-Buffer Register n (GTADTDBRn) (n = A, B)

Address(es): GPT32EHm.GTADTDBRA 4007 8078h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTDBRA 4007 8078h + 0100h × m (m = 4 to 7)

GPT32EHm.GTADTDBRB 4007 8084h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTDBRB 4007 8084h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The GTADTDBRn registers are 32-bit read/write registers that function as buffer registers for GTADTBRn (double-buffer registers for GTADTR). GTADTDBRn must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited. Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read with the value after reset.

22.2.27 General PWM Timer Dead Time Control Register (GTDTCR)

Address(es): GPT32EHm.GTDTCR 4007 8088h + 0100h × m (m = 0 to 3)
GPT32Em.GTDTCR 4007 8088h + 0100h × m (m = 4 to 7)
GPT32m.GTDTCR 4007 8088h + 0100h × m (m = 8 to 12)

- GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TDE	Negative-Phase Waveform Setting	0: GTCCRB is set without using GTDVU and GTDVD 1: GTDVU and GTDVD set the compare match value for negative-phase waveform with automatic dead time in GTCCRB.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TDBUE	GTDVU Buffer Operation Enable	0: GTDVU buffer operation disabled 1: GTDVU buffer operation enabled.	R/W

Bit	Symbol	Bit name	Description	R/W
b5	TDBDE	GTDVD Buffer Operation Enable	0: GTDVD buffer operation disabled 1: GTDVD buffer operation enabled.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TDFER	GTDVD Setting	0: GTDVU and GTDVD are set separately 1: The value written to GTDVU to GTDVD is automatically set.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDTCR enables automatic setting of a compare match value for negative-phase waveform with dead time.

GPT32EH, GPT32E and GPT32 have dead time control function. GPT32 does not have the dead time buffer function and only GTDVU register is used for setting dead time value.

TDE bit (Negative-Phase Waveform Setting)

The TDE bit specifies whether to use GTDVU and GTDVD. When GTDVU and GTDVD are used, the compare match value for a negative-phase waveform with dead time obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (GTDVU and GTDVD), is automatically set in GTCCRB. The TDE bit setting is ignored in saw-wave PWM mode, and automatic setting does not take place.

The GTCCRB value is automatically set and has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB and the GTST.DTEF flag is set to 1. However, in triangle waves, when the obtained GTCCRB value exceeds the upper limit value, the GTST.DTEF flag is set to 0.

- Triangle waves:
  Upper limit value: GTPR - 1
  Lower limit value: 1 in up-counting, 0 in down-counting
- Saw-wave one-shot pulse mode:

  Upper limit value: GTPR
  Lower limit value: 0.

TDBUE bit (GTDVU Buffer Operation Enable)

The TDBUE bit enables buffer operation with GTDVU and GTDBU combined. The buffer transfer timing is the trough for triangle waves, and an overflow or underflow for saw waves.

Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

TDBDE bit (GTDVD Buffer Operation Enable)

The TDBDE bit enables buffer operation with GTDVD and GTDBD combined. The buffer transfer timing is the trough for triangle waves, and an overflow or underflow for saw waves. When this bit and the TDFER bit are set to 1 simultaneously, the TDFER bit setting is given priority.

Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

TDFER bit (GTDVD Setting)

The TDFER bit selects whether the value written to GTDVU is also set to GTDVD automatically.

Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

22.2.28 General PWM Timer Dead Time Value Register n (GTDVn) (n = U, D)

Address(es): GPT32EHm.GTDVU 4007 808Ch + 0100h x m (m = 0 to 3)
GPT32Em.GTDVU 4007 808Ch + 0100h x m (m = 4 to 7)
GPT32m.GTDVU 4007 808Ch + 0100h x m (m = 8 to 12)
GPT32EHm.GTDVD 4007 8090h + 0100h x m (m = 0 to 3)
GPT32Em.GTDVD 4007 8090h + 0100h x m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTDVn is a 32-bit read/write register that sets the dead time for generating PWM waveforms with dead time. Dead time for the transition in the first half is set in GTDVU and that in the second half is set in GTDVD.

Setting a GTDVn value greater than or equal to GTPR is prohibited. Setting a dead time value that exceeds the cycle is prohibited. The compare match value set by the automatic dead time setting function for a negative waveform can be confirmed by reading from GTCCRB.

When GTDVn is used, writing to GTCCRB is not allowed. When this register is set to 0, waveforms without dead time are output. GTDVn must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited. The way to rewrite GTDVn differs by GPT channel number.

GPT32EH0 to GPT32EH3 and GPT32E4 to GPT32E7

When GTDVm buffer operation is enabled, GTDBm can be written at anytime. GTDBm is transferred to GTDVm at the cycle end. When GTDVm buffer operation is disabled, stop the GPT using the CST bit in the GTCR register before changing GTDVm to a new value.

GPT328 to GPT3212

While the GPT is running, changing the GTDVU values is prohibited. To change GTDVU to a new value, stop the GPT with the CST bit in the GTCR register.

Only GPT32EH and GPT32E have the GTDVD register. GPT32 does not have the GTDVD register. This register is read with the value after reset.

22.2.29 General PWM Timer Dead Time Buffer Register n (GTDBn) (n = U, D)

Address(es): GPT32EHm.GTDBU 4007 8094h + 0100h × m (m = 0 to 3)
GPT32Em.GTDBU 4007 8094h + 0100h × m (m = 4 to 7)

GPT32EHm.GTDBD 4007 8098h + 0100h × m (m = 0 to 3)
GPT32Em.GTDBD 4007 8098h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTDBn is a 32-bit read/write register that functions as a buffer register for GTDVn.

Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read with the value after reset.

22.2.30 General PWM Timer Output Protection Function Status Register (GTSOS)

Address(es): GPT32EHm.GTSOS 4007 809Ch + 0100h x m (m = 0 to 3)
GPT32Em.GTSOS 4007 809Ch + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	SOS[1:0]	Output Protection Function Status	b1 b0 0 0: Normal operation 0 1: Protected state (set GTCCRA = 0 during transfer at trough or crest) 1 0: Protected state (set GTCCRA ≥ GTPR during transfer at trough) 1 1: Protected state (set GTCCRA ≥ GTPR during transfer at crest).	R
b31 to b2	—	Reserved	These bits are read as 0. Writing to these bits is ignored.	R

GTSOS is a register that indicates the status of the output protection function. The output protection function is enabled only when the dead time is automatically set (GTDTCR.TDE bit = 1) in triangle-wave mode.

Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read as 0000 0000h.

SOS[1:0] bits (Output Protection Function Status)

The SOS[1:0] bits indicate the status of the output protection function in triangle-wave PWM mode.

22.2.31 General PWM Timer Output Protection Function Temporary Release Register (GTSOTR)

Address(es): GPT32EHm.GTSOTR 4007 80A0h + 0100h x m (m = 0 to 3)
GPT32Em.GTSOTR 4007 80A0h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SOTR	Output Protection Function Temporary Release	0: Protected state is not released 1: Protected state is released.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTSOTR temporarily releases the protected state of GTIOCB pin output when output protection is set. The protected state can be released only when GTSOS.SOS[1:0] bits = 10b (protected state in which GTCCRA ≥ GTPR has occurred during transfer at trough). The protected state cannot be released in any other case.

Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read as 0000 0000h.

SOTR bit (Output Protection Function Temporary Release)

The SOTR bit specifies whether to temporarily release the protected state of GTIOCB pin output in an output protected state. When the SOTR bit is set to 1, the output protection function is canceled from the first trough. When the SOTR bit is set to 0, output protection resumes from the first trough.

22.2.32 Output Phase Switching Control Register (OPSCR)

Address(es): GPT_OPS.OPSCR 4007 8FF0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	—	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	UF	Input Phase Soft Setting	These bits set the input phase from the software settings. Setting these bits is valid when the OPSCR.FB bit = 1.	R/W
b1	VF			R/W
b2	WF			R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	U	Input U-Phase Monitor	These bits monitor the state of the input phase: OPSCR.FB = 0: External inputs that are synchronized by PCLKD OPSCR.FB = 1: The OPSCR.U, OPSCR.V, and OPSCR.W bits can read the OPSCR.UF. OPSCR.VF, and OPSCR.WF bits.	R
b5	V	Input V-Phase Monitor		R
b6	W	Input W-Phase Monitor		R
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	EN	Enable-Phase Output Control	0: Do not output (Hi-Z on external pin) 1: Output.*1	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	FB	External Feedback Signal Enable	This bit selects the input phase from the software settings or external input: 0: Select the external input 1: Select the software settings (OPSCR.UF, VF, WF).	R/W
b17	P	Positive-Phase Output (P) Control	0: Output level signal 1: Output level signal (PWM of GPT32EH0).	R/W
b18	N	Negative-Phase Output (N) Control	0: Output level signal 1: Output PWM signal (PWM of GPT32EH0).	R/W
b19	INV	Invert-Phase Output Control	0: Output positive logic (active-high) 1: Output negative logic (active-low).	R/W
b20	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b21	ALIGN	Input Phase Alignment	0: Input phase aligned to PCLKD 1: Input phase aligned to PWM.	R/W
b23, b22	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	GRP[1:0]	Output Disabled Source Selection	b25 b24 0 0: Select group A output disable source 0 1: Select group B output disable source 1 0: Select group C output disable source 1 1: Select group D output disable source.	R/W

Bit	Symbol	Bit name	Description	R/W
b26	GODF	Group Output Disable Function	0: This bit function is ignored 1: Group disable clears the OPSCR.EN bit.*1	R/W
b28, b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b29	NFEN	External Input Noise Filter Enable	0: Do not use a noise filter on the external input 1: Use a noise filter on the external input.	R/W
b31, b30	NFCS[1:0]	External Input Noise Filter Clock Selection	Noise filter sampling clock setting of the external input: b31 b30 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W

Note 1. When OPSCR.GODF = 1 and the signal value selected by the OPSCR.GRP[1:0] bits is high, the OPSCR.EN bit is set to 0.

The OPSCR sets the output of the signal waveform required for brushless DC motor control.

UF, VF, WF bits (Input Phase Soft Setting)

The UF, VF, and WF bits set the input phase from the software settings. When OPSCR.FB bit is 1, these bits are valid. The set value of the UF/VF/WF bits takes the place of the U/V/W external input.

U, V, W bits (Input Phase Monitor)

When the OPSCR.FB bit is 0, external inputs that are synchronized by PCLKD are monitored by these bits. When the OPSCR.FB bit is 1, the OPSCR.U, OPSCR.V, and OPSCR.W bits can read the OPSCR.UF, OPSCR.VF, and OPSCR.WF bits.

EN bit (Enable-Phase Output Control)

The EN bit controls the output enable signal output phase (positive phase/reverse phase).

When the OPSCR.EN bit is 1, the signal waveform is output.

When the OPSCR.EN bit is 0, first set OPSCR.FB, OPSCR.UF/VF/WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.RV, OPSCR.ALIGN, OPSCR.GRP, OPSCR.GODF, OPSCR.NFEN, and OPSCR.NFCS. Then, set the EN bit to 1. Also, when OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP bit is high, the OPSCR.EN bit is set to 0.

FB bit (External Feedback Signal Enable)

The FB bit selects the input phase from the software settings (OPSCR.UF, VF, WF) and external input such as a Hall element.

P bit (Positive-Phase Output (P) Control)

The P bit selects one of the level signal output (PWM of GPT32EH0) or PWM signal output for the positive-phase output (GTOUUP pin, GTOVUP pin, GTOWUP pin).

N bit (Negative-Phase Output (N) Control)

The N bit selects one of the level signal output (PWM of GPT32EH0) or PWM signal output for the negative-phase output (GTOULO pin, GTOVLO pin, GTOWLO pin).

INV bit (Invert-Phase Output Control)

The INV bit selects either positive logic (active-high) output or negative logic (active-low) output for the output phase.

ALIGN bit (Input Phase Alignment)

The ALIGN bit selects the PCLKD or PWM for the sampling of the input phase (input phase is specified in the OPSCR.FB bit). When OPSCR.ALIGN bit is 0, input phase is aligned to PCLKD.

Note: When PWM output is selected (OPSCR.P/N is 1) and the PCLKD input phase is aligned, the PWM pulse might be short-pulsed.

Note: When OPSCR.ALIGN bit is 1, input phase is aligned with PWM output.

GRP[1:0] bits (Output Disabled Source Selection)

The GRP[1:0] bits select the output disable source (A to D).

GODF bit (Group Output Disable Function)

When the GODF bit is 1 and the signal value selected by the OPSCR.GRP bit is high, the OPSCR.EN bit is set to 0. When the GODF bit is 0, the bit is ignored.

NFEN bit (External Input Noise Filter Enable)

The NFEN bit selects the noise filter for external input. When OPSCR.NFEN bit is 0, a noise filter is not used for the external input.

Note: When this bit is switched because of an unintentional internal edge, set the OPSCR.EN bit to 0.

NFCS[1:0] bits (External Input Noise Filter Clock Selection)

The NFCS[1:0] bits select the clock for the external input noise filter. When the OPSCR.NFEN bit is 1, noise filter sampling clock setting for external input is enabled.

1. Set the NFCS[1:0].
2. Wait for 2 cycles.
3. Set the OPSCR.EN bit to 1.

22.3 Operation

22.3.1 Basic Operation

Each channel has a 32-bit timer that performs a periodic count operation using the count clock and hardware sources. The count function provides both up-counting and down-counting. The GTPR controls the count cycle.

When the GTCNT counter value matches the value in GTCCRA or GTCCRB, the output from the associated pin GTIOCA or GTIOCB can be changed. GTCCRA or GTCCRB can be used as an input capture register with hardware resources.

GTCCRC and GTCCRD can function as buffer registers for GTCCRA. GTCCRE and GTCCRF can function as buffer registers for GTCCRB.

22.3.1.1 Counter operation

(1) Counter start and stop

The counter for each channel starts the count operation when GTCR.CST is set to 1. The GTCR.CST bit value is changed by the following sources:

- Writing to GTCR register
- Writing 1 to the bit in GTSTR associated with the GPT channel number when the GTSSR.CSTRT bit is set to 1
- Writing 1 to the bit in GTSTP associated with the GPT channel number when the GTPSR.CSTOP bit is set to 1
- The hardware source selected in the GTSSR register
- The hardware source selected in the GTPSR register.

(2) Periodic count operation in up-counting by count clock

The GTCNT counter in each channel starts up-counting when the associated GTCR.CST bit is set to 1 with the GTUPSR and GTDNSR registers set to 0000 0000h. When the GTCNT value changes from the GTPR value to 0 (overflow), the GTST.TCFPO flag is set to 1. When GTCNT overflows, up-counting resumes from 0000 0000h.

Figure 22.3 shows an example of a periodic count operation in up-counting.

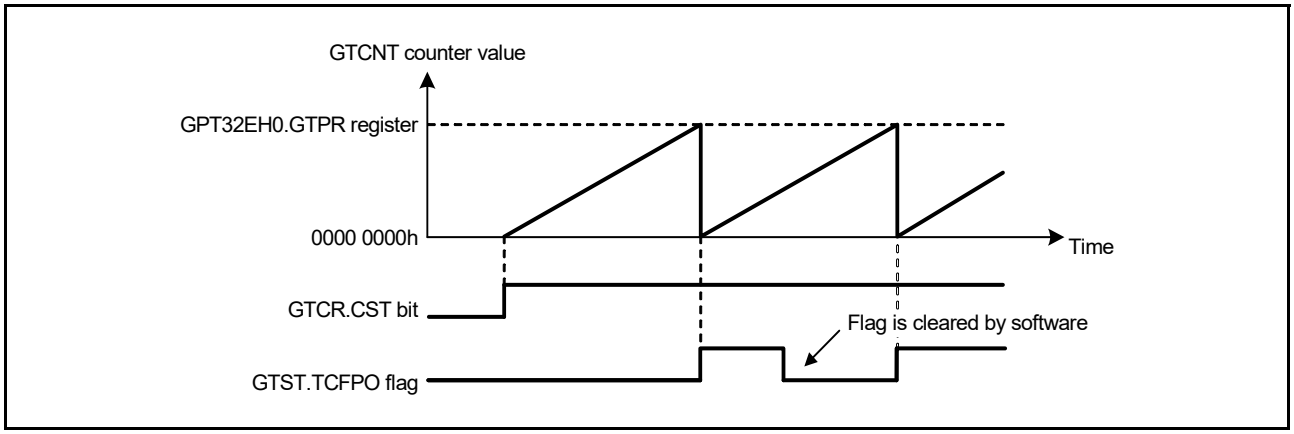


Figure 22.3 Example of periodic count operation in up-counting by the count clock

Figure 22.4 shows an example for setting periodic count operation in up-counting.

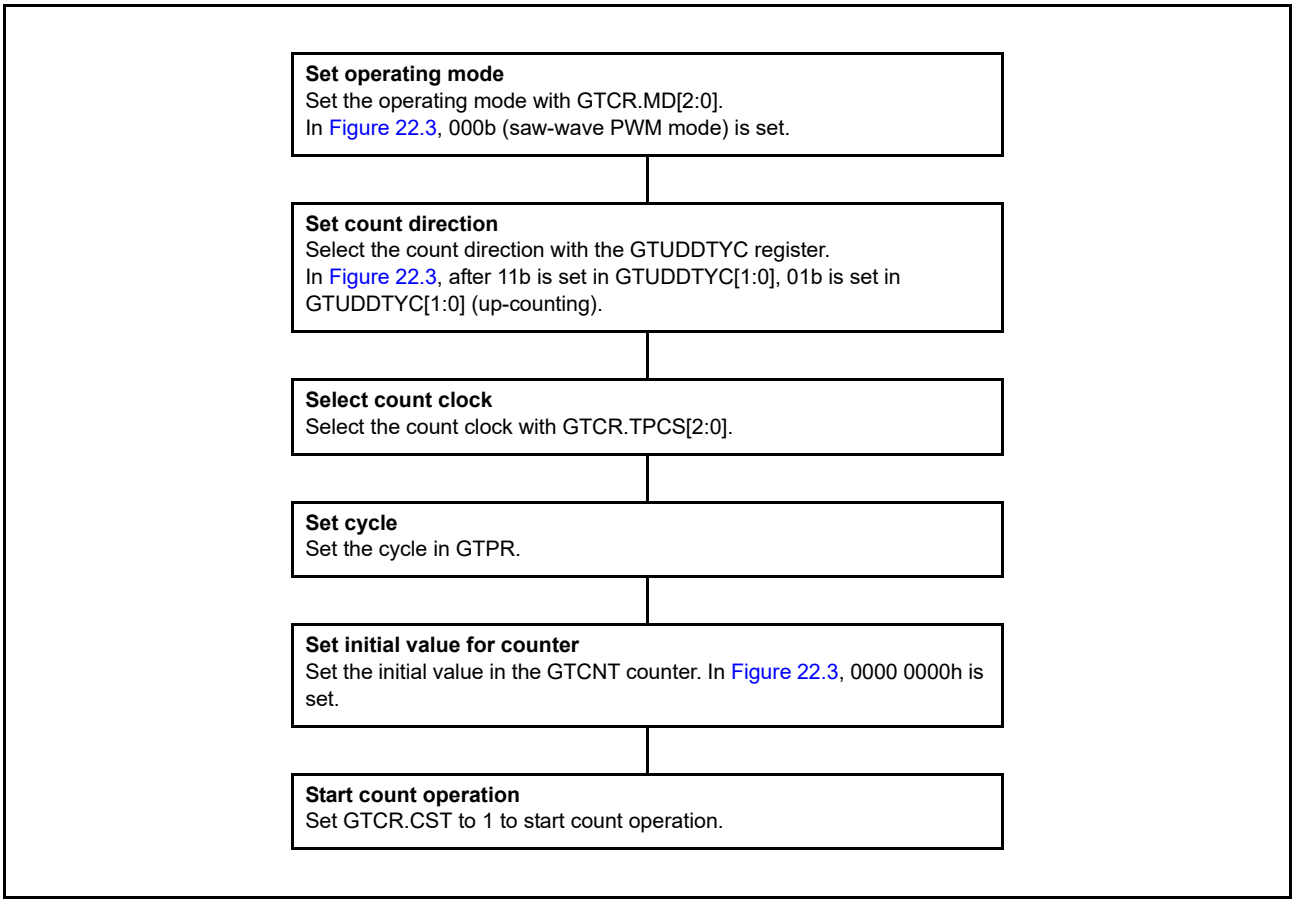


Figure 22.4 Example setting for a periodic count operation in up-counting by the count clock

(3) Periodic count operation in down-counting by count clock

The GTCNT counter in each channel can perform down-counting by setting GTUDDTYC.UD with the GTUPSR and GTDNSR registers set to 0000 0000h. When GTCNT changes from 0 to the GTPR value (underflow), GTST.TCFPU is set to 1. When the GTCNT counter underflows, down-counting resumes from the GTPR value.

Figure 22.5 shows an example of periodic count operation in down-counting by the count clock.

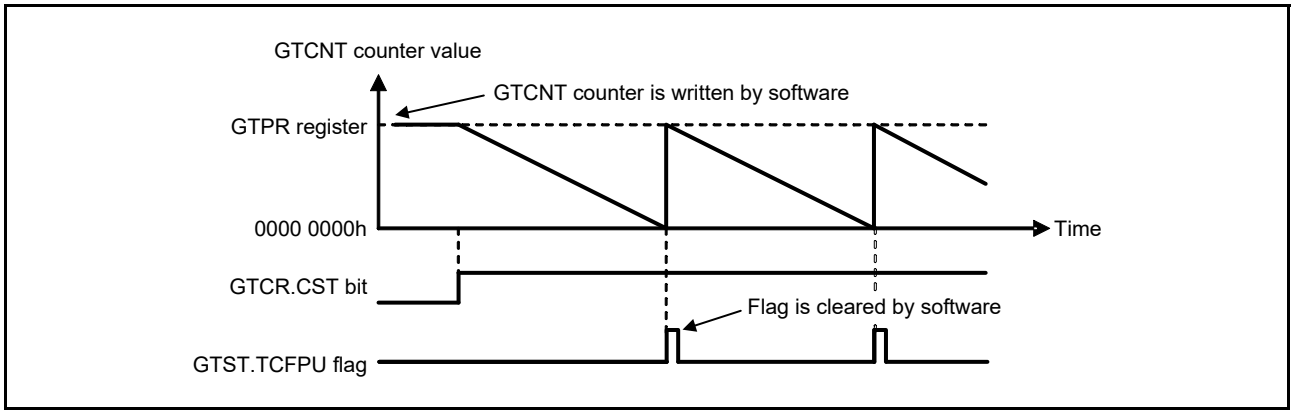


Figure 22.5 Example of periodic count operation in down-counting by the count clock

Figure 22.6 shows an example setting for periodic count operation in down-counting by the count clock.

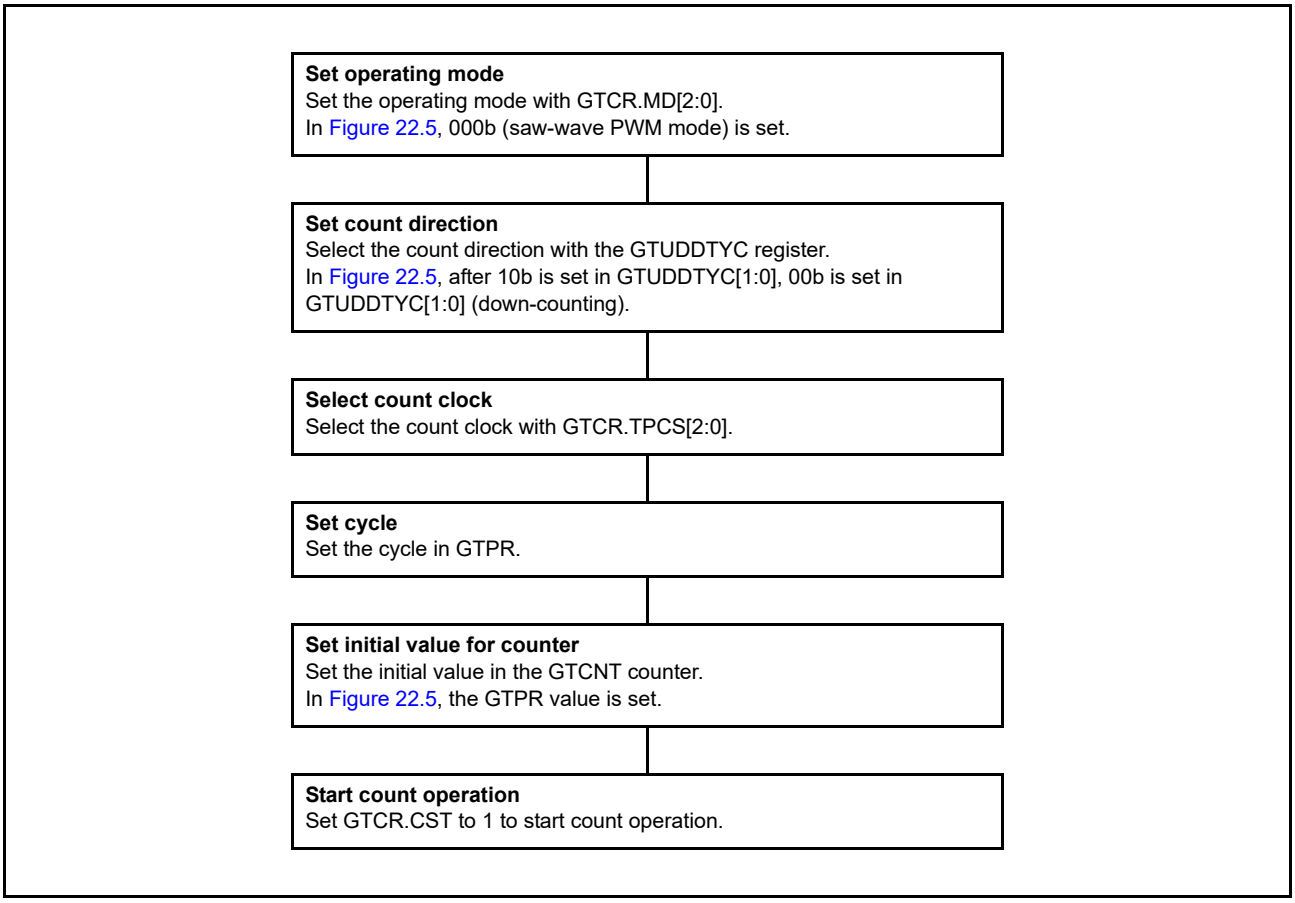


Figure 22.6 Example setting for periodic count operation in down-counting by count clock

(4) Event count operation in up-counting using hardware sources

The GTCNT counter in each channel can perform up-counting using hardware sources as set in GTUPSR.

When GTUPSR is set to enable, the count clock selected in GTCR.TPCS[2:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The overflow behavior for up-counting using hardware sources is the same as for up-counting by the count clock.

When GTCR.CST bit is set to 1 to count up using hardware sources, the count operation is enabled. When GTCR.CST is set to 1, the counter cannot count up for 1 clock cycle as specified in GTCR.TPCS[2:0] because the count operation is

synchronized by the count clock selected in GTCR.TPCS[2:0]. When count up with 1 PCLKD clock delay, set GTCR.TPCS[2:0] to 000b.

Figure 22.7 shows an example of a periodic count operation in up-counting by a hardware source (rising edge of the GTETRGA pin).

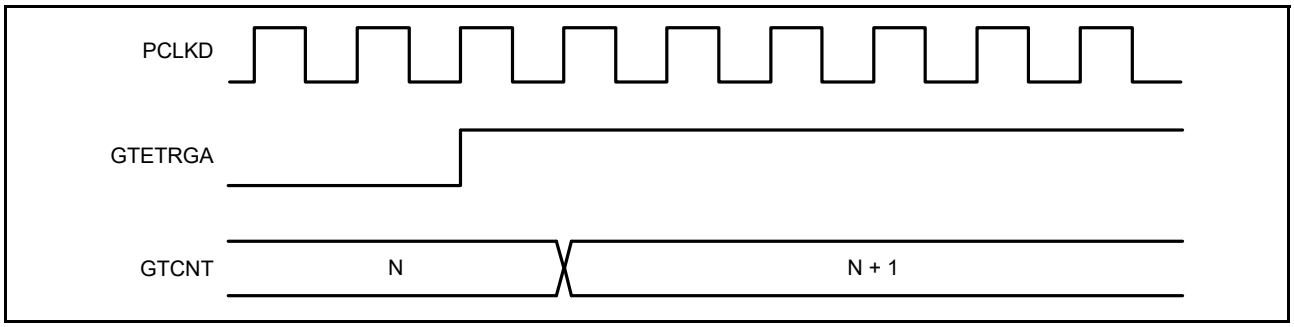


Figure 22.7 Example of periodic count operation in up-counting using hardware sources

Figure 22.8 shows an example setting for periodic count operation in up-counting by a hardware source.

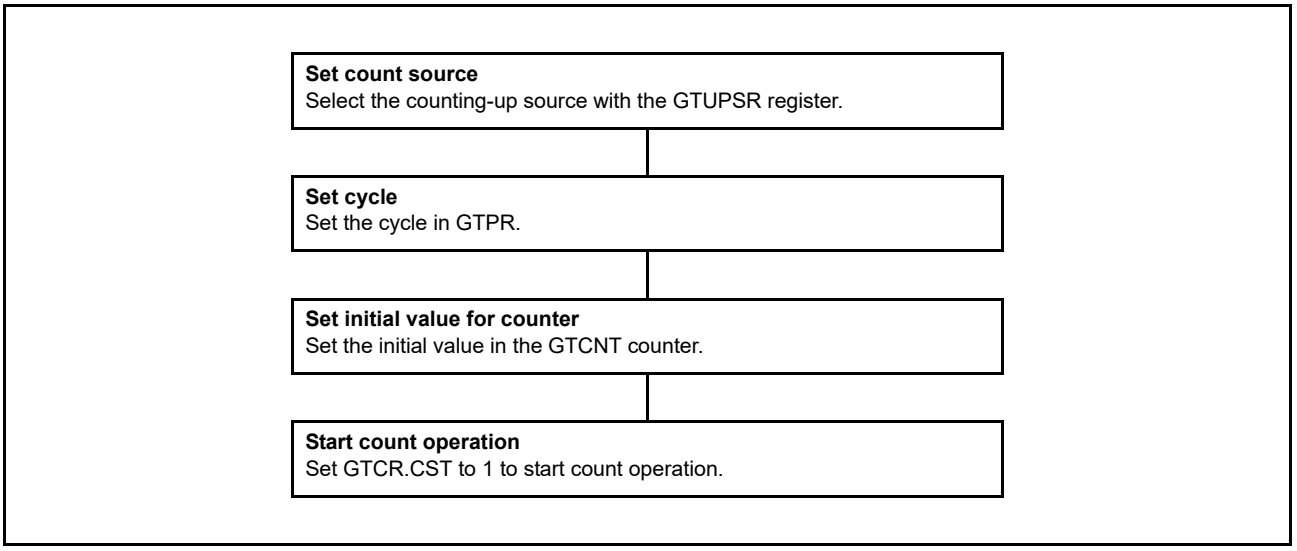


Figure 22.8 Example setting for an event count operation in up-counting using hardware sources

(5) Event count operation in down-counting using hardware sources

The GTCNT counter in each channel can perform down-counting using hardware sources set in the GTDNSR register.

When GTDNSR is set to enable, the count clock selected in GTCR.TPCS[2:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The underflow behavior for down-counting using hardware sources is the same as for down-counting by the count clock.

When GTCR.CST bit is set to 1 to count down using hardware sources, the count operation is enabled. When GTCR.CST is set to 1, the counter cannot count down for 1 clock cycle as specified in GTCR.TPCS[2:0] because the count operation is synchronized with the count clock selected in GTCR.TPCS[2:0]. When count down with 1 PCLKD clock delay, set GTCR.TPCS[2:0] to 000b.

Figure 22.9 shows an example of a periodic count operation in down-counting by a hardware source (rising edge of the GTETRGA pin).

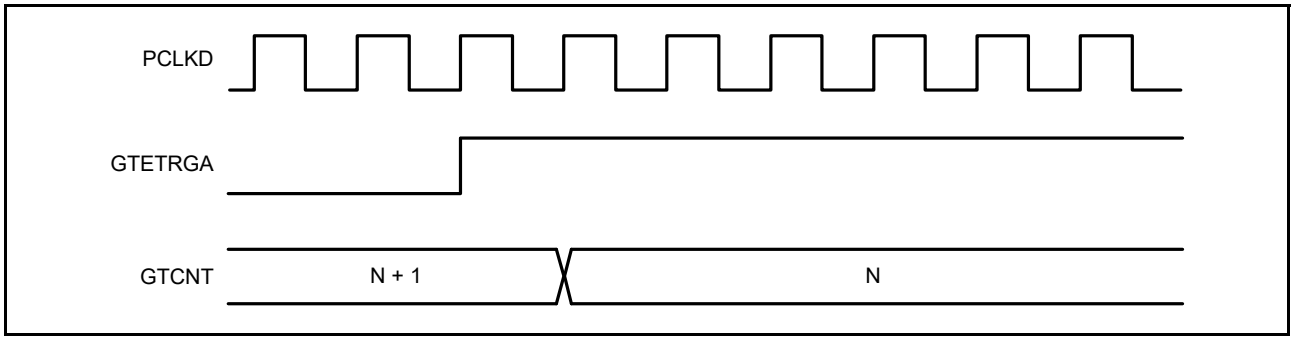


Figure 22.9 Example of event count operation in down-counting using hardware sources

Figure 22.10 shows an example setting for a periodic count operation in down-counting using a hardware source.

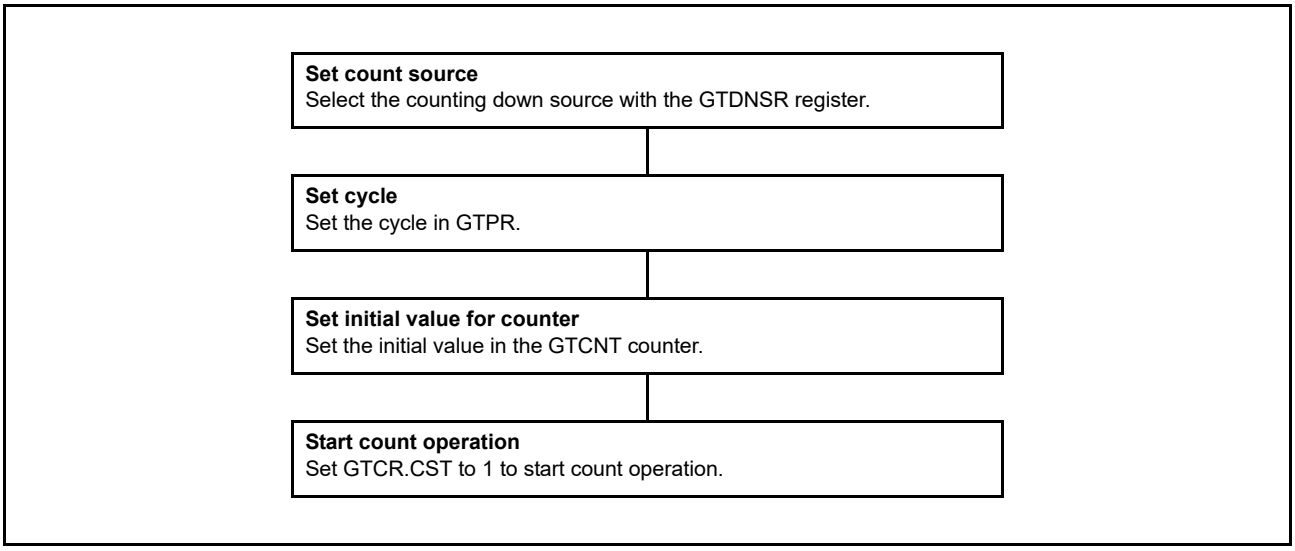


Figure 22.10 Example setting for an event count operation in down-counting using hardware sources

(6) Counter clear operation

The counter of each channel is cleared by the following sources:

- Writing 0 to GTCNT register
- Writing 1 to the bit in GTCLR associated with the GPT channel number when the GTCSR.CCLR bit is set to 1
- The hardware source selected in GTCSR register.

Writing to the GTCNT register is prohibited during count operation. The GTCNT counter can be cleared both by writing 1 to the GTCLR and by the clear request of hardware sources, whether GTCNT is counting (GTCR.CST is 1) or not (GTCR.CST is 0).

For saw waves selected by setting GTCR.MD[2:0] and the count direction flag showing down-counting (GTST.TUCF is 0), the GTCNT register is set to the value of the GTPR register when writing 1 to the GTCLR register or when clearing by hardware sources is performed.

When not in saw wave mode and down-counting, the GTCNT register is set to 0 when writing 1 to the GTCLR register and when clearing by hardware sources is performed.

In event count operation when at least 1 bit in the GTUPSR or GTDNSR is set to 1, after clear sources occur, both writing to the GTCLR register and clearing by hardware sources are performed immediately to synchronize with PCLKD. If other settings are used, clear is synchronized with the counter clock selected in GTCR.TPCS[2:0].

22.3.1.2 Waveform output by compare match

Compare match means that the GTCNT counter value matches the value of GTCCRA or GTCCRB. When a compare match occurs, the compare match flag is generated synchronously with the count clock, including the event count. At the same time the GPT can output low, high, or toggle output from the associated GTIOCA or GTIOCB output pin. In addition, the GTIOCA or GTIOCB pin output can be low, high, or toggled at the cycle end, which is determined by GTPR.

The cycle end is:

- For saw waves in up-counting — when GTCNT changes from the GTPR value to 0 (overflow)
- For saw waves in down-counting — when GTCNT changes from 0 to the GTPR value (underflow)
- For saw waves — when the GTCNT counter is cleared
- For triangle waves — when the GTCNT changes from 0 to 1 (trough).

(1) Low output and high output

Figure 22.11 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.

In this example, the GPT32EH0.GTCNT counter performs up-counting, and settings are made so that high is output from the GTIOC0A pin by a GPT32EH0.GTCCRA compare match, and low is output from the GTOC0B pin by a GPT32EH0.GTCCRB compare match. The pin level does not change when the specified level and pin level match.

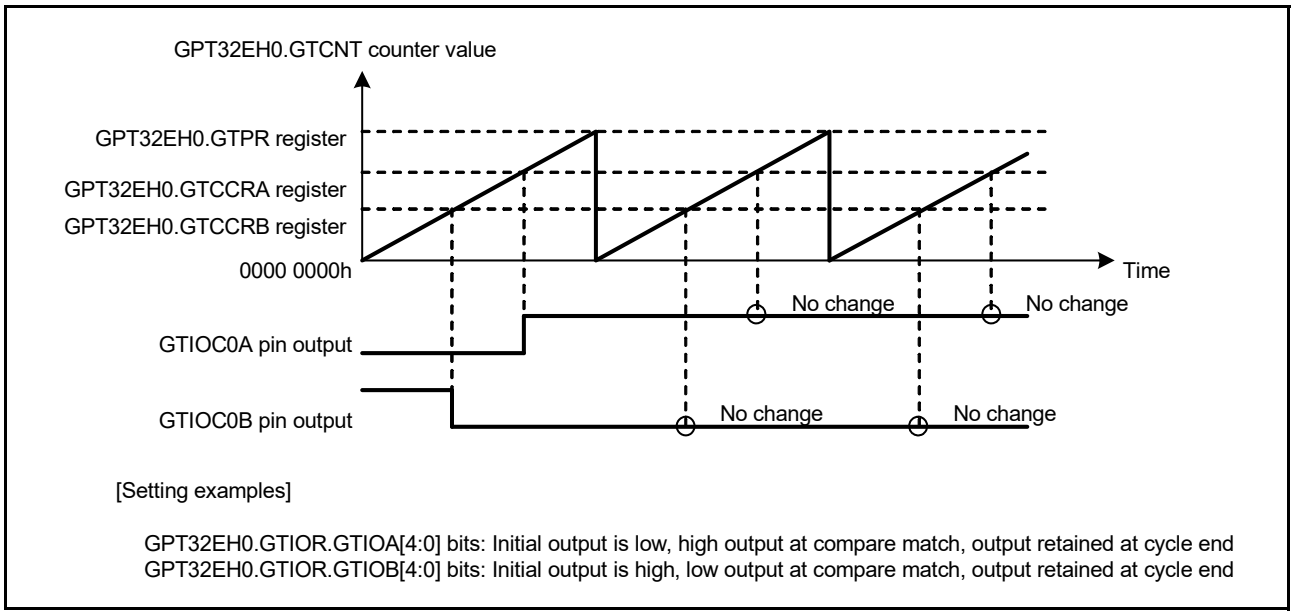


Figure 22.11 Example of low output and high output operation

Figure 22.12 shows an example setting for low output and high output operation.

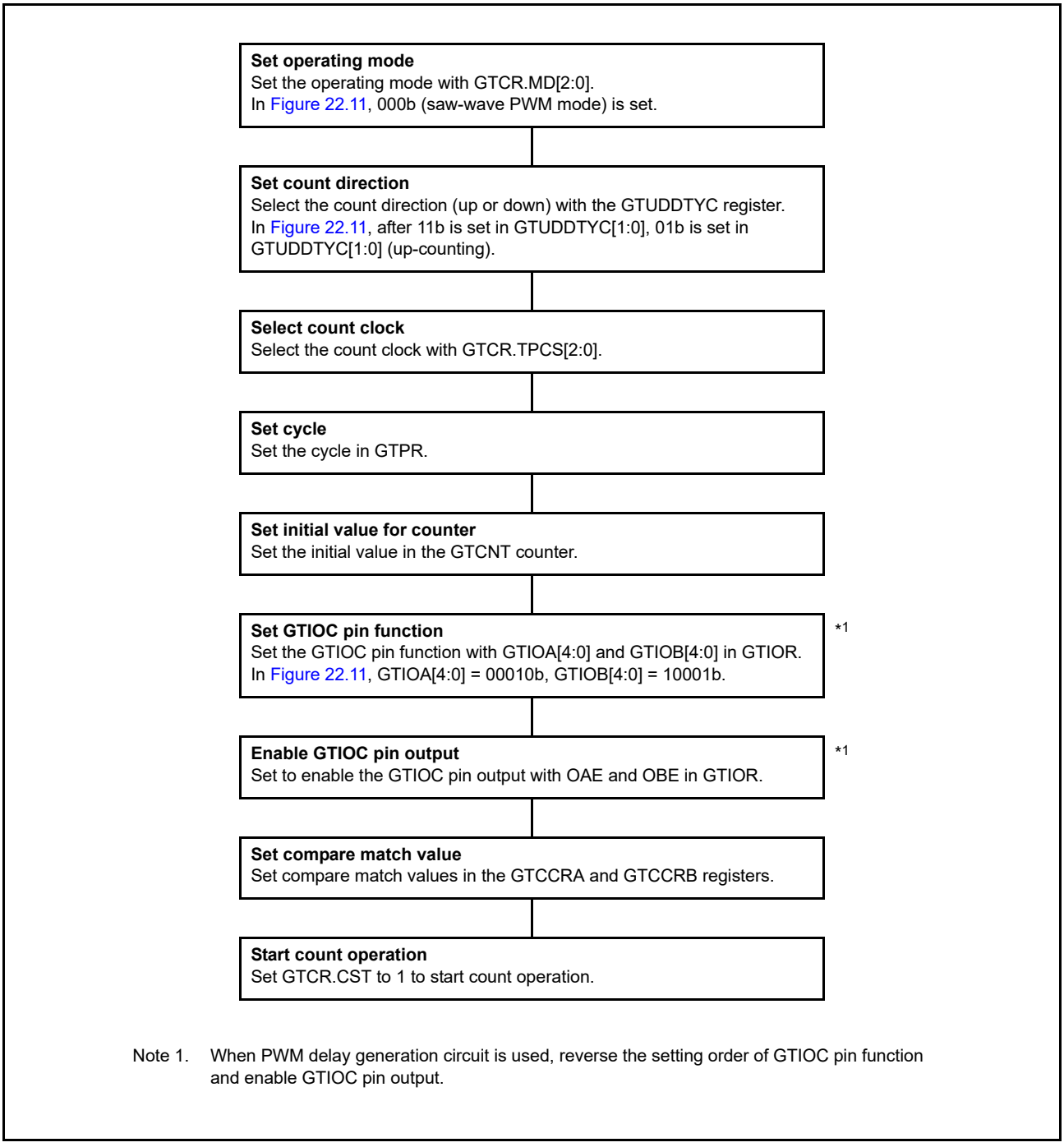


Figure 22.12 Example setting for low output and high output operation

(2) Toggled output

Figure 22.13 and Figure 22.14 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB. In Figure 22.13, the GPT32EH0.GTCNT counter performs up-counting, and settings are made so that the GTIOC0A pin output by a GPT32EH0.GTCCRA compare match and GTIOC0B pin output by a GPT32EH0.GTCCRB compare match are toggled.

In Figure 22.14, the GPT32EH0.GTCNT counter performs up-counting, and settings are made so that the GTIOC0A output is toggled by a compare match of GPT32EH0.GTCCRA and the GTIOC0B output is toggled at the cycle end.

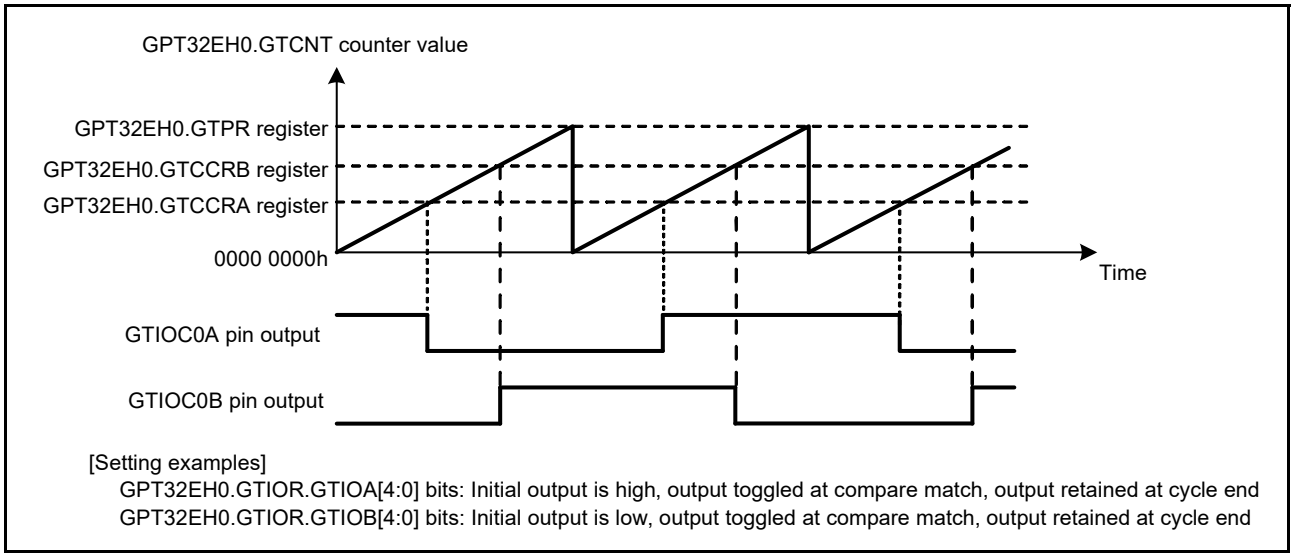


Figure 22.13 Example of toggled output operation (1)

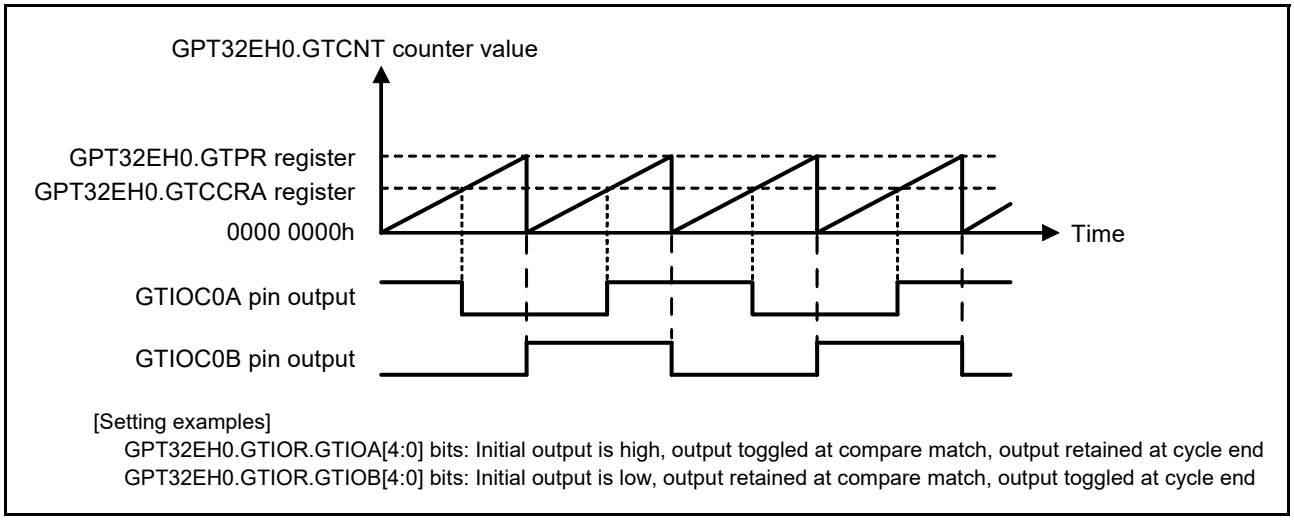


Figure 22.14 Example of toggled output operation (2)

Figure 22.15 shows an example setting for toggled output operation.

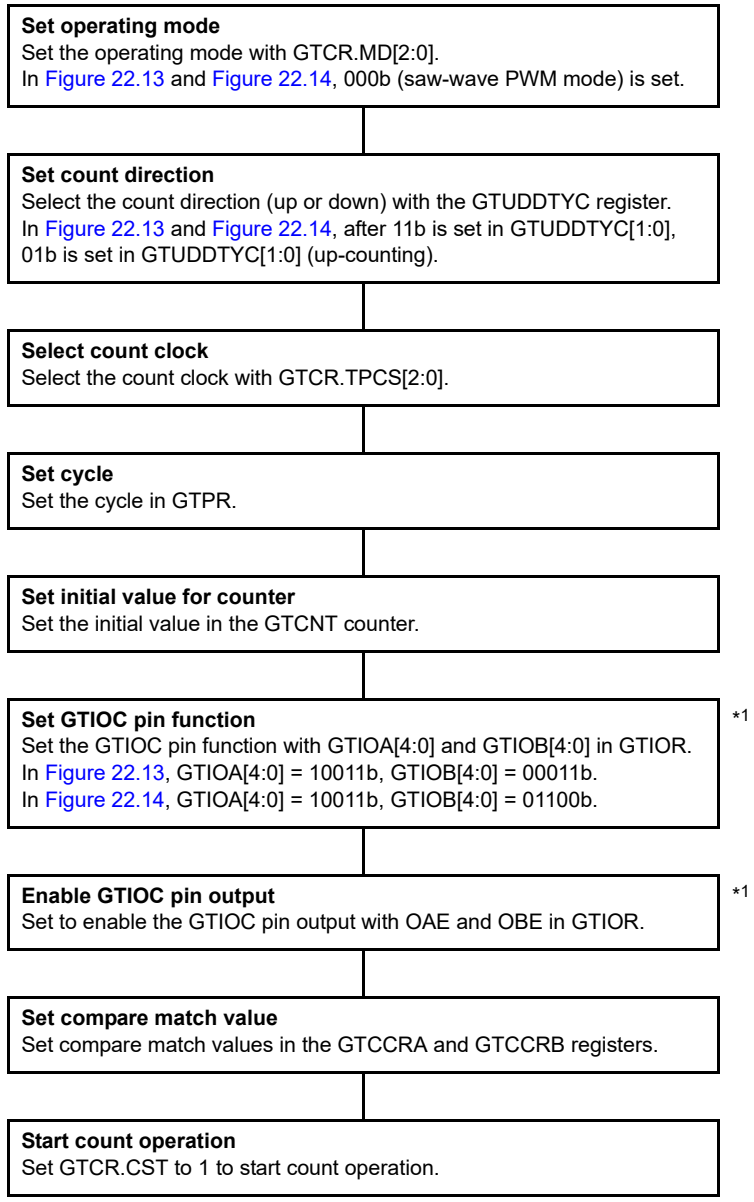


Figure 22.15 Example setting for toggled output operation

22.3.1.3 Input capture function

The GTCNT counter value can be transferred to either GTCCRA or GTCCRB on detection of the hardware source that is set in GTICASR and GTICBSR.

Figure 22.16 shows an example of the input capture function.

In this example, the GPT32EH0.GTCNT counter performs up-counting by the count clock, and settings are made so that an input capture is performed to GTICCRA at both edges of the GTIOC0A input pin and to GTICCRB on the rising edge of the GTIOC0B input pin.

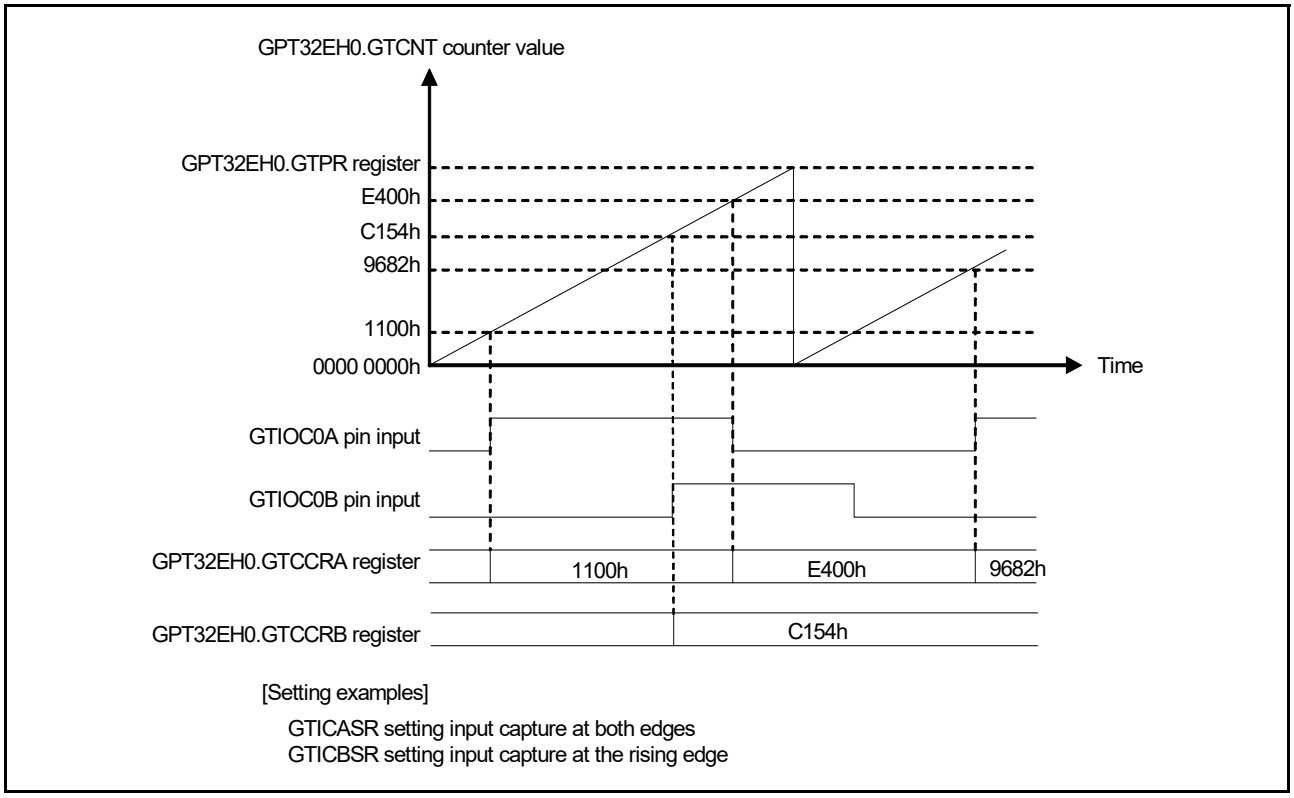


Figure 22.16 Example of input capture operation

Figure 22.17 shows an example setting for an input capture operation with count operation by the count clock.

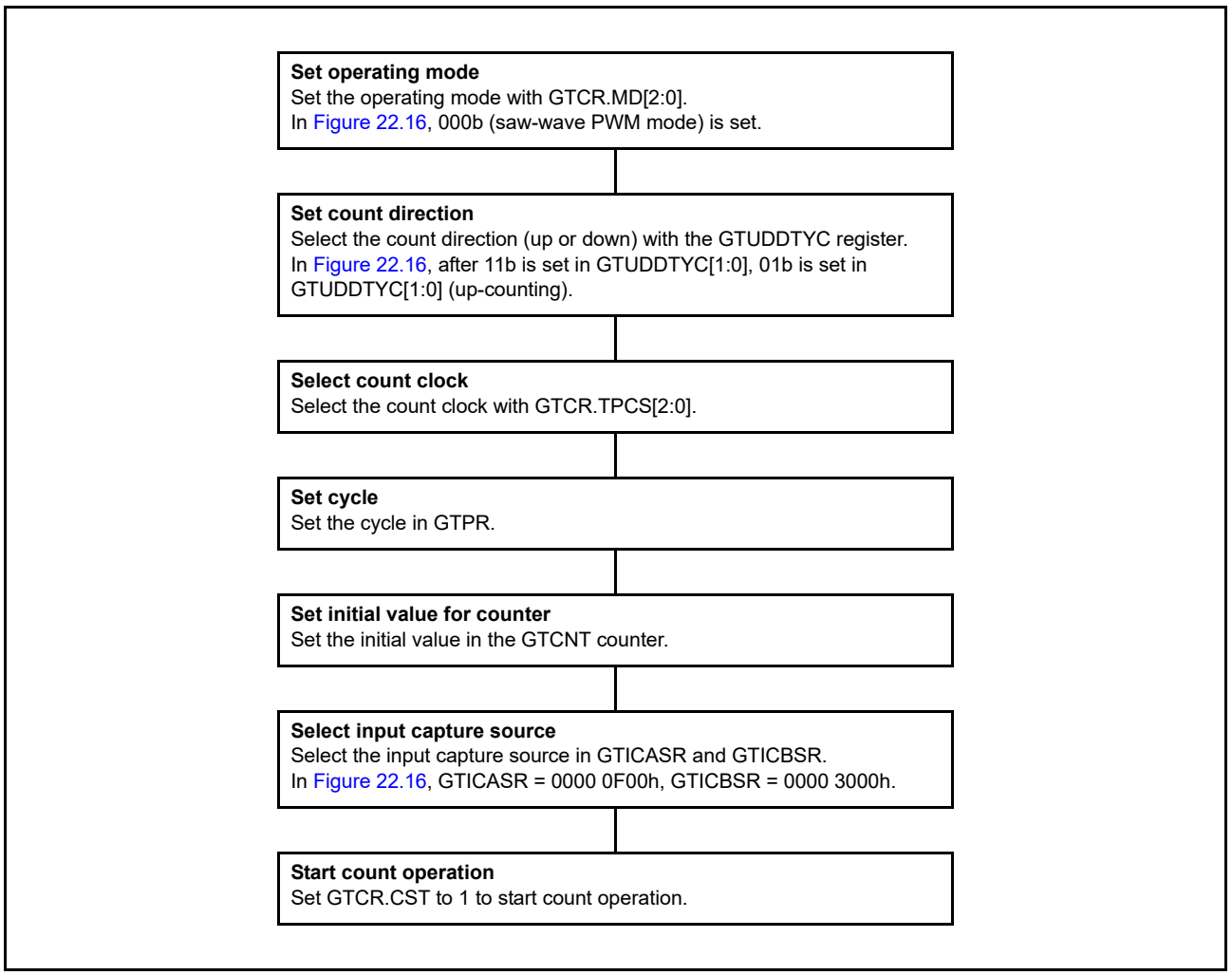


Figure 22.17 Example setting for input capture operation

22.3.2 Buffer Operation

The following buffer operations can be set with GTBER:

- GTPR, GTPBR, and GTPDBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF
- GTADTRA, GTADTBRA, and GTADTDBRA
- GTADTRB, GTADTBRB, and GTADTDBRB.

The following buffer operations can be set with GTDTCR:

- GTDVU and GTDBU
- GTDVD and GTDBD.

22.3.2.1 GTPR register buffer operation

GTPBR can function as a buffer register for GTPR, and GTPDBR can function as a buffer register for GTPBR (double-buffer register for GTPR). The buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count, and at a trough in triangle-wave mode.

In saw-wave mode or in event count, the buffer transfer is performed when the following counter clear operations occur during counting:

- Clear by hardware sources (the clear source is selected in GTCSR[23:0])
- Clear by software (when GTCSR.CCLR bit is 1 and GTCLR[n] bit is set to 1, n = channel number).

To set GTPR to function as double buffer, set GTBER.PR[1:0] to 10b or 11b. To set GTPR to not function as a buffer, set GTBER.PR[1:0] to 00b.

Figure 22.18 to Figure 22.20 show examples of GTPR buffer operation, and Figure 22.21 shows an example setting for GTPR buffer operation.

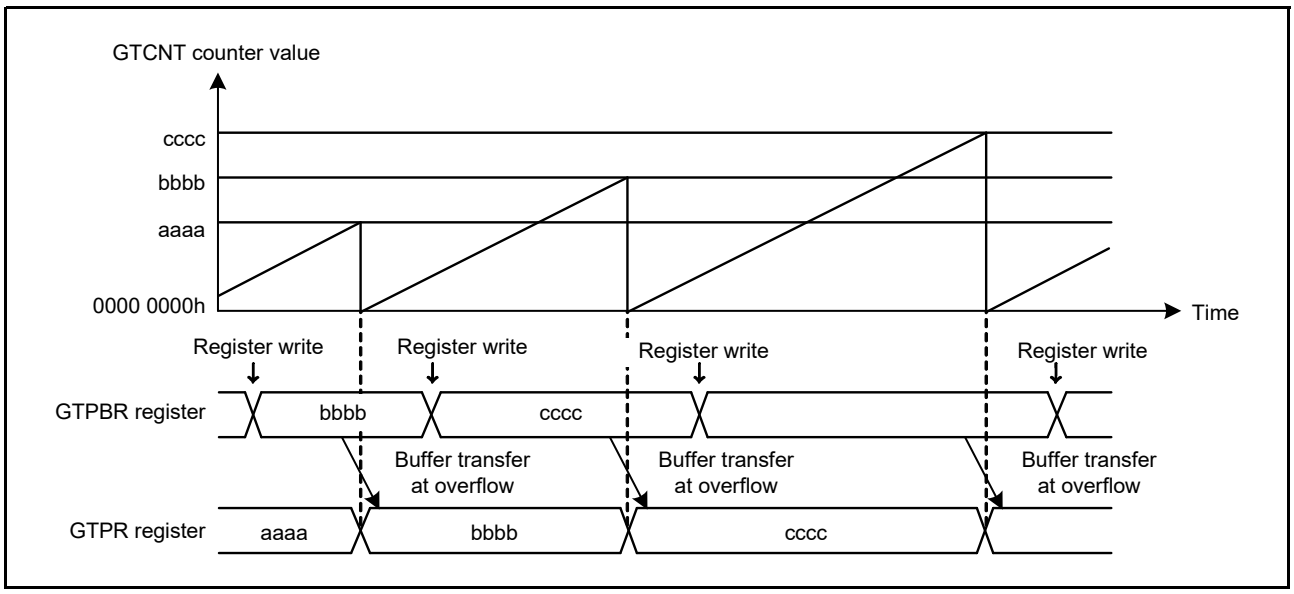


Figure 22.18 Example of GTPR buffer operation with saw waves in up-counting

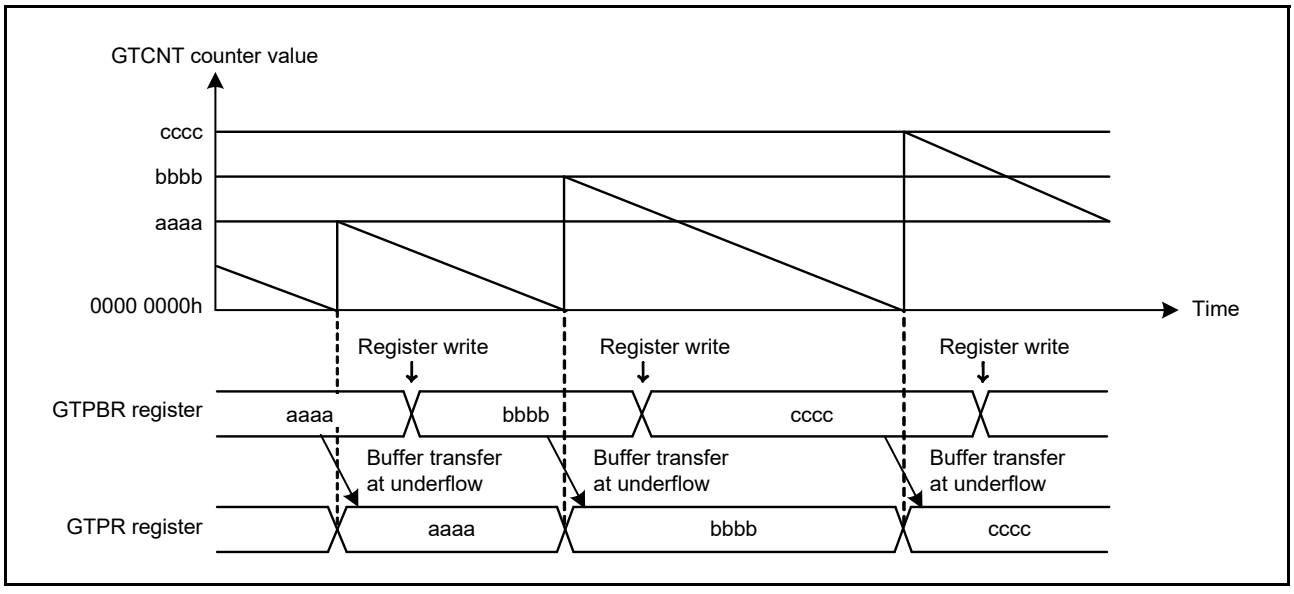


Figure 22.19 Example of GTPR buffer operation with saw waves in down-counting

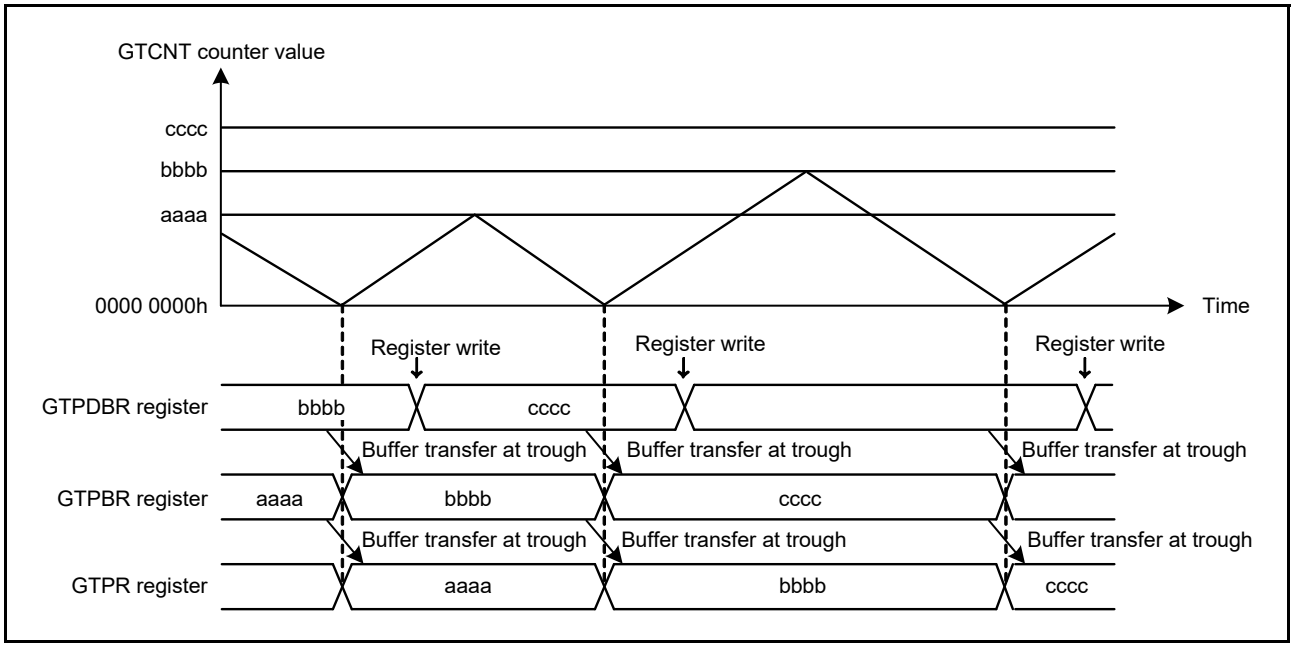


Figure 22.20 Example of GTPR double buffer operation with triangle waves

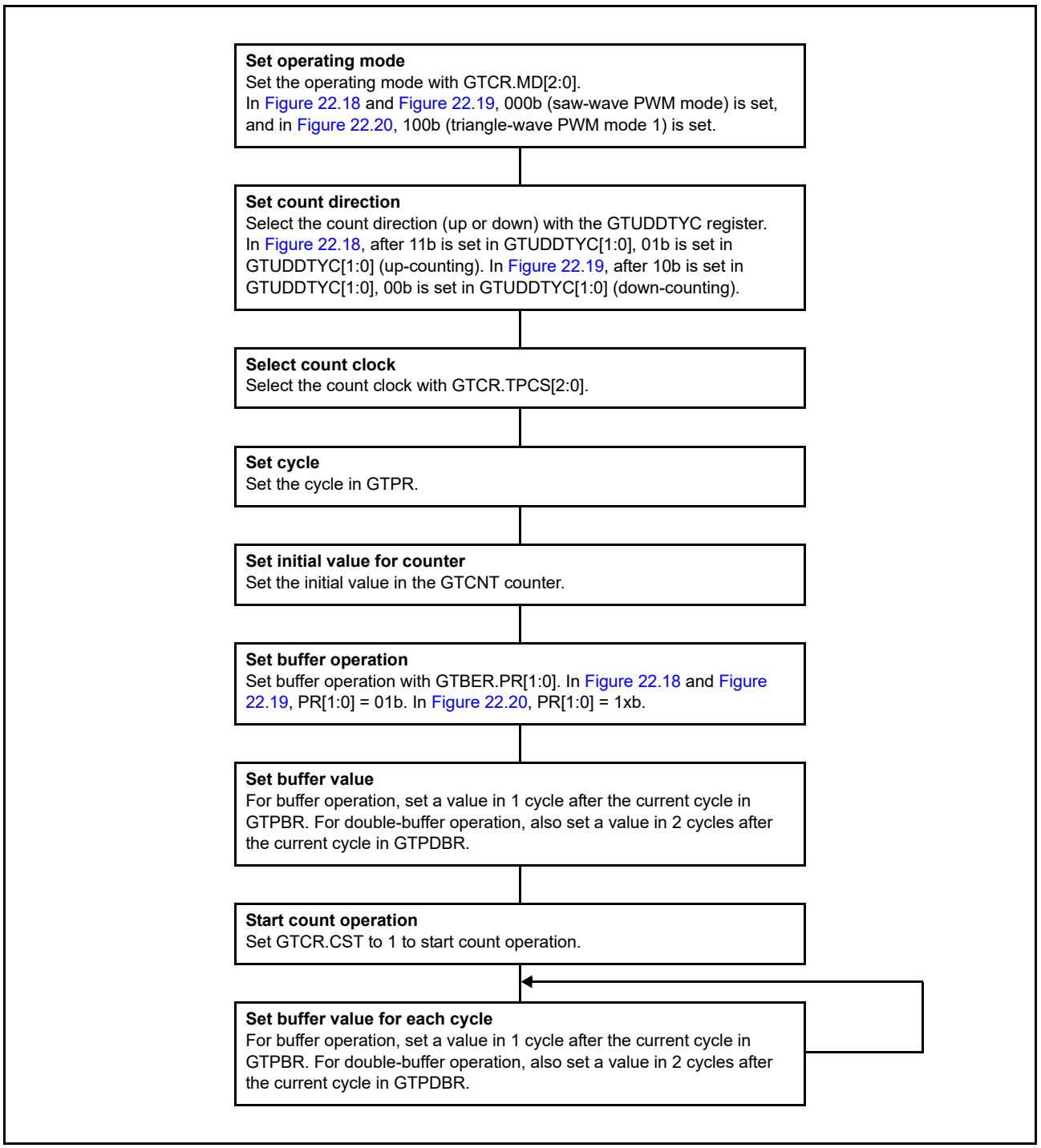


Figure 22.21 Example setting for GTPR buffer operation

22.3.2.2 Buffer operation for GTCCRA and GTCCRB

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).

To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For single-buffer operation, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 01b. To set GTCCRA or GTCCRB to not function as a buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 00b.

(1) When GTCCRA or GTCCRB functions as an output compare register

Buffer transfer occurs in the following situations:

- Buffer transfer by overflow or underflow
  Buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count operation. In triangle-wave mode, buffer transfer is performed at a trough (triangle-wave PWM mode 1) or a crest and trough (triangle-wave PWM mode 2).
- Buffer transfer by counter clear
  In saw-wave mode or in event count operation, during counting, buffer transfer (which is the same as an overflow during up-counting or an underflow during down-counting) is performed by the counter clear sources similar to the case shown in section 22.3.2.1, GTPR register buffer operation. In triangle-wave mode, buffer transfer is not performed by the counter clear.
- Forcible buffer transfer
  When GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the GTCCRA and the GTCCRB register buffer transfers are performed forcibly in saw-wave mode, in event count operation, and in triangle-wave mode. Additionally, buffer transfer from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B are performed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3.

Figure 22.22 to Figure 22.24 show examples of GTCCRA and GTCCRB buffer operation and Figure 22.25 shows an example setting for GTCCRA and GTCCRB buffer operation.

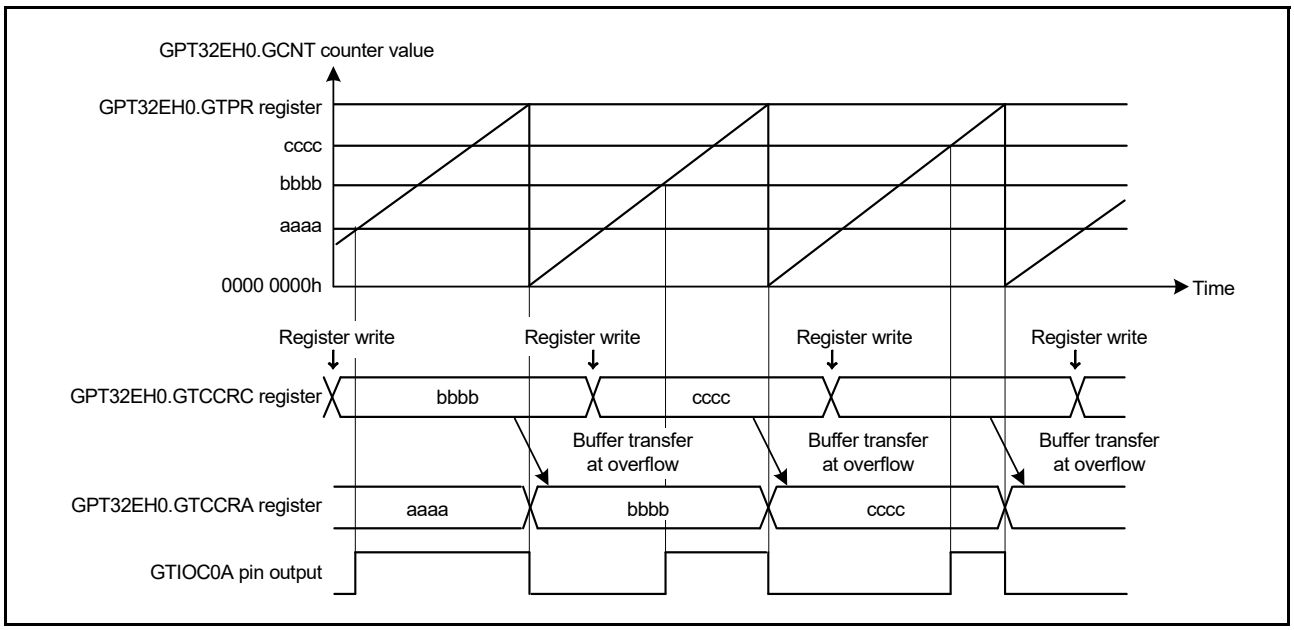


Figure 22.22 Example of GTCCRA and GTCCRB buffer operation with output compare, saw waves in up-counting, high output at GTCCRA compare match, and low output at cycle end

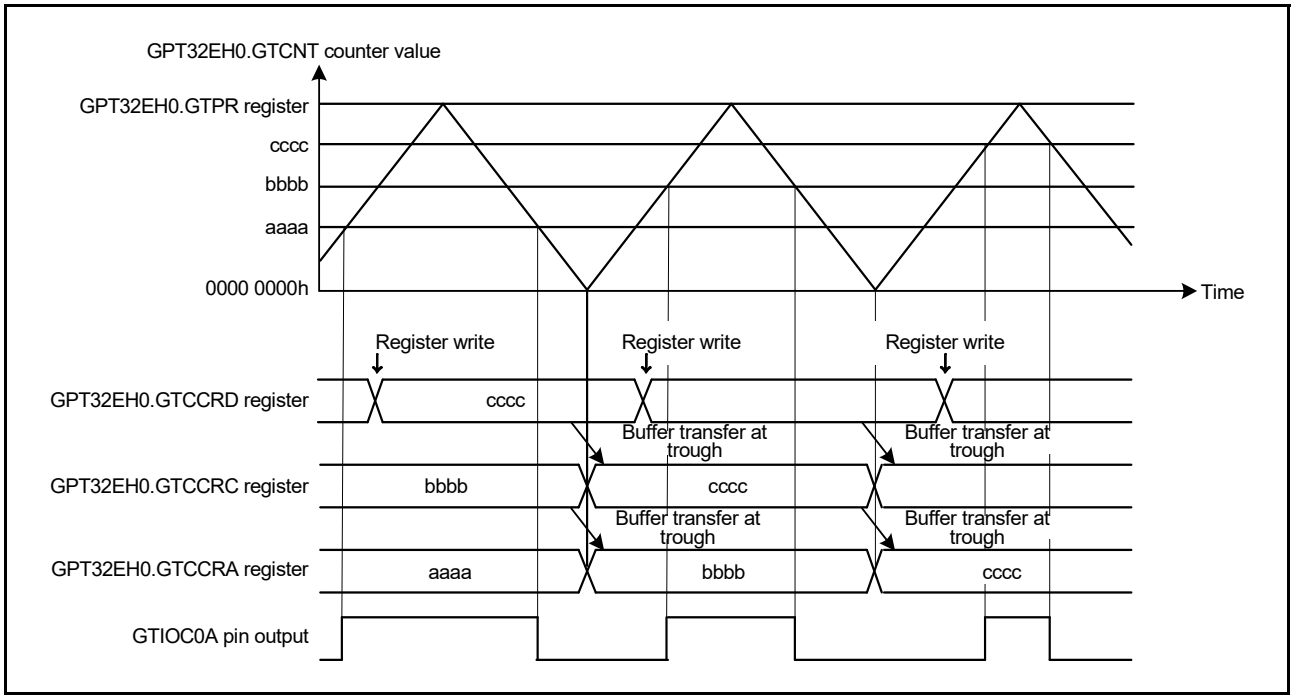


Figure 22.23 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at trough, output toggled at GTCCRA compare match, and output retained at cycle end

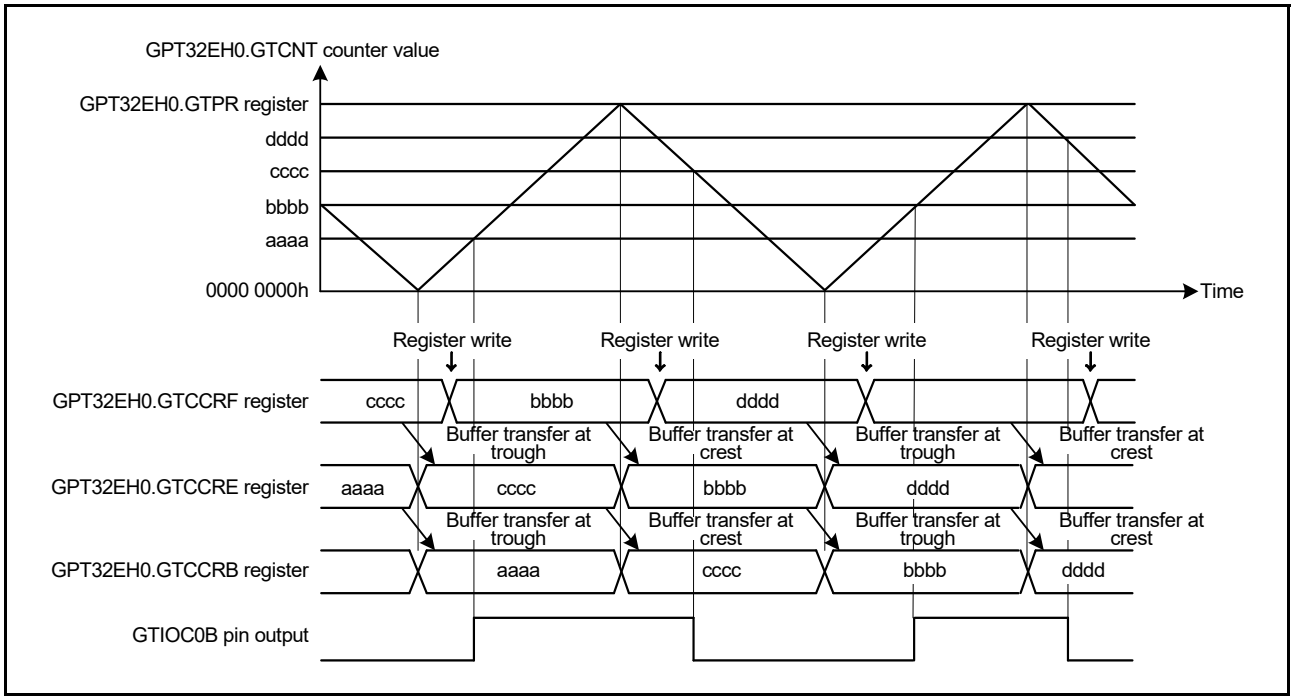
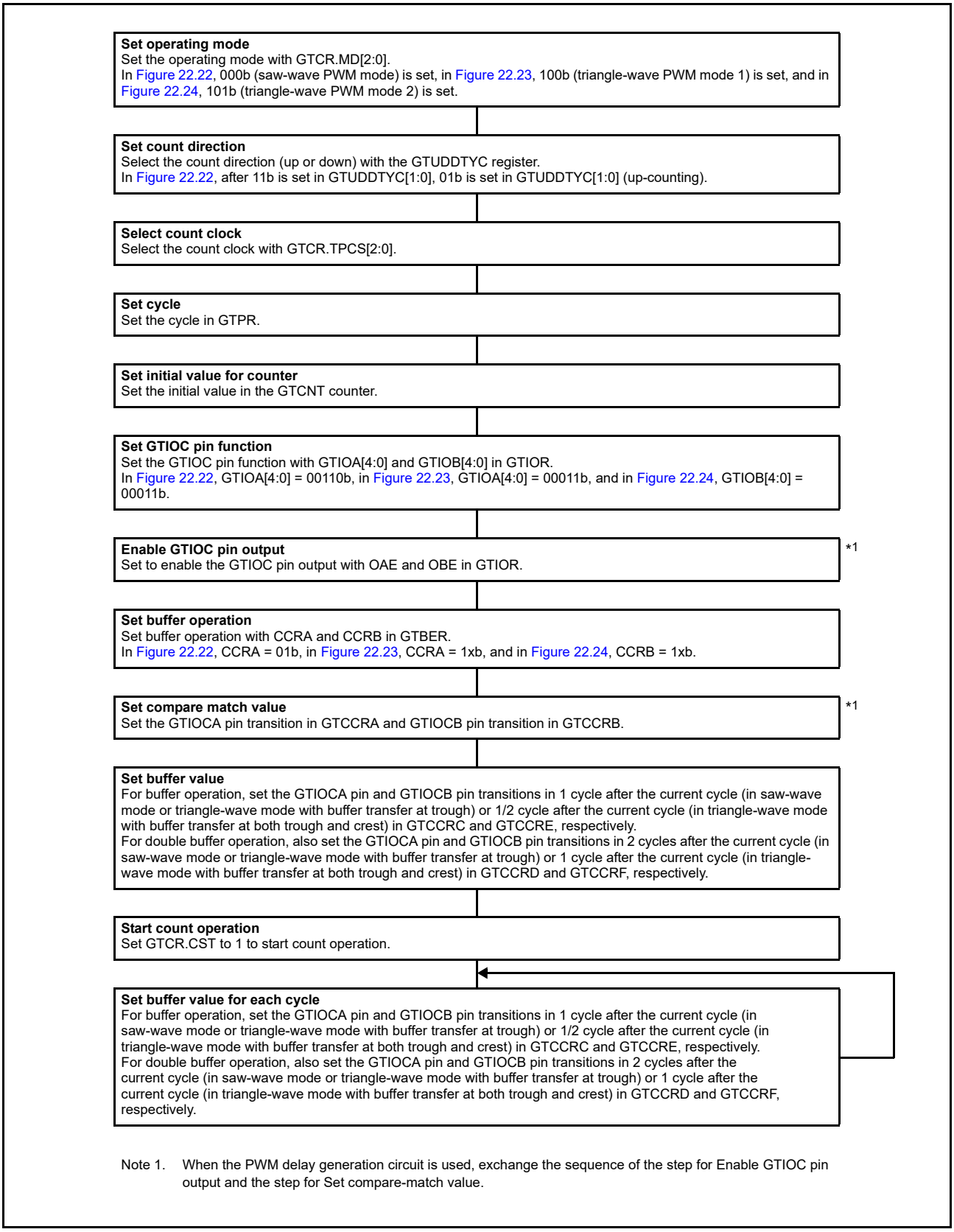


Figure 22.24 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at both troughs and crests, output toggled at GTCCRB compare match, and output retained at cycle end



Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set compare-match value.

Figure 22.25 Example setting for GTCCRA and GTCCRB buffer operation with output compare

(2) When GTCCRA or GTCCRB functions as an Input Capture Register

When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to the buffer registers. In input capture operation, the buffer transfer is not performed by the counter clear.

Figure 22.26 and Figure 22.27 show examples of GTCCRA and GTCCRB buffer operation, and Figure 22.28 shows an example setting for GTCCRA and GTCCRB buffer operation.

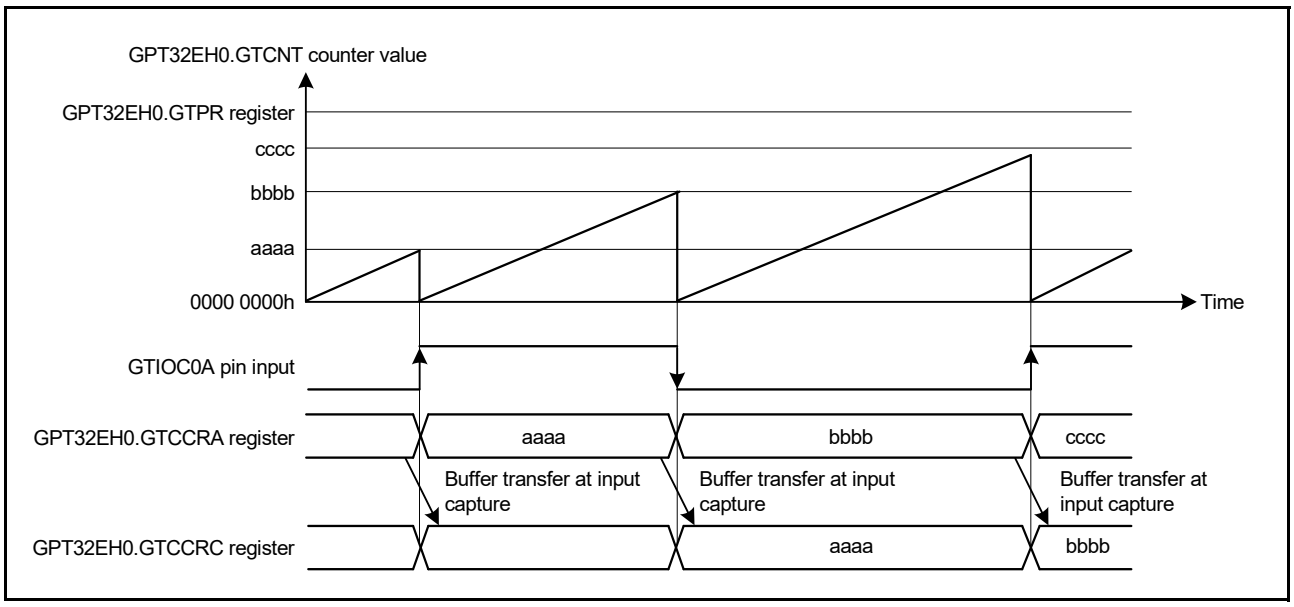


Figure 22.26 Example of GTCCRA and GTCCRB buffer operation with input capture at both edges of GTIOC0A input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOC0A input

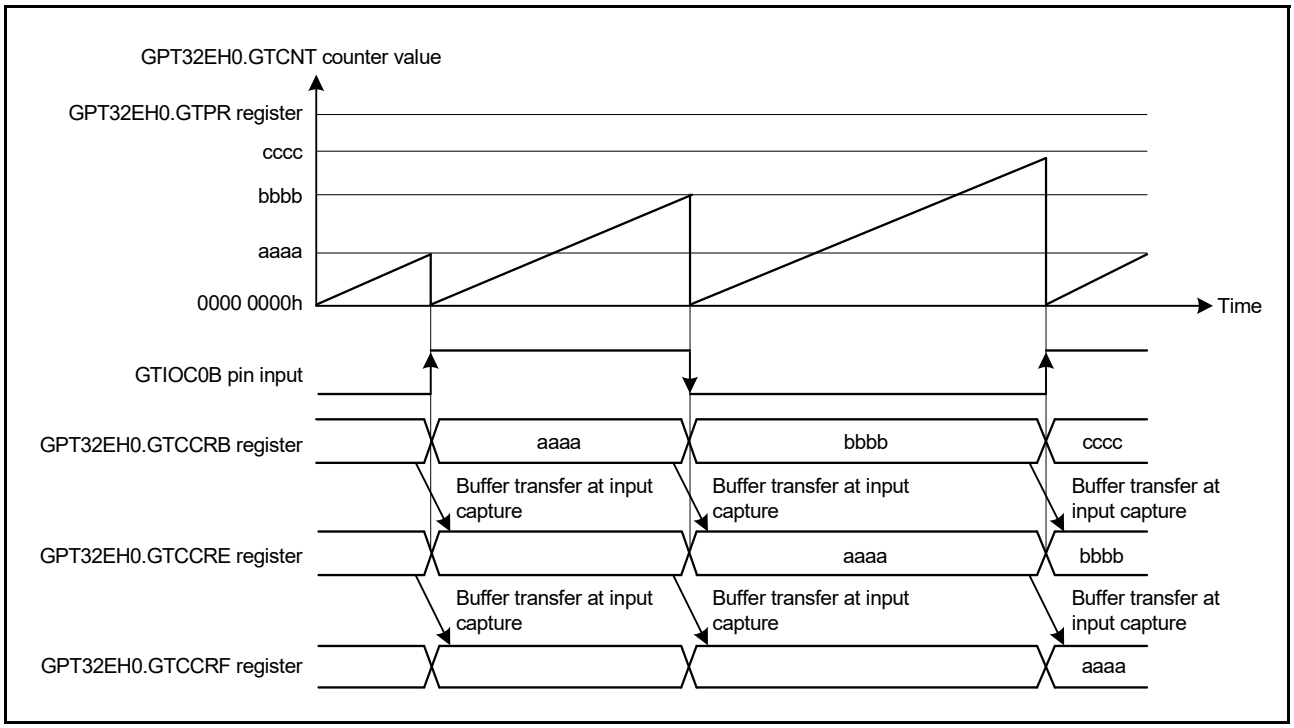


Figure 22.27 Example of GTCCRA and GTCCRB double buffer operation with input capture at both edges of GTIOC0B input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOC0B input

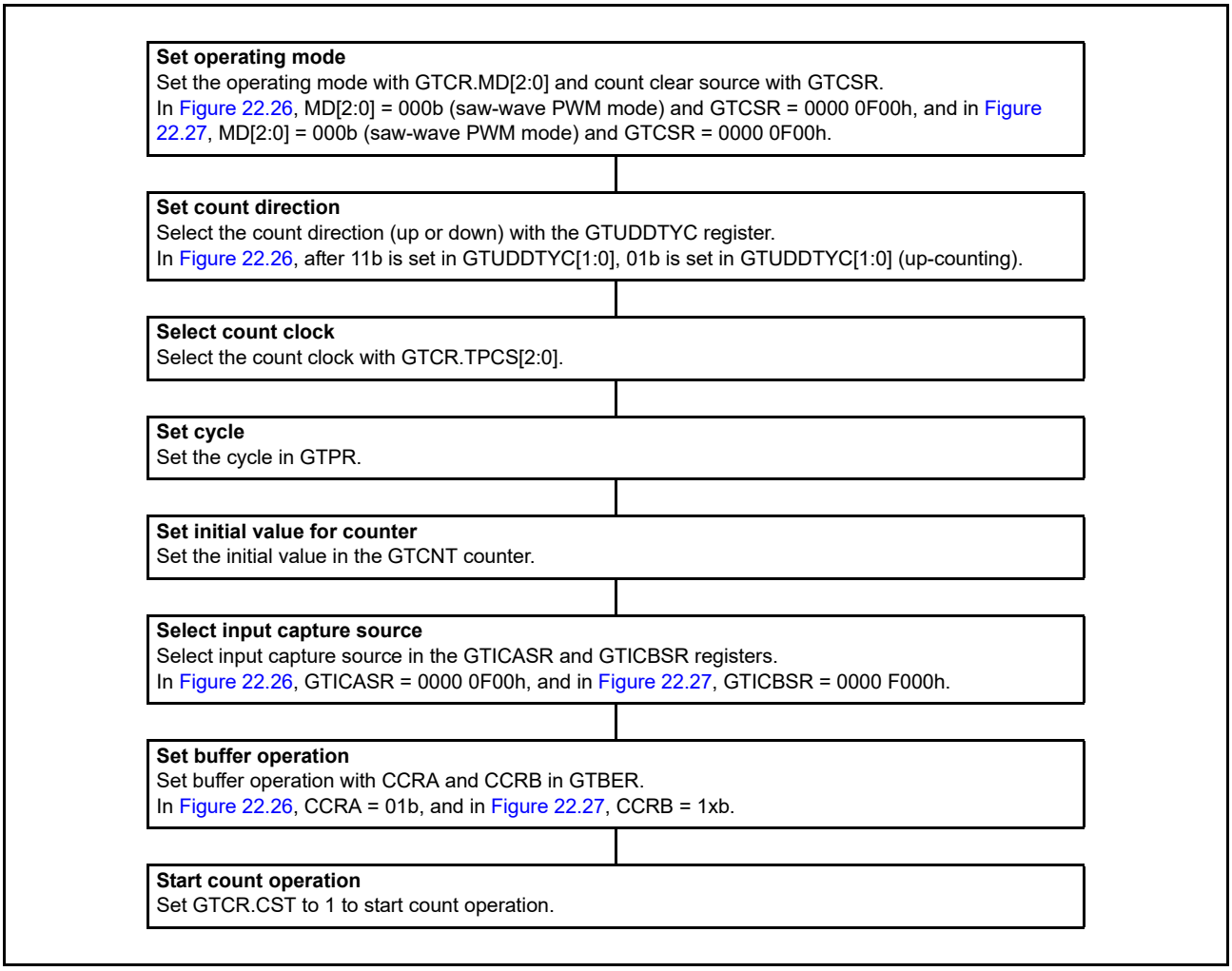


Figure 22.28 Example setting for GTCCRA and GTCCRB buffer operation with input capture

22.3.2.3 Buffer operation for GTADTRA and GTADTRB

GTADTBRA can function as the GTADTRA buffer register and GTADTDBRA can function as the GTADTBRA buffer register (double-buffer register for GTADTRA). Similarly, GTADTBRB can function as the GTADTRB buffer register and GTADTDBRB can function as the GTADTBRB buffer register (double-buffer register for GTADTRB).

To set GTADTRA or GTADTRB to function as a double buffer, set GTBER.ADTDA or GTBER.ADTDB to 1. For single-buffer operation, set GTBER.ADTDA or GTBER.ADTDB to 0. To set GTADTRA or GTADTRB to not function as a buffer, set GTBER.ADTTA[1:0] or GTBER.ADTTB[1:0] to 00b.

The buffer transfer timing can be set with the GTBER.ADTTA[1:0] bits. For saw waves, overflows (during up-counting) or underflows (during down-counting) can be selected. For triangle waves, crests are selected when GTBER.ADTTA[1:0] = 01b, troughs are selected when GTBER.ADTTA[1:0] = 10b, and both crests and troughs are selected when GTBER.ADTTA[1:0] = 11b.

Figure 22.29 to Figure 22.31 show examples of GTADTRA and GTADTRB buffer operation and Figure 22.32 shows an example setting for GTDTRA and GTADTRB buffer operation.

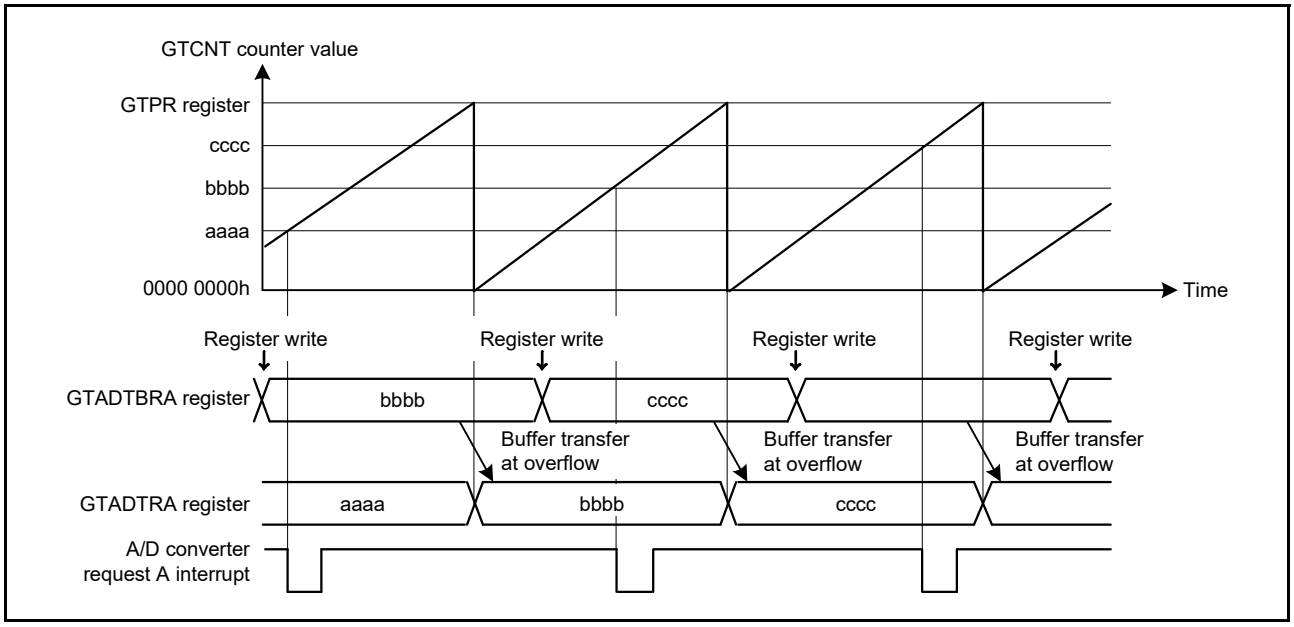


Figure 22.29 Example of GTADTRA and GTADTRB buffer operation with saw waves in up-counting and A/D converter start request interrupt generated by up-counting

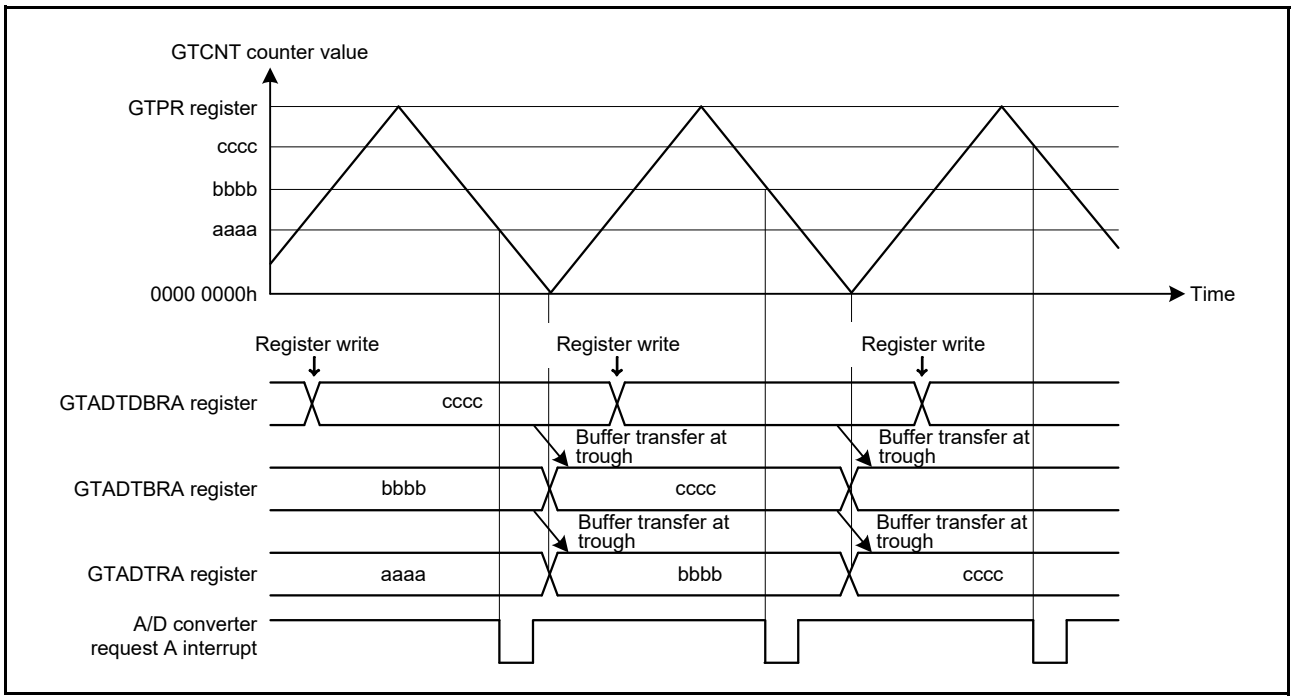


Figure 22.30 Example of GTADTRA and GTADTRB double buffer operation with triangle waves, buffer transfer at troughs, and A/D converter start request interrupt generated by down-counting

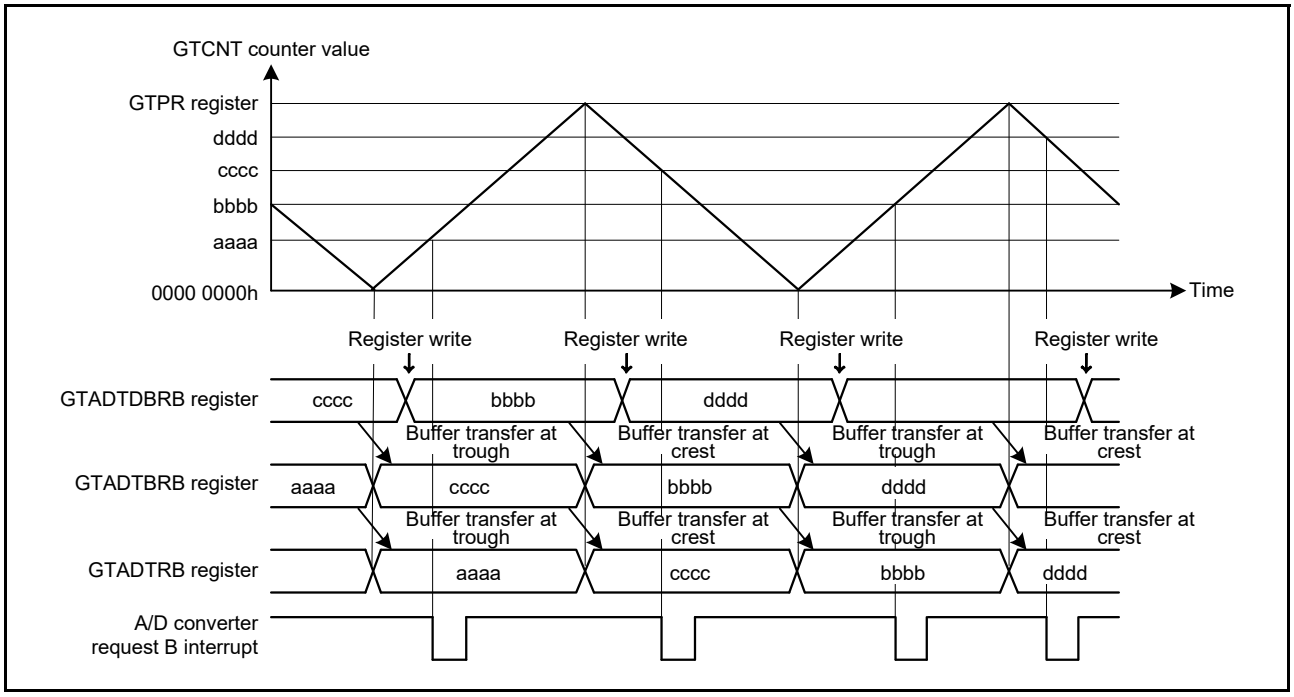


Figure 22.31 Example of GTADTRA and GTADTRB double buffer operation with triangle waves, buffer transfer at both troughs and crests, and A/D converter start request interrupt generated by both up- and down-counting

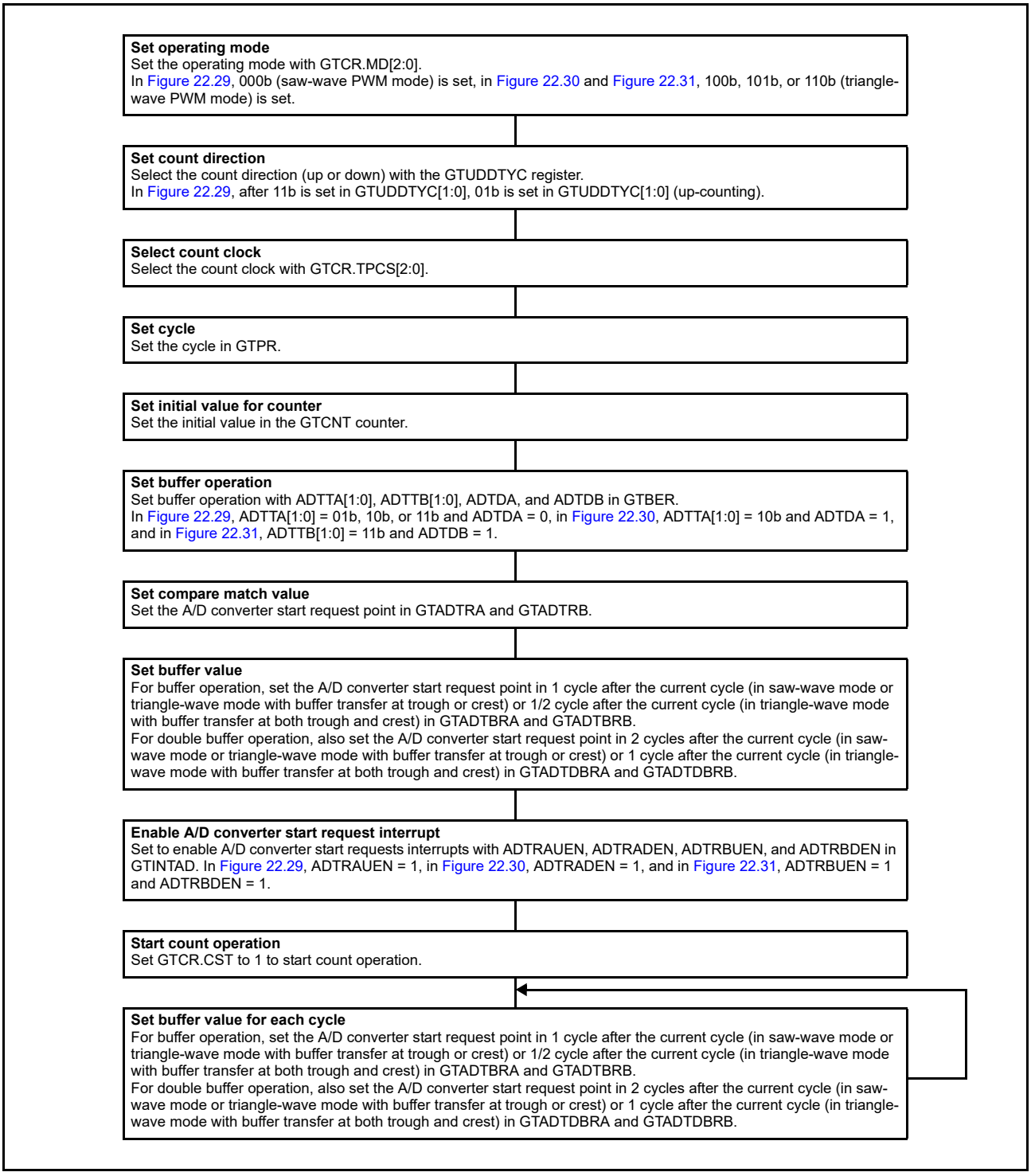


Figure 22.32 Example setting for GTADTRA and GTADTRB buffer operation

22.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCA or GTIOCB pin by a compare match between the GTCNT counter and GTCCRA or GTCCRB. By setting GTDTCR, GTDVU, and GTDVD, the compare match value for a negative-phase waveform with dead time can be automatically set to GTCCRB.

22.3.3.1 Saw-wave PWM mode

In saw-wave PWM mode, GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR. A PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

Figure 22.33 shows an example of saw-wave PWM mode operation, and Figure 22.34 shows an example setting for saw-wave PWM mode.

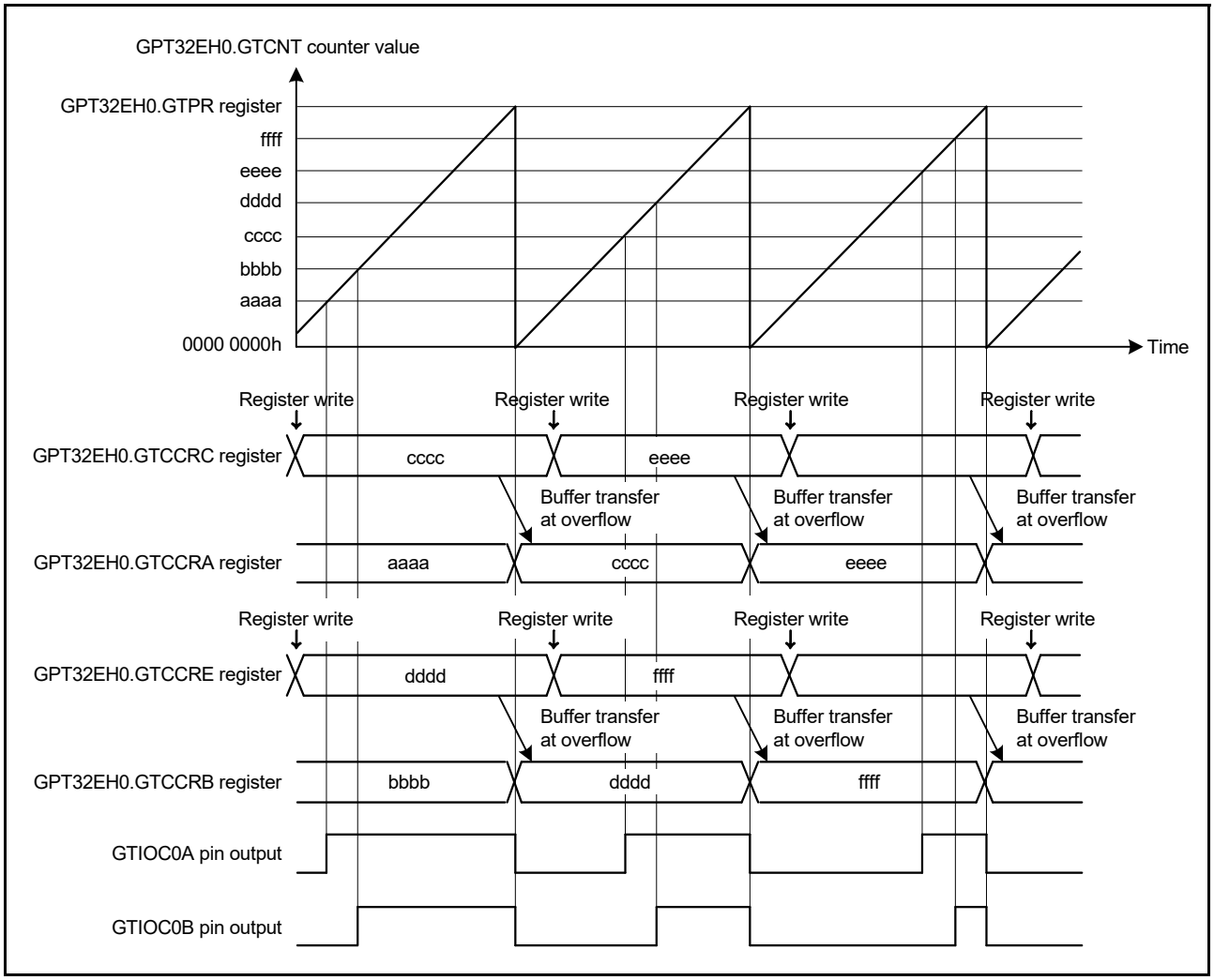
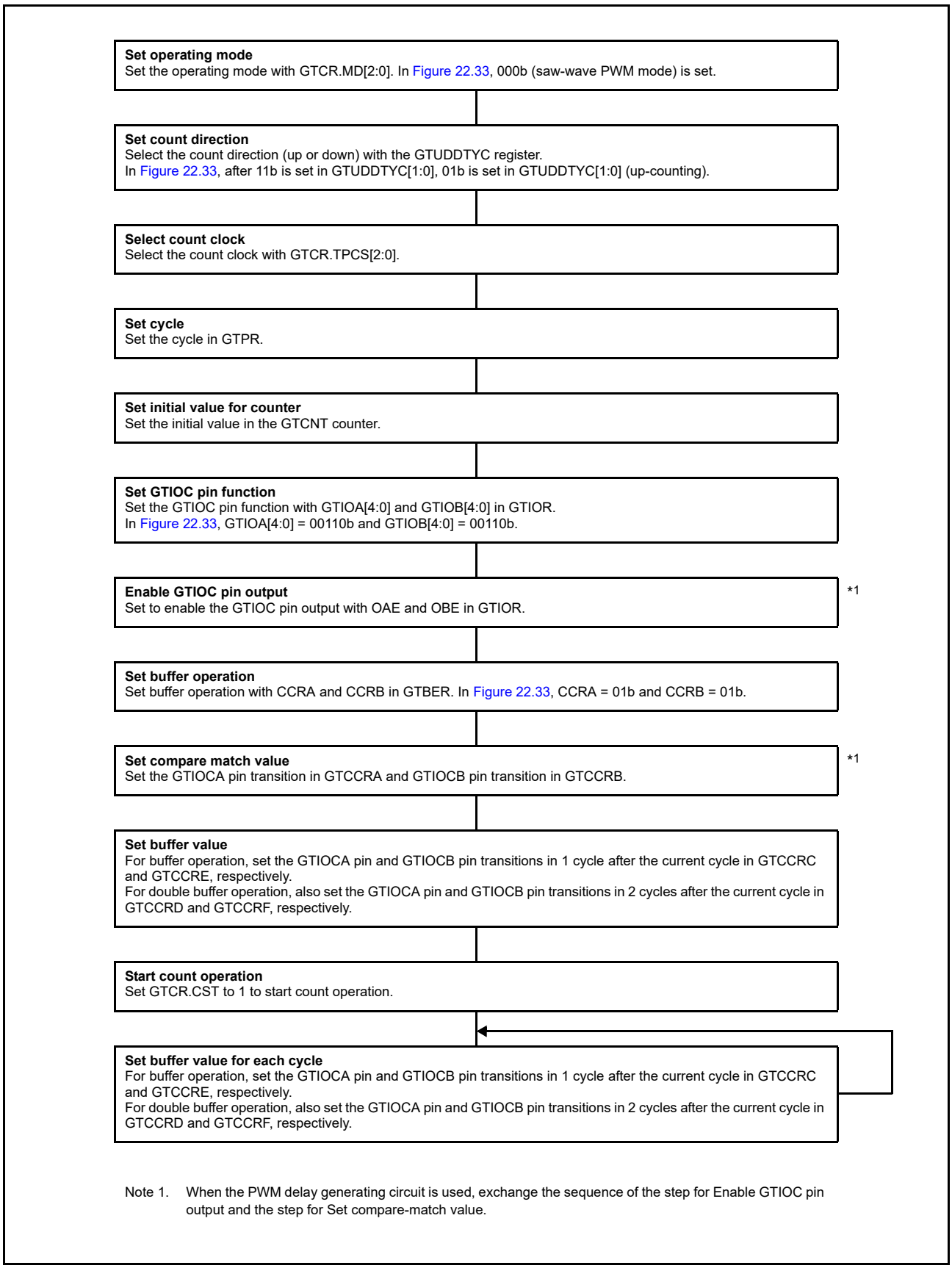


Figure 22.33 Example of saw-wave PWM mode operation with up-counting, buffer operation, high output at GTCCRA/GTCCRB compare match, and low output at cycle end



Note 1. When the PWM delay generating circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set compare-match value.

Figure 22.34 Example setting for saw-wave PWM mode

22.3.3.2 Saw-wave one-shot pulse mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GTPR. The GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCA or GTIOCB pin at a compare match of GTCCRA or GTCCRB with buffer operation fixed.

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the cycle end
- GTCCRE to GTCCRB at the cycle end
- GTCCRD to temporary register A at the cycle end
- GTCCRF to temporary register B at the cycle end
- Temporary register A to GTCCRA at a GTCCRA compare match
- Temporary register B to GTCCRB at a GTCCRB compare match.

The pin output value can be selected from low output, high output, or toggle output separately for a compare match and the cycle end according to the GTIOR setting. When the GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the buffer is transferred forcibly from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B. By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 22.35 shows an example of saw-wave one-shot pulse mode operation, and Figure 22.36 shows an example setting for saw-wave one-shot pulse mode.

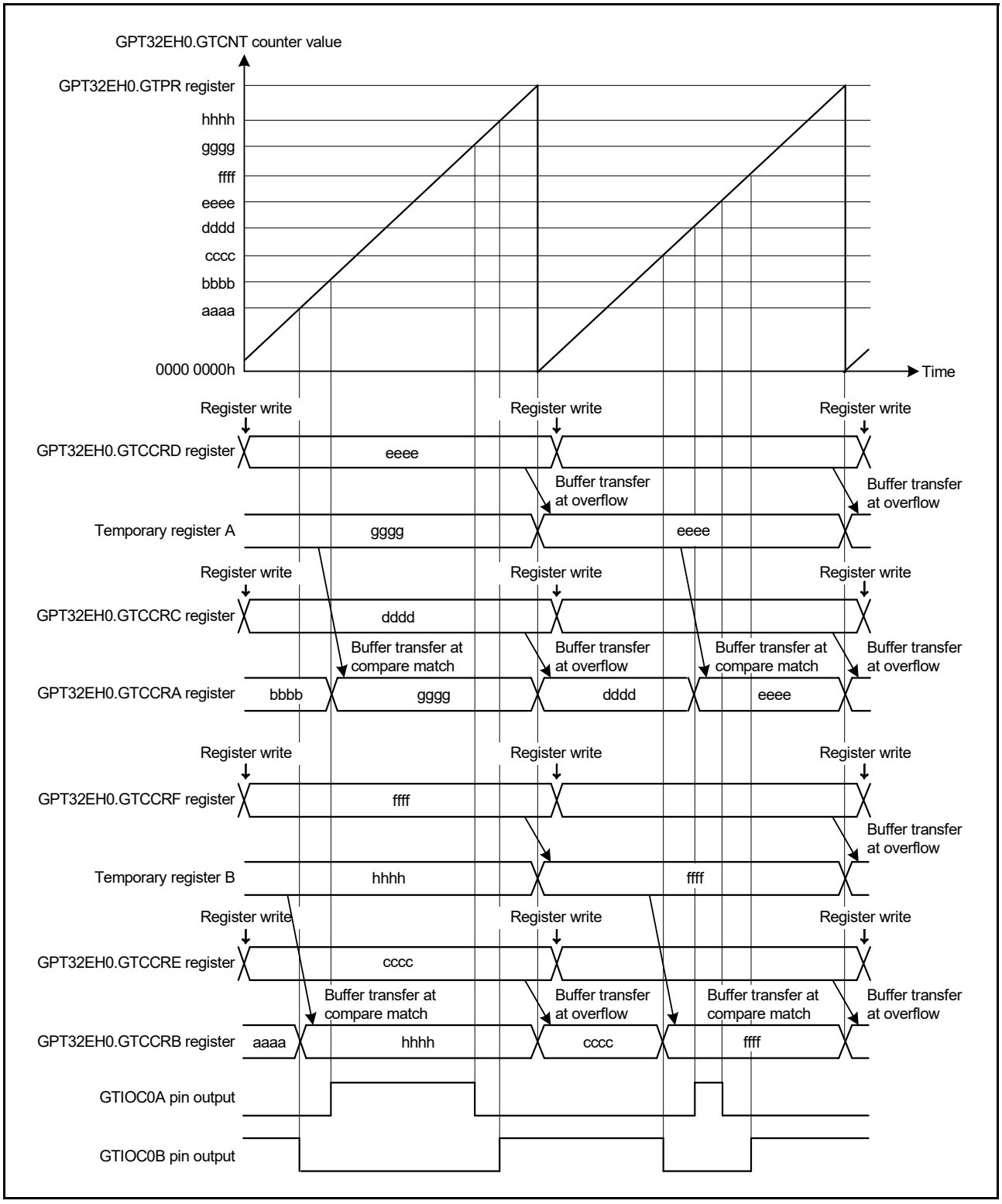
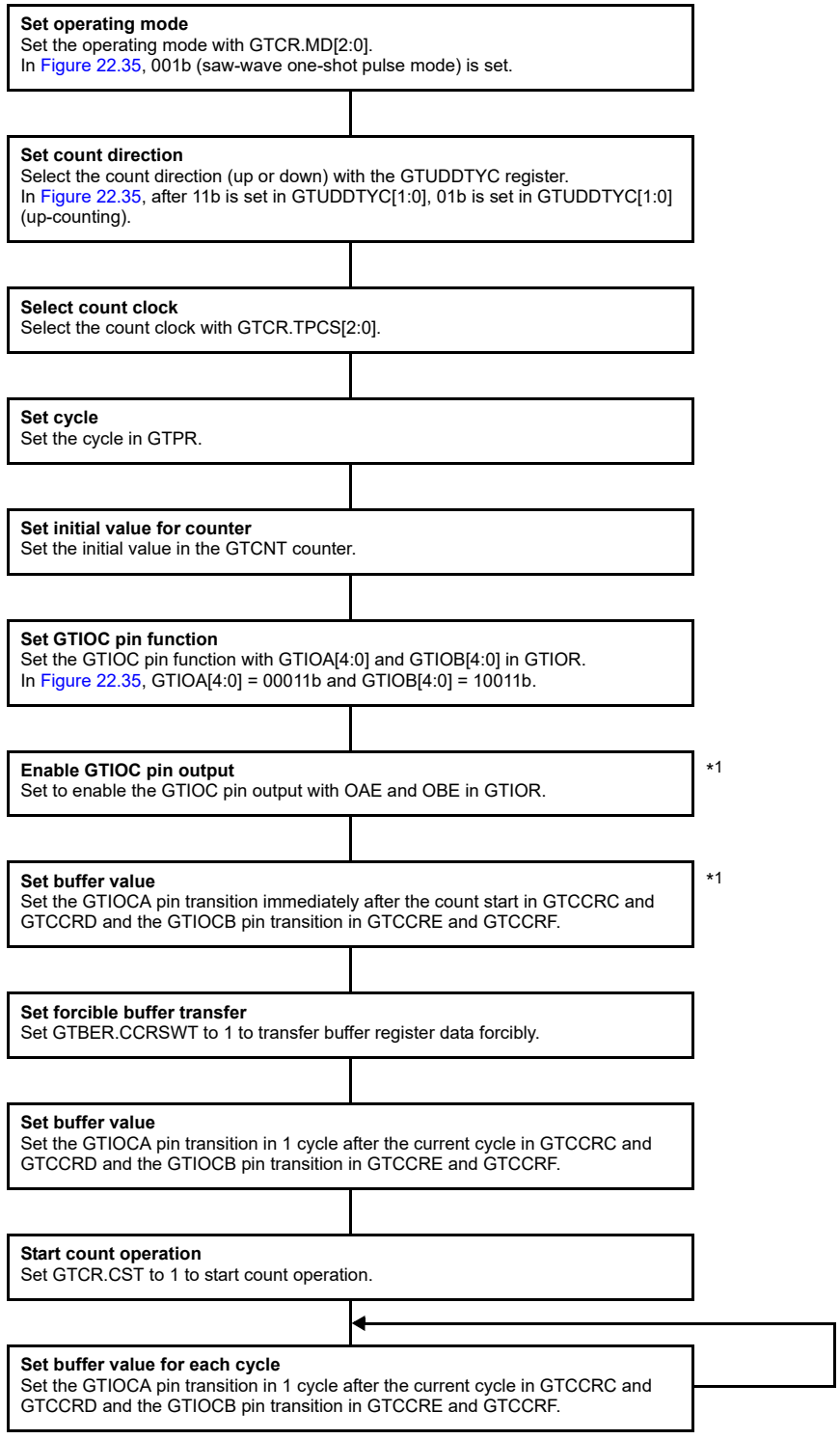


Figure 22.35 Example of saw-wave one-shot pulse mode operation with up-counting, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end



Note 1. When the PWM delay generating circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set buffer value.

Figure 22.36 Example setting for saw-wave one-shot pulse mode

22.3.3.3 Triangle-wave PWM mode 1 (32-bit transfer at trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end based on the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 22.37 shows an example of a triangle-wave PWM mode 1 operation, and Figure 22.38 shows an example setting for a triangle-wave PWM mode 1.

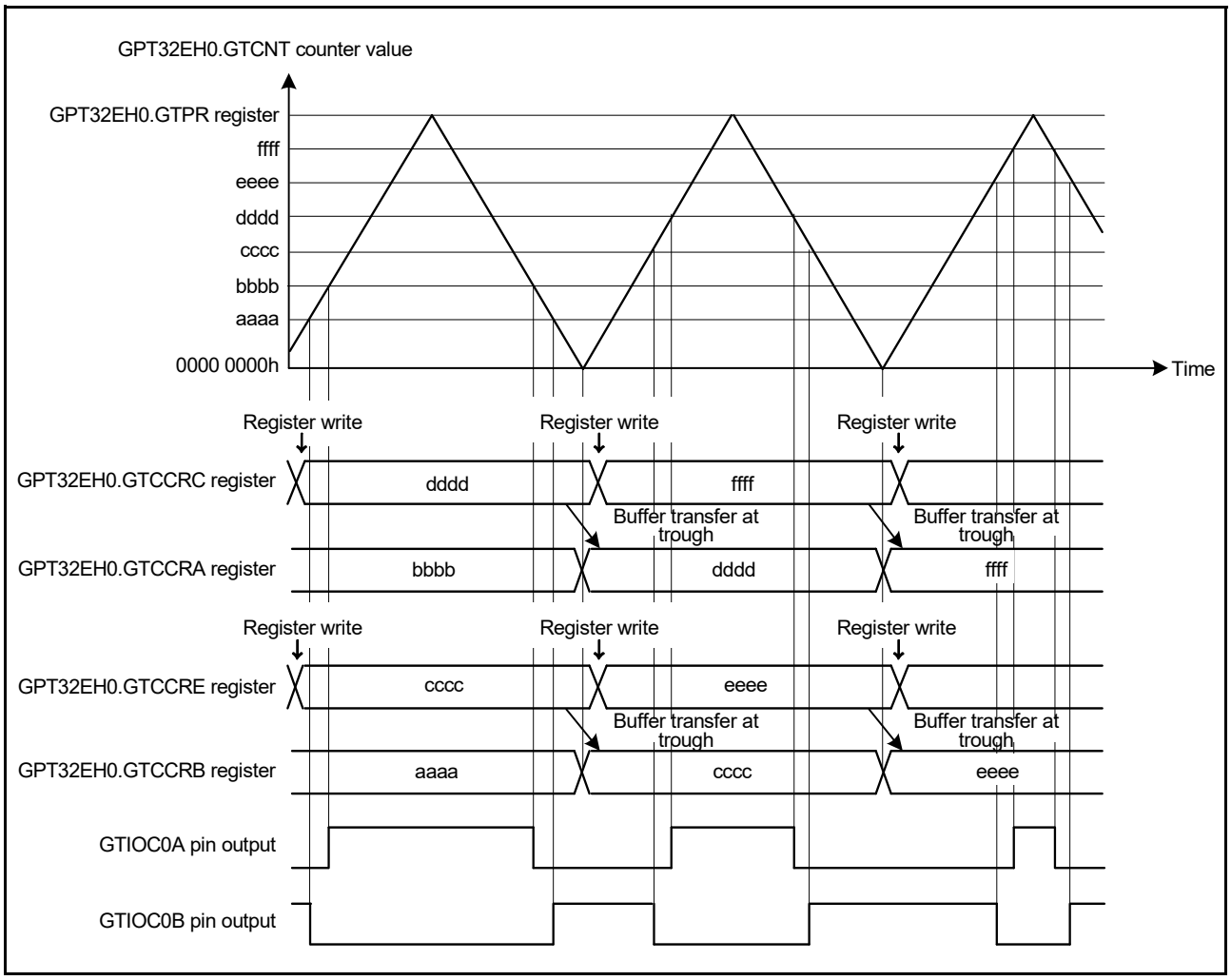
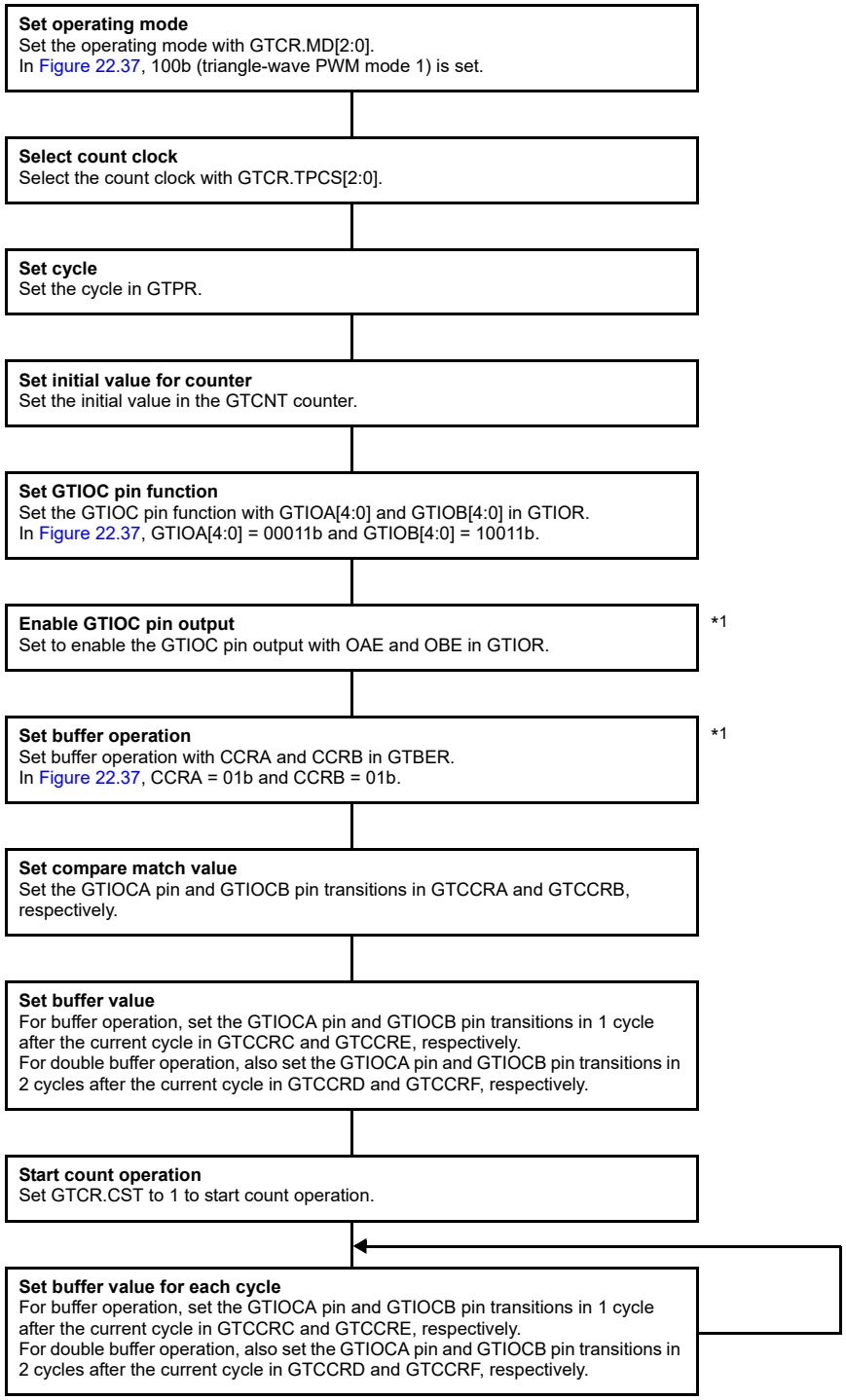


Figure 22.37 Example of triangle-wave PWM mode 1 operation with buffer operation, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/GTCCRB register compare match, and output retained at cycle end



Note 1. When the PWM delay generating circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set buffer value.

Figure 22.38 Example setting for triangle-wave PWM mode 1

22.3.3.4 Triangle-wave PWM mode 2 (32-bit transfer at crest and trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 22.39 shows an example of triangle-wave PWM mode 2 operation, and Figure 22.40 shows an example setting for triangle-wave PWM mode 2.

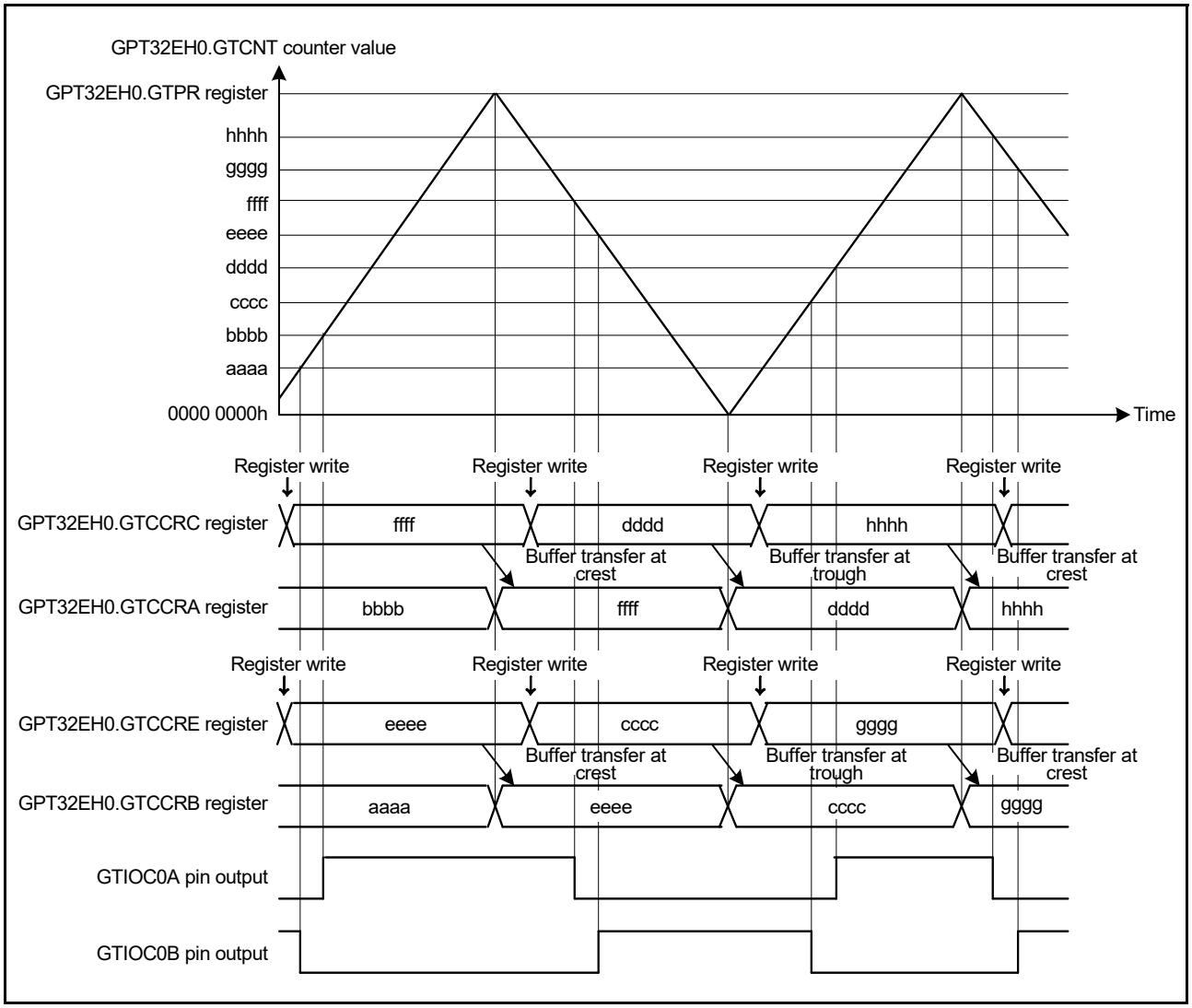
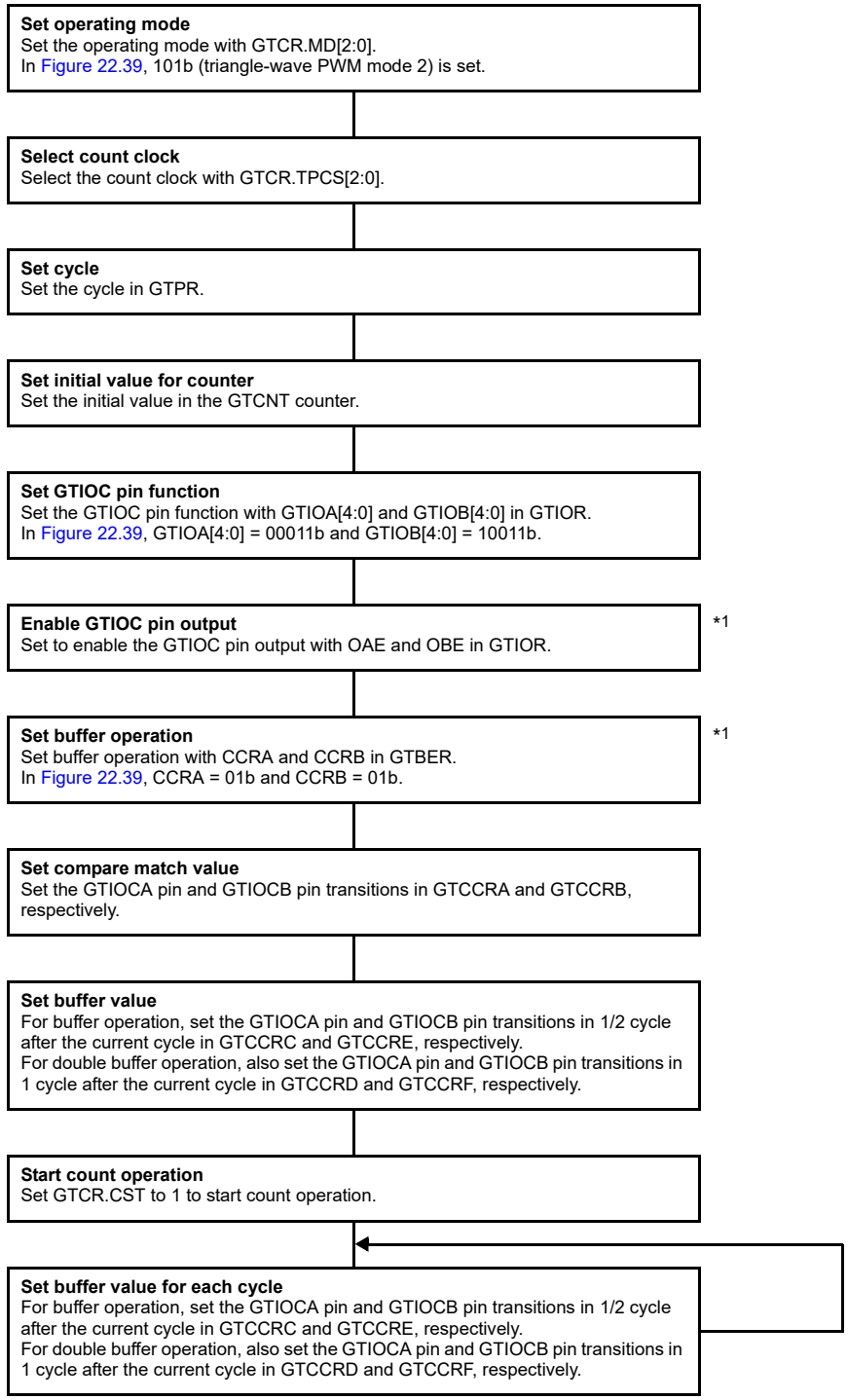


Figure 22.39 Example of triangle-wave PWM mode 2 operation with buffer operation, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end



Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set buffer value.

Figure 22.40 Example setting for triangle-wave PWM mode 2

22.3.3.5 Triangle-wave PWM mode 3 (64-bit transfer at trough)

The triangle-wave PWM mode 3 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCA or GTIOCB pin at a compare match of GTCCRA or GTCCRB with buffer operation fixed. Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the trough
- GTCCRE to GTCCRB at the trough
- GTCCRD to temporary register A at the trough
- GTCCRF to temporary register B at the trough
- Temporary register A to GTCCRA at the crest
- Temporary register B to GTCCRB at the crest.

The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 22.41 shows an example of triangle-wave PWM mode 3 operation, and Figure 22.42 shows an example setting for triangle-wave PWM mode 3.

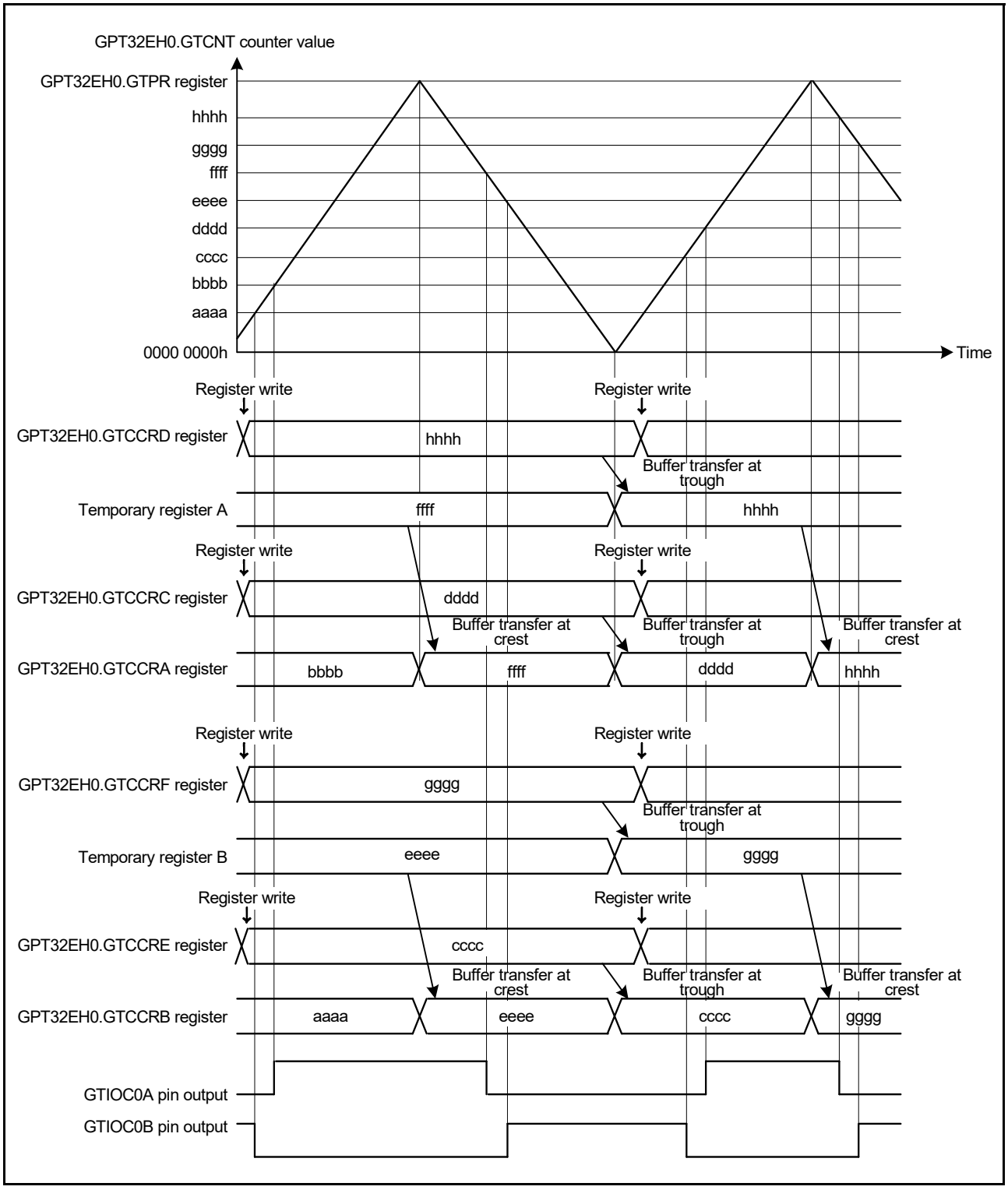
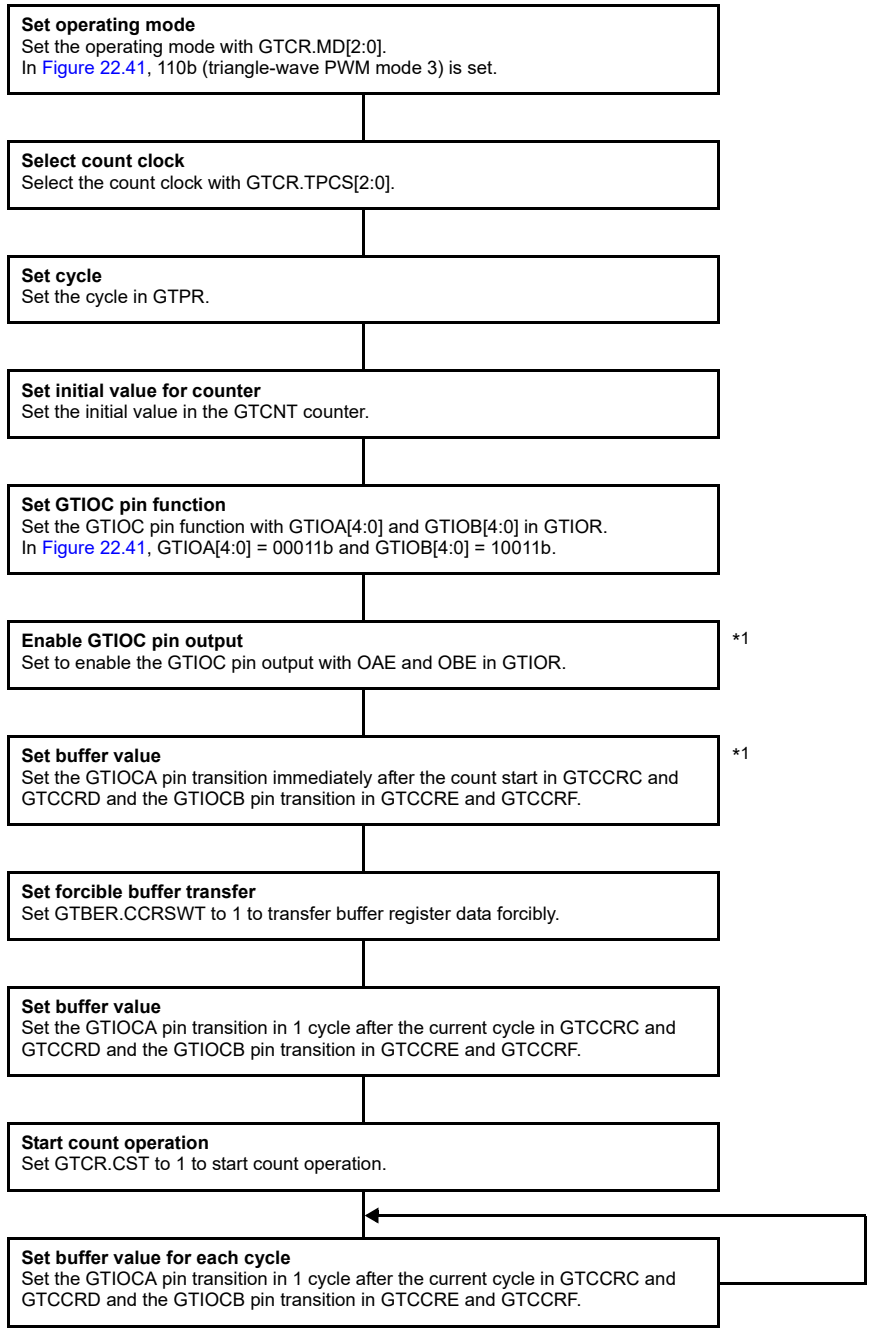


Figure 22.41 Example of triangle-wave PWM mode 3 operation with low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end



Note 1. When the PWM delay generating circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set buffer value.

Figure 22.42 Example setting for triangle-wave PWM mode 3

22.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time values (GTDVU and GTDVD values) can automatically be set to GTCCRB. The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.

Dead time can be separately set for the first half and second half of a waveform. Dead time for the transition in the first half of a negative waveform is set in GTDVU and that in the second half is set in GTDVD. The same dead time can also be set for the first and second halves by setting the GTDTCR.TDFER bit to 1.

GTDBU can be used as a buffer register of GTDVU, and GTDBD can be used as a buffer register of GTDVD. Buffer transfer is performed at a GTCNT overflow (during up-counting), an underflow (during down-counting), or at a GTCNT counter clear for saw waves and at the trough for triangle waves.

The compare match value set by automatic dead time setting function can be confirmed by reading from GTCCRB. Writing to GTCCRB is prohibited when the automatic dead time setting function is used.

Dead time setting beyond the cycle is prohibited. When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 22.6. The adjusted value for the negative waveform is set for GTCCRB automatically. The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

In saw-wave one-shot pulse mode, when the adjusted value is beyond the cycle or the adjusted waveform toggle points are in disorder, the complementarity of the waveforms is not guaranteed.

In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCR = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 22.8.4, Output Protection Function for GTIOC Pin Output. When the GTCCRA is GTCCRA ≥ GTPR + GTDVm, GTPR-1 is set for GTCCRB as the upper limit value. The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers used for calculating the automatic dead time value are updated.

The way to rewrite GTDVm differs by GPT channel number.

Table 22.6 Compare match value after adjusting for dead time error

PWM output operating mode	Count direction	First half/ Second half	Condition of dead time error	Compare match value after adjusting	
				Positive waveform	Negative waveform
Saw-wave one-shot pulse mode	Up	First half	GTCCRA - GTDVU < 0	GTDVU	0
		Second half	GTCCRA + GTDVD > GTPR	GTPR - GTDVD	GTPR
	Down	First half	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		Second half	GTCCRA - GTDVD < 0	GTDVD	0
Triangle-wave PWM mode 1/2/3	Up	First half	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down	Second half	GTCCRA - GTDVD < 0	GTDVD	0

GPT32EH0 to GPT32EH3 and GPT32E4 to GPT32E7

When GTDVm buffer operation is enabled, GTDBm can be written at anytime. GTDBm is transferred to GTDVm at the cycle end.

When GTDVm buffer operation is disabled, stop the GPT using the CST bit in the GTCR register before changing GTDVm to a new value.

GPT328 to GPT3212

While GPT is running, changing the GTDVU values is prohibited. To change GTDVU to a new value, first stop the GPT using the CST bit in the GTCR register.

Figure 22.43 to Figure 22.46 show examples of automatic dead time setting function operation for GPT32EH and GPT32E. Figure 22.47 and Figure 22.48 show the setting examples.

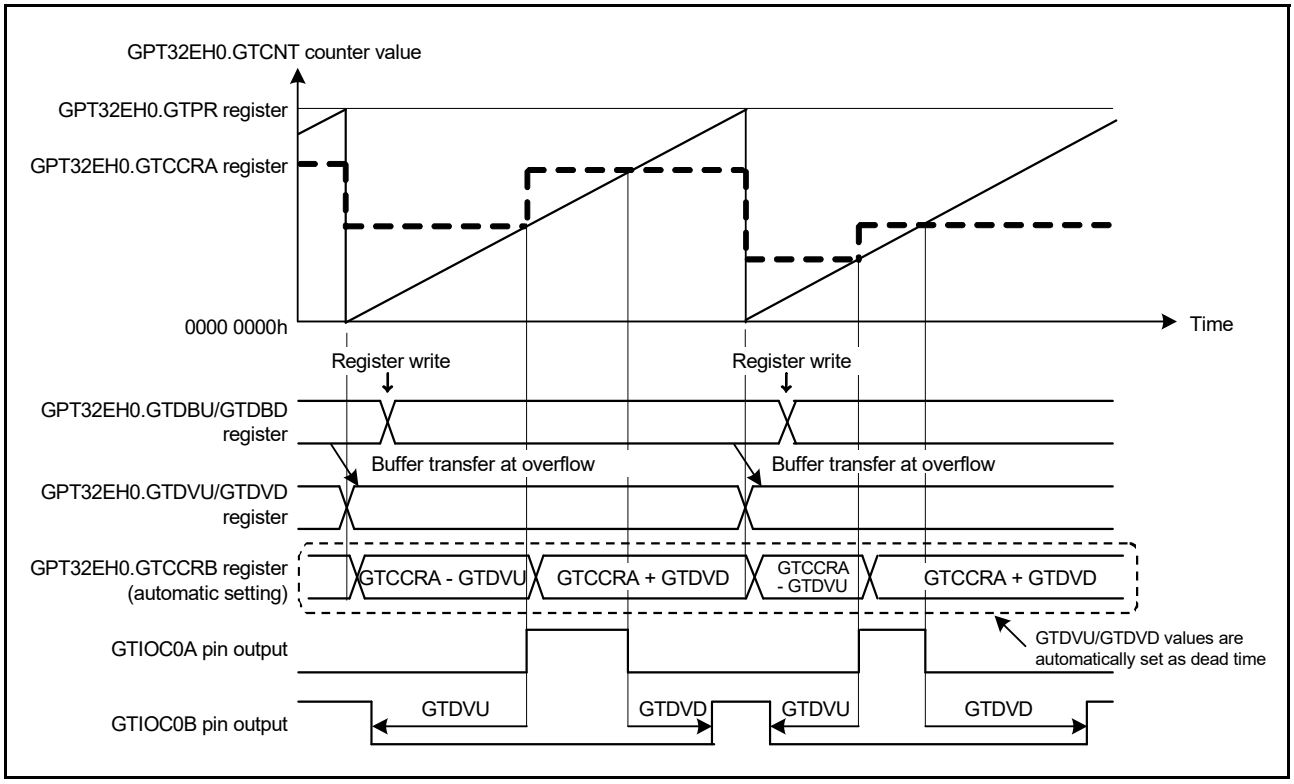


Figure 22.43 Example of automatic dead time setting function operation with saw-wave one-shot pulse mode, up-counting, GTDVU and GTDVD set to buffer operation, and active-high

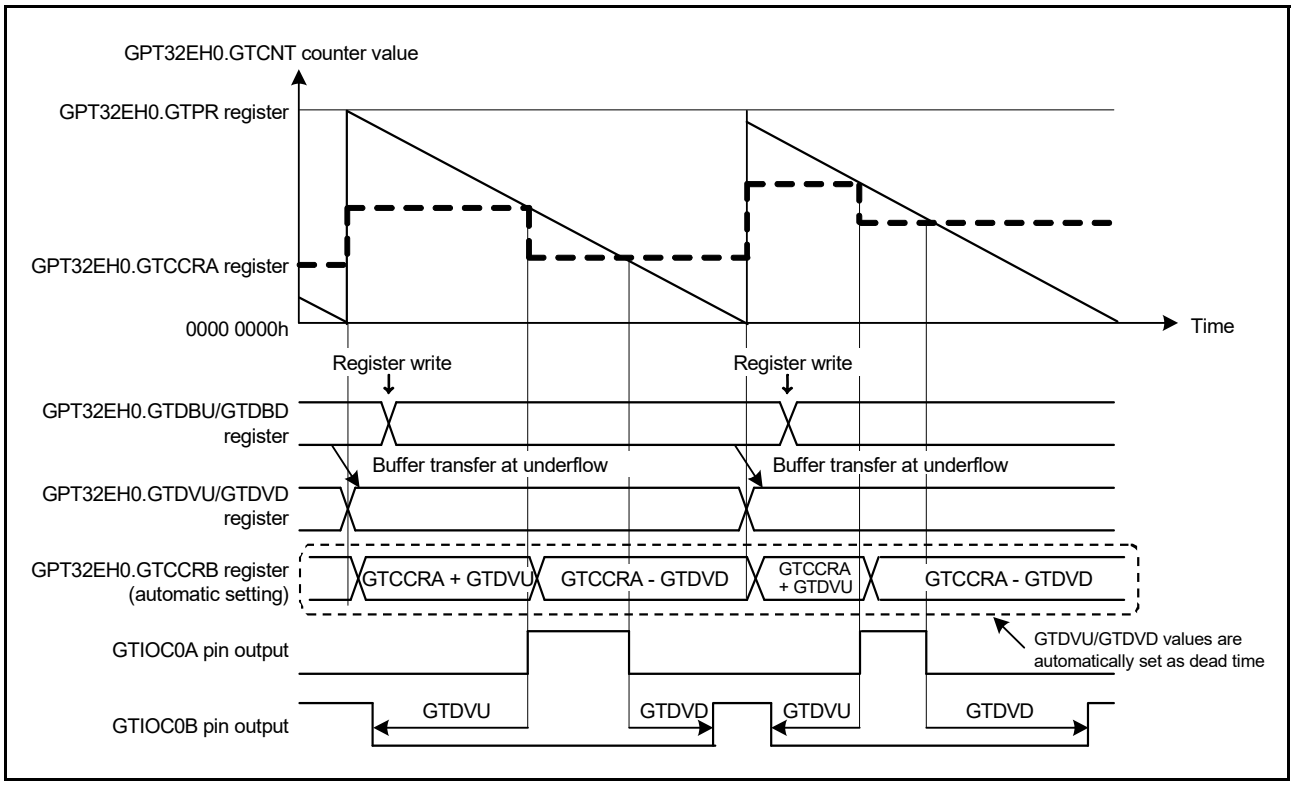


Figure 22.44 Example of automatic dead time setting function operation with saw-wave one-shot pulse mode, down-counting, GTDVU and GTDVD set to buffer operation, and active-high

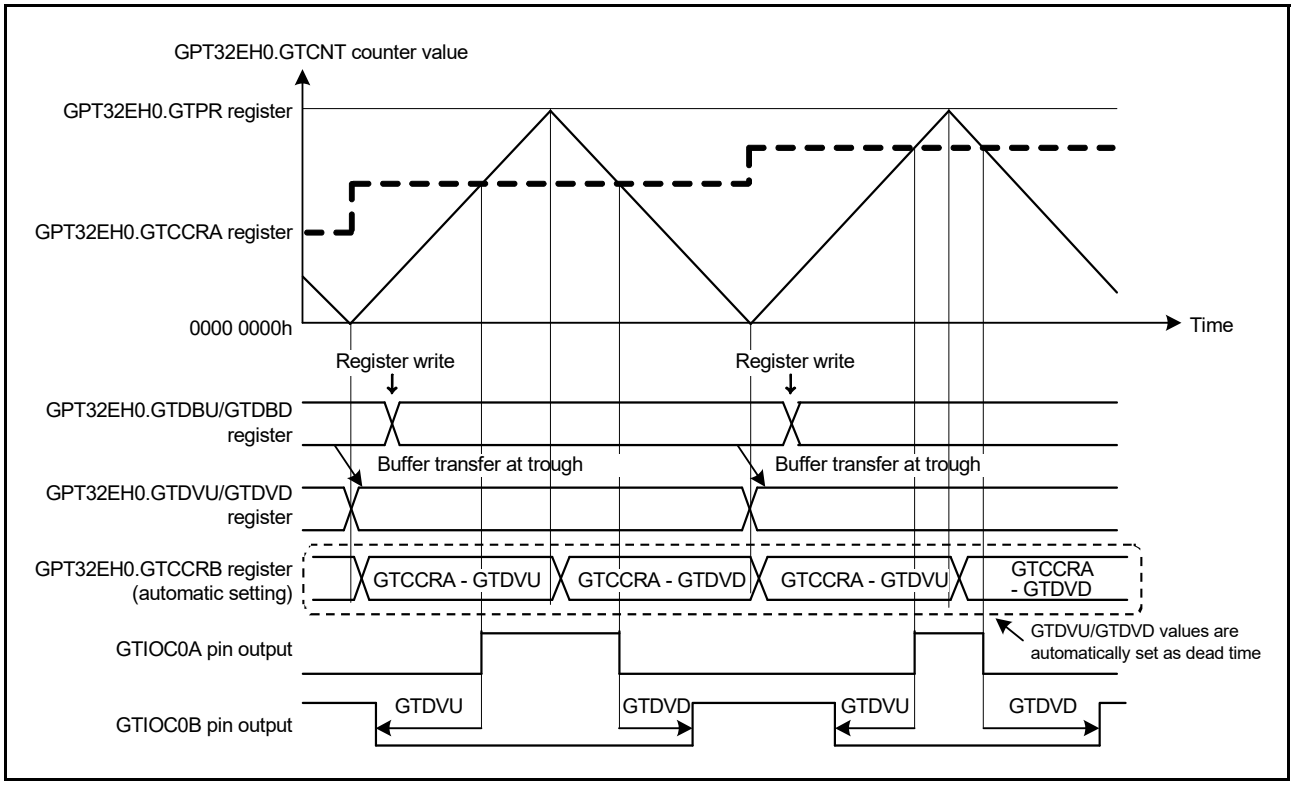


Figure 22.45 Example of automatic compare-match value setting function with dead time, triangle-wave PWM mode 1, GTDVU and GTDVD set to buffer operation, active-high

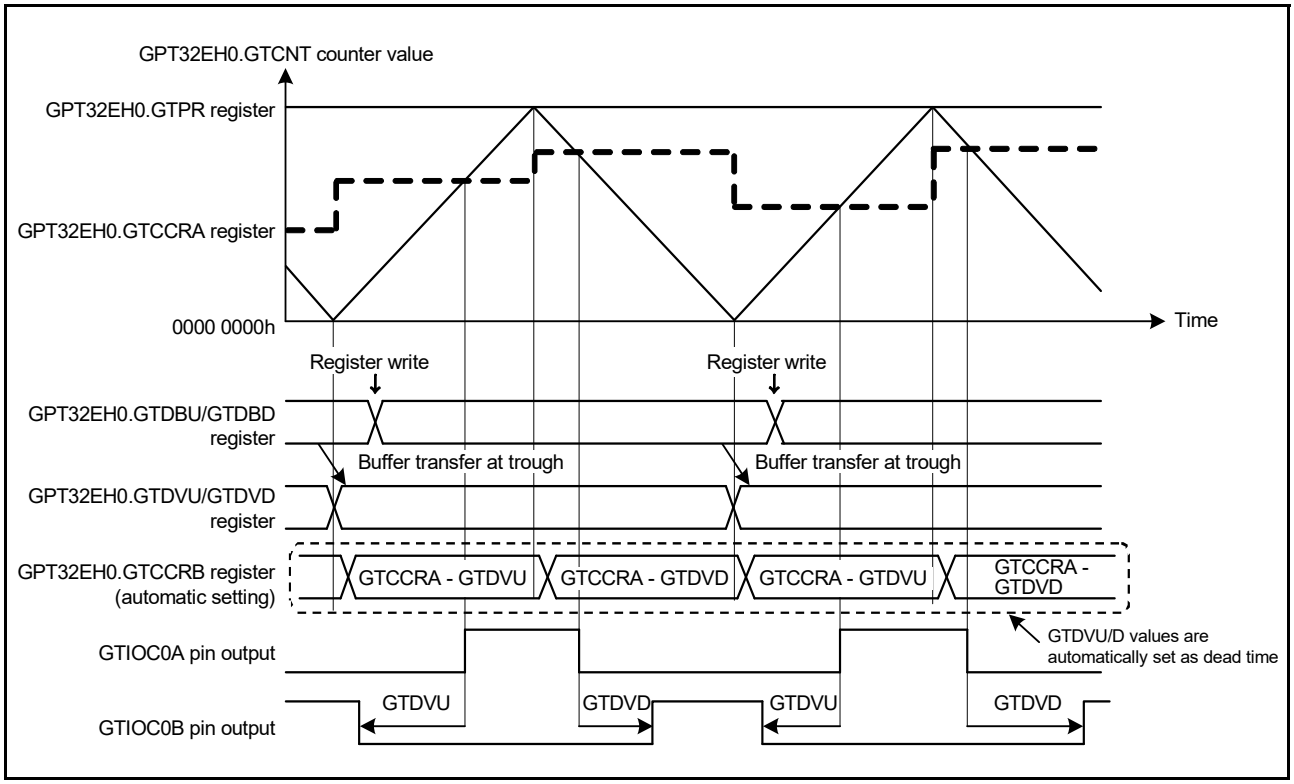


Figure 22.46 Example of automatic compare-match value setting function with dead time, triangle-wave PWM mode 2 or 3, GTDVU and GTDVD set to buffer operation, and active-high

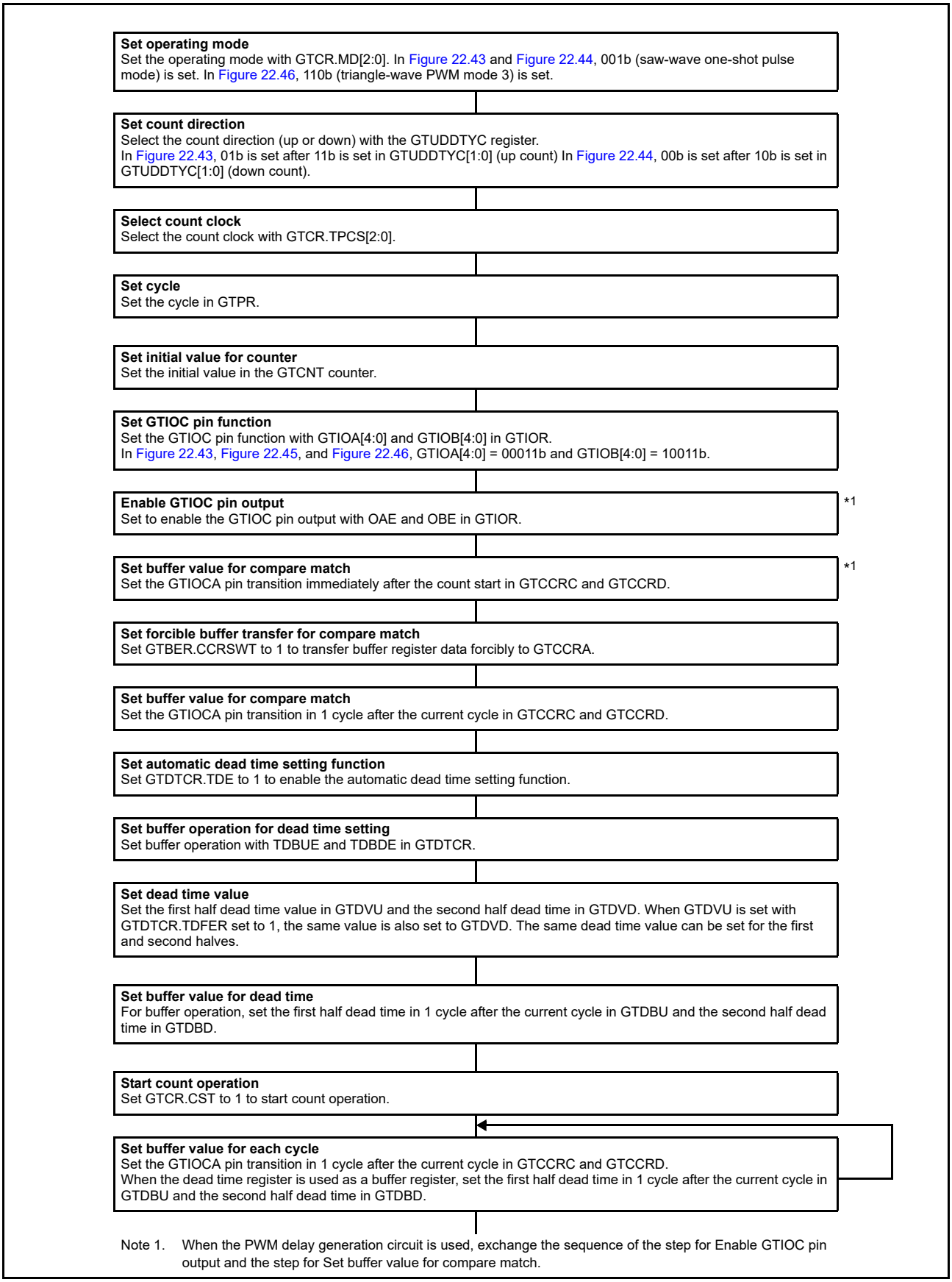
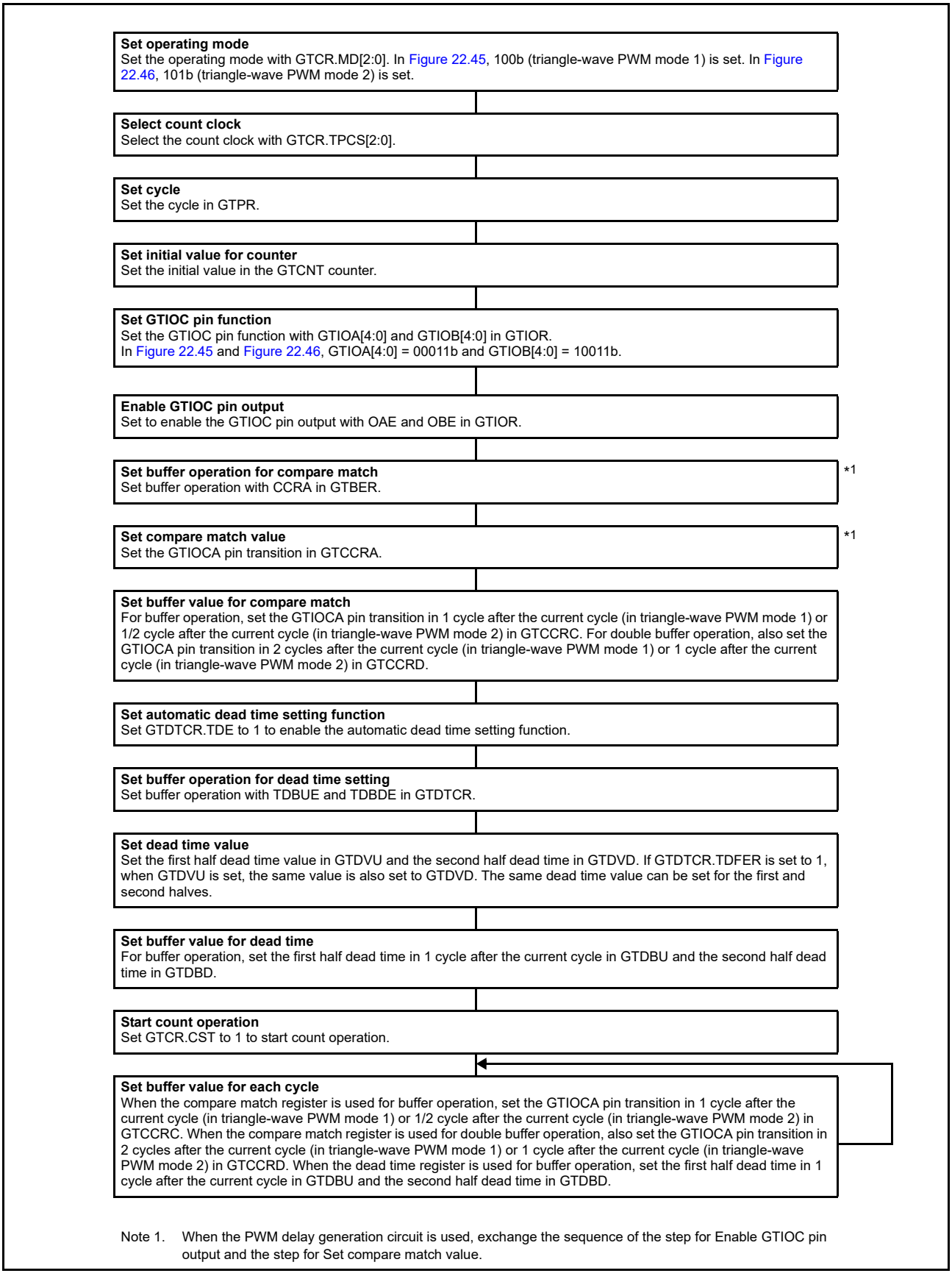


Figure 22.47 Example setting for automatic dead time setting function with saw-wave one-shot pulse mode, and triangle-wave PWM mode 3



Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set compare match value.

Figure 22.48 Example setting for automatic dead time setting function with triangle-wave PWM mode 1 or 2

22.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDDTYC.

In saw-wave mode, if the UD bit in GTUDDTYC is modified during count operation, the count direction is changed at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.UD bit is modified while the count operation is stopped and the GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while the count operation is stopped, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

In triangle-wave mode, the count direction does not change when the UD bit in GTUDDTYC is modified during the count operation. Similarly, when the GTUDDTYC.UD bit is modified while the count operation is stopped and GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit value is not reflected in the count operation. If the GTUDDTYC.UDF bit is set to 1 while the count operation is stopped, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

If the count direction changes during a saw-wave count operation, the GTPR value after the start of up-counting is reflected in the count cycle during up-counting, and the GTPR value before the start of down-counting is reflected during down-counting.

Figure 22.49 shows an example operation of count direction changing function.

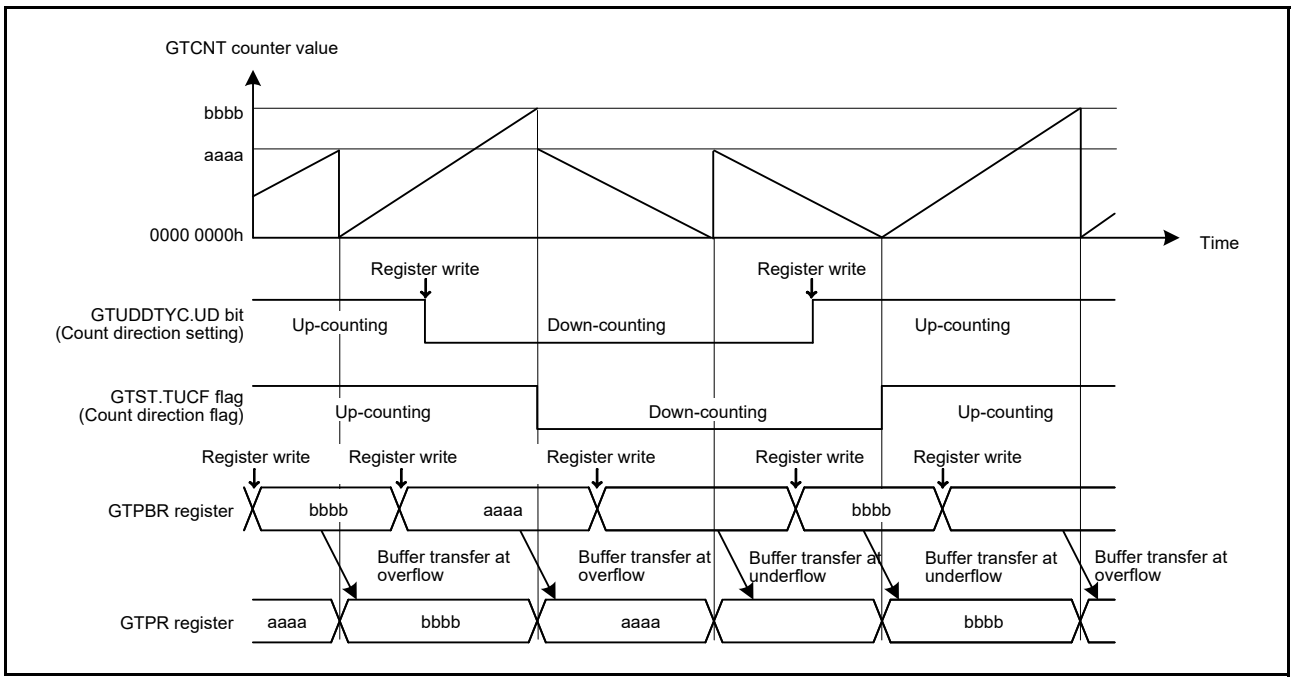


Figure 22.49 Example operation of count direction changing function during buffer operation

22.3.6 Function of Output Duty 0% and 100%

The output duty of the GTIOCA and GTIOCB pins are set to 0% or 100% by changing the GTUDDTYC.OADTY bit or GTUDDTYC.OBDTY bit.

In saw-wave mode, if the GTUDDTYC.OADTY or GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.OADTY or GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an overflow or an underflow. If the GTUDDTYC.OADTYF or GTUDDTYC.OBDTYF bit is set to 1 while the count operation is stopped, the GTUDDTYC.OADTY or GTUDDTYC.OBDTY bit value at that time is reflected at the start of counting.

In triangle-wave mode, if the GTUDDTYC.OADTY or GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an underflow.

If the GTUDDTYC.OADTY or GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an underflow. If the GTUDDTYC.OADTY or GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or GTUDDTYC.OBDTYF bit is 1, the output duty modification is reflected at the start of counting.

In performing 0%/100% duty operation, GPT internally continues to:

- Perform compare match operation
- Set compare match flag
- Output interrupt
- Perform buffer operation.

When the control is changed from 0% or 100% duty setting to compare match, the output value of GTIOCA pin at cycle end is determined by GTIOR.GTIOA[3:2] and GTUDDTYC.OADTYR. The output value of GTIOCB pin at cycle end is determined by GTIOR.GTIOB[3:2] and GTUDDTYC.OBDTYR.

When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 01b, the output pins output low at cycle end. When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 10b, the output pins output high at cycle end.

GTUDDTYC.OADTYR selects the value that is the object of output retained/toggled at cycle end, when GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or when GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end). Table 22.7 shows the values of GTIOCA/GTIOCB pin output at cycle end.

Table 22.7 Output values after releasing 0% or 100% duty setting (m = A, B)

GTIOR.GTIOm[3:2]	Compare match value at cycle end masked by 0% or 100% duty setting	GTUDDTYC.OmDTYR in duty 0% setting		GTUDDTYC.OmDTYR in duty 100% setting	
		0	1	0	1
00 (output retained at cycle end)	0	0	0	1	0
	1	0	1	1	1
01 (low output at cycle end)	-	0	0	0	0
10 (high output at cycle end)	-	1	1	1	1
11 (output toggled at cycle end)	0	1	1	0	1
	1	1	0	0	0

Figure 22.50 shows an example of output duty 0% and 100% function.

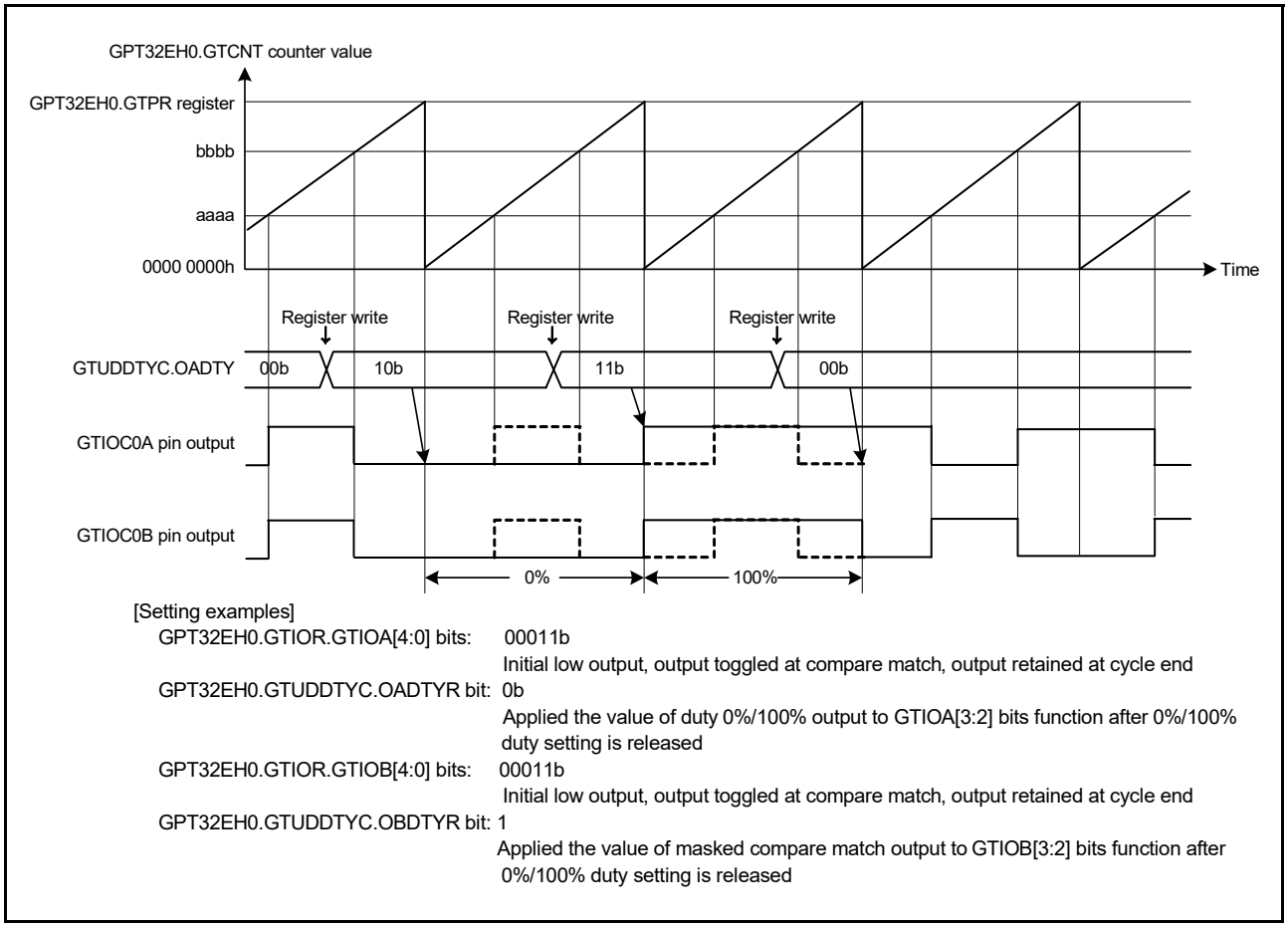


Figure 22.50 Example of output duty 0% and 100% functions

22.3.7 Hardware Count Start/Count Stop and Clear Operation

The GTCNT counter can be started, stopped, or cleared by the following hardware sources:

- External trigger input
- ELC event input
- GTIOCA/GTIOCB pin input.

22.3.7.1 Hardware start operation

The GTCNT counter can be started by selecting a hardware source using GTSSR.

Figure 22.51 shows an example of a count start operation by a hardware source. Figure 22.52 shows the setting example.

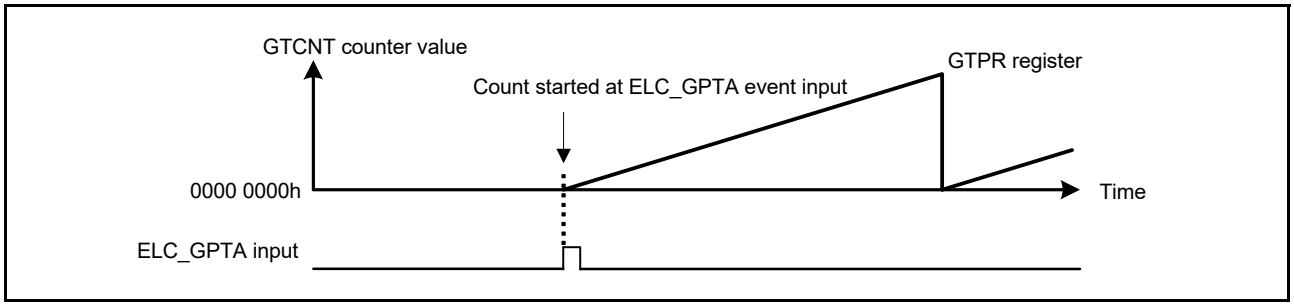


Figure 22.51 Example of count start operation by hardware source, started at the input of the signal from the ELC_GPTA event

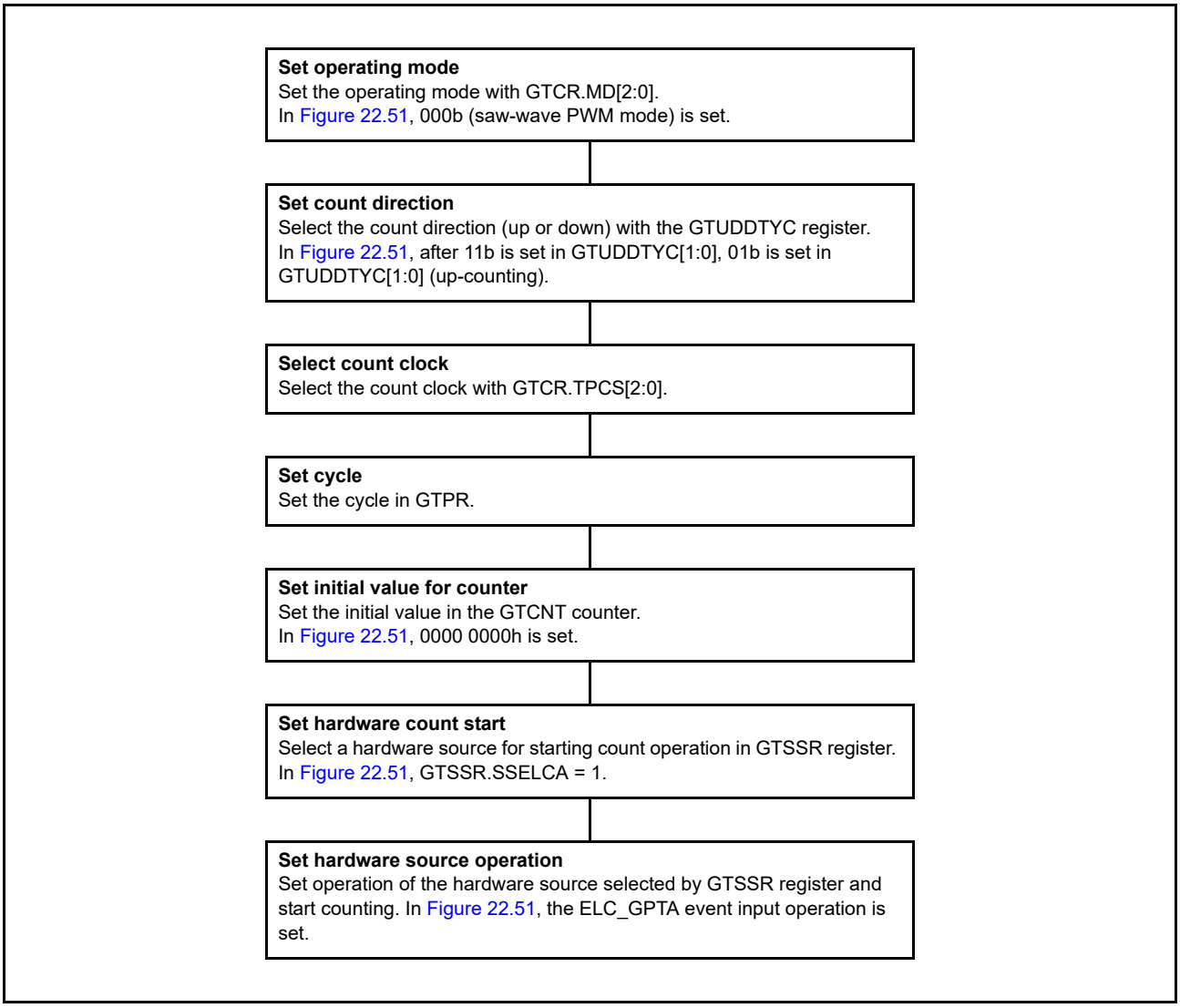


Figure 22.52 Example setting for count start operation by a hardware source

22.3.7.2 Hardware stop operation

The GTCNT counter can be stopped by selecting a hardware source using GTPSR.

Figure 22.53 shows an example of a count stop operation by a hardware source. Figure 22.54 shows the setting example. In this example, the count operation stops at the edge of the ELC_GPTA event input, and restarts at the edge of the ELC_GPTB event input.

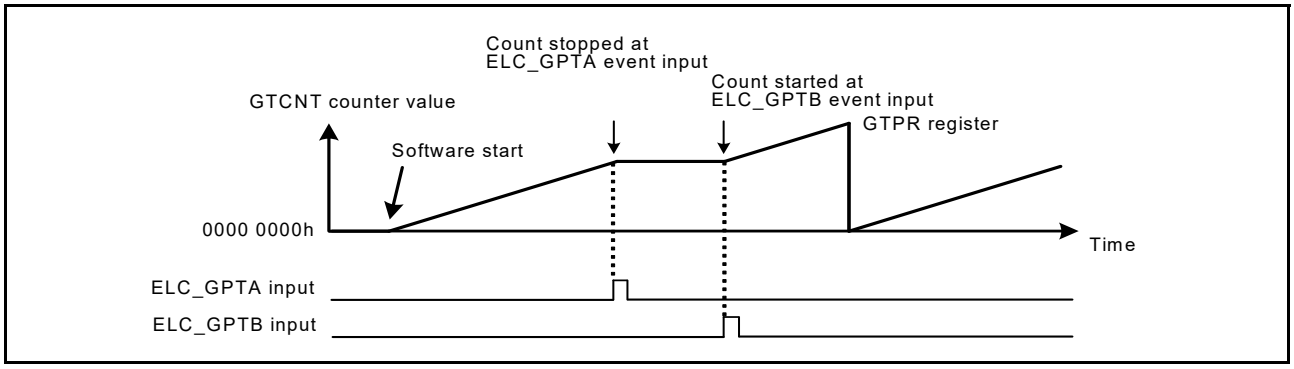


Figure 22.53 Example of count stop operation by a hardware source, started by software, stopped at ELC_GPTA event input, and restarted at ELC_GPTB event input

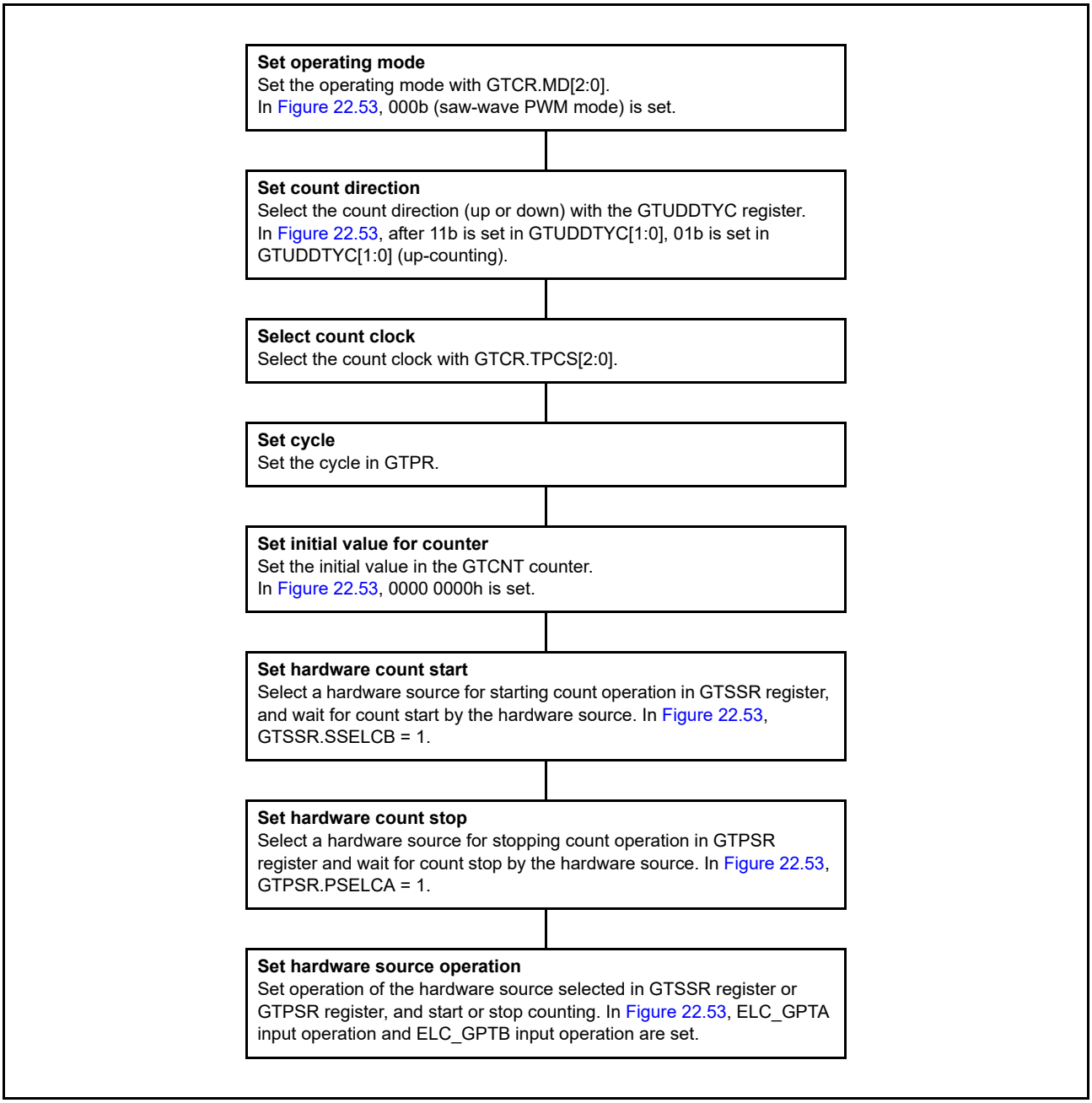


Figure 22.54 Example setting for count stop operation by a hardware source

Figure 22.55 shows an example of a count start/stop operation by a hardware source. Figure 22.56 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRGA.

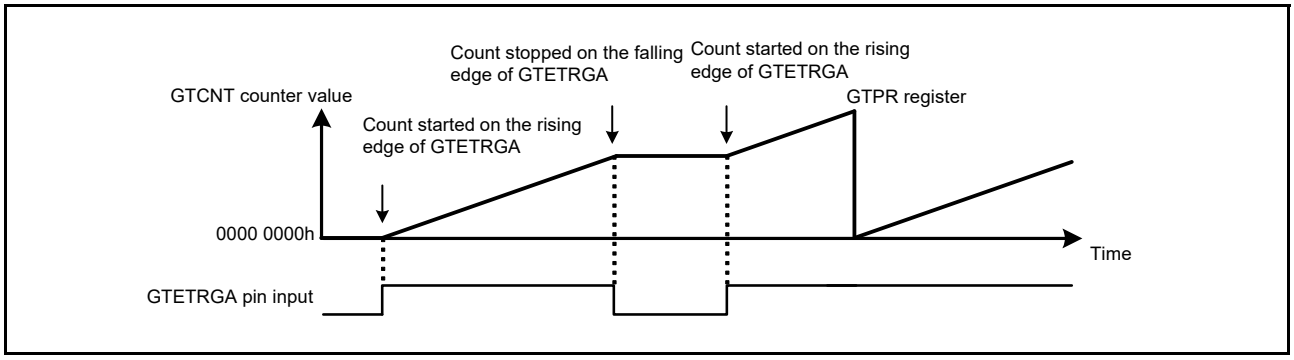


Figure 22.55 Example of count start/stop operation by hardware source, started on the rising edge of GTETRGA pin input, and stopped on the falling edge of GTETRGA pin input

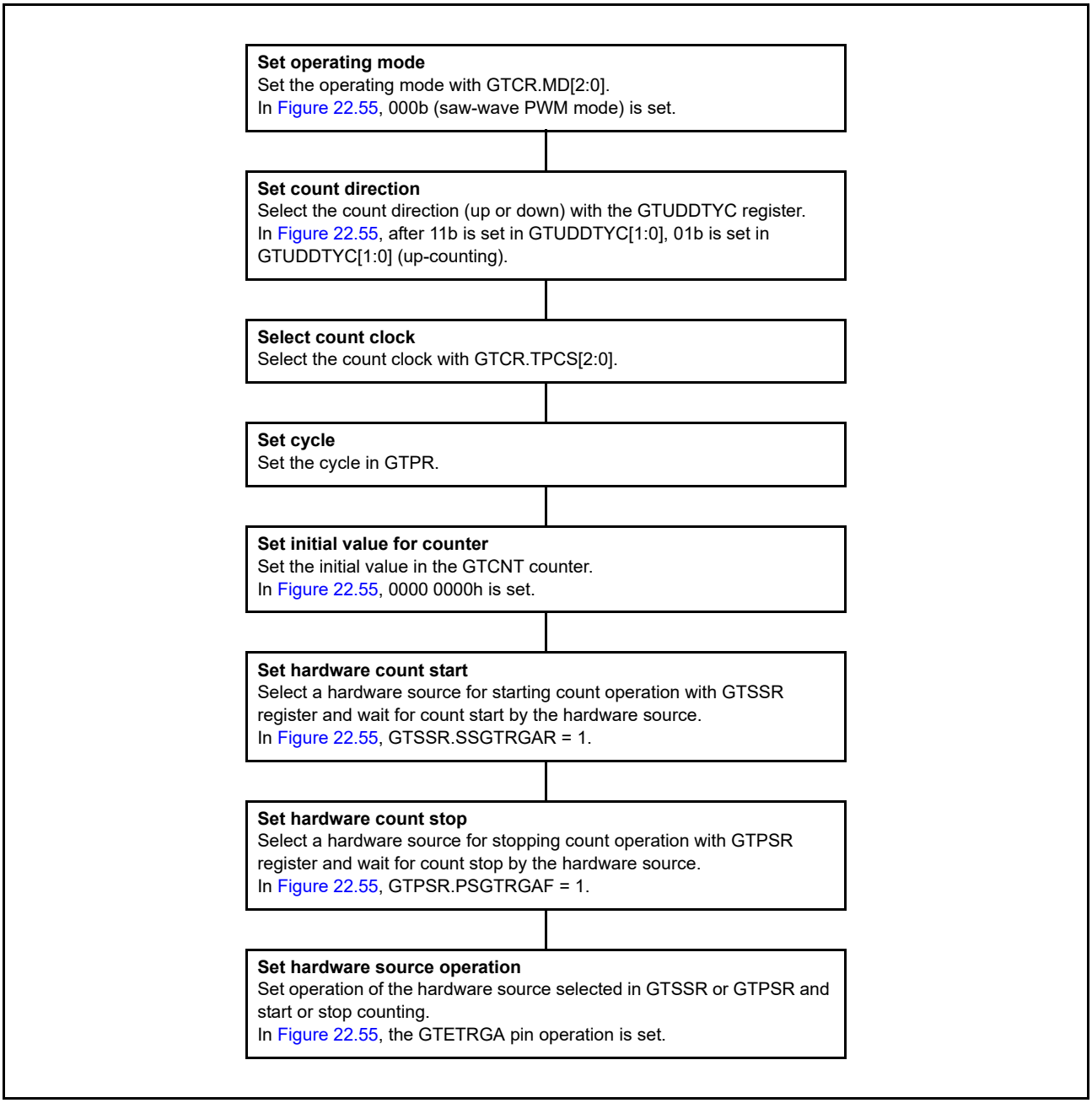


Figure 22.56 Example setting for count start/stop operation by a hardware source

22.3.7.3 Hardware clear operation

The GTCNT counter can be cleared by selecting a hardware source using GTCSR. The GPTn_OVF/GPTn_UDF (n = 0 to 12) interrupt (overflow/underflow interrupt) is not generated when the GTCNT counter is cleared by a hardware source or by software.

Figure 22.57 and Figure 22.58 show examples of the GTCNT counter clearing operation by a hardware source. Figure 22.59 shows the setting example. In this example, the GTCNT counter starts at the edge of the ELC_GPTA event input, and the counter stops and clears at the edge of the ELC_GPTB event input.

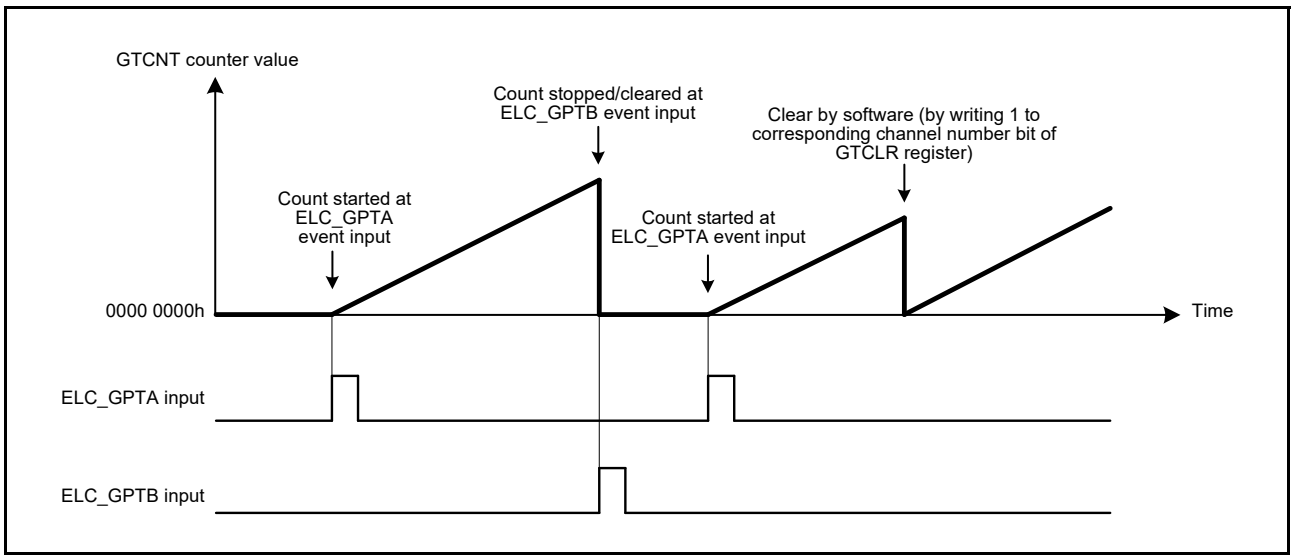


Figure 22.57 Examples of count clearing operation by hardware source in saw-wave up-counting, started at ELC_GPTA event input, and stopped/cleared at ELC_GPTB event input

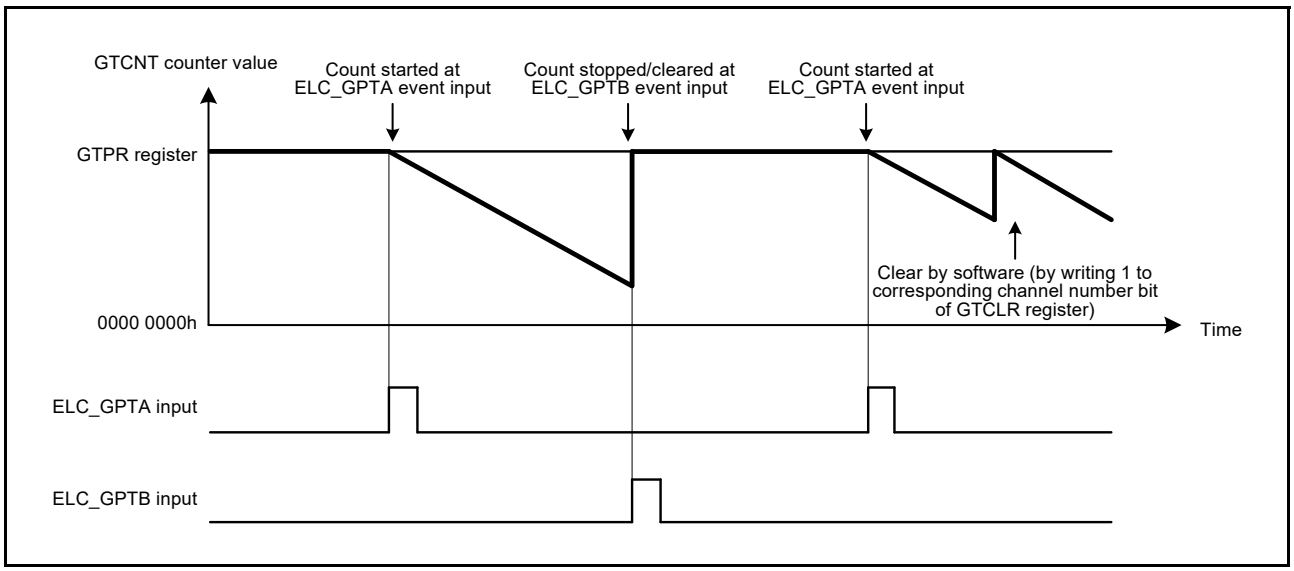


Figure 22.58 Examples of count clearing operation by hardware source in saw-wave down-counting, started at ELC_GPTA event input, and stopped/cleared at ELC_GPTB event input

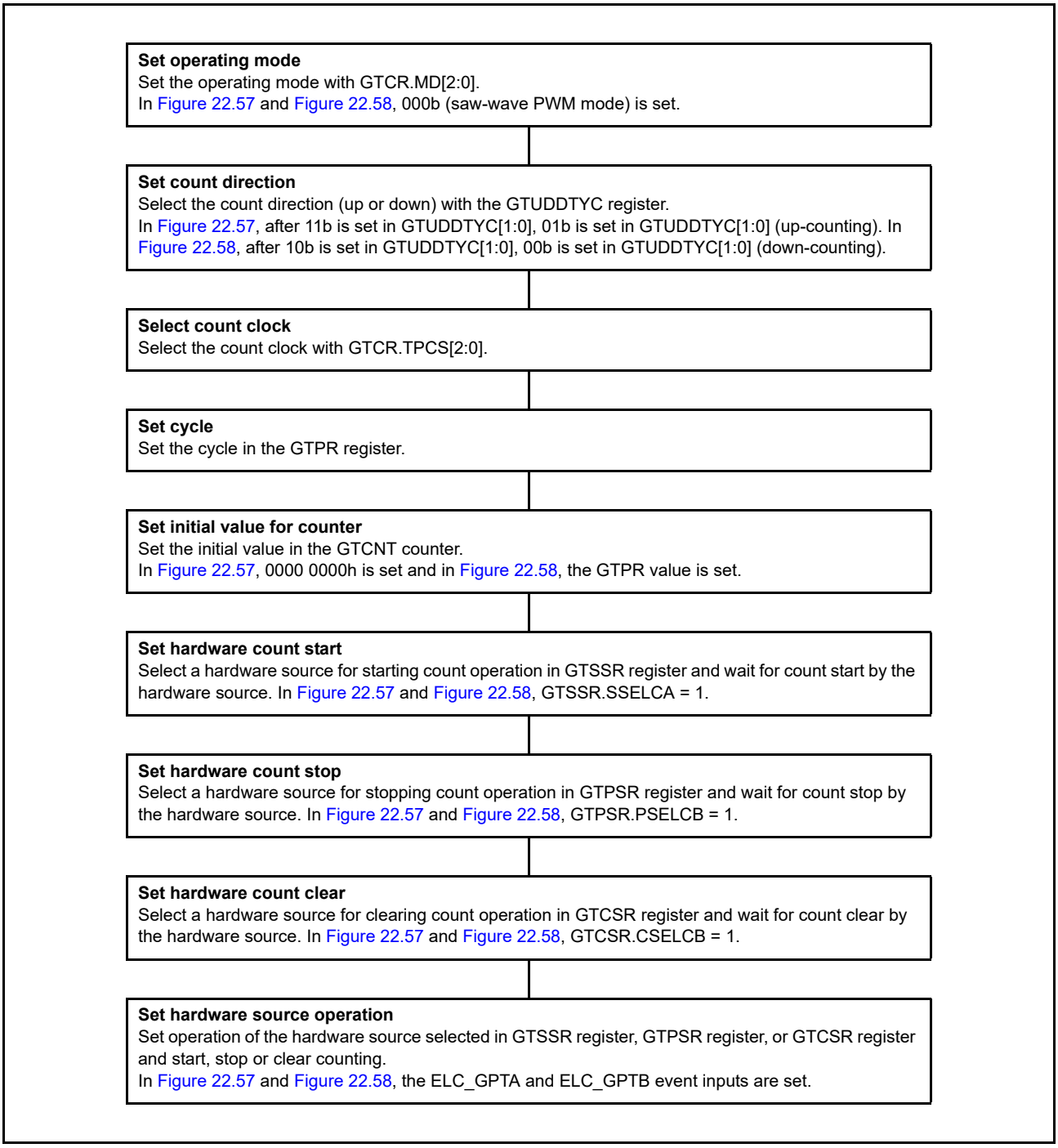


Figure 22.59 Example setting for count clearing operation by a hardware source

The GPTn_OVF/GPTn_UDF (n = 0 to 12) interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 22.60 shows the relationship between the counter clearing by a hardware source and the GPTn_OVF (n = 0 to 12) interrupt.

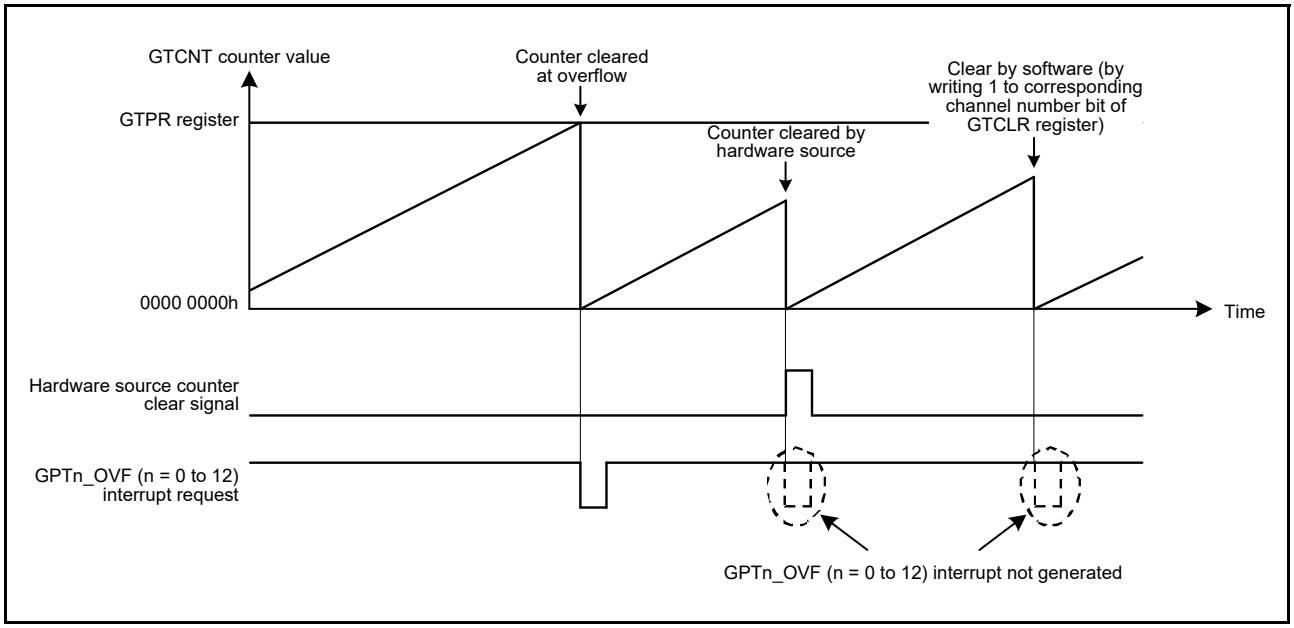


Figure 22.60 Relationship between counter clearing by hardware source and GPTn_OVF (n = 0 to 12) interrupt

22.3.8 Synchronized Operation

Synchronized operation on channels such as a synchronized start, stop, and clear operation can be performed.

22.3.8.1 Synchronized operation by software

The GTCNT counters can be started, stopped, and cleared on multiple channels by setting the associated GTSTR, GTSTP, or GTCLR bits simultaneously to 1.

Count start with a phase difference is possible by setting the initial value in the GTCNT counter and setting the associated GTSTR bits simultaneously to 1.

Figure 22.61 shows an example of a simultaneous start, stop, and clear by software. Figure 22.62 shows an example of phase start operation by software.

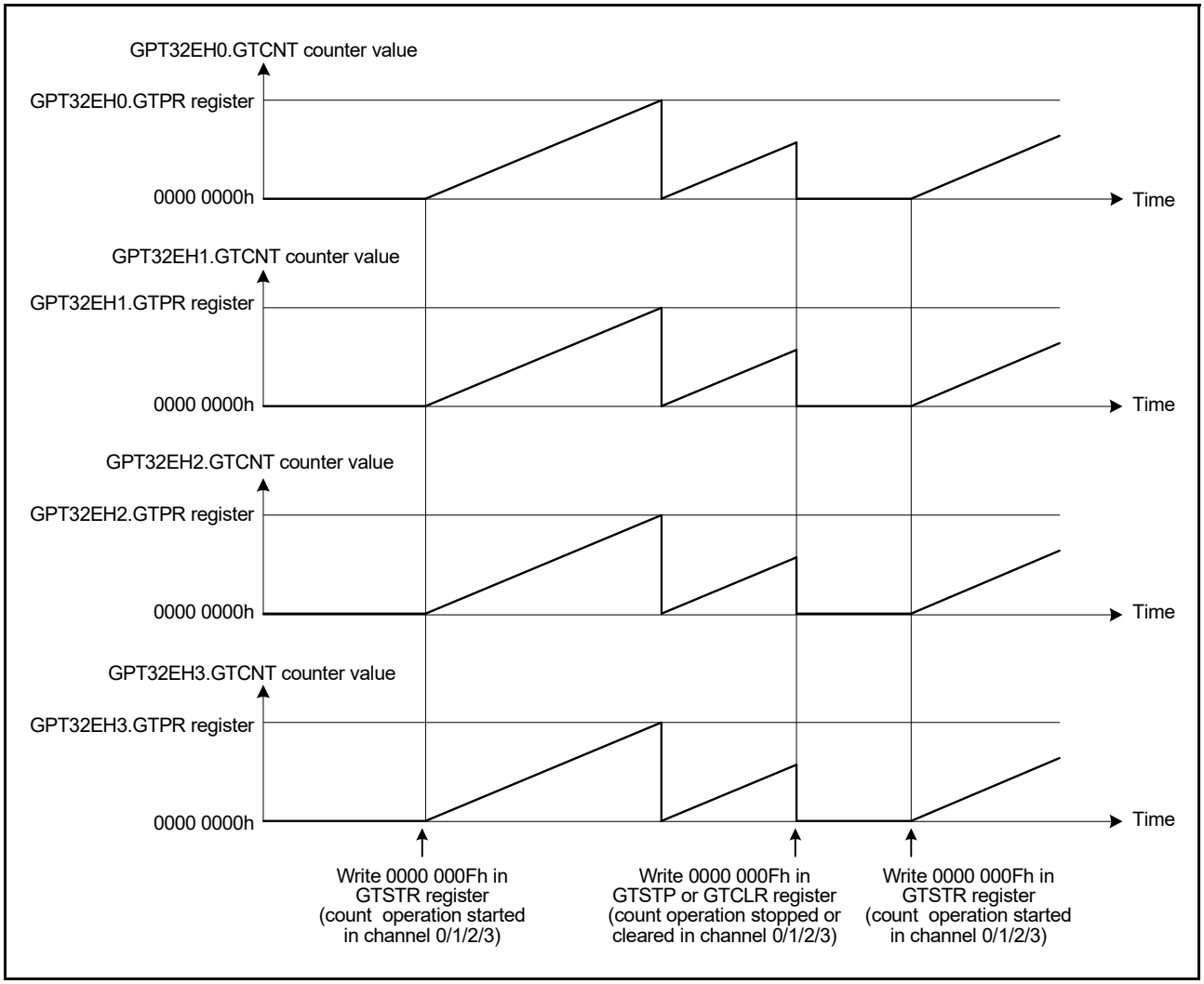


Figure 22.61 Example of a simultaneous start, stop, and clear by software, with the same count cycle (GTPR register value)

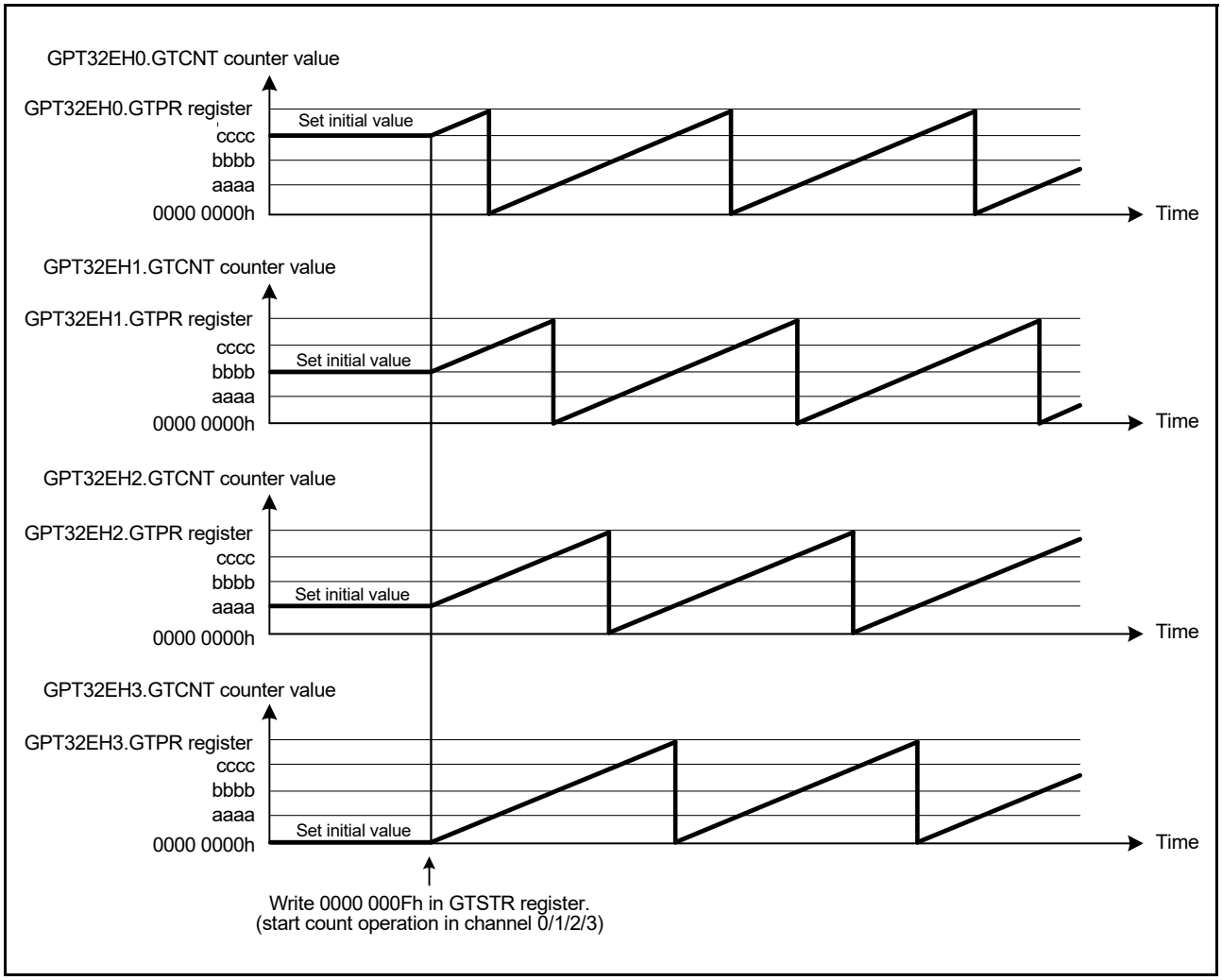


Figure 22.62 Example of software phase start with the same count cycle (GTPR register value)

22.3.8.2 Synchronized operation by hardware

The GTCNT counters can be started simultaneously by the following hardware sources:

- External trigger input
- ELC event input.

Figure 22.63 shows an example of a simultaneous start, stop, and clear operation by a hardware source. Figure 22.64 shows the setting example.

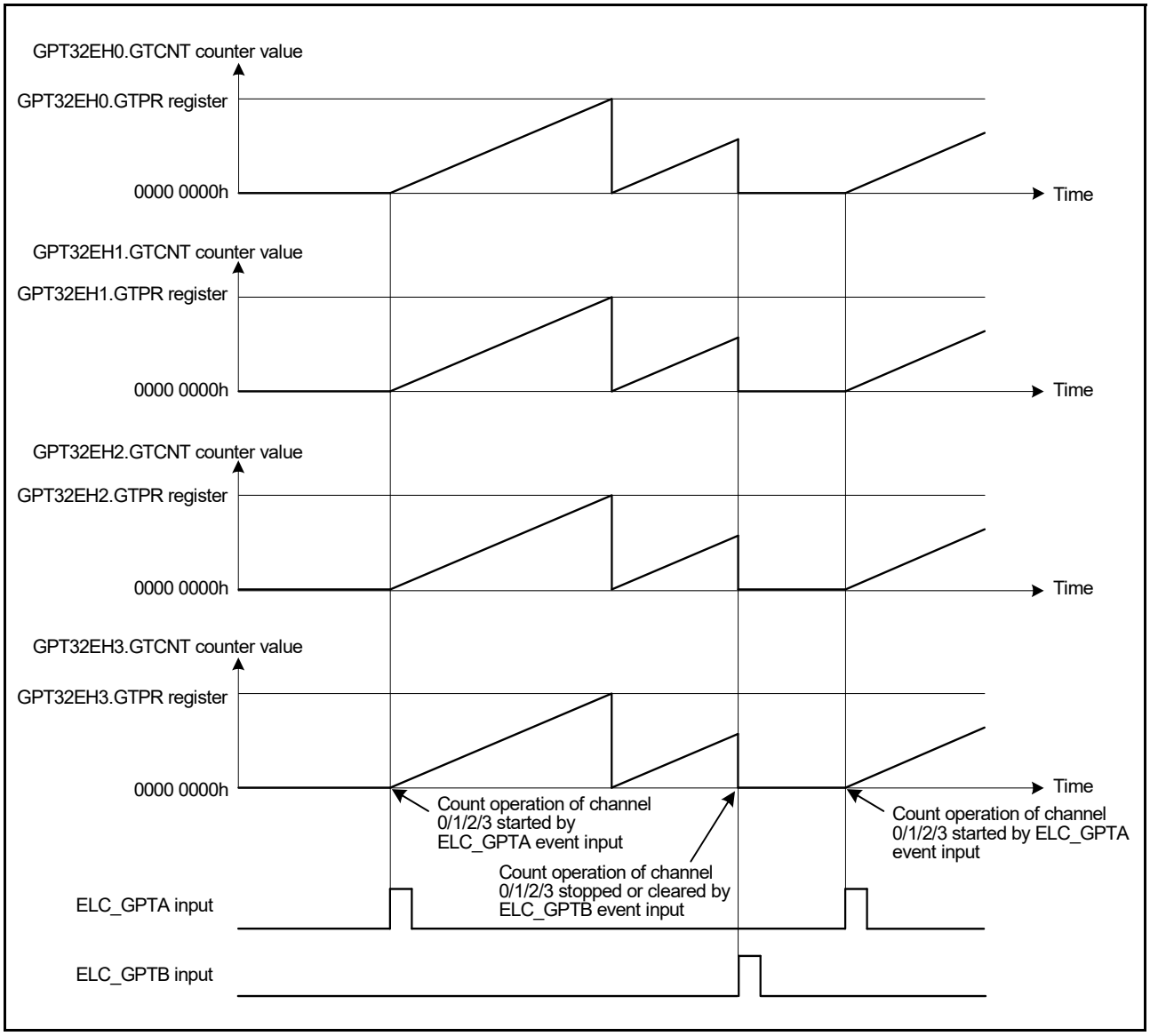


Figure 22.63 Example of a simultaneous start, stop, and clear by hardware source with the same count cycle (GTPR register value)

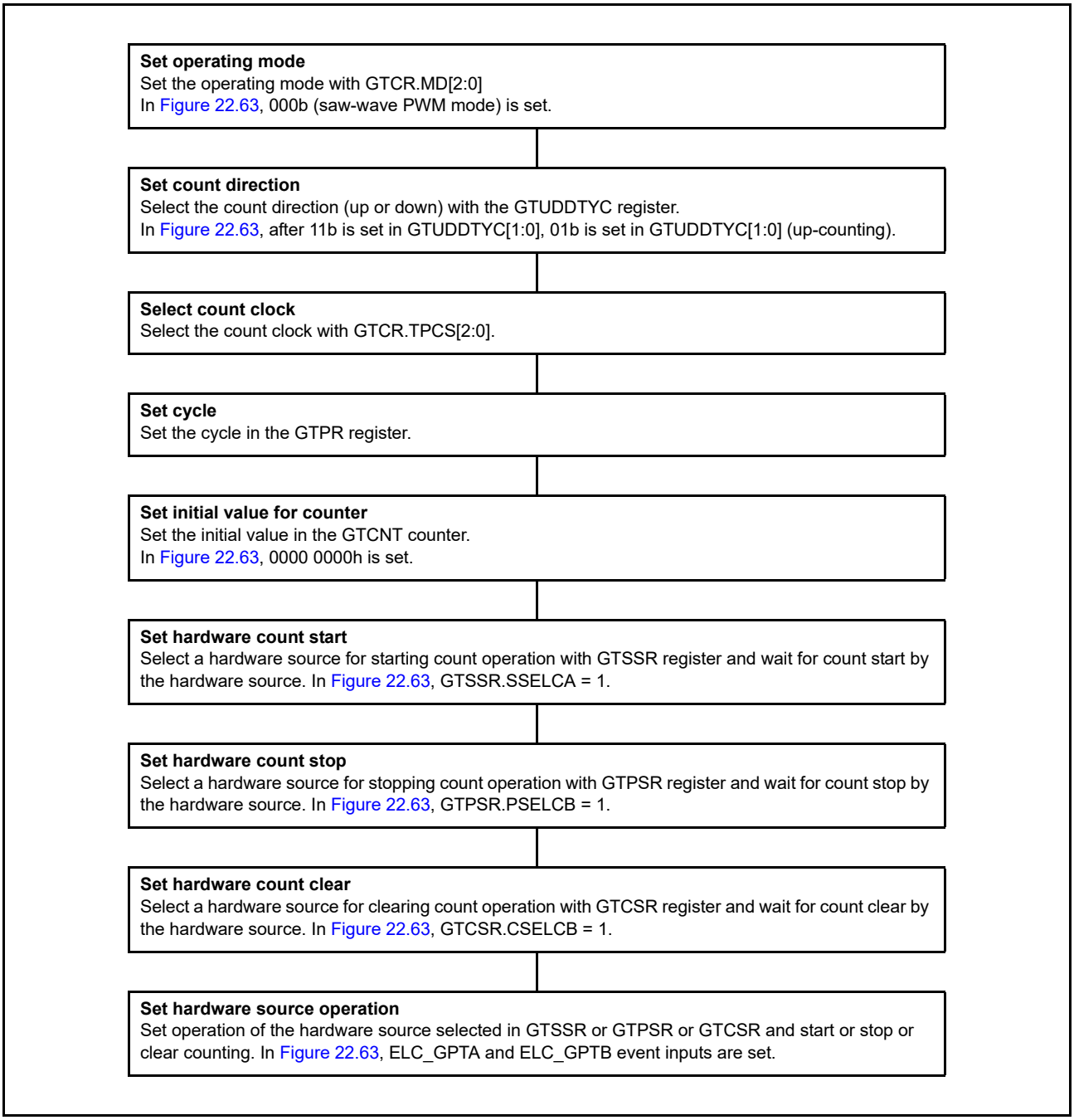


Figure 22.64 Example setting for simultaneous start by a hardware source

22.3.9 PWM Output Operation Examples

(1) Synchronized PWM output

The GPT outputs 26 phases of linked PWM waveforms for a maximum of 13 channels by multiple GPTs.

Figure 22.65 shows an example in which four channels perform synchronized operation in saw-wave PWM mode and eight phases of PWM waveforms are output. The GTIOCA is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCB is set so that it outputs low as the initial value, high at a GTCCRB compare match, and low at the cycle end.

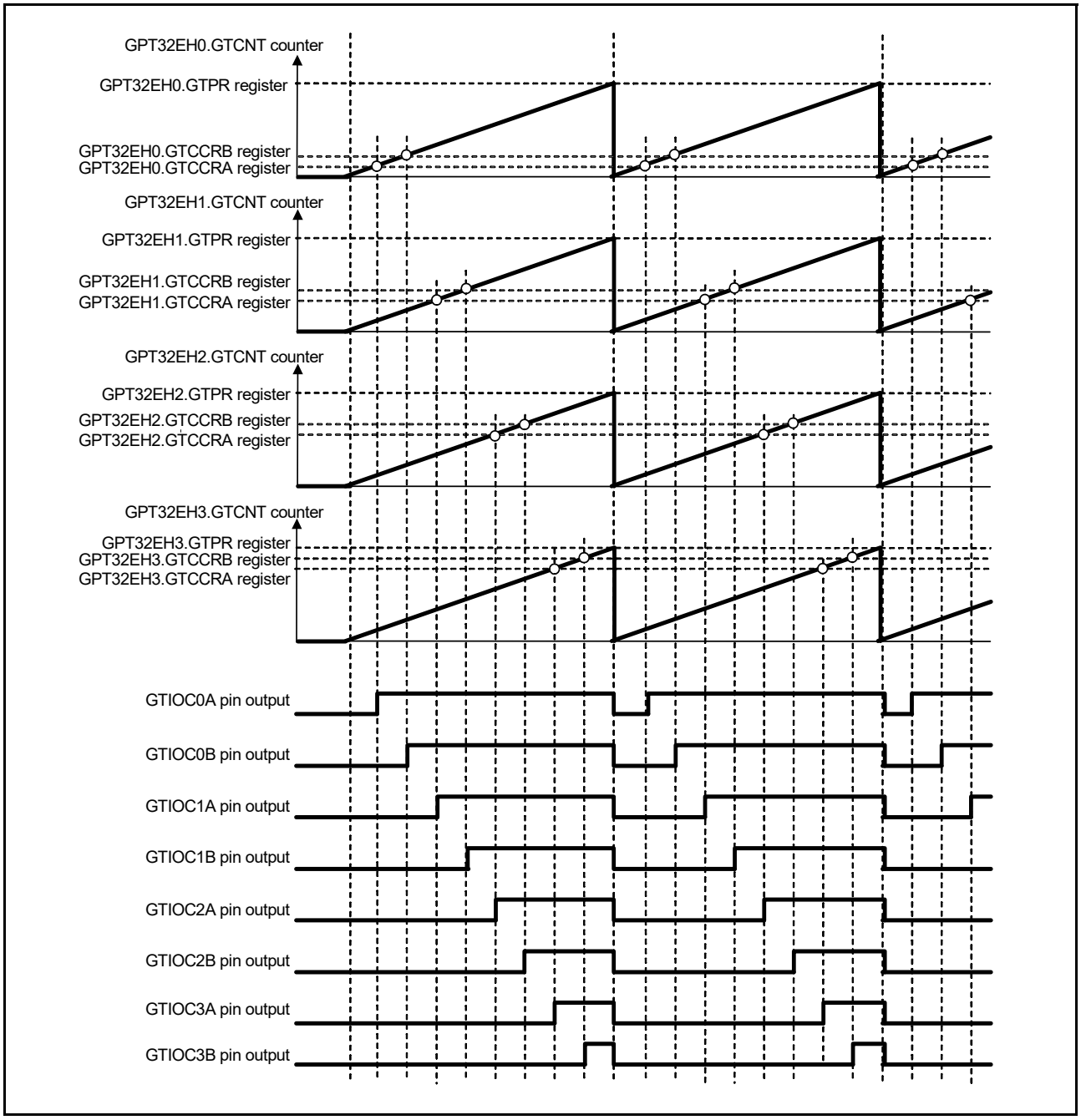


Figure 22.65 Example of synchronized PWM output

(2) 3-phase saw-wave complementary PWM output

Figure 22.66 shows an example in which three channels perform synchronized operation in saw-wave PWM mode and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

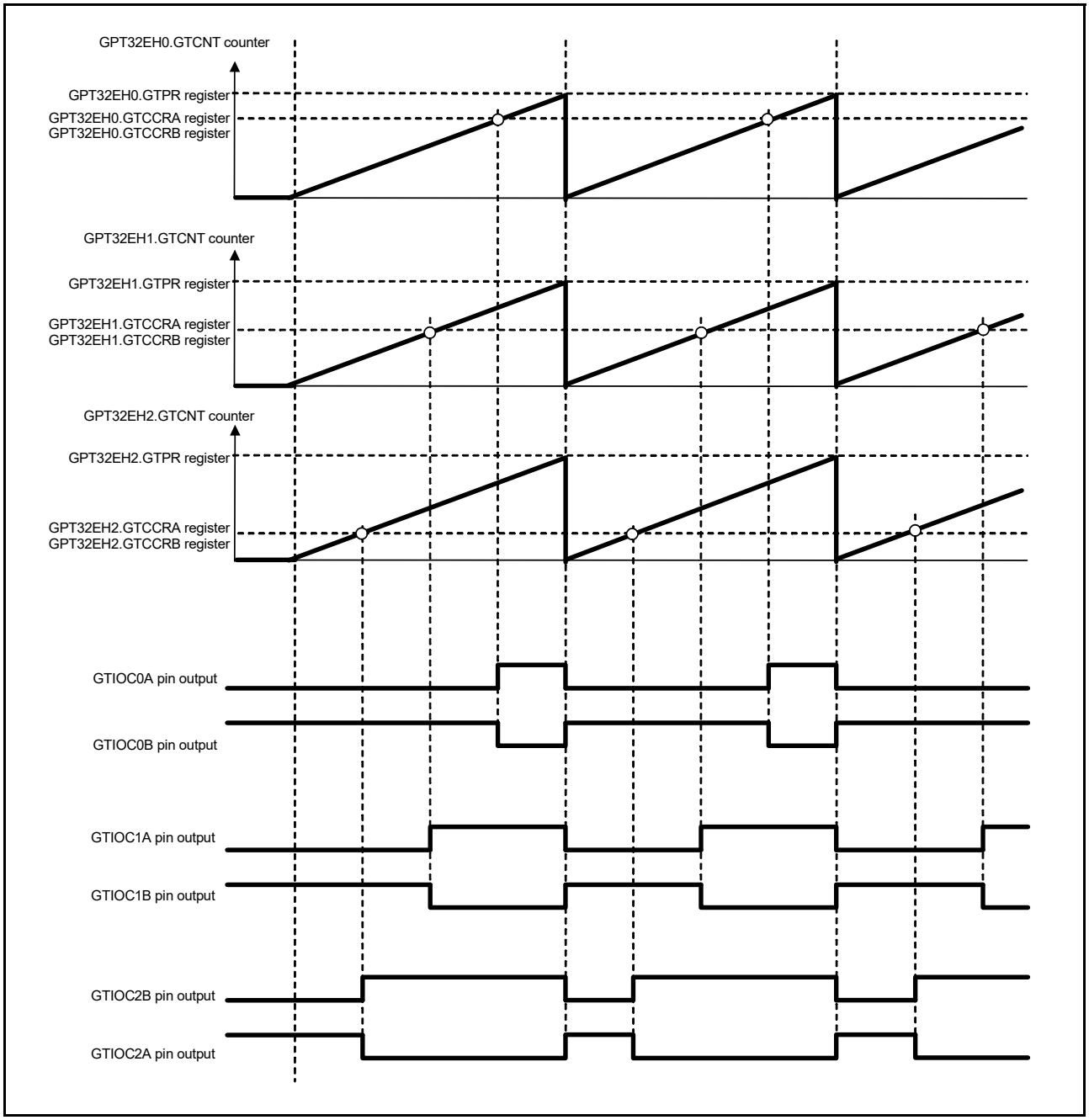


Figure 22.66 Example of 3-phase saw-wave complementary PWM output

(3) 3-phase saw-wave complementary PWM output with automatic dead time setting

Figure 22.67 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

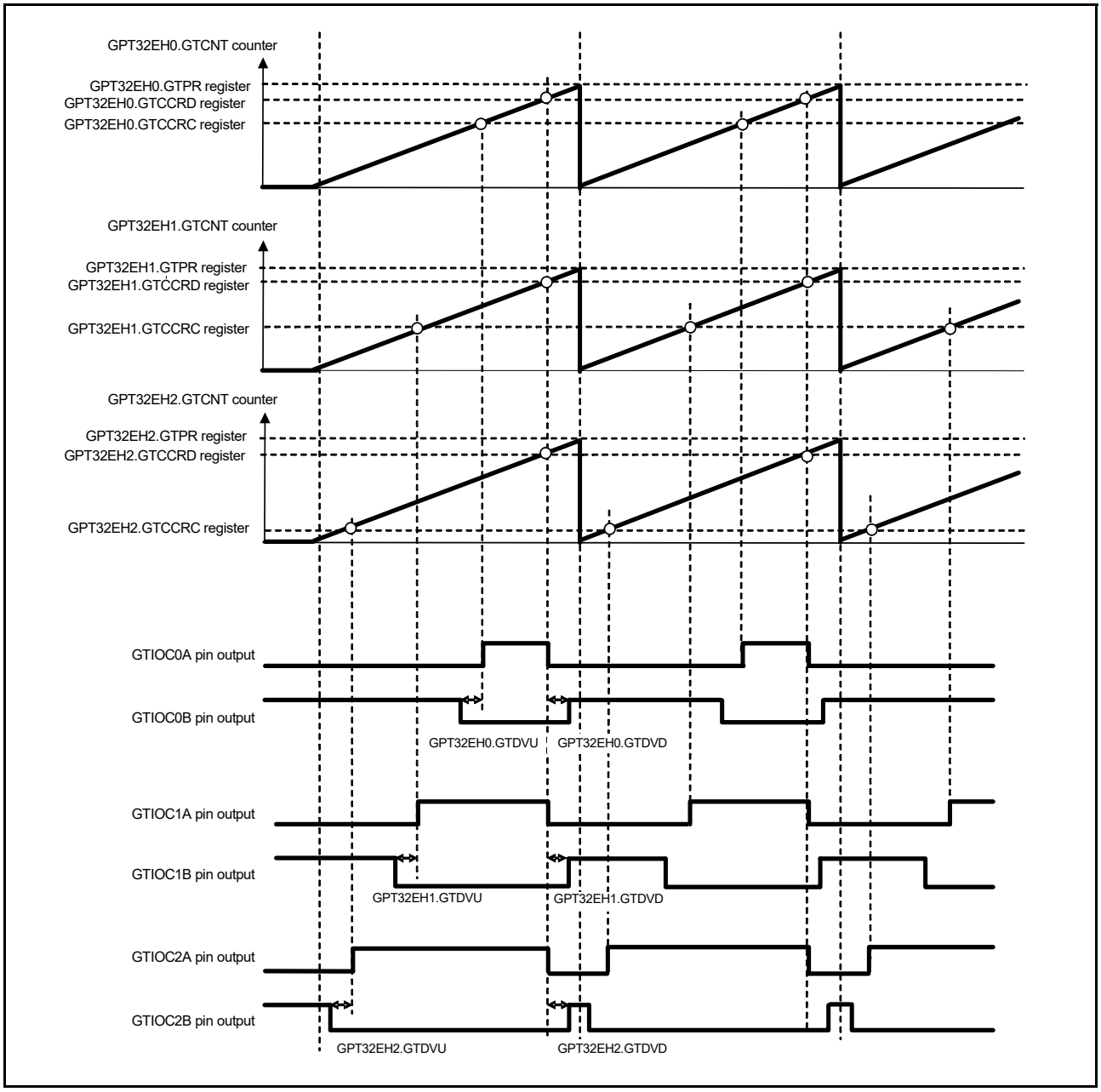


Figure 22.67 Example of 3-phase saw-wave complementary PWM output with automatic dead time setting

(4) 3-phase triangle-wave complementary PWM output

Figure 22.68 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

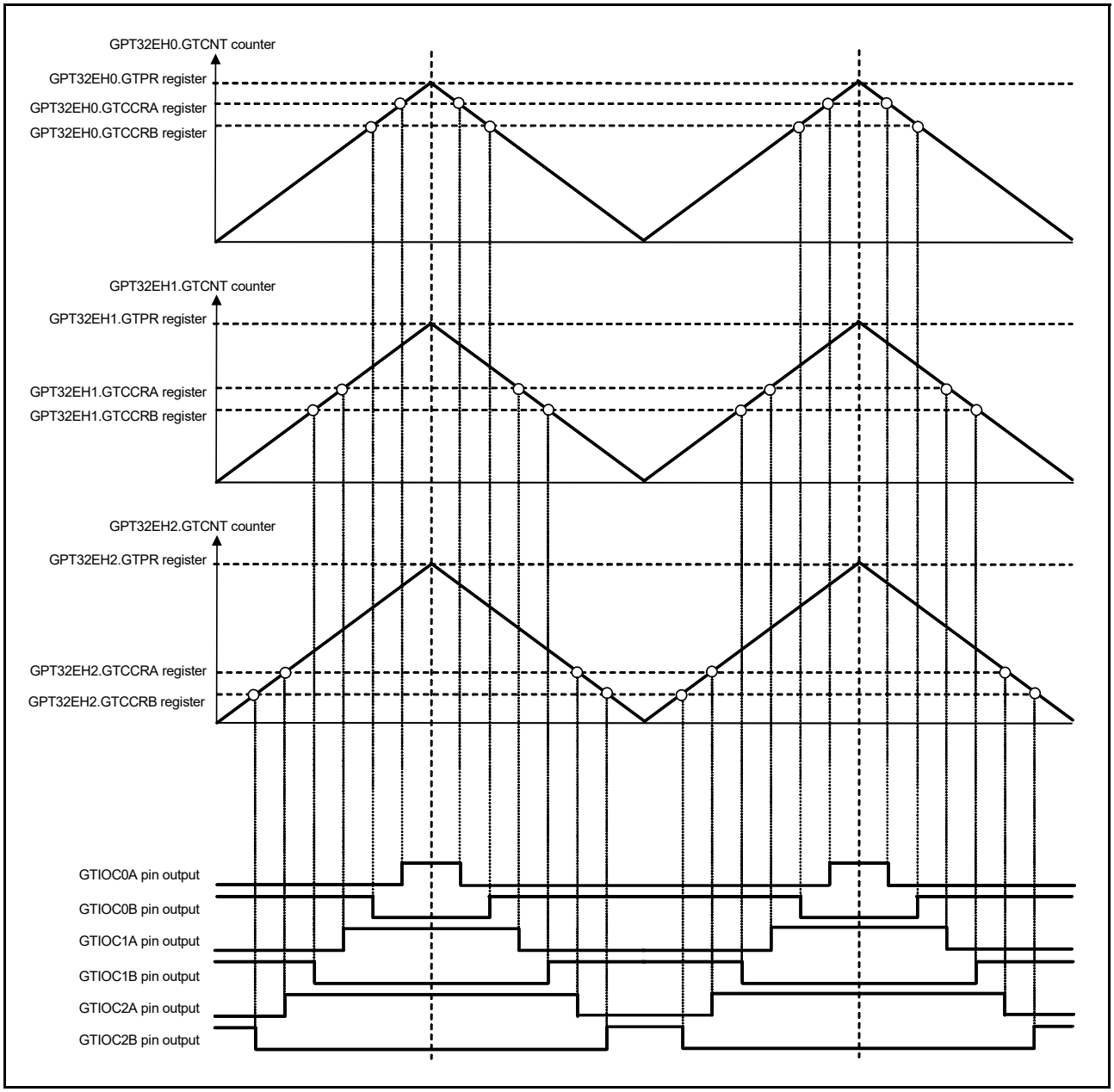


Figure 22.68 Example of 3-phase triangle-wave complementary PWM output

(5) 3-phase triangle-wave complementary PWM output with automatic dead time setting

Figure 22.69 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

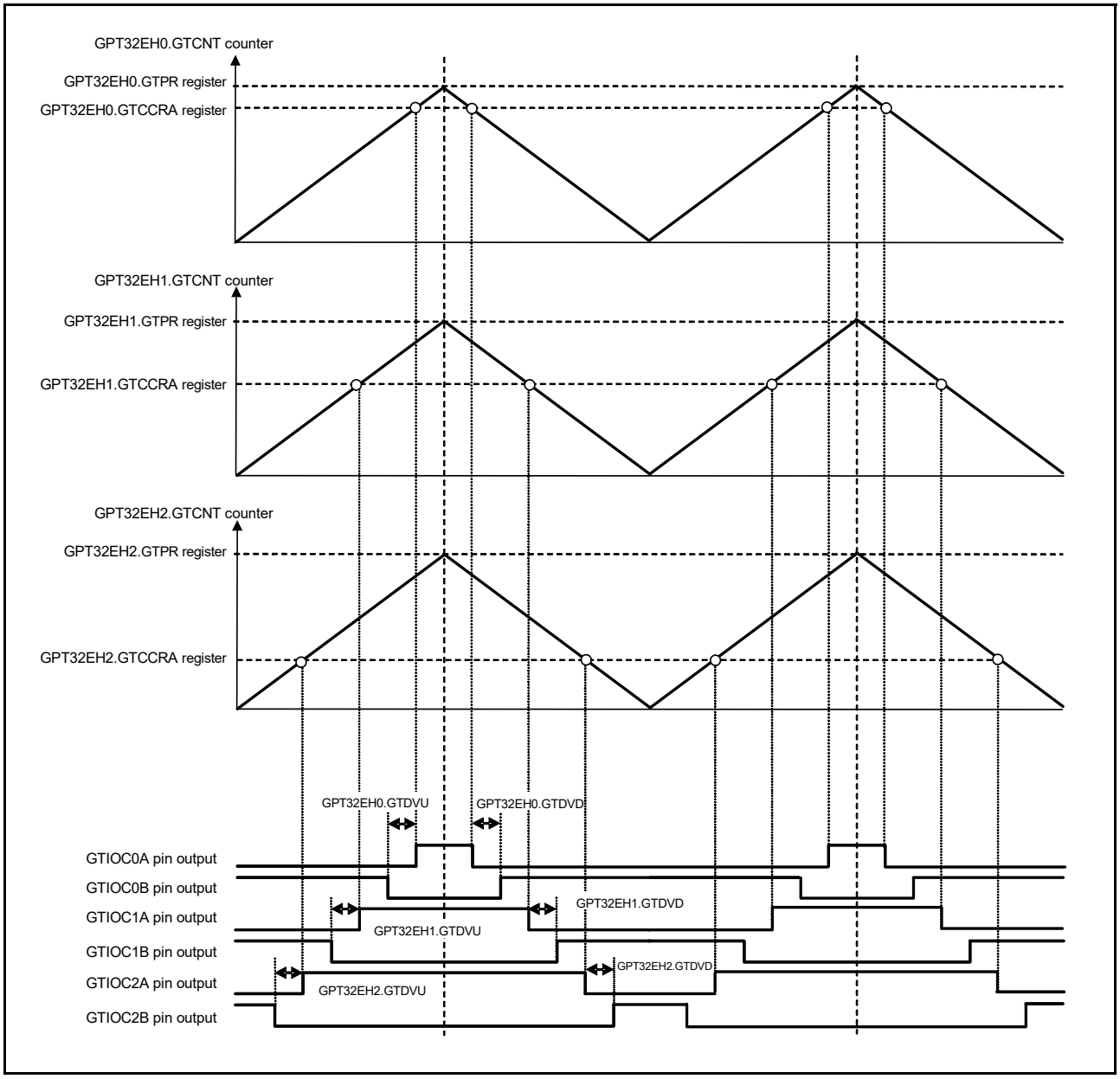


Figure 22.69 Example of 3-phase triangle-wave complementary PWM output with automatic dead time setting

(6) 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

Figure 22.70 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

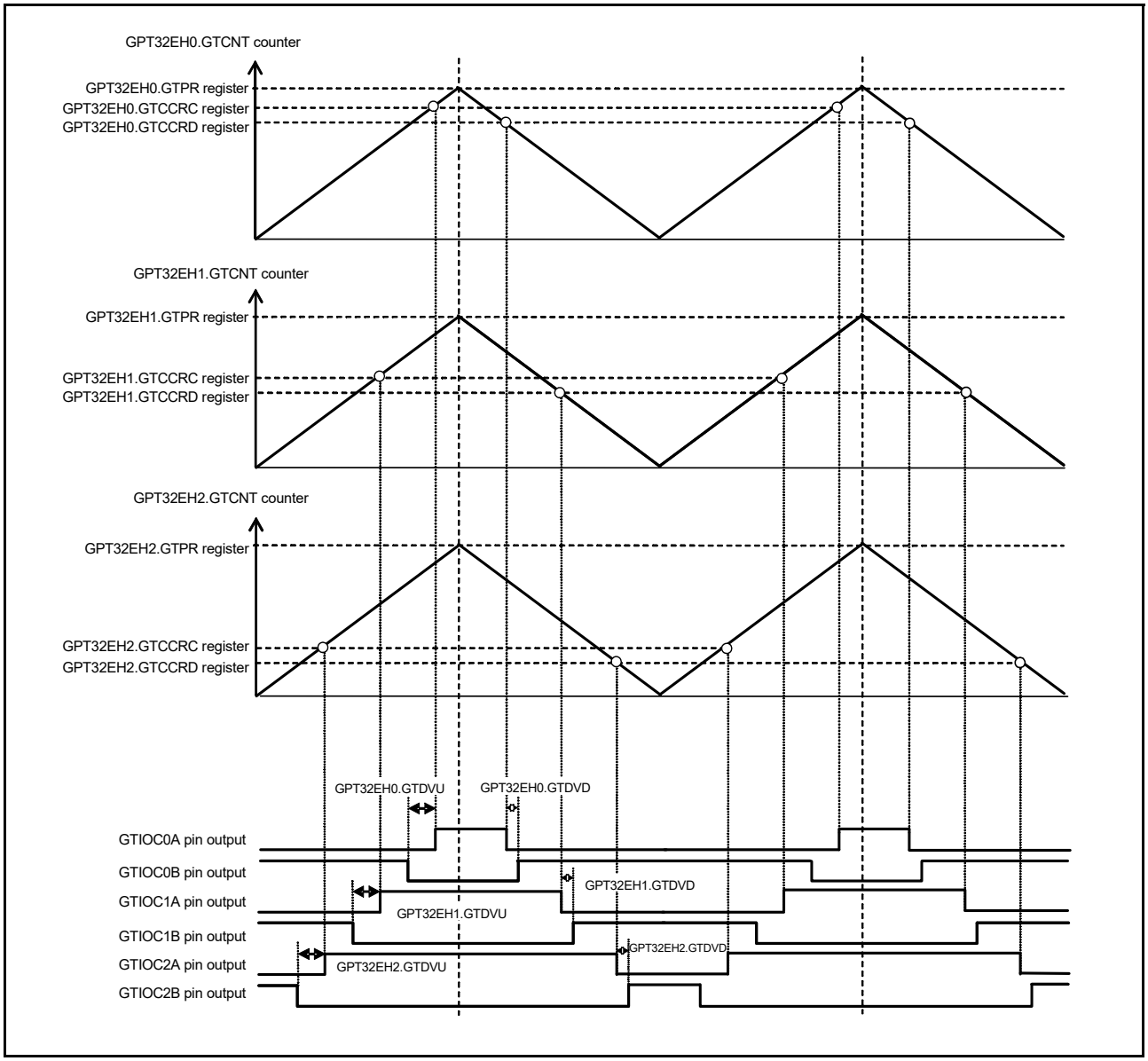


Figure 22.70 Example of 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

22.3.10 Phase Counting Function

The phase difference between the GTIOCA and GTIOCB pin inputs is detected and the associated GTCNT counts up or counts down. The detectable phase difference is available in any combination with the relationship between the edge and the level of GTIOCA and GTIOCB pin inputs being set in the GTUPSR and GTDNSR registers. For details on count operation, see section 22.3.1.1, Counter operation.

Figure 22.71 to Figure 22.80 show phase counting functions 1 to 5. Table 22.8 to Table 22.17 show conditions of up-counting or down-counting and list settings for the GTUPSR and GTDNSR registers.

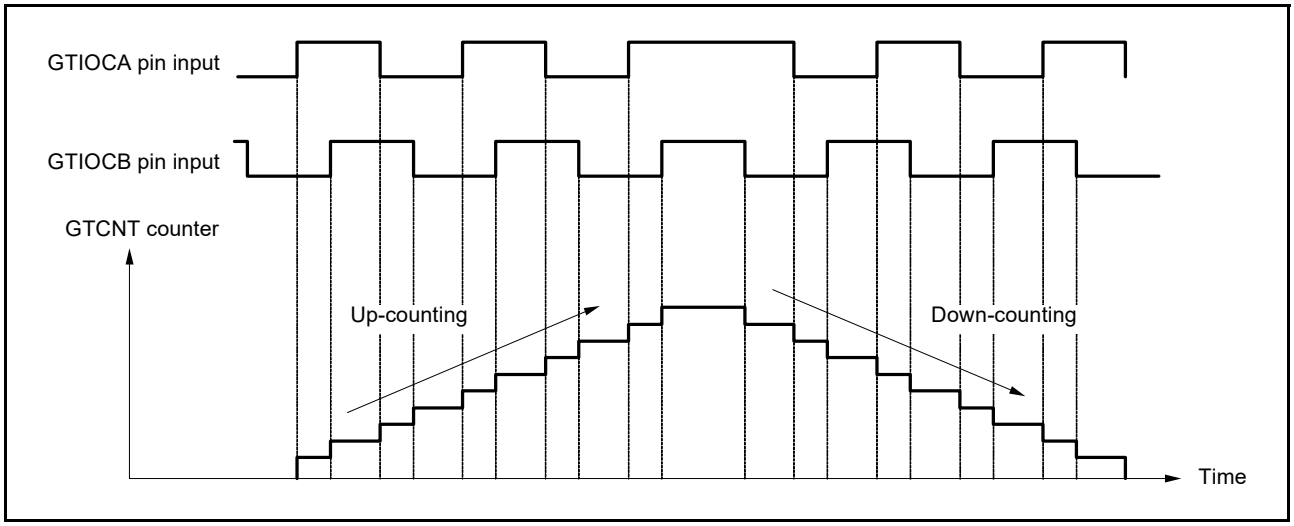


Figure 22.71 Example of phase counting function 1

Table 22.8 Conditions of up-counting/down-counting in phase counting function 1

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0000 6900h GTDNSR = 0000 9600h
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

↑ : Rising edge

↓ : Falling edge

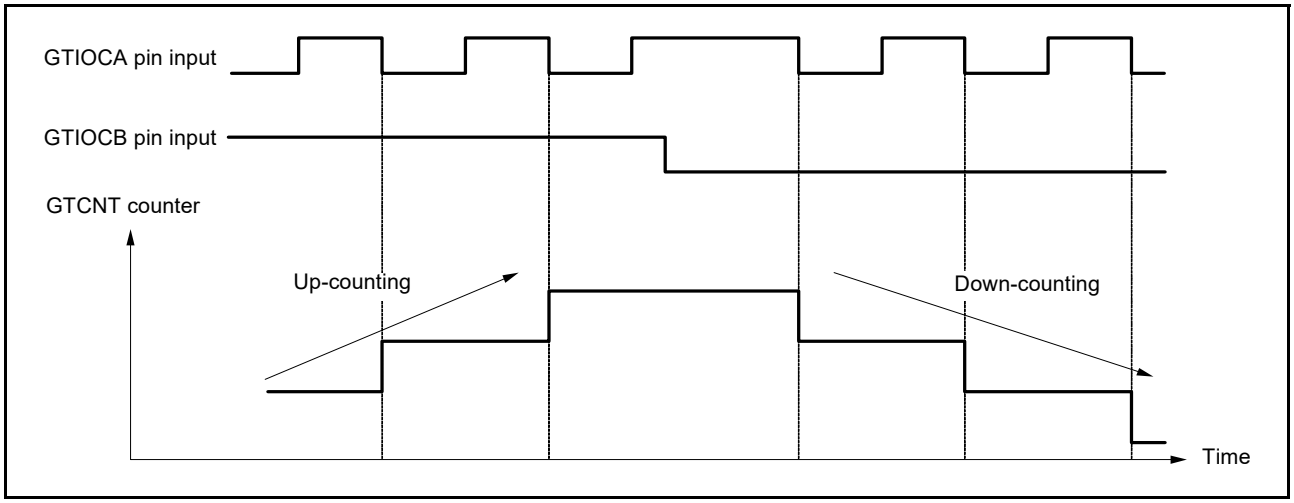


Figure 22.72 Example of phase counting function 2 (A)

Table 22.9 Conditions of up-counting/down-counting in phase counting function 2 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0800h GTDNSR = 0000 0400h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Don't care	
Low	↑		
↑	High		
↓	Low	Down-counting	

↑ : Rising edge

↓ : Falling edge

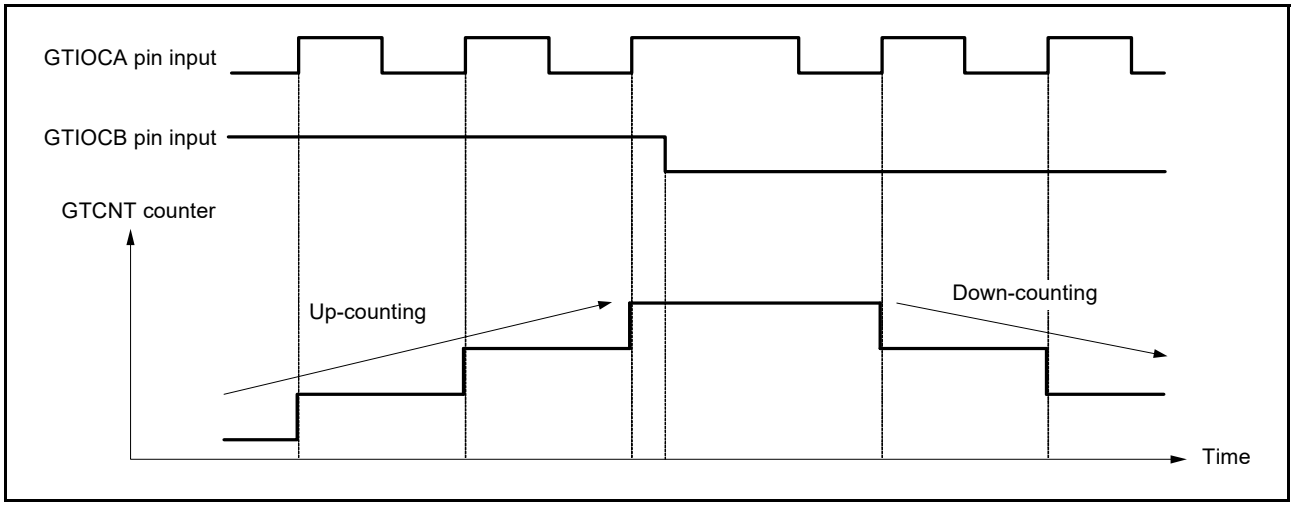


Figure 22.73 Example of phase counting function 2 (B)

Table 22.10 Conditions of up-counting/down-counting in phase counting function 2 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0200h GTDNSR = 0000 0100h
Low	↓		
↑	Low	Down-counting	
↓	High	Don't care	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Don't care	

↑ : Rising edge

↓ : Falling edge

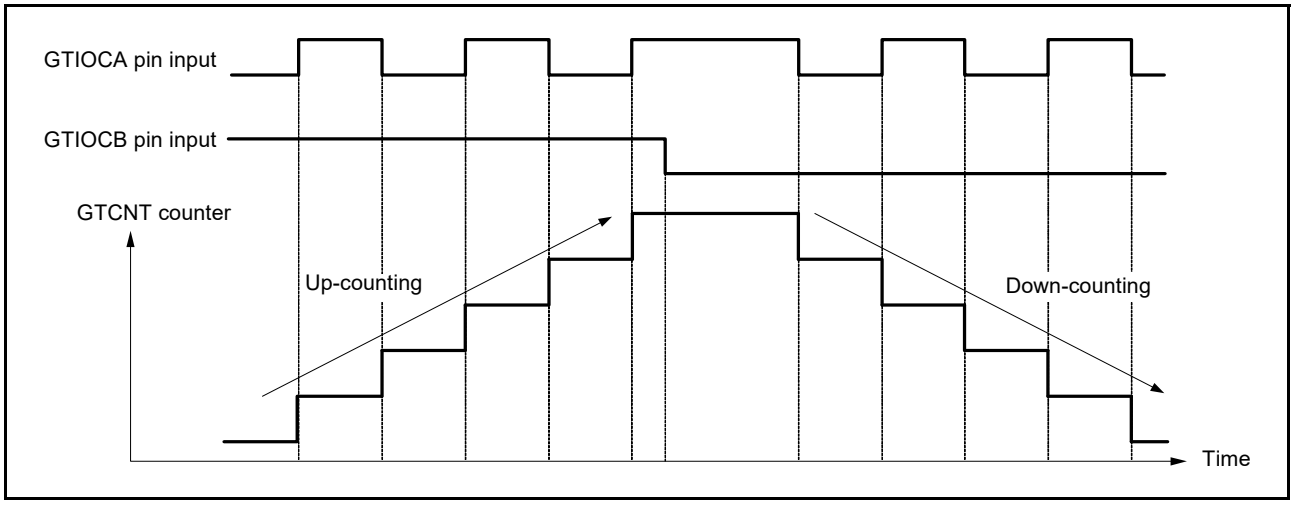


Figure 22.74 Example of phase counting function 2 (C)

Table 22.11 Conditions of up-counting/down-counting in phase counting function 2 (C)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0A00h GTDNSR = 0000 0500h
Low	↓		
↑	Low	Down-counting	
↓	High	Don't care	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

↑ : Rising edge

↓ : Falling edge

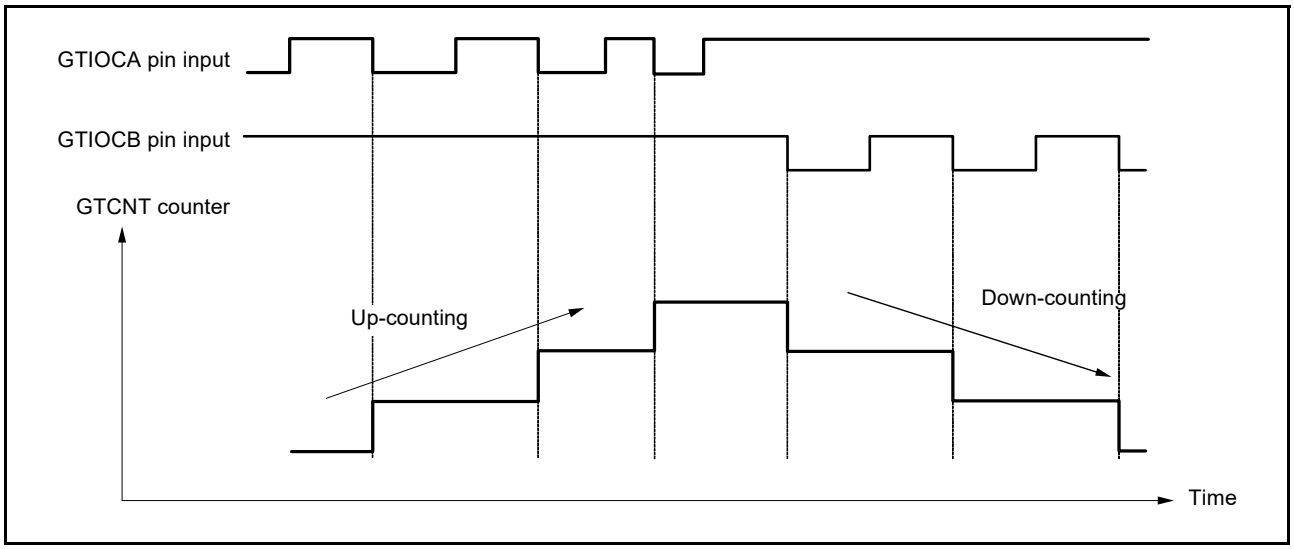


Figure 22.75 Example of phase counting function 3 (A)

Table 22.12 Conditions of up-counting/down-counting in phase counting function 3 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0800h GTDNSR = 0000 8000h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Don't care	
↑	High		
↓	Low		

↑ : Rising edge

↓ : Falling edge

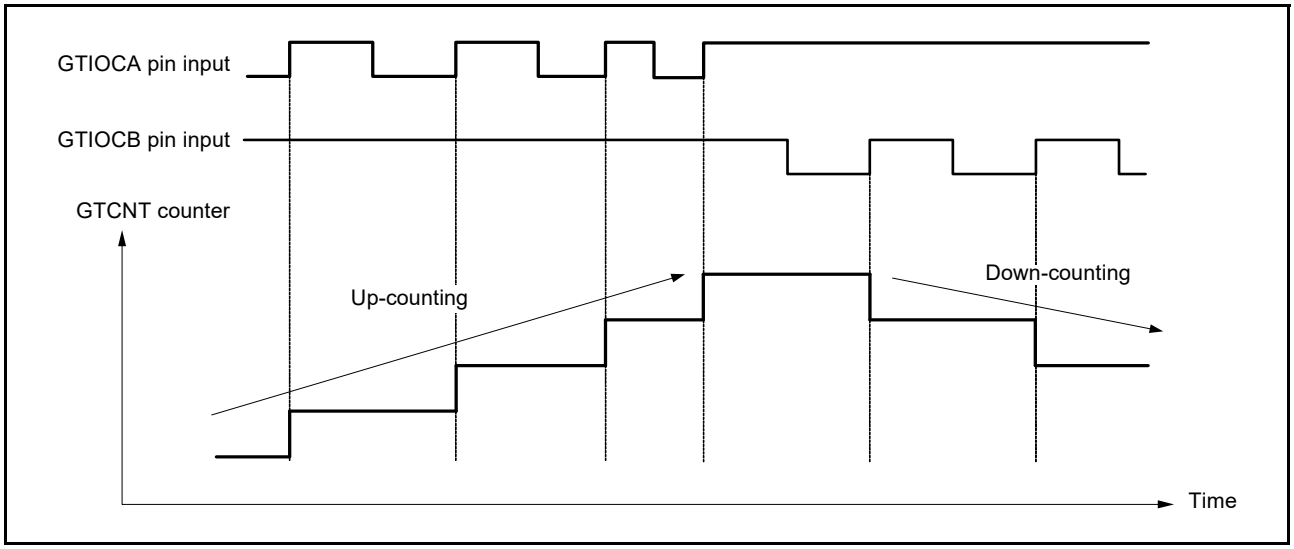


Figure 22.76 Example of phase counting function 3 (B)

Table 22.13 Conditions of up-counting/down-counting in phase counting function 3 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0000 0200h GTDNSR = 0000 2000h
Low	↓	Don't care	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Don't care	

↑ : Rising edge

↓ : Falling edge

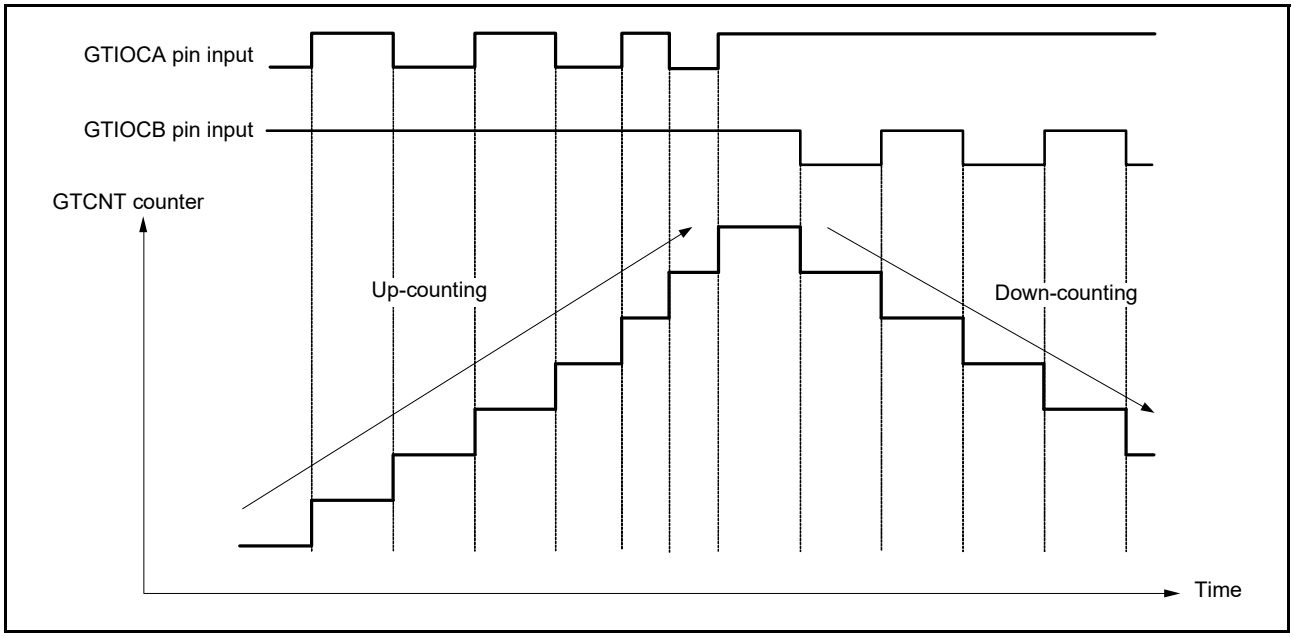


Figure 22.77 Example of phase counting function 3 (C)

Table 22.14 Conditions of up-counting/down-counting in phase counting function 3 (C)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0000 0A00h GTDNSR = 0000 A000h
Low	↓	Don't care	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Don't care	
↑	High	Up-counting	
↓	Low	Don't care	

↑ : Rising edge

↓ : Falling edge

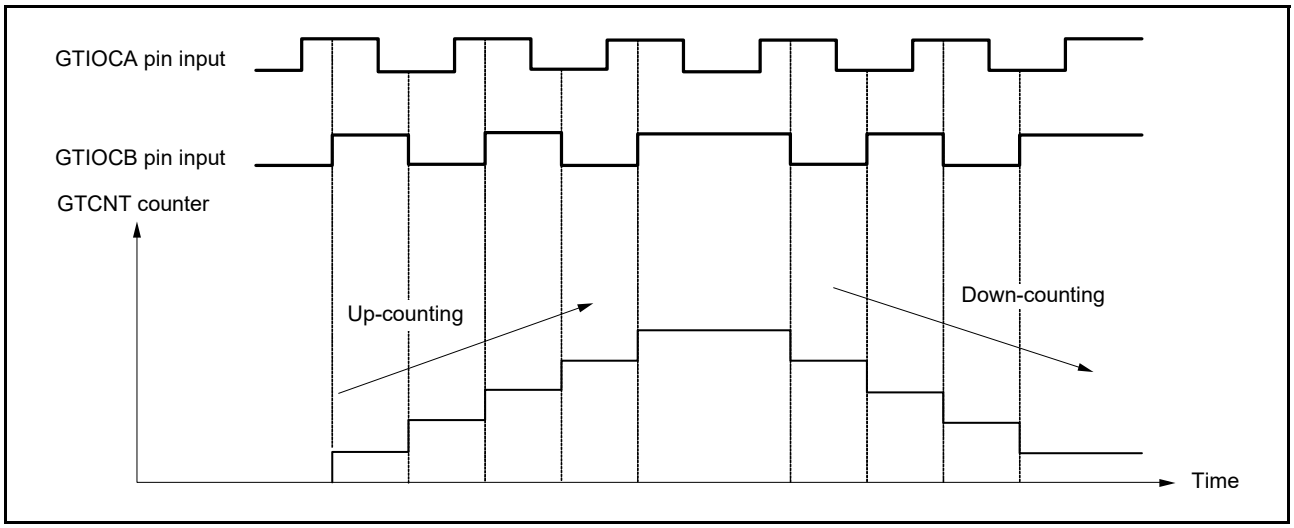


Figure 22.78 Example of phase counting function 4

Table 22.15 Conditions of up-counting/down-counting in phase counting function 4

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0000 6000h GTDNSR = 0000 9000h
Low	↓		
↑	Low	Don't care	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	Don't care	
↓	Low		

↑ : Rising edge

↓ : Falling edge

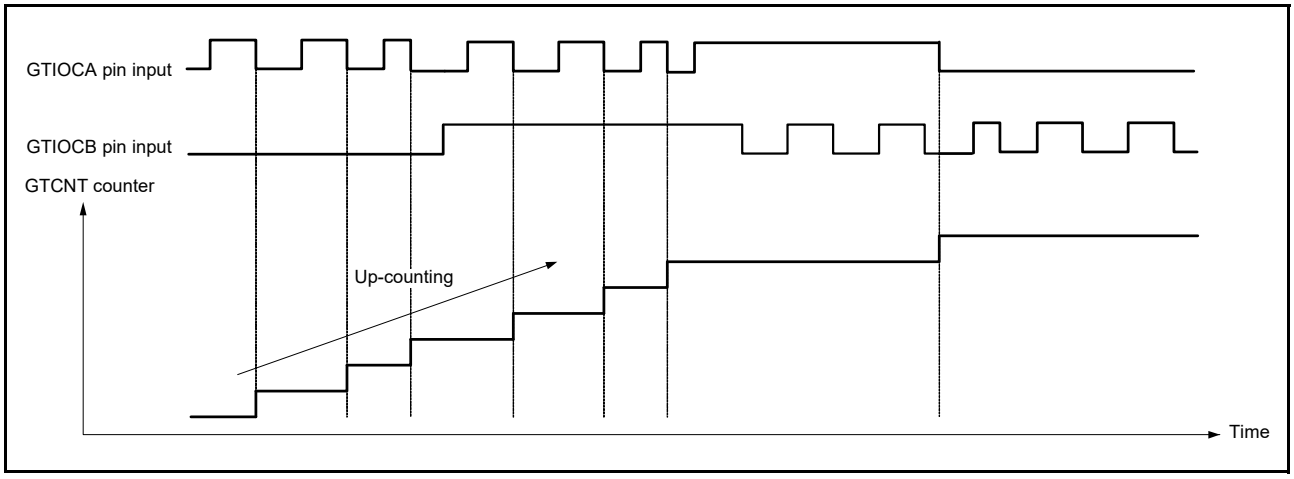


Figure 22.79 Example of phase counting function 5 (A)

Table 22.16 Conditions of up-counting/down-counting in phase counting function 5 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0C00h GTDNSR = 0000 0000h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Don't care	
Low	↑		
↑	High		
↓	Low	Up-counting	

↑ : Rising edge

↓ : Falling edge

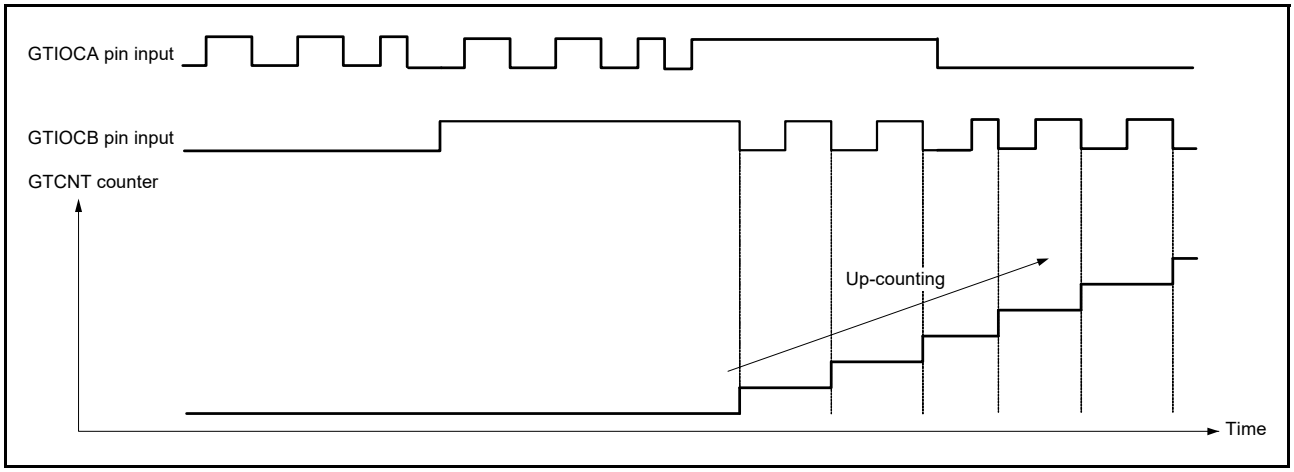


Figure 22.80 Example of phase counting function 5 (B)

Table 22.17 Conditions of up-counting/down-counting in phase counting function 5 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0C00h GTDNSR = 0000 0000h
Low	↓	Up-counting	
↑	Low	Don't care	
↓	High		
High	↓	Up-counting	
Low	↑	Don't care	
↑	High		
↓	Low		

↑ : Rising edge

↓ : Falling edge

22.3.11 Output Phase Switching (GPT_OPS)

GPT_OPS provides a function for easy control of brushless DC motor operation using the Output Phase Switching Control Register (OPSCR).

GPT_OPS outputs a PWM signal to be used for chopper control or level signal for each phase (U-positive phase/negative phase, V-positive phase/negative phase, W-positive phase/negative phase) of the 6-phase motor control. This function uses a soft setting value (OPSCR.UF, VF, WF) set by software or external signals detected by the Hall element, a PWM waveform of GPT32EH0.GTIOCA.

Figure 22.81 shows the conceptual diagram of GPT_OPS control flow.

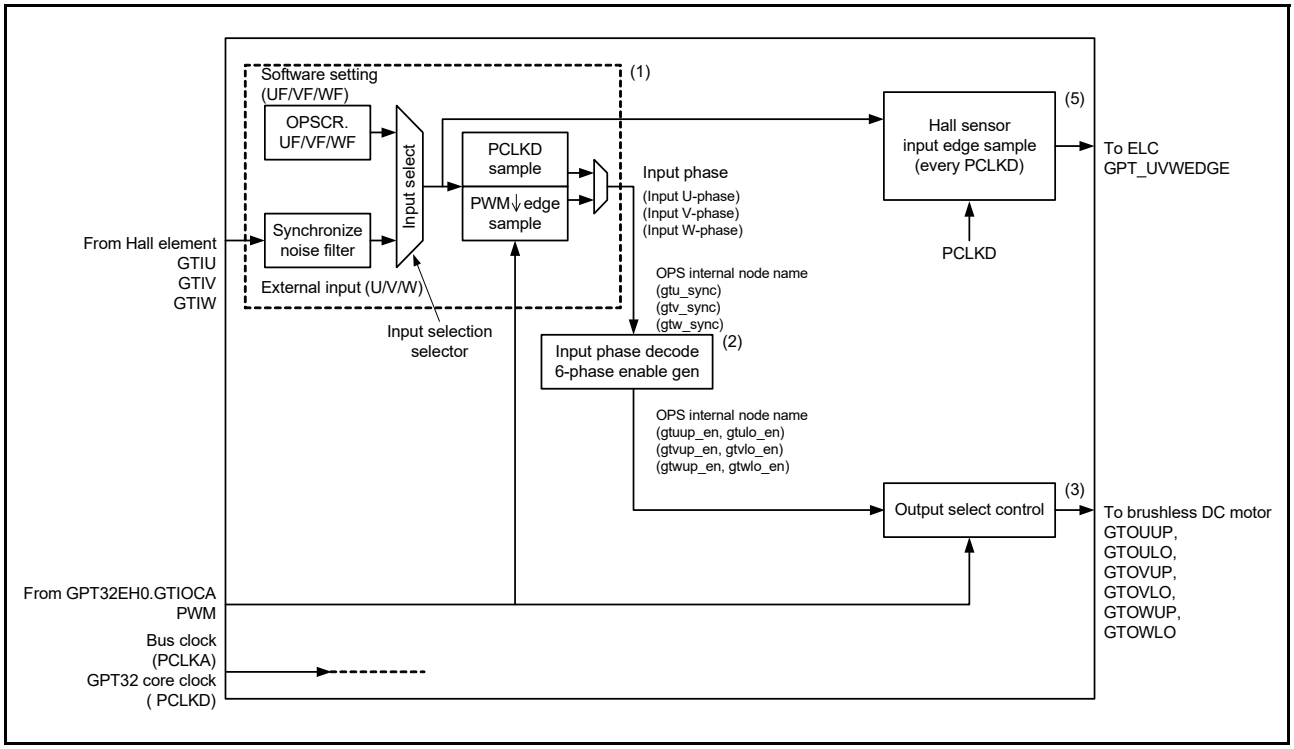


Figure 22.81 Conceptual diagram of GPT_OPS control flow

Figure 22.82 shows a 6-phase level signals output example of a GPT_OPS operation.

The GPT_UVWEDGE signal in Figure 22.82 is the Hall sensor input edge to ELC output.

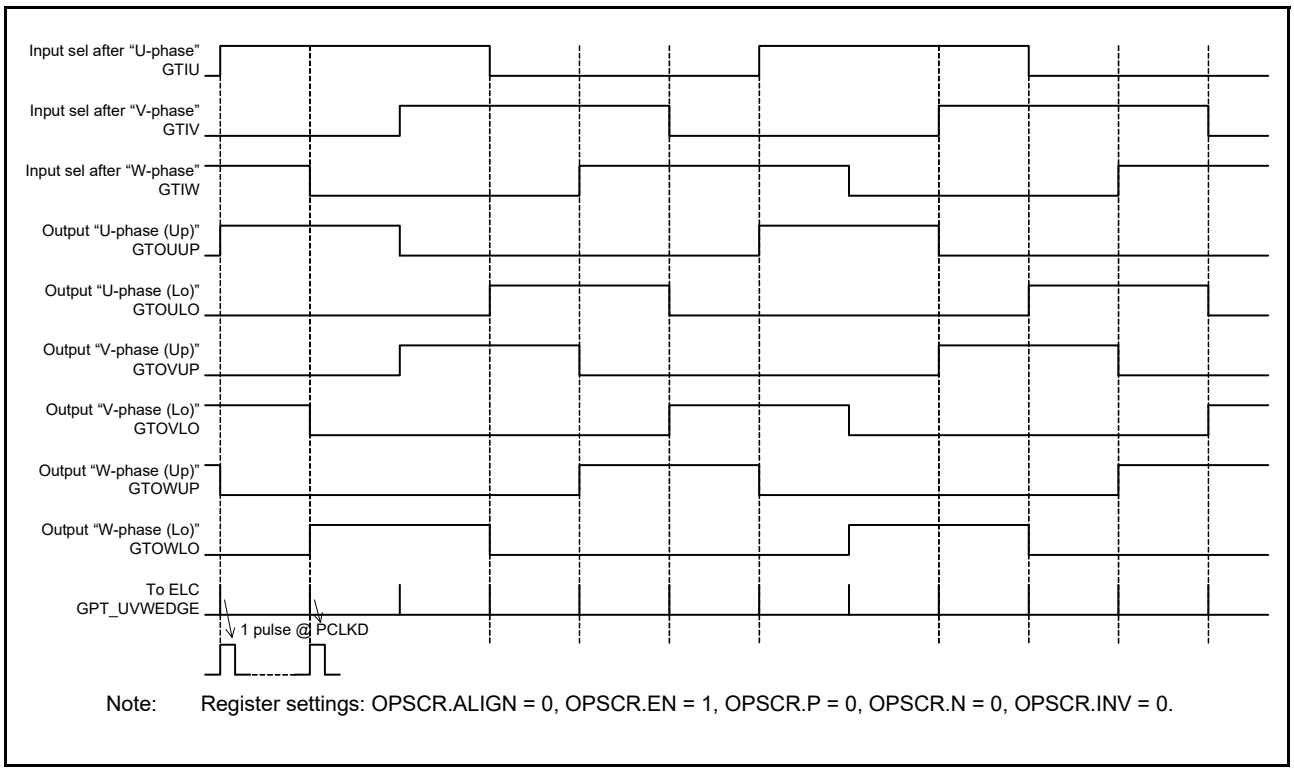


Figure 22.82 Example of 6-phase level output operation

Figure 22.83 shows a 6-phase PWM output example of a GPT_OPS operation with chopper control.

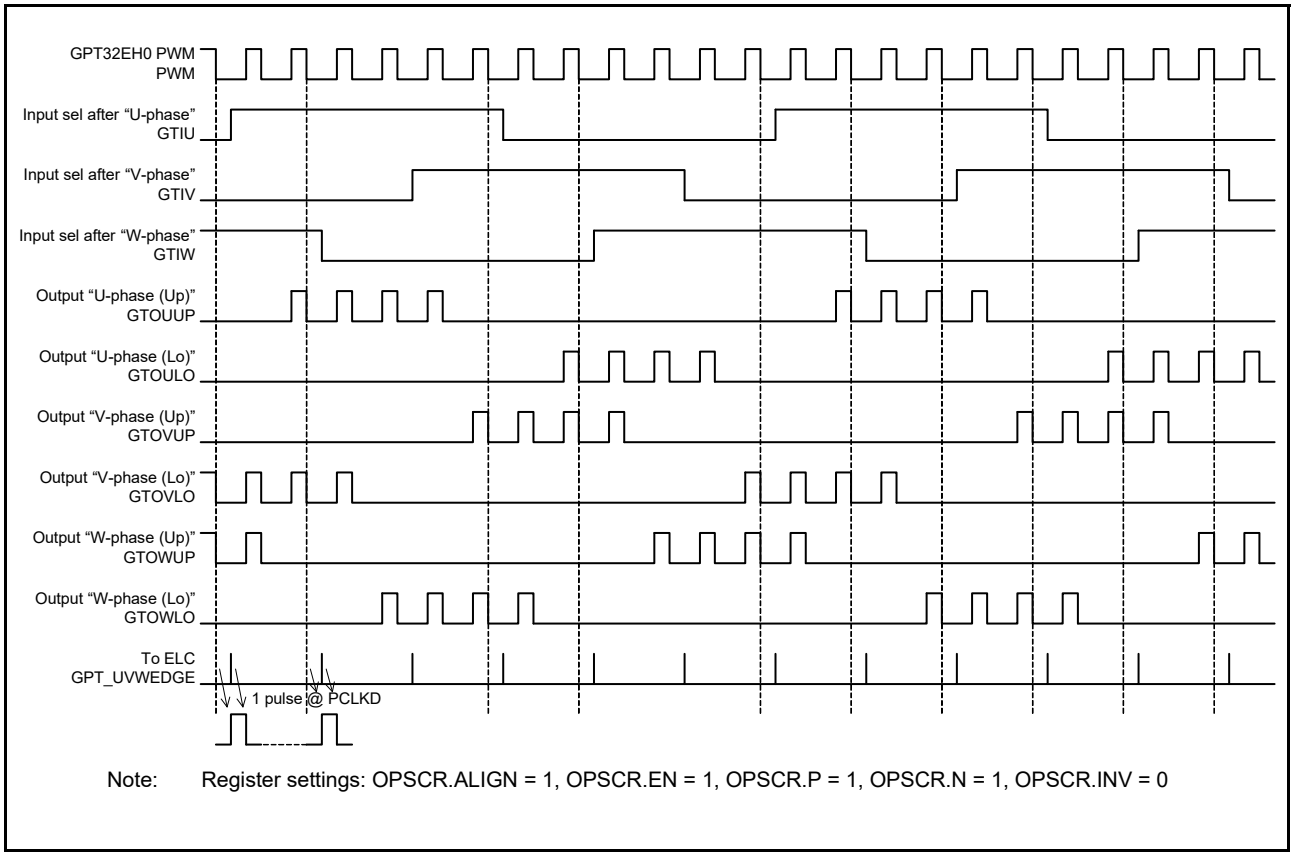


Figure 22.83 Example of 6-phase PWM output operation with chopper control

Figure 22.84 shows a 6-phase PWM output example of an output disable control operation.

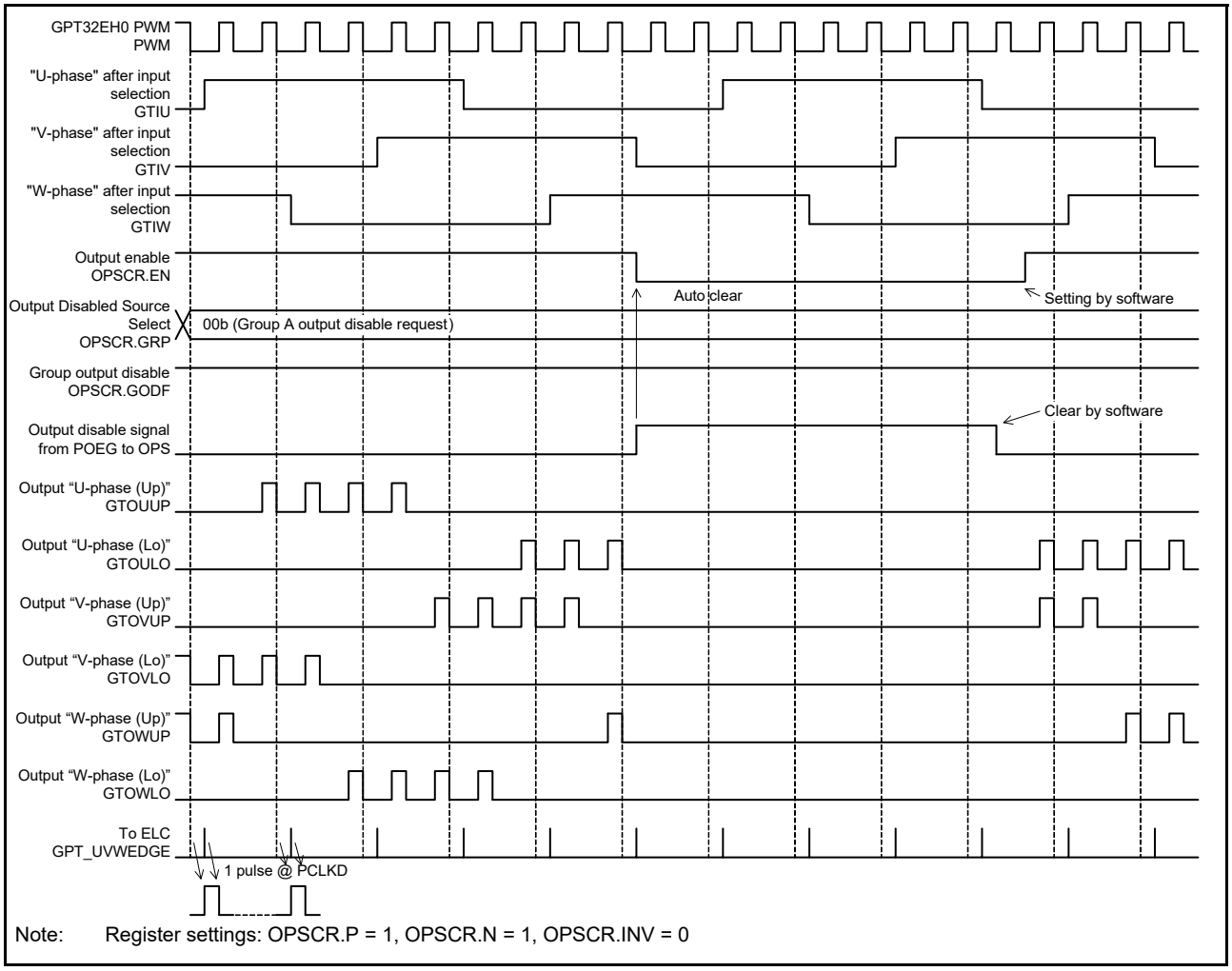


Figure 22.84 Example of group output disable control operation

22.3.11.1 Input selection and synchronization of external input signal

In the GPT_OPS control flow conceptual diagram shown in Figure 22.81, (1) is a selection of input phase from the software settings and external input by the OPSCR.FB bit.

When OPSCR.FB bit is 0, select the external input. Enable the input signal after synchronization with the GPT core clock (PCLKD). After carrying out noise filtering (optional), set the external input to the input phase of PWM (PWM of GPT32EH0.GTIOCA) using falling edge sampling with OPSCR.ALIGN bit set to 1.

When OPSCR.FB bit is 1, select the software setting (OPSCR.UF, VF, WF) with the value of the input phase of PWM (PWM of GPT32EH0.GTIOCA) using falling edge sampling with OPSCR.ALIGN bit set to 1.

When OPSCR.ALIGN bit is 0, GPT_OPS operates with the input phase of PCLKD synchronization with either OPSCR.FB bit set to 0 or OPSCR.FB bit set to 1. However, in some situations, the PWM pulse width of the output U/V/W phases (PWM output mode) of switch timing (just before or just after) is shortened.

Table 22.18 shows the input selection process and setting of associated OPSCR bits.

Table 22.18 Input selection processing method

OPSCR register		Selection of input phase sampling method (U/V/W-phase)	Synchronization input/output selection process (GPT_OPS internal node name)
FB bit	ALIGN bit		
0	1	External Input at PWM Falling Edge Sampling (PCLKD synchronization + falling edge sample)	Input Phase Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	External Input at PCLKD Synchronization Output (PCLKD synchronization + through mode)	
1	1	Software Settings at PWM Falling Edge Sampling (OPSCR.UF, VF, WF of falling edge sample)	
	0	Software Setting Value Selection (= OPSCR.UF/VF/WF value) (= PCLKD synchronization)	

22.3.11.2 Input sampling

The OPSCR.U, V, W bits indicate the PCLKD sampling results of the input selected by the OPSCR.FB bit.

When OPSCR.FB bit is 0 and after synchronization with the GPT core clock (PCLKD) and noise filtering (optional), OPSCR.U, V, W bits indicate the sampling results of the external input. When OPSCR.FB bit is 1, OPSCR.U, V, W bits have the value (OPSCR.UF, VF, WF) of the software setting.

22.3.11.3 Input phase decode

In the GPT_OPS control flow conceptual diagram shown in Figure 22.81, (2) enables the 6-phase signals by decoding the input phase selected by the OPSCR.FB bit. The 6-phase enable signal is used for internal processing of GPT_OPS.

Table 22.19 shows the decode table of input phase.

Table 22.19 Decode table of input phase

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-phase	Input V-phase	Input W-phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

22.3.11.4 Output selection control

In the GPT_OPS control flow conceptual diagram in Figure 22.81, (3) represents the selection of the output waveform by setting the OPSCR register bit.

For output selection, the following bits are relevant:

- The OPSCR.EN bit controls whether to output the 6-phase output, or to stop
- The OPSCR.P and OPSCR.N bits can select from the level signal or PWM signal (chopper output) for the output phase
- The polarity of the output phase can be set to positive logic or negative logic by the OPSCR.INV bit.

Table 22.20 and Table 22.21 show the output selection control method using the OPSCR register bit.

Table 22.20 Output selection control method (positive phase)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.P bit	OPSCR.INV bit	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS => 0 output
1	0	0	Level signal (gtuup_en) (gtvup_en) (gtwup_en)	Level Output Mode (Positive phase) (Positive logic)
1	0	1	Level signal (~gtuup_en) (~gtvup_en) (~gtwup_en)	Level Output Mode (Positive phase) (Negative logic)
1	1	0	PWM signal (PWM & gtuup_en) (PWM & gtvup_en) (PWM & gtwup_en)	PWM Output Mode (Positive phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtuup_en)) (~(PWM & gtvup_en)) (~(PWM & gtwup_en))	PWM Output Mode (Positive phase) (Negative logic)

Table 22.21 Output selection control method (negative phase) (1 of 2)

Enable-phase output control	Negative-phase output (N) control	Invert-phase output control	Output port name (negative phase = Lo) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.N bit	OPSCR.INV bit	GTOULO GTOVLO GTOWLO	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output
1	0	0	Level signal (gtulo_en) (gtvlo_en) (gtwlo_en)	Level Output Mode (Negative phase) (Positive logic)
1	0	1	Level signal (~gtulo_en) (~gtvlo_en) (~gtwlo_en)	Level Output Mode (Negative phase) (Negative logic)

Table 22.21 Output selection control method (negative phase) (2 of 2)

Enable-phase output control	Negative-phase output (N) control	Invert-phase output control	Output port name (negative phase = Lo) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.N bit	OPSCR.INV bit	GTOULO GTOVLO GTOWLO	Mode
1	1	0	PWM signal (PWM & gtulo_en) (PWM & gtvlo_en) (PWM & gtwlo_en)	PWM Output Mode (Negative phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtulo_en)) (~(PWM & gtvlo_en)) (~(PWM & gtwlo_en))	PWM Output Mode (Negative phase) (Negative logic)

22.3.11.5 Output selection control (group output disable function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP bit is high (output disable request), the GPT_OPS output pins change to Hi-Z asynchronously and the OPSCR.EN bit is set to 0 by the output disable request signal synchronized with PCLKD. For the return, set the OPSCR.EN bit to 1 after clearing the output disable request with software.

The timing of OPSCR.EN bit cleared to 0 is 3 PCLKD cycles after generating the output disable request. To perform output disable control reliably, allow at least 4 PCLKD cycles after generating the output disable request (by clearing the output disable request flag in POEG) until the output disable request is terminated. For an example of the operation of group output disable control, see Figure 22.84.

22.3.11.6 Event Link Controller (ELC) output

In the GPT_OPS control flow conceptual diagram shown in Figure 22.81, (5) outputs the Hall sensor input signal edge to the ELC.

The Hall sensor input edge signal is the logical OR of the rising and falling edge signals of each U-phase/V-phase/W-phase input sampled at PCLKD. That is, if the high period of each of the U-phase/V-phase/W-phase input is short in duration, the Hall sensor edge input signal is not output at that time.

When OPSCR.FB bit is 0, the Hall sensor input edge signal is the logical OR of the edge signals of the external input phase sampled at PCLKD.

When OPSCR.FB bit is 1, the Hall sensor input edge signal is the logical OR of the edge of the software setting (OPSCR.UF, VF, WF) sampled at PCLKD.

See Figure 22.82 to Figure 22.84 for examples of the output signal to the ELC.

22.3.11.7 GPT_OPS start operation setting flow

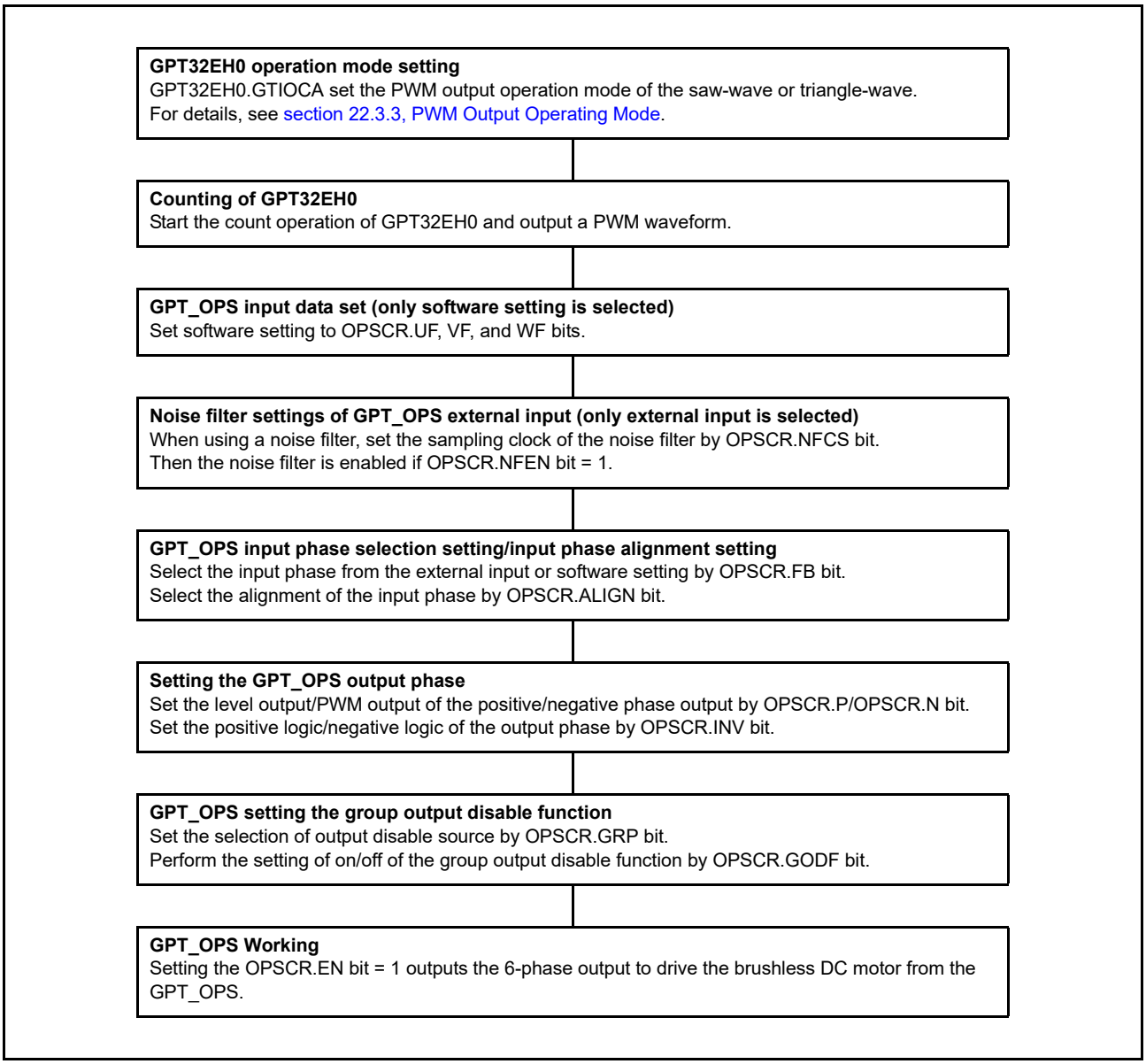


Figure 22.85 Example setting of GPT_OPS start operation

22.4 Interrupt Sources

The GPT provides the following interrupt sources:

- GTCCR input capture/compare match
- GTADTR compare match
- GTCNT counter overflow (GTPR compare match)/underflow.

Each interrupt source has its own status flag. When an interrupt source signal is generated, the associated status flag in GTST is set to 1. The associated status flag in GTST can be cleared by writing 0. If flag set and flag clear occur at the same time, flag clear takes priority over flag set. These flags are automatically updated by the internal state.

Table 22.22 lists the GPT interrupt sources.

Table 22.22 Interrupt sources (1 of 4)

Channel	Name	Interrupt source	Interrupt flag	DMAC/DTC activation
0	GPT0_CCMPA	GPT32EH0.GTCCRA input capture/compare match	TCFA	Possible
	GPT0_CCMPB	GPT32EH0.GTCCRB input capture/compare match	TCFB	Possible
	GPT0_CMPC	GPT32EH0.GTCCRC compare match	TCFC	Possible
	GPT0_CMPD	GPT32EH0.GTCCRD compare match	TCFD	Possible
	GPT0_CMPE	GPT32EH0.GTCCRE compare match	TCFE	Possible
	GPT0_CMPF	GPT32EH0.GTCCRF compare match	TCFF	Possible
	GPT0_ADTRGA	GPT32EH0.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT0_ADTRGB	GPT32EH0.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT0_OVF	GPT32EH0.GTCNT overflow (GPT32EH0.GTPR compare match)	TCFPO	Possible
	GPT0_UDF	GPT32EH0.GTCNT underflow	TCFPU	Possible
1	GPT1_CCMPA	GPT32EH1.GTCCRA input capture/compare match	TCFA	Possible
	GPT1_CCMPB	GPT32EH1.GTCCRB input capture/compare match	TCFB	Possible
	GPT1_CMPC	GPT32EH1.GTCCRC compare match	TCFC	Possible
	GPT1_CMPD	GPT32EH1.GTCCRD compare match	TCFD	Possible
	GPT1_CMPE	GPT32EH1.GTCCRE compare match	TCFE	Possible
	GPT1_CMPF	GPT32EH1.GTCCRF compare match	TCFF	Possible
	GPT1_ADTRGA	GPT32EH1.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT1_ADTRGB	GPT32EH1.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT1_OVF	GPT32EH1.GTCNT overflow (GPT32EH1.GTPR compare match)	TCFPO	Possible
	GPT1_UDF	GPT32EH1.GTCNT underflow	TCFPU	Possible
2	GPT2_CCMPA	GPT32EH2.GTCCRA input capture/compare match	TCFA	Possible
	GPT2_CCMPB	GPT32EH2.GTCCRB input capture/compare match	TCFB	Possible
	GPT2_CMPC	GPT32EH2.GTCCRC compare match	TCFC	Possible
	GPT2_CMPD	GPT32EH2.GTCCRD compare match	TCFD	Possible
	GPT2_CMPE	GPT32EH2.GTCCRE compare match	TCFE	Possible
	GPT2_CMPF	GPT32EH2.GTCCRF compare match	TCFF	Possible
	GPT2_ADTRGA	GPT32EH2.GTCCRE compare match	ADTRAUF ADRTADF	Possible
	GPT2_ADTRGB	GPT32EH2.GTCCRF compare match	ADTRBUF ADRTBDF	Possible
	GPT2_OVF	GPT32EH2.GTCNT overflow (GPT32EH2.GTPR compare match)	TCFPO	Possible
	GPT2_UDF	GPT32EH2.GTCNT underflow	TCFPU	Possible

Table 22.22 Interrupt sources (2 of 4)

Channel	Name	Interrupt source	Interrupt flag	DMAC/DTC activation
3	GPT3_CCMPA	GPT32EH3.GTCCRA input capture/compare match	TCFA	Possible
	GPT3_CCMPB	GPT32EH3.GTCCRB input capture/compare match	TCFB	Possible
	GPT3_CMPC	GPT32EH3.GTCCRC compare match	TCFC	Possible
	GPT3_CMPD	GPT32EH3.GTCCRD compare match	TCFD	Possible
	GPT3_CMPE	GPT32EH3.GTCCRE compare match	TCFE	Possible
	GPT3_CMPF	GPT32EH3.GTCCRF compare match	TCFF	Possible
	GPT3_ADTRGA	GPT32EH3.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT3_ADTRGB	GPT32EH3.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT3_OVF	GPT32EH3.GTCNT overflow (GPT32EH3.GTPR compare match)	TCFPO	Possible
	GPT3_UDF	GPT32EH3.GTCNT underflow	TCFPU	Possible
4	GPT4_CCMPA	GPT32E4.GTCCRA input capture/compare match	TCFA	Possible
	GPT4_CCMPB	GPT32E4.GTCCRB input capture/compare match	TCFB	Possible
	GPT4_CMPC	GPT32E4.GTCCRC compare match	TCFC	Possible
	GPT4_CMPD	GPT32E4.GTCCRD compare match	TCFD	Possible
	GPT4_CMPE	GPT32E4.GTCCRE compare match	TCFE	Possible
	GPT4_CMPF	GPT32E4.GTCCRF compare match	TCFF	Possible
	GPT4_ADTRGA	GPT32E4.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT4_ADTRGB	GPT32E4.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT4_OVF	GPT32E4.GTCNT overflow (GPT32E4.GTPR compare match)	TCFPO	Possible
	GPT4_UDF	GPT32E4.GTCNT underflow	TCFPU	Possible
5	GPT5_CCMPA	GPT32E5.GTCCRA input capture/compare match	TCFA	Possible
	GPT5_CCMPB	GPT32E5.GTCCRB input capture/compare match	TCFB	Possible
	GPT5_CMPC	GPT32E5.GTCCRC compare match	TCFC	Possible
	GPT5_CMPD	GPT32E5.GTCCRD compare match	TCFD	Possible
	GPT5_CMPE	GPT32E5.GTCCRE compare match	TCFE	Possible
	GPT5_CMPF	GPT32E5.GTCCRF compare match	TCFF	Possible
	GPT5_ADTRGA	GPT32E5.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT5_ADTRGB	GPT32E5.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT5_OVF	GPT32E5.GTCNT overflow (GPT32E5.GTPR compare match)	TCFPO	Possible
	GPT5_UDF	GPT32E5.GTCNT underflow	TCFPU	Possible

Table 22.22 Interrupt sources (3 of 4)

Channel	Name	Interrupt source	Interrupt flag	DMAC/DTC activation
6	GPT6_CCMPA	GPT32E6.GTCCRA input capture/compare match	TCFA	Possible
	GPT6_CCMPB	GPT32E6.GTCCRB input capture/compare match	TCFB	Possible
	GPT6_CMPC	GPT32E6.GTCCRC compare match	TCFC	Possible
	GPT6_CMPD	GPT32E6.GTCCRD compare match	TCFD	Possible
	GPT6_CMPE	GPT32E6.GTCCRE compare match	TCFE	Possible
	GPT6_CMPF	GPT32E6.GTCCRF compare match	TCFF	Possible
	GPT6_ADTRGA	GPT32E6.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT6_ADTRGB	GPT32E6.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT6_OVF	GPT32E6.GTCNT overflow (GPT32E6.GTPR compare match)	TCFPO	Possible
	GPT6_UDF	GPT32E6.GTCNT underflow	TCFPU	Possible
7	GPT7_CCMPA	GPT32E7.GTCCRA input capture/compare match	TCFA	Possible
	GPT7_CCMPB	GPT32E7.GTCCRB input capture/compare match	TCFB	Possible
	GPT7_CMPC	GPT32E7.GTCCRC compare match	TCFC	Possible
	GPT7_CMPD	GPT32E7.GTCCRD compare match	TCFD	Possible
	GPT7_CMPE	GPT32E7.GTCCRE compare match	TCFE	Possible
	GPT7_CMPF	GPT32E7.GTCCRF compare match	TCFF	Possible
	GPT7_ADTRGA	GPT32E7.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT7_ADTRGB	GPT32E7.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT7_OVF	GPT32E7.GTCNT overflow (GPT32E7.GTPR compare match)	TCFPO	Possible
	GPT7_UDF	GPT32E7.GTCNT underflow	TCFPU	Possible
8	GPT8_CCMPA	GPT328.GTCCRA input capture/compare match	TCFA	Possible
	GPT8_CCMPB	GPT328.GTCCRB input capture/compare match	TCFB	Possible
	GPT8_CMPC	GPT328.GTCCRC compare match	TCFC	Possible
	GPT8_CMPD	GPT328.GTCCRD compare match	TCFD	Possible
	GPT8_CMPE	GPT328.GTCCRE compare match	TCFE	Possible
	GPT8_CMPF	GPT328.GTCCRF compare match	TCFF	Possible
	GPT8_OVF	GPT328.GTCNT overflow (GPT328.GTPR compare match)	TCFPO	Possible
	GPT8_UDF	GPT328.GTCNT underflow	TCFPU	Possible
9	GPT9_CCMPA	GPT329.GTCCRA input capture/compare match	TCFA	Possible
	GPT9_CCMPB	GPT329.GTCCRB input capture/compare match	TCFB	Possible
	GPT9_CMPC	GPT329.GTCCRC compare match	TCFC	Possible
	GPT9_CMPD	GPT329.GTCCRD compare match	TCFD	Possible
	GPT9_CMPE	GPT329.GTCCRE compare match	TCFE	Possible
	GPT9_CMPF	GPT329.GTCCRF compare match	TCFF	Possible
	GPT9_OVF	GPT329.GTCNT overflow (GPT329.GTPR compare match)	TCFPO	Possible
	GPT9_UDF	GPT329.GTCNT underflow	TCFPU	Possible

Table 22.22 Interrupt sources (4 of 4)

Channel	Name	Interrupt source	Interrupt flag	DMAC/DTC activation
10	GPT10_CCMPA	GPT3210.GTCCRA input capture/compare match	TCFA	Possible
	GPT10_CCMPB	GPT3210.GTCCRB input capture/compare match	TCFB	Possible
	GPT10_CMPC	GPT3210.GTCCRC compare match	TCFC	Possible
	GPT10_CMPD	GPT3210.GTCCRD compare match	TCFD	Possible
	GPT10_CMPE	GPT3210.GTCCRE compare match	TCFE	Possible
	GPT10_CMPF	GPT3210.GTCCRF compare match	TCFF	Possible
	GPT10_OVF	GPT3210.GTCNT overflow (GPT3210.GTPR compare match)	TCFPO	Possible
	GPT10_UDF	GPT3210.GTCNT underflow	TCFPU	Possible
11	GPT11_CCMPA	GPT3211.GTCCRA input capture/compare match	TCFA	Possible
	GPT11_CCMPB	GPT3211.GTCCRB input capture/compare match	TCFB	Possible
	GPT11_CMPC	GPT3211.GTCCRC compare match	TCFC	Possible
	GPT11_CMPD	GPT3211.GTCCRD compare match	TCFD	Possible
	GPT11_CMPE	GPT3211.GTCCRE compare match	TCFE	Possible
	GPT11_CMPF	GPT3211.GTCCRF compare match	TCFF	Possible
	GPT11_OVF	GPT3211.GTCNT overflow (GPT3211.GTPR compare match)	TCFPO	Possible
	GPT11_UDF	GPT3211.GTCNT underflow	TCFPU	Possible
12	GPT12_CCMPA	GPT3212.GTCCRA input capture/compare match	TCFA	Possible
	GPT12_CCMPB	GPT3212.GTCCRB input capture/compare match	TCFB	Possible
	GPT12_CMPC	GPT3212.GTCCRC compare match	TCFC	Possible
	GPT12_CMPD	GPT3212.GTCCRD compare match	TCFD	Possible
	GPT12_CMPE	GPT3212.GTCCRE compare match	TCFE	Possible
	GPT12_CMPF	GPT3212.GTCCRF compare match	TCFF	Possible
	GPT12_OVF	GPT3212.GTCNT overflow (GPT3212.GTPR compare match)	TCFPO	Possible
	GPT12_UDF	GPT3212.GTCNT underflow	TCFPU	Possible

(1) GPTn_ADTRGA interrupt (n = 0 to 7)

When the GTCNT counter value matches with the GTADTRA register, an interrupt request is generated under the following conditions:

- In up-counting, the interrupt enable bit (ADTRAUEN) in the GTINTAD register is 1
- In down-counting, the interrupt enable bit (ADTRADEN) in the GTINTAD register is 1.

In event count operation, this interrupt request is not generated.

(2) GPTn_ADTRGB interrupt (n = 0 to 7)

When the GTCNT counter value matches with the GTADTRB register, an interrupt request is generated under the following conditions:

- In up-counting, the interrupt enable bit (ADTRBUEN) in the GTINTAD register is 1
- In down-counting, the interrupt enable bit (ADTRBDEN) in the GTINTAD register is 1.

In event count operation, this interrupt request is not generated.

(3) GPTn_CCMPA interrupt (n = 0 to 12)

An interrupt request is generated under the following conditions:

- When the GTCCRA register functions as a compare match register, the GTCNT counter value matches with the GTCCRA register.
- When the GTCCRA register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRA register.

(4) GPTn_CCMPB interrupt (n = 0 to 12)

An interrupt request is generated under the following conditions:

- When the GTCCRB register functions as a compare match register, the GTCNT counter value matches with the GTCCRB register
- When the GTCCRB register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRB register.

(5) GPTn_CMPC interrupt (n = 0 to 12)

An interrupt request is generated under the following condition:

- When the GTCCRC register functions as a compare match register, the GTCNT counter value matches with the GTCCRC register.

A compare match is not performed and an interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC register).

(6) GPTn_CMPD interrupt (n = 0 to 12)

An interrupt request is generated under the following condition:

- When the GTCCRD register functions as a compare match register, the GTCNT counter value matches with the GTCCRD register.

A compare match is not performed and an interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD register).

(7) GPTn_CMPE interrupt (n = 0 to 12)

An interrupt request is generated under the following condition.

- When the GTCCRE register functions as a compare match register, the GTCNT counter value matches with the GTCCRE register.

A compare match is not performed and an interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRE register).

(8) GPTn_CMPF interrupt (n = 0 to 12)

An interrupt request is generated under the following condition:

- When the GTCCRF register functions as a compare match register, the GTCNT counter value matches with the GTCCRF register.

A compare match is not performed and an interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (buffer operation with the GTCCRF register).

(9) GPTn_OVF interrupt (n = 0 to 12)

An interrupt request is generated under the following conditions:

- In saw-wave mode, interrupt requests are enabled at overflows (when the GTCNT counter value changes from GTPR to 0 during up-counting)
- In triangle-wave mode, interrupt requests are enabled at crests (GTCNT changes from GTPR to GTPR - 1)
- In counting by hardware sources, overflow (GTCNT changes from GTPR to 0 in up count) has occurred.

(10) GPTn_UDF interrupt (n = 0 to 12)

An interrupt request is generated under the following conditions:

- In saw-wave mode, interrupt requests are enabled at underflows (when the GTCNT counter value changes from 0 to GTPR during down-counting)
- In triangle-wave mode, interrupt requests are enabled at troughs (GTCNT changes from 0 to 1)
- In counting by hardware sources, underflow (GTCNT changes from 0 to GTPR in down count) has occurred.

Table 22.23 Interrupt signals, interrupt permission bits, and interrupt status flags

Interrupt signal	Interrupt permission bit	Interrupt status flag
GPTn_UDF	- *1	GTST[7] (TCFPU)
GPTn_OVF		GTST[6] (TCFPO)
GPTn_ADTRGB	GTINTAD[19] (ADTRBDEN) GTINTAD[18] (ADTRBUEN)	GTST[19] (ADTRBDF) GTST[18] (ADTRBUF)
GPTn_ADTRGA	GTINTAD[17] (ADTRADEN) GTINTAD[16] (ADTRAUEN)	GTST[17] (ADTRADF) GTST[16] (ADTRAUF)
GPTn_CMPF	- *1	GTST[5] (TCFF)
GPTn_CMPE		GTST[4] (TCFE)
GPTn_CMPD		GTST[3] (TCFD)
GPTn_CMPC		GTST[2] (TCFC)
GPTn_CCMPB		GTST[1] (TCFB)
GPTn_CCMPA		GTST[0] (TCFA)

Note 1. Interrupt is always permitted.

22.4.1 DMAC/DTC Activation

The DMAC and DTC can be activated by the interrupt in each channel. For details, see section 13, Interrupt Controller Unit (ICU), and section 17, Data Transfer Controller (DTC).

22.4.2 Interrupt and A/D Conversion Request Skipping Function

By setting the GTITC register, the GTCNT counter overflow (GTPR compare match) interrupt (GPTn_OVF) and underflow interrupt (GPTn_UDF) can be skipped. Other interrupts and A/D converter start request signals can be skipped in coordination with the GPTn_OVF/GPTn_UDF skipping function.

The interrupt request skipping function only depends on the setting of GTITC register and is independent of the setting of interrupt permission bits in the GTINTAD register.

When both troughs and crests are counted and skipped in triangle-wave mode, if the number of times for skipping is odd, GPTn_OVF/GPTn_UDF interrupt requests cannot be generated at troughs only or at crests only depending on the skipping counter start timing. To count both troughs and crests and generate the GPTn_OVF/GPTn_UDF interrupts at troughs only or crests only in triangle-wave mode, you must set an even number of skips.

Similarly, in saw-wave mode, when both overflows and underflows are counted and skipped with the count direction changed, GPTn_OVF interrupt requests cannot be generated on either overflows or underflows only. To count both overflows and underflows with the count direction changed and generate the GPTn_OVF/GPTn_UDF interrupts on either overflows or underflows only in saw wave mode, you must first check the skipping state.

Before changing the skipping count, you must release the skipping count setting (GTITC.IVTC[1:0] bits = 00b).

Figure 22.86 to Figure 22.91 show examples of skipping function operation.

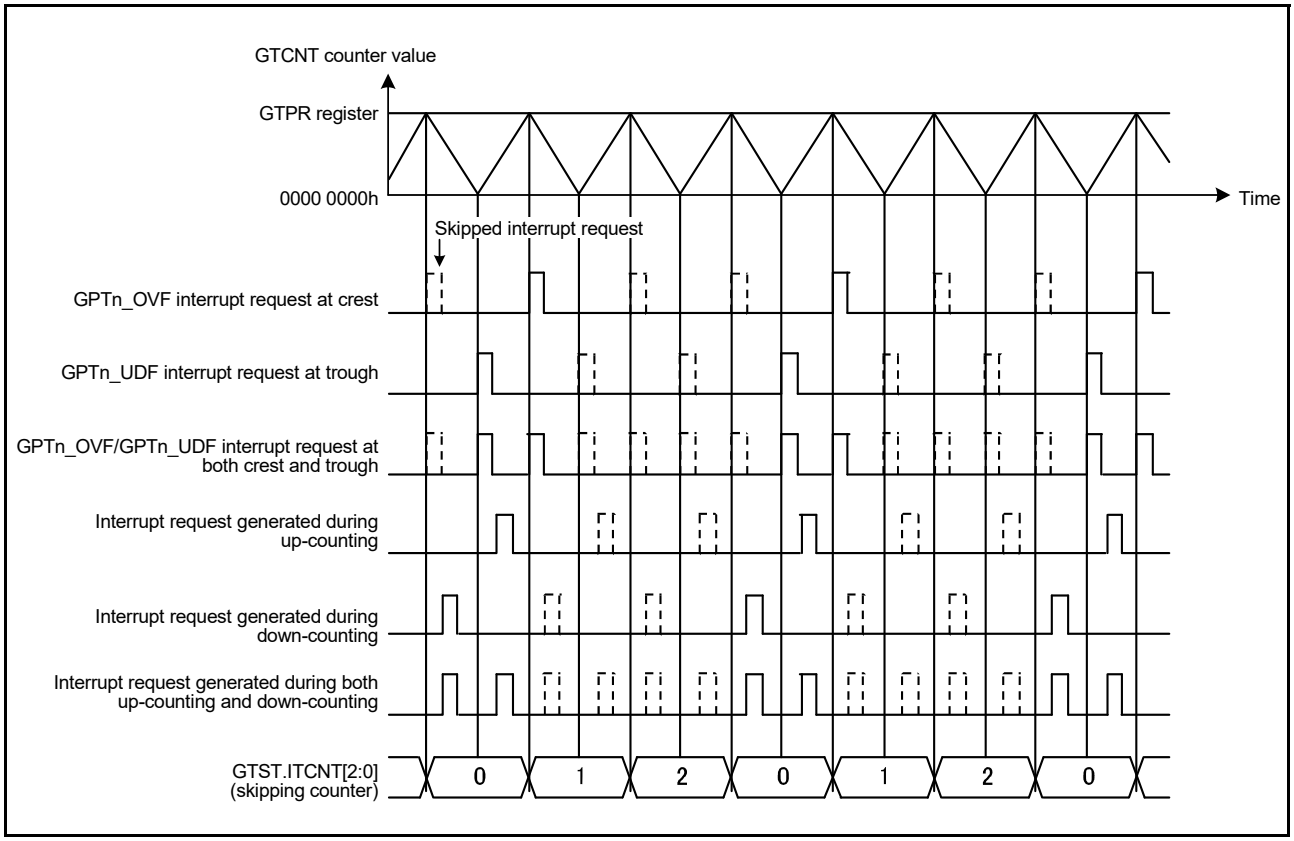


Figure 22.86 Example of interrupt skipping function operation with triangle waves, counting and skipping crests, and skipping count = 2

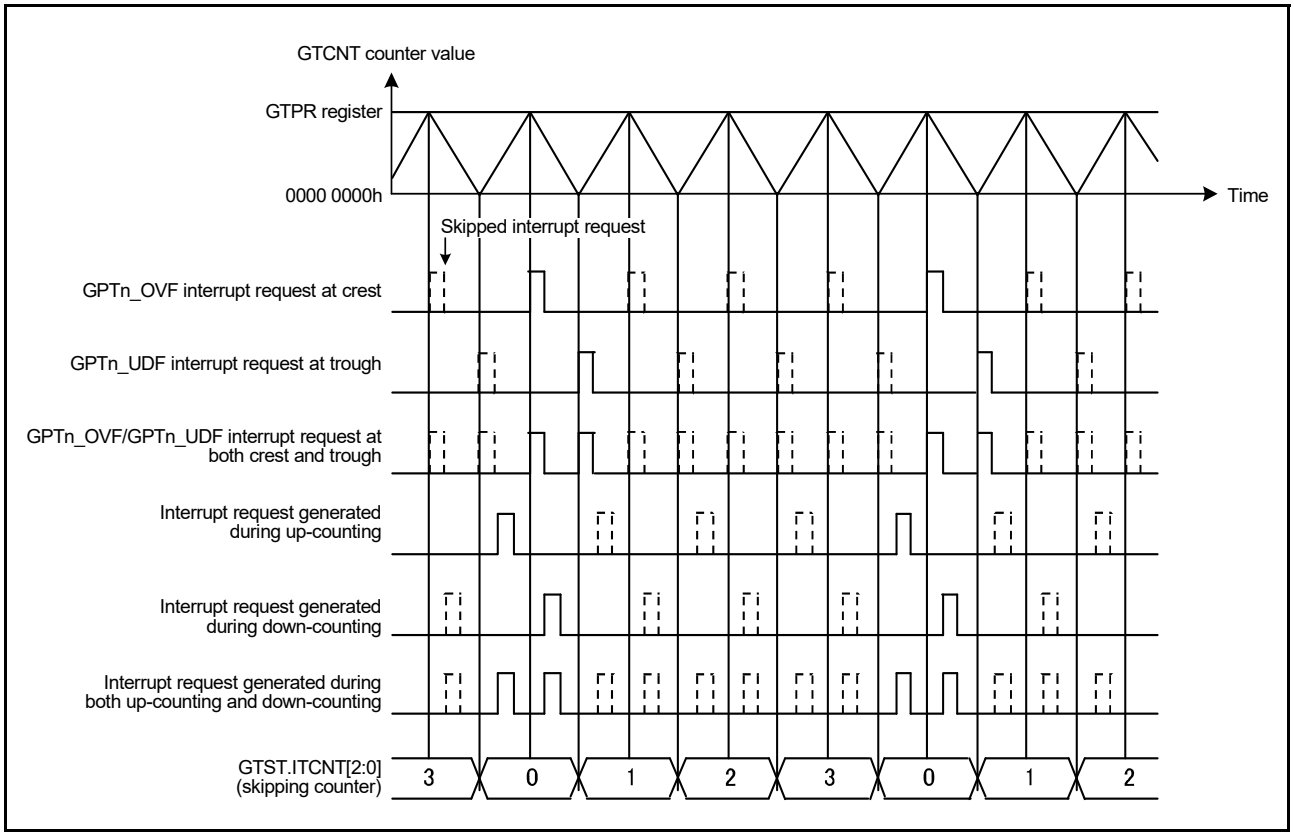


Figure 22.87 Example of interrupt skipping function operation with triangle waves, counting and skipping troughs, and skipping count = 3

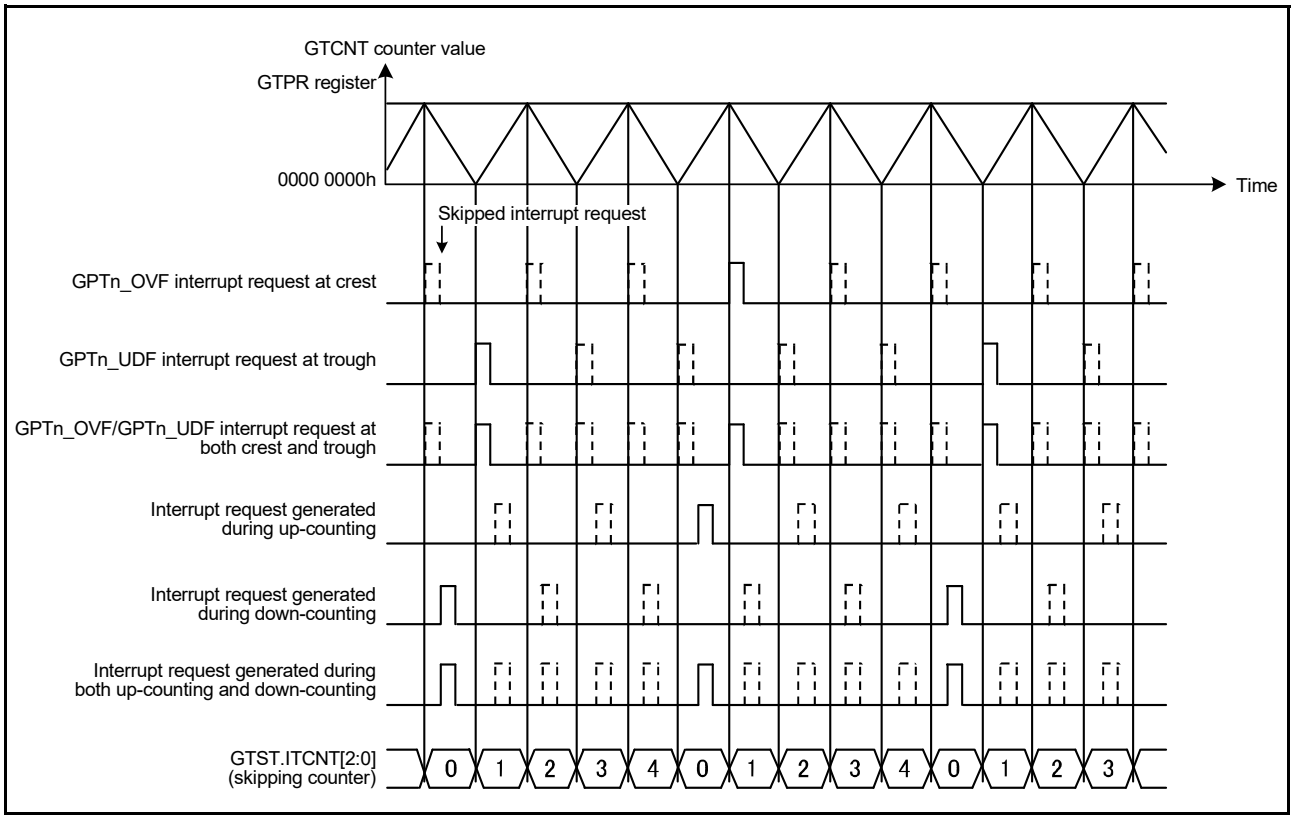


Figure 22.88 Example of interrupt skipping function operation with triangle waves, counting and skipping both troughs and crests, and skipping count = 4

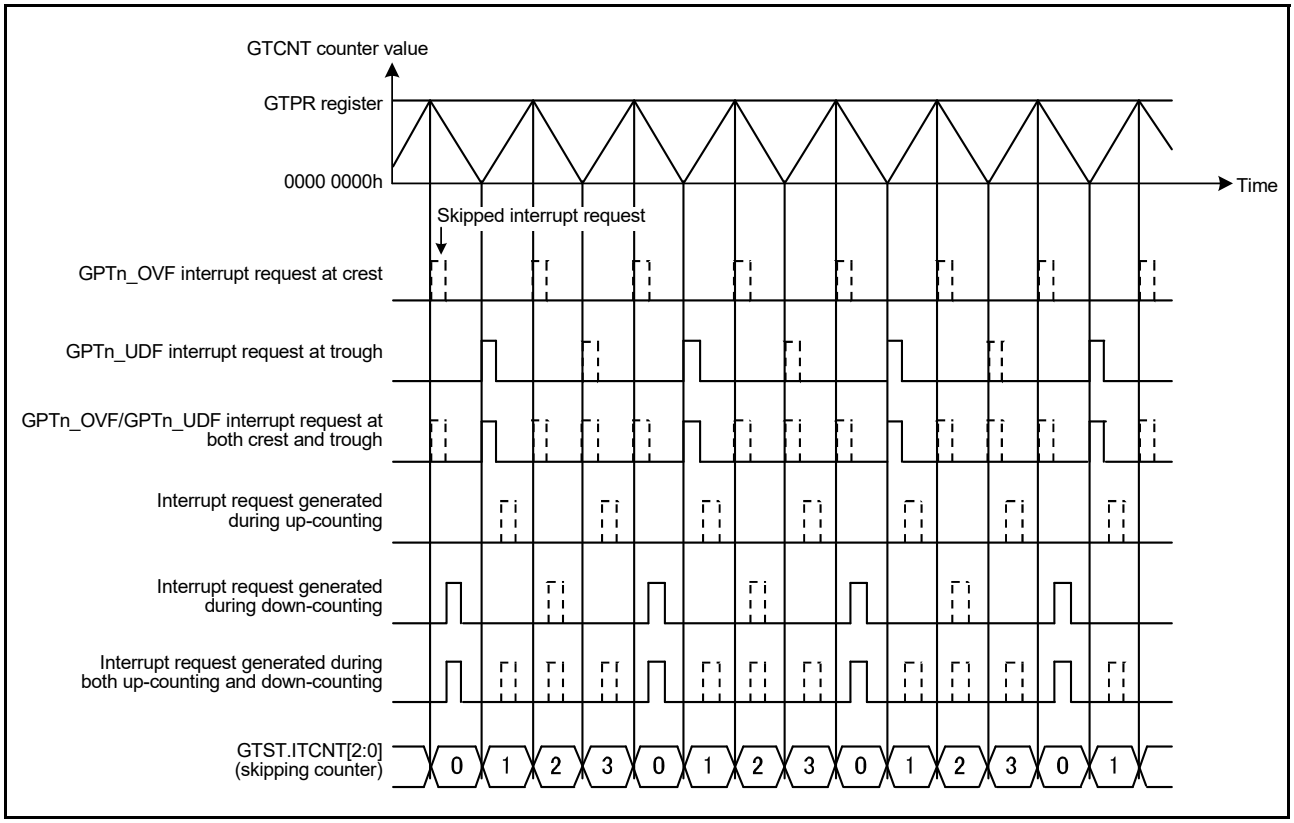


Figure 22.89 Example of interrupt skipping function operation with triangle waves, counting and skipping both troughs and crests, skipping count = 3, and skipping started at up-counting

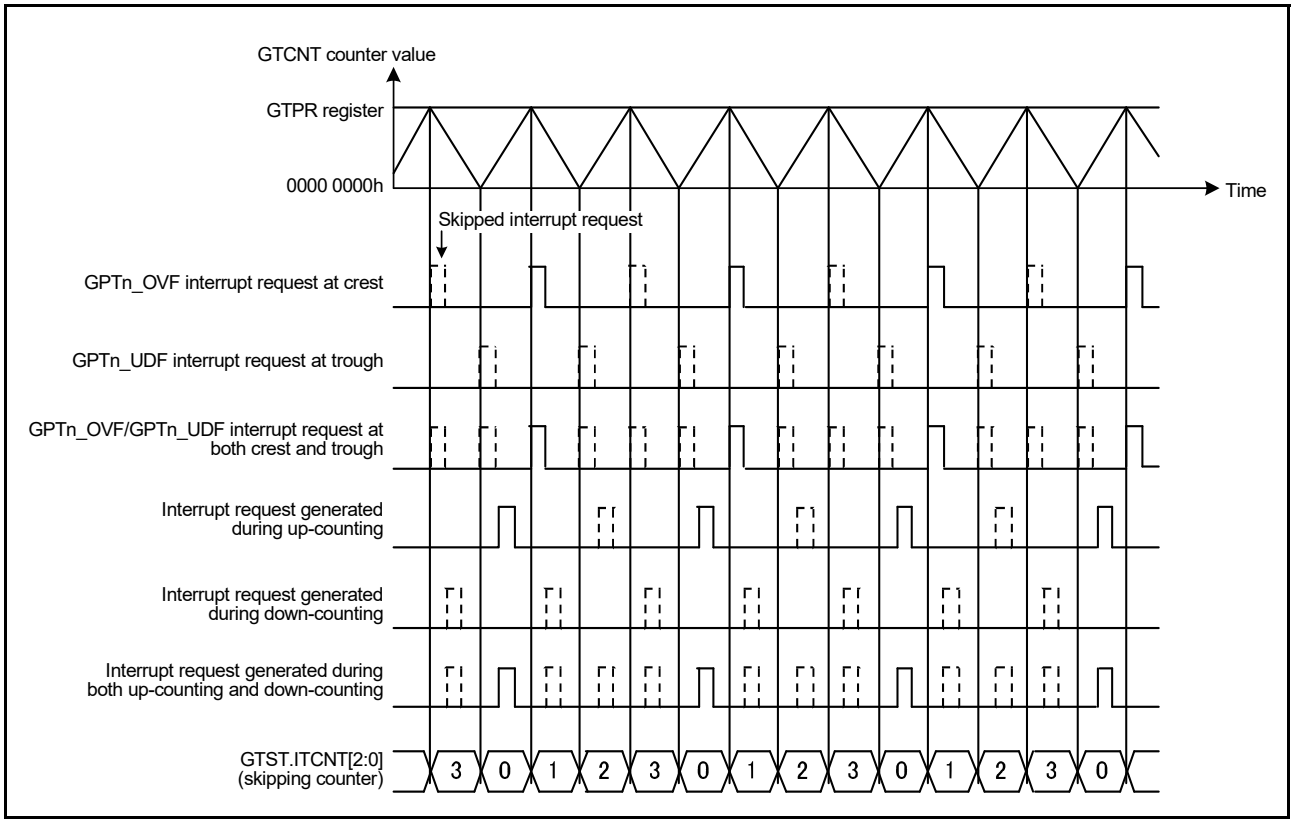


Figure 22.90 Example of interrupt skipping function operation with triangle waves, counting and skipping both troughs and crests, skipping count = 3, and skipping started at down-counting

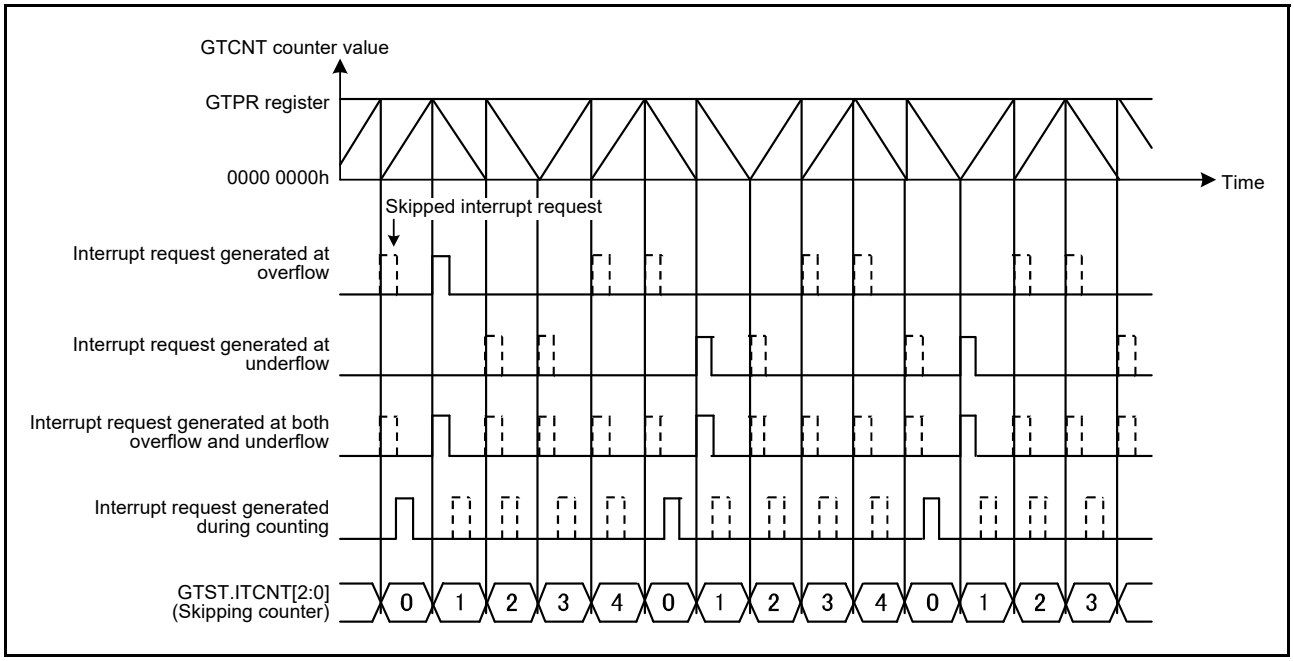


Figure 22.91 Example of interrupt skipping function operation with saw waves, operation with count direction changed, counting and skipping both overflows and underflows, and skipping count = 4

22.5 A/D Converter Start Request

An A/D converter start request can be issued at a compare match between the GTCNT counter and GTADTRA or GTADTRB, and up-counting only, down-counting only, or both up-counting and down-counting can be specified.

In event count operation performing, A/D converter start requests interrupt cannot be generated. An A/D converter start request does not direct output to the A/D converter module but results in output to ELC as event signals.

GTADTRA and GTADTRB each have two buffer registers. Buffer operation with GTADTRA combined with GTADTBRA and GTADTDBRA, and buffer operation with GTADTRB combined with GTADTBRB and GTADTDBRB can be performed.

Figure 22.92 shows an example of A/D converter start request operation, and Figure 22.93 shows an example setting for A/D converter start request operation.

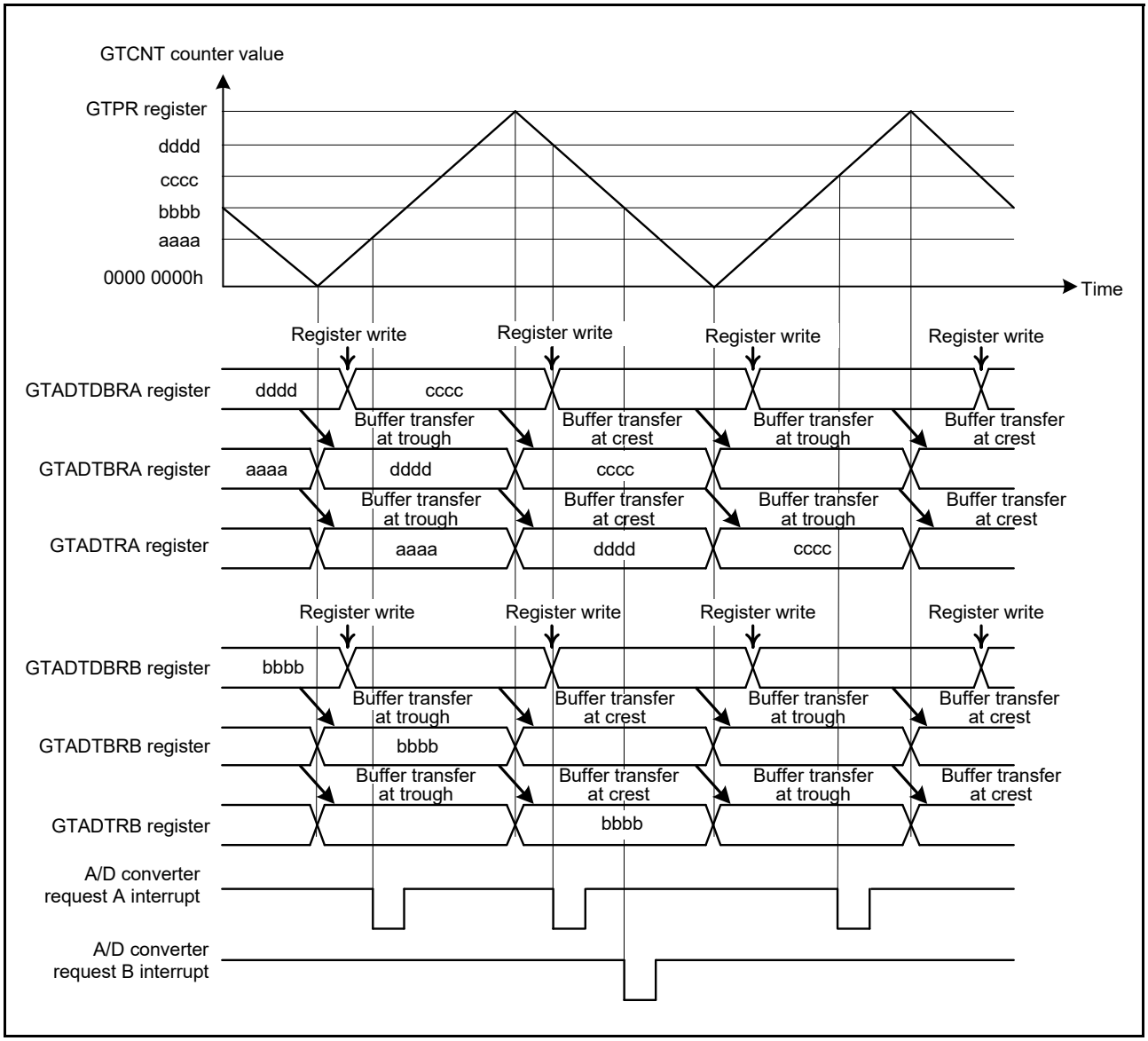


Figure 22.92 Example of A/D converter start request timing operation with triangle waves, double buffer operation, buffer transfer at both troughs and crests, A/D converter start request interrupt by GTADTRA at both up-counting and down-counting, and A/D converter start request interrupt by GTADTRB at down-counting

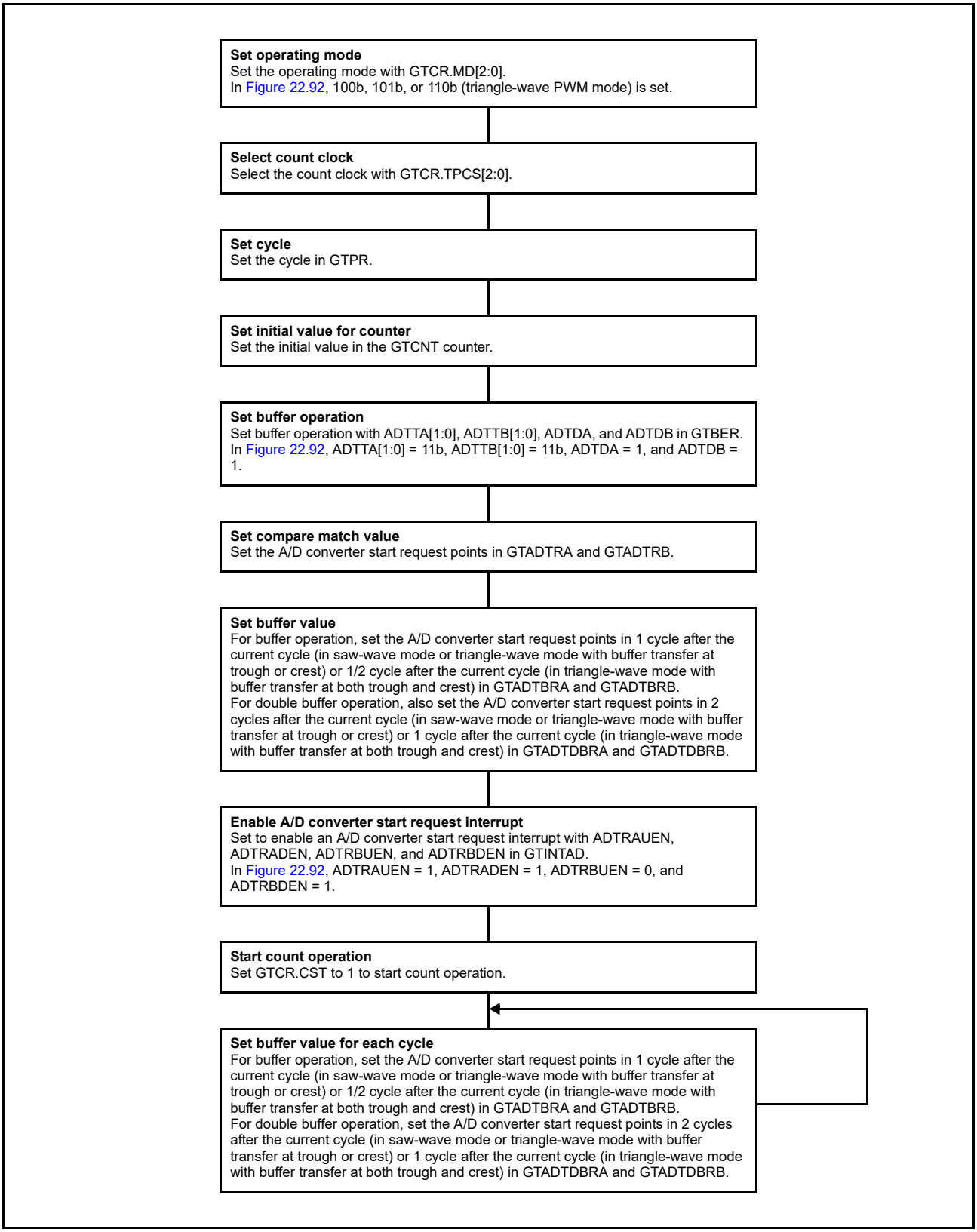


Figure 22.93 Example setting for A/D converter start request timing operation

22.6 Operations Linked by the ELC

22.6.1 Event Signal Output to the ELC

The GPT can perform operation linked with another module set in advance when its interrupt request signal is used as an event signal by the Event Link Controller (ELC).

A/D converter start requests can be enabled and disabled individually with each up-counting and down-counting for both interrupts and events output to ELC by enable bits of the interrupt request.

The GPT has the following ELC event signals:

- Generation of compare match A interrupt (GPTn_CCMPA (n = 0 to 12))
- Generation of compare match B interrupt (GPTn_CCMPB (n = 0 to 12))
- Generation of compare match C interrupt (GPTn_CMPC (n = 0 to 12))
- Generation of compare match D interrupt (GPTn_CMPD (n = 0 to 12))
- Generation of compare match E interrupt (GPTn_CMPE (n = 0 to 12))
- Generation of compare match F interrupt (GPTn_CMPF (n = 0 to 12))
- Generation of overflow interrupt (GPTn_OVF (n = 0 to 12))
- Generation of underflow interrupt (GPTn_UDF (n = 0 to 12))
- A/D converter start request A interrupt (GPTn_ADTRGA (n = 0 to 7))
- A/D converter start request B interrupt (GPTn_ADTRGB (n = 0 to 7)).

22.6.2 Event Signal Inputs from the ELC

The GPT can perform the following operations in response to a maximum of eight events from the ELC:

- Start counting, stop counting, clear counting
- Up-counting, down counting
- Input capture.

See section 22.3, Operation for detail on hardware resources.

22.7 Noise Filter Function

Each pin for use in input capture and Hall sensor input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses whose length is less than 3 sampling cycles.

The noise filter functionality includes enabling and disabling the noise filter for each pin and setting of the sampling clock for each channel.

Figure 22.94 shows the timing of noise filtering.

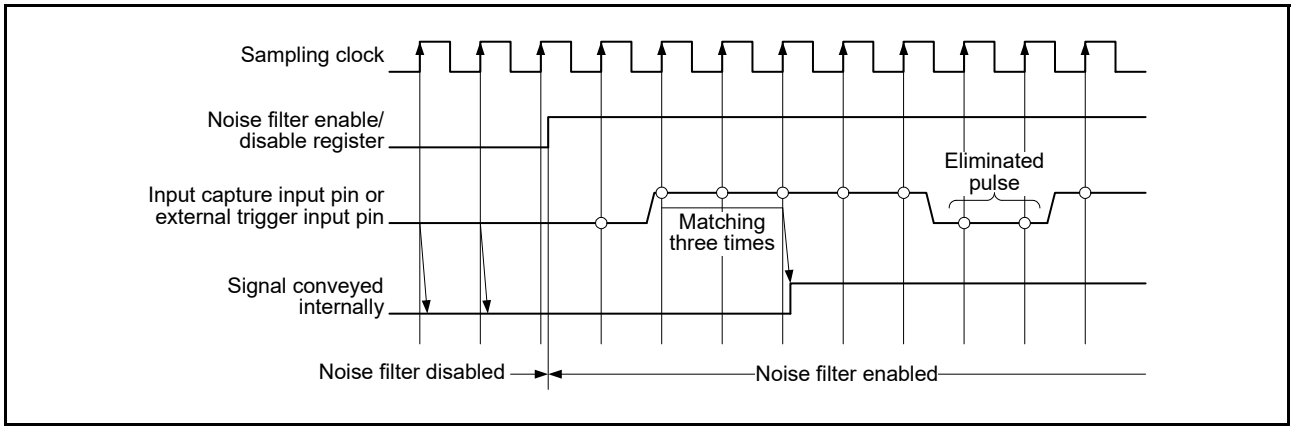


Figure 22.94 Timing of noise filtering

If noise filtering is enabled, the input capture operation or external trigger operation performs on the edges of the noise filtered signal after a delay of a sampling interval × 3 + PCLKD. This is caused by the noise filtering for the input capture input or external trigger operation.

22.8 Protection Function

22.8.1 Write-Protection for Registers

To prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WP. Write-protection can be set for the following registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD,GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR.

22.8.2 Disabling of Buffer Operation

If the timing of buffer register write is delayed relative to the timing for the buffer transfer, buffer operation can be suspended with the GTBER.BD bit setting. Specifically, buffer transfer can be temporarily disabled even when a buffer transfer condition is generated during a buffer register write. This can be done by setting the associated GTBER.BD bit to 1 (buffer operation disabled) before a buffer register write and clearing the bit to 0 (buffer operation enabled) after completion of writing to all the buffer registers.

Figure 22.95 shows an example of operation for disabling buffer operation.

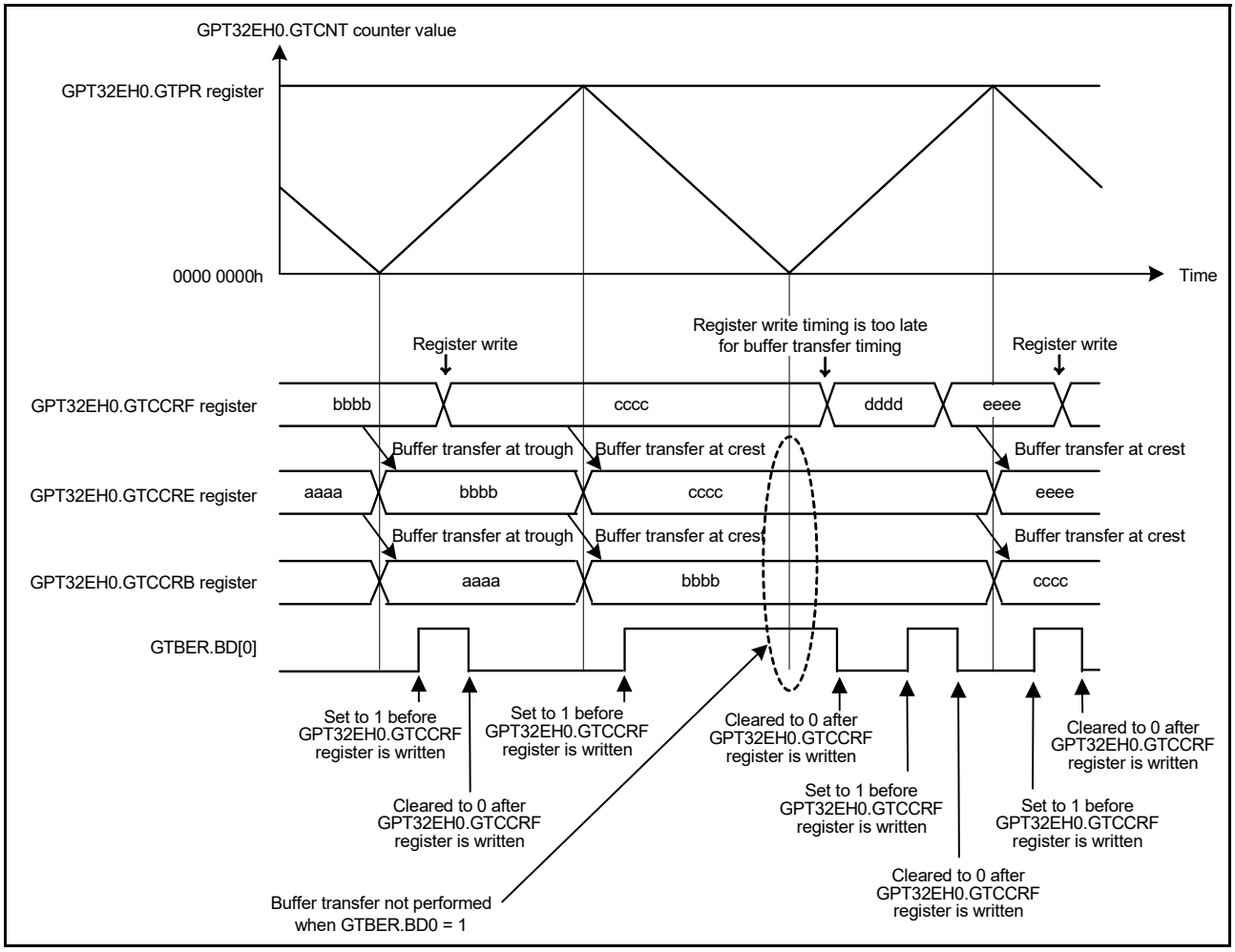


Figure 22.95 Example of operation for disabling buffer operation with triangle waves, double buffer operation, and buffer transfer at both troughs and crests

22.8.3 GTIOC Pin Output Negate Control

For protection from system failure, the output disable control that changes the GTIOC pin output value forcibly is provided for GTIOC pin output by the request of output disable from POEG.

When dead time error occurs or the GTIOCA pin output value is the same as the GTIOCB pin output value, output protection is required. The GPT detects this condition and generates output disable requests to POEG according to the settings in the output disable request permission bits, such as GTINTAD.GRPDTE, GTINTAD.GRPABH, and GTINTAD.GRPABL. After the POEG receives output disable requests from each channel and calculates external input using an OR operation, the POEG generates output disable requests to GPT.

One output disable signal (representing the shared output disable request signal of the GTIOCA pin and the GTIOCB pin) out of four output disable requests generated by the POEG is selected by setting GTINTAD.GRP[1:0]. The status of the selected disable output request is monitored by reading the GTST.ODF bit. The output level during output disable is based on the GTIOR.OADF[1:0] setting for the GTIOCA pin and the GTIOR.OBDF[1:0] setting for the GTIOCB pin.

The change to the output disable state is performed asynchronously by generating the output disable request from the POEG. The release of the output disable state is performed at end of cycle by terminating the output disable request. The timing of release of the output disable state is a minimum of 3 PCLKD cycles after terminating the output disable request. To perform output disable control reliably, allow at least 4 PCLKD cycles after generating the output disable request (by clearing the output disable request flag in POEG) until the output disable request is terminated.

When event count is performed or when the output disable state is to be released immediately without waiting for an end of cycle, GTIOR.OADF[1:0] must be set to 00b (for GTIOCA pin) or GTIOR.OBDF[1:0] must be set to 00b (for GTIOCB pin).

Figure 22.96 shows an example of the GTIOC pin output disable control operation.

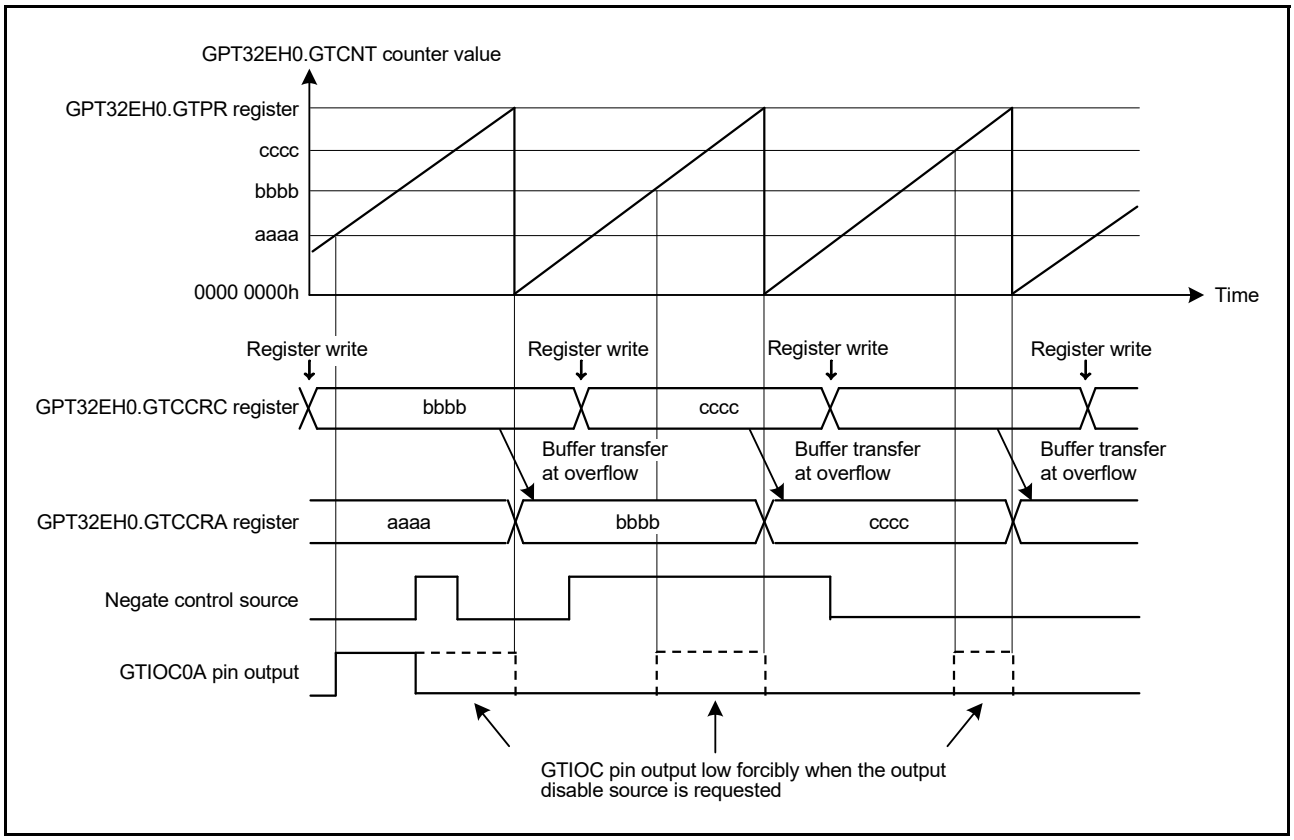


Figure 22.96 Example of GTIOC pin output disable control operation with saw-wave up-counting, buffer operation, active level 1, high output at GTCCRA compare match, low output at cycle end, and low output at output disable

22.8.4 Output Protection Function for GTIOC Pin Output

In preparation for incorrect settings of the GTCCRA register (settings outside the range of 0 < GTCCRA < GTPR), the output protection function for the GTIOC pin output (disabling function) is activated when the automatic dead time setting (GTDTCR.TDE = 1) is made in triangle-wave mode. The status of the output protection function can be read from GTSOS.SOS[1:0].

Figure 22.97 shows the state transition of the output protection function.

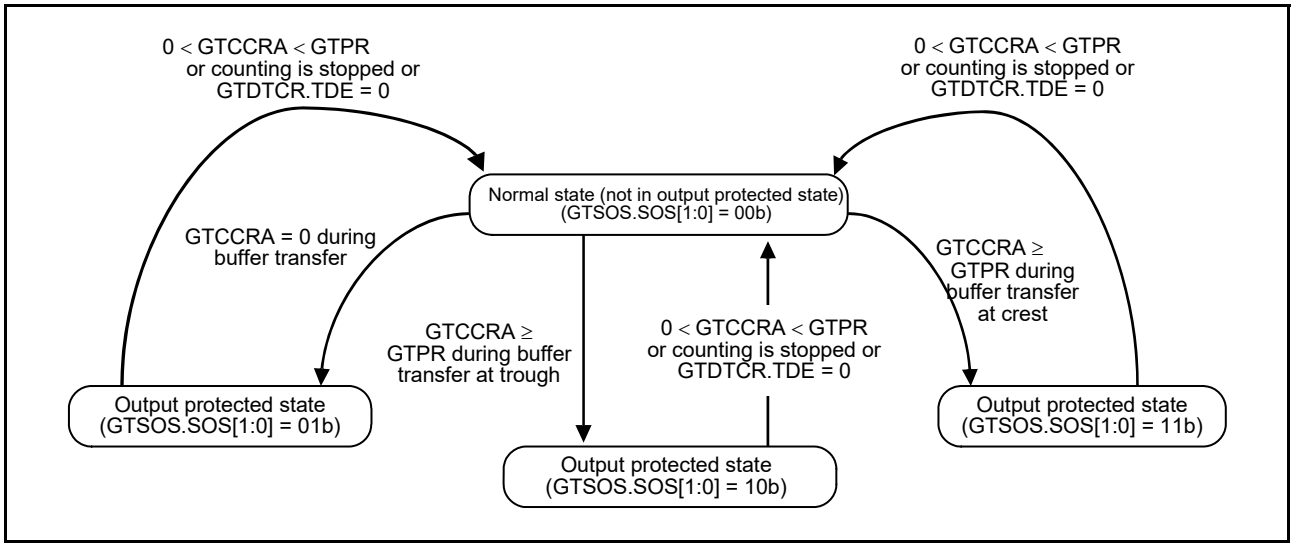
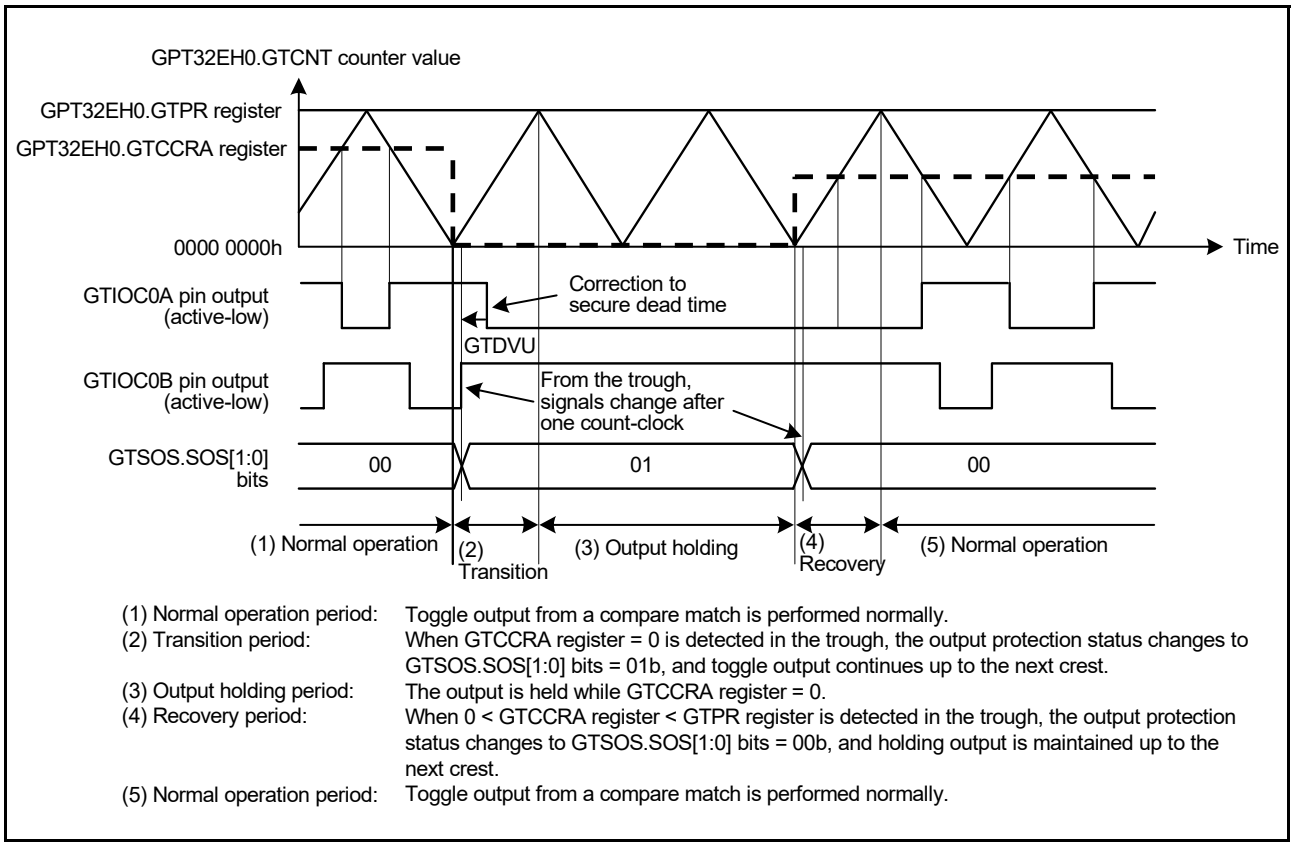


Figure 22.97 Output protection function

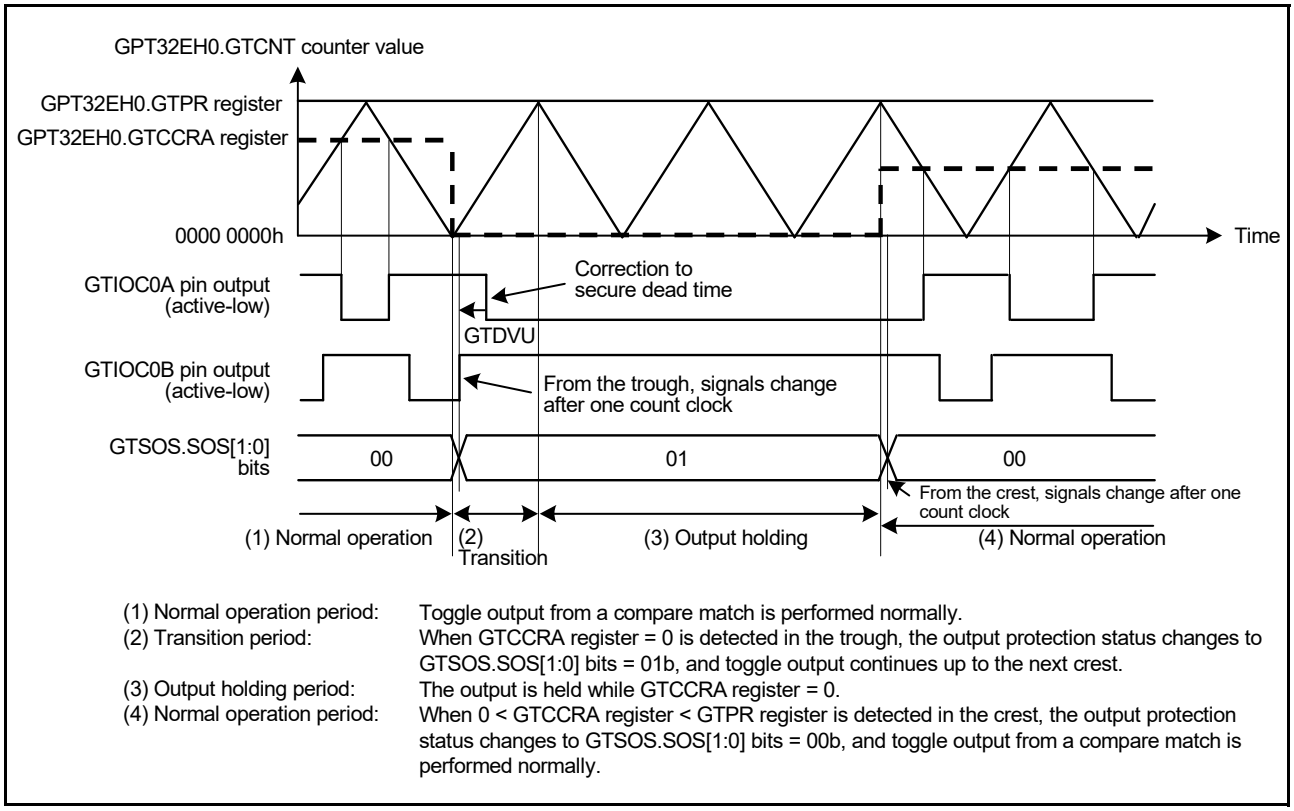
22.8.4.1 Output protection function when the GTCCRA register is set to 0 during buffer transfer

Figure 22.98 and Figure 22.99 show examples of output protection function operation when the GTCCRA register is set to 0 during buffer transfer at troughs, and Figure 22.100 and Figure 22.101 show examples when the GTCCRA register is set to 0 during buffer transfer at crests.



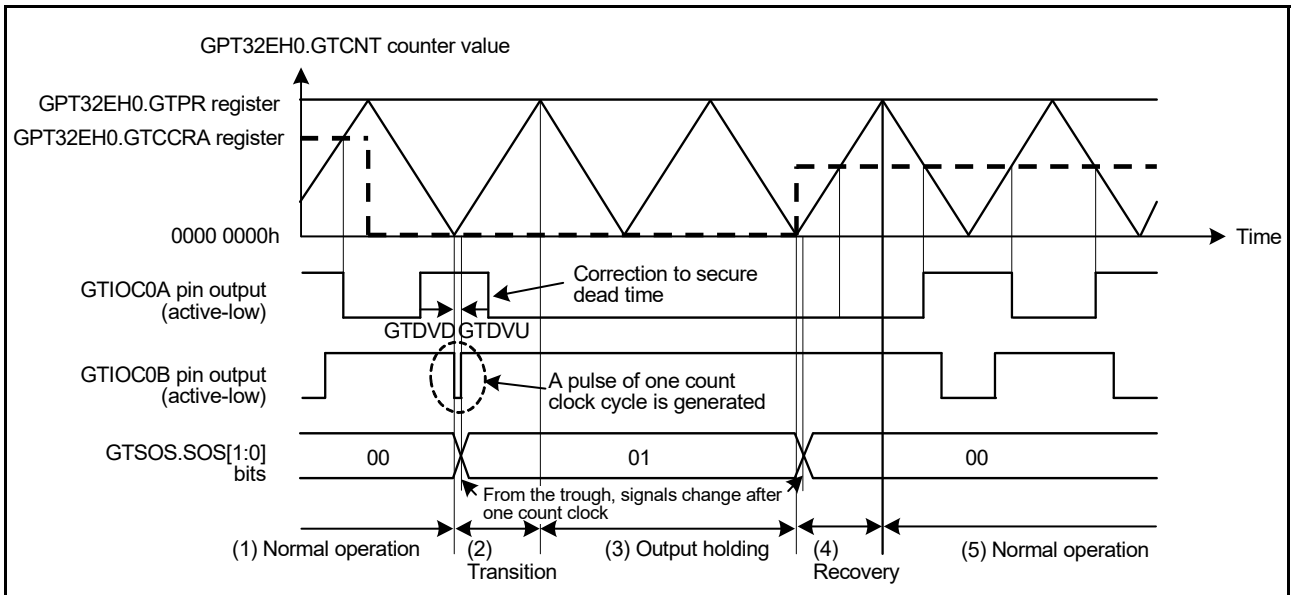
(1) Normal operation period: Toggle output from a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output continues up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Recovery period: When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output from a compare match is performed normally.

Figure 22.98 Example of output protection operation when GTCCRA is set to 0 during buffer transfer at troughs, with 0 < GTCCRA < GTPR restored during buffer transfer at troughs, and active-low



(1) Normal operation period: Toggle output from a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output continues up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Normal operation period: When 0 < GTCCRA register < GTPR register is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output from a compare match is performed normally.

Figure 22.99 Example of output protection operation when GTCCRA is set to 0 during buffer transfer at troughs, with 0 < GTCCRA < GTPR restored during buffer transfer at crests, and active-low



(1) Normal operation period: Toggle output from a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output continues up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Recovery period: When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output from a compare match is performed normally.

Figure 22.100 Example of output protection operation when GTCCRA is set to 0 during buffer transfer at crests, with 0 < GTCCRA < GTPR restored during buffer transfer at troughs, and active-low

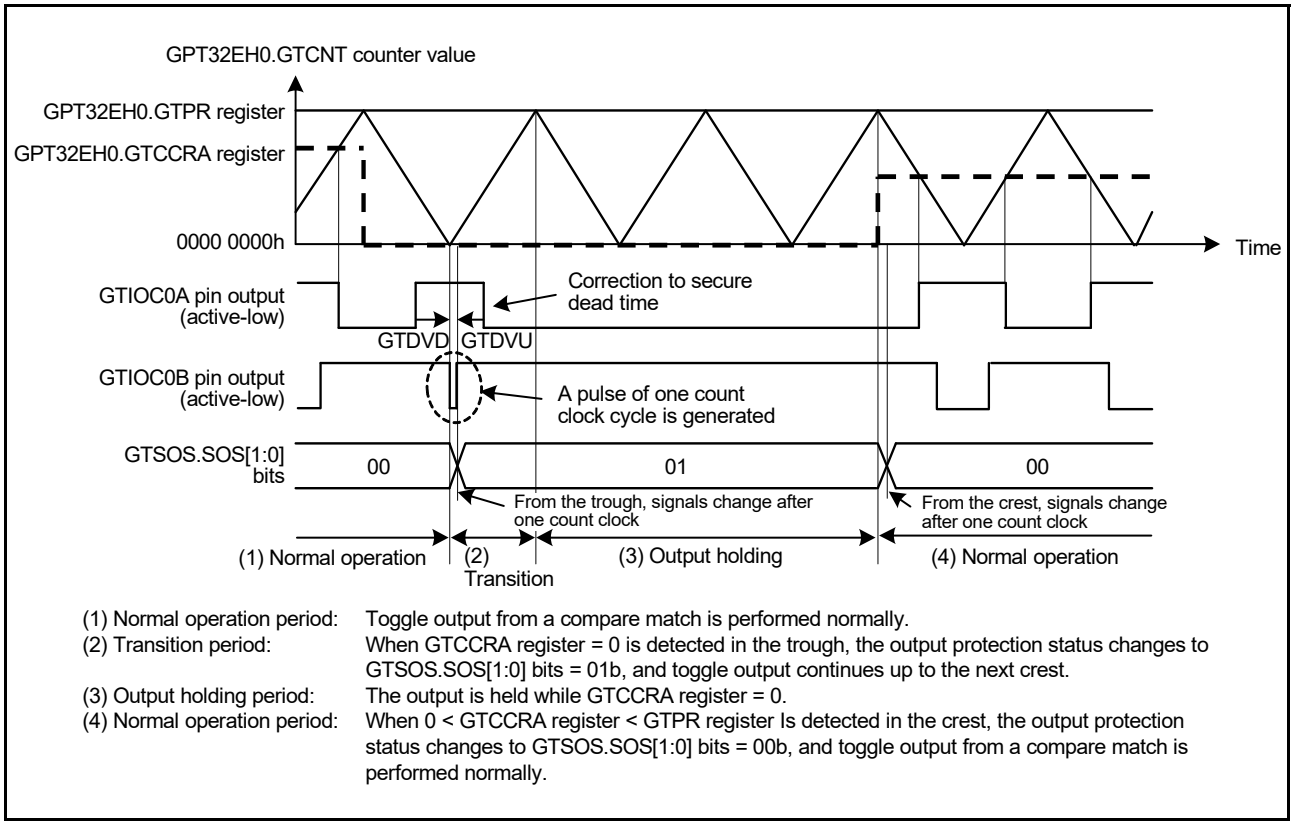
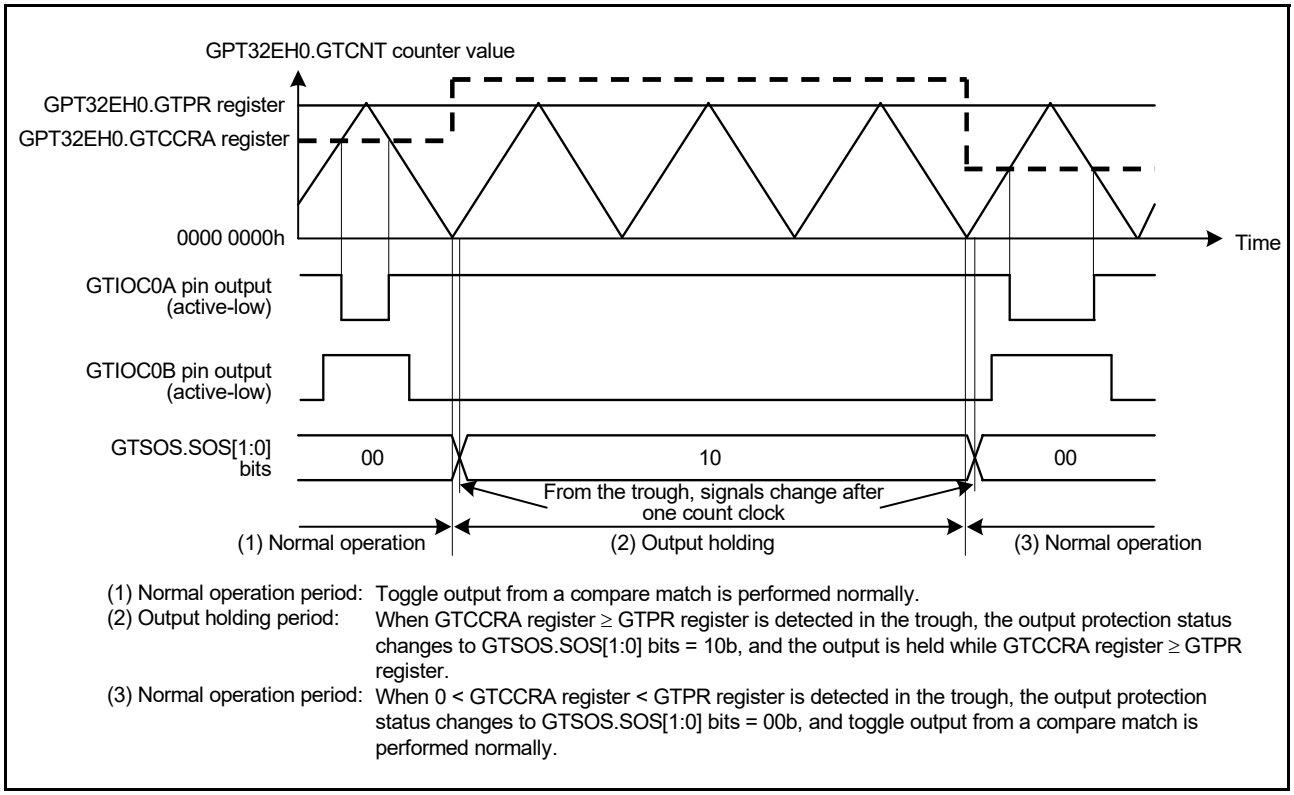


Figure 22.101 Example of output protection operation when GTCCRA is set to 0 during buffer transfer at crests, with 0 < GTCCRA < GTPR restored during buffer transfer at crests, and active-low

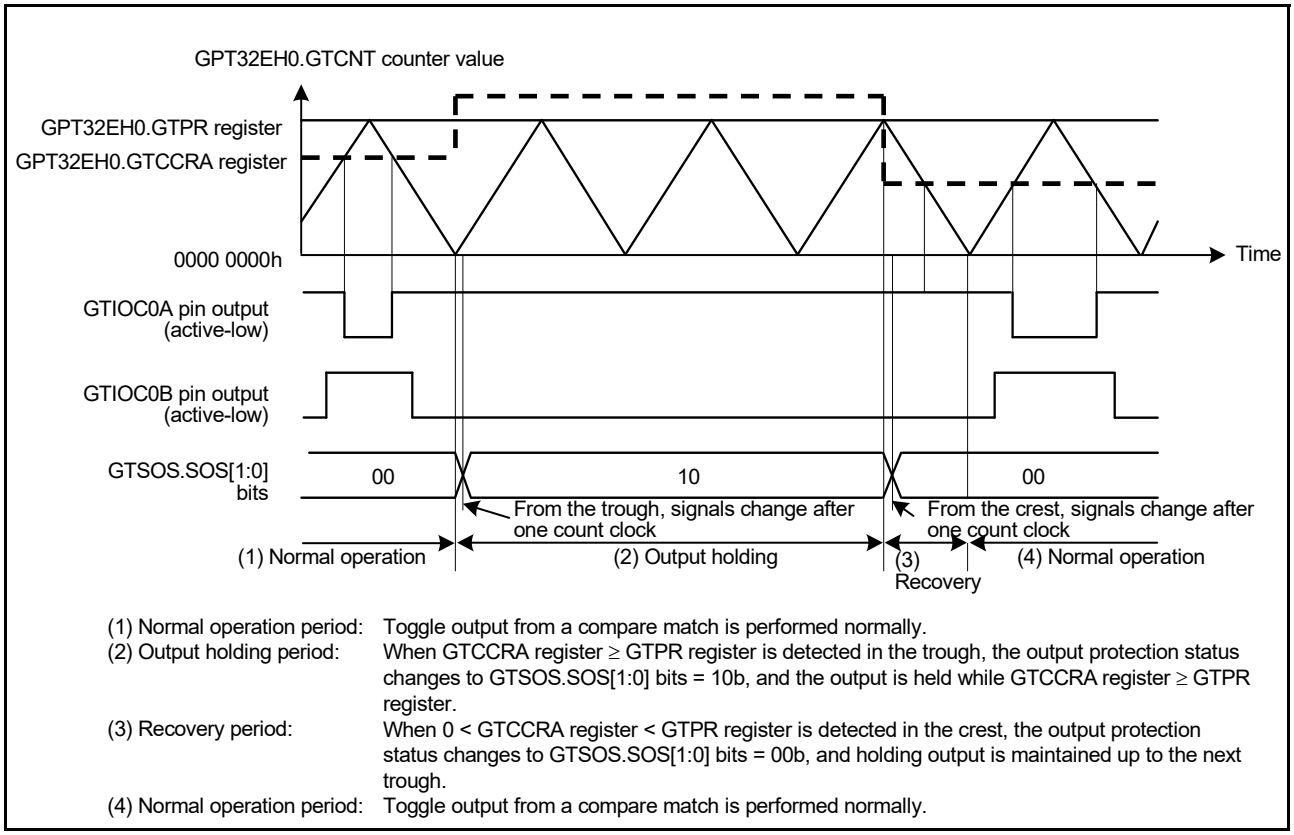
22.8.4.2 Output protection function when GTCCRA ≥ GTPR is set during buffer transfer at troughs

Figure 22.102 and Figure 22.103 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs.



(1) Normal operation period: Toggle output from a compare match is performed normally.
(2) Output holding period: When GTCCRA register ≥ GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA register ≥ GTPR register.
(3) Normal operation period: When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output from a compare match is performed normally.

Figure 22.102 Example of output protection operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs, with 0 < GTCCRA < GTPR restored during buffer transfer at troughs, and active-low



(1) Normal operation period: Toggle output from a compare match is performed normally.
(2) Output holding period: When GTCCRA register ≥ GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA register ≥ GTPR register.
(3) Recovery period: When 0 < GTCCRA register < GTPR register is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next trough.
(4) Normal operation period: Toggle output from a compare match is performed normally.

Figure 22.103 Example of output protection operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs, with 0 < GTCCRA < GTPR restored during buffer transfer at crests, and active-low

22.8.4.3 Output protection function when GTCCRA ≥ GTPR is set during buffer transfer at crests

Figure 22.104 and Figure 22.105 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests.

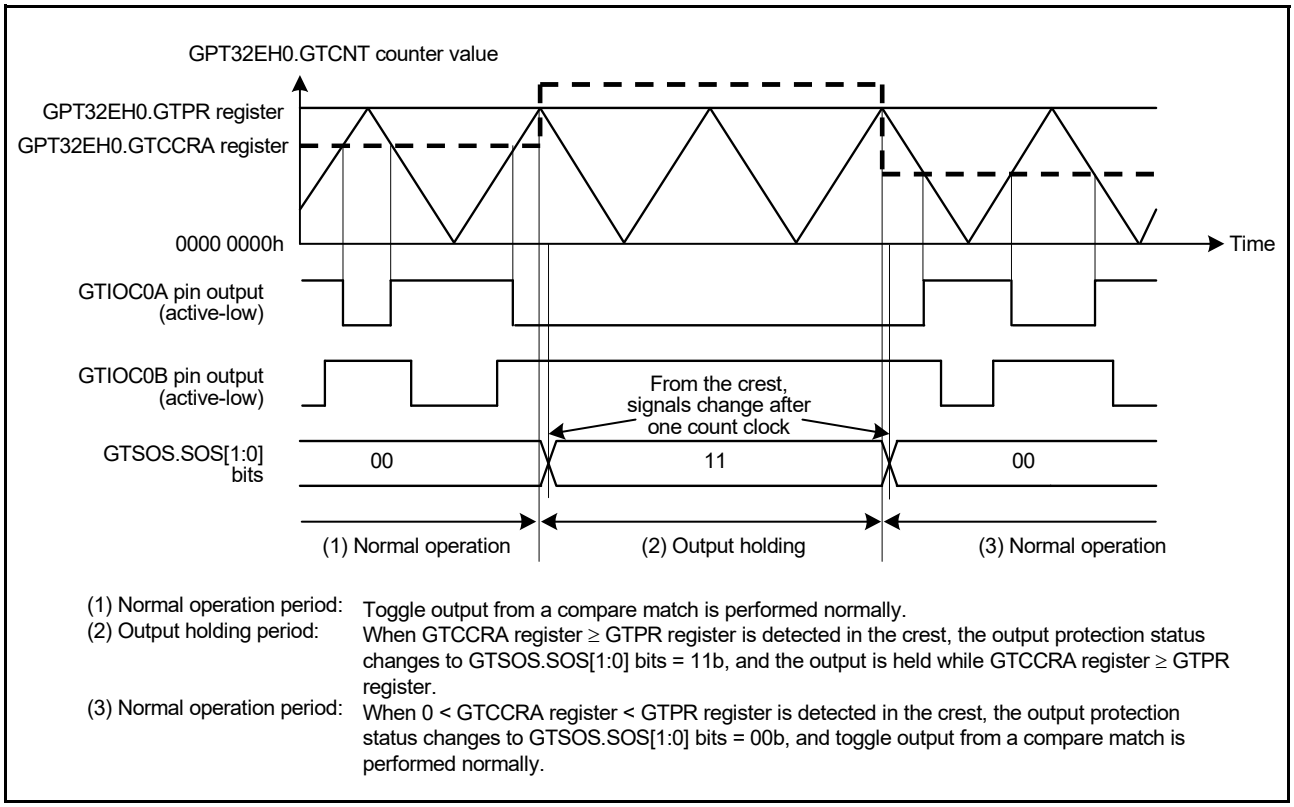


Figure 22.104 Example of output protection operation when GTCCRA ≥ GTPR is set during buffer transfer at crests, with 0 < GTCCRA < GTPR restored during buffer transfer at crests, and active-low

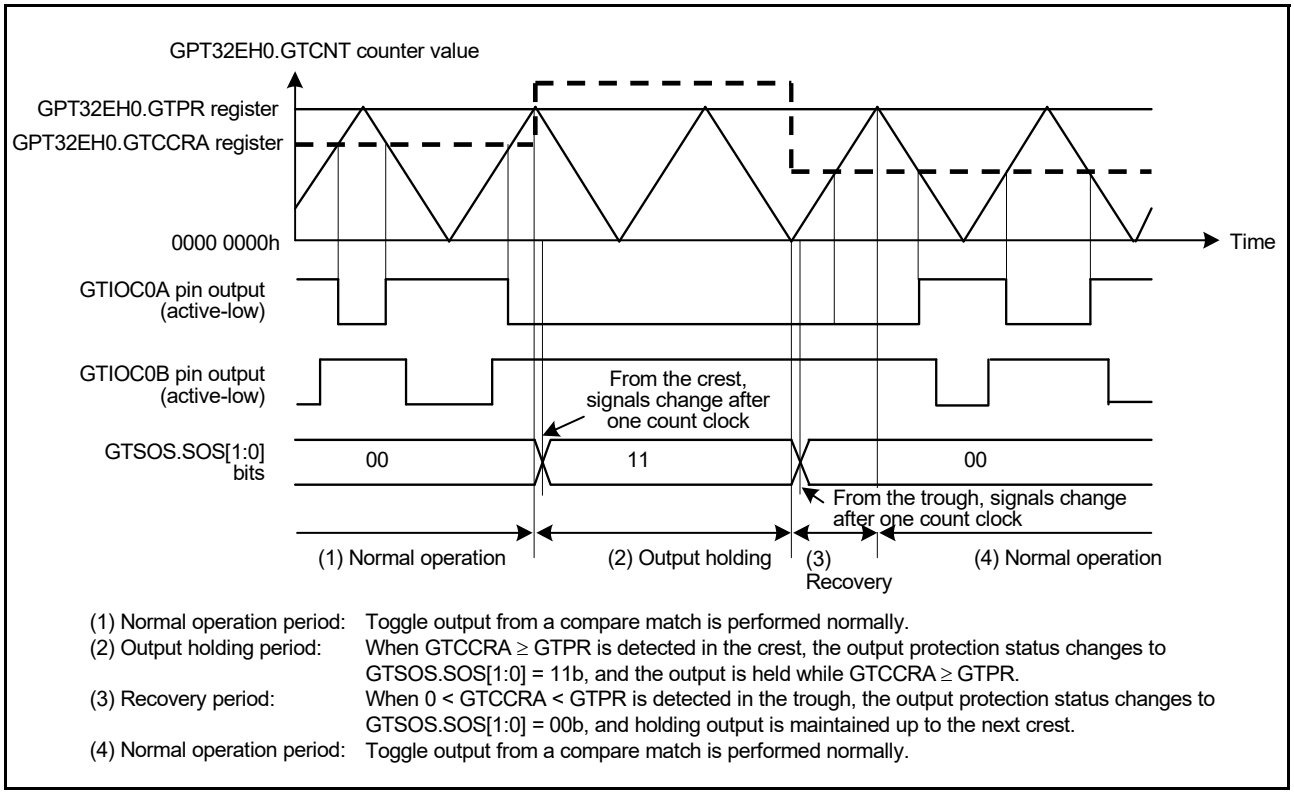


Figure 22.105 Example of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests, with 0 < GTCCRA < GTPR restored during buffer transfer at troughs, and active-low

22.8.4.4 Restricted specification of output protection function

The value of the GTCCRA register must be set within the range of (0 < GTCCRA < GTPR) at count start. If an incorrect value is set in the GTCCRA register during counting (a setting outside the range of 0 < GTCCRA < GTPR), the output protection function deactivates the level of one of the positive and negative outputs.

The function does not operate correctly if the following condition is not satisfied:

- 0 < GTCCRA < GTPR when counting starts.

22.8.4.5 Temporary cancellation of output protection function

When the GTSOTR.SOTR bit is set to 1 with GTSOS.SOS[1:0] bits equal to 10b (showing output protection state by GTCCRA ≥ GTPR during buffer transfer at troughs), the output protection function for GTIOCB pin is temporarily canceled. GTSOS.SOS[1:0] bits retain the value of 10b even when the output protection function is canceled. When the SOTR bit is set to 0, the output protection function for GTIOCB pin resumes.

Figure 22.106 shows examples of temporary cancellation of output protection function operation when the GTCCRA ≥ GTPR is set during buffer transfer at troughs.

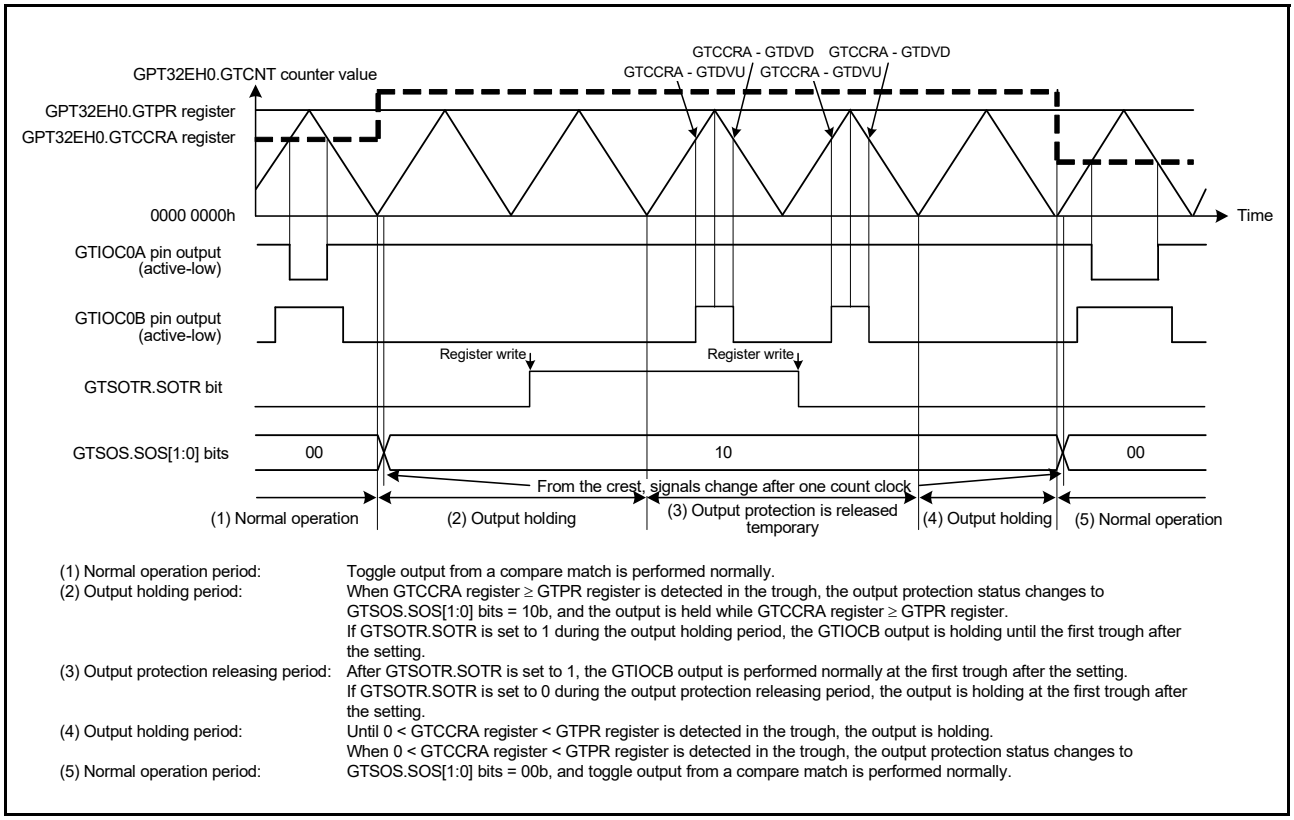


Figure 22.106 Example of temporary cancellation of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs, with 0 < GTCCRA < GTPR restored during buffer transfer at troughs, and active-low

22.9 Initialization Method of Output Pins

22.9.1 Pin Settings after Reset

The GPT registers are initialized at a reset. Start counting after selecting the port pin function with the PmnPFS register, setting GTIOR.OAE and GTIOR.OBE bits, and outputting the GPT function to external pins.

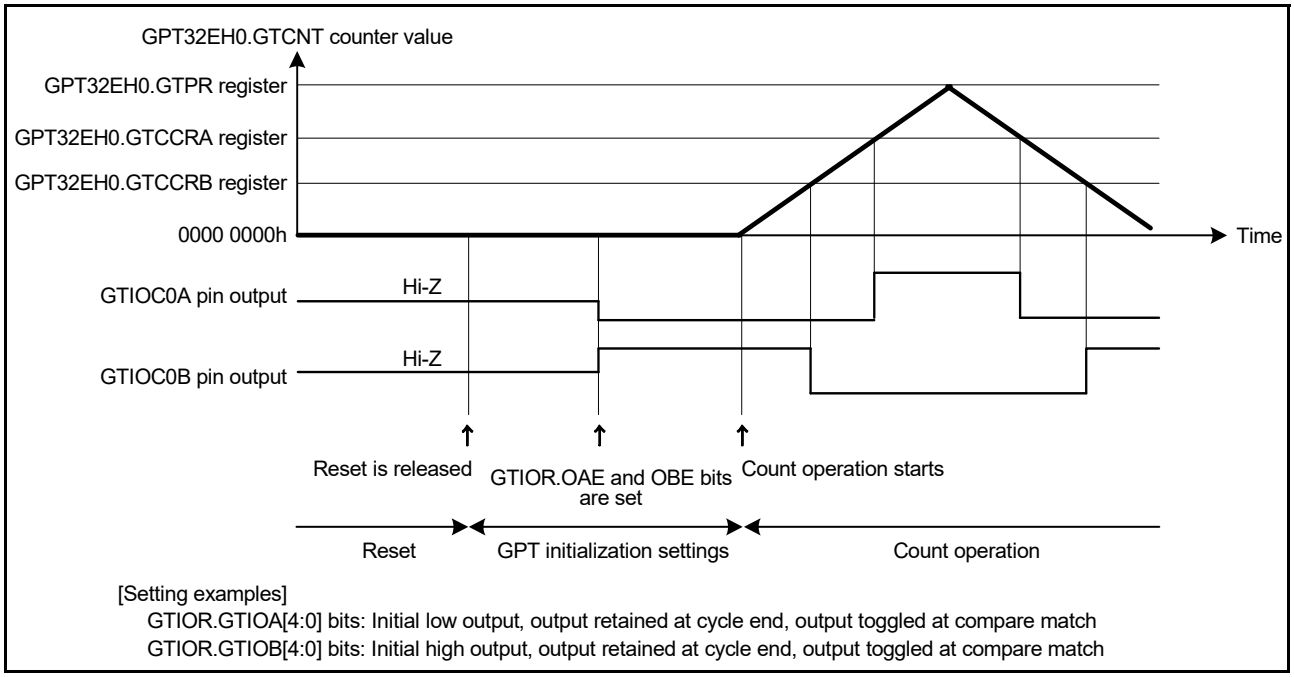


Figure 22.107 Example of pin settings after reset

22.9.2 Pin Initialization Caused by Error during Operation

If an error occurs during GPT operation, the following four types of pin processing can be performed before pin initialization:

- Set the OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop
- Set the OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values of OADFLT and OBDFLT in GTIOR, and output the arbitrary values on count stop
- Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR, and PmnPFS registers of the I/O port in advance. Set the OAE and OBE bits in GTIOR to 0, and the control bit associated with the pin in PmnPFS.PMR to 0 to allow arbitrary values to be output from the pin set as a general output port when an error occurs.
- Drive the output to a high impedance state using the POEG function.

When the automatic dead time setting is made, clear the GTDTCR.TDE bit to 0 after counting stops. When counting stops, only the values of registers that are changed by a GPT external source change. If counting resumes, operation continues from where it stopped. If counting stops, registers must be initialized before counting starts.

22.10 Usage Notes

22.10.1 Module-Stop Function Setting

The Module Stop Control Register can enable or disable GPT operation. The GPT module is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

22.10.2 GTCCRn Settings during Compare Match Operation (n = A to F)

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy all of the following conditions:

- GTDVU < GTCCRA
- GTDVD < GTCCRA
- GTCCRA < GTPR.

When the setting of GTCCRA = 0 or GTCCRA ≥ GTPR is made during count operation, the output protection function is activated.

However, the function does not operate correctly if the following condition is not satisfied:

- 0 < GTCCRA < GTPR when counting starts.

For details, see section 22.8.4, Output Protection Function for GTIOC Pin Output.

(2) When automatic dead time setting is not made in triangle-wave PWM mode

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. When GTCCRA > GTPR, no compare match occurs.

Similarly, GTCCRB must be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, correct output waveforms with secured dead time might not be obtained:

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVD
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVD.

(4) When automatic dead time setting is not made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed:

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0.

Similarly, GTCCRE and GTCCRF must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed:

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) In saw-wave PWM mode

The GTCCRA register must be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.

Similarly, GTCCRB must be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

22.10.3 Setting Range for the GTCNT Counter

The GTCNT counter register must be set with the range of 0 ≤ GTCNT ≤ GTPR.

22.10.4 Starting and Stopping the GTCNT Counter

The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[2:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock selected in GTCR.TPCS[2:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored. On the other hand, there might be cases where an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

22.10.5 Priority Order of Each Event

(1) GTCNT register

Table 22.24 shows a priority order of events updating GTCNT register.

Table 22.24 Priority order of sources updating GTCNT

Source updating GTCNT	Priority order
Writing by CPU (writing to GTCNT/GTCLR)	High ↑ Low
Clear by hardware sources set in GTCSR	
Count up or down by hardware sources set in GTUPSR/GTDNSR	
Count operation	

If up-counting and down-counting by hardware sources occur at the same time, the GTCNT counter value does not change. When there is a conflict between updating the GTCNT register and reading by the CPU, pre-update data is read.

(2) GTCR.CST bit

When there is a conflict between starting/stopping by hardware sources set in the GTSSR/GTPSR registers and writing by the CPU (writing to GTCR/GTSTR/GTSTP registers), writing by CPU has priority over starting/stopping by hardware sources.

When there is a conflict between starting by hardware sources set in the GTSSR register and stopping by hardware sources set in GTPSR register, the GTCR.CST bit value does not change. Where there is a conflict between updating the GTCR.CST bit and reading by the CPU, pre-update data is read.

(3) GTCCRm registers (m = A to F)

When there is a conflict between input capture/buffer transfer operation and writing to GTCCRm registers, writing to GTCCRm registers has priority over input capture/buffer transfer operation. When there is a conflict between input capture and writing to the counter register by the CPU or updating the counter register by hardware sources, the pre-update counter value is captured. Where there is a conflict between updating the GTCCRm registers and reading by the CPU, pre-update data is read.

(4) GTPR registers

When there is a conflict between buffer transfer operation and writing to the GTPR register, writing to GTPR register has priority over buffer transfer operation. When there is a conflict between updating GTPR register and reading by the CPU, pre-update data is read.

(5) GTADTRm registers (m = A, B)

When there is a conflict between buffer transfer operation and writing to the GTADTRm registers, writing to the GTADTRm registers has priority over buffer transfer operation. When there is a conflict between updating GTADTRm registers and reading by the CPU, pre-update data is read.

(6) GTDVm registers (m = U, D)

When there is a conflict between buffer transfer operation and writing to GTDVm registers, writing to GTDVm registers has priority over buffer transfer operation. When there is a conflict between updating GTDVm registers and reading by the CPU, pre-update data is read.

23. PWM Delay Generation Circuit

23.1 Overview

The MCU has four channel delay circuits that can connect to the General PWM Timer (GPT). Table 23.1 lists the PWM Delay Generation Circuit specifications, Figure 23.1 shows a block diagram, and Table 23.2 lists the I/O pins.

Table 23.1 PWM delay generation circuit specifications

Parameter	Specifications
Function	The circuit can control the timing with which signals on the two PWM output pins for channel 0/1/2/3 rise and fall to an accuracy of up to 1/32 times the period of the GPT clock (PCLKD)

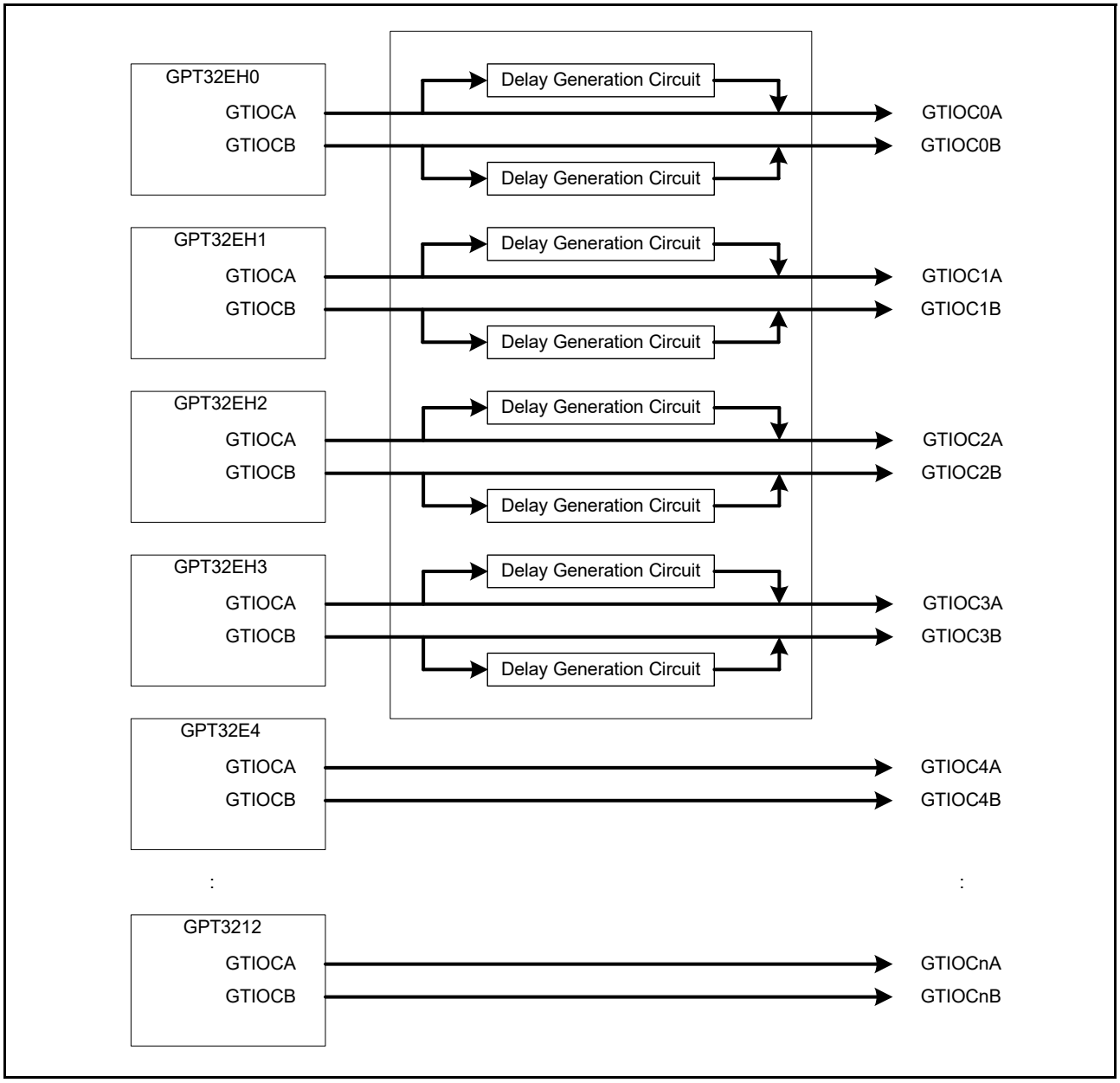


Figure 23.1 PWM delay generation circuit block diagram

Table 23.2 PWM delay generation circuit I/O pins

I/O pin	I/O	Function
GTIOC0A	Output	Delayed output of GTIOCA pin for GPT channel 0
GTIOC0B	Output	Delayed output of GTIOCB pin for GPT channel 0
GTIOC1A	Output	Delayed output of GTIOCA pin for GPT channel 1
GTIOC1B	Output	Delayed output of GTIOCB pin for GPT channel 1
GTIOC2A	Output	Delayed output of GTIOCA pin for GPT channel 2
GTIOC2B	Output	Delayed output of GTIOCB pin for GPT channel 2
GTIOC3A	Output	Delayed output of GTIOCA pin for GPT channel 3
GTIOC3B	Output	Delayed output of GTIOCB pin for GPT channel 3

23.2 Register Descriptions

23.2.1 PWM Output Delay Control Register (GTDLYCR)

Address(es): GPT_ODC.GTDLYCR 4007 B000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DLYRST	DLLEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLLEN	DLL Operation Enable	0: DLL operation disabled 1: DLL operation enabled.	R/W
b1	DLYRST	PWM Delay Generation Circuit Reset	0: Normal operation 1: Reset.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYCR register controls the PWM delay generation circuit, which applies delays to the PWM outputs. The GTDLYCR can be written when register write protection is disabled (GPT32EH0.GTWP.WP = 0).

DLLEN bit (DLL Operation Enable)

The DLLEN bit selects whether the on-chip DLL in the PWM delay generation circuit is activated or not.

DLYRST bit (PWM Delay Generation Circuit Reset)

The DLYRST bit resets the internal state of the PWM delay generation circuit.

23.2.2 PWM Output Delay Control Register 2 (GTDLYCR2)

Address(es): GPT_ODC.GTDLYCR2 4007 B002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	DLYEN3	DLYEN2	DLYEN1	DLYEN0	—	—	—	—	DLYBS3	DLYBS2	DLYBS1	DLYBS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLYBS0	PWM Delay Generation Circuit bypass for channel 0	0: Delay generation circuit of channel 0 bypassed 1: Delay generation circuit of channel 0 not bypassed.	R/W

Bit	Symbol	Bit name	Description	R/W
b1	DLYBS1	PWM Delay Generation Circuit bypass for channel 1	0: Delay generation circuit of channel 1 bypassed 1: Delay generation circuit of channel 1 not bypassed.	R/W
b2	DLYBS2	PWM Delay Generation Circuit bypass for channel 2	0: Delay generation circuit of channel 2 bypassed 1: Delay generation circuit of channel 2 not bypassed.	R/W
b3	DLYBS3	PWM Delay Generation Circuit bypass for channel 3	0: Delay generation circuit of channel 3 bypassed 1: Delay generation circuit of channel 3 not bypassed.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DLYEN0	PWM Delay Generation Circuit enable for channel 0	0: Delay generation circuit of channel 0 enabled 1: Delay generation circuit of channel 0 disabled.	R/W
b9	DLYEN1	PWM Delay Generation Circuit enable for channel 1	0: Delay generation circuit of channel 1 enabled 1: Delay generation circuit of channel 1 disabled.	R/W
b10	DLYEN2	PWM Delay Generation Circuit enable for channel 2	0: Delay generation circuit of channel 2 enabled 1: Delay generation circuit of channel 2 disabled.	R/W
b11	DLYEN3	PWM Delay Generation Circuit enable for channel 3	0: Delay generation circuit of channel 3 enabled 1: Delay generation circuit of channel 3 disabled.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYCR2 register controls each channel of PWM delay generation circuit. The GTDLYCR2 can be written when register write protection is disabled (GPT32EH0.GTWP.WP = 0).

DLYBSn (n = 0 to 3) bit (PWM Delay Generation Circuit Bypass for channel n)

The DLYBSn bit selects whether delays are applied to PWM output signals from the GTIOCnA and GTIOCnB pins (n = 0 to 3) by the PWM delay generation circuit or whether the circuit is bypassed.

A signal delayed in the PWM delay generation circuit is output 3 PCLKD cycles of GPT operation clock later than if it bypasses the PWM delay generation circuit.

DLYENn (n = 0 to 3) bit (PWM Delay Generation Circuit Enable for channel n)

The DLYENn bit selects whether channel n (n = 0 to 3) of PWM delay generation circuit is power on or off. If channel n of the PWM delay generation circuit is not used, set this bit to 1.

23.2.3 GTIOCnA Rising Output Delay Register (GTDLYRnA) (n = 0 to 3)

Address(es): GPT_ODC.GTDLYR0A 4007 B018h, GPT_ODC.GTDLYR1A 4007 B01Ch, GPT_ODC.GTDLYR2A 4007 B020h, GPT_ODC.GTDLYR3A 4007 B024h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnA Output Rising Edge Delay Setting	b4 b0 0 0 0 0 0: Delay on rising edges is not applied 0 0 0 0 1: Delay of 1/32 times PCLKD period applied 0 0 0 1 0: Delay of 2/32 times PCLKD period applied 0 0 0 1 1: Delay of 3/ 32 times PCLKD period applied 0 0 1 0 0: Delay of 4/ 32 times PCLKD period applied 0 0 1 0 1: Delay of 5/ 32 times PCLKD period applied 0 0 1 1 0: Delay of 6/ 32 times PCLKD period applied 0 0 1 1 1: Delay of 7/ 32 times PCLKD period applied 0 1 0 0 0: Delay of 8/ 32 times PCLKD period applied 0 1 0 0 1: Delay of 9/ 32 times PCLKD period applied 0 1 0 1 0: Delay of 10/ 32 times PCLKD period applied 0 1 0 1 1: Delay of 11/ 32 times PCLKD period applied 0 1 1 0 0: Delay of 12/ 32 times PCLKD period applied 0 1 1 0 1: Delay of 13/ 32 times PCLKD period applied 0 1 1 1 0: Delay of 14/ 32 times PCLKD period applied 0 1 1 1 1: Delay of 15/ 32 times PCLKD period applied 1 0 0 0 0: Delay of 16/ 32 times PCLKD period applied 1 0 0 0 1: Delay of 17/ 32 times PCLKD period applied 1 0 0 1 0: Delay of 18/ 32 times PCLKD period applied 1 0 0 1 1: Delay of 19/ 32 times PCLKD period applied 1 0 1 0 0: Delay of 20/ 32 times PCLKD period applied 1 0 1 0 1: Delay of 21/ 32 times PCLKD period applied 1 0 1 1 0: Delay of 22/ 32 times PCLKD period applied 1 0 1 1 1: Delay of 23/ 32 times PCLKD period applied 1 1 0 0 0: Delay of 24/ 32 times PCLKD period applied 1 1 0 0 1: Delay of 25/ 32 times PCLKD period applied 1 1 0 1 0: Delay of 26/ 32 times PCLKD period applied 1 1 0 1 1: Delay of 27/ 32 times PCLKD period applied 1 1 1 0 0: Delay of 28/ 32 times PCLKD period applied 1 1 1 0 1: Delay of 29/ 32 times PCLKD period applied 1 1 1 1 0: Delay of 30/ 32 times PCLKD period applied 1 1 1 1 1: Delay of 31/ 32 times PCLKD period applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYRnA register sets a delay to be applied to rising edges of output signals on the GTIOCnA pin. On the timing for the transfer of settings, see section 23.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

The GTDLYRnA can be written when register write protection is disabled (GPT32EHn.GTWP.WP = 0).

23.2.4 GTIOCnA Falling Output Delay Register (GTDLYFnA) (n = 0 to 3)

Address(es): GPT_ODC.GTDLYF0A 4007 B028h, GPT_ODC.GTDLYF1A 4007 B02Ch, GPT_ODC.GTDLYF2A 4007 B030h, GPT_ODC.GTDLYF3A 4007 B034h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnA Output Falling Edge Delay Setting	b4 b0 0 0 0 0 0: Delay on falling edges is not applied 0 0 0 0 1: Delay of 1/32 times PCLKD period applied 0 0 0 1 0: Delay of 2/32 times PCLKD period applied 0 0 0 1 1: Delay of 3/ 32 times PCLKD period applied 0 0 1 0 0: Delay of 4/ 32 times PCLKD period applied 0 0 1 0 1: Delay of 5/ 32 times PCLKD period applied 0 0 1 1 0: Delay of 6/ 32 times PCLKD period applied 0 0 1 1 1: Delay of 7/ 32 times PCLKD period applied 0 1 0 0 0: Delay of 8/ 32 times PCLKD period applied 0 1 0 0 1: Delay of 9/ 32 times PCLKD period applied 0 1 0 1 0: Delay of 10/ 32 times PCLKD period applied 0 1 0 1 1: Delay of 11/ 32 times PCLKD period applied 0 1 1 0 0: Delay of 12/ 32 times PCLKD period applied 0 1 1 0 1: Delay of 13/ 32 times PCLKD period applied 0 1 1 1 0: Delay of 14/ 32 times PCLKD period applied 0 1 1 1 1: Delay of 15/ 32 times PCLKD period applied 1 0 0 0 0: Delay of 16/ 32 times PCLKD period applied 1 0 0 0 1: Delay of 17/ 32 times PCLKD period applied 1 0 0 1 0: Delay of 18/ 32 times PCLKD period applied 1 0 0 1 1: Delay of 19/ 32 times PCLKD period applied 1 0 1 0 0: Delay of 20/ 32 times PCLKD period applied 1 0 1 0 1: Delay of 21/ 32 times PCLKD period applied 1 0 1 1 0: Delay of 22/ 32 times PCLKD period applied 1 0 1 1 1: Delay of 23/ 32 times PCLKD period applied 1 1 0 0 0: Delay of 24/ 32 times PCLKD period applied 1 1 0 0 1: Delay of 25/ 32 times PCLKD period applied 1 1 0 1 0: Delay of 26/ 32 times PCLKD period applied 1 1 0 1 1: Delay of 27/ 32 times PCLKD period applied 1 1 1 0 0: Delay of 28/ 32 times PCLKD period applied 1 1 1 0 1: Delay of 29/ 32 times PCLKD period applied 1 1 1 1 0: Delay of 30/ 32 times PCLKD period applied 1 1 1 1 1: Delay of 31/ 32 times PCLKD period applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYFnA register sets a delay to be applied to falling edges of output signals on the GTIOCnA pin. On the timing for the transfer of settings, see section 23.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

The GTDLYFnA can be written when register write protection is disabled (GPT32EHn.GTWP.WP = 0).

23.2.5 GTIOCnB Rising Output Delay Register (GTDLYRnB) (n = 0 to 3)

Address(es): GPT_ODC.GTDLYR0B 4007 B01Ah, GPT_ODC.GTDLYR1B 4007 B01Eh, GPT_ODC.GTDLYR2B 4007 B022h, GPT_ODC.GTDLYR3B 4007 B026h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnB Output Rising Edge Delay Setting	b4 b0 0 0 0 0 0: Delay on rising edges is not applied 0 0 0 0 1: Delay of 1/32 times PCLKD period applied 0 0 0 1 0: Delay of 2/32 times PCLKD period applied 0 0 0 1 1: Delay of 3/ 32 times PCLKD period applied 0 0 1 0 0: Delay of 4/ 32 times PCLKD period applied 0 0 1 0 1: Delay of 5/ 32 times PCLKD period applied 0 0 1 1 0: Delay of 6/ 32 times PCLKD period applied 0 0 1 1 1: Delay of 7/ 32 times PCLKD period applied 0 1 0 0 0: Delay of 8/ 32 times PCLKD period applied 0 1 0 0 1: Delay of 9/ 32 times PCLKD period applied 0 1 0 1 0: Delay of 10/ 32 times PCLKD period applied 0 1 0 1 1: Delay of 11/ 32 times PCLKD period applied 0 1 1 0 0: Delay of 12/ 32 times PCLKD period applied 0 1 1 0 1: Delay of 13/ 32 times PCLKD period applied 0 1 1 1 0: Delay of 14/ 32 times PCLKD period applied 0 1 1 1 1: Delay of 15/ 32 times PCLKD period applied 1 0 0 0 0: Delay of 16/ 32 times PCLKD period applied 1 0 0 0 1: Delay of 17/ 32 times PCLKD period applied 1 0 0 1 0: Delay of 18/ 32 times PCLKD period applied 1 0 0 1 1: Delay of 19/ 32 times PCLKD period applied 1 0 1 0 0: Delay of 20/ 32 times PCLKD period applied 1 0 1 0 1: Delay of 21/ 32 times PCLKD period applied 1 0 1 1 0: Delay of 22/ 32 times PCLKD period applied 1 0 1 1 1: Delay of 23/ 32 times PCLKD period applied 1 1 0 0 0: Delay of 24/ 32 times PCLKD period applied 1 1 0 0 1: Delay of 25/ 32 times PCLKD period applied 1 1 0 1 0: Delay of 26/ 32 times PCLKD period applied 1 1 0 1 1: Delay of 27/ 32 times PCLKD period applied 1 1 1 0 0: Delay of 28/ 32 times PCLKD period applied 1 1 1 0 1: Delay of 29/ 32 times PCLKD period applied 1 1 1 1 0: Delay of 30/ 32 times PCLKD period applied 1 1 1 1 1: Delay of 31/ 32 times PCLKD period applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYRnB register sets a delay to be applied to rising edges of output signals on the GTIOCnB pin. On the timing for the transfer of settings, see section 23.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

The GTDLYRnB can be written when register write protection is disabled (GPT32EHn.GTWP.WP = 0).

23.2.6 GTIOCnB Falling Output Delay Register (GTDLYFnB) (n = 0 to 3)

Address(es): GPT_ODC.GTDLYF0B 4007 B02Ah, GPT_ODC.GTDLYF1B 4007 B02Eh, GPT_ODC.GTDLYF2B 4007 B032h, GPT_ODC.GTDLYF3B 4007 B036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnB Output Falling Edge Delay Setting	b4 b0 0 0 0 0 0: Delay on falling edges is not applied 0 0 0 0 1: Delay of 1/32 times PCLKD period applied 0 0 0 1 0: Delay of 2/32 times PCLKD period applied 0 0 0 1 1: Delay of 3/ 32 times PCLKD period applied 0 0 1 0 0: Delay of 4/ 32 times PCLKD period applied 0 0 1 0 1: Delay of 5/ 32 times PCLKD period applied 0 0 1 1 0: Delay of 6/ 32 times PCLKD period applied 0 0 1 1 1: Delay of 7/ 32 times PCLKD period applied 0 1 0 0 0: Delay of 8/ 32 times PCLKD period applied 0 1 0 0 1: Delay of 9/ 32 times PCLKD period applied 0 1 0 1 0: Delay of 10/ 32 times PCLKD period applied 0 1 0 1 1: Delay of 11/ 32 times PCLKD period applied 0 1 1 0 0: Delay of 12/ 32 times PCLKD period applied 0 1 1 0 1: Delay of 13/ 32 times PCLKD period applied 0 1 1 1 0: Delay of 14/ 32 times PCLKD period applied 0 1 1 1 1: Delay of 15/ 32 times PCLKD period applied 1 0 0 0 0: Delay of 16/ 32 times PCLKD period applied 1 0 0 0 1: Delay of 17/ 32 times PCLKD period applied 1 0 0 1 0: Delay of 18/ 32 times PCLKD period applied 1 0 0 1 1: Delay of 19/ 32 times PCLKD period applied 1 0 1 0 0: Delay of 20/ 32 times PCLKD period applied 1 0 1 0 1: Delay of 21/ 32 times PCLKD period applied 1 0 1 1 0: Delay of 22/ 32 times PCLKD period applied 1 0 1 1 1: Delay of 23/ 32 times PCLKD period applied 1 1 0 0 0: Delay of 24/ 32 times PCLKD period applied 1 1 0 0 1: Delay of 25/ 32 times PCLKD period applied 1 1 0 1 0: Delay of 26/ 32 times PCLKD period applied 1 1 0 1 1: Delay of 27/ 32 times PCLKD period applied 1 1 1 0 0: Delay of 28/ 32 times PCLKD period applied 1 1 1 0 1: Delay of 29/ 32 times PCLKD period applied 1 1 1 1 0: Delay of 30/ 32 times PCLKD period applied 1 1 1 1 1: Delay of 31/ 32 times PCLKD period applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYFnB register sets a delay to be applied to falling edges of output signals on the GTIOCnB pin. On the timing for the transfer of settings, see section 23.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

The GTDLYFnB can be written when register write protection is disabled (GPT32EHn.GTWP.WP = 0).

23.3 Operation

23.3.1 Adjustments to the Timing of Rising and Falling Edges in PWM Waveforms

The timing of rising and falling edges in PWM waveforms which are output from the GTIOCnA and GTIOCnB pins, where n = channel number, can be delayed to an accuracy of 1/32 of the GPT operating clock (PCLKD) period.

If the timing of rising or falling edges in PWM waveforms output from the GTIOCnA and GTIOCnB pins must be adjusted, initialize the PWM generation circuit as shown in the procedure in Figure 23.2.

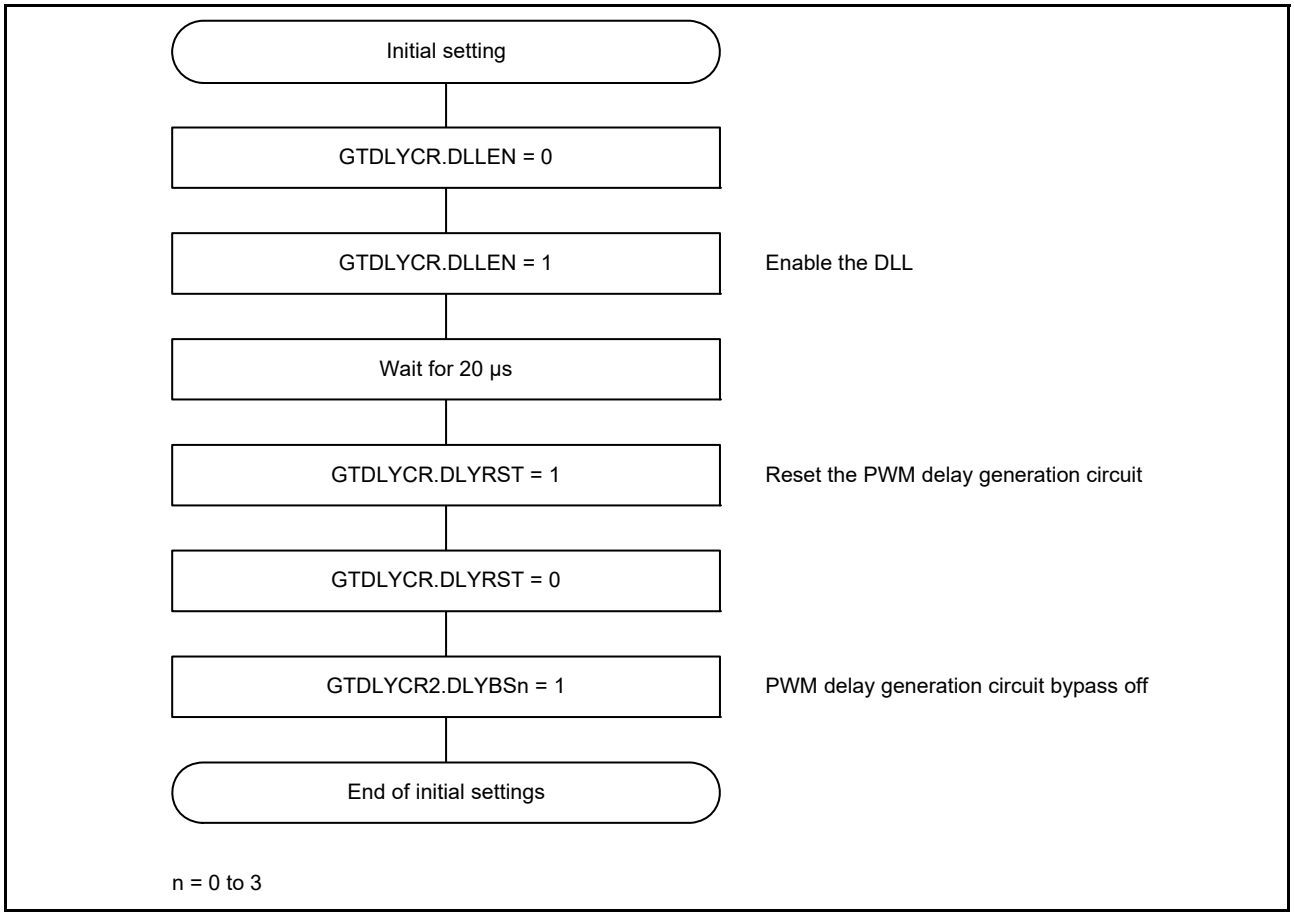


Figure 23.2 Example of initialization flow for the PWM delay generation circuit

In the PWM delay generation circuit, delay can be applied to rising and falling edges of the PWM output to an accuracy of 1/32 of the period of the GPT operation clock (PCLKD). This is described in section 22.3.3, PWM Output Operating Mode. Delays associated with the settings are reflected in the PWM output with the timing described in section 23.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

Table 23.3 shows the association between the GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB registers and the PWM outputs.

Table 23.3 Association between PWM output pins and delay setting registers

PWM output pin	Rising-edge delay setting register	Falling-edge delay setting register
GTIOC0A	GTDLYR0A	GTDLYF0A
GTIOC0B	GTDLYR0B	GTDLYF0B
GTIOC1A	GTDLYR1A	GTDLYF1A
GTIOC1B	GTDLYR1B	GTDLYF1B
GTIOC2A	GTDLYR2A	GTDLYF2A
GTIOC2B	GTDLYR2B	GTDLYF2B
GTIOC3A	GTDLYR3A	GTDLYF3A
GTIOC3B	GTDLYR3B	GTDLYF3B

When the PWM delay generation circuit is in use, the timing with which a PWM output signal rises and falls can be controlled to an accuracy of 1/32 of the period of the GPT operation clock (PCLKD). When this option is not in use, the period of the PWM output waveform is controlled to an accuracy of one period of the input clock for the timer counter, which is PCLKD. With the PWM delay generation circuit, the output can be controlled to an accuracy 32 times better. Additionally, the delay settings also control the periods at high and low level for the PWM waveform to the given accuracy. PWM delay generation circuit channels can be individually enabled or disabled.

23.3.2 Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings

Settings for the GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB registers are initially transferred to temporary registers, and then reflected in the delay on the GTIOCnA and GTIOCnB (n = 0 to 3) outputs. Transfer of the settings takes place on overflows (in up-counting) or underflows (in down-counting) for saw waves, and in the troughs of triangle waves.

Figure 23.3 and Figure 23.4 show examples of the operation of the GTDLYR0A and GTDLYF0A registers.

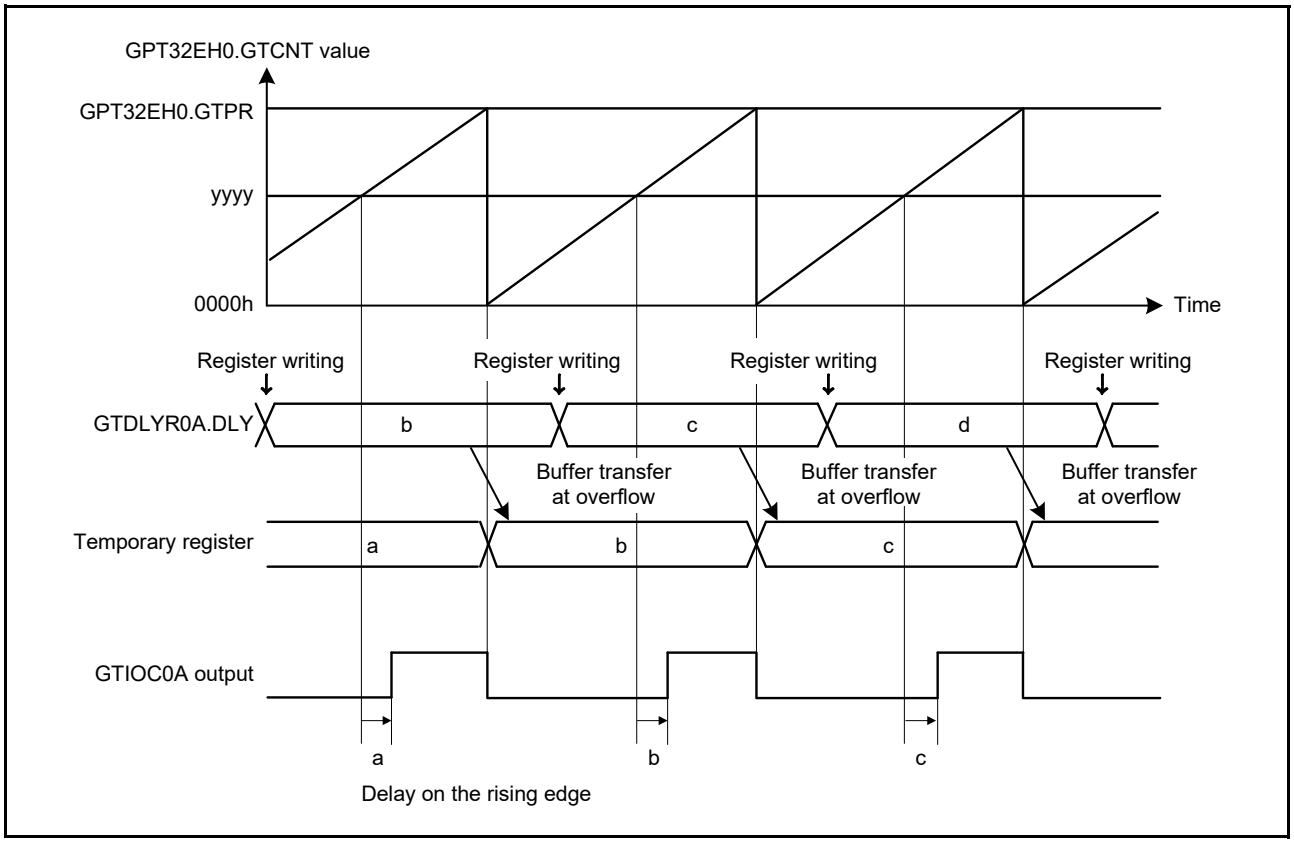


Figure 23.3 Example of GTLDYR0A register operation with PWM saw-wave generation

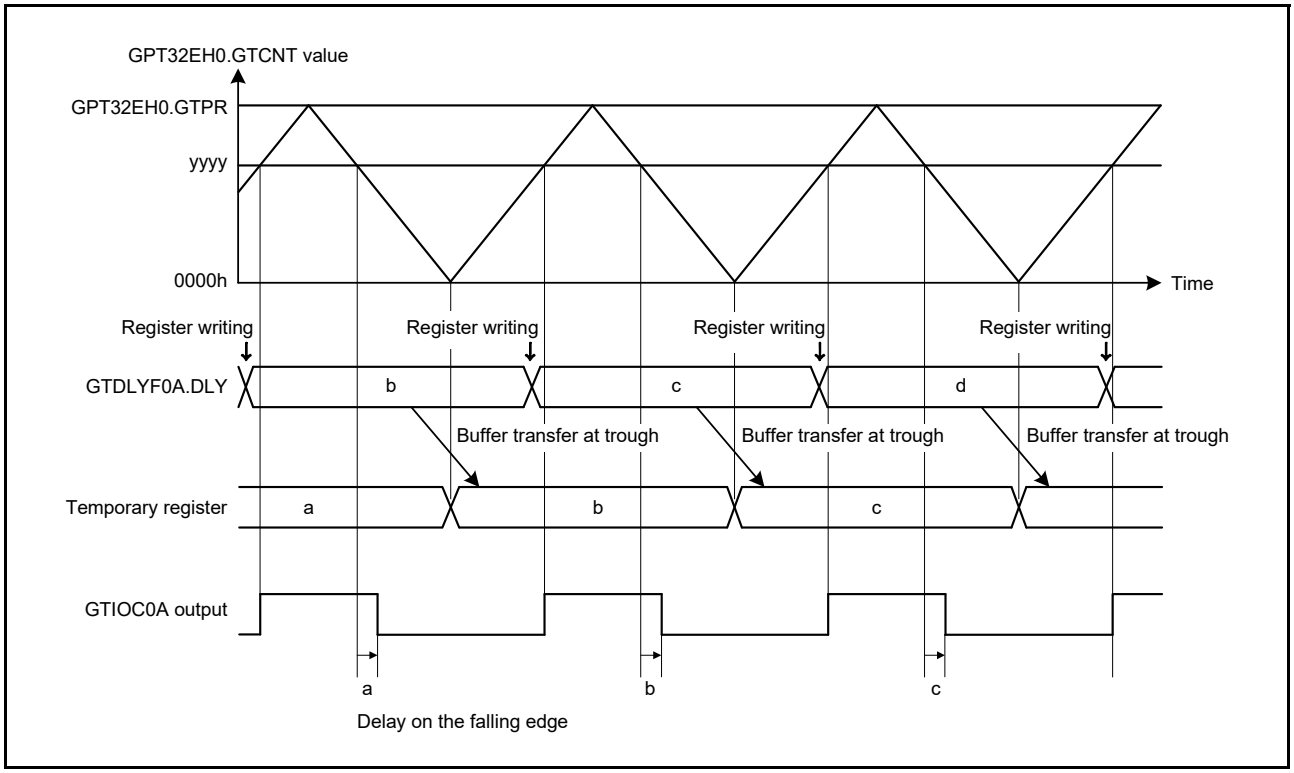


Figure 23.4 Example of GTLDYF0A register operation with PWM triangle-wave generation

23.4 Usage Notes

23.4.1 Module-Stop Function Settings

The Module Stop Control Register D (MSTPCRD) can enable or disable operation of the PWM delay generation circuit. The PWM delay generation circuit is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

23.4.2 Notes on Delay Settings for PWM Delay Generation Circuit

When the PWM delay generation circuit generates delays for a PWM output waveform and the waveform is toggled in response to compare-matches, do not change the settings for delay while the compare-match value is within the ranges listed in Table 23.4. This constraint applies to the GTDLYFnA, GTDLYRnA, GTDLFnB, and GTDLYRnB registers.

Table 23.4 Constraints on delay settings

Mode	Direction of counting	Compare-match value
Saw-wave mode	Up	GTPR - 2 or above
	Down	2 or below
Triangle-wave mode	Down	2 or below

Figure 23.5 shows an example of how the constraints apply to the timing of setting GTDLYFnA in saw-wave waveform one-shot pulse mode (counting up). Do not change the value set in GTDLYFnA while GTCCRD ≥ GTPR - 2.

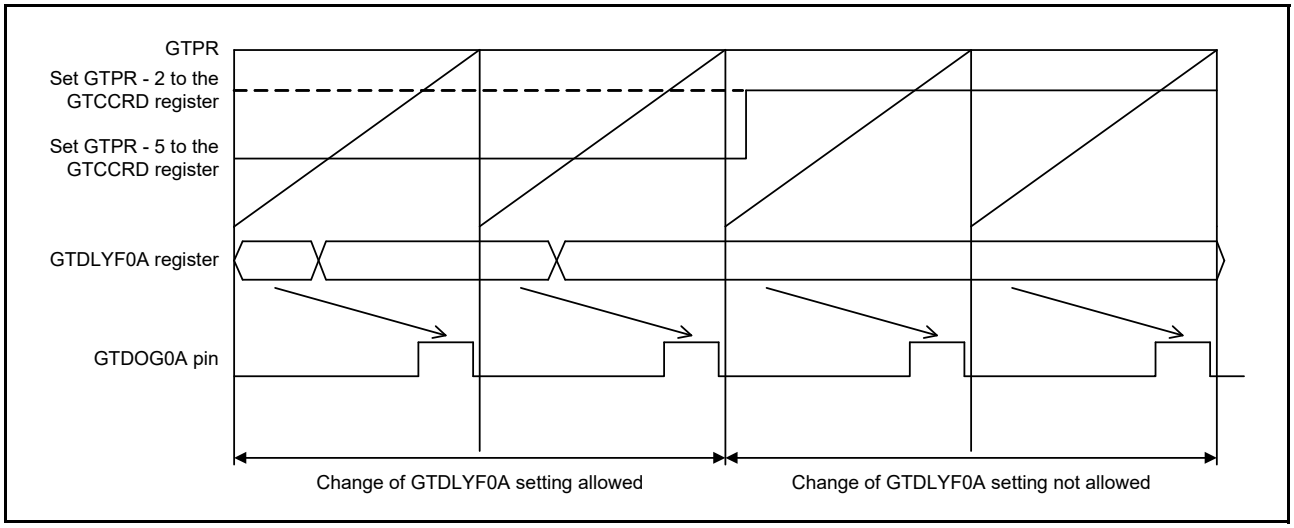


Figure 23.5 Constraints on the timing of GTDLYF0A register settings

Changing the values in the GTDLYFnA, GTDLYRnA, GTDLYFnB, and GTDLYRnB registers during periods where changes to settings are not allowed, might lead to faulty output waveforms such as shifts in the timing of output waveform transitions from the expected values.

24. Low Power Asynchronous General-Purpose Timer (AGT)

24.1 Overview

The Low Power Asynchronous General-Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events.

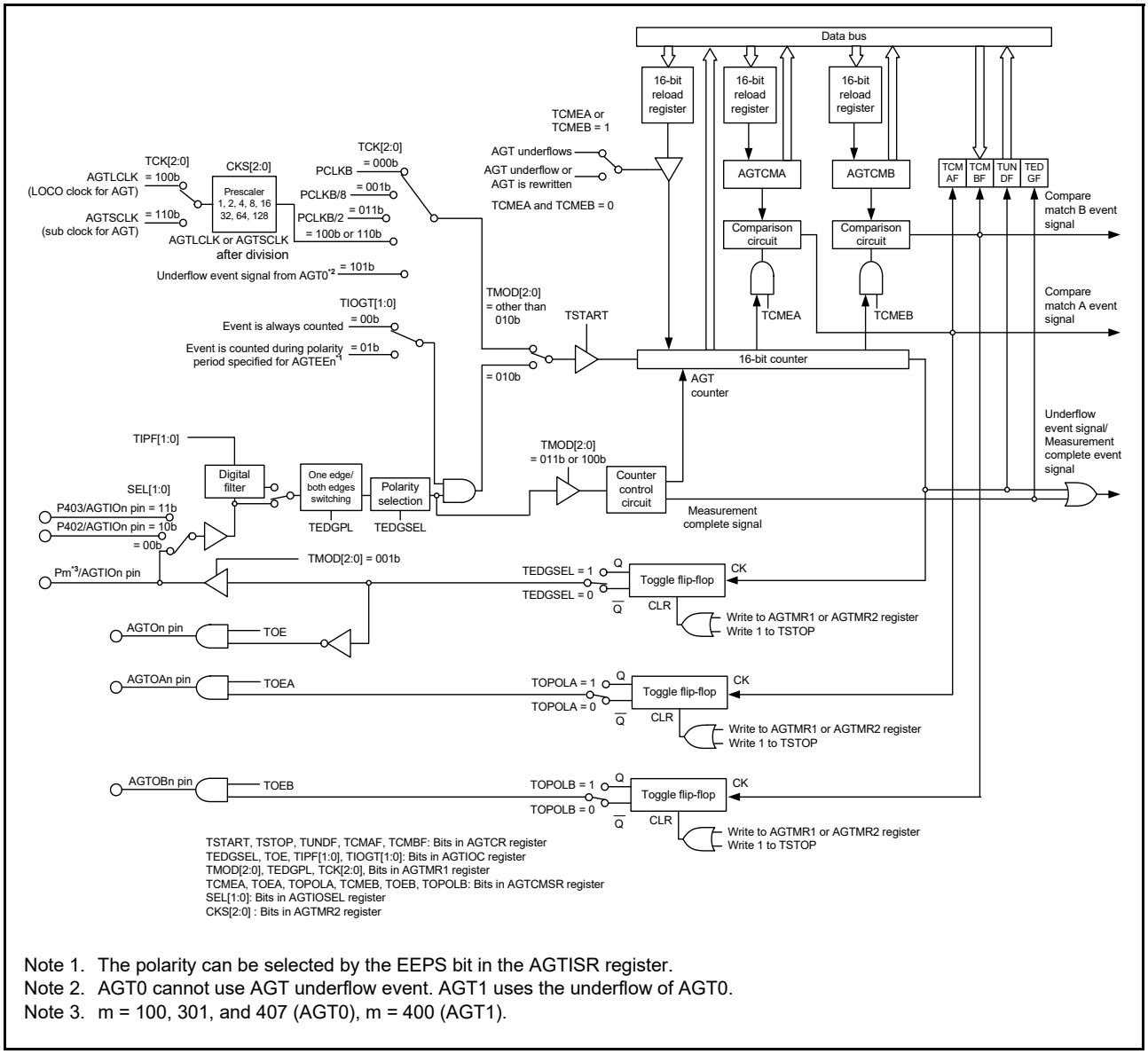
This 16-bit timer consists of a reload register and a down counter. The reload register and the down counter are allocated in the same address, and can be accessed with the AGT register.

Table 24.1 lists the AGT specifications, Figure 24.1 shows a block diagram, and Table 24.2 lists the I/O pins.

Table 24.1 AGT specifications

Parameter		Specifications
Operating modes	Timer mode	The count source is counted
	Pulse output mode	The count source is counted and the output is inverted at each timer underflow
	Event counter mode	An external event is counted
	Pulse width measurement mode	An external pulse width is measured
	Pulse period measurement mode	An external pulse period is measured
Count source (operating clock)*2		PCLKB, PCLKB/2, PCLKB/8, AGTLCLK, AGTLCLK/2, AGTLCLK/4, AGTLCLK/8, AGTLCLK/16, AGTLCLK/32, AGTLCLK/64, AGTLCLK/128, AGTSCLK, AGTSCLK/2, AGTSCLK/4, AGTSCLK/8, AGTSCLK/16, AGTSCLK/32, AGTSCLK/64, AGTSCLK/128, or underflow signal of AGT0*1 selectable.
Interrupt/event link function (output)		• Underflow event signal or measurement complete event signal – When the counter underflows – When the measurement of the active width of the external input (AGTIO) is complete in pulse width measurement mode – When the set edge of the external input (AGTIO) is input in pulse period measurement mode. • Compare match A event signal – When the values of AGT and AGTCMA matched (compare match A function enabled) • Compare match B event signal – When the values of AGT and AGTCMB matched (compare match B function enabled).
Selectable functions		• Compare match function One or two of the compare match A and B registers is selectable.

Note 1. AGT0 cannot use the AGT0 underflow signal. AGT1 connects directly with the underflow event signal from the AGT0 timer.
Note 2. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source clock.



Note 1. The polarity can be selected by the EEPS bit in the AGTISR register.
Note 2. AGT0 cannot use AGT underflow event. AGT1 uses the underflow of AGT0.
Note 3. m = 100, 301, and 407 (AGT0), m = 400 (AGT1).

Figure 24.1 AGT block diagram

Table 24.2 AGT I/O pins

Pin name	I/O	Function
AGTEEn	Input	External event input for AGT
AGTIOn*1	Input*1/output	External event input and pulse output for AGT
AGTOn	Output	Pulse output for AGT
AGTOAn	Output	Output compare match A output for AGT
AGTOBn	Output	Output compare match B output for AGT

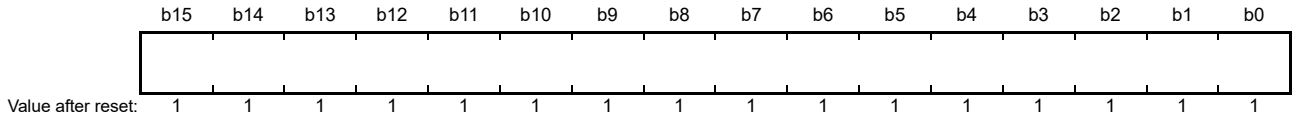
Note: Channel number (n = 0, 1).
Note 1. AGTIO can also be used in Deep Software Standby mode.

AGTIO can be controlled by the VBTICTLR register. For details, see section 19.2.7, AGT Input Control Register (VBTICTLR) and section 19.5.5, I/O Buffer Specification.

24.2 Register Descriptions

24.2.1 AGT Counter Register (AGT)

Address(es): AGT0.AGT 4008 4000h, AGT1.AGT 4008 4100h



Bit	Description	Setting range	R/W
b15 to b0	16-bit counter and reload register *1, *2	0000h to FFFFh	R/W

Note 1. When 1 is written to the TSTOP bit in the AGTCR register, the 16-bit counter is forcibly stopped and set to FFFFh.
Note 2. When the TCK[2:0] bit setting in the AGTMR1 register is a value other than 001b (PCLKB/8) or 011b (PCLKB/2), if the AGT register is set to 0000h, a request signal to the ICU, the DTC, and the ELC is generated once immediately after the count starts. The AGTOn and AGTIOn outputs are toggled.
When the AGT register is set to 0000h in event counter mode, regardless of the value of TCK[2:0] bits, a request signal to the ICU, the DTC, and the ELC is generated once immediately after the count starts.
In addition, the AGTOn output toggles even during a period other than the specified count period. When the AGT register is set to 0001h or more, a request signal is generated each time AGT underflows.

AGT is a 16-bit register. The write value is written to the reload register and the read value is read from the counter.

The states of the reload register and the counter change according to the TSTART bit in the AGTCR register and TCMEA/TCMEB bit in the AGTCMSR register. For details, see section 24.3.1, Reload Register and Counter Rewrite Operation. The AGT register can be set with a 16-bit memory manipulation instruction.

24.2.2 AGT Compare Match A Register (AGTCMA)

Address(es): AGT0.AGTCMA 4008 4002h, AGT1.AGTCMA 4008 4102h

Bit	Description	Setting range	R/W
b15 to b0	16-bit compare match A data is stored.*1	0000h to FFFFh	R/W

Note 1. Set the AGTCMA register to FFFFh when the compare match A is not used.

The AGTCMA register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register A change according to the TSTART bit in the AGTCR register. For details, see section 24.3.2, Reload Register and Compare Register A/B Rewrite Operation. The AGTCMA register can be set by a 16-bit memory manipulation instruction.

24.2.3 AGT Compare Match B Register (AGTCMB)

Address(es): AGT0.AGTCMB 4008 4004h, AGT1.AGTCMB 4008 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	Setting range	R/W
b15 to b0	16-bit compare match B data is stored.*1	0000h to FFFFh	R/W

Note 1. Set the AGTCMB register to FFFFh when compare match B is not used.

The AGTCMB register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register B change according to the TSTART bit in the AGTCR register. For details, see section 24.3.2, Reload Register and Compare Register A/B Rewrite Operation. The AGTCMB register can be set by a 16-bit memory manipulation instruction.

24.2.4 AGT Control Register (AGTCR)

Address(es): AGT0.AGTCR 4008 4008h, AGT1.AGTCR 4008 4108h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSTART	AGT Count Start*2	0: Count stops 1: Count starts.	R/W
b1	TCSTF	AGT Count Status Flag*2	0: Count stops 1: Count in progress.	R
b2	TSTOP	AGT Count Forced Stop*1	0: Writing is invalid 1: The count is forcibly stopped.	W
b3	—	Reserved	The read value is 0. The write value should be 0.	R/W
b4	TEDGF	Active Edge Judgment Flag	0: No active edge received 1: Active edge received.	R/(W)*3
b5	TUNDF	Underflow Flag	0: No underflow 1: Underflow.	R/(W)*3
b6	TCMAF	Compare Match A Flag	0: No match 1: Match.	R/(W)*3
b7	TCMBF	Compare Match B Flag	0: No match 1: Match.	R/(W)*3

Note 1. When 1 (count is forcibly stopped) is written to the TSTOP bit, the TSTART and TCSTF bits are initialized at the same time. The pulse output level is also initialized. The read value is 0.
Note 2. For information on using the TSTART and TCSTF bits, see section 24.4.1, Count Operation Start and Stop Control.
Note 3. Only 0 can be written to clear the flag.

TSTART bit (AGT Count Start*2)

The count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When this bit is set to 1 (count starts), the TCSTF bit is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count stopped) in synchronization with the count source. For details, see section 24.4.1, Count Operation Start and Stop Control.

TCSTF flag (AGT Count Status Flag*2)

The TCSTF flag indicates the AGT count status.

[Setting condition]

- When 1 is written to the TSTART bit (the TCSTF flag is set to 1 in synchronization with the count source).

[Clearing conditions]

- When 0 is written to the TSTART bit (the TCSTF flag is set to 0 in synchronization with the count source)
- When 1 is written to the TSTOP bit.

TSTOP bit (AGT Count Forced Stop*1)

When 1 is written to the TSTOP bit, the count is forcibly stopped. The read value is 0.

TEDGF flag (Active Edge Judgment Flag)

The TEDGF flag indicates that an active edge was detected.

[Setting condition]

- When the measurement of the active width of the external input (AGTIO) is complete in pulse width measurement mode
- When the set edge of the external input (AGTIO) is input in pulse period measurement mode.

[Clearing condition]

- When 0 is written to this flag by software.

TUNDF flag (Underflow Flag)

The TUNDF flag indicates that the counter underflowed.

[Setting condition]

- When the counter underflows.

[Clearing condition]

- When 0 is written to this flag by software.

TCMAF flag (Compare Match A Flag)

The TCMAF flag indicates that compare match A was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMA register.

[Clearing condition]

- When 0 is written to this flag by software.

TCMBF flag (Compare Match B Flag)

The TCMBF flag indicates that compare match B was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMB register.

[Clearing condition]

- When 0 is written to this flag by software.

24.2.5 AGT Mode Register 1 (AGTMR1)

Address(es): AGT0.AGTMR1 4008 4009h, AGT1.AGTMR1 4008 4109h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	TMOD[2:0]	Operating Mode*3	b2 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode. Other settings are prohibited.	R/W
b3	TEDGPL	Edge Polarity*4	0: Single-edge 1: Both-edge.	R/W
b6 to b4	TCK[2:0]	Count Source*1, *2, *5	b6 b4 0 0 0: PCLKB 0 0 1: PCLKB/8 0 1 1: PCLKB/2 1 0 0: Divided clock AGTLCLK specified in CKS[2:0] bits in AGTMR2 register 1 0 1: Underflow event signal from AGT0*6 1 1 0: Divided clock AGTSCLK specified in CKS[2:0] bits in AGTMR2 register. Other settings are prohibited.	R/W
b7	—	Reserved	The read value is 0. The write value should be 0.	R/W

Note: Write access to the AGTMR1 register initializes the output from the AGTOn, AGTIOn, AGTOAn and AGTOBn pins of the AGT (n = 0, 1). For details on the output level at initialization, see section 24.2.7, AGT I/O Control Register (AGTIOC).

Note 1. When event counter mode is selected, the external input (AGTIOn) is selected as the count source regardless of the setting of TCK[2:0] bits.

Note 2. Do not switch count sources during count operation. Only switch count sources when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped).

Note 3. The operating mode can only be changed when the count is stopped while both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped). Do not change the operating mode during count operation.

Note 4. The TEDGPL bit is enabled only in event counter mode.

Note 5. When running AGT in Software Standby and Deep Software Standby modes, set AGTSCLK or AGTLCLK (TCK[2:0] = 100b or 110b) as the count source.

Note 6. AGT0 cannot use AGT0 underflow (setting prohibited). AGT1 uses the AGT0 underflow.

24.2.6 AGT Mode Register 2 (AGTMR2)

Address(es): AGT0.AGTMR2 4008 400Ah, AGT1.AGTMR2 4008 410Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	LPM	—	—	—	—	CKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKS[2:0]	AGTSCLK/AGTLCLK Count Source Clock Frequency Division Ratio *1, *2, *3	b2 b0 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	LPM	Low Power Mode	0: Normal mode 1: Low power mode.	R/W

Note 1. Do not rewrite CKS[2:0] during count operation. Only rewrite the CKS[2:0] bits when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped).
Note 2. When count source is AGTSCLK/AGTLCLK, the switch of CKS[2:0] is valid.
Note 3. Do not switch the TCK[2:0] bits in the AGTMR1 register when CKS[2:0] are not 000b. Switch the TCK[2:0] bits in the AGTMR1 register after CKS[2:0] are set to 000b, and wait for 1 cycle of the count source.

LPM bit (Low Power Mode)

The LPM bit sets the low power operation, which impacts access to certain AGT registers. Set this bit to 1 to operate in low power. When this bit is 1, access to the following registers is prohibited:

- AGT/AGTCMA/AGTCMB/AGTCR.

After this bit is switched from 1 to 0, the first access to the register is constrained as follows:

- AGT — Read AGT register twice. Only the second reading of data is valid.
- AGT, AGTCMA, AGTCMB, and AGTCR — Allow at least 2 cycles of the count source clock when writing to the register.

24.2.7 AGT I/O Control Register (AGTIOC)

Address(es): AGT0.AGTIOC 4008 400Ch, AGT1.AGTIOC 4008 410Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDGSEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TEDGSEL	I/O Polarity Switch	Function varies depending on the operating mode. See Table 24.3 and Table 24.4. The TEDGSEL bit switches the AGTO output polarity and the AGTIO input/output edge and polarity. In pulse output mode, it only controls the polarity of AGTOn and AGTIOn output. The AGTOn and AGTIOn output are initialized when the AGTMR1 register is written and the TSTOP bit in the AGTCR register is written with 1.	R/W

Bit	Symbol	Bit name	Description	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	TOE	AGTOn Output Enable	0: AGTOn output disabled 1: AGTOn output enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5, b4	TIPF[1:0]	Input Filter*3	b5 b4 0 0: No filter 0 1: Filter sampled at PCLKB 1 0: Filter sampled at PCLKB/8 1 1: Filter sampled at PCLKB/32. These bits specify the sampling frequency of the filter for the AGTIOn input. If the input to the AGTIOn pin is sampled and the value matches three successive times, that value is taken as the input value.	R/W
b7, b6	TIOGT[1:0]	Count Control*1,*2,*4	b7 b6 0 0: Event is always counted 0 1: Event is counted during polarity period specified for AGTEEn. Other settings are prohibited.	R/W

Note 1. When AGTEEn pin is used, the polarity to count an event can be selected with the EEPS bit in the AGTISR register.
Note 2. TIOGT[1:0] bits are enabled only in event counter mode.
Note 3. When event counter mode operation is performed during Software Standby and Deep Software Standby modes, the digital filter function cannot be used.
Note 4. When using in Deep Software Standby mode, set TIOGT[1:0] = 00b (event is always counted).

Table 24.3 AGTIOn I/O edge and polarity switching

Operating mode	Function
Timer mode	Not used
Pulse output mode	0: Output is started at high (initialization level: high) 1: Output is started at low (initialization level: low).
Event counter mode	0: Count on rising edge 1: Count on falling edge.
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge.

Table 24.4 AGTOn output polarity switching

Operating mode	Function
All modes	0: Output is started at low (initialization level: low) 1: Output is started at high (initialization level: high).

24.2.8 AGT Event Pin Select Register (AGTISR)

Address(es): AGT0.AGTISR 4008 400Dh, AGT1.AGTISR 4008 410Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	EEPS	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	EEPS	AGTEEn Polarity Selection	0: An event is counted during the low-level period 1: An event is counted during the high-level period.	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

24.2.9 AGT Compare Match Function Select Register (AGTCMSR)

Address(es): AGT0.AGTCMSR 4008 400Eh, AGT1.AGTCMSR 4008 410Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TCMEA	Compare Match A Register Enable*1, *2	0: Compare match A register disabled 1: Compare match A register enabled.	R/W
b1	TOEA	AGTOAn Output Enable*1, *2	0: AGTOAn output disabled 1: AGTOAn output enabled.	R/W
b2	TOPOLA	AGTOAn Polarity Select*1, *2	0: AGTOAn output is started on low 1: AGTOAn output is started on high.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	TCMEB	Compare Match B Register Enable*1, *2	0: Compare match B register disabled 1: Compare match B register enabled.	R/W
b5	TOEB	AGTOBn Output Enable*1, *2	0: AGTOBn output disabled 1: AGTOBn output enabled.	R/W
b6	TOPOLB	AGTOBn Polarity Select*1, *2	0: AGTOBn output is started on low 1: AGTOBn output is started on high.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite the AGTCMSR register during a count operation. Only rewrite the AGTCMSR register when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped).
Note 2. Do not set to 1 when in pulse width measurement mode or pulse period measurement mode.

24.2.10 AGT Pin Select Register (AGTIOSEL)

Address(es): AGT0.AGTIOSEL 4008 400Fh, AGT1.AGTIOSEL 4008 410Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TIES	—	—	SEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	SEL[1:0]	AGTIO Pin Select*1, *3	b1 b0 0 0: Select Pm*2/AGTIO as AGTIO Pm/AGTIO cannot be used as AGTIO input pin in Deep Software Standby mode. 0 1: Setting prohibited 1 0: Select P402/AGTIO as AGTIO P402/AGTIO can be used as AGTIO input pin in Deep Software Standby mode. P402/AGTIOn is input only. It cannot be used for output. 1 1: Select P403/AGTIO as AGTIO. P403/AGTIO can be used as AGTIO input pin in Deep Software Standby mode. P403/AGTIOn is input only. It cannot be used for output.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b4	TIES	AGTIO Input Enable	0: External event input is disabled during Software Standby mode 1: External event input is enabled during Software Standby mode.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. P402/AGTIO and P403/AGTIO can be used as external event input pins for the AGT in Deep Software Standby mode. Pm*2/AGTIO cannot be used as external event input pins for the AGT in Deep Software Standby mode. P402/AGTIO and P403/AGTIO are input only.
When Pm/AGTIO is selected, you must set the Port mn Pin Function Select (PmnPFS) register. See section 19, I/O Ports.
Note 2. m = 100, 301, and 407 (AGT0), m = 400 (AGT1).
Note 3. When P402/AGTIO and P403/AGTIO are selected, you must set the VBTICTLR register. See section 19.2.7, AGT Input Control Register (VBTICTLR).

The AGTIOSEL register sets the AGTIO pin when using the AGTIO in Deep Software Standby mode and Software Standby mode. The AGTIOSEL register can be set with an 8-bit memory manipulation instruction.

SEL[1:0] bits (AGTIO Pin Select*1, *3)

The SEL[1:0] bits select the AGTIO pin function.

TIES bit (AGTIO Input Enable)

The TIES bit enables or disables an external event input.

24.3 Operation

24.3.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value of the TSTART bit in the AGTCR register and of the TCMEA and TCMEB bit in the AGTCMSR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTART bit is 1 (count starts) and the TCMEA and TCMEB bits are 0 (compare match A/B registers are invalid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source. When the TSTART bit is 1 (count starts) and the TCMEA or TCMEB bit is 1 (compare match A register or compare match B register is valid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the underflow of the counter.

Figure 24.2 and Figure 24.3 show the timing of rewrite operation with TSTART bit value and TCMEA/TCMEB bit value.

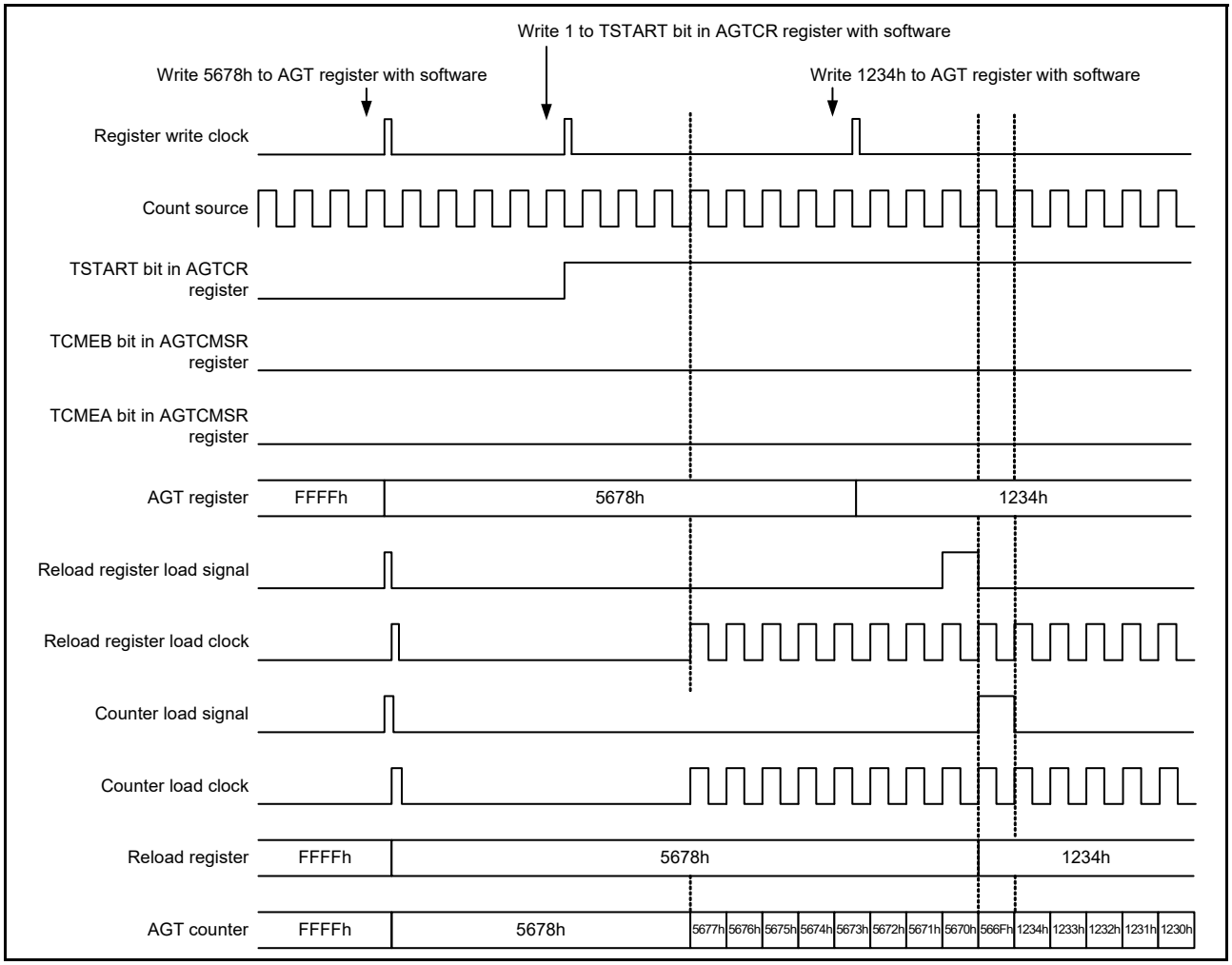


Figure 24.2 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when compare match register A or compare match B register is invalid

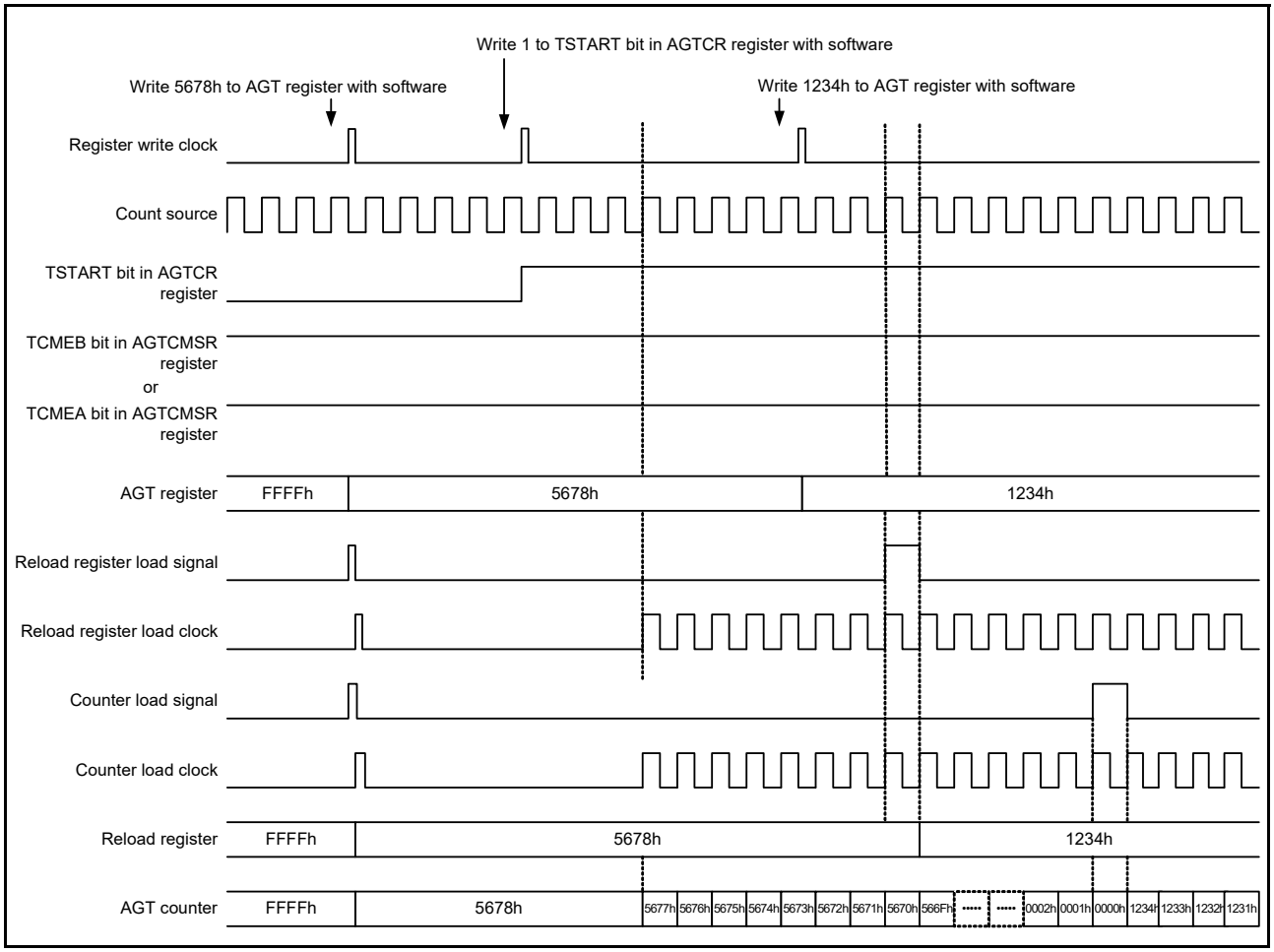


Figure 24.3 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when compare match register A or compare match B register is valid

24.3.2 Reload Register and Compare Register A/B Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to compare register A/B depends on the value of the TSTART bit in the AGTCR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and compare register A/B. When the TSTART bit is 1 (count starts), the value is written to the reload register in synchronization with the count source, and then to the compare register in synchronization with the underflow of the counter.

Figure 24.4 shows the timing of rewrite operation with TSTART bit value for compare register A. Compare register B has the same timing as compare register A.

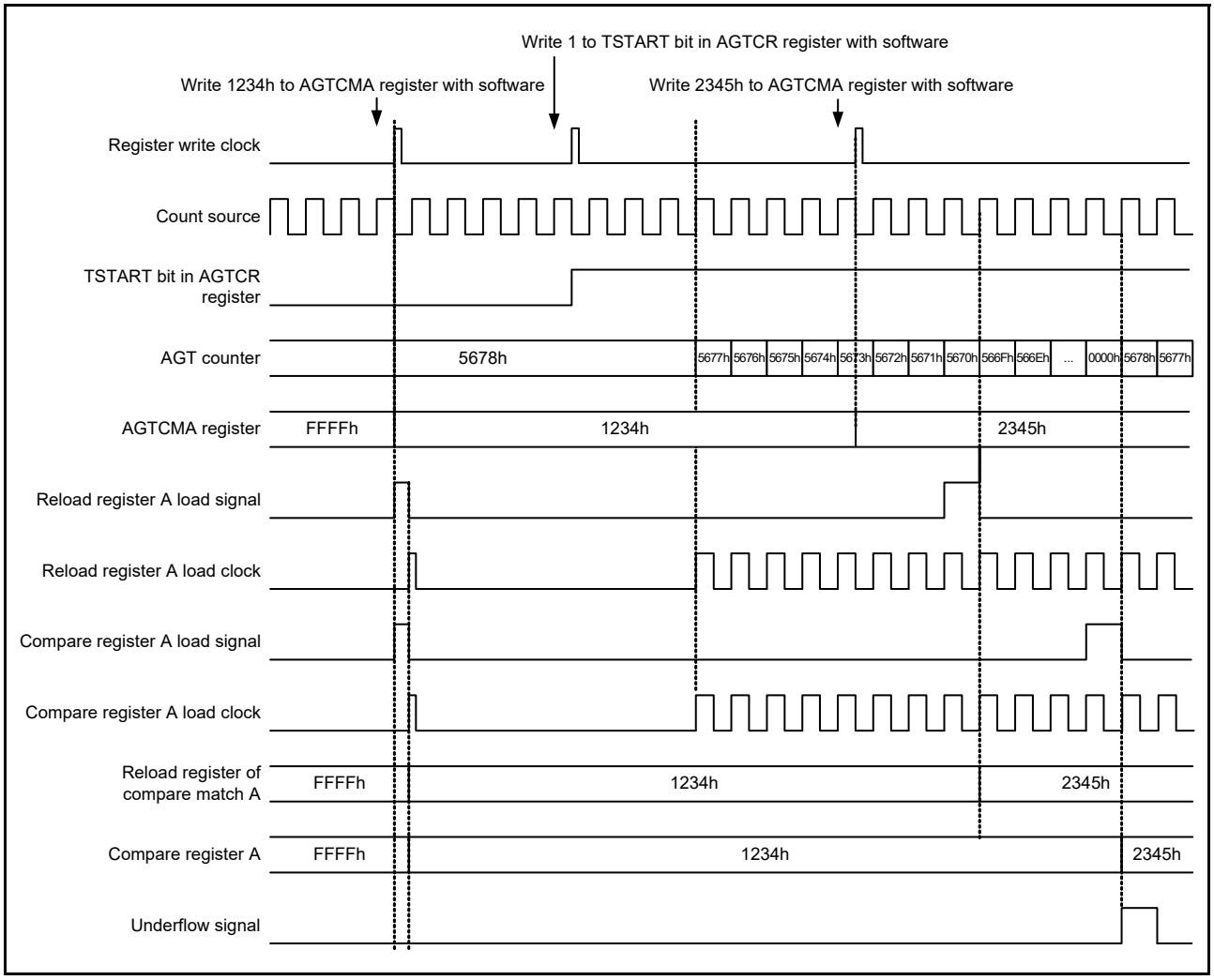


Figure 24.4 Timing of rewrite operation with the TSTART bit value for compare register A

24.3.3 Timer Mode

In timer mode, the AGT counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. In timer mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0000h and the next count source is input, an underflow occurs and an interrupt request is generated.

Figure 24.5 shows the operation example in timer mode.

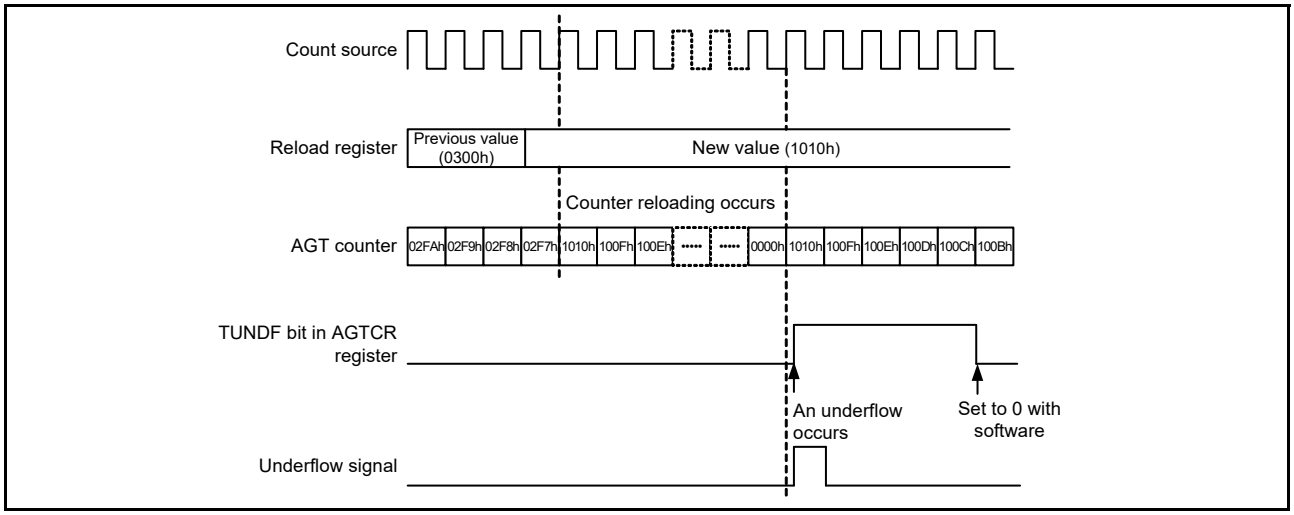


Figure 24.5 Operation example in timer mode

24.3.4 Pulse Output Mode

In pulse output mode, the counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and the output level of the AGTIOn and AGTOn pins is inverted each time an underflow occurs.

In pulse output mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0000h and the next count source is input, an underflow occurs and an interrupt request is generated. In addition, a pulse can be output from the AGTIOn and AGTOn pins. The output level is inverted each time an underflow occurs. The pulse output from the AGTOn pin can be stopped with the TOE bit in the AGTIOC register. The output level can be selected with the TEDGSEL bit in the AGTIOC register.

Figure 24.6 shows the operation example in pulse output mode.

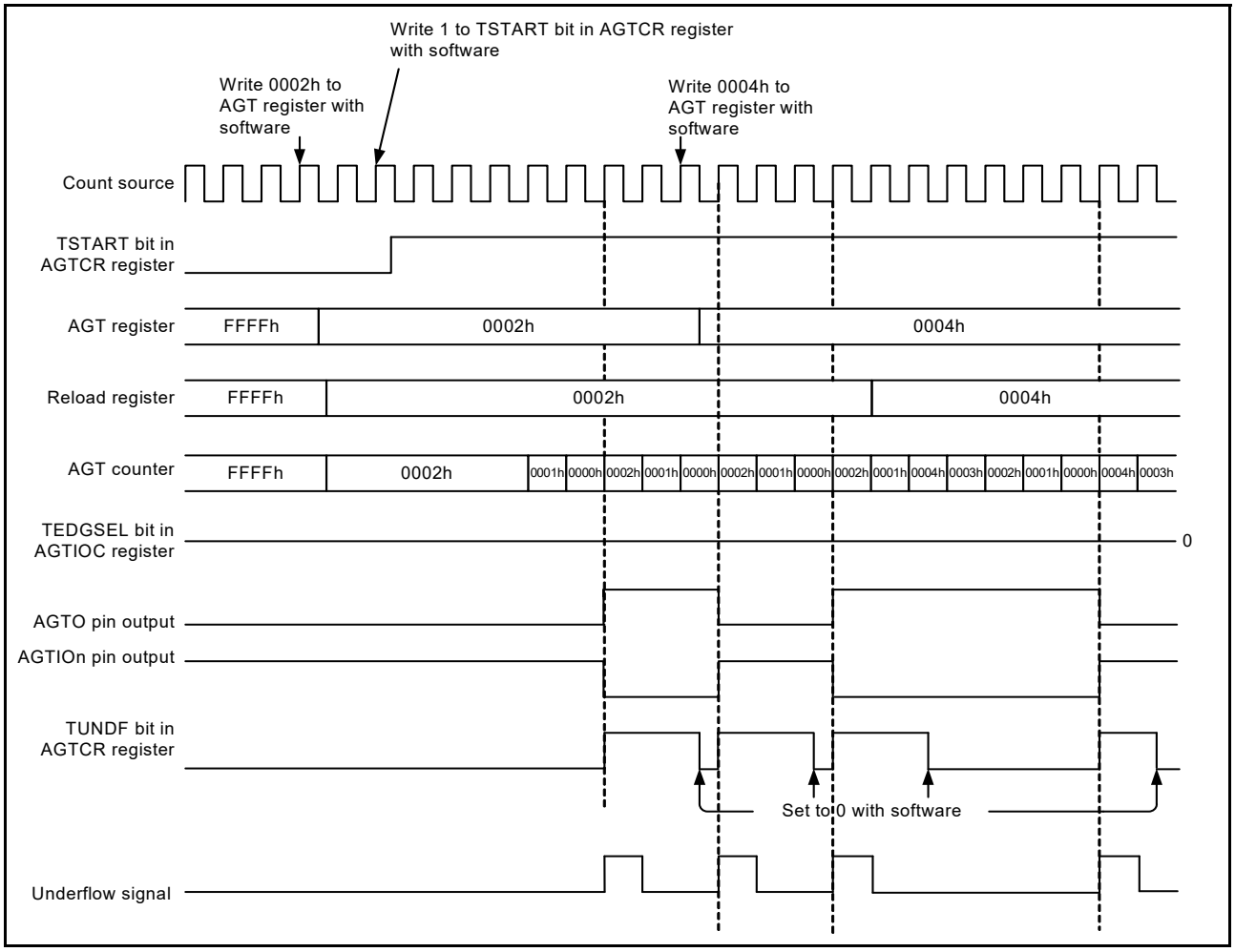


Figure 24.6 Operation example in pulse output mode

24.3.5 Event Counter Mode

In event counter mode, the counter is decremented by an external event signal (count source) input to the AGTIOn pin. Various periods for counting events can be set with the TIOGT[1:0] bits in the AGTIOC and AGTISR registers. In addition, the filter function for the AGTIOn input can be specified with the TIPF[1:0] bits in the AGTIOC register. The output from the AGTOn pin can be toggled even in event counter mode.

Figure 24.7 shows the operation example in event counter mode.

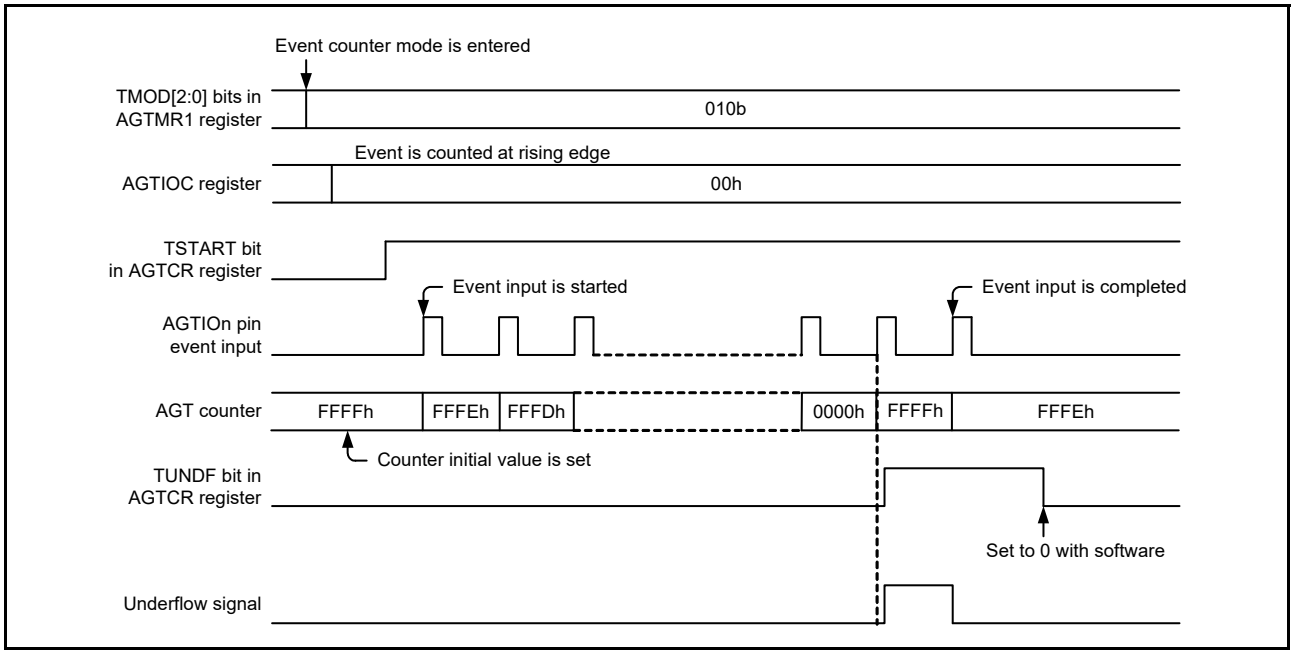
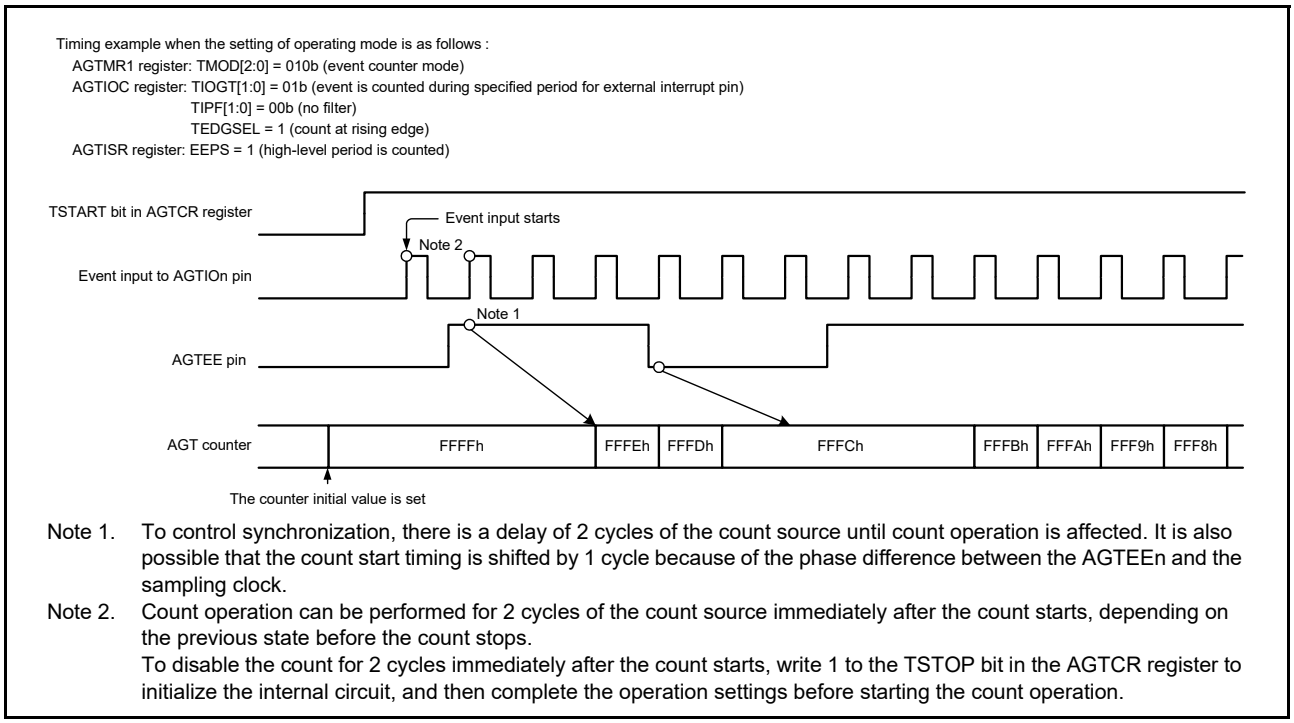


Figure 24.7 Operation example 1 in event counter mode

Figure 24.8 shows an operation example for counting during the specified period in event counter mode (TIOGT[1:0] bits in the AGTIOC register are set to 01b).



Note 1. To control synchronization, there is a delay of 2 cycles of the count source until count operation is affected. It is also possible that the count start timing is shifted by 1 cycle because of the phase difference between the AGTEEn and the sampling clock.

Note 2. Count operation can be performed for 2 cycles of the count source immediately after the count starts, depending on the previous state before the count stops.
To disable the count for 2 cycles immediately after the count starts, write 1 to the TSTOP bit in the AGTCR register to initialize the internal circuit, and then complete the operation settings before starting the count operation.

Figure 24.8 Operation example 2 in event counter mode

24.3.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the AGTIOn pin is measured. When the level specified in the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. When the specified level on the AGTIOn pin ends, the counter is stopped, the TEDGF bit in the AGTCR register is set to 1 (active edge received), and an interrupt request is generated. The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when the counter underflows during measurement, the TUNDF bit in the AGTCR register is set to 1 and an interrupt request is generated.

Figure 24.9 shows the operation example in pulse width measurement mode.

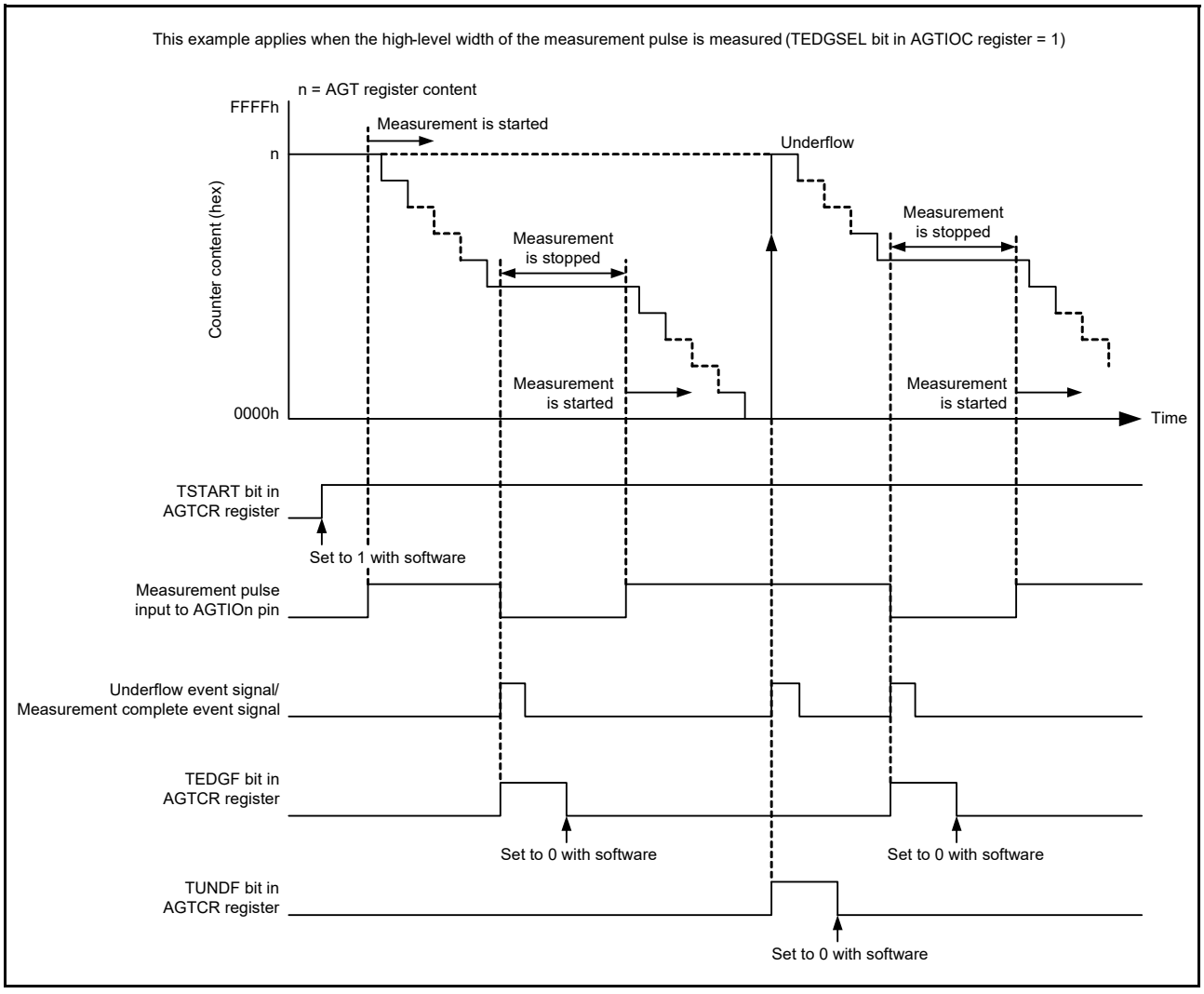


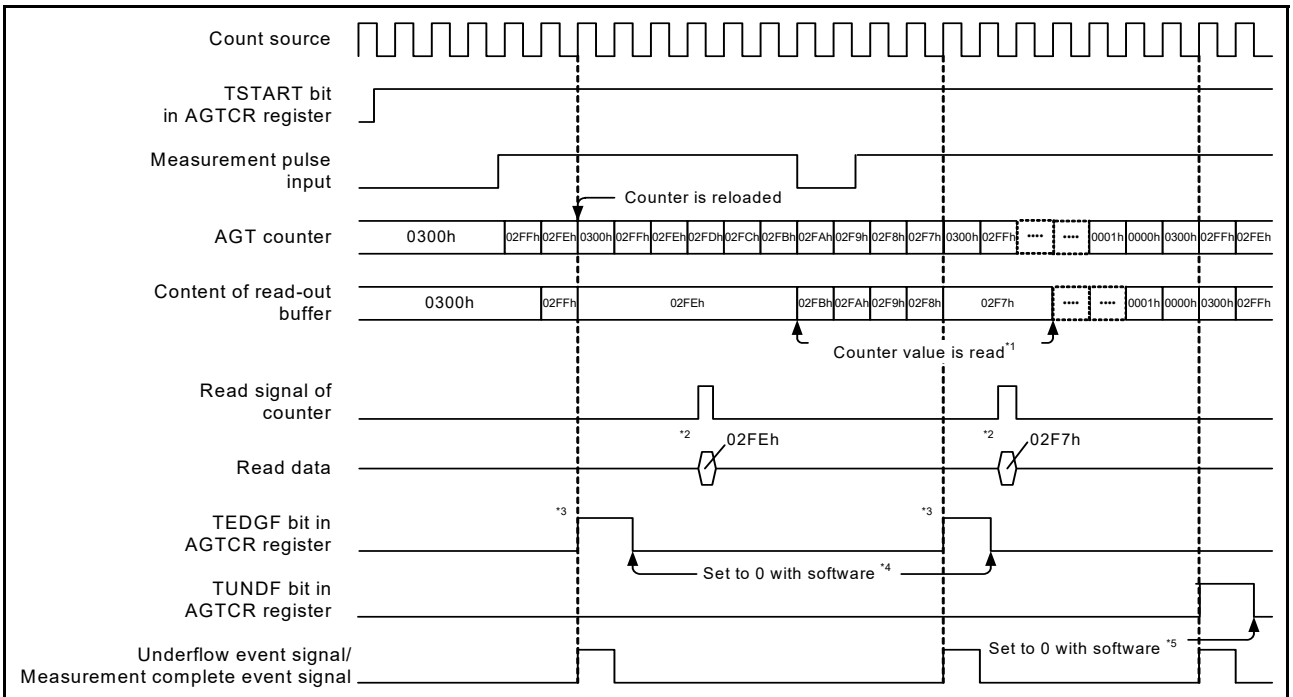
Figure 24.9 Operation example in pulse width measurement mode

24.3.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the AGTIOn pin is measured. The counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. When a pulse with the level specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the count value is transferred to the read-out buffer on the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge. Simultaneously, the TEDGF bit in the AGTCR register is set to 1 (active edge received) and an interrupt request is generated. The read-out buffer (AGT register) is read at this time and the difference from the reload value (see section 24.4.5, How to Calculate Event Number, Pulse Width, and Pulse Period) is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF bit in the AGTCR register is set to 1 (underflow) and an interrupt request is generated.

Figure 24.10 shows the operation example in pulse period measurement mode.

Only input pulses with a period longer than twice the period of the count source are measured. Also, the low-level and high-level widths must both be longer than the period of the count source. If a pulse period shorter than these conditions is input, the input might be ignored.



This example applies when the initial value of the AGT register is set to 0300h, the TEDGSEL bit in the AGTIOC register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.

Note 1. Reading from the AGT register must be performed during the period from when the TEDGF bit is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the AGT register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
Note 2. When the AGT register is read in pulse period measurement mode, the content of the read-out buffer is read.
Note 3. When the active edge of the measurement pulse is input and then the set edge of an external pulse is input, the TEDGF bit in the AGTCR register is set to 1 (active edge received).
Note 4. To set to 0 with software, write 0 to the TEDGF bit in the AGTCR register using an 8-bit memory manipulation instruction.
Note 5. To set to 0 with software, write 0 to the TUNDF bit in the AGTCR register using an 8-bit memory manipulation instruction.

Figure 24.10 Operation example in pulse period measurement mode

24.3.8 Compare Match Function

The compare match function detects matches (compare match) between the content of the AGTCMA or AGTCMB register and the content of the AGT register. This function is enabled when the TCMEA or TCMEB bit in the AGTCMSR register is 1 (compare match A register or compare match B register is valid). The counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and when the values of AGT and AGTCMA or AGTCMB match, the TCMAF/TCMBF bit in the AGTCR register is set to 1 (match), and an interrupt request is generated.

When compare match function is enabled, the timing of the rewrite operation to the reload register and the counter differs. See section 24.3.1, Reload Register and Counter Rewrite Operation for details. In addition, the output level of the AGTOAn and AGTOBn pins is inverted by the match and by the underflow. The output level can be selected with the TOPOLA or TOPOLB bit in the AGTCMSR register.

Figure 24.11 shows the operation example in compare match mode.

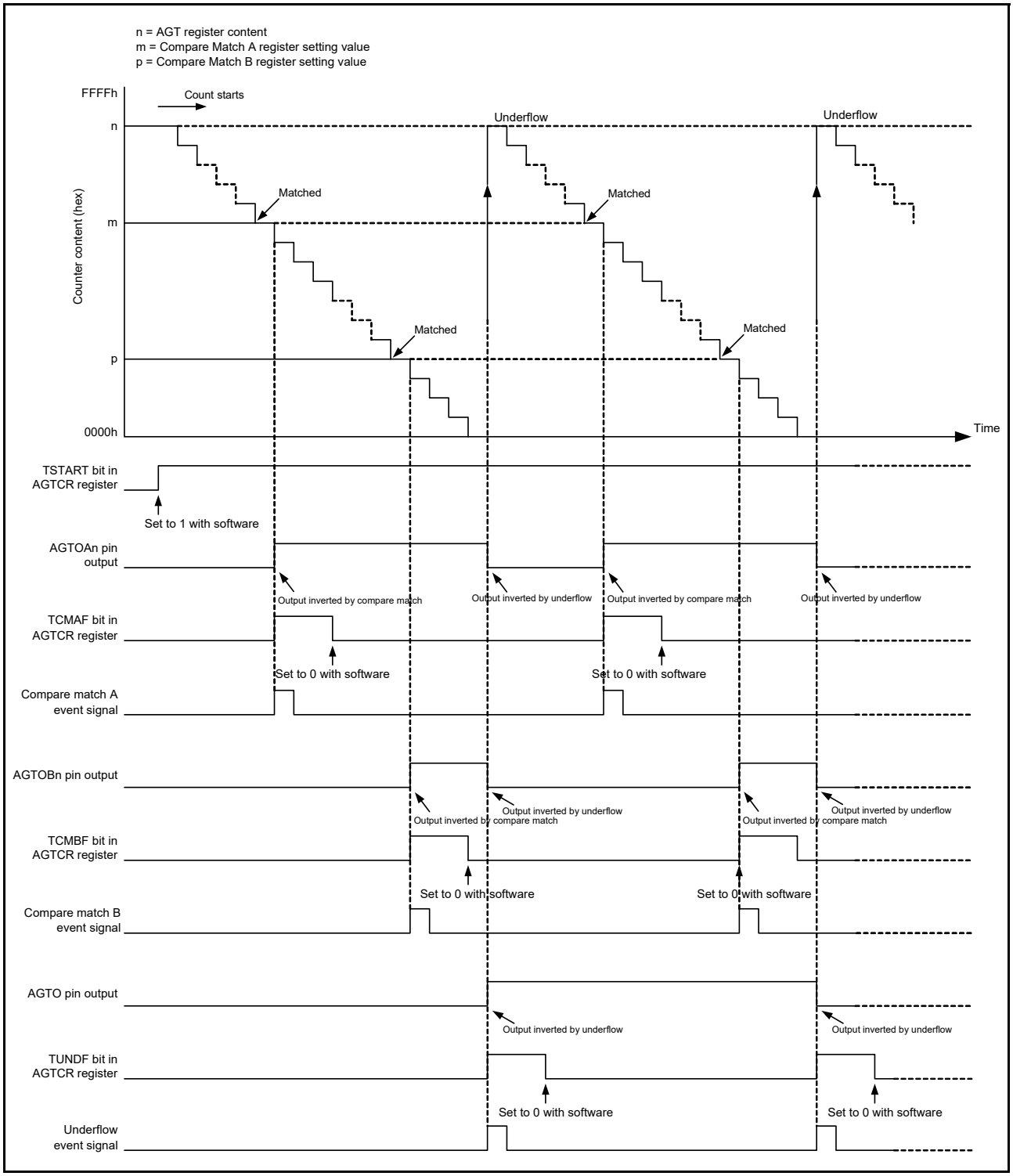


Figure 24.11 Operation example in compare match mode (TOPOLA = 0, TOPOLB = 0)

24.3.9 Output Settings for Each Mode

Table 24.5 to Table 24.8 list the states of pins AGTOn, AGTIOn, AGTOAn, and AGTOBn in each mode.

Table 24.5 AGTOn pin setting

	AGTIOC register		
Operating mode	**TOE bit**	**TEDGSEL bit**	**AGTOn pin output**
All modes	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled

Table 24.6 AGTIOn pin setting

	AGTIOC register	
Operating mode	**TEDGSEL bit**	**AGTIOn pin I/O**
Timer mode	0 or 1	Input (not used)
Pulse output mode	1	Normal output
	0	Inverted output
Event counter mode	0 or 1	Input
Pulse width measurement mode		
Pulse period measurement mode		

Table 24.7 AGTOAn pin setting

	AGTCMSR register		
Operating mode	**TOEA bit**	**TOPOLA bit**	**AGTOAn pin output**
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

Table 24.8 AGTOBn pin setting (1 of 2)

	AGTCMSR register		
Operating mode	**TOEB bit**	**TOPOLB bit**	**AGTOBn pin output**
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)

Table 24.8 AGTOBn pin setting (2 of 2)

Operating mode	AGTCMSR register TOEB bit	TOPOLB bit	AGTOBn pin output
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

24.3.10 Standby Mode

The AGT can operate in Software Standby and Deep Software Standby modes. Set it to Software Standby mode or Deep Software Standby mode with count operation start (TSTART = 1, TCSTF = 1).

Table 24.9 and Table 24.10 show the settings that can be used in Software Standby and Deep Software Standby modes.

Table 24.9 Usable settings in Software Standby and Deep Software Standby modes (AGT0)

Operating mode	TCK[2:0] bits of AGTMR1 register	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b	AGTLCLK or AGTSCLK	—
Pulse output mode	100b or 110b	AGTLCLK or AGTSCLK	—
Event counter mode	- (Invalid)	AGTIOn	—
Pulse width measurement mode	100b or 110b	AGTLCLK or AGTSCLK	—
Pulse period measurement mode	100b or 110b	AGTLCLK or AGTSCLK	—

Table 24.10 Usable settings in Software Standby and Deep Software Standby modes (AGT1)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Pulse output mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Event counter mode	— (invalid)	AGTIOn	• Underflow • Compare match A/B
Pulse width measurement mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge
Pulse period measurement mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge

Note: Release of Software Standby mode or Deep Software Standby mode is only AGT1.
Note 1. Only when AGT0 operates in Table 24.9.

24.3.11 Interrupt Sources

The AGT has three interrupt sources described in Table 24.11.

Table 24.11 AGT interrupt sources

Name	Interrupt source	DMAC/DTC activation
AGTn_AGTI	• When the counter underflows • When measurement of the active width of the external input (AGTIO) is complete in pulse width measurement mode • When the set edge of the external input (AGTIO) is input in pulse period measurement mode.	Possible
AGTn_AGTCMAI	When the values of AGT and AGTCMA match	Possible
AGTn_AGTCMBI	When the values of AGT and AGTCMB match	Possible

Note: Channel number (n = 0 or 1).

24.3.12 Event Signal Output to ELC

The AGT uses the Event Link Controller (ELC) to perform a link operation to a specified module using the interrupt request signal as the event signal. The AGT outputs compare match A, compare match B, and underflow/measurement complete signals as event signals. For details, see section 18, Event Link Controller (ELC).

24.4 Usage Notes

24.4.1 Count Operation Start and Stop Control

- When the operating mode (see Table 24.1) is set to other than the event counter mode, or the count source is set to other than AGT0 underflow (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF bit in the AGTCR register remains 0 (count stops) for 3 cycles of the count source. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for 3 cycles of the count source. When the TCSTF bit is set to 0, the count stops. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 0.
  - Clear the interrupt register before changing the TSTART bit from 0 to 1. See section 13, Interrupt Controller Unit (ICU) for details.

Note 1. Registers associated with AGT: AGT, AGTCMA, AGTCMB, AGTCR, AGTMR1, AGTMR2, AGTIOC, AGTISR, and AGTCMSR.

- When the operating mode (see Table 24.1) is set to event counter mode, or the count source is set to AGT0 underflow (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF bit in the AGTCR register remains 0 (count stops) for 2 PCLKB cycles. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for 2 cycles of the PCLKB. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 0.
  - Clear the interrupt register before changing the TSTART bit from 0 to 1. See section 13, Interrupt Controller Unit (ICU) for details.

Note 1. Registers associated with AGT: AGT, AGTCMA, AGTCMB, AGTCR, AGTMR1, AGTMR2, AGTIOC, AGTISR and AGTCMSR.

24.4.2 Access to Counter Register

When the TSTART and TCSTF bits in the AGTCR register are both 1 (count starts), allow at least 3 cycles of the count source clock between writes when writing to the AGT register successively.

24.4.3 When Changing Mode

The registers associated with AGT operating mode (AGTMR1, AGTMR2, AGTIOC, AGTISR, AGTCMSR and AGTIOC) can be changed only when the count is stopped with both the TSTART and TCSTF bits set to 0 (count stops). Do not change these registers during count operation.

When the registers associated with AGT operating mode are changed, the values of bits TEDGF, TUNDF, TCMAF and TCMBF are undefined. Before starting the count, write 0 to the following bits:

- TEDGF (no active edge received)
- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

24.4.4 Digital Filter

When using the digital filter, do not start the timer operation for 5 cycles of the digital filter clock after setting TIPF[1:0] bits and when the TEDGSEL bit in the AGTIOC register changes.

24.4.5 How to Calculate Event Number, Pulse Width, and Pulse Period

- In event counter mode, event number is expressed mathematically as follows:
  Event number = initial value of counter [AGT register] - counter value of active event end
- In pulse width measurement mode, pulse width is expressed mathematically as follows:
  Pulse width = counter value of stopping measurement - counter value of next stopping measurement
- In pulse period measurement mode, input pulse period is expressed mathematically as follows:
  Period of input pulse = (initial value of counter [AGT register] - reading value of the read-out buffer) + 1

24.4.6 When Count Is Forcibly Stopped by TSTOP Bit

After the counter is forcibly stopped by the TSTOP bit in the AGTCR register, do not access the following I/O registers for 1 cycle of the count source:

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

24.4.7 When Selecting AGT0 Underflow as the Count Source

Operate the AGT according to the procedures described in this section when selecting the underflow signal of AGT as the count source.

(1) Procedure for starting operation

1. Set AGT0 and AGT1.
2. Start the count operation of AGT1.
3. Start the count operation of AGT0.

(2) Procedure for stopping operation

1. Stop the count operation of AGT0.
2. Stop the count operation of AGT1.
3. Stop the count source clock of AGT1 (write 000b in the AGT1.AGTMR1.TCK[2:0] bits).

24.4.8 Reset of I/O Register

The I/O register of the AGT is not initialized by different types of resets. For details, see section 6, Resets.

24.4.9 When Selecting PCLKB, PCLKB/8, or PCLKB/2 as the Count Source

When a reset is generated, the operation of AGT cannot be guaranteed. Set the registers associated with AGT again.

24.4.10 When Selecting AGTSCLK or AGTLCLK as the Count Source

The MSTPD2 bit in the MSTPCRD register must be set to 1 except when accessing the AGT1 registers. The MSTPD3 bit in the MSTPCRD register must be set to 1 except when accessing the AGT0 registers. When a reset occurs while MSTPD2 or MSTPD3 bit is 0, the operation of AGT1 or AGT0 cannot be guaranteed. Set the registers associated with AGT again.

24.4.11 When Switching Source Clock

When switching a clock source by changing SCKSCR.CKSEL[2:0], the clock output from the selector stops for 4 cycles of the switched clock. Therefore, when using the AGTIO, AGTEE, or both input as external event input, the clock source should not be switched. If switching the clock source while using the external event input, extend the input pulse width by 4 clock cycles of the switched source clock cycles.

25. Watchdog Timer (WDT)

25.1 Overview

The Watchdog Timer (WDT) is a 14-bit down-counter and can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt. The refresh-permitted period can be set to refresh the counter and to detect when the system runs out of control.

Table 25.1 lists the WDT specifications and Figure 25.1 shows a block diagram.

Table 25.1 WDT specifications

Parameter	Specifications
Count source	Peripheral clock (PCLKB)
Clock division ratio	Division by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Auto start mode: Counting automatically starts after a reset, or after an underflow or refresh error occurs • Register start mode: Counting is started with a refresh by writing to the WDTRR register.
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated.
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
WDT reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading of the counter value	The down-counter value can be read by the WDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output.

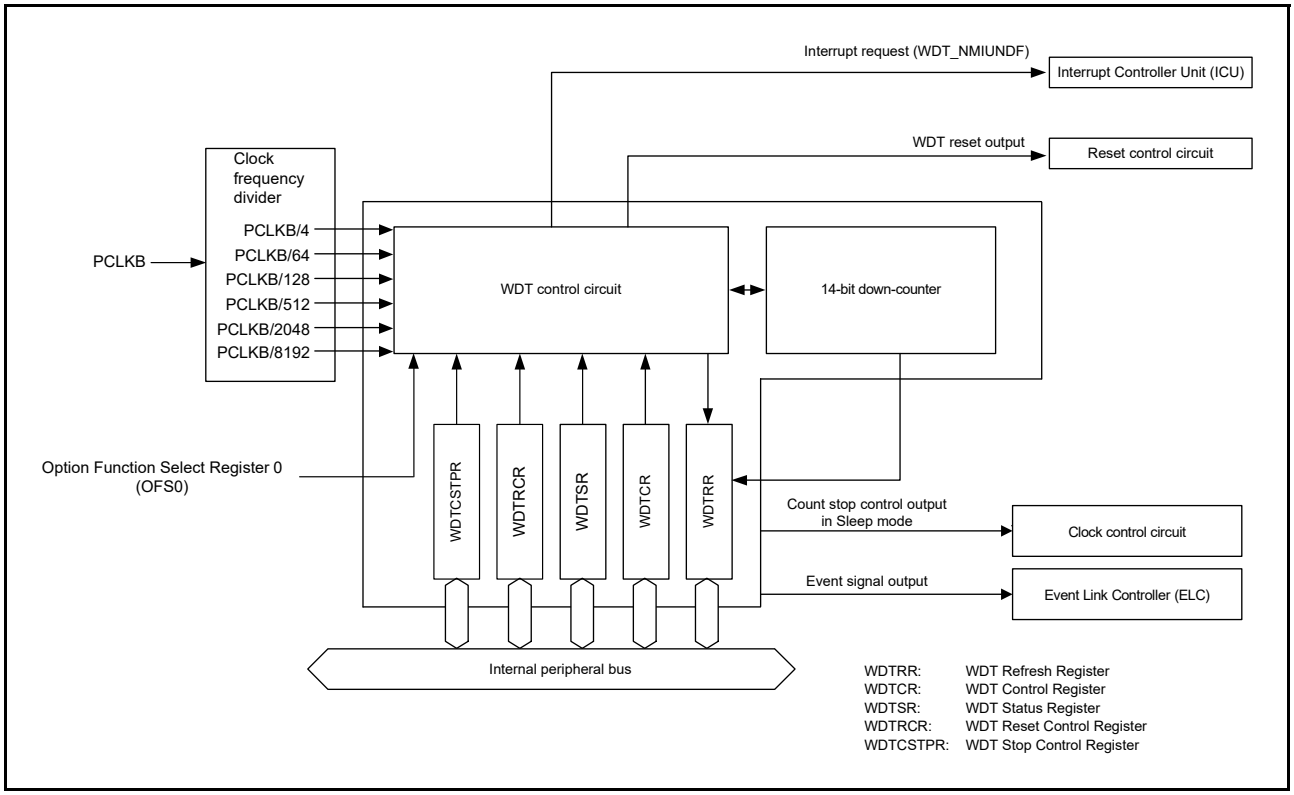


Figure 25.1 WDT block diagram

25.2 Register Descriptions

25.2.1 WDT Refresh Register (WDTRR)

Address(es): WDT.WDTRR 4004 4200h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	The down-counter is refreshed by writing 00h and then writing FFh to this register	R/W

The WDTRR register refreshes the down-counter of the WDT.

The down-counter of the WDT is refreshed by writing 00h and then writing FFh to WDTRR (refresh operation) within the refresh-permitted period.

After the down-counter is refreshed, it starts counting down from the value selected in the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]) in the Option Function Select Register 0 in auto start mode. In register start mode, counting down starts from the value selected in the Timeout Period Select bits (WDTCR.TOPS[1:0]) in the WDT Control Register.

When 00h is written, the read value is 00h. When a value other than 00h is written, the read value is FFh. For details on the refresh operation, see section 25.3.3, Refresh Operation.

25.2.2 WDT Control Register (WDTCR)

Address(es): WDT.WDTCR 4004 4202h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	TOPS[1:0]	Timeout Period Select	b1 b0 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh).	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7 to b4	CKS[3:0]	Clock Division Ratio Select	b7 b4 0 0 0 1: PCLKB/4 0 1 0 0: PCLKB/64 1 1 1 1: PCLKB/128 0 1 1 0: PCLKB/512 0 1 1 1: PCLKB/2048 1 0 0 0: PCLKB/8192. Other settings are prohibited.	R/W
b9, b8	RPES[1:0]	Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (do not specify window end position).	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	RPSS[1:0]	Window Start Position Select	b13 b12 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (do not specify window start position).	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Some constraints apply to writes to the WDTCR register. For details, see section 25.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the settings in the WDTCR register are disabled, and the settings in the Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made for the OFS0 register. For details, see section 25.3.7, Association between Option Function Select Register 0 (OFS0) and WDT Registers.

TOPS[1:0] bits (Timeout Period Select)

The TOPS[1:0] bits select the timeout period, the period until the down-counter underflows, from 1024, 4096, 8192, and 16384 cycles, taking the divided clock specified in the CKS[3:0] bits as 1 cycle. After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the number of PCLKB cycles until the counter underflows.

Table 25.2 lists the relationship between the CKS[3:0] and TOPS[1:0] bit settings, the timeout period, and the number of PCLKB cycles.

Table 25.2 Timeout period settings

CKS[3:0] bits				TOPS[1:0] bits		Clock division ratio	Timeout period (number of cycles)	PCLKB clock cycles
b7	b6	b5	b4	b1	b0			
0	0	0	1	0	0	PCLKB/4	1024	4096
				0	1		4096	16384
				1	0		8192	32768
				1	1		16384	65536
0	1	0	0	0	0	PCLKB/64	1024	65536
				0	1		4096	262144
				1	0		8192	524288
				1	1		16384	1048576
1	1	1	1	0	0	PCLKB/128	1024	131072
				0	1		4096	524288
				1	0		8192	1048576
				1	1		16384	2097152
0	1	1	0	0	0	PCLKB/512	1024	524288
				0	1		4096	2097152
				1	0		8192	4194304
				1	1		16384	8388608
0	1	1	1	0	0	PCLKB/2048	1024	2097152
				0	1		4096	8388608
				1	0		8192	16777216
				1	1		16384	33554432
1	0	0	0	0	0	PCLKB/8192	1024	8388608
				0	1		4096	33554432
				1	0		8192	67108864
				1	1		16384	134217728

CKS[3:0] bits (Clock Division Ratio Select)

The CKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the peripheral clock (PCLKB) divided by 4, 64, 128, 512, 2048, and 8192. Combined with the TOPS[1:0] bit setting, a count period between 4096 and 134217728 PCLKB clock cycles can be selected for the WDT.

RPES[1:0] bits (Window End Position Select)

The RPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. The selected window end position should be a value less than the value for the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

RPSS[1:0] bits (Window Start Position Select)

The RPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. The selected window start position should be a value greater than the value for the window end position. If the window start position is set to a value less than or equal to the window end position, the window end position is set to 0%.

Table 25.3 lists the counter values for the window start and end positions, and Figure 25.2 shows the refresh-permitted period set in the RPSS[1:0], RPES[1:0], and TOPS[1:0] bits.

Table 25.3 Relationship between the timeout period and window start and end counter values

TOPS[1:0] bits		Timeout period		Window start and end counter value			
		Cycles	Counter value	100%	75%	50%	25%
0	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
0	1	4096	0FFFh	0FFFh	0BFFh	07FFh	03FFh
1	0	8192	1FFFh	1FFFh	17FFh	0FFFh	07FFh
1	1	16384	3FFFh	3FFFh	2FFFh	1FFFh	0FFFh

RPSS[1:0] bits		RPES[1:0] bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75

Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

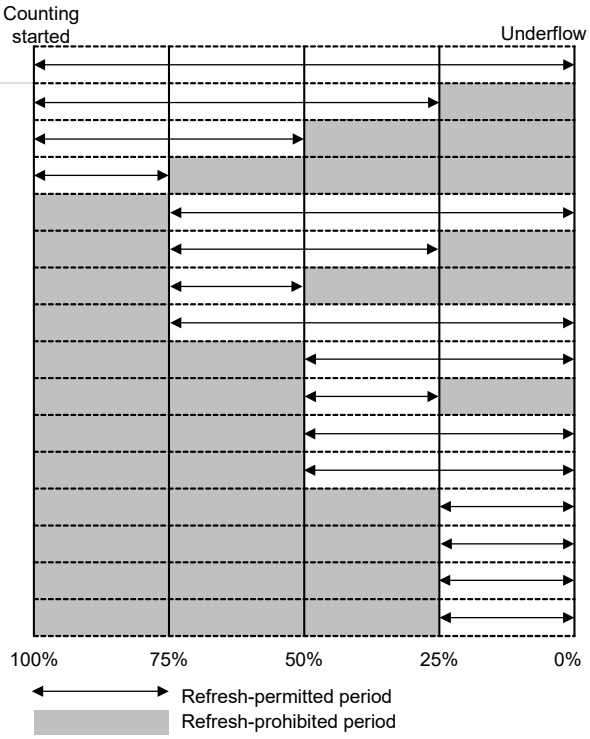


Figure 25.2 RPSS[1:0] and RPES[1:0] bit settings and refresh-permitted period

25.2.3 WDT Status Register (WDTSR)

Address(es): WDT.WDTSR 4004 4204h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CNTVAL[13:0]	Down-Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred.	R(/W) *1
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred.	R(/W) *1

Note 1. Only 0 can be written to clear the flag.

CNTVAL[13:0] bits (Down-Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. A value of 1 indicates that the down-counter underflowed. Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N + 1) PCLKB cycles. In addition, clearing of the flag is ignored for (N + 1) PCLKB cycles after an underflow. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0001b, N = 4
- When WDTCR.CKS[3:0] = 0100b, N = 64
- When WDTCR.CKS[3:0] = 1111b, N = 128
- When WDTCR.CKS[3:0] = 0110b, N = 512
- When WDTCR.CKS[3:0] = 0111b, N = 2048
- When WDTCR.CKS[3:0] = 1000b, N = 8192.

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred. A value of 1 indicates that a refresh error occurred. Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N + 1) PCLKB cycles. In addition, clearing of the flag is ignored for (N + 1) PCLKB cycles following a refresh error. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0001b, N = 4
- When WDTCR.CKS[3:0] = 0100b, N = 64
- When WDTCR.CKS[3:0] = 1111b, N = 128
- When WDTCR.CKS[3:0] = 0110b, N = 512
- When WDTCR.CKS[3:0] = 0111b, N = 2048
- When WDTCR.CKS[3:0] = 1000b, N = 8192.

25.2.4 WDT Reset Control Register (WDTRCR)

Address(es): WDT.WDTRCR 4004 4206h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	RSTIRQS	Reset Interrupt Request Select	0: Non-maskable interrupt request or interrupt request output is enabled 1: Reset output is enabled.	R/W

Some constraints apply to writes to the WDTRCR register. For details, see section 25.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTRCR register settings are disabled, and the settings in the Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made for the OFS0 register. For details, see section 25.3.7, Association between Option Function Select Register 0 (OFS0) and WDT Registers.

25.2.5 WDT Count Stop Control Register (WDTCSTPR)

Address(es): WDT.WDTCSTPR 4004 4208h

	b7	b6	b5	b4	b3	b2	b1	b0
	SLCSTP	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SLCSTP	Sleep-Mode Count Stop Control	0: Count stop is disabled 1: Count is stopped when transition to Sleep mode.	R/W

The WDTCSTPR register controls whether to stop the WDT counter in a low power mode. Some restrictions apply to writes to the WDTCSTPR register. For details, see section 25.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTCSTPR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTCSTPR register can also be made for the OFS0 register. For details, see section 25.3.7, Association between Option Function Select Register 0 (OFS0) and WDT Registers.

SLCSTP bit (Sleep-Mode Count Stop Control)

The SLCSTP bit selects whether to stop counting when transition to Sleep mode.

25.2.6 Option Function Select Register 0 (OFS0)

For information on the OFS0 register, see section 25.3.7, Association between Option Function Select Register 0 (OFS0) and WDT Registers.

25.3 Operation

25.3.1 Count Operation in each Start Mode

The WDT has two start modes:

- Auto start mode, in which counting automatically starts after a release from the reset state
- Register start mode, in which counting is started with a refresh by writing to the register.

In auto start mode, counting automatically starts after a release from the reset state based on the settings in the Option Function Select Register 0 (OFS0) in the flash.

In register start mode, counting starts with a refresh by writing to the register after the respective registers are set after a release from the reset state.

Select auto start mode or register start mode by setting the WDT Start Mode Select bit (OFS0.WDTSTRT) in the OFS0 register. When the auto start mode is selected, the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled, while the settings in the OFS0 register are enabled.

When the register start mode is selected, the OFS0 register setting is disabled while the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

25.3.1.1 Register start mode

When the WDT Start Mode Select bit (OFS0.WDTSTRT) is 1, register start mode is selected and the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

After the reset state is released, set the following to Sleep mode in the WDTCSTPR register:

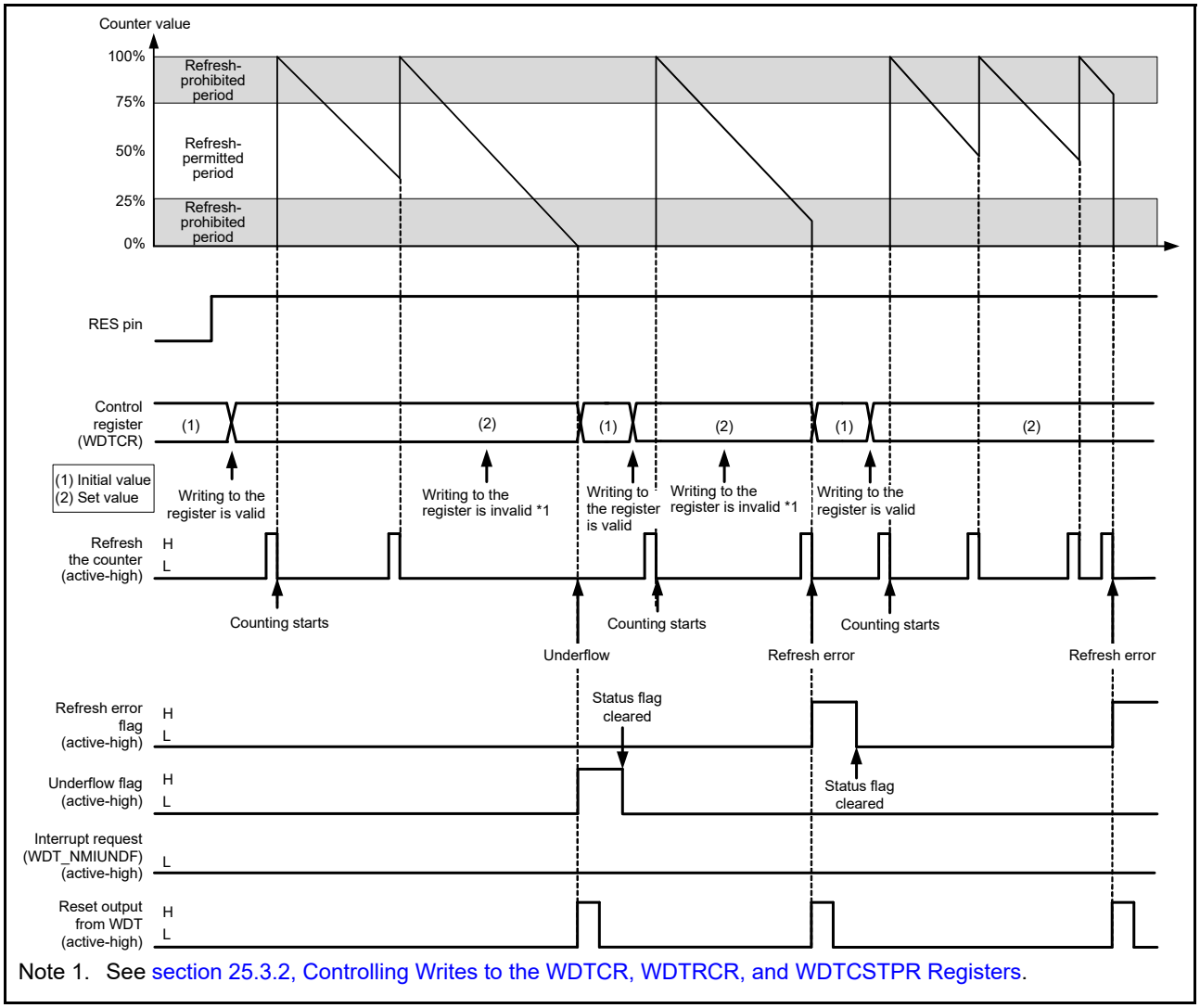
- Clock division ratio
- Window start and end positions
- Timeout period in the WDTCR register
- Reset output or interrupt request output in the WDTRCR register
- Counter stop control during transitions to Sleep mode in the WDTCSTPR register.

Refresh the down-counter to start counting down from the value set in the Timeout Period Select bits (WDTCR.TOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The WDT does not output the reset signal as long as counting continues. However, if the down-counter underflows because the down-counter cannot be refreshed because of a program runaway, or if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the WDT outputs a reset signal or a non-maskable interrupt request/interrupt request (WDT_NMIUNDF). Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (WDTRCR.RSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 25.3 shows an example of operation under the following conditions:

- Register start mode (OFS0.WDTSTRT = 1)
- Reset output is enabled (WDTRCR.RSTIRQS = 1)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b).



Note 1. See section 25.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

Figure 25.3 Operation example in register start mode

25.3.1.2 Auto start mode

When the WDT Start Mode Select bit (OFS0.WDTSTRT) in the Option Function Select Register 0 (OFS0) is 0, auto start mode is selected. The WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled while the settings in the OFS0 register are enabled.

Within the reset state, the following values in the Option Function Select Register 0 (OFS0) are set in the WDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control on transition to Sleep mode.

When the reset state is released, the down-counter automatically starts counting down from the value set in the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The WDT does not output the reset signal as long as the counting continues. However, if the down-counter underflows because refreshing of the down-counter is not possible due to a runaway program or if a refresh error occurs due to refreshing outside the refresh-permitted period, the WDT outputs the

reset signal or non-maskable interrupt request/interrupt request (WDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle. The value of the timeout period is set in the down-counter and counting restarts.

Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 25.4 shows an example of operation (non-maskable interrupt) under the following conditions:

- Auto start mode (OFS0.WDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.WDTRSTIRQS = 0)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b).

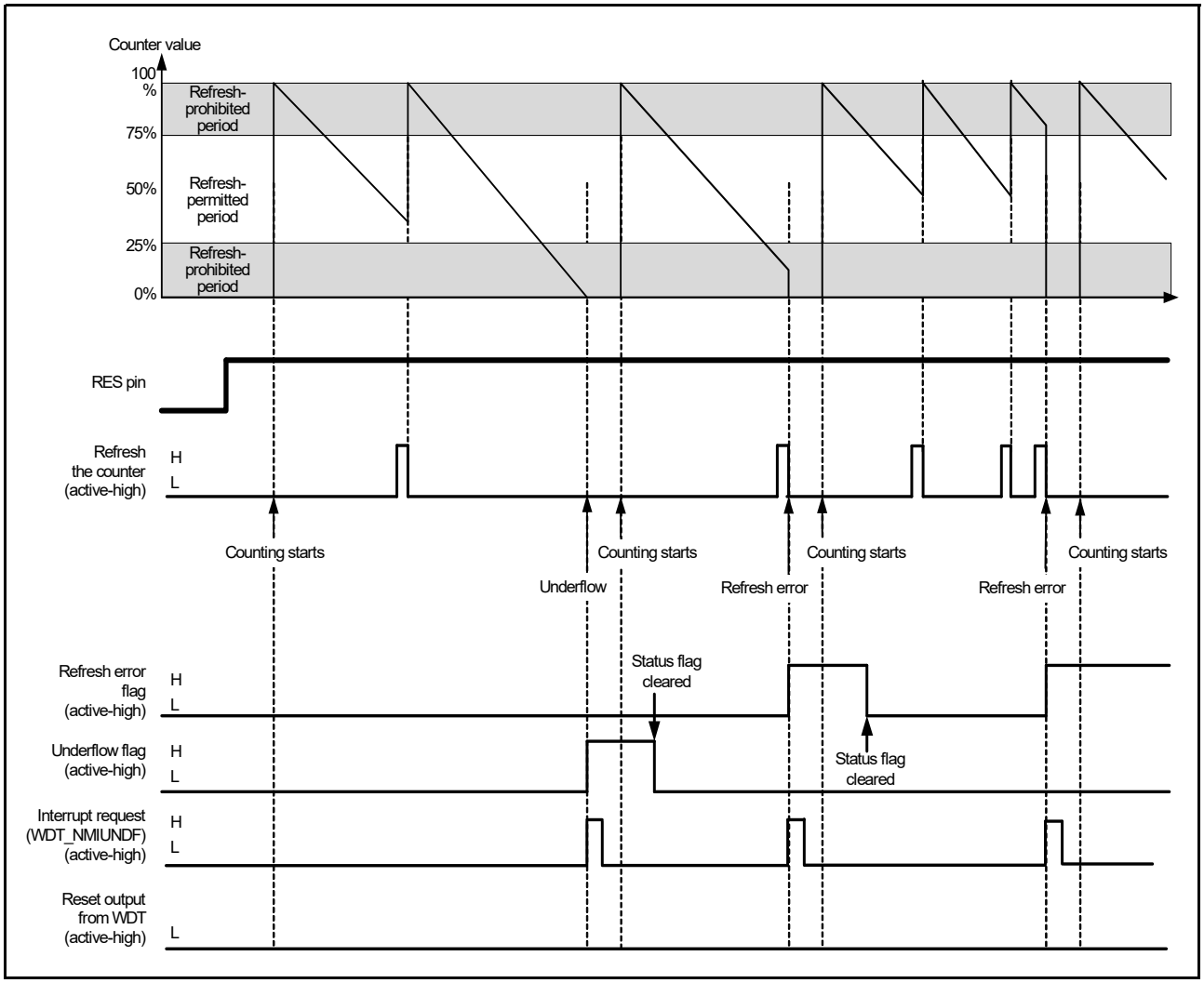


Figure 25.4 Operation example in auto start mode

25.3.2 Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers

Writing to the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), or WDT Count Stop Control Register (WDTCSTPR) is possible once between the release from the reset state and the first refresh operation.

After a refresh (counting starts) or a write to WDTCR, WDTRCR or WDTCSTPR, the protection signal in the WDT becomes 1 to protect WDTCR, WDTRCR and WDTCSTPR against subsequent write attempts. This protection is released by a reset source of the WDT. With other reset sources, the protection is not released.

Figure 25.5 shows control waveforms produced in response to writing to the WDTCR.

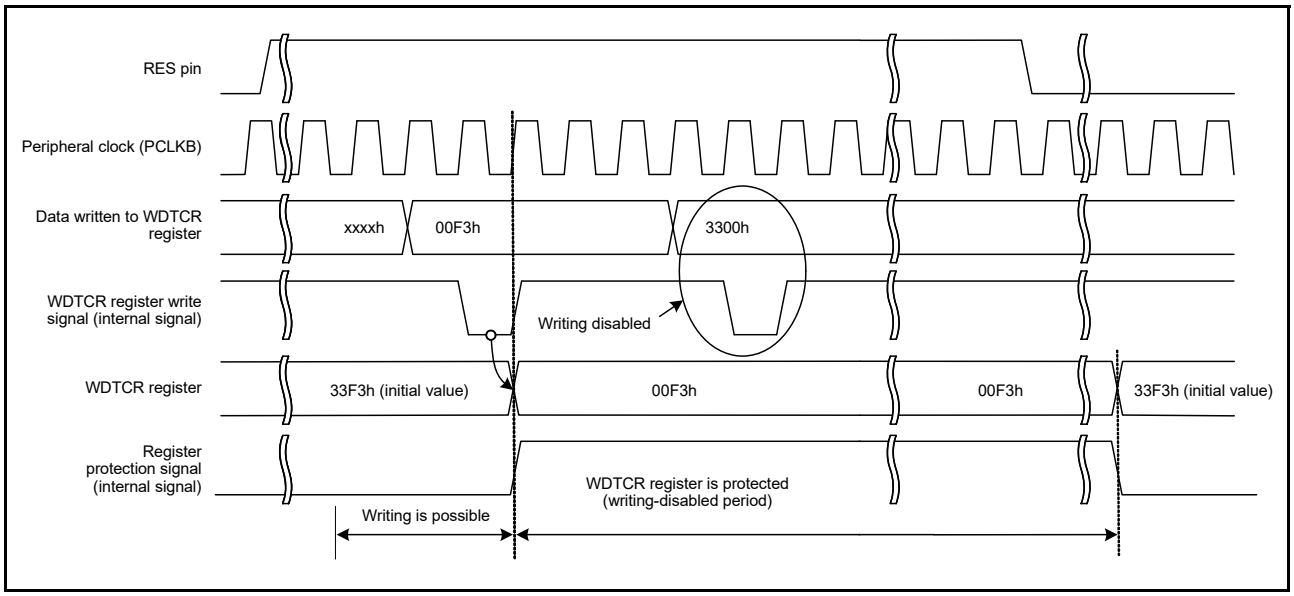


Figure 25.5 Control waveforms produced in response to writes to the WDTCR register

25.3.3 Refresh Operation

The down-counter is refreshed by writing the values 00h and FFh to the WDT Refresh Register (WDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes by writing 00h and FFh to the WDTRR register.

Correct refreshing is performed when a register other than WDTRR is accessed or when WDTRR is read between writing 00h and writing FFh to WDTRR.

Writing to refresh the counter must be performed within the refresh-permitted period, and whether this is done is determined by writing FFh. For this reason, correct refreshing is performed even when 00h is written outside the refresh-permitted period.

[Example write sequences that are valid when refreshing the counter]

- 00h → FFh
- 00h ((n - 1)th time) → 00h (nth time) → FFh
- 00h → access to another register or read from WDTRR → FFh.

[Example write sequences that are invalid when refreshing the counter]

- 23h (a value other than 00h) → FFh
- 00h → 54h (a value other than FFh)
- 00h→ AAh (00h and a value other than FFh) → FFh.

After FFh is written to the WDT Refresh Register (WDTRR), refreshing the down-counter requires up to 4 cycles of the signal for counting. To meet this requirement, complete writing FFh to WDTRR 4 cycle counts before the down-counter underflows.

Figure 25.6 shows the WDT refresh-operation waveforms when the clock division ratio is PCLKB/64.

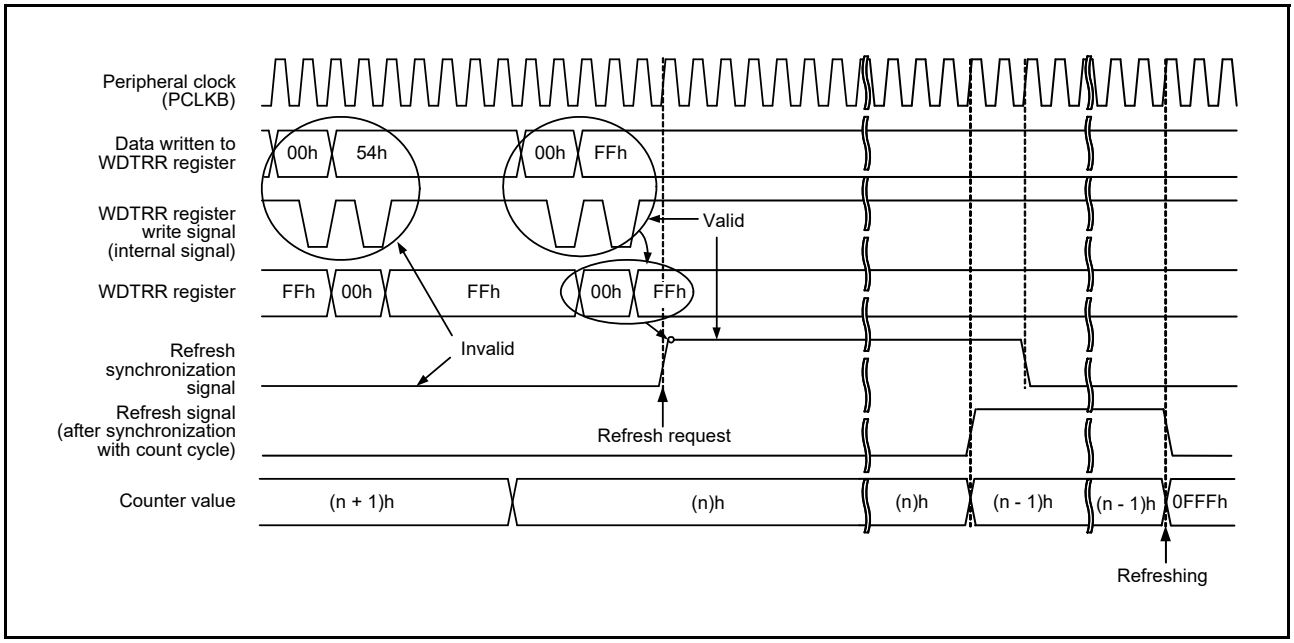


Figure 25.6 WDT refresh operation waveforms when WDTCR.CKS[3:0] = 0100b and WDTCR.TOPS[1:0] = 01b

25.3.4 Reset Output

When the Reset Interrupt Request Select bit (WDTRCR.RSTIRQS) is set to 1 in register start mode, or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1 in auto start mode, a reset signal is output for 1 cycle count when an underflow in the down-counter or a refresh error occurs.

In register start mode, the down-counter is initialized (all bits set to 0) and stopped in that state after output of a reset signal. After the reset state is released and the program is restarted, the counter is set up and counting down starts again with a refresh. In auto start mode, counting down starts automatically after the reset state is released.

25.3.5 Interrupt Sources

When the Reset Interrupt Request Select bit (WDTRCR.RSTIRQS) is set to 0 in register start mode or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0 in auto start mode, an interrupt signal (WDT_NMIUNDF) is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 13, Interrupt Controller Unit (ICU).

Table 25.4 WDT interrupt sources

Name	Interrupt source	DTC activation	DMAC activation
WDT_NMIUNDF	• Down-counter underflow • Refresh error.	Not possible	Not possible

25.3.6 Reading the Down-Counter Value

The WDT stores the counter value in the down-counter value bits (WDTSR.CNTVAL[13:0]) in the WDT Status Register. Check these bits to obtain the counter value.

Figure 25.7 shows the processing for reading the WDT down-counter value when the clock division ratio is PCLKB/64.

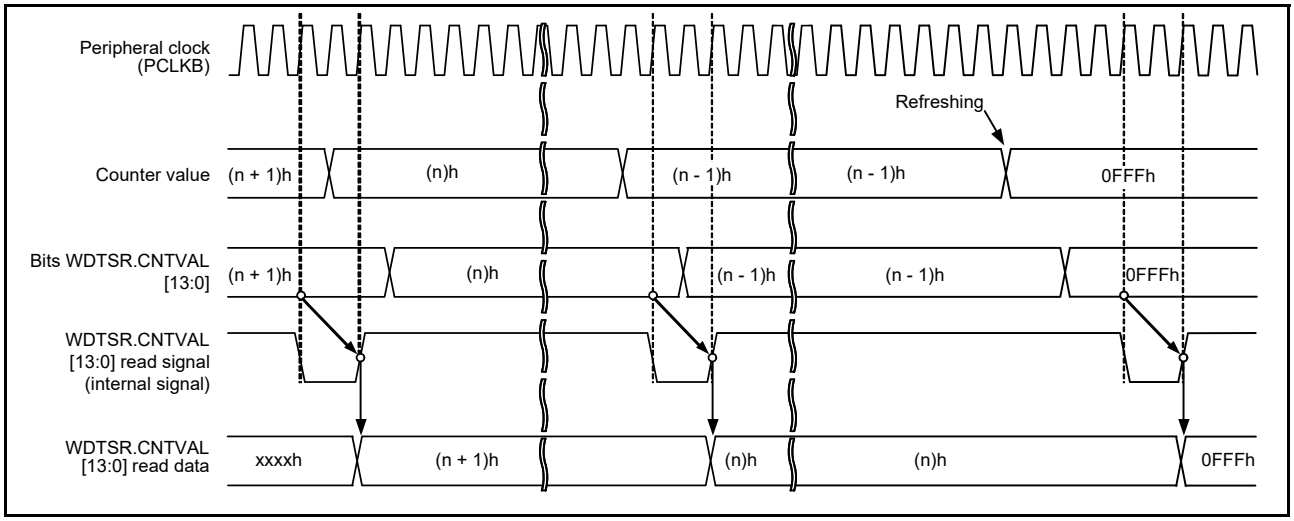


Figure 25.7 Processing for reading WDT down-counter value when WDTCR.CKS[3:0] = 0100b and WDTCR.TOPS[1:0] = 01b

25.3.7 Association between Option Function Select Register 0 (OFS0) and WDT Registers

Table 25.5 lists the association between the Option Function Select Register 0 (OFS0) used in auto start mode, and the registers used in register start mode. Do not change the OFS0 register settings during WDT operation. For details on the Option Function Select Register 0 (OFS0), see section 7, Option Function Select Register 0 (OFS0).

Table 25.5 Association between Option Function Select Register 0 (OFS0) and the WDT registers

Control target	Function	OFS0 register (enabled in auto start mode) OFS0.WDTSTRT = 0	WDT registers (enabled in register start mode) OFS0.WDTSTRT = 1
Down-counter	Timeout period select	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	Clock division ratio select	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	Window start position select	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	Window end position select	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
Reset output or interrupt request output	Reset output or interrupt request output select	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
Count stop	Sleep-mode count stop control	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

25.4 Link Operation by ELC

The WDT is capable of a link operation for the previously specified module when interrupt request signal is used as an event signal by the ELC. The event signal is output by the counter underflow or refresh error.

An event signal is output regardless of the setting in the Reset Interrupt Request Select bit (WDTRCR.RSTIRQS) in register start mode or the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in auto start mode. An event signal can also be output when the next interrupt source is generated while the Refresh Error flag (WDTSR.REFEF) or Underflow flag (WDTSR.UNDFF) is 1. For details, see section 18, Event Link Controller (ELC).

25.5 Usage Notes

25.5.1 ICU Event Link Setting Register n (IELSRn) Setting

Setting 47h to the ICU Event Link Setting Register n (IELSRn.IELS[8:0] bits) is prohibited when enabling the WDT reset assertion (OFS0.WDTRSTIRQS = 1 or WDTRCR.RSTIRQS = 1), or when enabling the event link operation (47h is set to ELSRm.ELS[8:0]).

26. Independent Watchdog Timer (IWDT)

26.1 Overview

The Independent Watchdog Timer (IWDT) is a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT can be used to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates using an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a failsafe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

The functions of the IWDT are different from those of the WDT in the following ways:

- The divided IWDT-dedicated clock (IWDTCLK) is used as the count source (not affected by PCLKB)
- IWDT does not support the register start mode
- When transitioning to a low power mode (excluding Deep Software Standby mode), the OFS0.IWDTSTPCTL bit can be used to select whether to stop the counter or not.

Table 26.1 lists the IWDT specifications and Figure 26.1 shows a block diagram.

Table 26.1 IWDT specifications

Parameter	Specifications
Count source*1	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	Counting automatically starts after a reset
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated (counting restarts automatically).
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
IWDT reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading of the counter value	The down-counter value can be read by the IWDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output.
Auto start mode	Configurable to the following triggers: • Clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Timeout period of the IWDT (OFS0.IWDTTOPS[1:0] bits) • Window start position in the IWDT (OFS0.IWDTRPSS[1:0] bits) • Window end position in the IWDT (OFS0.IWDTRPES[1:0] bits) • Reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Down-count stop function at transition to Sleep mode, Software Standby mode, or Snooze mode (OFS0.IWDTSTPCTL bit).

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

To use the IWDT, you must supply the IWDT-dedicated clock (IWDTCLK). The bus interface and registers operate with PCLKB, and the 14-bit counter and control circuits operate with IWDTCLK.

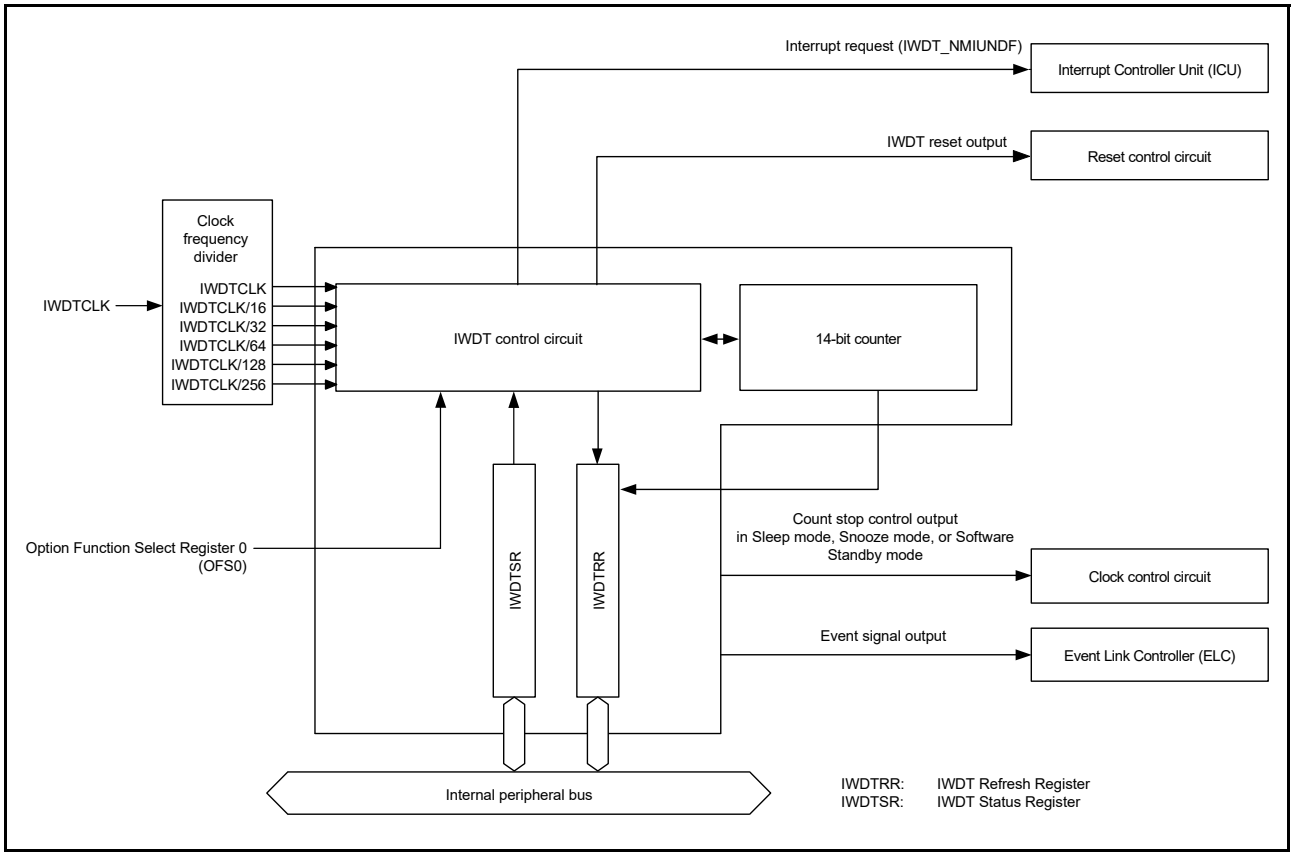


Figure 26.1 IWDT block diagram

26.2 Register Descriptions

26.2.1 IWDT Refresh Register (IWDTRR)

Address(es): IWDT.IWDTRR 4004 4400h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	The down-counter is refreshed by writing 00h and then writing FFh to this register	R/W

The IWDTRR register refreshes the down-counter of the IWDT. The down-counter of the IWDT is refreshed by writing 00h and then writing FFh to IWDTRR (refresh operation) within the refresh-permitted period. After the down-counter is refreshed, it starts counting down from the value selected in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]) in Option Function Select Register 0 (OFS0).

When 00h is written, the read value is 00h. When a value other than 00h is written, the read value is FFh. For details on the refresh operation, see section 26.3.2, Refresh Operation.

26.2.2 IWDT Status Register (IWDTSR)

Address(es): IWDT.IWDTSR 4004 4404h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CNTVAL[13:0]	Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred.	R/(W)*1
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred.	R/(W)*1

Note 1. Only 0 can be written to clear the flag.

CNTVAL[13:0] bits (Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. A value of 1 indicates that the down-counter underflowed. Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N + 2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of the flag is ignored for (N + 2) IWDTCLK cycles after an underflow. N is specified in the IWDTCKS[3:0] bits as follows:

- When IWDTCKS[3:0] = 0000b, N = 1
- When IWDTCKS[3:0] = 0010b, N = 16
- When IWDTCKS[3:0] = 0011b, N = 32
- When IWDTCKS[3:0] = 0100b, N = 64
- When IWDTCKS[3:0] = 1111b, N = 128
- When IWDTCKS[3:0] = 0101b, N = 256.

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred. This indicates that a refresh operation was performed during a prohibited period. A value of 1 indicates that a refresh error occurred. Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N + 2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of the flag is ignored for (N + 2) IWDTCLK cycles after a refresh error. N is specified in the IWDTCKS[3:0] bits as follows:

- When IWDTCKS[3:0] = 0000b, N = 1
- When IWDTCKS[3:0] = 0010b, N = 16
- When IWDTCKS[3:0] = 0011b, N = 32
- When IWDTCKS[3:0] = 0100b, N = 64
- When IWDTCKS[3:0] = 1111b, N = 128
- When IWDTCKS[3:0] = 0101b, N = 256.

26.2.3 Option Function Select Register 0 (OFS0)

For information on the Option Function Select Register 0 (OFS0), see section 7.2.1, Option Function Select Register 0 (OFS0).

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits select the timeout period, that is, the period until the down-counter underflows, from 128, 512, 1024, or 2048 cycles, taking the divided clock specified in the IWDTCKS[3:0] bits as 1 cycle.

After the down-counter is refreshed, the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits determines the number of IWDTCLK cycles until the counter underflows.

Table 26.2 lists the relationship between the IWDTCKS[3:0] and IWDTTOPS[1:0] bit settings, the timeout period, and the number of IWDTCLK cycles.

Table 26.2 Timeout period settings

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits				
b7	b6	b5	b4	b1	b0	Clock division ratio	Timeout period (number of cycles)	IWDTCLK cycles
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the IWDT-dedicated clock (IWDTCLK) divided by 1, 16, 32, 64, 128, and 256. Combined with the IWDTTOPS[1:0] bit setting, the IWDT can be configured to a count period between 128 and 524288 IWDTCLK cycles.

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

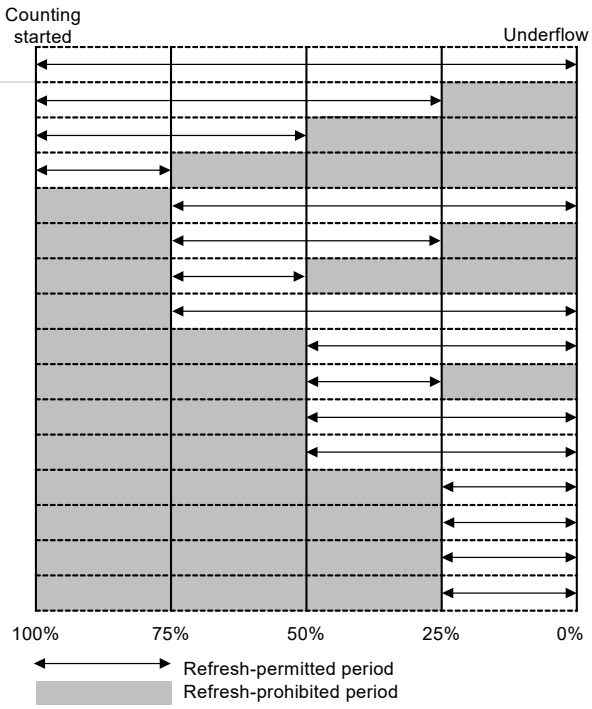
The IWDTRPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the window end position. If the window start position is less than or equal to the window end position, the window end position is set to 0%.

Table 26.3 lists the counter values for the window start and end positions, and Figure 26.2 shows the refresh-permitted period set in the IWDTRPSS[1:0], IWDTRPES[1:0], and IWDTTOPS[1:0] bits.

Table 26.3 Relationship between the timeout period and window start and end counter values

IWDTTOPS[1:0] bits		Timeout period		Window start and end counter value			
b1	b0	Cycles	Counter value	100%	75%	50%	25%
0	0	128	007Fh	007Fh	005Fh	003Fh	001Fh
0	1	512	01FFh	01FFh	017Fh	00FFh	007Fh
1	0	1,024	03FFh	03FFh	02FFh	01FFh	00FFh
1	1	2,048	07FFh	07FFh	05FFh	03FFh	01FFh

IWDTRPSS[1:0] bits		IWDTRPES[1:0] bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 26.2 IWDTRPSS[1:0] and IWDTRPES[1:0] bit settings and refresh-permitted period

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit specifies the behavior when an underflow or a refresh error occurred. Set this bit to 1 to select reset output. Set this bit to 0 for non-maskable interrupt or interrupt.

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit selects whether to stop counting on transition to Sleep, Snooze, or Software Standby mode.

26.3 Operation

26.3.1 Auto Start Mode

When the IWDT Start Mode Select bit (OFS0.IWDTSTRT) in the Option Function Select Register 0 is 0, auto start mode is selected, otherwise the IWDT is disabled.

Within the reset state, the following values in Option Function Select Register 0 (OFS0) are set in the IWDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control at transitions to low power mode.

When the reset state is released, the down-counter automatically starts counting down from the value set in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]).

After that, as long as the program continues normal operation and the counter is refreshed within the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The IWDT does not output the reset signal as long as this procedure continues. However, if the counter underflows because the program crashed, or because a refresh error occurred when an attempt is made to refresh outside the refresh-permitted period, the IWDT asserts the reset signal or non-maskable interrupt request/interrupt request (IWDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle, and restarts the count. Reset output or interrupt request output can be selected in the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the IWDT Underflow/Refresh Error Interrupt Enable bit (NMIER.IWDTEN).

Figure 26.3 shows an example of operation under the following conditions:

- Auto start mode (OFS0.IWDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.IWDTRSTIRQS = 0)
- The window start position is 75% (OFS0.IWDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.IWDTRPES[1:0] = 10b).

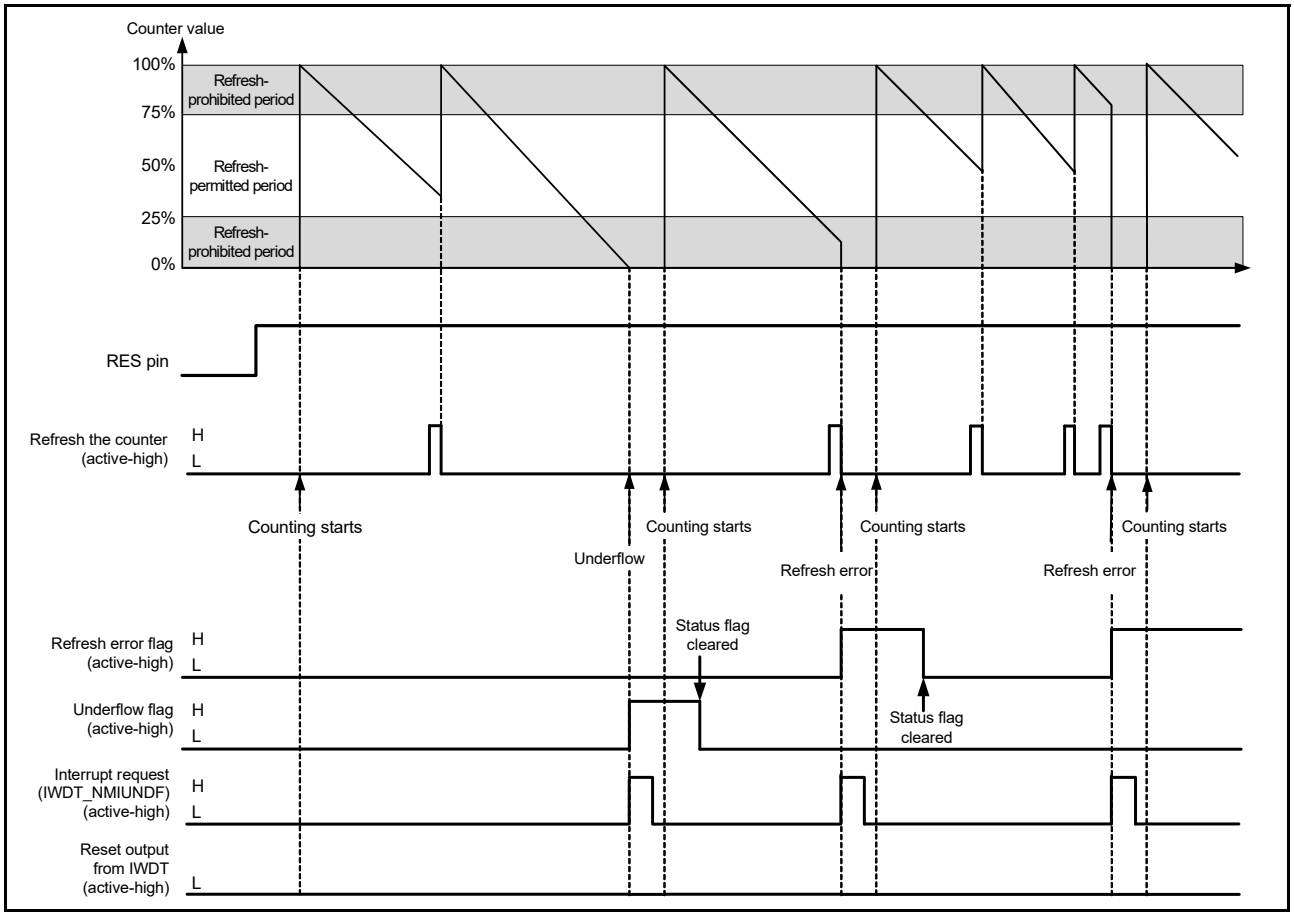


Figure 26.3 Operation example in auto start mode

26.3.2 Refresh Operation

The down-counter is refreshed by writing the values 00h and FFh to the IWDT Refresh Register (IWDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on writing 00h and FFh to the IWDTRR.

When writing is done in the order of 00h (first time) → 00h (second time), and if FFh is written after that, the writing order 00h → FFh is satisfied. Writing 00h ((n - 1)th time) → 00h (nth time) → FFh is valid, and the refresh is performed correctly. Even when the first value written before 00h is not 00h, correct refreshing is performed as long as the operation contains the write sequence 00h → FFh.

Correct refreshing is also performed regardless of whether a register other than IWDTRR is accessed or IWDTRR is read between writing 00h and writing FFh to IWDTRR. Writes to refresh the counter must be made within the refresh-permitted period, and this is determined by writing FFh. For this reason, correct refreshing is performed even when 00h is written outside the refresh-permitted period.

[Example write sequences that are valid to refresh the counter]

- 00h → FFh
- 00h ((n - 1)th time) → 00h (nth time) → FFh
- 00h → access to another register or read from IWDTRR → FFh.

[Example write sequences that are invalid to refresh the counter]

- 23h (a value other than 00h) → FFh
- 00h → 54h (a value other than FFh)
- 00h → AAh (00h and a value other than FFh) → FFh.

After FFh is written to the IWDTRR, refreshing the down-counter requires up to 4 cycles of the signal for counting (the IWDT-Dedicated Clock Frequency Division Ratio Select bits (OFS0.IWDTCKS[3:0]) to determine how many cycles of the IWDT-dedicated clock (IWDTCLK) make up 1 counting cycle. To meet this requirement, writing FFh to IWDTRR must be completed 4 count cycles before the end of the refresh-permitted period or a counter underflow. The value of the counter can be checked in the counter bits (IWDTSR.CNTVAL[13:0]).

[Example refreshing timings]

- When the window start position is set to 1FFFh, even if 00h is written to IWDTRR before 1FFFh is reached (at 2002h, for example), refreshing occurs if FFh is written to IWDTRR after the value of the IWDTSR.CNTVAL[13:0] bits reaches 1FFFh
- When the window end position is set to 1FFFh, refreshing occurs if 2003h (4 count cycles before 1FFFh) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to IWDTRR
- When the refresh-permitted period continues until count 0000h, refreshing can be performed immediately before an underflow. In this case, if 0003h (4 count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to IWDTRR, no underflow occurs and refreshing is performed.

Figure 26.4 shows the IWDT refresh-operation waveforms when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

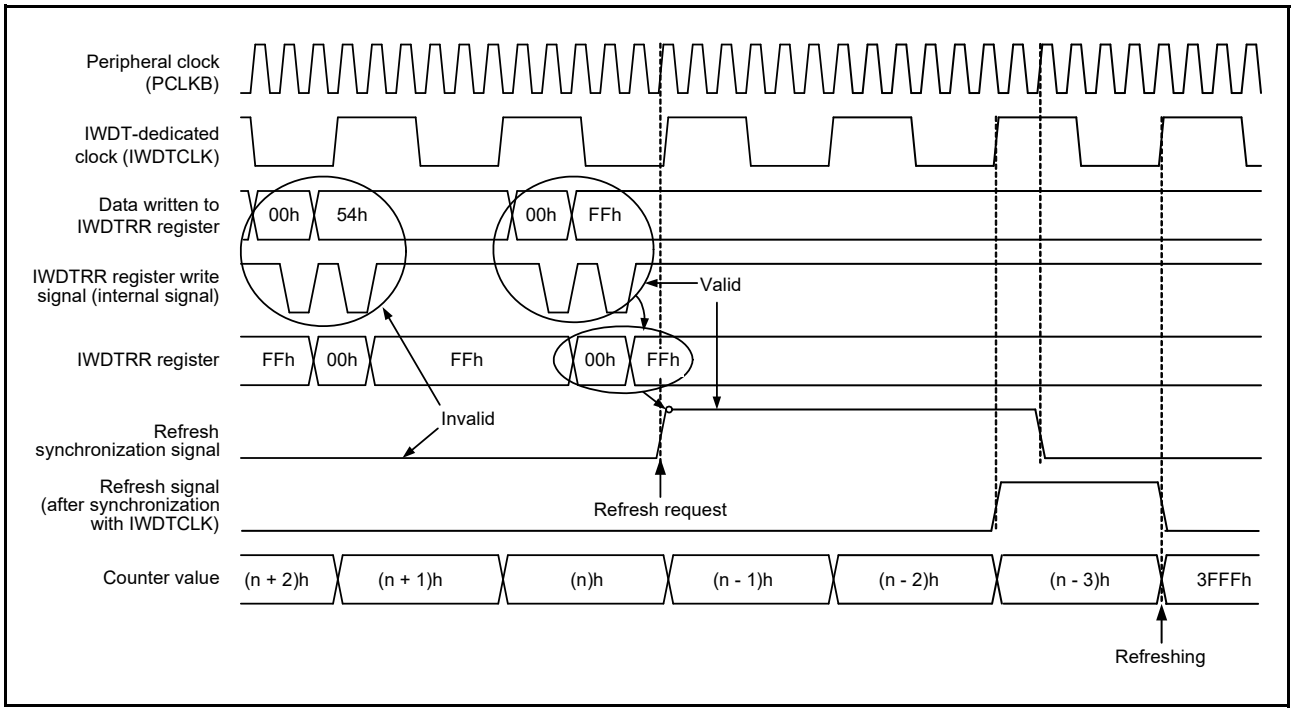


Figure 26.4 IWDT refresh operation waveforms when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

26.3.3 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the reset signal output or the source of the interrupt request from the IWDT. After a release from the reset state or interrupt request generation, read the IWDTSR.REFEF and UNDFF flags to check for the reset or interrupt source. For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared on the next reset or interrupt request from the IWDT, the earlier reset or interrupt source is cleared and the new reset or interrupt source is written. After 0 is written to each flag, up to 3 IWDTCLK cycles and 2 PCLKB cycles are required before the value is reflected.

26.3.4 Reset Output

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1, a reset signal is output when an underflow in the down-counter or a refresh error occurs. Counting down automatically starts after the reset output.

26.3.5 Interrupt Sources

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0, an interrupt signal (IWDT_NMIUNDF) is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 13, Interrupt Controller Unit (ICU).

Table 26.4 IWDT interrupt source

Name	Interrupt source	DTC activation	DMAC activation
IWDT_NMIUNDF	• Down-counter underflow • Refresh error.	Not possible	Not possible

26.3.6 Reading the Down-Counter Value

Because the counter is a IWDT-dedicated clock (IWDTCLK), the counter value cannot be read directly. The IWDT synchronizes the counter value with the peripheral clock (PCLKB) and stores it in the down-counter value bits (IWDTSR.CNTVAL[13:0]) in the IWDT Status register. Check these bits to obtain the counter value indirectly.

Reading the counter value requires multiple PCLKB clock cycles (up to 4 clock cycles), and the read counter value might differ from the actual counter value by a value of one count.

Figure 26.5 shows the processing for reading the IWDT counter value when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

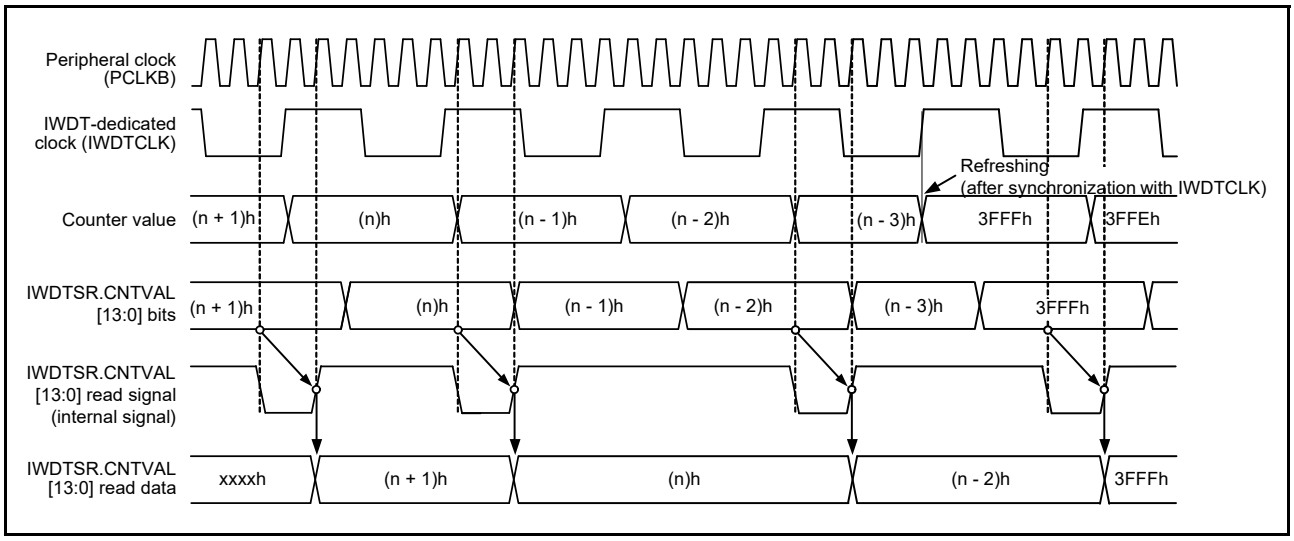


Figure 26.5 Processing for reading IWDT counter value when OFS0.IWDTCKS[3:0] = 0000b and OFS0.IWDTTOPS[1:0] = 11b

26.4 Link Operation by the ELC

The IWDT is capable of link operation for a specified module when the interrupt request signal is used as an event signal by the ELC. The event signal is output by the counter underflow or refresh error.

An event signal is output regardless of the setting in the OFS0.WDTRSTIRQS bit. An event signal can also be output when the next interrupt source is generated while the Refresh Error flag (IWDTSR.REFEF) or Underflow flag (IWDTSR.UNDFF) is 1. For details, see section 18, Event Link Controller (ELC).

26.5 Usage Notes

26.5.1 Refresh Operations

While configuring the refresh time, consider variations in the range of errors given the accuracy of PCLKB and IWDTCLK. Set values that ensure refreshing is possible.

26.5.2 Restrictions on the Clock Division Ratio Setting

Satisfy the following required frequency of the peripheral module clock (PCLKB):

PCLKB ≥ 4 × (the frequency of the count clock source after division).

27. Serial Communications Interface (SCI)

27.1 Overview

The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces:

- Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))
- 8-bit clock synchronous interface
- Simple IIC (master-only)
- Simple SPI
- Smart card interface.

The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI channel has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.

Table 27.1 lists the SCI specifications, Figure 27.1 shows a block diagram of SCI channel n, and Table 27.2 lists the I/O pins by mode.

Table 27.1 SCI specifications (1 of 2)

Parameter	Specifications
Serial communication modes	• Asynchronous • Clock synchronous • Smart card interface • Simple IIC • Simple SPI.
Transfer speed	Bit rate specifiable with the on-chip baud rate generator
Full-duplex communications	• Transmitter: Continuous transmission possible using double-buffering • Receiver: Continuous reception possible using double-buffering.
I/O pins	See Table 27.2
Data transfer	Selectable as LSB-first or MSB-first transfer
Interrupt sources	• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and address match • Completion of generation of a start condition, restart condition, or stop condition (for simple IIC mode).
Module-stop function	Module-stop state can be set for each channel
Snooze end request	SCI0 address mismatch (SCI0_DCUF)

Table 27.1 SCI specifications (2 of 2)

Parameter		Specifications
Asynchronous mode	Data length	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission/reception	Selectable to 1-stage register or 16-stage FIFO
	Address match	Interrupt request/event output can be issued on detecting a match between the received data and the value in the compare match register
	Address mismatch (SCI0 only) receive data	Snooze end request can be issued on detecting a mismatch between the received data and the value in the compare match register
	Start-bit detection	Selectable to low level or falling edge detection
	Break detection	Breaks from framing errors detectable by reading from the SPTR register
	Clock source	Selectable to internal or external clock
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Multi-processor communications function	Serial communication enabled between multiple processors
	Noise cancellation	Digital noise filters included on signal paths from RXDn pin inputs
Clock synchronous mode	Data length	8 bits
	Receive error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission/reception	Selectable to 1-stage register or 16-stage FIFO
Smart card interface mode	Error processing	Error signal can be automatically transmitted on detecting a parity error during reception
		Data can be automatically retransmitted on receiving an error signal during transmission
	Data type	Both direct and inverse convention supported
Simple IIC mode	Transfer format	I^2C bus format (MSB-first only)
	Operating mode	Master (single-master operation only)
	Transfer rate	Up to 400 kbps
	Noise cancellation	The signal paths from input on the SCLn and SDAn pins incorporate digital noise filters and provide an adjustable interval for noise cancellation
Simple SPI mode	Data length	8 bits
	Error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	SS input pin function	High impedance state can be invoked on the output pins by driving the SSn pin high
	Clock settings	Configurable between four clock phase and clock polarity settings
Bit rate modulation function		Error reduction through correction of outputs from the on-chip baud rate generator
Event link function		Error event output (SCIn_ERI)*1 for receive error or error signal detection
		Receive data full event output (SCIn_RXI)*1,*2
		Transmit data empty event output (SCIn_TXI)*1,*2
		Transmit end event output (SCIn_TEI)*1,*2
		Address match event output (SCIn_AM)*1

Note 1. Channel number (n = 0 to 4, 8, 9).

Note 2. Using this event link function is prohibited when FIFO operation is selected in asynchronous mode.

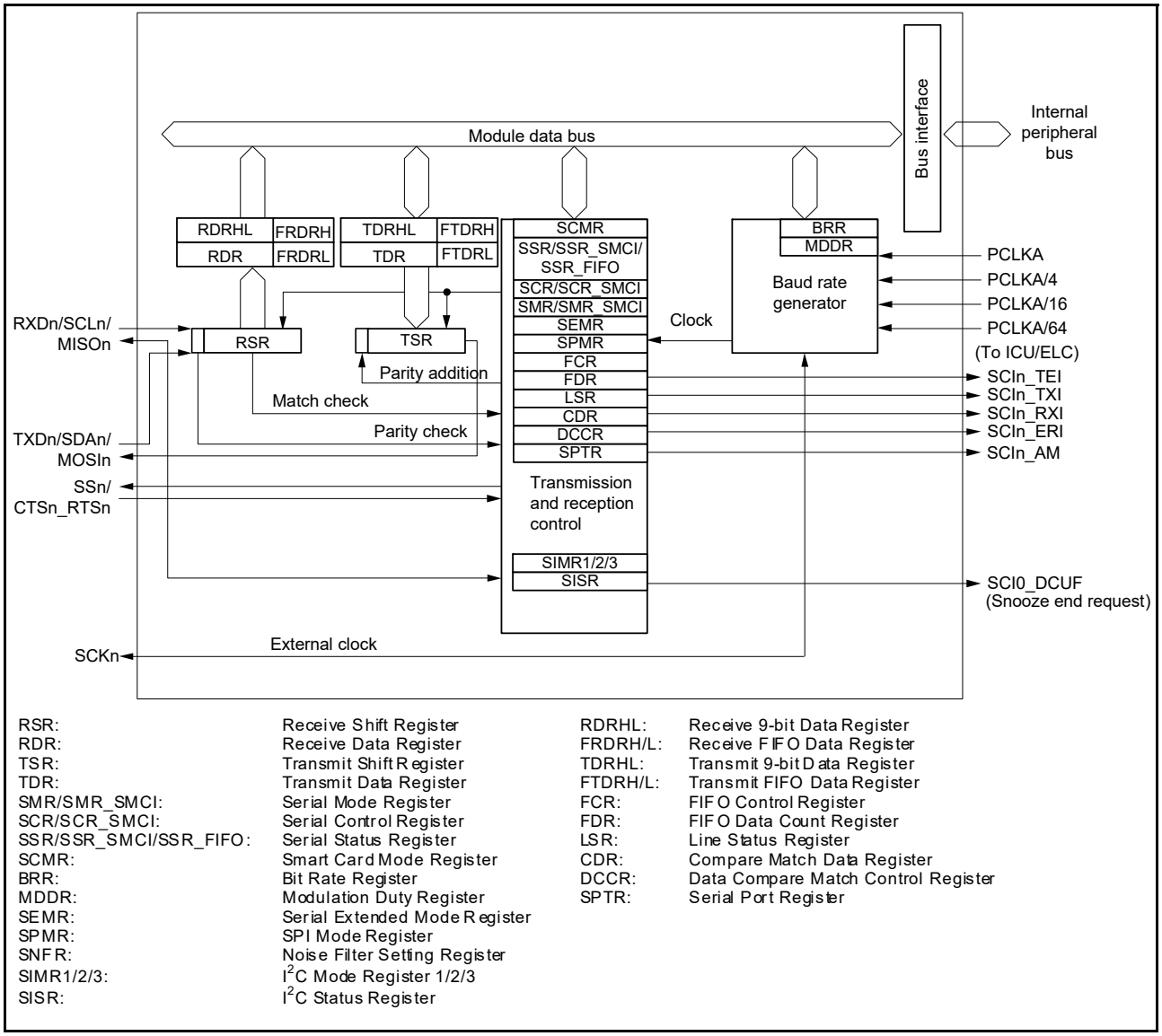


Figure 27.1 SCI channel n block diagram

Table 27.2 SCI I/O pins (1 of 2)

Channel	Pin name	Input/Output	Function
SCI0	SCK0	Input/Output	SCI0 clock input/output
	RXD0/SCL0/MISO0	Input/Output	SCI0 receive data input SCI0 I2C clock input/output SCI0 slave transmit data input/output
	TXD0/SDA0/MOSI0	Input/Output	SCI0 transmit data output SCI0 I2C data input/output SCI0 master transmit data input/output
	SS0/CTS0_RTS0	Input/Output	SCI0 chip select input, active-low SCI0 transfer start control input/output, active-low
SCI1	SCK1	Input/Output	SCI1 clock input/output
	RXD1/SCL1/MISO1	Input/Output	SCI1 receive data input SCI1 I2C clock input/output SCI1 slave transmit data input/output
	TXD1/SDA1/MOSI1	Input/Output	SCI1 transmit data output SCI1 I2C data input/output SCI1 master transmit data input/output
	SS1/CTS1_RTS1	Input/Output	SCI1 chip select input, active-low SCI1 transfer start control input/output, active-low
SCI2	SCK2	Input/Output	SCI2 clock input/output
	RXD2/SCL2/MISO2	Input/Output	SCI2 receive data input SCI2 I2C clock input/output SCI2 slave transmit data input/output
	TXD2/SDA2/MOSI2	Input/Output	SCI2 transmit data output SCI2 I2C data innput/output SCI2 master trasmit data input/output
	SS2/CTS2_RTS2	Input/Output	SCI2 chip select input, active-low SCI2 transfer start control input/output, active-low
SCI3	SCK3	Input/Output	SCI3 clock input/output
	RXD3/SCL3/MISO3	Input/Output	SCI3 receive data input SCI3 I2C clock input/output SCI3 slave transmit data input/output
	TXD3/SDA3/MOSI3	Input/Output	SCI3 transmit data output SCI3 I2C data input/output SCI3 master transmit data input/output
	SS3/CTS3_RTS3	Input/Output	SCI3 chip select input, active-low SCI3 transfer start control input/output, active-low
SCI4	SCK4	Input/Output	SCI4 clock input/output
	RXD4/SCL4/MISO4	Input/Output	SCI4 receive data input SCI4 I2C clock input/output SCI4 slave transmit data input/output
	TXD4/SDA4/MOSI4	Input/Output	SCI4 transmit data output SCI4 I2C data input/output SCI4 master transmit data input/output
	SS4/CTS4_RTS4	Input/Output	SCI4 chip select input, active-low SCI4 transfer start control input/output, active-low
SCI8	SCK8	Input/Output	SCI8 clock input/output
	RXD8/SCL8/MISO8	Input/Output	SCI8 receive data input SCI8 I2C clock input/output SCI8 slave transmit data input/output
	TXD8/SDA8/MOSI8	Input/Output	SCI8 transmit data output SCI8 I2C data input/output SCI8 master transmit data input/output
	SS8/CTS8_RTS8	Input/Output	SCI8 chip select input, active-low SCI8 transfer start control input/output, active-low

Table 27.2 SCI I/O pins (2 of 2)

Channel	Pin name	Input/Output	Function
SCI9	SCK9	Input/Output	SCI9 clock input/output
	RXD9/SCL9/MISO9	Input/Output	SCI9 receive data input SCI9 I2C clock input/output SCI9 slave transmit data input/output
	TXD9/SDA9/MOSI9	Input/Output	SCI9 transmit data output SCI9 I2C data input/output SCI9 master transmit data input/output
	SS9/CTS9_RTS9	Input/Output	SCI9 chip select input, active-low SCI9 transfer start control input/output, active-low

27.2 Register Descriptions

27.2.1 Receive Shift Register (RSR)

RSR is a shift register that receives serial data input from the RXDn pin and converts it into parallel data. When one frame of data is received, the data is automatically transferred to the RDR, RDRHL, or the receive FIFO register. The RSR register cannot be directly accessed by the CPU.

27.2.2 Receive Data Register (RDR)

Address(es): SCI0.RDR 4007 0005h, SCI1.RDR 4007 0025h, SCI2.RDR 4007 0045h, SCI3.RDR 4007 0065h, SCI4.RDR 4007 0085h, SCI8.RDR 4007 0105h, SCI9.RDR 4007 0125h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

RDR is an 8-bit register that stores receive data. When one frame of serial data is received, it is transferred from RSR to RDR, and the RSR register can receive more data. Because RSR and RDR function as a double buffer, continuous received operations can be performed.

Read the RDR register only once after a receive data full interrupt (SCIn_RXI) occurs.

Note: If the next frame of data is received before reading the received data from RDR, an overrun error occurs. The CPU cannot write to the RDR.

27.2.3 Receive 9-Bit Data Register (RDRHL)

Address(es): SCI0.RDRHL 4007 0010h, SCI1.RDRHL 4007 0030h, SCI2.RDRHL 4007 0050h, SCI3.RDRHL 4007 0070h, SCI4.RDRHL 4007 0090h, SCI8.RDRHL 4007 0110h, SCI9.RDRHL 4007 0130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RDRHL is a 16-bit register that stores receive data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of RDRHL are the shadow register of RDR, so access to RDRHL affects the RDR register. Access to the RDRHL register is prohibited if 7-bit or 8-bit data length is selected.

After one frame of data is received, the received data is transferred from the RSR to the RDR or RDRHL register, allowing the RSR register to receive more data.

The RSR and RDRHL registers have a double-buffered structure to enable continuous reception. RDRHL should be read only when a receive data full interrupt (SCIn_RXI) request is issued. An overrun error occurs when the next frame of data is received before the received data is read from RDRHL. The CPU cannot write to the RDRHL register. Bits [15:9] of the RDRHL register are fixed to 0. These bits are read as 0. The write value should be 0.

27.2.4 Receive FIFO Data Register H, L, HL (FRDRH, FRDRL, FRDRHL)

Receive FIFO Data Register H (FRDRH)

Address(es): SCI0.FRDRH 4007 0010h, SCI1.FRDRH 4007 0030h, SCI2.FRDRH 4007 0050h, SCI3.FRDRH 4007 0070h, SCI4.FRDRH 4007 0090h, SCI8.FRDRH 4007 0110h, SCI9.FRDRH 4007 0130h

Receive FIFO Data Register L (FRDRL)

Address(es): SCI0.FRDRL 4007 0011h, SCI1.FRDRL 4007 0031h, SCI2.FRDRL 4007 0051h, SCI3.FRDRL 4007 0071h, SCI4.FRDRL 4007 0091h, SCI8.FRDRL 4007 0111h, SCI9.FRDRL 4007 0131h

Receive FIFO Data Register HL (FRDRHL)

Address(es): SCI0.FRDRHL 4007 0010h, SCI1.FRDRHL 4007 0030h, SCI2.FRDRHL 4007 0050h, SCI3.FRDRHL 4007 0070h, SCI4.FRDRHL 4007 0090h, SCI8.FRDRHL 4007 0110h, SCI9.FRDRHL 4007 0130h

SCIn.FRDRHL

SCIn.FRDRH | SCIn.FRDRL

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	RDAT[8:0]	Serial Receive Data	Received serial data, valid only in asynchronous mode, including multi-processor mode or clock synchronous mode, with FIFO selected	R
b9	MPB	Multi-Processor Bit Flag	Multi-processor bit associated with serial receive data (RDAT[8:0]): 0: Data transmission cycle 1: ID transmission cycle. MPB is valid only in asynchronous mode with SMR.MP = 1, and with FIFO selected.	R
b10	DR	Receive Data Ready Flag	This flag is the same as SSR_FIFO.DR: 0: Receiving is in progress, or no received data remains in FRDRH and FRDRL after successfully completed reception 1: Next receive data is not received for a period after successfully completed reception.	R*1
b11	PER	Parity Error Flag	0: No parity error occurred in the first data of FRDRH and FRDRL 1: Parity error occurred in the first data of FRDRH and FRDRL.	R
b12	FER	Framing Error Flag	0: No framing error occurred in the first data of FRDRH and FRDRL 1: Framing error occurred in the first data of FRDRH and FRDRL.	R
b13	ORER	Overrun Error Flag	This flag is the same as SSR_FIFO.ORER: 0: No overrun error occurred 1: Overrun error occurred.	R*1
b14	RDF	Receive FIFO Data Full Flag	This flag is the same as SSR_FIFO.RDF: 0: The amount of receive data written in FRDRH and FRDRL is less than the specified receive triggering number 1: The amount of receive data written in FRDRH and FRDRL is equal to or greater than the specified receive triggering number.	R*1
b15	—	Reserved	This bit is read as 0	R

Note 1. If this flag is read, it indicates the same value as that read from the SSR_FIFO register. Write 0 to the SSR_FIFO register to clear the flag.

FRDRHL is a 16-bit register that consists of the 8-bit FRDRH and FRDRL registers.

FRDRH and FRDRL constitute a 16-stage FIFO register that stores serial receive data and related status information readable by software. This register is only valid in asynchronous mode, including multi-processor mode, or clock synchronous mode.

The SCI completes reception of one frame of serial data by transferring the received data from the RSR register into FRDRH and FRDRL for storage. Continuous reception is executed until 16 stages are stored. If data is read when there is no received data in FRDRH and FRDRL, the value is undefined. When FRDRH and FRDRL are full of receive data, subsequent serial receive data is lost. The CPU can read from FRDRH and FRDRL but cannot write to them.

Reading 1 from the RDF, ORER, or DR flag of the FRDRH register is the same as reading from those bits in the SSR_FIFO register. When writing 0 to clear a flag in the SSR_FIFO register after reading the FRDRH register, write 0 only to the flag that is to be cleared and write 1 to the other flags.

When reading both the FRDRH and FRDRL registers, read in the order from FRDRH to FRDRL. The FDRHL register can be accessed in 16-bit units.

27.2.5 Transmit Data Register (TDR)

Address(es): SCI0.TDR 4007 0003h, SCI1.TDR 4007 0023h, SCI2.TDR 4007 0043h, SCI3.TDR 4007 0063h, SCI4.TDR 4007 0083h, SCI8.TDR 4007 0103h, SCI9.TDR 4007 0123h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

TDR is an 8-bit register that stores transmit data.

When the SCI detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts transmission.

The double-buffered structure of TDR and TSR enables continuous serial transmission. If the next transmit data is already written to TDR when one frame of data is transmitted, the SCI transfers the written data to TSR to continue transmission.

The CPU can read from or write to TDR at any time. Only write transmit data to TDR once after each instance of the transmit data empty interrupt (SCIn_TXI).

27.2.6 Transmit 9-Bit Data Register (TDRHL)

Address(es): SCI0.TDRHL 4007 000Eh, SCI1.TDRHL 4007 002Eh, SCI2.TDRHL 4007 004Eh, SCI3.TDRHL 4007 006Eh, SCI4.TDRHL 4007 008Eh, SCI8.TDRHL 4007 010Eh, SCI9.TDRHL 4007 012Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TDRHL is a 16-bit register that stores transmit data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of TDRHL are the shadow register of TDR, so access to TDRHL affects the TDR register. Access to the TDRHL register is prohibited if 7-bit or 8-bit data length is selected. When empty space is detected in the TSR register, the transmit data stored in the TDRHL register is transferred to TSR and transmission starts.

The TSR and TDRHL registers have a double-buffered structure to support continuous transmission. When the next data to be transmitted is stored in TDRHL after one frame of data is transmitted, the transmitting operation continues by transferring the data from the TDRHL register to the TSR register.

The CPU can read from and write to the TDRHL register. Bits [15:9] in TDRHL are fixed to 1. These bits are read as 1. The write value should be 1. Write transmit data to the TDRHL register only when a transmit data empty interrupt (SCIn_TXI) request is issued.

27.2.7 Transmit FIFO Data Register H, L, HL (FTDRH, FTDRL, FTDRHL)

Transmit FIFO Data Register H (FTDRH)

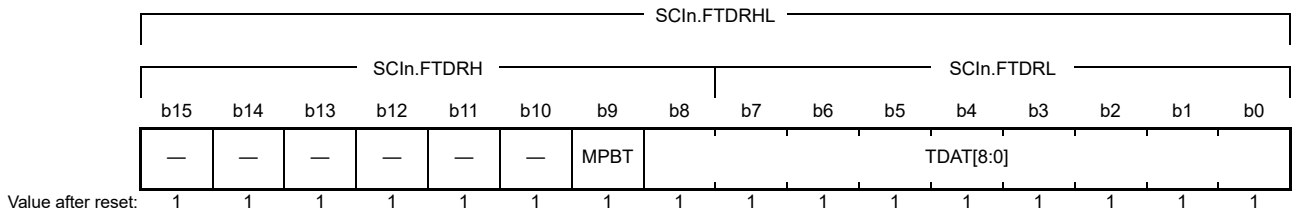
Address(es): SCI0.FTDRH 4007 000Eh, SCI1.FTDRH 4007 002Eh, SCI2.FTDRH 4007 004Eh, SCI3.FTDRH 4007 006Eh, SCI4.FTDRH 4007 008Eh, SCI8.FTDRH 4007 010Eh, SCI9.FTDRH 4007 012Eh

Transmit FIFO Data Register L (FTDRL)

Address(es): SCI0.FTDRL 4007 000Fh, SCI1.FTDRL 4007 002Fh, SCI2.FTDRL 4007 004Fh, SCI3.FTDRL 4007 006Fh, SCI4.FTDRL 4007 008Fh, SCI8.FTDRL 4007 010Fh, SCI9.FTDRL 4007 012Fh

Transmit FIFO Data Register HL (FTDRHL)

Address(es): SCI0.FTDRHL 4007 000Eh, SCI1.FTDRHL 4007 002Eh, SCI2.FTDRHL 4007 004Eh, SCI3.FTDRHL 4007 006Eh, SCI4.FTDRHL 4007 008Eh, SCI8.FTDRHL 4007 010Eh, SCI9.FTDRHL 4007 012Eh



Bit	Symbol	Bit name	Description	R/W
b8 to b0	TDAT[8:0]	Serial Transmit Data	Serial transmit data, valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, with FIFO selected	W
b9	MPBT	Multi-Processor Transfer Bit Flag	Specifies the multi-processor bit in the transmission frame: 0: Data transmission cycle 1: ID transmission cycle. Valid only in asynchronous mode with SMR.MP = 1 and FIFO selected.	W
b15 to b10	—	Reserved	The write value should be 1	W

FTDRHL is a 16-bit register that consists of 8-bit FTDRH and FTDRL registers.

FTDRH and FTDRL constitute a 16-stage FIFO register that stores data for serial transmission and a multi-processor transfer bit. This register is valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode.

When the SCI detects that the Transmit Shift Register (TSR) is empty, it transfers data written in the FTDRH and FTDRL registers to the TSR register and starts serial transmission. Continuous serial transmission is executed until no transmit data is left in FTDRH and FTDRL. When FTDRHL is full of transmit data, no more data can be written. If writing new data is attempted, the data is ignored. The CPU can write to the FTDRH and FTDRL registers but cannot read them.

When writing to both the FTDRH and FTDRL registers, write in the order from FTDRH to FTDRL.

MPBT flag (Multi-Processor Transfer Bit Flag)

The MPBT flag specifies the value of the multi-processor bit of the transmit frame. When FCR.FM = 1, SSR.MPBT is not valid.

27.2.8 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first automatically transfers transmit data from TDR, TDRHL, or transmit FIFO to TSR, then sends the data to the TXDn pin. The CPU cannot directly access the TSR.

27.2.9 Serial Mode Register (SMR) for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Address(es): SCI0.SMR 4007 0000h, SCI1.SMR 4007 0020h, SCI2.SMR 4007 0040h, SCI3.SMR 4007 0060h, SCI4.SMR 4007 0080h, SCI8.SMR 4007 0100h, SCI9.SMR 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLKA clock (n = 0)*1 0 1: PCLKA/4 clock (n = 1)*1 1 0: PCLKA/16 clock (n = 2)*1 1 1: PCLKA/64 clock (n = 3)*1.	R/W*4
b2	MP	Multi-Processor Mode	Valid only in asynchronous mode: 0: Multi-processor communications function is disabled 1: Multi-processor communications function is enabled.	R/W*4
b3	STOP	Stop Bit Length	Valid only in asynchronous mode: 0: 1 stop bit 1: 2 stop bits.	R/W*4
b4	PM	Parity Mode	Valid only when the PE bit is 1: 0: Even parity is selected 1: Odd parity is selected.	R/W*4
b5	PE	Parity Enable	Valid only in asynchronous mode: • When transmitting: 0: Parity bit is not added 1: Parity bit is added. • When receiving: 0: Parity bit is not checked 1: Parity bit is checked.	R/W*4
b6	CHR	Character Length	Valid only in asynchronous mode*2. Selects the transmit/receive character length in combination with the SCMR.CHR1 bit: CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length*3.	R/W*4
b7	CM	Communication Mode	0: Asynchronous mode or simple IIC mode 1: Clock synchronous mode or simple SPI mode.	R/W*4

Note 1. n is the decimal notation of the value of n in BRR, see section 27.2.17, Bit Rate Register (BRR).
Note 2. In any mode other than asynchronous mode, this bit setting is invalid and a fixed data length of 8 bits is used.
Note 3. LSB-first is fixed and the MSB bit [7] in TDR is not transmitted.
Note 4. Writable only when SCR.TE = 0 and SCR.RE = 0 (both serial transmission and reception are disabled).

The SMR register sets the communication format and the clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator.

For the relationship between the settings of these bits and the baud rate, see section 27.2.17, Bit Rate Register (BRR).

MP bit (Multi-Processor Mode)

The MP bit disables or enables the multi-processor communications function. The settings of the PE and PM bits are invalid in multi-processor mode.

STOP bit (Stop Bit Length)

The STOP bit selects the stop bit length in transmission.

In reception, only the first stop bit is checked regardless of this bit setting. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

PM bit (Parity Mode)

The PM bit selects the parity mode (even or odd) for transmission and reception.

The PM bit setting is invalid in multi-processor mode.

PE bit (Parity Enable)

When the PE bit is set to 1, the parity bit is added to transmit data, and the parity bit is checked at reception.

Regardless of the PE bit setting, the parity bit is not added or checked in multi-processor format.

CHR bit (Character Length)

The CHR bit selects the data length for transmission and reception in combination with the SCMR.CHR1 bit.

In modes other than asynchronous, a fixed data length of 8 bits is used.

CM bit (Communication Mode)

The CM bit selects the communication mode:

- Asynchronous mode or simple IIC mode
- Clock synchronous mode or simple SPI mode.

27.2.10 Serial Mode Register for Smart Card Interface Mode (SMR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SMR_SMCI 4007 0000h, SCI1.SMR_SMCI 4007 0020h, SCI2.SMR_SMCI 4007 0040h, SCI3.SMR_SMCI 4007 0060h, SCI4.SMR_SMCI 4007 0080h, SCI8.SMR_SMCI 4007 0100h, SCI9.SMR_SMCI 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLKA clock (n = 0)*1 0 1: PCLKA/4 clock (n = 1)*1 1 0: PCLKA/16 clock (n = 2)*1 1 1: PCLKA/64 clock (n = 3)*1.	R/W*2
b3, b2	BCP[1:0]	Base Clock Pulse	Selects the number of base clock cycles in combination with the SCMR.BCP2 bit. Table 27.3 lists the combinations of the SCMR.BCP2 and SMR.BCP[1:0] bits.	R/W*2

Bit	Symbol	Bit name	Description	R/W
b4	PM	Parity Mode	Valid only when the PE bit is 1: 0: Even parity is selected 1: Odd parity is selected.	R/W*2
b5	PE	Parity Enable	When this bit is set to 1, a parity bit is added to transmit data, and the parity of received data is checked. Set this bit to 1 in smart card interface mode.	R/W*2
b6	BLK	Block Transfer Mode	0: Non-block transfer mode operation 1: Block transfer mode operation.	R/W*2
b7	GM	GSM Mode	0: Non-GSM mode operation 1: GSM mode operation.	R/W*2

Note 1. n is the decimal notation of the value of n in BRR, see section 27.2.17, Bit Rate Register (BRR).
Note 2. Writable only when SCR_SMCI.TE = 0 and SCR_SMCI.RE = 0 (both serial transmission and reception are disabled).

The SMR_SMCI register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bit (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator.

For the relationship between the settings of these bits and the baud rate, see section 27.2.17, Bit Rate Register (BRR).

BCP[1:0] bits (Base Clock Pulse)

The BCP[1:0] bits select the number of base clock cycles in a 1-bit data transfer time in smart card interface mode.

Set these bits in combination with the SCMR.BCP2 bit.

For details, see section 27.6.4, Receive Data Sampling Timing and Reception Margin.

Table 27.3 Combinations of SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
0	00	93 clock cycles (S = 93)*1
0	01	128 clock cycles (S = 128)*1
0	10	186 clock cycles (S = 186)*1
0	11	512 clock cycles (S = 512)*1
1	00	32 clock cycles (S = 32)*1 (initial value)
1	01	64 clock cycles (S = 64)*1
1	10	372 clock cycles (S = 372)*1
1	11	256 clock cycles (S = 256)*1

Note 1. S is the value of S in BRR, see section 27.2.17, Bit Rate Register (BRR).

PM bit (Parity Mode)

The PM bit selects the parity mode for transmission and reception (even or odd). For details on the usage of this bit in smart card interface mode, see section 27.6.2, Data Format (Except in Block Transfer Mode).

PE bit (Parity Enable)

Set the PE bit to 1. The parity bit is added to the transmit data before transmission, and the parity bit is checked at reception.

BLK bit (Block Transfer Mode)

Set the BLK bit to 1 to enable the block transfer mode operation. For details, see section 27.6.3, Block Transfer Mode.

GM bit (GSM Mode)

Set the GM bit to 1 to enable GSM mode operation. In GSM mode, the SSR_SMCI.TEND flag set timing is moved forward to 11.0 ETUs (elementary time unit = 1-bit transfer time) from the start bit, and the clock output control function is enabled. For details, see section 27.6.6, Serial Data Transmission (Except in Block Transfer Mode) and section 27.6.8, Clock Output Control.

27.2.11 Serial Control Register (SCR) for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Address(es): SCI0.SCR 4007 0002h, SCI1.SCR 4007 0022h, SCI2.SCR 4007 0042h, SCI3.SCR 4007 0062h, SCI4.SCR 4007 0082h, SCI8.SCR 4007 0102h, SCI9.SCR 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	• Asynchronous mode: b1 b0 0 0: On-chip baud rate generator. The SCKn pin is available for use as an I/O port based on the I/O port settings. 0 1: On-chip baud rate generator. A clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock. A clock with a frequency 16 times the bit rate should be input from the SCKn pin when the SEMR.ABCS bit is 0. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. • Clock synchronous mode: b1 b0 0 x: Internal clock. The SCKn pin functions as the clock output pin. 1 x: External clock. The SCKn pin functions as the clock input pin.	R/W*1
b2	TEIE	Transmit End Interrupt Enable	0: An SCIn_TEI interrupt request is disabled 1: An SCIn_TEI interrupt request is enabled.	R/W
b3	MPIE	Multi-Processor Interrupt Enable	Valid in asynchronous mode when SMR.MP = 1: 0: Non-multi-processor reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in SSR to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically set to 0, and non-multi-processor reception is resumed.	R/W*3
b4	RE	Receive Enable	0: Serial reception is disabled 1: Serial reception is enabled.	R/W*2
b5	TE	Transmit Enable	0: Serial transmission is disabled 1: Serial transmission is enabled.	R/W*2
b6	RIE	Receive Interrupt Enable	0: SCIn_RXI and SCIn_ERI interrupt requests are disabled 1: SCIn_RXI and SCIn_ERI interrupt requests are enabled.	R/W
b7	TIE	Transmit Interrupt Enable	0: An SCIn_TXI interrupt request is disabled 1: An SCIn_TXI interrupt request is enabled.	R/W

x: Don't care

Note 1. Writable only when TE = 0 and RE = 0.

Note 2. 1 can be written only when TE = 0 and RE = 0, when the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written to TE and RE. When the SMR.CM bit is 0 and the SIMR1.IICM bit is 0, writing is enabled under any condition.

Note 3. When writing a new value to a bit other than the MPIE bit of this register in multi-processor mode (SMR.MP bit = 1), write 0 to the MPIE bit using the store instruction to avoid accidentally setting the MPIE bit to 1 by a read-modify-write operation when using a bit manipulation instruction.

The SCR controls operation and clock source selection for transmission and reception.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits select the clock source and the SCKn pin function.

TEIE bit (Transmit End Interrupt Enable)

The TEIE bit enables or disables an SCIn_TEI interrupt request. Set the TEIE bit to 0 to disable the SCIn_TEI interrupt request.

In simple IIC mode, SCIn_TEI is allocated to the interrupt on completion of issuing a start, restart, or stop condition (STIn). In this case, the TEIE bit can be used to enable or disable the STI.

MPIE bit (Multi-Processor Interrupt Enable)

When the MPIE bit is set to 1 and data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, RDF, ORER, and FER in SSR/SSR_FIFO to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically set to 0, and non-multi-processor reception resumes. For details, see section 27.4, Multi-Processor Communication Function.

When the MPB bit in the SSR is 0, the receive data is not transferred from the RSR to the RDR, a receive error is not detected, and setting the flags ORER and FER to 1 is disabled.

When the MPB bit is 1, the MPIE bit is automatically set to 0, SCIn_RXI and SCIn_ERI interrupt requests are enabled (if the RIE bit in SCR is set to 1), and setting of the ORER and FER flags to 1 is enabled.

Set MPIE to 0 if the multi-processor communications function is not used.

RE bit (Receive Enable)

The RE bit enables or disables serial reception.

When this bit is set to 1, serial reception starts by detecting the start bit in asynchronous mode or the synchronous clock input in clock synchronous mode. Set the reception format in the SMR register before setting the RE bit to 1.

When non-FIFO operation is selected and reception is halted by setting the RE bit to 0, the RDRF, ORER, FER, and PER flags in the SSR register are not affected, and the previous values are saved.

When FIFO operation is selected and reception is halted by setting the RE bit to 0, the RDF, ORER, FER, PER, and DR flags in SSR_FIFO are not affected and the previous values are saved.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission.

When the TE bit is set to 1, serial transmission starts by writing transmit data to TDR. Set the transmission format in the SMR register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

Setting the RIE bit to 0 disables SCIn_RXI and SCIn_ERI interrupt requests.

To cancel an SCIn_ERI interrupt request, read 1 from the ORER, FER, or PER flag in SSR/SSR_FIFO, then set the flag to 0, or set the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt requests.

Setting the TIE bit to 0 disables an SCIn_TXI interrupt request. For the SCIn_TXI interrupt to occur, set the TE and TIE bits to 1 simultaneously, before transfer starts.

27.2.12 Serial Control Register for Smart Card Interface Mode (SCR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SCR_SMCI 4007 0002h, SCI1.SCR_SMCI 4007 0022h, SCI2.SCR_SMCI 4007 0042h, SCI3.SCR_SMCI 4007 0062h, SCI4.SCR_SMCI 4007 0082h, SCI8.SCR_SMCI 4007 0102h, SCI9.SCR_SMCI 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	• When GM in SMR_SMCI = 0: b1 b0 0 0: Output disabled. The SCKn pin is available for use as an I/O port based on the I/O port settings 0 1: Output clock 1 x: Setting prohibited. • When GM in SMR_SMCI = 1: b1 b0 0 0: Output fixed low x 1: Output clock 1 0: Output fixed high.	R/W*1
b2	TEIE	Transmit End Interrupt Enable	This bit should be 0 in smart card interface mode	R/W
b3	MPIE	Multi-Processor Interrupt Enable	This bit should be 0 in smart card interface mode	R/W
b4	RE	Receive Enable	0: Serial reception is disabled 1: Serial reception is enabled.	R/W*2
b5	TE	Transmit Enable	0: Serial transmission is disabled 1: Serial transmission is enabled.	R/W*2
b6	RIE	Receive Interrupt Enable	0: SCIn_RXI and SCIn_ERI interrupt requests are disabled 1: SCIn_RXI and SCIn_ERI interrupt requests are enabled.	R/W
b7	TIE	Transmit Interrupt Enable	0: SCIn_TXI interrupt request is disabled 1: SCIn_TXI interrupt request is enabled.	R/W

x: Don't care
Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0. After setting TE or RE to 1, only 0 can be written to TE and RE.

The SCR_SMCI sets transmission and reception control, interrupt control, and clock source selection for transmission and reception.

For details on interrupt requests, see section 27.10, Interrupt Sources.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits control the clock output from the SCKn pin.

In GSM mode, clock output can be dynamically switched. For details, see section 27.6.8, Clock Output Control.

TEIE bit (Transmit End Interrupt Enable)

Set the TEIE bit to 0 in smart card interface mode.

MPIE bit (Multi-Processor Interrupt Enable)

Set the MPIE bit to 0 in smart card interface mode.

RE bit (Receive Enable)

The RE bit enables or disables serial reception.

When this bit is set to 1, serial reception starts by detecting the start bit. Set the reception format in the SMR_SMCI register before setting the RE bit to 1.

If reception is halted by setting the RE bit to 0, the ORER, FER, and PER flags in SSR_SMCI are not affected and the previous values are saved.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission. When this bit is set to 1, serial transmission starts by writing transmit data to TDR. Set the transmission format in the SMR_SMCI register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

Setting the RIE bit to 0 disables SCIn_RXI and SCIn_ERI interrupt requests.

To cancel an SCIn_ERI interrupt request, read 1 from the ORER, FER, or PER flag in the SSR_SMCI register, then set the flag to 0, or set the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables an SCIn_TXI interrupt request.

Setting the TIE bit to 0 disables an SCIn_TXI interrupt request. Set the TIE bit to 1 while the TE bit is 1. For the SCIn_TXI interrupt to occur, set the TE and TIE bits to 1 simultaneously before transfer starts.

27.2.13 Serial Status Register (SSR) for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0)

Address(es): SCI0.SSR 4007 0004h, SCI1.SSR 4007 0024h, SCI2.SSR 4007 0044h, SCI3.SSR 4007 0064h, SCI4.SSR 4007 0084h, SCI8.SSR 4007 0104h, SCI9.SSR 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	Value of the multi-processor bit in the transmission frame: 0: Data transmission cycle 1: ID transmission cycle.	R/W
b1	MPB	Multi-Processor	Value of the multi-processor bit in the reception frame: 0: Data transmission cycle 1: ID transmission cycle.	R
b2	TEND	Transmit End Flag	0: A character is being transmitted 1: Character transfer is complete.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*1
b4	FER	Framing Error Flag	0: No framing error occurred 1: Framing error occurred.	R/(W)*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: Overrun error occurred.	R/(W)*1
b6	RDRF	Receive Data Full Flag	0: No received data in RDR register 1: Received data in RDR register.	R/(W)*1
b7	TDRE	Transmit Data Empty Flag	0: Transmit data in TDR register 1: No transmit data in TDR register.	R/(W)*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR register provides the SCI status flags and transmission/reception multi-processor bits.

MPBT bit (Multi-Processor Bit Transfer)

The MPBT bit selects the multi-processor bit in the transmit frame.

MPB bit (Multi-Processor)

The MPB bit holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

TEND flag (Transmit End Flag)

The TEND flag indicates completion of transmission.

[Setting conditions]

- When the SCR.TE bit is set to 0 to disable serial transmission and the FCR.FM bit is set to 0 (non-FIFO selected)
- When the SCR.TE bit is set to 1, the TEND flag is not affected and keeps the value 1
- When the TDR register is not updated on transmission of the tail-end bit of a character.

[Clearing conditions]

- When transmit data is written to the TDR register when the SCR.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 when the SCR.TE bit is 1.

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When a parity error is detected during reception in asynchronous mode and the address match function is disabled (DCCR.DCME = 0).

  Although receive data is transferred to the RDR register when the parity error occurs, no SCIn_RXI interrupt request occurs. When the PER flag is set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to the PER flag after reading PER = 1. After writing 0 to this flag, read it to verify that its value is 0.

When the SCR.RE bit is set to 0 to disable serial reception, the PER flag is not affected and keeps its previous value.

FER flag (Framing Error Flag)

The FER flag indicates that a framing error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When 0 is sampled as the stop bit during reception in asynchronous mode and the address match function is disabled (DCCR.DCME = 0).

  In 2-stop-bit mode, only the first stop bit is checked, but the second stop bit is not checked. Although receive data is transferred to the RDR register when the framing error occurs, no SCIn_RXI interrupt request occurs. Also, when the FER flag is set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to the FER flag after reading FER = 1. After writing 0 to this flag, read it to verify that its value is 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the FER flag is not affected and keeps its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ended abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error and a framing error is read from RDR.

  In RDR, data received prior to an overrun error occurrence is saved, but data received after the overrun error is lost. When the ORER flag is set to 1, data received is not forwarded to the RDR register. In clock synchronous mode, serial transmission and reception are stopped.

[Clearing condition]

- When 0 is written to the ORER flag after 1 is read. After writing 0 to this flag, read it to verify that its value is 0.

When the SCR.RE bit is set to 0 to disable serial reception, the ORER flag is not affected and keeps its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to RDRF flag after 1 is read
- When data is read from the RDR register.

Note: Do not clear RDRF flag by accessing RDRF bit in SSR register unless communication is aborted.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR.TE bit is 0
- When data is transmitted from the TDR register to the TSR register.

[Clearing conditions]

- When 0 is written to TDRE flag after 1 is read
- When the SCR.TE bit is 1 and data is written to the TDR register.

Note: Do not clear TDRE flag by accessing TDRE in the SSR register unless communication is aborted.

27.2.14 Serial Status Register for Non-Smart Card Interface and FIFO Mode (SSR_FIFO) (SCMR.SMIF = 0 and FCR.FM = 1)

Address(es): SCI0.SSR_FIFO 4007 0004h, SCI1.SSR_FIFO 4007 0024h, SCI2.SSR_FIFO 4007 0044h, SCI3.SSR_FIFO 4007 0064h, SCI4.SSR_FIFO 4007 0084h, SCI8.SSR_FIFO 4007 0104h, SCI9.SSR_FIFO 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDFE	RDF	ORER	FER	PER	TEND	—	DR
Value after reset:	1	0	0	0	0	0	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	DR	Receive Data Ready Flag	0: Reception is in progress, or no received data remains in FRDRHL after successfully completed reception (receive FIFO is empty) 1: Next receive data is not received for a period after successfully completed reception, and when the amount of data stored in the FIFO is equal to or less than the receive triggering number.	R/(W)*1
b1	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b2	TEND	Transmit End Flag	0: A character is being transmitted 1: Character transfer is complete.	R/(W)*1
b3	PER	Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*1
b4	FER	Framing Error Flag	0: No framing error occurred 1: Framing error occurred.	R/(W)*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: Overrun error occurred.	R/(W)*1
b6	RDF	Receive FIFO Data Full Flag	0: The amount of receive data written in FRDRHL is less than the specified receive triggering number 1: The amount of receive data written in FRDRHL is equal to or greater than the specified receive triggering number.	R/(W)*1
b7	TDFE	Transmit FIFO Data Empty Flag	0: The amount of transmit data written in FTDRHL exceeds the specified transmit triggering number 1: The amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number.	R/(W)*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR_FIFO register provides the SCI with FIFO mode status flags.

DR flag (Receive Data Ready Flag)

The DR flag indicates that the amount of data stored in the Receive FIFO Data Register (FRDRHL) falls below the specified receive triggering number, and that no next data is received after 15 ETUs (elementary time units) from the last stop bit in asynchronous mode. This flag is valid only in asynchronous mode, including multi-processor mode, and when FIFO operation is selected. In clock synchronous mode, this flag is not set to 1.

[Setting condition]

- When FRDRHL contains less data than the specified receive triggering number, and no next data is received after 15 ETUs*1 from the last stop bit, and the SSR_FIFO.FER and SSR_FIFO.PER flags are 0.

[Clearing conditions]

- When 1 is read from DR, after all received data is read
- When the FCR.FM bit is changed from 0 to 1.

Note 1. This is equivalent to 1.5 frames in the 8-bit format with one stop bit.
The DR flag is only set to 1 when FIFO is selected in asynchronous mode, including multi-processor mode. It is not set to 1 in other operation modes.

TEND flag (Transmit End Flag)

The TEND flag indicates that FTDRHL does not contain valid data when transmitting the last bit of a serial character, so the transmission is halted.

[Setting condition]

- TEND is set to 1 when FTDRHL does not contain transmit data when the last bit of a 1-byte serial character is transmitted.

[Clearing conditions]

- When transmit data is written to FTDRHL when the SCR.TE bit is 1
- When 0 is written to TEND after 1 is read, when the SCR.TE bit is 1
- When the FCR.FM bit is changed from 0 to 1.

PER flag (Parity Error Flag)

The PER flag indicates whether there is a parity error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When data is received and a parity error is detected, and the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to PER after 1 is read.

The receive operation is continuous when receive data is stored in the FRDRHL register even when a parity error occurs during reception.

When the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and keeps its previous value.

FER flag (Framing Error Flag)

The FER flag indicates whether there is a framing error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When 0 is sampled as the stop bit during reception and the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to FER after 1 is read.

The receive operation is continuous, and receive data is stored to the FRDRHL register even when a framing error occurs during reception.

When the SCR.RE bit is set to 0 (serial reception is disabled), the FER flag is not affected and keeps its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that the receive operation stopped abnormally because an overrun error occurred.

[Setting condition]

- When the next serial reception completes while the receive FIFO is full with 16-byte receive data.

[Clearing condition]

- When 0 is written to ORER after 1 is read.

When the SCR.RE bit is set to 0 (serial reception is disabled), the ORER flag is not affected and keeps its previous value.

RDF flag (Receive FIFO Data Full Flag)

The RDF flag indicates that receive data is transferred to the FRDRHL register, and the amount of data in FRDRHL is equal to or exceeds the specified receive triggering number. When RTRG is set to 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0.

[Setting condition]

- When the amount of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL,*1 and the FIFO is not empty.

[Clearing conditions]

- When 0 is written to RDF after 1 is read
- When FRDRHL is read by the DMAC or DTC, but only when the block transfer is the last transmission
- When the setting and clearing conditions occur at the same time, the RDF flag is 0. After that, when the amount of data stored in the FRDRHL register is equal to or greater than the RTRG value, RDF is set to 1 after 1 PCLKA.

Note: Do not clear the RDF flag by accessing RDF in the SSR register before reading receive data unless communication is aborted.

Note 1. Because FRDRHL is a 16-stage FIFO register, the maximum amount of data that can be read when RDF is 1 is equivalent to the specified receive triggering number. If an attempt is made to read after all the data in FRDRHL is read, the data is undefined.

TDFE flag (Transmit FIFO Data Empty Flag)

The TDFE flag indicates that when data is transferred from the FTDRHL register into the TSR register, the amount of data in FTDRHL is less than the specified transmit triggering number, and writing of transmit data to FTDRHL is enabled.

[Setting conditions]

- When the TE bit in SCR is 0
- When the amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number.*1

[Clearing conditions]

- When writing to FTDRHL is executed on the last transmission while the DMAC or DTC is activated
- When 0 is written to the TDFE flag after 1 is read.
  The setting conditions are given priority when TE = 0. When the setting and clearing conditions occur at the same time, the TDFE flag is 0. After that, when the amount of data stored in the FTDRHL register is equal to or less than the TTRG value, TDFE is set to 1 after 1 PCLKA.

Note: Do not clear the TDFE flag by accessing TDFE in the SSR register before writing transmit data unless communication is aborted.

Note 1. Because the FTDRHL register is a 16-stage FIFO register, the maximum amount of data that can be written when the TDFE flag is set to 1 is 16 minus FDR.T[4:0]. If more data is written, data is discarded.

27.2.15 Serial Status Register for Smart Card Interface Mode (SSR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SSR_SMCI 4007 0004h, SCI1.SSR_SMCI 4007 0024h, SCI2.SSR_SMCI 4007 0044h, SCI3.SSR_SMCI 4007 0064h, SCI4.SSR_SMCI 4007 0084h, SCI8.SSR_SMCI 4007 0104h, SCI9.SSR_SMCI 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	Set this bit to 0 in smart card interface mode	R/W
b1	MPB	Multi-Processor	Set this bit to 0 in smart card interface mode	R
b2	TEND	Transmit End Flag	0: A character is being transmitted 1: Character transfer is complete.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*1
b4	ERS	Error Signal Status Flag	0: Low error signal is not sampled 1: Low error signal is sampled.	R/(W)*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: Overrun error occurred.	R/(W)*1
b6	RDRF	Receive Data Full Flag	0: No received data in RDR register 1: Received data in RDR register.	R/(W)*1
b7	TDRE	Transmit Data Empty Flag	0: Transmit data in TDR register 1: No transmit data in TDR register.	R/(W)*1

Note 1. Only 0 can be written to clear the flag after 1 is read.

The SSR_SMCI register provides SCI with smart card interface mode status flags.

TEND flag (Transmit End Flag)

When there is no error signal from the receiving side, the TEND flag is set to 1 when more data is ready to be transferred to the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit = 0 (serial transmission is disabled). When the SCR_SMCI.TE bit changes from 0 to 1, the TEND flag is not affected and keeps the value 1.
- When a specified period elapses after the latest transmission of 1 byte, the ERS flag is 0, and the TDR register is not updated.

  The set timing is determined by the following register settings:
  - When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 0, 12.5 ETUs after the start of transmission
  - When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 1, 11.5 ETUs after the start of transmission
  - When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 0, 11.0 ETUs after the start of transmission
  - When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 1, 11.0 ETUs after the start of transmission.

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR_SMCI.TE bit is 1
- When 0 is written to TDRE after 1 is read while the SCR_SMCI.TE bit is 1.

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When a parity error is detected during reception. Although receive data is transferred to RDR when a parity error occurs, no SCIn_RXI interrupt request occurs. After the PER flag is set to 1, the next receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after 1 is read. After writing 0 to the PER flag, read it to verify that its value is 0.

When the RE bit in SCR_SMCI is set to 0 (serial reception is disabled), the PER flag is not affected and keeps its previous value.

ERS flag (Error Signal Status Flag)

[Setting condition]

- When a low error signal is sampled.

[Clearing condition]

- When 0 is written to the ERS flag after 1 is read.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ended abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error is read from the RDR register. The data received before an overrun error occurred is saved in the RDR, but data received after the overrun error is lost. When the ORER flag is set to 1, receive data is not forwarded to the RDR register.

[Clearing condition]

- When 0 is written to the ORER flag after 1 is read. After writing 0 to the ORER flag, read it to verify that its value is 0.

When the RE bit in SCR_SMCI is set to 0, the ORER flag is not affected and keeps its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to the RDRF flag after 1 is read
- When data is read from the RDR register.

Note: Do not clear the RDRF flag by accessing RDRF in the SSR register unless communication is aborted.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit is 0
- When data is transmitted from the TDR register to the TSR register.

[Clearing conditions]

- When 0 is written to the TDRE flag after 1 is read
- When the SCR_SMCI.TE bit is 1 and data is written to the TDR register.

Note: Do not clear TDRE flag by accessing TDRE in the SSR register unless communication is aborted.

27.2.16 Smart Card Mode Register (SCMR)

Address(es): SCI0.SCMR 4007 0006h, SCI1.SCMR 4007 0026h, SCI2.SCMR 4007 0046h, SCI3.SCMR 4007 0066h, SCI4.SCMR 4007 0086h, SCI8.SCMR 4007 0106h, SCI9.SCMR 4007 0126h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
Value after reset:	1	1	1	1	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	SMIF	Smart Card Interface Mode Select	0: Non-smart card interface mode (asynchronous mode, clock synchronous mode, simple SPI mode, or simple IIC mode) 1: Smart card interface mode.	R/W*1
b1	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b2	SINV	Transmitted/Received Data Invert	0: TDR register contents are transmitted as is. Receive data is stored as received in the RDR. 1: TDR register contents are inverted before transmitted. Receive data is stored in inverted form in the RDR. This bit can be used in the following modes: • Smart card interface mode • Asynchronous mode including multi-processor mode • Clock synchronous mode • Simple SPI mode. Set this bit to 0 for operation in simple IIC mode.	R/W*1
b3	SDIR	Transmitted/Received Data Transfer Direction	0: Transfer with LSB-first 1: Transfer with MSB-first. This bit can be used in the following modes: • Smart card interface mode • Asynchronous mode including multi-processor mode • Clock synchronous mode • Simple SPI mode. Set this bit to 1 for operation in simple IIC mode.	R/W*1
b4	CHR1	Character Length 1	Valid only in asynchronous mode.*2 Selects the transmit/receive character length in combination with the SMR.CHR bit: CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length.*3	R/W*1
b6, b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b7	BCP2	Base Clock Pulse 2	Selects the number of base clock cycles in combination with the SMR_SMCI.BCP[1:0] bits. Table 27.4 lists the combinations of the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits.	R/W*1

Note 1. Writable only when the TE and RE bits in SCR/SCR_SMCI are 0 (both serial transmission and reception are disabled).
Note 2. The setting is invalid and a fixed data length of 8 bits is used in modes other than asynchronous mode.
Note 3. LSB-first should be selected and the value of the MSB bit [7] in TDR cannot be transmitted.

The SCMR register selects the smart card interface and communication format.

SMIF bit (Smart Card Interface Mode Select)

Setting the SMIF bit to 1 selects the smart card interface mode. Setting it to 0 selects all other modes as follows:

- Asynchronous mode, including multi-processor mode
- Clock synchronous mode
- Simple SPI mode
- Simple IIC mode.

SINV bit (Transmitted/Received Data Invert)

The SINV bit inverts the transmit/receive data logic level. This bit does not affect the logic level of the parity bit. To invert the parity bit, invert the PM bit in SMR or SMR_SMCI.

CHR1 bit (Character Length 1)

The CHR1 bit selects the data length of transmit/receive data in combination with the CHR bit in SMR.

A fixed data length of 8 bits is used in modes other than asynchronous mode.

BCP2 bit (Base Clock Pulse 2)

The BCP2 bit selects the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set this bit in combination with the SMR_SMCI.BCP[1:0] bits.

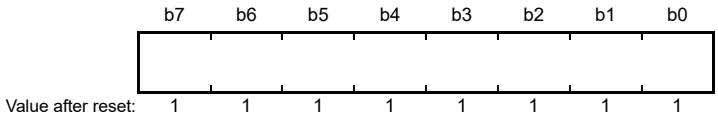
Table 27.4 Combinations of SCMR.BCP2 bit and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
0	00	93 clock cycles (S = 93)*1
0	01	128 clock cycles (S = 128)*1
0	10	186 clock cycles (S = 186)*1
0	11	512 clock cycles (S = 512)*1
1	00	32 clock cycles (S = 32)*1 (initial value)
1	01	64 clock cycles (S = 64)*1
1	10	372 clock cycles (S = 372)*1
1	11	256 clock cycles (S = 256)*1

Note 1. For S, see section 27.2.17, Bit Rate Register (BRR).

27.2.17 Bit Rate Register (BRR)

Address(es): SCI0.BRR 4007 0001h, SCI1.BRR 4007 0021h, SCI2.BRR 4007 0041h, SCI3.BRR 4007 0061h, SCI4.BRR 4007 0081h, SCI8.BRR 4007 0101h, SCI9.BRR 4007 0121h



BRR is an 8-bit register that adjusts the bit rate.

As each SCI channel has independent baud rate generator control, different bit rates can be set for each channel. Table 27.5 shows the relationship between the setting (N) and the bit rate (B) in the BRR for asynchronous mode, multi-processor transfer, clock synchronous mode, smart card interface mode, simple SPI mode, and simple IIC mode.

The initial value of the BRR register is FFh. The BRR can be read by the CPU, but can only be written to when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 27.5 Relationship between N setting in BRR and bit rate B

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCSE bit		
Asynchronous, multiprocessor transfer	0	0	0	$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	1	0	0	$N = \frac{PCLKA \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLKA \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLKA \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
Clock synchronous, simple SPI				$N = \frac{PCLKA \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	-
Smart card interface				$N = \frac{PCLKA \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\} \times 100$
Simple IIC*1				$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	-

B: Bit rate (bps)
N: BRR setting for on-chip baud rate generator ($0 \le N \le 255$)
PCLKA: Operating frequency (MHz)
n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 27.7 and Table 27.8.

Note 1. Adjust the bit rate so that the high and low-level widths of the SCLn output in simple IIC mode satisfy the I^2C bus standard.

Table 27.6 Calculating widths at high and low level for SCL

Mode	SCL	Formula (result in seconds)
Simple IIC	Width at high level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLKA \times 10^6}$
	Width at low level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLKA \times 10^6}$

Table 27.7 Clock source settings

SMR or SMR_SMCI.CKS[1:0] bit setting		
CKS[1:0] bits	Clock source	n
0 0	PCLKA clock	0
0 1	PCLKA/4 clock	1
1 0	PCLKA/16 clock	2
1 1	PCLKA/64 clock	3

Table 27.8 Base clock settings in smart card interface mode

SCMR.BCP2 bit setting	SMR_SMCI.BCP[1:0] bit setting	Base clock cycles for 1-bit period	S
0	0 0	93 clock cycles	93
0	0 1	128 clock cycles	128
0	1 0	186 clock cycles	186
0	1 1	512 clock cycles	512
1	0 0	32 clock cycles	32
1	0 1	64 clock cycles	64
1	1 0	372 clock cycles	372
1	1 1	256 clock cycles	256

Table 27.9 and Table 27.10 list examples of BRR (N) settings in asynchronous mode. Table 27.11 lists the maximum bit rate selectable for each operating frequency. Table 27.15 lists examples of BRR (N) settings in smart card interface mode.

Table 27.17 lists examples of BRR (N) settings in simple IIC mode. In smart card interface mode, the number of base clock cycles S in a 1-bit data transfer time can be selected. For details, see section 27.6.4, Receive Data Sampling Timing and Reception Margin. Table 27.12 and Table 27.14 list the maximum bit rates with external clock input.

When either the Asynchronous Mode Base Clock Select bit (ABCS) or the Baud Rate Generator Double-Speed Mode Select bit (BGDM) in the Serial Extended Mode Register (SEMR) is set to 1 in asynchronous mode, the bit rate becomes twice the value listed in Table 27.16. When both of those bits are set to 1, the bit rate becomes four times the listed value.

Table 27.9 Examples of BRR settings for different bit rates in asynchronous mode (1)

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	-0.26	2	177	-0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	-1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	-2.34	0	19	0.00
31250	0	7	0.00	0	9	-1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	-	-	-	0	7	0.00	0	7	1.73	0	9	-2.34	0	9	0.00

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	-0.17	3	70	0.03	3	75	0.48	3	79	-0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	45	-0.93	0	51	0.16	0	55	0.00	0	58	-0.69	0	63	0.00
19200	0	22	-0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	-1.70
38400	-	-	-	0	12	0.16	0	13	0.00	0	14	-2.34	0	15	0.00

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS and BGDM are set to 1, the bit rate quadruples.

Table 27.10 Examples of BRR settings for different bit rates in asynchronous mode (2)

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	-0.25	3	110	-0.02	3	132	0.13	3	145	0.33	3	177	-0.25
150	3	64	0.16	3	80	0.47	3	97	-0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	-0.15	2	194	0.16	2	214	-0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	-0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	-0.15	1	194	0.16	1	214	-0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	-0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	-0.15	0	194	0.16	0	214	-0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	-0.35	0	106	0.39	0	129	0.16
19200	0	32	-1.36	0	40	-0.76	0	48	-0.35	0	53	-0.54	0	64	0.16
31250	0	19	0.00	0	24	0.00	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	-0.54	0	32	-1.36

Bit rate (bps)	Operating frequency PCLKA (MHz)								
	50			60			120		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	221	-0.02	-	-	-	-	-	-
150	3	162	-0.15	3	194	0.16	-	-	-
300	3	80	0.47	3	97	-0.35	3	194	0.16
600	2	162	-0.15	3	48	-0.35	3	97	-0.35
1200	2	80	0.47	2	97	-0.35	3	48	-0.35
2400	1	162	-0.15	2	48	-0.35	2	97	-0.35
4800	1	80	0.47	1	97	-0.35	2	48	-0.35
9600	0	162	-0.15	1	48	-0.35	1	97	-0.35
19200	0	80	0.47	0	97	-0.35	1	48	-0.35
31250	0	49	0.00	0	59	0.00	0	119	0
38400	0	40	-0.76	0	48	-0.35	0	97	-0.35

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS and BGDM are set to 1, the bit rate quadruples.

Table 27.11 Maximum bit rate for each operating frequency in asynchronous mode (1 of 2)

PCLKA (MHz)	SEMR settings					Maximum bit rate (bps)	PCLKA (MHz)	SEMR settings					Maximum bit rate (bps)
	BGDM bit	ABCS bit	ABCSE bit	n	N			BGDM bit	ABCS bit	ABCSE bit	n	N	
8	0	0	0	0	0	250000	16	0	0	0	0	0	500000
		1	0	0	0	500000			1	0	0	0	1000000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1000000			1	0	0	0	2000000
	Don't care	Don't care	1	0	0	1333333		Don't care	Don't care	1	0	0	2666666
9.8304	0	0	0	0	0	307200	17.2032	0	0	0	0	0	537600
		1	0	0	0	614400			1	0	0	0	1075200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1228800			1	0	0	0	2150400
	Don't care	Don't care	1	0	0	1638400		Don't care	Don't care	1	0	0	2867200
10	0	0	0	0	0	312500	18	0	0	0	0	0	562500
		1	0	0	0	625000			1	0	0	0	1125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1250000			1	0	0	0	2250000
	Don't care	Don't care	1	0	0	1666666		Don't care	Don't care	1	0	0	3000000
12	0	0	0	0	0	375000	19.6608	0	0	0	0	0	614400
		1	0	0	0	750000			1	0	0	0	1228800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1500000			1	0	0	0	2457600
	Don't care	Don't care	1	0	0	2000000		Don't care	Don't care	1	0	0	3276800
12.288	0	0	0	0	0	384000	20	0	0	0	0	0	625000
		1	0	0	0	768000			1	0	0	0	1250000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1536000			1	0	0	0	2500000
	Don't care	Don't care	1	0	0	2048000		Don't care	Don't care	1	0	0	3333333
14	0	0	0	0	0	437500	25	0	0	0	0	0	781250
		1	0	0	0	875000			1	0	0	0	1562500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1750000			1	0	0	0	3125000
	Don't care	Don't care	1	0	0	2333333		Don't care	Don't care	1	0	0	4166666
30	0	0	0	0	0	937500	50	0	0	0	0	0	1562500
		1	0	0	0	1875000			1	0	0	0	3125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	3750000			1	0	0	0	6250000
	Don't care	Don't care	1	0	0	5000000		Don't care	Don't care	1	0	0	8333333
33	0	0	0	0	0	1031250	60	0	0	0	0	0	1875000
		1	0	0	0	2062500			1	0	0	0	3750000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	4125000			1	0	0	0	7500000
	Don't care	Don't care	1	0	0	5500000		Don't care	Don't care	1	0	0	10000000

Table 27.11 Maximum bit rate for each operating frequency in asynchronous mode (2 of 2)

PCLKA (MHz)	SEMR settings					Maximum bit rate (bps)	PCLKA (MHz)	SEMR settings					Maximum bit rate (bps)
	BGDM bit	ABCS bit	ABCSE bit	n	N			BGDM bit	ABCS bit	ABCSE bit	n	N	
40	0	0	0	0	0	1250000	120	0	0	0	0	0	3750000
		1	0	0	0	2500000			1	0	0	0	7500000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	5000000			1	0	0	0	15000000
	Don't care	Don't care	1	0	0	6666666		Don't care	Don't care	1	0	0	20000000

Table 27.12 Maximum bit rate with external clock input in asynchronous mode

		Maximum bit rate (bps)	
PCLKA (MHz)	External input clock (MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125000	250000
9.8304	2.4576	153600	307200
10	2.5000	156250	312500
12	3.0000	187500	375000
12.288	3.0720	192000	384000
14	3.5000	218750	437500
16	4.0000	250000	500000
17.2032	4.3008	268800	537600
18	4.5000	281250	562500
19.6608	4.9152	307200	614400
20	5.0000	312500	625000
25	6.2500	390625	781250
30	7.5000	468750	937500
33	8.2500	515625	1031250
40	10.0000	625000	1250000
50	12.5000	781250	1562500
60	15.0000	937500	1875000
120	30.0000	1875000	3750000

Table 27.13 BRR settings for different bit rates in clock synchronous and simple SPI modes (1 of 2)

Bit rate (bps)	Operating frequency PCLKA (MHz)																					
	8		10		16		20		25		30		33		40		50		60		120	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
250	3	124	—	—	3	249	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
500	2	249	—	—	3	124	—	—	x	x	3	233	x	x	x	x	x	x	x	x	x	x
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	155	3	194	3	233	x	x
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	249	3	77	3	93	3	186
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	124	2	155	3	46	3	93
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	249	2	77	2	93	3	46
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	99	1	124	1	149	2	74
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	49	1	61	1	74	1	149
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	99	0	124	0	149	1	74
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	39	0	49	0	59	1	29
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	19	0	24	0	29	1	14

Table 27.13 BRR settings for different bit rates in clock synchronous and simple SPI modes (2 of 2)

Bit rate (bps)	Operating frequency PCLKA (MHz)																					
	8		10		16		20		25		30		33		40		50		60		120	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
1 M	0	1			0	3	0	4	—	—	—	—	—	—	0	9	—	—	0	14	0	29
2.5 M	x	x	0	0*1	x	x	0	1	—	—	0	2	—	—	0	3	0	4	0	5	0	11
5 M	x	x	x	x	x	x	0	0*1	—	—	—	—	—	—	0	1	—	—	0	2	0	5
7.5 M	x	x	x	x	x	x	x	x	x	x	0	0*1	x	x	x	x	x	x	0	1	0	3
10 M	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0*1	x	x	x	x	0	2

x: Setting prohibited.

—: Can be set, but an error occurs.

Note 1. Continuous transmission or reception is not possible. After transmitting or receiving one frame of data, a 1-bit period elapses before starting to transmit or receive the next frame of data. The output of the synchronization clock is stopped for a 1-bit period. Therefore, it takes 9 bits worth of time to transfer one frame (8 bits) of data, and the average transfer rate is 8/9 times the bit rate. When the FIFO is selected, this setting (BRR = 00h and SMR.CKS[1:0] = 00b) is not available.

Table 27.14 Maximum bit rate with external clock input in clock synchronous mode and simple SPI mode

PCLKA (MHz)	External input clock (MHz)	Maximum bit rate (Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333
25	4.1667	4.1666667
30	5.0000	5.0000000
33	5.5000	5.5000000
40	6.6667	6.6666667
50	8.3333	8.3333333
60	10.0000	10.0000000
120	20.0000 (clock synchronous mode)	20.00000000
	10.0000 (simple SPI mode)	10.00000000

Table 27.15 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372

Bit rate (bps)	Operating frequency PCLKA (MHz)											
	7.1424			10.00			10.7136			13.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	-30	0	1	-25	0	1	-8.99

Bit rate (bps)	Operating frequency PCLKA (MHz)											
	14.2848			16.00			18.00			20.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	-15.99	0	2	-6.66

Bit rate (bps)	Operating frequency PCLKA (MHz)											
	25.00			30.00			33.00			40.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	-12.49	0	3	5.01	0	4	-7.59	0	5	–6.66

Bit rate (bps)	Operating frequency PCLKA (MHz)								
	50.00			60.00			120.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	6	0.01	0	7	5.01	0	16	–1.17

Table 27.16 Maximum bit rate for each operating frequency in smart card interface mode (S = 32)

PCLKA (MHz)	Maximum bit rate (bps)	n	N
10.00	156250	0	0
10.7136	167400	0	0
13.00	203125	0	0
16.00	250000	0	0
18.00	281250	0	0
20.00	312500	0	0
25.00	390625	0	0
30.00	468750	0	0
33.00	515625	0	0
40.00	625000	0	0
50.00	781250	0	0
60.00	937500	0	0
120.00	1875000	0	0

Table 27.17 BRR settings for different bit rates in simple IIC mode

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	8			10			16			20			25		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	30	0.8	1	12	-3.8	1	15	-2.3	1	19	-2.3
25 k	0	9	0.0	0	12	-3.8	1	4	0.0	1	5	4.2	1	7	-2.3
50 k	0	4	0.0	0	5	4.2	1	2	-16.7	1	2	4.2	1	3	-2.3
100 k*1	0	2	-16.7	0	3	-21.9	0	4	0.0	0	6	-10.7	1	1	-2.3
250 k	0	0	0.0	0	0	25	0	1	0.0	0	2	-16.7	0	2	4.2
350 k										0	1	-10.7	0	1	11.6*2
400 k*1										0	1	-21.9	0	1	-2.3*2

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	30			33			40			50			60		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	1	22	1.9	1	25	-0.8	0	124	0.0	2	9	-2.3	1	46	-0.3
25 k	1	8	4.2	1	9	3.1	0	49	0.0	2	3	-2.3	0	74	0.0
50 k	1	4	-6.3	1	4	3.1	0	24	0.0	2	1	-2.3	0	37	-1.3
100 k*1	1	2	-21.9	1	2	-14.1	0	12	-3.9	1	3	-2.3	0	18	-1.3
250 k	0	3	-6.3	0	3	3.1	0	4	0.0	0	5	4.2	0	7	-6.3
350 k	0	2	-10.7	0	2	-1.8	0	3	-10.7	0	4	-10.7	0	4	7.1
400 k*1	0	1	17.2	0	2	-14.1	0	3	-21.9	0	3	-2.3*2	0	4	-6.3

Bit rate (bps)	Operating frequency PCLKA (MHz)		
	120		
	n	N	Error (%)
10 k	1	93	-0.3
25 k	0	149	0.0
50 k	0	74	0.0
100 k*1	0	37	-1.3
250 k	0	14	0.0
350 k	0	10	-2.6
400 k*1	0	9	-6.3

Note 1. The bit rate of 100 kbps and 400 kbps indicates the set value at which the error is on the negative side.
Note 2. The minimum value of low width is smaller than 1.3 µs which is the standard value in the fast mode.

Table 27.18 Minimum widths at SCL high and low levels at multiple bit rates in simple IIC mode

Bit rate (bps)	Operating frequency PCLKA (MHz)											
	8			10			16			20		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
10 k	0	24	43.75/50.00	0	30	43.40/49.60	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	5	16.80/19.20
50 k	0	4	8.75/10.00	0	5	8.40/9.60	1	2	10.50/12.00	1	2	8.40/9.60
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.38/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	0	1.40/1.60	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60
400 k										0	1	1.40/1.60

Bit rate (bps)	Operating frequency PCLKA (MHz)											
	25			30			33			40		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
10 k	1	19	44.80/51.20	1	22	42.93/49.60	1	25	44.12/50.42	0	124	43.75/50.00
25 k	1	7	17.92/20.48	1	8	16.80/19.20	1	9	16.97/19.39	0	49	17.50/20.00
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	4	8.48/9.70	0	24	8.75/10.00
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.82	0	12	4.55/5.20
250 k	0	2	1.68/1.92	0	3	1.86/2.13	0	3	1.70/1.94	0	4	1.75/2.00
350 k	0	1	1.12/1.28*1	0	2	1.40/1.60	0	2	1.27/1.45	0	3	1.40/1.60
400 k	0	1	1.12/1.28*1	0	2	1.40/1.60	0	2	1.27 /1.45	0	3	1.40/1.60

Bit rate (bps)	Operating frequency PCLKA (MHz)								
	50			60			120		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
10 k	2	9	44.80/51.20	1	46	43.87/50.13	1	93	43.87/50.13
25 k	2	3	17.92/20.48	0	74	17.50/20.00	0	149	17.50/20.00
50 k	2	1	8.96/10.24	0	37	8.87/10.13	0	74	8.75/10.00
100 k	1	3	4.48/5.12	0	18	4.43/5.07	0	37	4.43/5.07
250 k	0	5	1.68/1.92	0	7	1.87/2.13	0	14	1.75/2.00

Bit rate (bps)	Operating frequency PCLKA (MHz)								
	50			60			120		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
350 k	0	4	1.40/1.60	0	4	1.17/1.33	0	10	1.28/1.47
400 k	0	3	1.12/1.28	0	4	1.17/1.33	0	8	1.05/1.20

Note 1. The minimum value of low width is smaller than 1.3 µs which is the standard value of the fast mode. The setting values are the same as in Table 27.17.

27.2.18 Modulation Duty Register (MDDR)

Address(es): SCI0.MDDR 4007 0012h, SCI1.MDDR 4007 0032h, SCI2.MDDR 4007 0052h, SCI3.MDDR 4007 0072h, SCI4.MDDR 4007 0092h, SCI8.MDDR 4007 0112h, SCI9.MDDR 4007 0132h

The MDDR register corrects the bit rate adjusted by the BRR register.

When the SEMR.BRME bit is set to 1, the bit rate generated by the on-chip baud rate generator is evenly corrected using the settings in the MDDR register (M/256). Table 27.19 shows the relationship between the MDDR setting (M) and the bit rate (B).

The initial value of the MDDR register is FFh. Bit [7] in this register is fixed to 1. The CPU can read the MDDR register, but the MDDR register is only writable when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 27.19 Relationship between MDDR setting (M) and bit rate (B) when bit rate modulation function is used

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCSE bit		
Asynchronous, multi-processor transfer	0	0	0	$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	Error (%) $= \{ \frac{PCLKA \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1 \} \times 100$
	1	0	0	$N = \frac{PCLKA \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	Error (%) $= \{ \frac{PCLKA \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1 \} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLKA \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	Error (%) $= \{ \frac{PCLKA \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1 \} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLKA \times 10^6}{12 \times 2^{2n-1} \times (256/M) \times B} - 1$	Error (%) $= \{ \frac{PCLKA \times 10^6}{B \times 12 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1 \} \times 100$
Clock synchronous, simple SPI*1				$N = \frac{PCLKA \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	-
Smart card interface				$N = \frac{PCLKA \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	Error (%) $= \{ \frac{PCLKA \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N+1)} - 1 \} \times 100$
Simple IIC*2				$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	-

B: Bit rate (bps)
M: MDDR setting (128 ≤ MDDR ≤ 255)

N: BRR setting for baud rate generator (0 ≤ N ≤ 255)
PCLKA: Operating frequency (MHz)
n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 27.7 and Table 27.8. See section 27.2.17, Bit Rate Register (BRR) for details.

Note 1. Do not use this function in clock synchronous mode or in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).
Note 2. Adjust the bit rate so that the high and low-level widths of the SCL output in simple IIC mode satisfy the I^2C standard.

Table 27.20 and Table 27.21 list examples of N settings in BRR and M settings in MDDR in asynchronous mode.

Table 27.20 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (1)

	Operating frequency PCLKA (MHz)														
	8					9.8304					16				
Bit rate (bps)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	-0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

	Operating frequency PCLKA (MHz)														
	12					12.288					14				
Bit rate (bps)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	-0.17	0	2	202	1	-0.11
460800	0	0	157	1	-0.18	0	0	154	1	-0.26	0	0	135	1	0.14

	Operating frequency PCLKA (MHz)														
	16					17.2032					18				
Bit rate (bps)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	-0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	-0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	-0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	-0.20	0	0	210	0	0.14

Note 1. In this example, the ABCS and ABCSE bits in the SEMR register are 0. SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

Table 27.21 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2) (1 of 2)

	Operating frequency PCLKA (MHz)														
	19.6608					20					25				
Bit rate (bps)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	15	(256)*2	0	0.00	0	10	173	0	-0.01	0	11	151	0	0.00
57600	0	9	240	0	0.00	0	9	236	0	0.03	0	7	151	0	0.00
115200	0	4	240	0	0.00	0	4	236	0	0.03	0	3	151	0	0.00
230400	0	1	192	0	0.00	0	4	236	1	0.03	0	1	151	0	0.00

Table 27.21 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2) (2 of 2)

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	19.6608					20					25				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
460800	0	0	192	0	0.00	0	0	189	0	0.14	0	0	151	0	0.00

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	30					33					40				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	-0.01
57600	0	10	173	0	-0.01	0	9	143	0	0.01	0	38	230	1	-0.01
115200	0	10	173	1	-0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	-0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.10	0	4	236	1	0.03

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	50					60					120				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	23	151	0	0.00	0	36	194	0	0.01	0	73	194	0	0.01
57600	0	15	151	0	0.00	0	21	173	0	-0.01	0	58	232	0	0.00
115200	0	7	151	0	0.00	0	10	173	0	-0.01	0	21	173	0	-0.01
230400	0	3	151	0	0.00	0	10	173	1	-0.01	0	10	173	0	-0.01
460800	0	1	151	0	0.00	0	6	220	1	-0.09	0	10	173	1	-0.09

Note 2. In this example, the ABCS and ABCSE bits in the SEMR register are 0.
SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

27.2.19 Serial Extended Mode Register (SEMR)

Address(es): SCI0.SEMR 4007 0007h, SCI1.SEMR 4007 0027h, SCI2.SEMR 4007 0047h, SCI3.SEMR 4007 0067h, SCI4.SEMR 4007 0087h, SCI8.SEMR 4007 0107h, SCI9.SEMR 4007 0127h

	b7	b6	b5	b4	b3	b2	b1	b0
	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	BRME	Bit Rate Modulation Enable	0: Bit rate modulation function is disabled 1: Bit rate modulation function is enabled.	R/W*1
b3	ABCSE	Asynchronous Mode Extended Base Clock Select 1	Valid only in asynchronous mode with SCR.CKE[1] = 0: 0: Clock cycle for 1-bit period is determined with combination of BGDM and ABCS bits in the SEMR register 1: Baud rate is 6 base clock cycles for 1-bit period.	R/W*1
b4	ABCS	Asynchronous Mode Base Clock Select	Valid only in asynchronous mode: 0: Selects 16 base clock cycles for 1-bit period 1: Selects 8 base clock cycles for 1-bit period.	R/W*1

Bit	Symbol	Bit name	Description	R/W
b5	NFEN	Digital Noise Filter Function Enable	In asynchronous mode: 0: Noise cancellation function for the RXDn input signal is disabled 1: Noise cancellation function for the RXDn input signal is enabled. In simple IIC mode: 0: Noise cancellation function for the SCLn and SDAn input signals is disabled 1: Noise cancellation function for the SCLn and SDAn input signals is enabled. The NFEN bit must be 0 in all other modes.	R/W*1
b6	BGDM	Baud Rate Generator Double-Speed Mode Select	Valid only in asynchronous mode with SCR.CKE[1] = 0: 0: Baud rate generator outputs the clock with single frequency 1: Baud rate generator outputs the clock with double frequency.	R/W*1
b7	RXDESEL	Asynchronous Start Bit Edge Detection Select	Valid only in asynchronous mode: 0: The low level on the RXDn pin is detected as the start bit 1: A falling edge on the RXDn pin is detected as the start bit.	R/W*1

Note 1. Writable only when the TE and RE bits in SCR/SCR_SMCI are 0 (both serial transmission and reception are disabled).

The SEMR register selects the clock source for a 1-bit period in asynchronous mode.

BRME bit (Bit Rate Modulation Enable)

The BRME bit enables or disables the bit rate modulation function. The bit rate generated by the on-chip baud rate generator is evenly corrected when this function is enabled.

ABCSE bit (Asynchronous Mode Extended Base Clock Select 1)

The ABCSE bit sets the pulse number for the base clock in a 1-bit period to 6, and the double-frequency clock is output from the baud rate generator. When the bit rate is set to 6 while dividing the bus clock frequency, use the ABCSE bit to set SMR.CKS[1:0] to 00b and BRR to 0. Set this bit to 0 except in asynchronous mode.

ABCS bit (Asynchronous Mode Base Clock Select)

The ABCS bit selects the clock cycles for a 1-bit period. Set this bit to 0 except in asynchronous mode.

NFEN bit (Digital Noise Filter Function Enable)

The NFEN bit enables or disables the digital noise filter function.

When the digital noise filter function is enabled:

- Noise cancellation is applied to the RXDn input signal in asynchronous mode
- Noise cancellation is applied to the SDAn and SCLn input signals in simple IIC mode.

In all other modes, set the NFEN bit to 0 to disable the digital noise filter function. When the function is disabled, input signals are transferred as received.

BGDM bit (Baud Rate Generator Double-Speed Mode Select)

The BGDM bit selects the cycle of output clock for the baud rate generator to be either single or double frequency.

This bit is valid when the on-chip baud rate generator is selected as the clock source (SCR.CKE[1] = 0) in asynchronous mode (SMR.CM = 0). The base clock is generated by the clock output from the baud rate generator. When the BGDM bit is set to 1, the base clock cycle is halved and the bit rate is doubled.

Set this bit to 0 in modes other than asynchronous mode.

RXDESEL bit (Asynchronous Start Bit Edge Detection Select)

The RXDSEL bit selects the detection method of the start bit for reception in asynchronous mode. When a break occurs, set this bit to 1 to stop reception, or to start reception without retaining the RXDn pin input at a high level for the period of one data frame or longer after completion of the break.

Set this bit to 0 in modes other than asynchronous mode.

27.2.20 Noise Filter Setting Register (SNFR)

Address(es): SCI0.SNFR 4007 0008h, SCI1.SNFR 4007 0028h, SCI2.SNFR 4007 0048h, SCI3.SNFR 4007 0068h, SCI4.SNFR 4007 0088h, SCI8.SNFR 4007 0108h, SCI9.SNFR 4007 0128h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	NFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	NFCS[2:0]	Noise Filter Clock Select	In asynchronous mode, the standard setting for the base clock is as follows: b2 b0 0 0 0: The clock signal divided by 1 is used with the noise filter. In simple IIC mode, the standard settings for the clock source of the on-chip baud rate generator selected in the SMR.CKS[1:0] bits are as follows: b2 b0 0 0 1: The clock signal divided by 1 is used with noise filter 0 1 0: The clock signal divided by 2 is used with noise filter 0 1 1: The clock signal divided by 4 is used with noise filter 1 0 0: The clock signal divided by 8 is used with noise filter. Other settings are prohibited.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in SCR/SCR_SMCI are 0 (serial reception and transmission disabled).

The SNFR register sets the digital noise filter clock.

NFCS[2:0] bits (Noise Filter Clock Select)

The NFCS[2:0] bits select the sampling clock for the digital noise filter. To use the noise filter in asynchronous mode, set these bits to 000b. In simple IIC mode, set the bits to a value in the range from 001b to 100b.

27.2.21 I2C Mode Register 1 (SIMR1)

Address(es): SCI0.SIMR1 4007 0009h, SCI1.SIMR1 4007 0029h, SCI2.SIMR1 4007 0049h, SCI3.SIMR1 4007 0069h, SCI4.SIMR1 4007 0089h, SCI8.SIMR1 4007 0109h, SCI9.SIMR1 4007 0129h

	b7	b6	b5	b4	b3	b2	b1	b0
	IICDL[4:0]					—	—	IICM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICM	Simple IIC Mode Select	SMIF IICM 0 0: Asynchronous mode, multi-processor mode, clock synchronous mode, or simple SPI mode 0 1: Simple IIC mode 1 0: Smart card interface mode 1 1: Setting prohibited.	R/W*1
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b3	IICDL[4:0]	SDA Delay Output Select	The following cycles are of the clock signal from the on-chip baud rate generator: b7 b3 0 0 0 0 0: No output delay 0 0 0 0 1: 0 to 1 cycle 0 0 0 1 0: 1 to 2 cycles 0 0 0 1 1: 2 to 3 cycles 0 0 1 0 0: 3 to 4 cycles 0 0 1 0 1: 4 to 5 cycles : 1 1 1 1 0: 29 to 30 cycles 1 1 1 1 1: 30 to 31 cycles.	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (both serial transmission and reception are disabled).

SIMR1 selects simple IIC mode and the number of delay stages for the SDAn output.

IICM bit (Simple IIC Mode Select)

In combination with the SMIF bit in SCMR, the IICM bit selects the operating mode.

IICDL[4:0] bits (SDA Delay Output Select)

The IICDL[4:0] bits specify an output delay on the SDAn pin relative to the falling edge of the output on the SCLn pin.

The available delay settings range from no delay to 31 cycles, with the clock signal from the on-chip baud rate generator as the base. The signal obtained by frequency-dividing PCLKA by the divisor set in SMR.CKS[1:0] is supplied as the clock signal from the on-chip baud rate generator. Set these bits to 00000b unless the operation is in simple IIC mode. In simple IIC mode, set the bits to a value in the range from 00001b to 11111b.

27.2.22 I²C Mode Register 2 (SIMR2)

Address(es): SCI0.SIMR2 4007 000Ah, SCI1.SIMR2 4007 002Ah, SCI2.SIMR2 4007 004Ah, SCI3.SIMR2 4007 006Ah, SCI4.SIMR2 4007 008Ah, SCI8.SIMR2 4007 010Ah, SCI9.SIMR2 4007 012Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IICACKT	—	—	—	IICCSC	IICINTM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICINTM	IIC Interrupt Mode Select	0: Use ACK/NACK interrupts 1: Use reception and transmission interrupts.	R/W*1
b1	IICCSC	Clock Synchronization	0: No synchronization with the clock signal 1: Synchronization with the clock signal.	R/W*1
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	IICACKT	ACK Transmission Data	0: ACK transmission 1: NACK transmission and ACK/NACK reception.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (serial reception and transmission disabled).

SIMR2 selects how reception and transmission are controlled in simple IIC mode.

IICINTM bit (IIC Interrupt Mode Select)

The IICINTM bit selects the sources of interrupt requests in simple IIC mode.

IICCSC bit (Clock Synchronization)

Set the IICCSC bit to 1 to synchronize the internally generated SCLn clock signal when the SCLn pin is driven low

because of a wait inserted by another device, for example.

The SCL clock signal is not synchronized if the IICCSC bit is 0. The SCLn clock signal is generated according to the rate selected in the BRR register regardless of the level being input on the SCLn pin.

Set this bit to 1 except during debugging.

IICACKT bit (ACK Transmission Data)

The IICACKT bit transmits data that contains ACK bits. Set this bit to 1 when ACK and NACK bits are received.

27.2.23 I2C Mode Register 3 (SIMR3)

Address(es): SCI0.SIMR3 4007 000Bh, SCI1.SIMR3 4007 002Bh, SCI2.SIMR3 4007 004Bh, SCI3.SIMR3 4007 006Bh, SCI4.SIMR3 4007 008Bh, SCI8.SIMR3 4007 010Bh, SCI9.SIMR3 4007 012Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTP REQ	IICRST AREQ	IICSTA REQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICSTAREQ	Start Condition Generation	0: Do not generate start condition 1: Generate start condition.*1, *3, *5, *6	R/W
b1	IICRSTAREQ	Restart Condition Generation	0: Do not generate restart condition 1: Generate restart condition.*2, *3, *5, *6	R/W
b2	IICSTPREQ	Stop Condition Generation	0: Do not generate stop condition 1: Generate stop condition.*2, *3, *5, *6	R/W
b3	IICSTIF	Issuing of Start, Restart, or Stop Condition Completed Flag	0: No requests are being made for generating conditions, or a condition is being generated 1: Generation of start, restart, or stop condition is complete. When 0 is written to IICSTIF, it is set to 0.*4	R/W*4
b5, b4	IICSDAS[1:0]	SDA Output Select	b5 b4 0 0: Output serial data 0 1: Generate start, restart, or stop condition 1 0: Output low on SDAn pin 1 1: Drive SDAn pin to high-impedance state.	R/W
b7, b6	IICSCLS[1:0]	SCL Output Select	b7 b6 0 0: Output serial clock 0 1: Generate start, restart, or stop condition 1 0: Output low on SCLn pin 1 1: Drive SCLn pin to high-impedance state.	R/W

Note 1. Only generate a start condition after checking the bus state and confirming that the bus is free.
Note 2. Generate a restart or stop condition after checking the bus state and confirming that the bus is busy.
Note 3. Do not set more than one of the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits to 1 at a given time.
Note 4. Write only 0. When 1 is written, the value is ignored.
Note 5. Execute the generation of a condition after the value of the IICSTIF flag is 0.
Note 6. Do not write 0 to this bit while it is 1. Generation of a condition is suspended by writing 0 to this bit while it is 1.

IICSTAREQ bit (Start Condition Generation)

When a start condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit.

[Clearing condition]

- When generation of a start condition is complete.

IICRSTAREQ bit (Restart Condition Generation)

When a restart condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b in addition to setting the IICRSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit.

[Clearing condition]

- When generation of a restart condition is complete.

IICSTPREQ bit (Stop Condition Generation)

When a stop condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b in addition to setting the IICSTPREQ bit to 1.

[Setting condition]

- Writing 1 to the bit.

[Clearing condition]

- When generation of a stop condition is complete.

IICSTIF flag (Issuing of Start, Restart, or Stop Condition Completed Flag)

After generating a condition, the IICSTIF flag indicates that the condition generation is complete. When using the IICSTAREQ, IICRSTAREQ, or IICSTPREQ bit to cause generation of a condition, do so after setting the IICSTIF flag to 0.

When the IICSTIF flag is 1 while an interrupt request is enabled by setting the SCR.TEIE bit, an STI request is output.

[Setting condition]

- When generation of a start, restart, or stop condition completes. If the setting condition conflicts with any of the clearing conditions for the flag, the clearing condition takes precedence.

[Clearing conditions]

- Writing 0 to the bit, then confirm that the IICSTIF flag is 0.
- Writing 0 to the SIMR1.IICM bit when operation is not in simple IIC mode
- Writing 0 to the SCR.TE bit.

IICSDAS[1:0] bits (SDA Output Select)

The IICSDAS[1:0] bits control output from the SDAn pin. Set the IICSDAS[1:0] and IICSCLS[1:0] bits to the same value.

IICSCLS[1:0] bits (SCL Output Select)

The IICSCLS[1:0] bits control output from the SCLn pin. Set the IICSCLS[1:0] and IICSDAS[1:0] bits to the same value.

27.2.24 I2C Status Register (SISR)

Address(es): SCI0.SISR 4007 000Ch, SCI1.SISR 4007 002Ch, SCI2.SISR 4007 004Ch, SCI3.SISR 4007 006Ch, SCI4.SISR 4007 008Ch, SCI8.SISR 4007 010Ch, SCI9.SISR 4007 012Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IICACKR
Value after reset:	0	0	x	x	0	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	IICACKR	ACK Reception Data Flag	0: ACK received 1: NACK received.	R
b1	—	Reserved	This bit is read as 0	R
b2	—	Reserved	The read value is undefined	R
b3	—	Reserved	This bit is read as 0	R
b5, b4	—	Reserved	The read value is undefined	R
b7, b6	—	Reserved	These bits are read as 0	R

SISR monitors the state in simple IIC mode.

IICACKR flag (ACK Reception Data Flag)

Received ACK and NACK bits can be read from the IICACKR flag. This flag is updated on the rising edge of the SCLn clock for the received ACK/NACK bit.

27.2.25 SPI Mode Register (SPMR)

Address(es): SCI0.SPMR 4007 000Dh, SCI1.SPMR 4007 002Dh, SCI2.SPMR 4007 004Dh, SCI3.SCI3 4007 006Dh, SCI4.SPMR 4007 008Dh, SCI8.SPMR 4007 010Dh, SCI9.SPMR 4007 012Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKPH	CKPOL	—	MFF	—	MSS	CTSE	SSE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSE	SSn Pin Function Enable	0: SSn pin function is disabled 1: SSn pin function is enabled.	R/W*1
b1	CTSE	CTS Enable	0: CTS function is disabled (RTS output function is enabled) 1: CTS function is enabled.	R/W*1
b2	MSS	Master Slave Select	0: Transmission is through the TXDn pin and reception is through the RXDn pin (master mode) 1: Reception is through the TXDn pin and transmission is through the RXDn pin (slave mode).	R/W*1
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	MFF	Mode Fault Flag	0: No mode fault error 1: Mode fault error.	R/W*2
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	CKPOL	Clock Polarity Select	0: Clock polarity is not inverted 1: Clock polarity is inverted.	R/W*1
b7	CKPH	Clock Phase Select	0: Clock is not delayed 1: Clock is delayed.	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (both serial transmission and reception

are disabled).
Note 2. Only 0 can be written to this bit to clear the flag.

The SPMR register selects settings for simple SPI mode.

SSE bit (SSn Pin Function Enable)

Set the SSE bit to 1 to use the SSn pin to control transmission and reception in simple SPI mode. Set this bit to 0 in all other modes. When master mode is selected (SCR.CKE[1:0] = 00b and SPMR.MSS = 0) and there is a single master, the SSn pin on the master side is not required to control reception and transmission. In such a case, set the SSE bit to 0. Do not set both the SSE and CTSE bits to 1 as the operation is the same as that when these bits are set to 0.

CTSE bit (CTS Enable)

Set the CTSE bit to 1 to use the SSn pin to input the CTS control signal for controlling transmission and reception. The RTS signal is output when this bit is set to 0. Set this bit to 0 in smart card interface mode, simple SPI mode, and simple IIC mode. Do not set both the CTSE and SSE bits to 1 as the operation is the same as that when these bits are set to 0.

MSS bit (Master Slave Select)

The MSS bit selects between master or slave operation in simple SPI mode. The functions of the TXDn and RXDn pins are reversed when this bit is set to 1, so that data is received through the TXDn pin and transmitted through the RXDn pin. Set this bit to 0 in modes other than simple SPI mode.

MFF flag (Mode Fault Flag)

The MFF flag indicates mode fault errors. In a multi-master configuration, determine the mode fault error occurrence by reading this flag.

[Setting condition]

- When input on the SSn pin is low during master operation in simple SPI mode (SSE bit = 1 and MSS bit = 0).

[Clearing condition]

- Writing 0 to the bit after 1 is read.

CKPOL bit (Clock Polarity Select)

The CKPOL bit selects the polarity of the clock signal output through the SCKn pin. See Figure 27.70 for details. Set the CKPOL bit to 0 in modes other than simple SPI mode and clock synchronous mode.

CKPH bit (Clock Phase Select)

The CKPH bit selects the phase of the clock signal output through the SCKn pin. See Figure 27.70 for details. Set the CKPH bit to 0 in modes other than simple SPI mode and clock synchronous mode.

27.2.26 FIFO Control Register (FCR)

Address(es): SCI0.FCR 4007 0014h, SCI1.FCR 4007 0034h, SCI2.FCR 4007 0054h, SCI3.FCR 4007 0074h, SCI4.FCR 4007 0094h, SCI8.FCR 4007 0114h, SCI9.FCR 4007 0134h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
Value after reset:	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FM	FIFO Mode Select	Valid only in asynchronous mode, including multi-processor or clock synchronous mode: 0: Non-FIFO mode. Selects TDR/RDR or TDRHL/RDRHL for communication. 1: FIFO mode. Selects FTDRHL/FRDRHL for communication.	R/W*1

Bit	Symbol	Bit name	Description	R/W
b1	RFRST	Receive FIFO Data Register Reset	Valid only when FCR.FM = 1: 0: Do not reset FRDRHL 1: Reset FRDRHL.	R/W
b2	TFRST	Transmit FIFO Data Register Reset	Valid only when FCR.FM = 1: 0: Do not reset FTDRHL 1: Reset FTDRHL.	R/W
b3	DRES	Receive Data Ready Error Select Bit	Selects the interrupt request when detecting a receive data ready: 0: Receive data full interrupt (SCIn_RXI) 1: Receive error interrupt (SCIn_ERI).	R/W
b7 to b4	TTRG[3:0]	Transmit FIFO Data Trigger Number	Valid only in asynchronous mode, including multi-processor or clock synchronous mode: 0000: Trigger number 0 : 1111: Trigger number 15.	R/W
b11 to b8	RTRG[3:0]	Receive FIFO Data Trigger Number	Valid only in asynchronous mode, including multi-processor or clock synchronous mode: 0000: Trigger number 0 : 1111: Trigger number 15.	R/W
b15 to b12	RSTRG[3:0]	RTS Output Active Trigger Number Select	Valid only in asynchronous mode, including multi-processor or clock synchronous mode, while FCR.FM = 1, SPMR.CTSE = 0, and SPMR.SSE = 0: 0000: Trigger number 0 : 1111: Trigger number 15.	R/W

Note 1. Writable only when TE = 0 and RE = 0.

FCR selects the FIFO mode, resets FTDRHL/FRDRHL, selects the FIFO data trigger number for transmission/reception, and selects the RTS output active trigger number.

FM bit (FIFO Mode Select)

When the FM bit is set to 1, FTDRHL and FRDRHL are selected for communication. When the FM bit is set to 0, TDR and RDR, or TDRHL and RDRHL are selected for communication.

RFRST bit (Receive FIFO Data Register Reset)

When the RFRST bit is set to 1, the FRDRHL register is reset, and the receive data count is reset to 0. When 1 is written to the RFRST bit, it is set to 0 after 1 PCLKA.

TFRST bit (Transmit FIFO Data Register Reset)

When the TFRST bit is set to 1, the FTDRHL register is reset, and the transmit data count is reset to 0. When 1 is written to the TFRST bit, it is set to 0 after 1 PCLKA.

DRES bit (Receive Data Ready Error Select Bit)

On detecting a receive data ready error, the DRES bit selects between an SCIn_RXI interrupt request or an SCIn_ERI interrupt request. Set the DRES bit to 1 when starting the DMAC or DTC and reading from the FRDRH and FRDRL registers.

TTRG[3:0] bits (Transmit FIFO Data Trigger Number)

The TDFE flag is set to 1 when the amount of transmit data in FTDRHL is equal to or less than the transmit triggering number specified in the TTRG[3:0] bits, and software can write data to FTDRHL. If SCR.TIE = 1, an SCIn_TXI interrupt request occurs.

RTRG[3:0] bits (Receive FIFO Data Trigger Number)

The RDF flag is set to 1 when the amount of receive data in FRDRHL is equal to or greater than the specified receive triggering number specified in the RTRG[3:0] bits, and software can read data from FRDRHL. If SCR.RIE = 1, an SCIn_RXI interrupt request occurs.

When RTRG[3:0] is set to 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0, and an SCIn_RXI interrupt does not occur.

RSTRG[3:0] bits (RTS Output Active Trigger Number Select)

When the amount of receive data stored in FRDRHL is equal to or greater than the receive triggering number specified in the RSTRG[3:0] bits, the RTS signal goes high.

When RSTRG[3:0] is 0, the RTS signal does not go high even when the amount of data in FRDRHL is equal to 0.

27.2.27 FIFO Data Count Register (FDR)

Address(es): SCI0.FDR 4007 0016h, SCI1.FDR 4007 0036h, SCI2.FDR 4007 0056h, SCI3.FDR 4007 0076h, SCI4.FDR 4007 0096h, SCI8.FDR 4007 0116h, SCI9.FDR 4007 0136h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	T[4:0]					—	—	—	R[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	R[4:0]	Receive FIFO Data Count	Indicates the amount of receive data stored in FRDRHL (valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1)	R
b7 to b5	—	Reserved	These bits are read as 0.	R
b12 to b8	T[4:0]	Transmit FIFO Data Count	Indicates the amount of non-transmitted data stored in FTDRHL (valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1)	R
b15 to b13	—	Reserved	These bits are read as 0	R

The FDR register indicates the amount of data stored in FRDRHL/FTDRHL.

R[4:0] bits (Receive FIFO Data Count)

The R[4:0] bits indicate the amount of receive data stored in FRDRHL. A value of 00h indicates no receive data, and 10h means that the maximum received data is stored in FRDRHL.

T[4:0] bits (Transmit FIFO Data Count)

The T[4:0] bits indicate the amount of non-transmitted data stored in FTDRHL. A value of 00h indicates no transmit data, and 10h indicates that all (maximum amount) of the data to be transmitted is stored in FTDRHL.

27.2.28 Line Status Register (LSR)

Address(es): SCI0.LSR 4007 0018h, SCI1.LSR 4007 0038h, SCI2.LSR 4007 0058h, SCI3.LSR 4007 0078h, SCI4.LSR 4007 0098h, SCI8.LSR 4007 0118h, SCI9.LSR 4007 0138h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ORER	Overrun Error Flag	Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, with FIFO operation selected: 0: No overrun error occurred 1: Overrun error occurred.	R*1
b1	—	Reserved	This bit is read as 0	R
b6 to b2	FNUM[4:0]	Framing Error Count	Indicates the amount of data with a framing error in the receive data stored in the Receive FIFO Data Register (FRDRHL)	R
b7	—	Reserved	This bit is read as 0	R

Bit	Symbol	Bit name	Description	R/W
b12 to b8	PNUM[4:0]	Parity Error Count	Indicates the amount of data with a parity error in the receive data stored in the Receive FIFO Data Register (FRDRHL)	R
b15 to b13	—	Reserved	These bits are read as 0	R

Note 1. If this flag is 1, write 0 to SSR_FIFO.ORER to clear the flag.

The LSR register indicates the status of receive error.

ORER flag (Overrun Error Flag)

The ORER flag reflects the value in SSR_FIFO.ORER.

FNUM[4:0] bits (Framing Error Count)

The FNUM[4:0] bit value indicates the amount of data with a framing error stored in the FRDRHL register.

PNUM[4:0] bits (Parity Error Count)

The PNUM[4:0] bit value indicates the amount of data with a parity error stored in the FRDRHL register.

27.2.29 Compare Match Data Register (CDR)

Address(es): SCI0.CDR 4007 001Ah, SCI1.CDR 4007 003Ah, SCI2.CDR 4007 005Ah, SCI3.CDR 4007 007Ah, SCI4.CDR 4007 009Ah, SCI8.CDR 4007 011Ah, SCI9.CDR 4007 013Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPD[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	CMPD[8:0]	Compare Match Data	Holds compare data pattern for address match wakeup function	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The CDR register sets the compare data for the address match function.

CMPD[8:0] bits (Compare Match Data)

The CMPD[8:0] bits set the data to be compared to receive data for the address match function when the address match function is enabled (DCCR.DCME = 1).

Three bit lengths are available:

- CMPD[6:0] with 7-bit length
- CMPD[7:0] with 8-bit length
- CMPD[8:0] with 9-bit length.

27.2.30 Data Compare Match Control Register (DCCR)

Address(es): SCI0.DCCR 4007 0013h, SCI1.DCCR 4007 0033h, SCI2.DCCR 4007 0053h, SCI3.DCCR 4007 0073h, SCI4.DCCR 4007 0093h, SCI8.DCCR 4007 0113h, SCI9.DCCR 4007 0133h

	b7	b6	b5	b4	b3	b2	b1	b0
	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DCMF	Data Compare Match Flag	0: Not matched 1: Matched.	R/(W)*1
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R
b3	DPER	Data Compare Match Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*1
b4	DFER	Data Compare Match Framing Error Flag	0: No framing error occurred 1: Framing error occurred.	R/(W)*1
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	IDSEL	ID Frame Select	Valid only in asynchronous mode, including multi-processor mode: 0: Always compare data regardless of the MPB bit value 1: Only compare data when MPB bit is 1 (ID frame).	R/W
b7	DCME	Data Compare Match Enable	Valid only in asynchronous mode, including multi-processor mode: 0: Address match function disabled 1: Address match function enabled.	R/W

Note 1. Only 0 can be written to clear the flag after reading 1.

The DCCR register sets control of the address match function.

DCMF flag (Data Compare Match Flag)

The DCMF flag indicates that the SCI detects a match of the comparison data (CDR.CMPD) with receive data.

[Setting condition]

- When comparison data (CDR.CMPD) matches the receive data, when DCCR.DCME = 1.

[Clearing condition]

- When 0 is written after 1 is read from DCMF.

Clearing the SCR.RE bit to 0 does not affect the DCMF flag, which keeps its previous value.

DPER flag (Data Compare Match Parity Error Flag)

The DPER flag indicates that a parity error occurred at address match detection (receive data match detection).

[Setting condition]

- When a parity error is detected in the frame in which an address match is detected.

[Clearing conditions]

- When 0 is written after 1 is read from DPER.

Clearing the SCR.RE bit to 0 (serial reception is disabled) does not affect the DPER flag, which keeps its previous value.

DFER flag (Data Compare Match Framing Error Flag)

The DFER flag indicates that a framing error occurred at address match detection (receive data match detection).

[Setting conditions]

- When a stop bit is 0 in the frame in which an address match is detected.

- When in 2-stop-bit mode, only the first stop bit is checked for a value of 1, while the second stop bit is not checked.

[Clearing condition]

- When 0 is written after 1 is read from DFER.

When the SCR.RE bit is set to 0 (serial reception is disabled), the DFER flag is not affected and keeps its previous value.

IDSEL bit (ID Frame Select)

The IDSEL bit selects whether to compare data regardless of the MPB bit value or to compare data only when MPB = 1 (ID frame), when the address match function is enabled.

DCME bit (Data Compare Match Enable)

The DCME bit enables or disables the address match function (data compare match function).

If the SCI detects a match between comparison data (CDR.CMPD) and receive data, the DCME bit is cleared automatically and the SCI operates in receive mode without the data compare match function. See section 27.3.6, Address Match (Receive Data Match Detection) Function.

The write value should be 0 for any mode other than asynchronous mode.

27.2.31 Serial Port Register (SPTR)

Address(es): SCI0.SPTR 4007 001Ch, SCI1.SPTR 4007 003Ch, SCI2.SPTR 4007 005Ch, SCI3.SPTR 4007 007Ch, SCI4.SPTR 4007 009Ch, SCI8.SPTR 4007 011Ch, SCI9.SPTR 4007 013Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPB2IO	SPB2DT	RXDMON
Value after reset:	0	0	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b0	RXDMON	Serial Input Data Monitor	Indicates the state of the RXDn pin: 0: RXDn pin is low 1: RXDn pin is high.	R
b1	SPB2DT	Serial Port Break Data Select	Selects the output level of the TXDn pin when SCR.TE = 0: 0: Output low on TXDn pin 1: Output high on TXDn pin.	R/W
b2	SPB2IO	Serial Port Break I/O	Selects whether the value of SPB2DT is output on the TXDn pin: 0: The value of SPB2DT bit is not output on TXDn pin 1: The value of SPB2DT bit is output on TXDn pin.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SPTR register provides confirmation of the serial reception pin (RXDn) status and sets the transmission pin (TXDn) status. This register can only be used in asynchronous mode.

The TXDn pin status is determined by the combination of SCR.TE, SPTR.SPB2IO, and SPTR.SPB2DT bit settings, as shown in Table 27.22.

Table 27.22 TXDn pin status

Value of SCR.TE	Value of SPTR.SPB2IO	Value of SPTR.SPB2DT	TXDn pin status
0	0	x	Hi-Z (initial value)
0	1	0	Low level output
0	1	1	High level output
1	x	x	Serial transmit data is output

x: Don't care.

Note: Use the SPTR register in asynchronous mode only. Using this register in any other mode is not guaranteed.

27.3 Operation in Asynchronous Mode

Figure 27.2 shows the general format for asynchronous serial communications. One frame consists of a start bit (low level), transmit/receive data, a parity bit, and stop bits (high level). In asynchronous serial communications, the communications line is held in the mark state (high level) when not communicating. The SCI monitors the communications line. When the SCI detects a low, it regards that as a start bit and starts serial communication.

Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications. Both the transmitter and receiver have a double-buffered structure in addition to FIFO mode, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

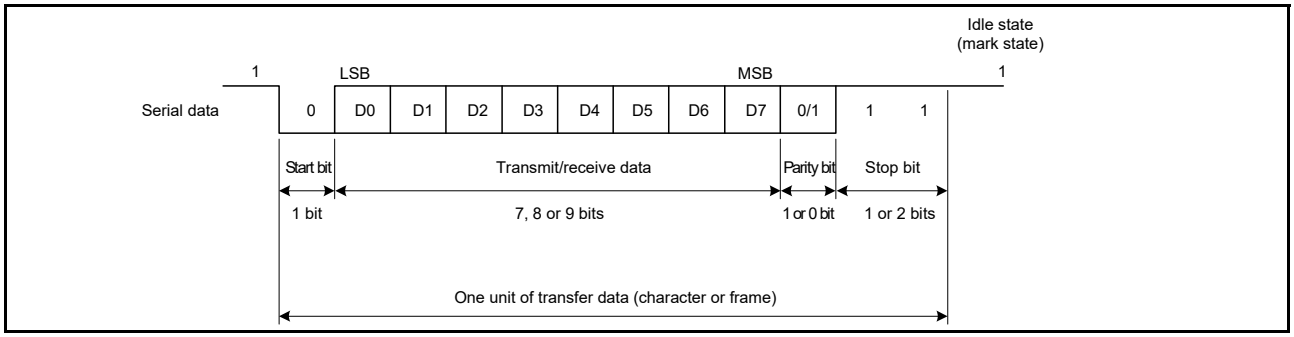


Figure 27.2 Data format in asynchronous serial communications with 8-bit data, parity bit, and 2 stop bits

27.3.1 Serial Data Transfer Format

Table 27.23 lists the serial data transfer formats that can be used in asynchronous mode. Any of the 18 transfer formats can be selected in the SMR and SCMR register settings. For details on the multi-processor function, see section 27.4, Multi-Processor Communication Function.

Table 27.23 Serial transfer formats in asynchronous mode (1 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length												
CHR1	CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12	13
0	0	0	0	0	S	9-bit data									STOP		
0	0	0	0	1	S	9-bit data									STOP	STOP	
0	0	1	0	0	S	9-bit data									P	STOP	
0	0	1	0	1	S	9-bit data									P	STOP	STOP
1	0	0	0	0	S	8-bit data								STOP			
1	0	0	0	1	S	8-bit data								STOP	STOP		

Table 27.23 Serial transfer formats in asynchronous mode (2 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length												
CHR1	CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12	13
1	0	1	0	0	S	8-bit data								P	STOP		
1	0	1	0	1	S	8-bit data								P	STOP	STOP	
1	1	0	0	0	S	7-bit data							STOP				
1	1	0	0	1	S	7-bit data							STOP	STOP			
1	1	1	0	0	S	7-bit data							P	STOP			
1	1	1	0	1	S	7-bit data							P	STOP	STOP		
0	0	-	1	0	S	9-bit data									MPB	STOP	
0	0	-	1	1	S	9-bit data									MPB	STOP	STOP
1	0	-	1	0	S	8-bit data								MPB	STOP		
1	0	-	1	1	S	8-bit data								MPB	STOP	STOP	
1	1	-	1	0	S	7-bit data							MPB	STOP			
1	1	-	1	1	S	7-bit data							MPB	STOP	STOP		

S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multi-processor bit

27.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate.

In reception, the SCI samples the falling edge of the start bit using the base clock, and performs internal synchronization.

Because receive data is sampled on the rising edge of the 8th pulse*1 of the base clock, data is latched at the middle of each bit, as shown in Figure 27.3. The reception margin in asynchronous mode is determined by the following formula (1):

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\ F - \frac{\left| D - 0.5 \right|}{N}\ (1 + F) \right| \times 100\ [\%] \cdots \text{Formula (1)}$$

M: Reception margin
N: Ratio of bit rate to clock
N = 16 when SEMR.ABCSE = 0 and SEMR.ABCS = 0
N = 8 when SEMR.ABCS = 1
N = 6 when SEMR.ABCSE = 1
D: Duty cycle of clock (D = 0.5 to 1.0)
L: Frame length (L = 9 to 13)
F: Absolute value of clock frequency deviation

Assuming values of F = 0 and D = 0.5 in formula (1), the reception margin is determined by the following formula:

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\%$$

This represents the computed value. Renesas recommends that a margin of 20% to 30% should be allowed in system design.

Note 1. In this example, the SEMR.ABCS bit is 0 and the SEMR.ABCSE is 0. When the ABCS bit is 1 and the ABCSE bit is 0, a frequency of 8 times the bit rate is used as a base clock, and receive data is sampled on the rising edge of the 4th pulse of the base clock.
When the ABCSE bit is 1, a frequency of 6 times the bit rate is used as a base clock, and the receive data is sampled on the rising edge of the 3rd pulse of the base clock.

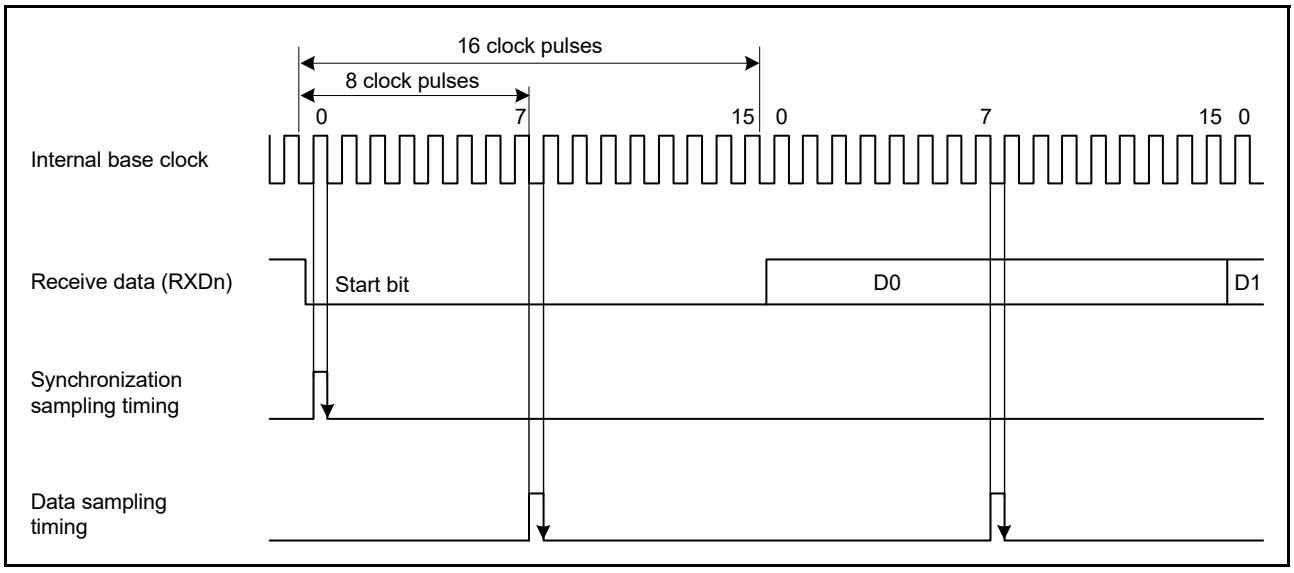


Figure 27.3 Receive data sampling timing in asynchronous mode

27.3.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCKn pin can be selected as the SCI transfer clock, based on the SMR.CM and SCR.CKE[1:0] bit settings.

When an external clock is input to the SCKn pin, the clock frequency must be 16 times the bit rate (when SEMR.ABCS = 0) or 8 times the bit rate (when SEMR.ABCS = 1).

When the SCI uses its internal clock, the clock can be output from the SCKn pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as Figure 27.4 shows.

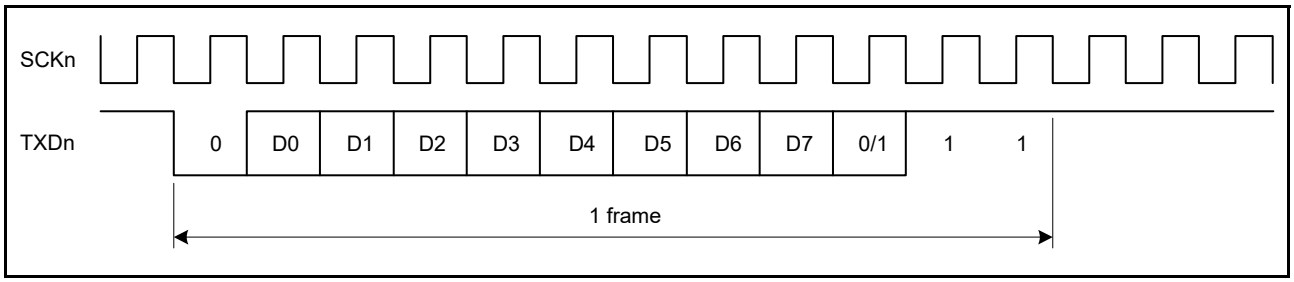


Figure 27.4 Phase relationship between output clock and transmit data in asynchronous mode when SMR.CHR = 0, PE = 1, MP = 0, and STOP = 1

27.3.4 Double-Speed Operation and Frequency of 6 Times the Bit Rate

When the SEMR.ABCS bit is set to 1 and 8 pulses of the base clock for a 1-bit period is selected, the SCI operates on the bit rate that is equal to twice the value when ABCS is set to 0. When the SEMR.BGDM bit is set to 1, the cycle of the base clock is half and the bit rate is double the value when BGDM is set to 0. When the SCR.CKE[1] bit is set to 0 and the on-chip baud rate generator is selected, setting the ABCS and BGDM bits to 1 allows the SCI to operate at a bit rate equal to four times the value when the ABCS and BGDM bits are set to 0. When the SEMR.ABCSE bit is set to 1, the number of basic clock pulses is 6 during a period of 1 bit, and the SCI operates at a bit rate that is equal to 16/3 times the value when SEMR.ABCS, SEMR.BGDM, and SMER.ABCSE are 0.

As shown by formula (1) in section 27.3.2, Receive Data Sampling Timing and Reception Margin in Asynchronous Mode, the reception margin decreases when the ABCS or ABCSE bit in SEMR is set to 1. Therefore, if the target bit rate can be obtained with ABCS or ABCSE set to 0, it is recommended that you use the SCI with ABCS and ABCSE set to 0.

27.3.5 CTS and RTS Functions

The CTS function uses the input on the CTSn_RTSn pin in transmission control. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, driving the CTSn_RTSn pin low causes transmission to start.

Driving the CTSn_RTSn pin high while transmission is in progress does not affect transmission of the current frame.

In the RTS function that uses the output on the CTSn_RTSn pin, a low level is output when reception becomes possible. Conditions for low level and high level output are shown in this section.

[Conditions for low-level output]

(a) Non-FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit is 1
- Reception is not in progress
- There is no receive data yet to be read
- The ORER, FER, and PER flags in the SSR register are all 0.

(b) FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit is 1

- The amount of receive data written in FRDRHL is equal to or less than the specified receive triggering number
- The ORER bit in the SSR_FIFO register (ORER in FRDRH) is 0.

[Condition for high-level output]

(a) Non-FIFO selected

- The conditions for low-level output are not satisfied
- When reception is terminated with SCR.RE = 0 without reading the RDR register after reception is complete, RTS remains high. At this time, read the SCR register for dummy values after writing 0 to SCR.RE.

(b) FIFO selected

- The conditions for low-level output are not satisfied.

27.3.6 Address Match (Receive Data Match Detection) Function

The address match function can be used only in asynchronous mode.

If the DCCR.DCME bit is set to 1*4, when one frame of data is received, the SCI compares that received data with the data set in CDR.CMPD. If SCI detects a match between the comparison data (CDR.CMPD*3) and the received data, the SCI can issue the SCIn_RXI interrupt request.

If the SMR.MP bit is set to 0, comparison occurs only for valid data in receive format. In multi-processor mode (SMR.MP bit = 1), if the DCCR.IDSEL bit is set to 1, receive data where the MPB bit is 1 is subject to comparison for address match. Receive data where the MPB bit is 0 is always treated as a mismatch.

If the DCCR.IDSEL bit is set to 0, the SCI performs address match detection regardless of the MPB bit value of the received data. Until the SCI detects a match between the comparison data (CDR.CMPD*3) and the receive data, the received data is skipped (discarded), and the SCI cannot detect a parity error or framing error. When the SCI detects a match, the DCCR.DCME bit is automatically cleared, and the DCCR.DCMF flag is set to 1.

If the DCCR.IDSEL bit is set to 1, the SCR.MPIE bit is automatically cleared. If DCCR.IDSEL is set to 0, the value of the SCR.MPIE bit is retained. If the SCR.RIE bit is set to 1, the SCI issues an SCIn_RXI interrupt request.

If the SCI detects a framing error in the receive data for which a match is detected, the DCCR.DFER bit is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER bit is set to 1. The compared receive data is not stored in the RDR register*1, and SSR.RDRF remains at 0.*2

After the SCI detects a match, and DCCR.DCME is automatically cleared, the SCI receives the next data continuously based on the current register setting.

When the DCCR.DFER or DCCR.DPER flag is set, the address match is not performed. Before enabling the address match function, set the DCCR.DFER and DCCR.DPER flags to 0.

Examples of the address match function are shown in Figure 27.5 and Figure 27.6.

Note 1. When FCR.FM = 1, this refers to the FRDRHL register.
Note 2. When FCR.FM = 1, this refers to the SSR_FIFO.RDF flag.
Note 3. This comparative target can select one length of 3 types: CMPD[6:0] with 7-bit length, CMPD[7:0] with 8-bit length, or CMPD[8:0] with 9-bit length.
Note 4. Set the DCCR.DCME bit to 1 before receiving the start bit of the received frame that performs address matching.

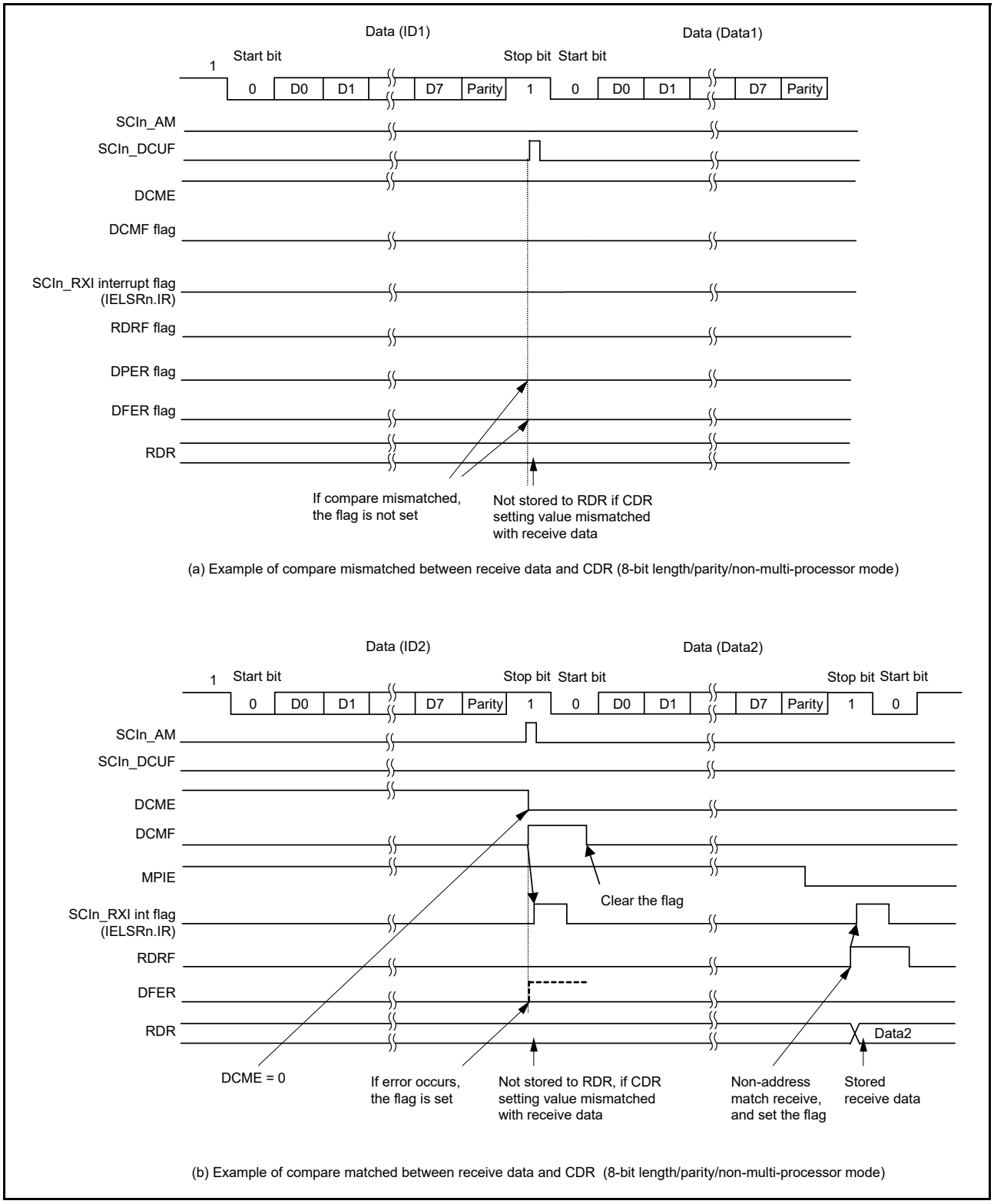


Figure 27.5 Example of address match (1) in non-multi-processor mode

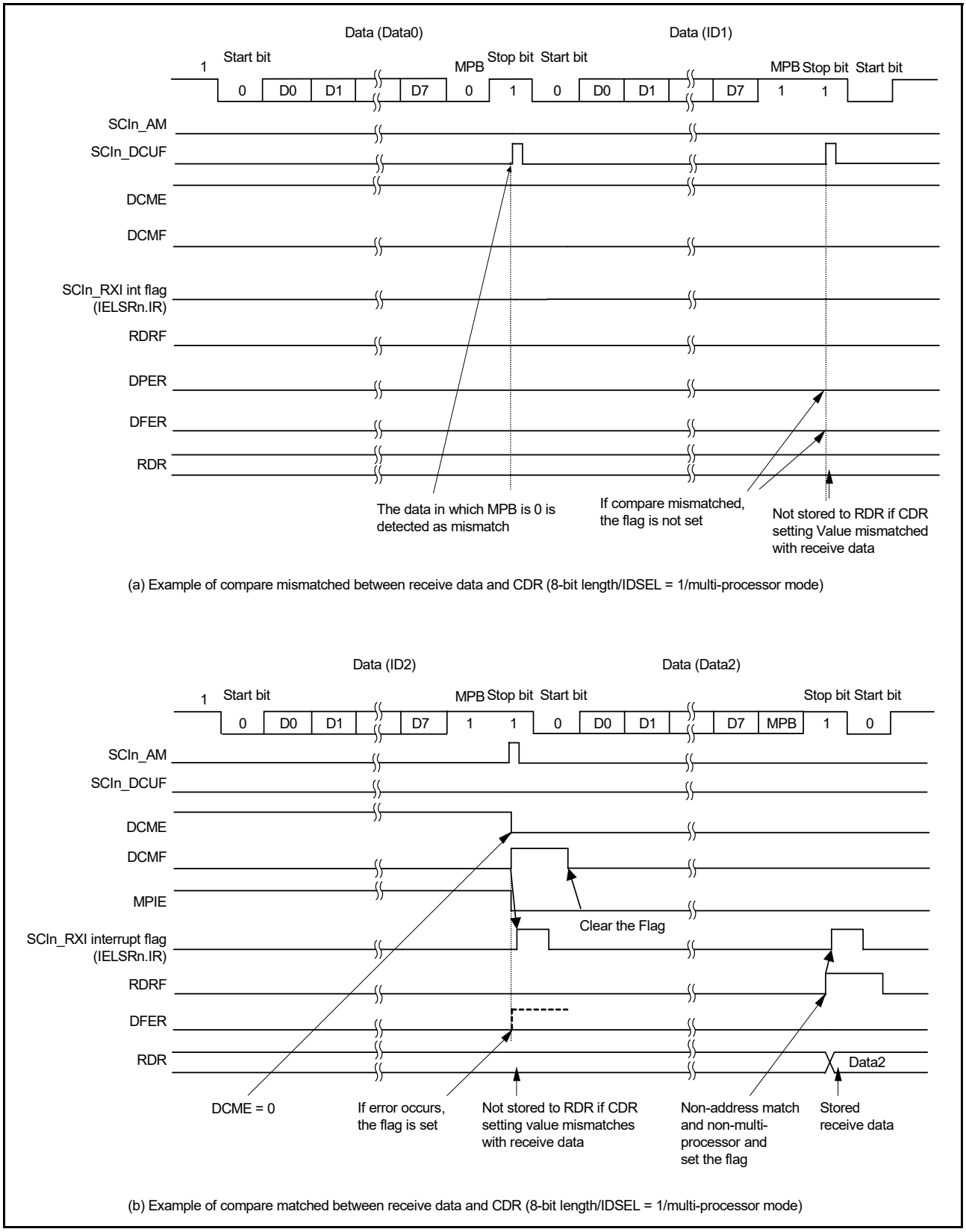


Figure 27.6 Example of address match (2) multi-processor mode

27.3.7 SCI Initialization in Asynchronous Mode

Before transmitting and receiving data, start by writing the initial value 00h to the SCR register, then continue through to the SCI initialization procedure (select non-FIFO or FIFO) shown in Figure 27.7 and Figure 27.8. Whenever the operating mode or transfer format is to be changed, the SCR register must be initialized before the change is made.

When the external clock is used in asynchronous mode, ensure that the clock signal is supplied during initialization.

Note: When the SCR.RE bit is set to 0, the ORER, FER, RDRF, RDF, PER, and DR flags in SSR/SSR_FIFO, and the RDR and RDRHL registers are not initialized. When the SCR.TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: Switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of an SCIn_TXI interrupt request.

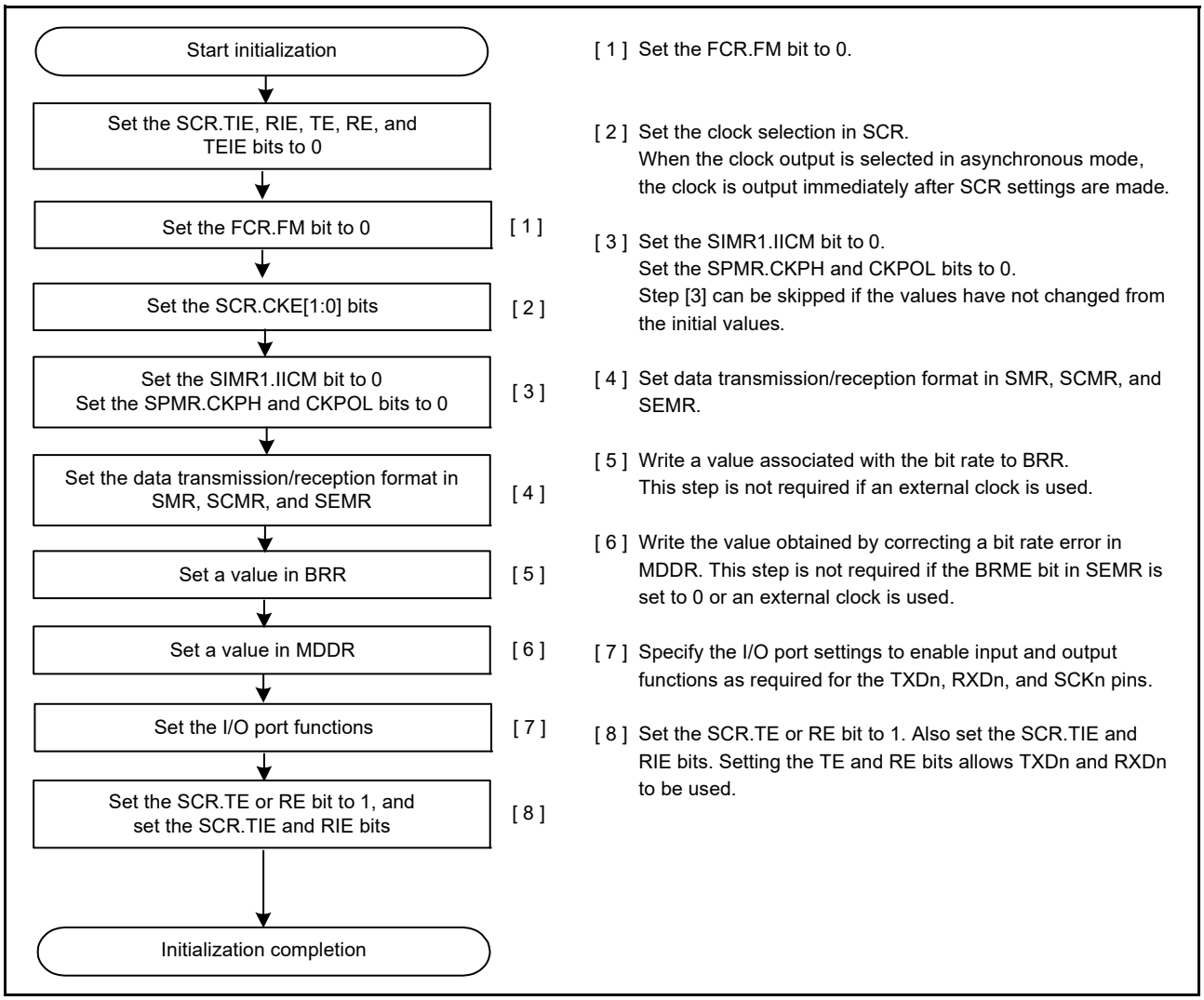


Figure 27.7 Example SCI initialization flow in asynchronous mode with non-FIFO selected

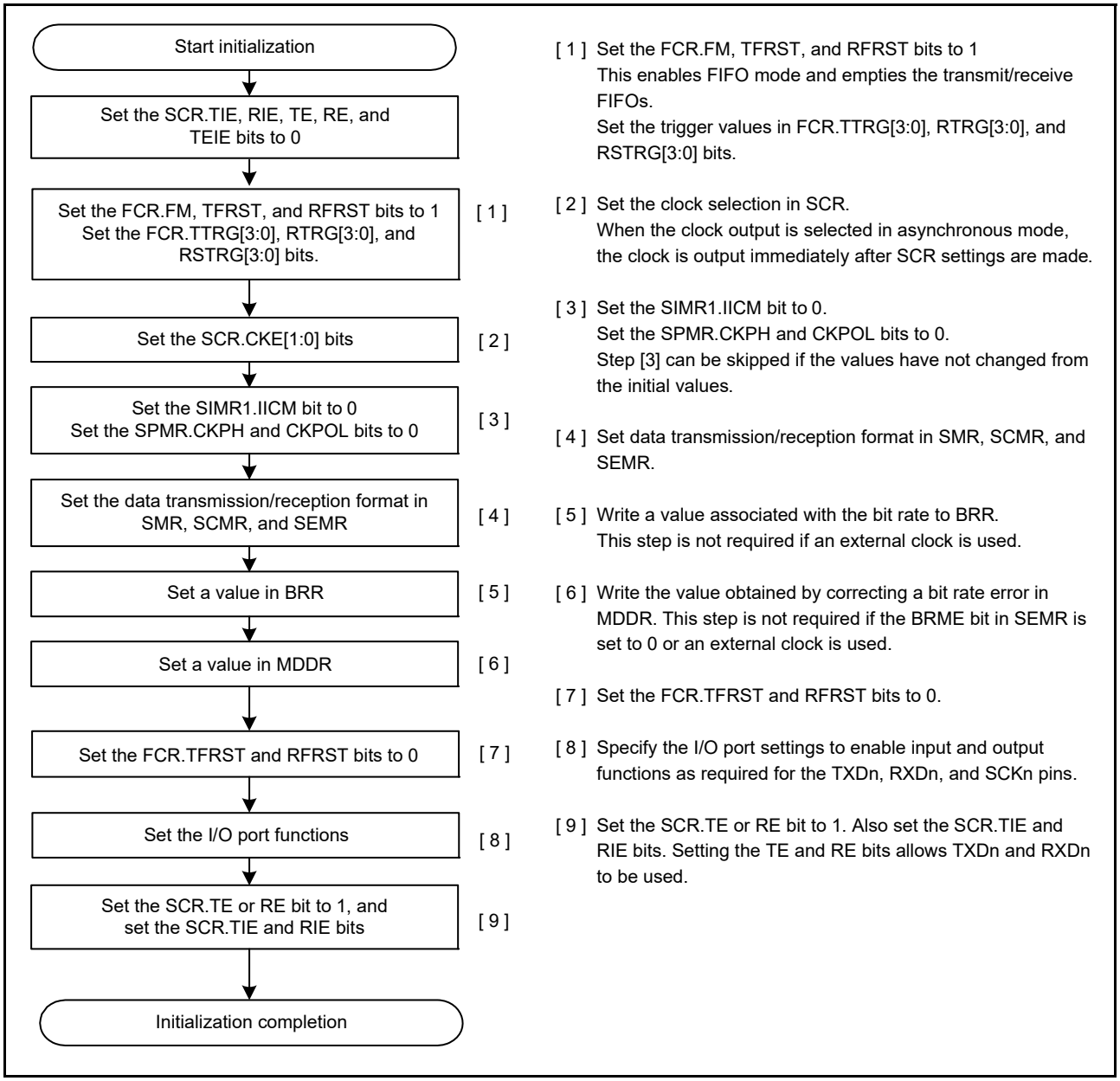


Figure 27.8 Example SCI initialization flow in synchronous mode with FIFO selected

27.3.8 Serial Data Transmission in Asynchronous Mode

(1) Non-FIFO selected

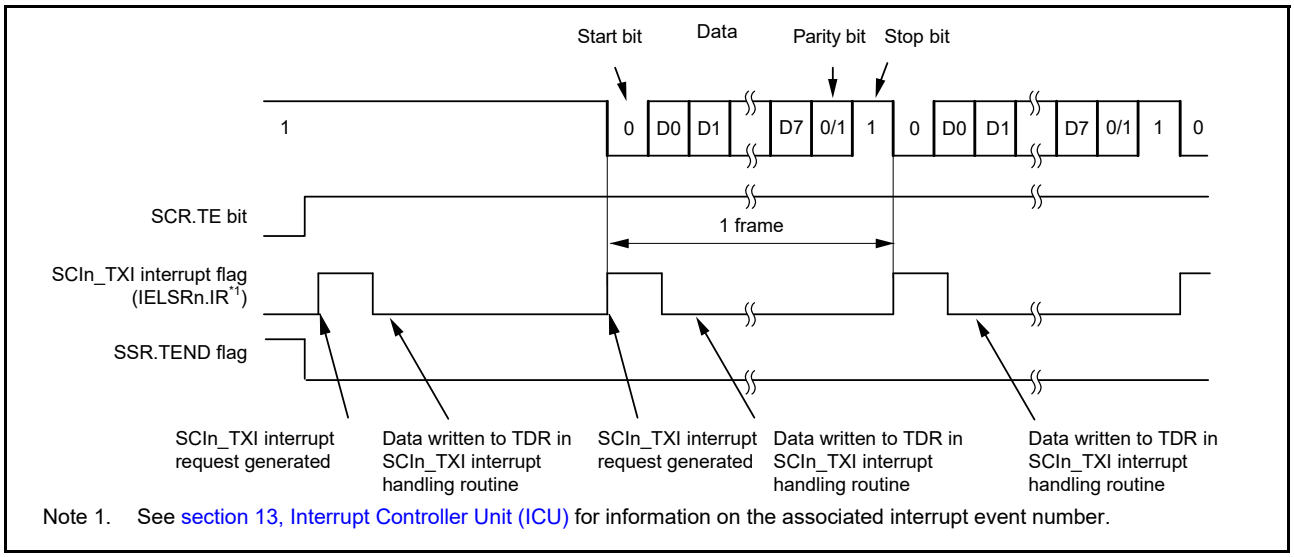
Figure 27.9, Figure 27.10, and Figure 27.11 show examples of serial transmission in asynchronous mode.

In serial transmission, the SCI operates as described in this section. When the SCR.TE bit is set to 1, the high level for one frame (preamble) is output to TXDn.

1. The SCI transfers data from TDR*1 to TSR when data is written to TDR*1 in the SCIn_TXI interrupt handling routine.
   The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE and TIE bits in the SCR are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from TDR*1 to TSR. If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to TDR*1 in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (an SCIn_TXI interrupt request is disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to TDR*1 from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit.
4. The SCI checks for an update of the TDR register on the output of the stop bit.
5. When TDR is updated, setting the SPMR.CTSE bit to 0 (CTS function is disabled) or a low-level input on the CTSn_RTSn pin, causes the transfer of the next transmit data from TDR*1 to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If TDR is not updated, the SSR.TEND flag is set to 1, the stop bit is sent, and the mark state is entered, where 1 is output. If the SCR.TEIE bit is 1, the SSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

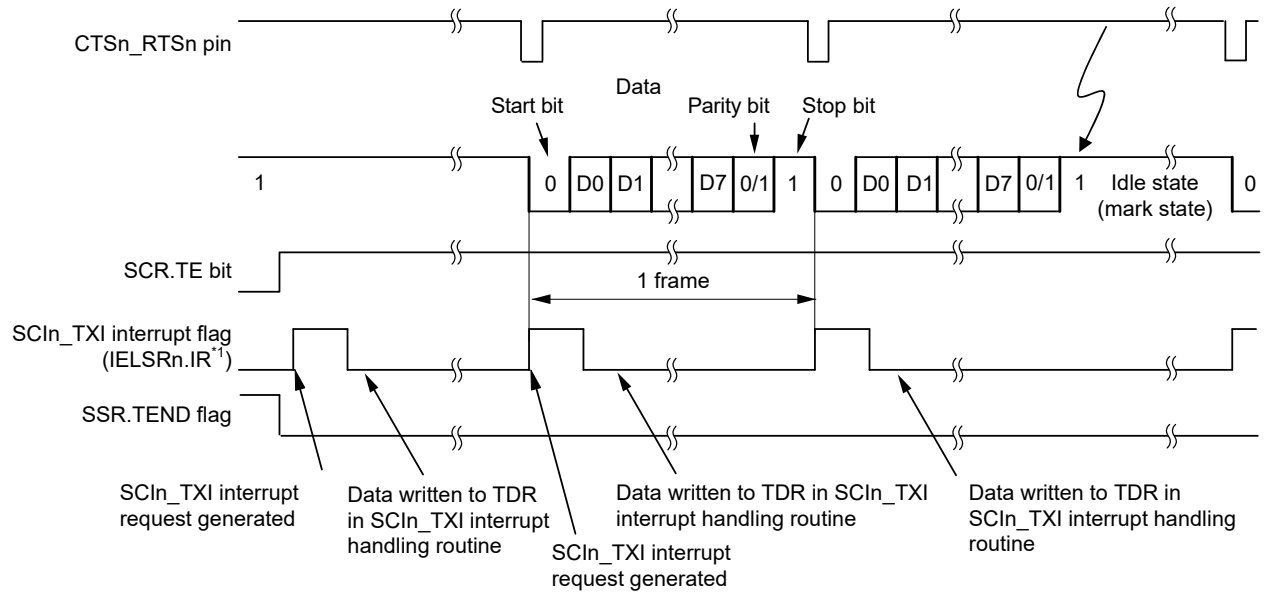
Note 1. Only write data to the TDRHL register when 9-bit data length is selected.

Figure 27.9, Figure 27.10, and Figure 27.11 show examples of serial transmission in asynchronous mode.



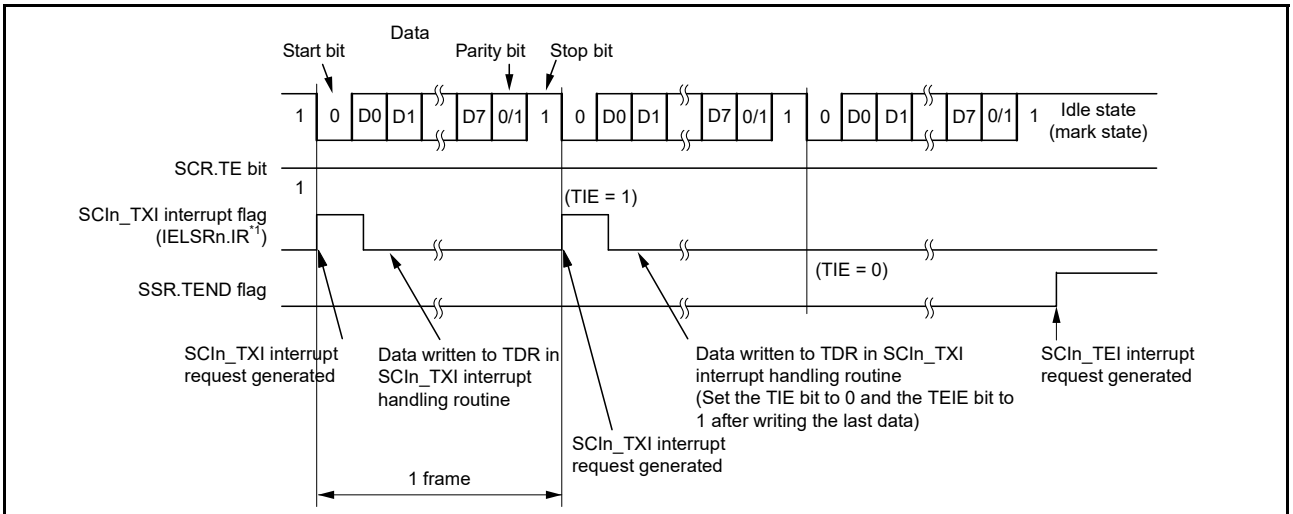
Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 27.9 Example of operation for serial transmission in asynchronous mode (1) with 8-bit data, parity bit, 1 stop bit, CTS function not used, and at the beginning of transmission



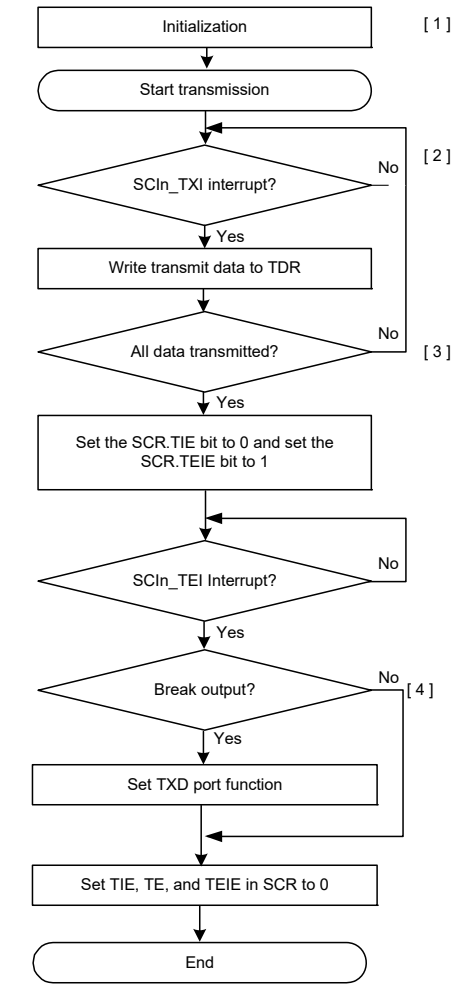
Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 27.10 Example of operation for serial transmission in asynchronous mode (2) with 8-bit data, parity bit, 1 stop bit, CTS function used, and at the beginning of transmission



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 27.11 Example of operation for serial transmission in asynchronous mode (3) with 8-bit data, parity bit, 1 stop bit, CTS function not used, and from the middle of transmission until transmission completion



[1] SCI Initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame (preamble), and transmission is enabled.

[2] Transmit data write to TDR by an SCIn_TXI interrupt request. When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated. Write transmit data to TDR while in the SCIn_TXI interrupt processing routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR once using an SCIn_TXI interrupt request. Transmit data can also be written to TDR by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to TDR.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (low-level output) of TXDn pin using the SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Note: The TDR register becomes the TDRHL register when 9-bit data length is selected.

Figure 27.12 Example of serial transmission flow in asynchronous mode with non-FIFO selected

(2) FIFO selected

Figure 27.13 shows an example of a data format that is written to FTDRH and FTDRL in asynchronous mode.

Data that corresponds to the data length is set to FTDRH and FTDRL. Write 0 for unused bits. Write in order from FTDRH to FTDRL.

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	—	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	—	9-bit transmit data								

—: Invalid. The write value should be 0.

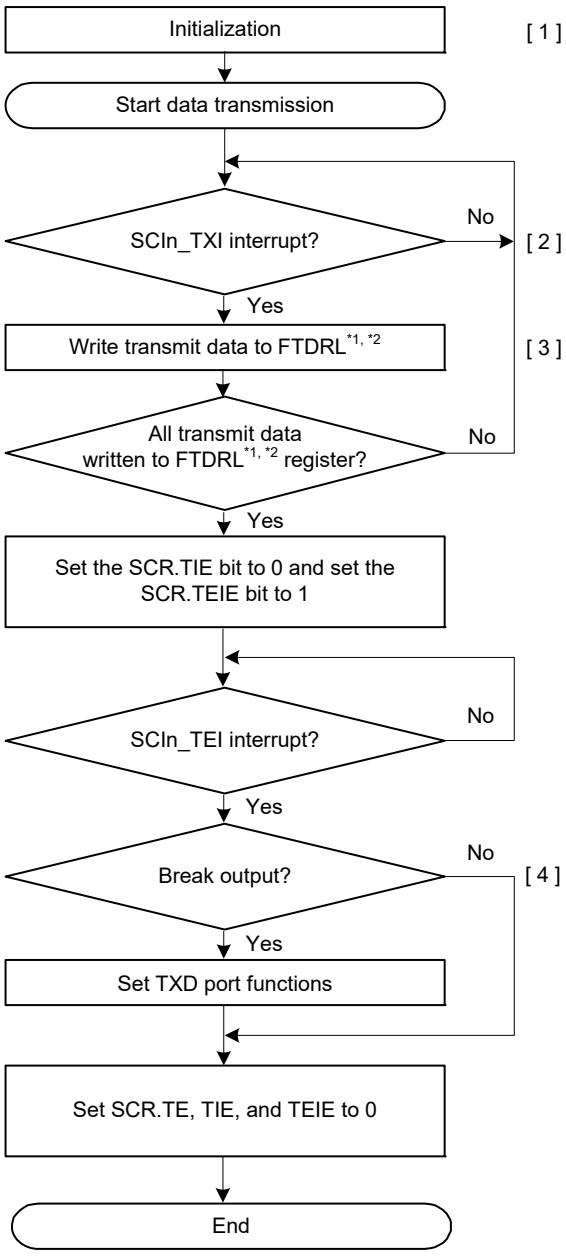
Figure 27.13 Data format written to FTDRH and FTDRL with FIFO selected

In serial transmission, the SCI operates as described in this section. When the TE bit is set to 1, the high level for one frame (preamble) is output to TXD.

1. The SCI transfers data from FTDRL*1 to TSR when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE and TIE bits in SCR are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from FTDRL*1 to TSR. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, SSR_FIFO.TDFE is set to 1. If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to FTDRL*1 in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (an SCIn_TXI interrupt request is disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to FTDRL*1 *2 from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit.
4. On output of the stop bit, the SCI checks whether non-transmitted data remains in FTDRL*3.
5. When data is set to FTDRL*3, setting the SPMR.CTSE bit to 0 (CTS function is disabled) or a low-level input on the CTSn_RTSn pin causes transfer of the next transmit data from FTDRL*1 to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If data is not set in FTDRL*3, the TEND flag in SSR_FIFO is set to 1, the stop bit is sent, and the mark state is entered where 1 is output. If the SCR.TEIE bit is 1, the SSR_FIFO.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Write data to the FTDRH and FTDRL registers when 9-bit data length is selected.
Note 2. Write data in order from FTDRH to FTDRL when 9-bit data length is selected.
Note 3. The SCI only checks for an update to the FTDRL register and not the FTDRH register when 9-bit data length is selected.

Figure 27.14 shows an example flow of serial transmission in asynchronous mode with FIFO selected.



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame (preamble), and transmission is enabled.

[2] Transmit data write to FTDRL*1 by an SCIn_TXI interrupt request:
For data transmission from FTDRL to TSR, when the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL*1, *2 once in the SCIn_TXI interrupt handling routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write all transmit data to FTDRL using an SCIn_TXI interrupt request and clear the SSR_FIFO.TDFE flag to 0. It is possible to write 16 minus the amount of data stored in the transmit FIFO. Transmit data can also be written to FTDRL by activating the DMAC or DTC. When data is written to FTDRL by DMAC or DTC, the TDFE flag is cleared automatically. Therefore, do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to FTDRL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (low-level output) of the TXDn pin using SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Note 1. When data length is 9 bits, FTDRH and FTDRL registers are used.
Note 2. When data length is 9 bits, write in order from FTDRH to FTDRL.

Figure 27.14 Example of serial transmission flow in asynchronous mode with FIFO selected

27.3.9 Serial Data Reception in Asynchronous Mode

(1) Non-FIFO selected

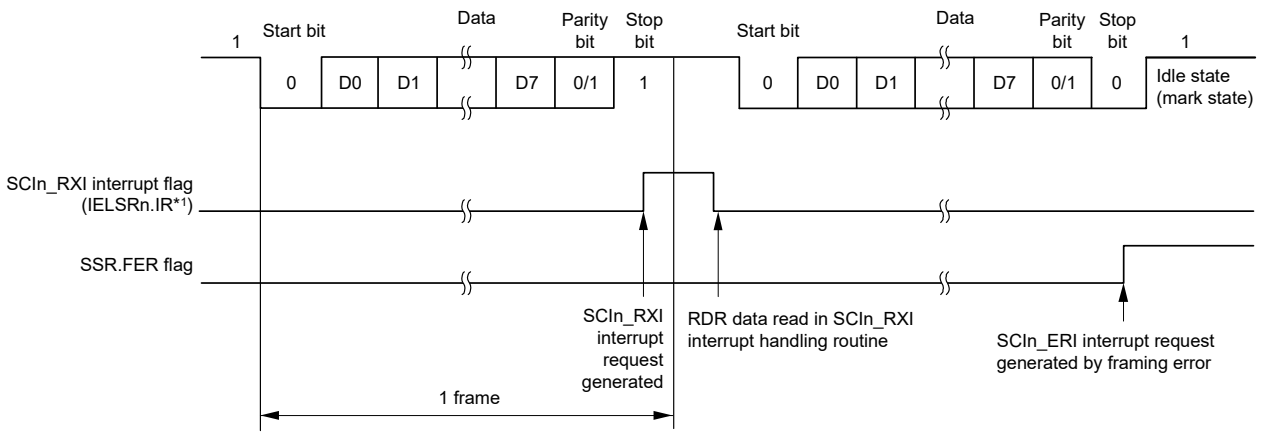
Figure 27.15 and Figure 27.16 show an example of the operation for serial data reception in asynchronous mode.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. When the SCI monitors the communications line and detects a start bit, it performs internal synchronization, stores receive data in RSR, and checks the parity bit and stop bit.
3. If an overrun error occurs, the SSR.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to RDR*1.

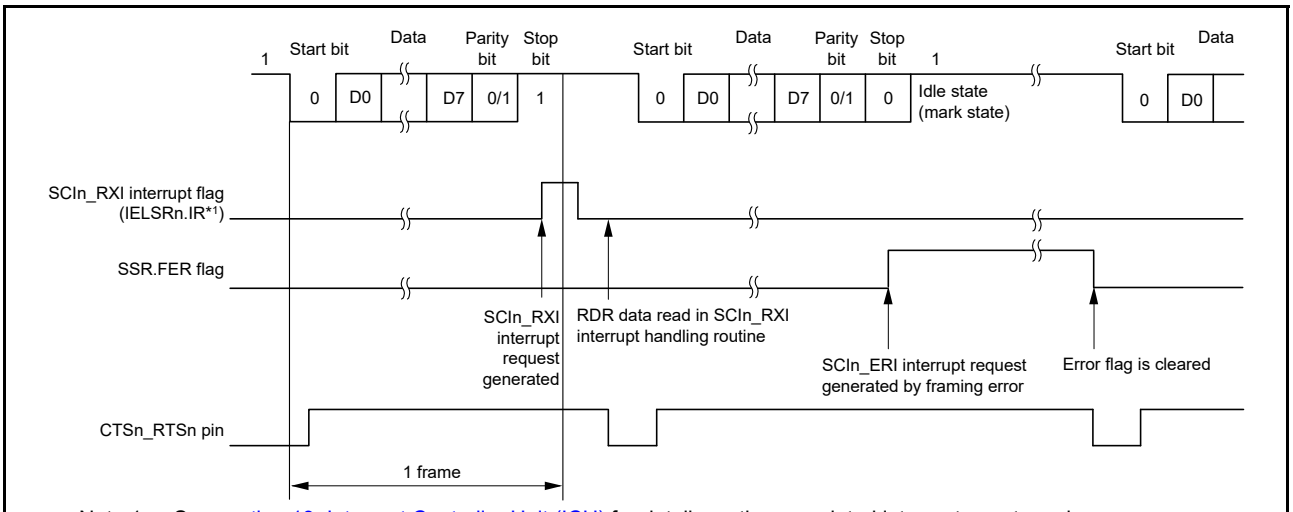
4. If a parity error is detected, the SSR.PER flag is set to 1 and receive data is transferred to RDR*1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
5. If a frame error is detected, the SSR.FER flag is set to 1 and receive data is transferred to RDR*1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
6. When reception finishes successfully, receive data is transferred to RDR*1. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to RDR in the SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data that was transferred to RDR causes the CTSn_RTSn pin to output low.

Note 1. Only read data in the RDRHL register when 9-bit data length is selected.



Note 1. See section 13, Interrupt Controller Unit (ICU) for details on the associated interrupt event number.

Figure 27.15 Example of SCI operation for serial reception in asynchronous mode (1) when the RTS function is not used, and with 8-bit data, parity bit, and 1 stop bit



Note 1. See section 13, Interrupt Controller Unit (ICU) for details on the associated interrupt event number.

Figure 27.16 Example of SCI operation for serial reception in asynchronous mode (2) when RTS function is used, and with 8-bit data, parity bit, and 1 stop bit

Table 27.24 lists the states of the flags in the SSR register and receive data handling when a receive error is detected.

If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated. Data reception cannot be resumed while the receive error flag is 1. Also, set the ORER, FER, and PER flags to 0 before resuming reception. In addition, be sure to read the RDR or RDRHL register during overrun error processing.

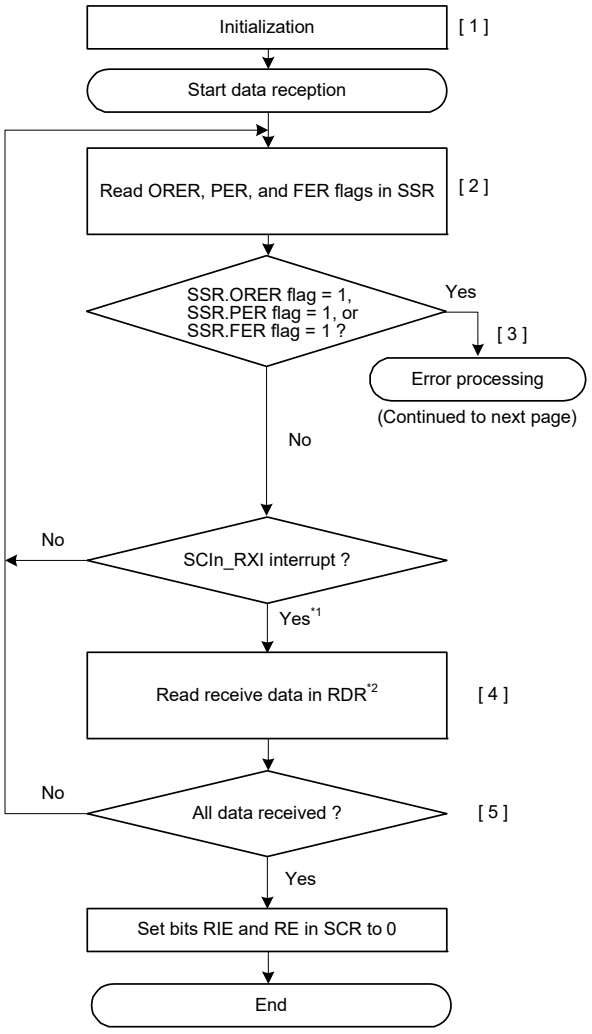
When a reception is forcibly terminated by setting the SCR.RE bit to 0 during operation, read the RDR or RDRHL register because the received data that is not yet read might be left in RDR or RDRHL.

Figure 27.17 and Figure 27.18 show example flows for serial data reception.

Table 27.24 Flags in SSR Status Register and receive data handling

Flags in the SSR Status Register				
ORER	**FER**	**PER**	**Receive data**	**Receive error type**
1	0	0	Lost	Overrun error
0	1	0	Transferred to RDR	Framing error
0	0	1	Transferred to RDR	Parity error
1	1	0	Lost	Overrun error + framing error
1	0	1	Lost	Overrun error + parity error
0	1	1	Transferred to RDR	Framing error + parity error
1	1	1	Lost	Overrun error + framing error + parity error

Note 1. Only read data in the RDRHL register when 9-bit data length is selected.



[1] SCI initialization:
Set data reception.

[2] [3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. The error type is identified by reading the ORER, PER, and FER flags in SSR. After performing the appropriate error processing, be sure to set the ORER, PER, and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. For a framing error, a break can be detected by reading the value of the input port associated with the RXDn pin.

[4] Read the receive data in RDR once in the SCIn_RXI interrupt handling routine.

[5] Serial reception continuation procedure:
To continue serial reception, before the stop bit of the current frame is received, read data from RDR in the SCIn_RXI interrupt processing routine. The RDR data can also be read by activating the DMAC or DTC.

Note 1. Do not set RE to 0 before reading RDR.
Note 2. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 27.17 Example flow of serial reception in asynchronous mode with non-FIFO selected (1)

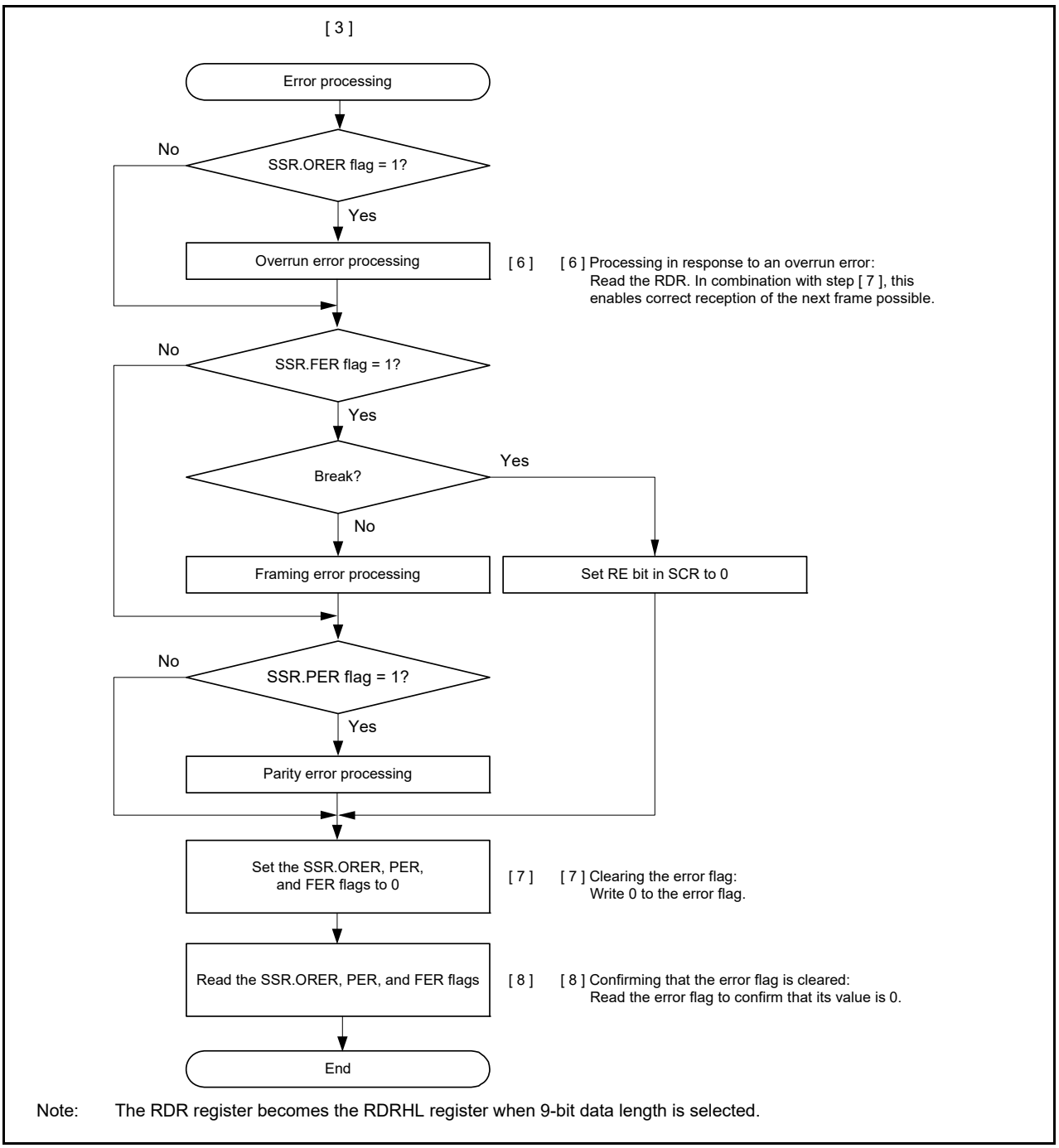


Figure 27.18 Example flow of serial reception in asynchronous mode with non-FIFO selected (2)

(2) FIFO selected

Figure 27.19 shows an example of a data format that is written to FRDRH and FRDRL in asynchronous mode.

In asynchronous mode, 0 is written to the MPB flag in FRDRH. Data that corresponds to the data length is written to FRDRH and FRDRL. Unused bits are written as 0. Read in the order from FRDRH to FRDRL. If software reads FRDRL, the SCI updates FER, PER, and receive data (RDAT[8:0]) in FRDRL with the next data. The RDF, ORER, and DR flags in FRDRH always reflect the associated flags in the SSR_FIFO register.

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	PER	DR	0	9-bit receive data								

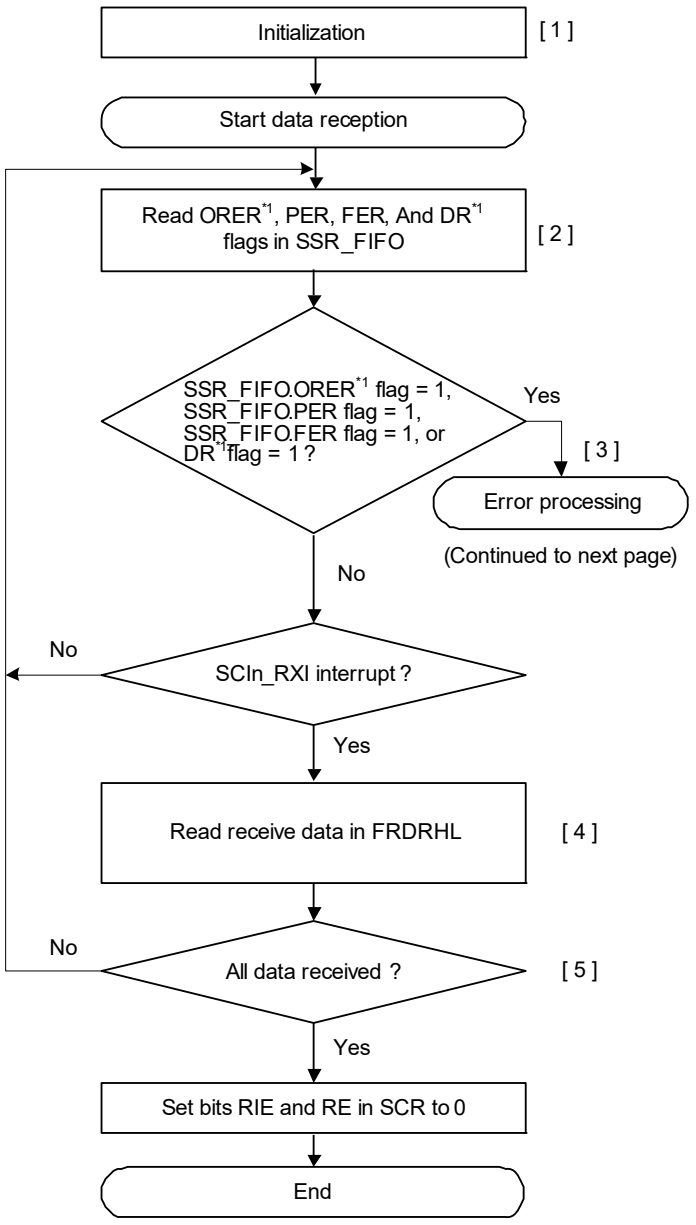
Note: 0 is always read for MPB flag (FRDRH[1]).
When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7].
When data length is 8 bits, 0 is always read for FRDRH[0].
FRDRH[7] bit is read as an indefinite value.

Figure 27.19 Data format stored in FRDRH and FRDRL with FIFO selected

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. When the SCI monitors the communications line and detects a start bit, it performs internal synchronization, stores receive data in the RSR register, and checks the parity bit and stop bit.
3. When the FRDRL register is full, an overrun error occurs. If an overrun error occurs, the SSR_FIFO.ORER flag is set to 1. When the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to FRDRL*1.
4. If a parity error is detected, the PER flag and receive data are transferred to FRDRL*1. When the RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
5. If a frame error is detected, the FER flag and receive data are transferred to FRDRL*1. When the RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
6. After a framing error is detected and when SCI detects that the continuous receive data is for one frame, reception stops.
7. When the amount of data stored in the FRDRL register falls below the specified receive triggering number, and the next data is not received after 15 ETUs from the last stop bit in asynchronous mode, the SSR_FIFO.DR bit is set to 1. When the RIE bit is 1 and the FCR.DRES bit is 0, the SCI generates an SCIn_RXI interrupt request. When the FCR.DRES bit is 1, SCI generates an SCIn_ERI interrupt request.
8. When reception finishes successfully, receive data is transferred to FRDRL*1. The RDF bit is set to 1 when the amount of receive data written to FRDRHL is equal to or greater than the specified receive triggering number. When the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to FRDRL*2 in the SCIn_RXI interrupt handling routine, before an overrun error occurs. If the received data that is transferred to FRDRL*3 is less than the RTS trigger number, the CTSn_RTSn pin outputs low.

Note 1. Only read the data in the FRDRH and FRDRL registers when 9-bit data length is selected.
Note 2. Read the data in the order from FRDRH to FRDRL when 9-bit data length is selected.
Note 3. The SCI only checks for an update to the FRDRL register and not to the FRDRH register when 9-bit data length is selected.



[1] SCI initialization:
Set data reception.

[2] [3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. A break can be detected by reading the SPTR.RXDMON bit. An error is identified by reading the ORER*1, PER, DR*1, and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the ORER*1 flag to 0. Reception cannot be resumed if ORER*1 flag is set to 1. The reception operation is continuous, even when FER = 1 or PER = 1 or DR*1 = 1.

[4] Read the receive data in FRDRHL in the SCIn_RXI interrupt handling routine. The receive data stored in the FRDRHL register is read until the number of stored data is below the FCR.RTRG[3:0] value. Confirm the number of receive data bits in the FIFO by reading the FDR.R[4:0] bits.

[5] Serial reception continuation procedure:
To continue serial reception, before an overrun error occurs, read data from FRDRHL in the SCIn_RXI interrupt handling routine and clear RDF and DR flags to 0.
The FRDRHL data can also be read by activating the DMAC or DTC. The RDF flag is cleared automatically in this case. Therefore, do not write to the RDF flag.

Note 1. Can be read by the FRDRHL.ORER and DR flags.

Figure 27.20 Example flow of serial reception in asynchronous mode with FIFO selected (1)

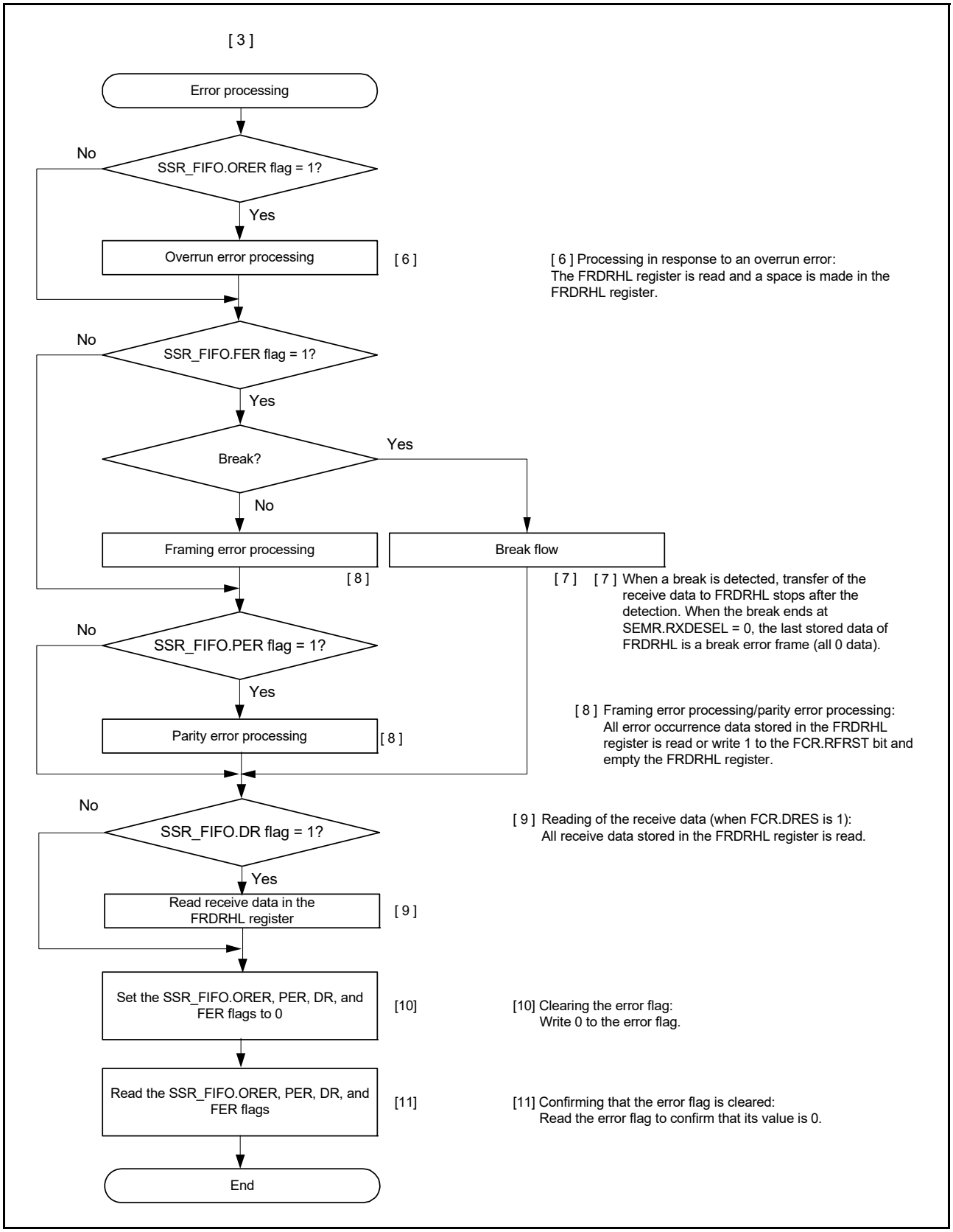


Figure 27.21 Example flow of serial reception in asynchronous mode with FIFO selected (2)

27.4 Multi-Processor Communication Function

The multi-processor communication function enables the SCI to transmit and receive data by sharing a communication line between multiple processors, using asynchronous serial communication in which the multi-processor bit is added. In multi-processor communication, a unique ID code is allocated to each receiving station. Serial communication cycles consist of an ID transmission cycle to specify the receiving station and a data transmission cycle to transmit data to the specified receiving station.

The multi-processor bit is used to distinguish between the ID transmission cycle and the data transmission cycle:

- When the multi-processor bit is set to 1, the transmission cycle is the ID transmission cycle
- When the multi-processor bit is set to 0, the transmission cycle is the data transmission cycle.

Figure 27.22 shows an example of communication between processors using a multi-processor format. First, a transmitting station transmits communication data in which the multi-processor bit set to 1, is added to the ID code of the receiving station. Next, the transmitting station transmits communication data in which the multi-processor bit set to 0, is added to the transmit data. After receiving communication data with the multi-processor bit set to 1, the receiving station compares the received ID with the ID of the receiving station itself. If the two match, the receiving station receives communication data that is subsequently transmitted. If the received ID does not match with the ID of the receiving station, the receiving station skips the communication data until it receives data again in which the multi-processor bit is set to 1.

(1) Non-FIFO selected

To support this function, the SCI provides the SCR.MPIE bit. When the MPIE bit is set to 1, the following operations are disabled until the reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR to the RDR (the RDRHL register when 9-bit data length is selected)
- Detection of a receive error
- Setting of the respective RDRF, ORER, and FER status flags in the SSR register.

When the SCI receives a character in which the multi-processor bit is set to 1, the SSR.MPBT bit is set to 1 and the SCR.MPIE bit is automatically cleared, returning the SCI to non-multi-processor reception operation. An SCIn_RXI interrupt is generated if the RIE bit in SCR is set.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in non-multi-processor asynchronous mode. The clock used for multi-processor communication is the same as the clock used in non-multi-processor asynchronous mode.

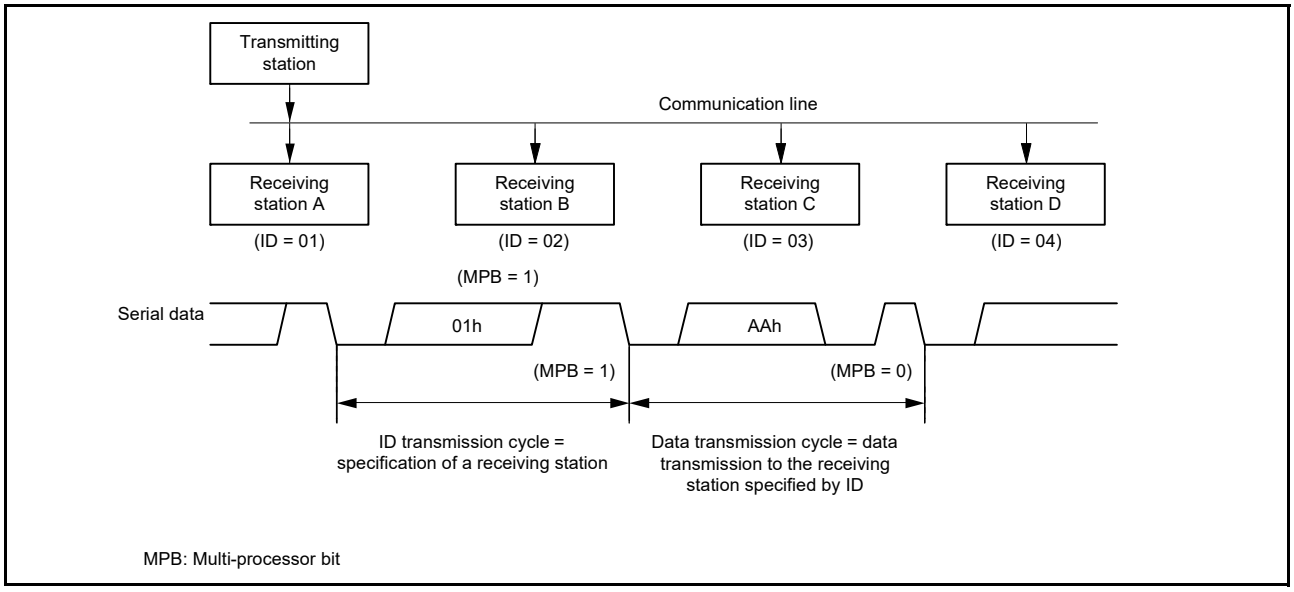


Figure 27.22 Example of communication using multi-processor format with transmission of data AAh to receiving station A

(2) FIFO selected

For data transmission, software must write data to FTDRHL.MPBT that corresponds to transmit data in FTDRHL.TDAT. For data reception, the multi-processor bit that is part of the receive data is written to FRDRHL.MPB, and receive data is written to FRDRL.

When the MPIE bit is set to 1, the following operations are disabled until reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from RSR to FRDRHL
- Detection of a receive error
- Break
- Setting of the respective RDF, ORER, and FER status flags in the SSR_FIFO register.

On receiving an 8-bit character in which the multi-processor bit is set to 1, the FRDRHL.MPB bit is set to 1 and receive data is written to FRDRHL.RDAT. The SCR.MPIE bit is automatically cleared, therefore returning the SCI to non-multi-processor reception operation. An SCIn_RXI interrupt is generated if the RIE bit in SCR is set.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in non multi-processor asynchronous mode with non-FIFO selected.

27.4.1 Multi-Processor Serial Data Transmission

(1) Non-FIFO selected

Figure 27.23 shows an example flow of multi-processor data transmission. In the ID transmission cycle, the ID must be transmitted with the SSR.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as in asynchronous mode.

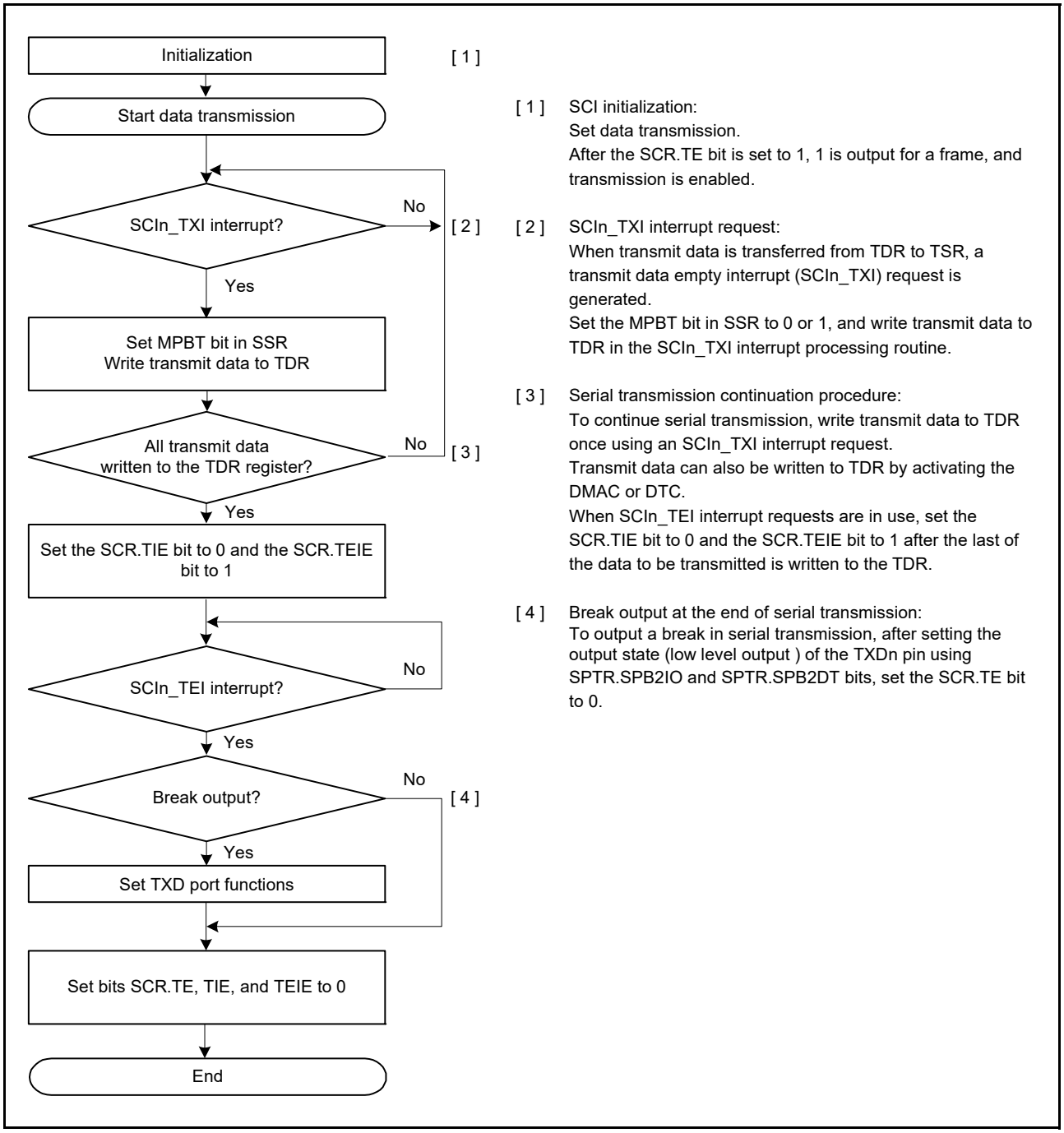


Figure 27.23 Example flow of multi-processor serial transmission with non-FIFO selected

(2) FIFO selected

Figure 27.24 shows an example of the data format that is written to FTDRH and FTDRL in multi-processor mode.

The FTDRH.MPBT bit is set to 1. Data is set to FTDRH and FTDRL with the correct data length. Write 0 for unused bits. Write in the order from FTDRH to FTDRL.

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	MPBT	9-bit transmit data								

—: Invalid. The write value should be 0.

Figure 27.24 Data format written to FTDRH and FTDRL in multi-processor mode with FIFO selected

Figure 27.25 shows an example flow of multi-processor data transmission with FIFO selected. In the ID transmission cycle, the ID must be transmitted with the FTDRH.MPBT bit set to 1. In the data transmission cycle, data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as in asynchronous mode with non-FIFO selected.

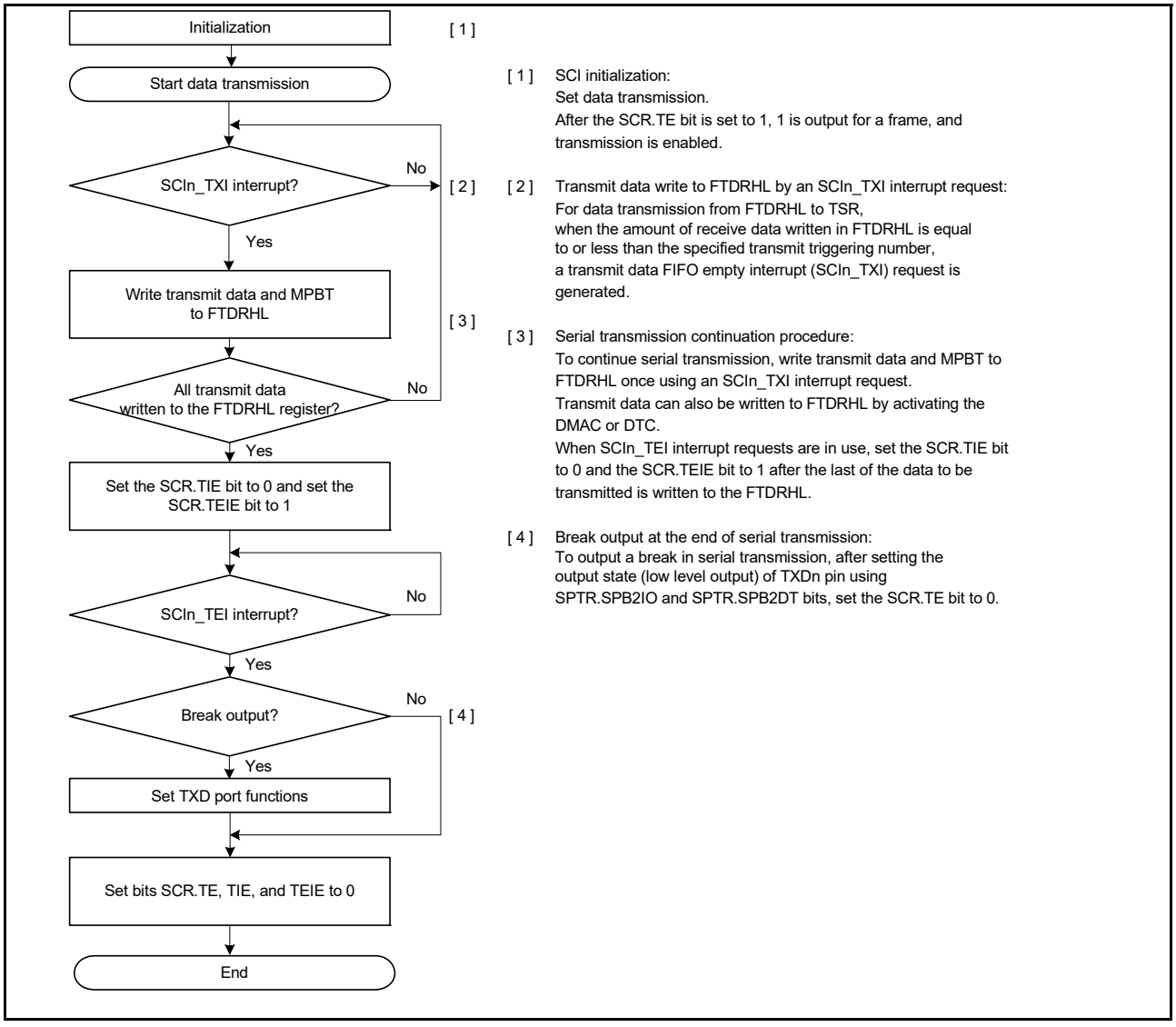


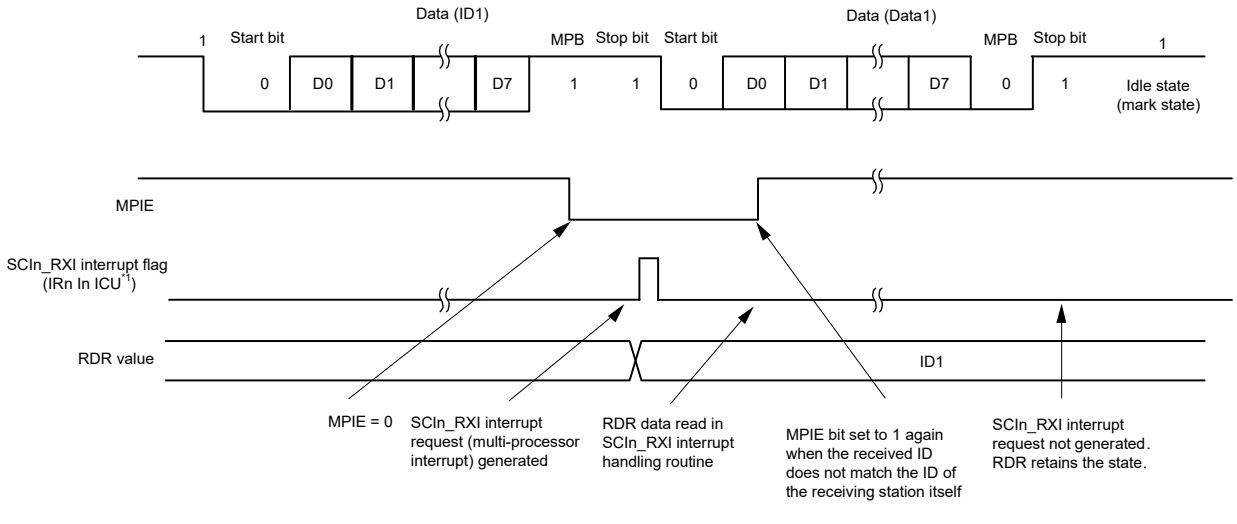
Figure 27.25 Example flow of serial transmission in multi-processor mode with FIFO selected

27.4.2 Multi-Processor Serial Data Reception

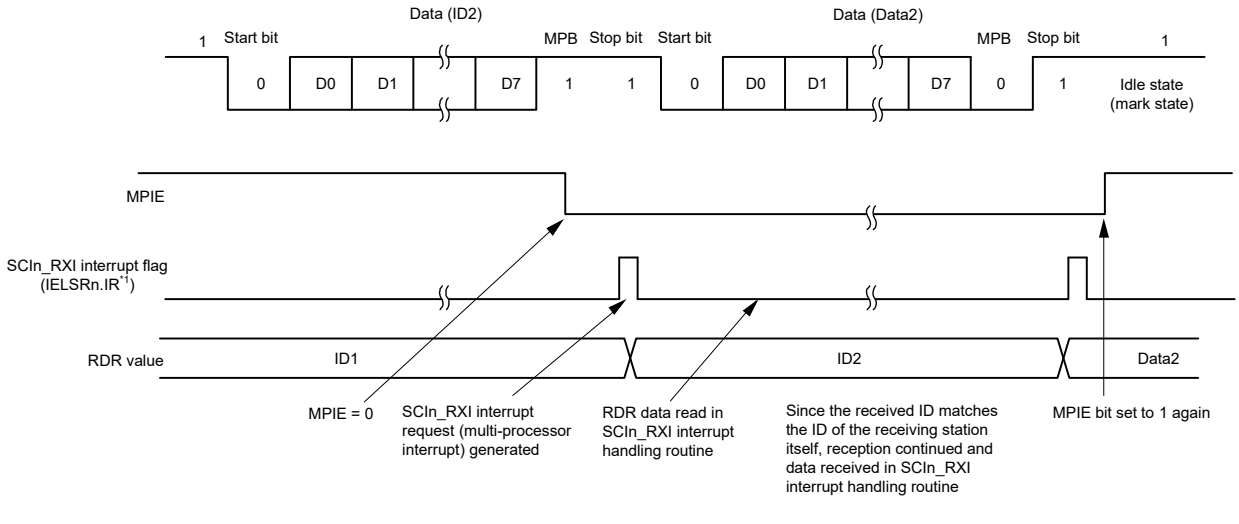
(1) Non-FIFO selected

Figure 27.27 and Figure 27.28 show example flows of multi-processor data reception. When the SCR.MPIE bit is set to 1, reading communication data is skipped until the reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data is transferred to RDR, or RDRHL when 9-bit data length is selected, and the SCIn_RXI interrupt request is generated. The rest of the operations are the same as in asynchronous mode.

Figure 27.26 shows an example of operation for data reception.



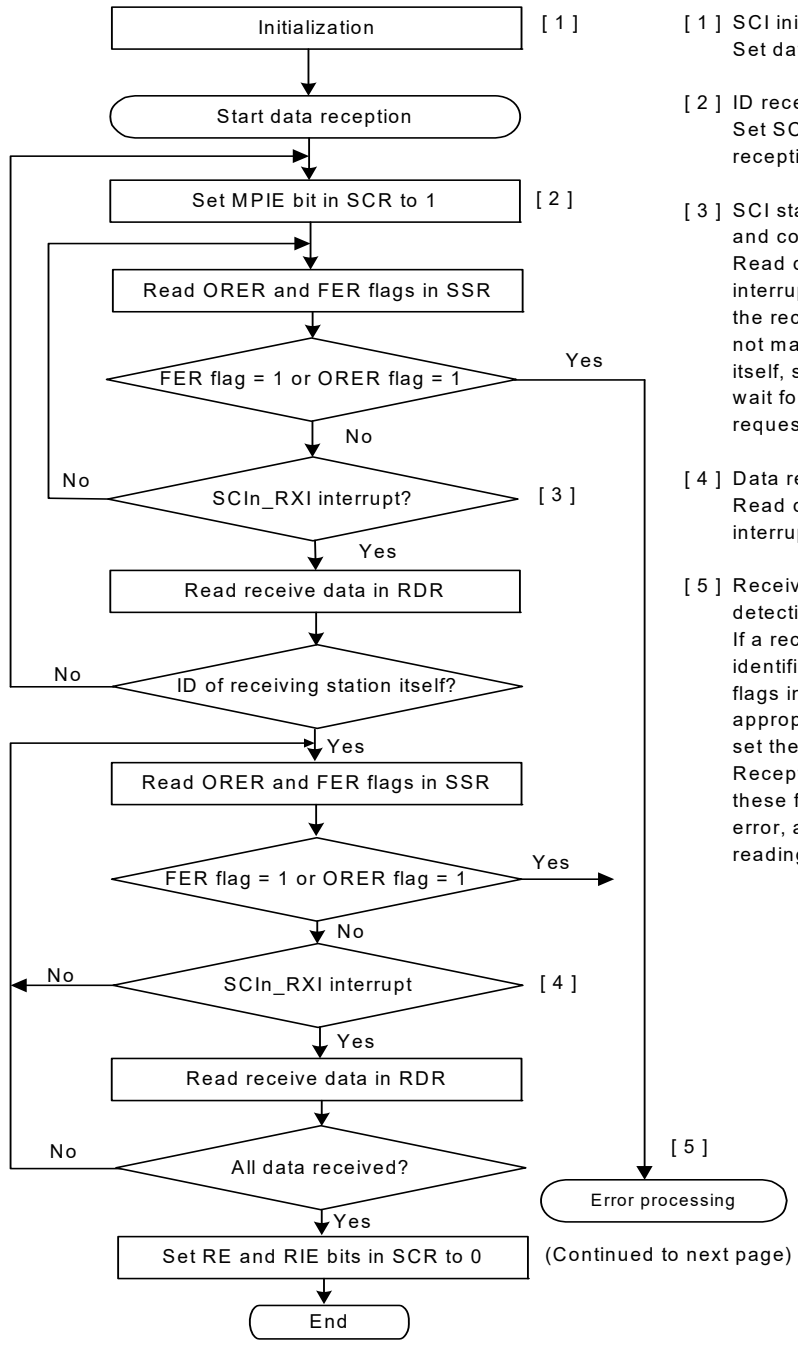
(a) When the received ID does not match the ID of the receiving station itself



(b) When the received ID matches the ID of the receiving station itself

Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 27.26 Example of SCI reception with 8-bit data, multi-processor bit, and 1 stop bit



Note 1. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 27.27 Example flow of multi-processor serial reception with non-FIFO selected (1)

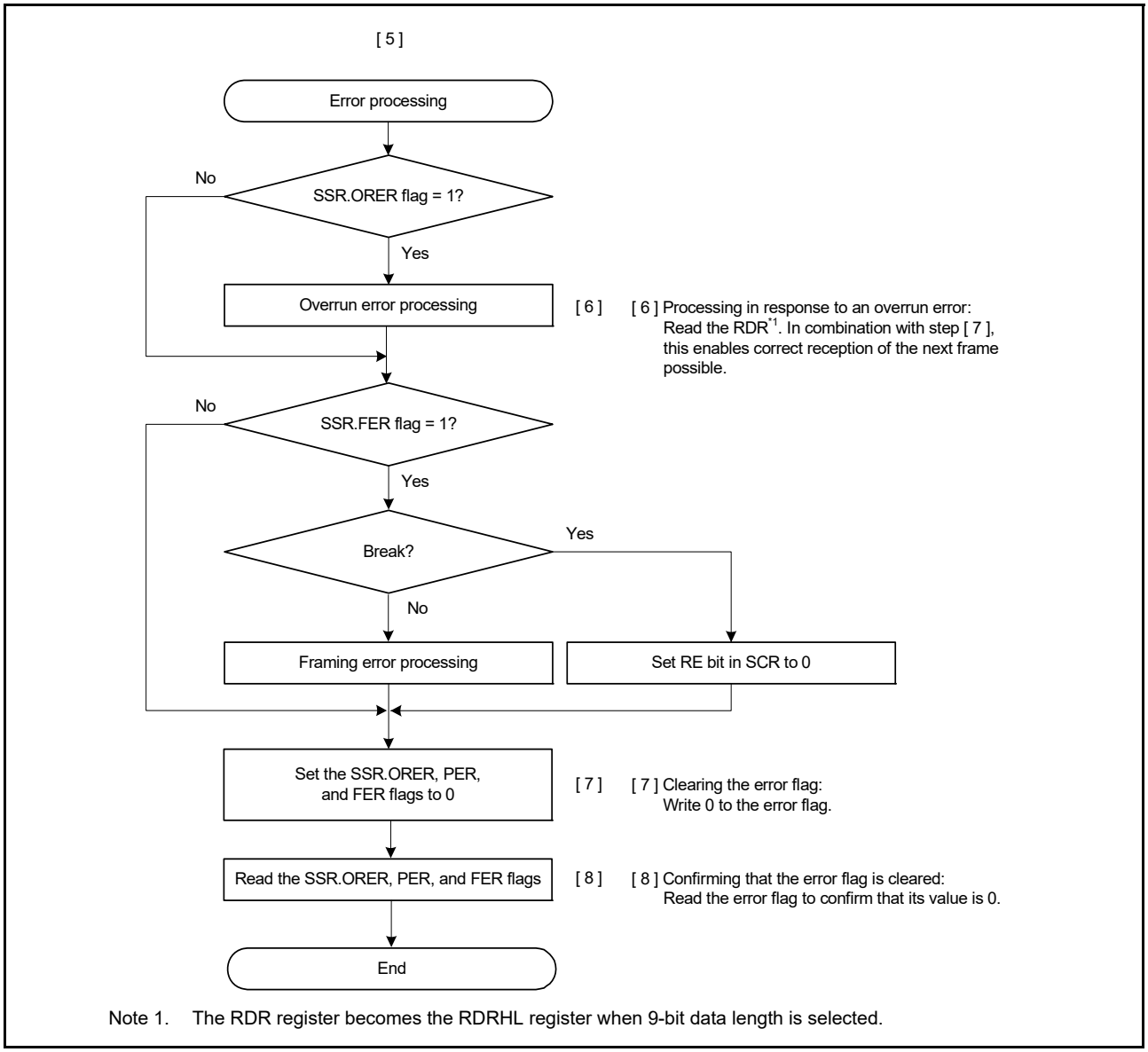


Figure 27.28 Example flow of multi-processor serial reception with non-FIFO selected (2)

(2) FIFO selected

Figure 27.29 shows an example of a data format that is written to FRDRH and FRDRL in multi-processor mode.

In multi-processor mode, the MPB value that is a part of the receive data is written to the FRDRH.MPB flag. A value of 0 is written to the FRDRH.PER flag. Data is written to FRDRH and FRDRL with the correct data length. Unused bits are written with 0.

Read in the order from FRDRH to FRDRL. When software reads the FRDRL register, the SCI updates FER, MPB, and receive data (RDAT[8:0]) in FRDRL with the next data. The RDF, ORER and DR flags in FRDRH always reflect the associated flags in the SSR_FIFO register.

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	0	DR	MPB	9-bit receive data								

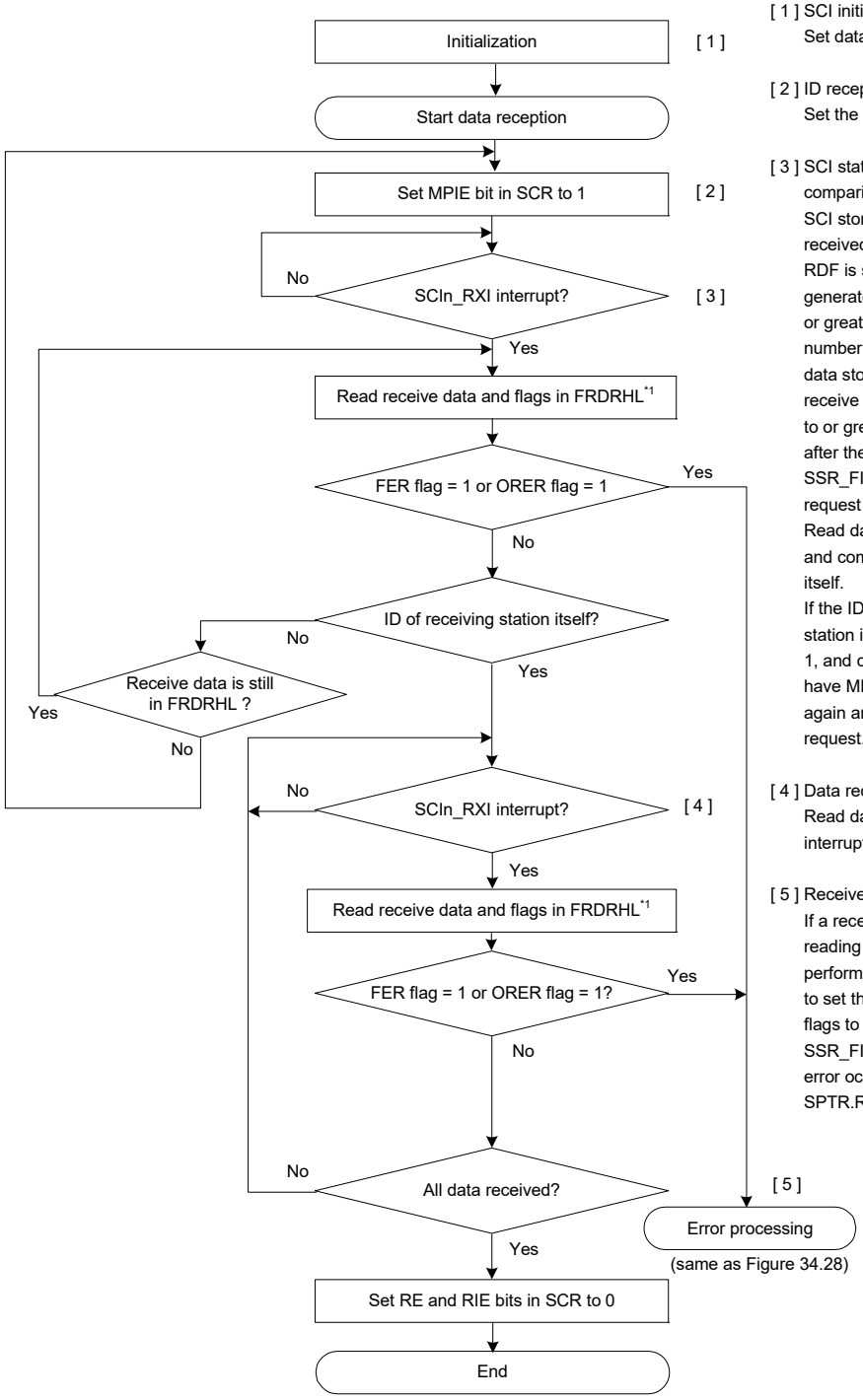
Note: When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7].
When data length is 8 bits, 0 is always read for FRDRH[0].
FRDRH[7] bit is read as an indefinite value.

Figure 27.29 Data format stored to FRDRH and FRDRL in multi-processor mode with FIFO selected

Figure 27.30 shows an example flow for multi-processor data reception with FIFO selected.

When the SCR.MPIE is set to 1, reading communication data is skipped until the reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data, MPB and the associated errors are transferred to the FRDRHL register. The SCR.MPIE bit is automatically cleared and non-multi-processor reception continues.

If a frame error occurs and the SSR_FIFO.FER flag is set to 1, the SCI continues data reception. The rest of the operations are the same as in asynchronous mode with non-FIFO selected.



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set the SCR.MPIE bit to 1 and wait for ID reception.

[3] SCI status confirmation and reception and comparison of ID:
SCI stores first data (MPB = 1) and subsequent received data in FRDRHL.
RDF is set to 1 and an SCIn_RXI interrupt request is generated when the amount of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL. When the amount of data stored in FRDRHL falls below the specified receive triggering number and received data is equal to or greater than 1, and no new data is received after the elapse of 15 ETUs from the last stop bit, SSR_FIFO.DR is set to 1. An SCIn_RXI interrupt request is generated when FCR.DRES bit is 0.
Read data in FRDRHL at the first SCIn_RXI interrupt, and compare it with the ID of the receiving station itself.
If the ID does not match the ID of the receiving station itself, the SCI reads until the data with MPB = 1, and compares the next ID. If the data does not have MPB = 1 in FRDRHL, set the MPIE bit to 1 again and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in FRDRHL once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading the ORER and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the SSR_FIFO.ORER and SSR_FIFO.FER flags to 0. Reception cannot be resumed if the SSR_FIFO.ORER flag is set to 1. When a framing error occurs, a break can be detected by reading the SPTR.RXDMON bit.

Note 1. If FRDRH and FRDRL are used instead of FRDRHL, read in the order from FRDRH to FRDRL.

Figure 27.30 Example flow of serial reception in multi-processor mode with FIFO selected

27.5 Operation in Clock Synchronous Mode

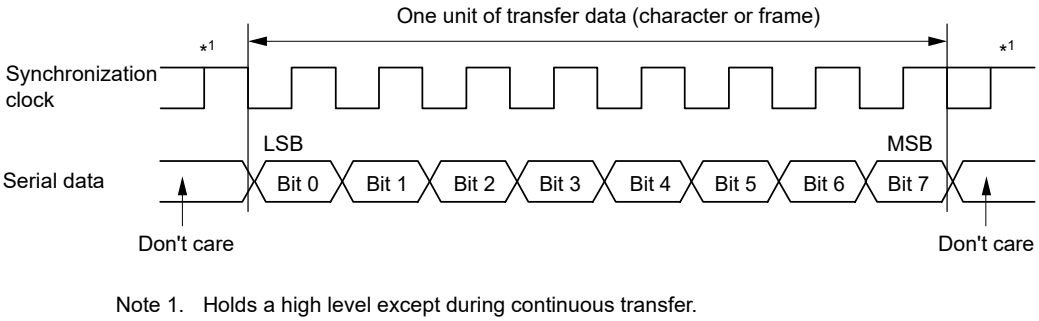
Figure 27.31 shows the data format for clock synchronous serial data communications.

In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. One character in transfer data consists of 8-bit data. In clock synchronous mode, no parity bit can be added.

In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the last bit as the output state. When the SPMR.CKPH bit is 1 in slave mode, the transmission line holds the first bit as the output state.

Within the SCI, the transmitter and receiver are independent units, enabling full-duplex communications by using a common clock. Both the transmitter and the receiver have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.

However, it is not possible to perform continuous transfer in the fastest bit rate setting (BRR[7:0] = 00h and SMR.CKS[1:0] = 00b). Therefore, when the FIFO is selected, this setting (BRR[7:0] = 00h and SMR.CKS[1:0] = 00b) is not available.



Note 1. Holds a high level except during continuous transfer.

Figure 27.31 Data format in clock synchronous serial communications with LSB-first

27.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCKn pin can be selected based on the SCR.CKE[1:0] setting.

When the SCI operates on an internal clock, the synchronization clock is output from the SCKn pin. Eight synchronization clock pulses are output in the transfer of one character. When no transfer is performed, the clock is held high. However, when only data reception is performed while the CTS function is disabled, the synchronization clock output starts when the SCR.RE bit is set to 1. The synchronization clock stops when it is held high*1 and when an overrun error occurs, or when the SCR.RE bit is set to 0.

When only data reception occurs and the CTS function is enabled, the clock output does not start when the SCR.RE bit is set to 1 and the CTSn_RTSn pin input is high. The synchronization clock output starts when the SCR.RE bit is set to 1 and the CTSn_RTSn pin input is low. When the CTSn_RTSn pin input is high on completion of the frame reception, the synchronization clock output stops when it goes high. If the CTSn_RTSn pin input continues to be low, the synchronization clock stops when it goes high*1 and when an overrun error occurs, or when the SCR.RE bit is set to 0.

Note 1. The signal is held high when SPMR.CKPH is 0 and SPMR.CKPOL is 0, or when SPMR.CKPH is 1 and SPMR.CKPOL is 1.
It is held low when SPMR.CKPH is 0 and SPMR.CKPOL is 1, or when SPMR.CKPH is 1 and SPMR.CKPOL is 0.

27.5.2 CTS and RTS Functions

In the CTS function, the CTSn_RTSn pin input controls the start of data reception or transmission when the clock source is the internal clock. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, setting the CTSn_RTSn pin low causes data reception or transmission to start.

Setting the CTSn_RTSn pin high while the data transmission or reception is in progress does not affect transmission or reception of the current frame.

In the RTS function, the CTSn_RTSn pin output is used to request the start of data reception or transmission when the clock source is an external synchronizing clock. The CTSn_RTSn output goes low when serial communication becomes possible. Conditions for output of CTSn_RTSn low and high are as follows:

[Conditions for low output]

(a) Non-FIFO selected when all of the following conditions are satisfied

- The value of the RE or TE bit in the SCR is 1
- When serial communication is enabled
- There is no received data available to be read when the SCR.RE bit is 1
- Transmit data is written when the SCR.TE bit is 1 and SCR.CKE[1] bit is 0
- Data is available for transmission in the TSR register when SCR.TE bit is 1 and SCR.CKE[1] bit is 1
- The ORER flag in SSR is 0.

(b) FIFO selected when all of the following conditions are satisfied

- The value of the RE or TE bit in SCR is 1
- When serial communication is enabled
- The amount of receive data written in FRDRHL is less than the specified CTSn_RTSn output triggering number when SCR.RE = 1
- Data that has not been transmitted is available in FTDRHL when the SCR.TE bit is 1 and the SCR.CKE[1] bit is 0
- Data is available for transmission in the TSR register when the SCR.TE bit is 1 and the SCR.CKE[1] bit is 1
- The ORER flag in SSR_FIFO is 0.

[Condition for high output]

(a) Non-FIFO selected

- The conditions for low output are not satisfied.
- When reception is terminated with SCR.RE = 0 without reading the RDR register after reception is complete, RTS remains high. At this time, read the SCR register for dummy values after writing 0 to SCR.RE.

(b) FIFO selected

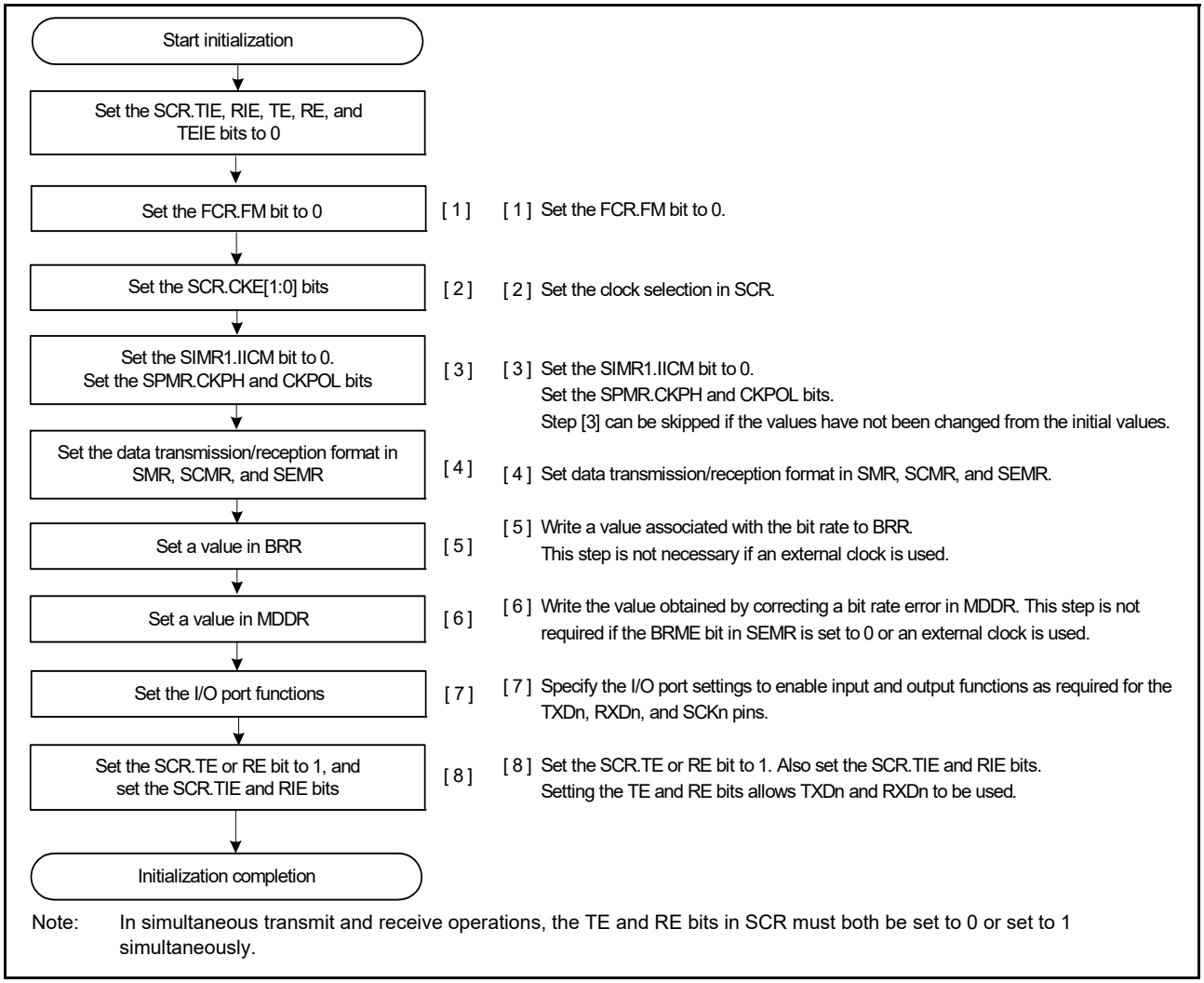
- The conditions for low output are not satisfied.

27.5.3 SCI Initialization in Clock Synchronous Mode

Before transmitting and receiving data, start by writing the initial value 00h to the SCR register, then continue through the SCI procedure in 27.5.2 CTS and RTS Functions. Any time the operating mode or transfer format is to be changed, the SCR register must be initialized before the change can be made.

Note: Setting the SCR.RE bit to 0 does not initialize the ORER, FER, RDRF, RDF, PER and DR flags in SSR/SSR_FIFO or the RDR and the RDRHL registers. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: Switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 when the SCR.TIE bit is 1 generates an SCIn_TXI interrupt request.



Note: In simultaneous transmit and receive operations, the TE and RE bits in SCR must both be set to 0 or set to 1 simultaneously.

Figure 27.32 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected

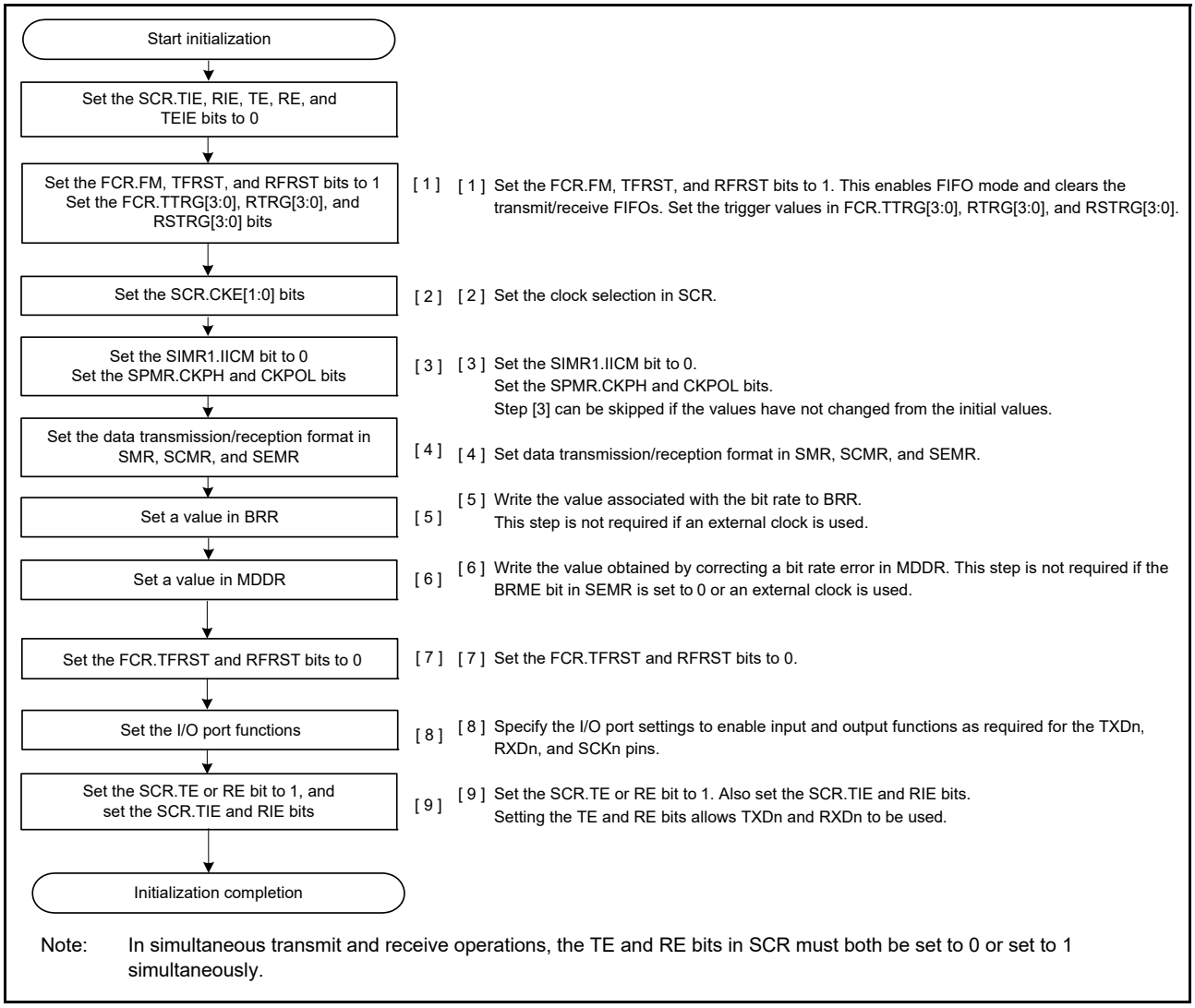


Figure 27.33 Example flow of SCI initialization in clock synchronous mode with FIFO selected

27.5.4 Serial Data Transmission in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 27.34, Figure 27.35, and Figure 27.36 show examples of serial transmission in clock synchronous mode.

In serial data transmission, the SCI operates as follows:

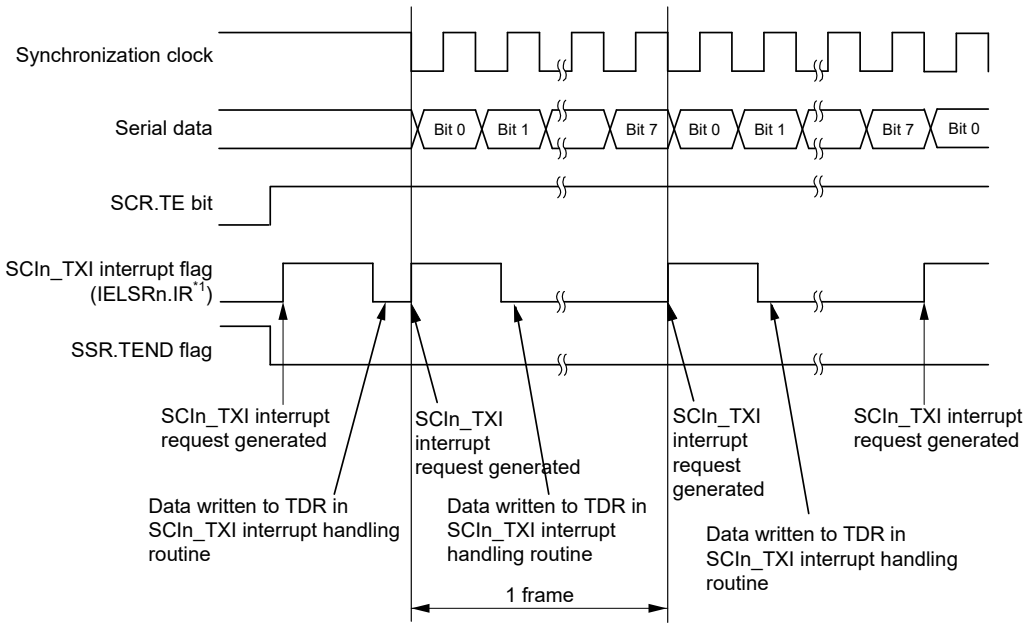
1. The SCI transfers data from the TDR register to the TSR register when data is written to TDR in the SCIn_TXI interrupt handling routine. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE bit is set to 1, but only after the SCR.TIE bit is also set to 1, or when SCR.TE and SCR.TIE are both set to 1 simultaneously by a single instruction.
2. After transferring data from TDR to TSR, the SCI starts transmission. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to TDR in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR register from the handling routine for SCIn_TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified, and in synchronization with the input clock, when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low and while the SPMR.CTSE bit is 1.
4. The SCI checks for updates to the TDR register on the output of the last bit.

5. When the TDR register is updated, the next transmit data is transferred from TDR to TSR, and serial transmission of the next frame starts.
6. If TDR is not updated, the SSR.TEND flag is set to 1. The TXDn pin keeps the output state of the last bit. If the SCR.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Figure 27.34, Figure 27.35, and Figure 27.36 show example flows of serial data transmission.

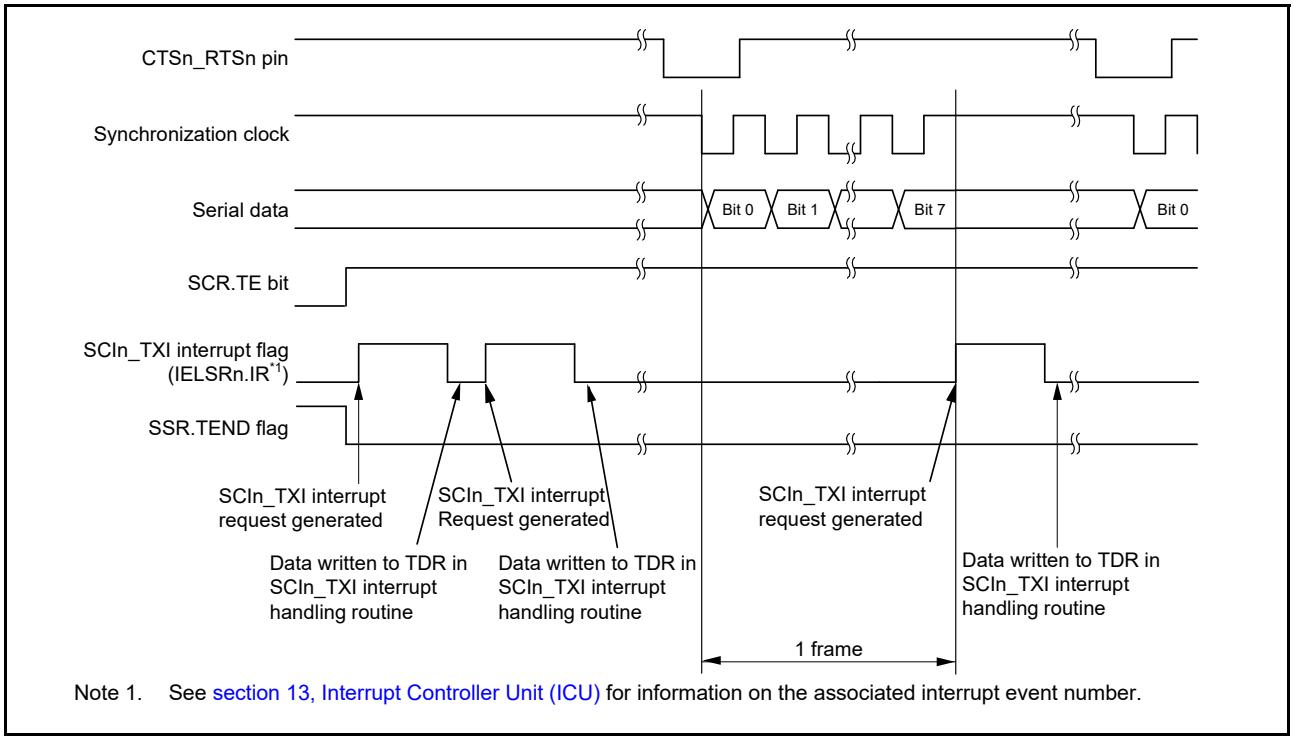
Transmission does not start while a receive error flag (ORER, FER, or PER in SSR) is set to 1. Be sure to set the receive error flags to 0 before starting transmission.

Note: Setting the SCR.RE bit to 0 does not clear the receive error flags.



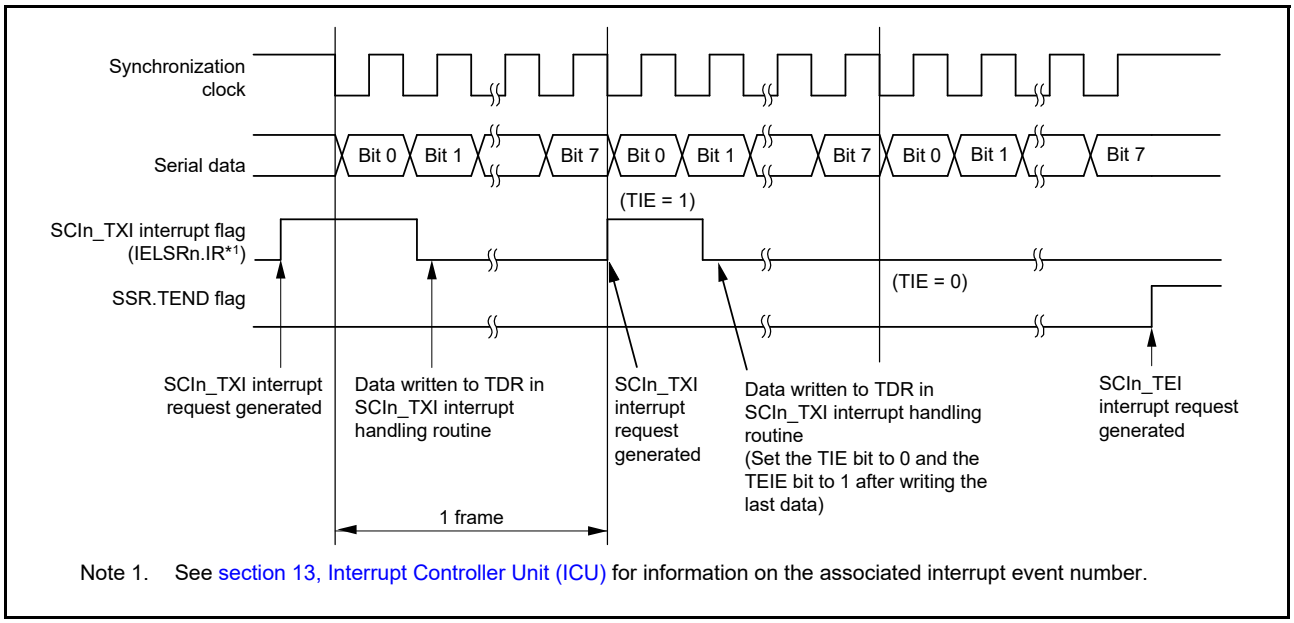
Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 27.34 Example of serial data transmission in clock synchronous mode when the CTS function is not used at the beginning of transmission



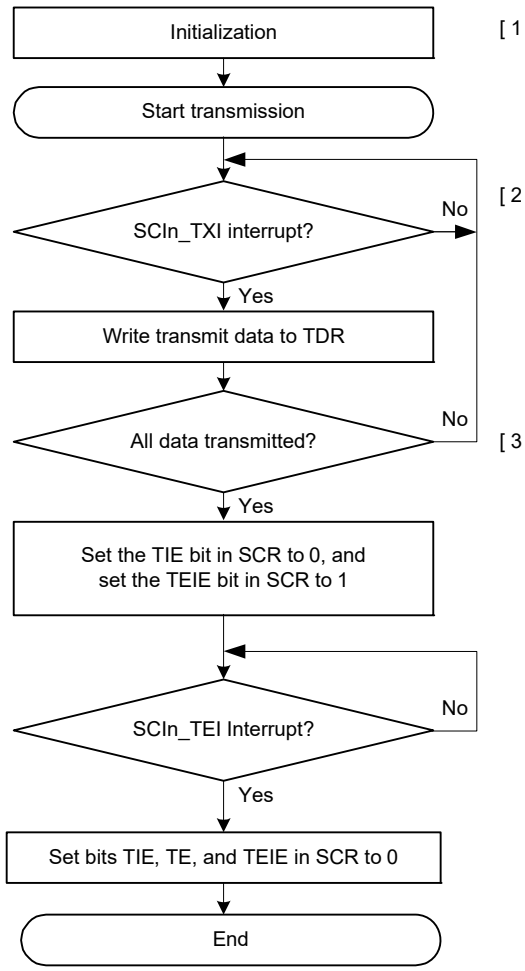
Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 27.35 Example of serial data transmission in clock synchronous mode when the CTS function is used at the beginning of transmission



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 27.36 Example of serial data transmission in clock synchronous mode from the middle of transmission until transmission completion



[1] [1] SCI initialization:
Set data transmission.

[2] [2] Write transmit data to TDR by an SCIn_TXI interrupt request:
When data transmission is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Transmit data is written to TDR once from the handling routine for SCIn_TXI requests.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR on accepting a transmit data empty interrupt (SCIn_TXI) request.
Transmit data can also be written to TDR by activating the DMAC or DTC by the SCIn_TXI interrupt request.
[3] When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to TDR.

Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCK pin for the last bit sets the SSR.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received data hold time on the receiver side.

Figure 27.37 Example flow of serial transmission in clock synchronous mode with non-FIFO selected

(2) FIFO selected

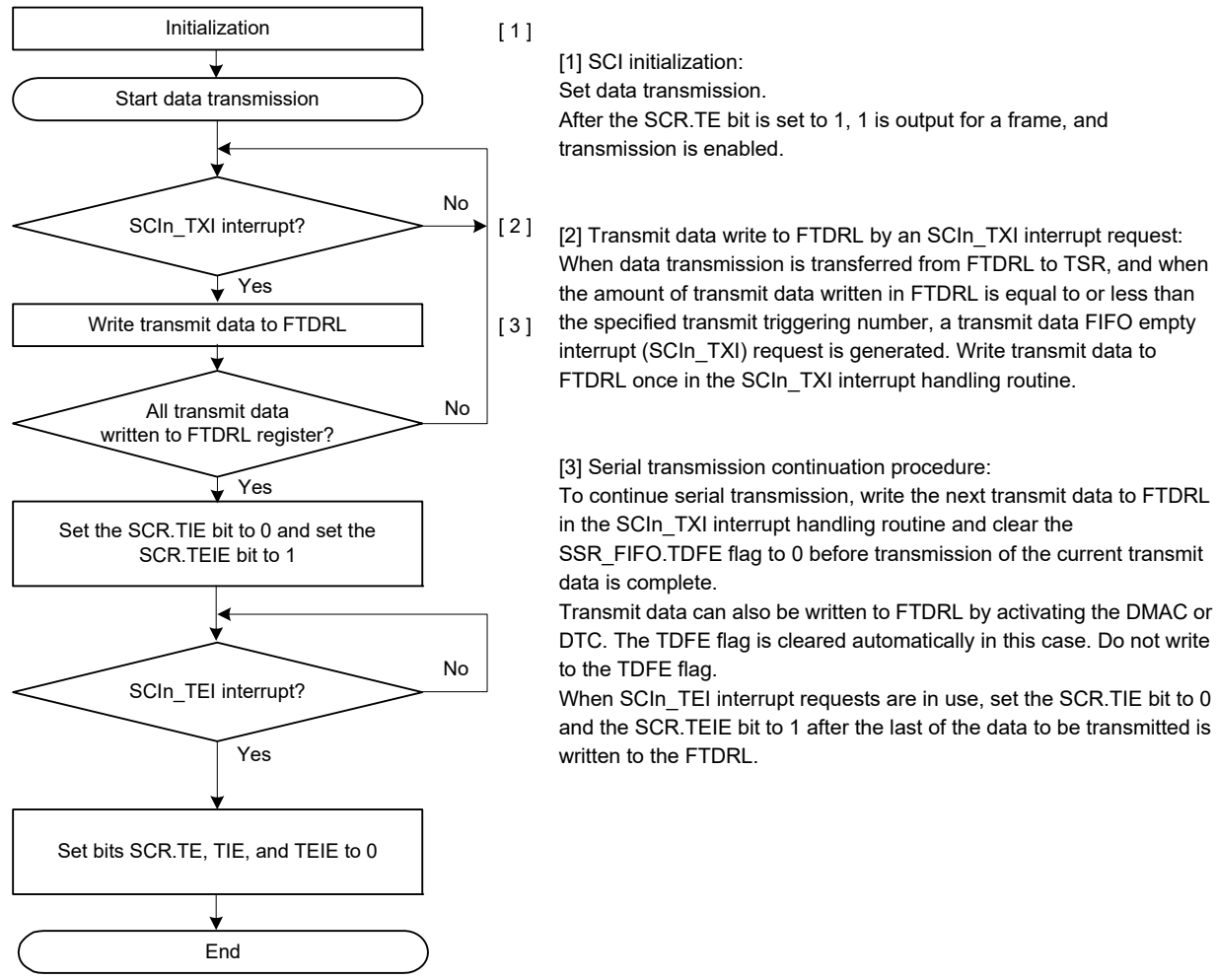
Figure 27.38 shows an example of serial transmission in clock synchronous mode with FIFO selected.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the FTDRL*1 register to the TSR register when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE bit is set to 1, but only after the SCR.TIE bit is also set to 1, or when SCR.TE and SCR.TIE are both set to 1 simultaneously by a single instruction.
2. After transferring data from FTDRL to TSR, the SCI starts transmission. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, the SSR_FIFO.TDFE is set to 1. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to FTDRL in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRL from the handling routine for SCIn_TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low and while the SPMR.CTSE bit is 1.

4. The SCI checks whether non-transmitted data remains in FTDRL on the output of the stop bit.
5. When FTDRL is updated, the next transmit data is transferred from FTDRL to TSR and serial transmission of the next frame starts.
6. If FTDRL is not updated, the SSR_FIFO.TEND flag is set to 1. The TXDn pin keeps the output state of the last bit. If the SCR.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Note 1. In clock synchronous mode, FTDRH is not used.



Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCK pin for the last bit sets the SSR_FIFO.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient hold time for received data on the receiver side.

Figure 27.38 Example flow of serial transmission in clock synchronous mode with FIFO selected

27.5.5 Serial Data Reception in Clock Synchronous Mode

(1) Non-FIFO selected

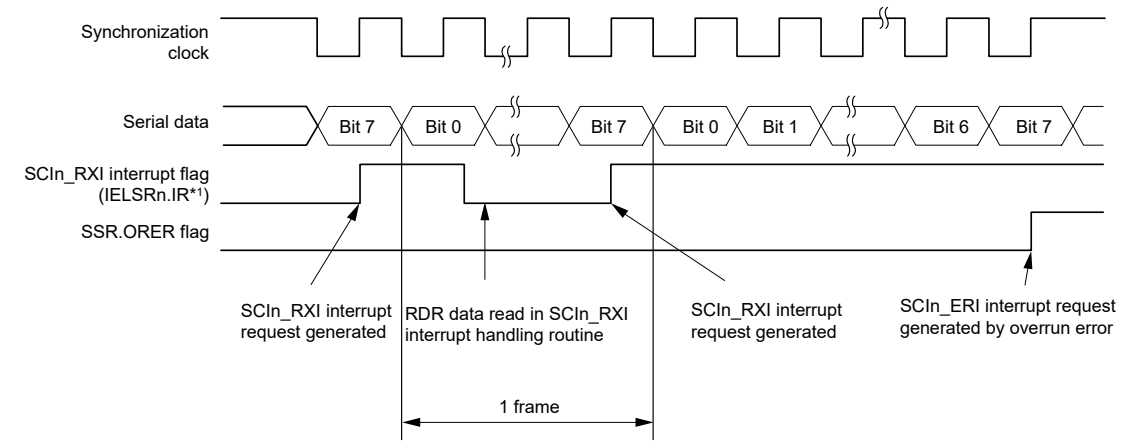
Figure 27.39 and Figure 27.40 show examples of SCI operation for serial reception in clock synchronous mode.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.
3. If an overrun error occurs, the SSR.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is

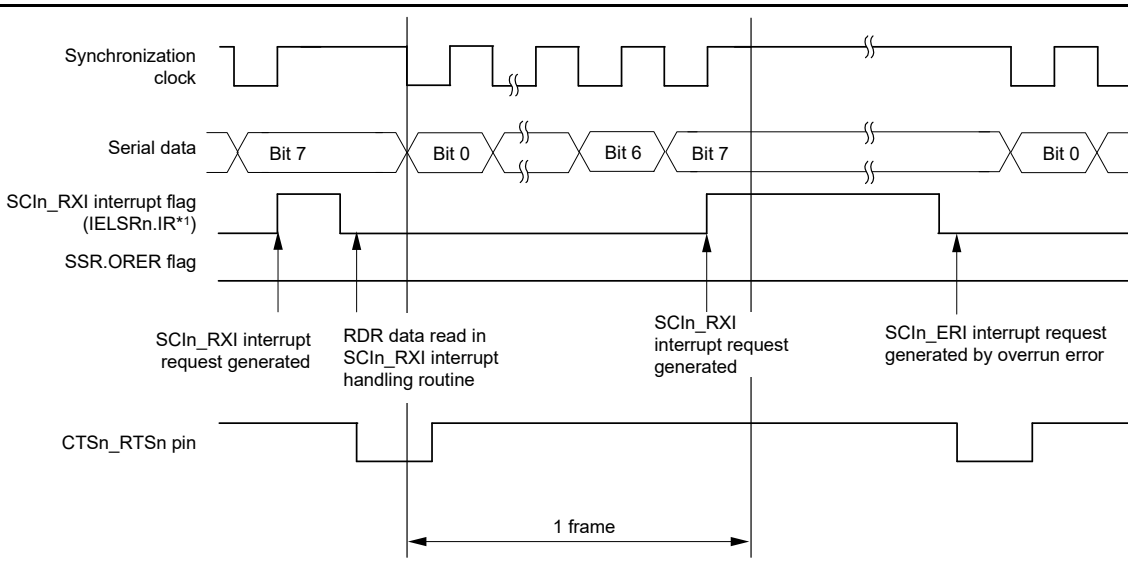
generated. Receive data is not transferred to the RDR register.

4. When reception completes successfully, receive data is transferred to the RDR register. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the received data transferred to the RDR register in the SCIn_RXI interrupt handling routine before the reception of the next receive data completes. Reading the received data from RDR causes the CTSn_RTSn pin to output low.



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 27.39 Example operation of serial reception in clock synchronous mode (1) when the RTS function is not used

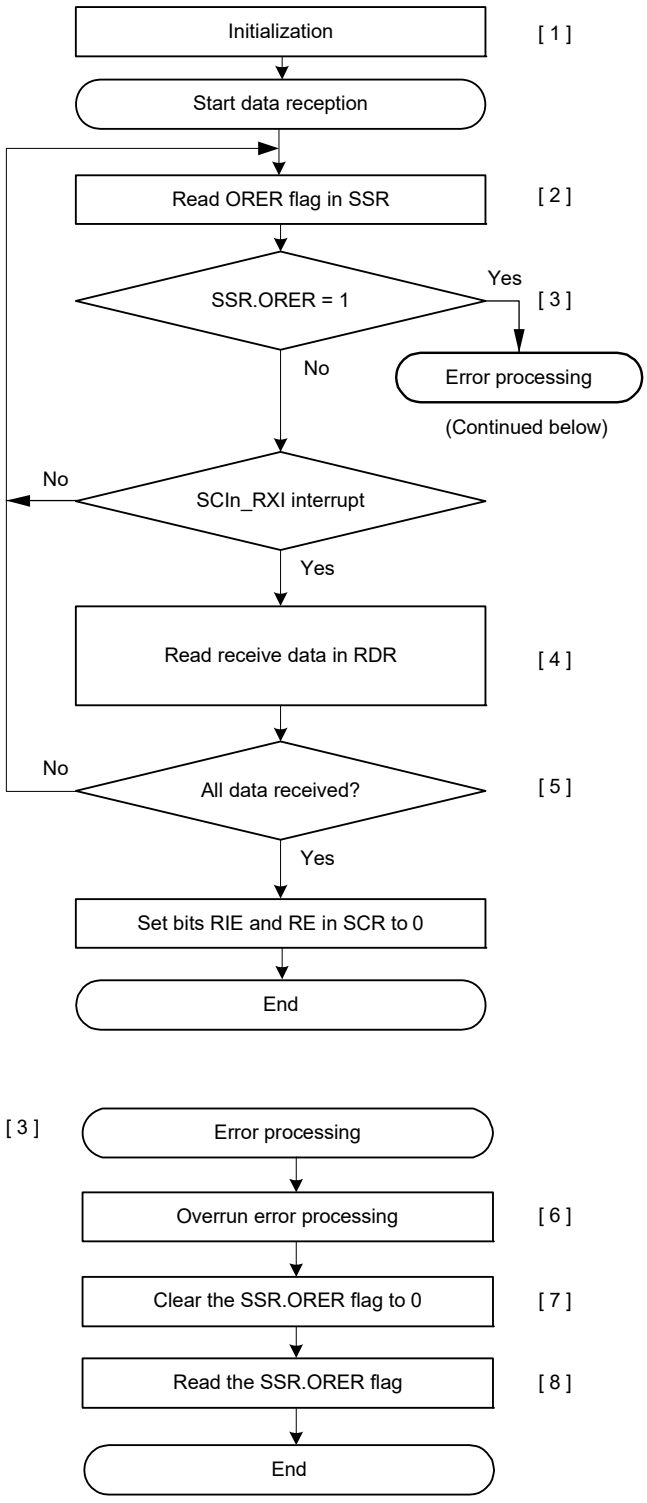


Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 27.40 Example operation of serial reception in clock synchronous mode (2) when RTS function is used

Data transfer cannot resume while the receive error flag is 1. Therefore, clear the ORER, FER, and PER flags in the SSR register to 0 before resuming data reception. Additionally, be sure to read the RDR register during overrun error processing. When a data reception is forcibly terminated by setting the SCR.RE bit to 0 during operation, read the RDR register because received data that is not yet read might be left in the RDR register.

Figure 27.41 shows an example flow of serial data reception.



[1] SCI initialization:
Set the input port for pins to be used as RXDn pins.

[2] [3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, perform the relevant error processing, then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Read the receive data in RDR once in the receive data full interrupt (SCIn_RXI) request handling routine.

[5] Serial reception continuation procedure:
To continue serial reception, before the MSB bit [7] of the current frame is received, finish reading the receive data in RDR. The RDR data can also be read by activating the DMAC or DTC by an SCIn_RXI interrupt request.

[6] Processing in response to an overrun error:
Read the RDR. In combination with step [7], this enables correct reception of the next frame possible.

[7] Clearing the error flag:
Write 0 to the error flag.

[8] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Figure 27.41 Example flow of serial reception in clock synchronous mode with non-FIFO selected

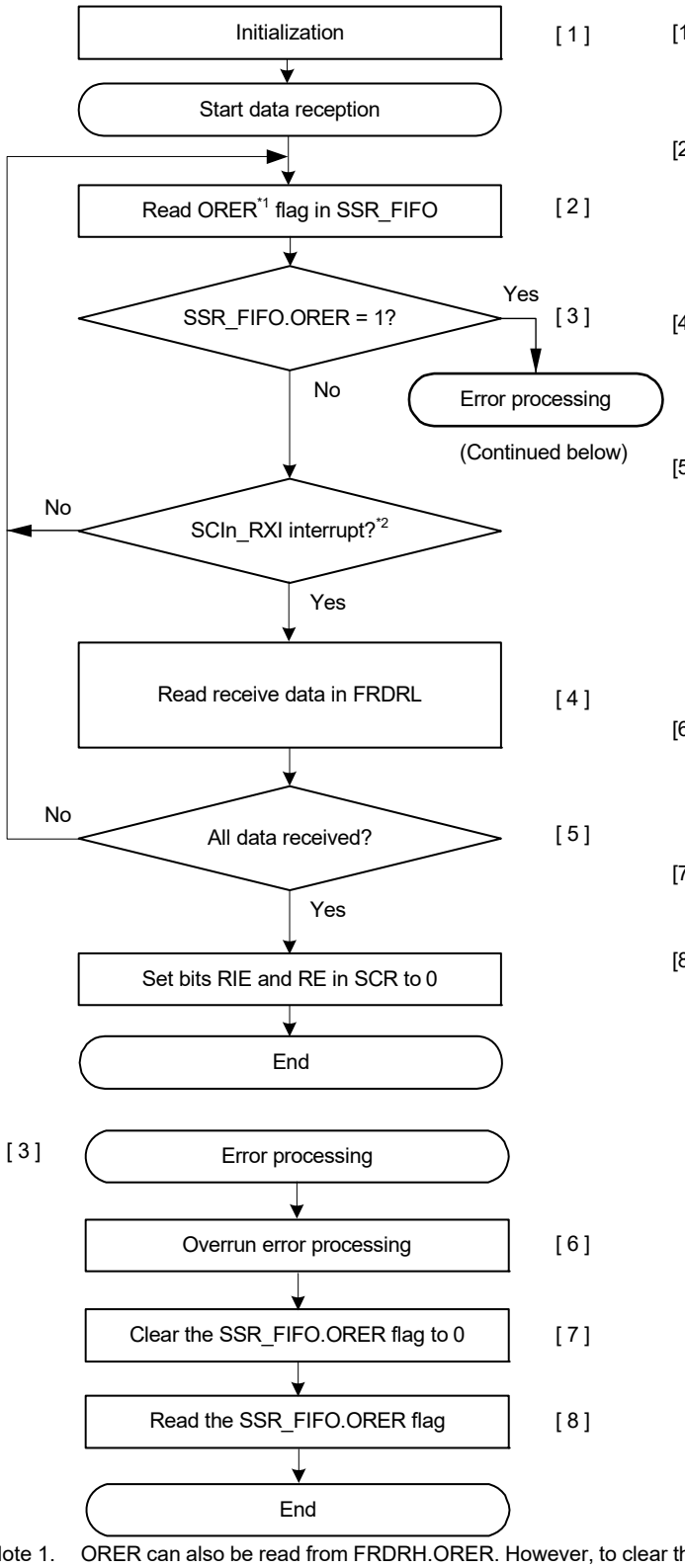
(2) FIFO selected

Figure 27.42 shows an example of serial reception in clock synchronous mode with FIFO selected.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in RSR.
3. If an overrun error occurs, the ORER flag in SSR_FIFO is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the FRDRL*1 register.
4. When data reception completes successfully, the receive data is transferred to the FRDRL*1 register. The RDF bit is set to 1 when the amount of the receive data stored in FRDRL is equal to or greater than the specified receive triggering number. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous data reception is enabled by reading the receive data transferred to FRDRL*2 in the SCIn_RXI interrupt handling routine before an overrun error occurs. If the amount of received data that is transferred to FRDRL is less than the RTS trigger number, the CTSn_RTSn pin goes low.

Note 1. In clock synchronous mode, FRDRH is not used.
Note 2. Read data in the order from FRDRH to FRDRL when RDF and ORER are read with receive data.



[1] SCI initialization:
Set the input port for pins to be used as RXDn pins.

[2] [3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, perform the relevant error processing, then set the SSR_FIFO.ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] The receive data stored in FRDRL register is read until the amount of stored data is less than the FCR.RTRG[3:0] value. Software can check readable data in FDR.R[4:0].

[5] Serial reception continuation procedure:
To continue serial reception before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0.The FRDRL data can also be read by activating the DMAC or DTC by an SCIn_RXI interrupt request. The RDF flag is cleared automatically in this case. Do not write to the RDF flag.

[6] Processing in response to an overrun error:
Read the FRDRL. In combination with step [7], this enables correct reception of the next frame possible.

[7] Clearing the error flag:
Write 0 to the error flag.

[8] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Note 1. ORER can also be read from FRDRH.ORER. However, to clear the ORER flag, write 0 to the associated bit in the SSR_FIFO register.
Note 2. All receive data is an integer multiple of the FIFO triggering number.

Figure 27.42 Example flow of serial reception in clock synchronous mode with FIFO selected

27.5.6 Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode

(1) Non-FIFO selected

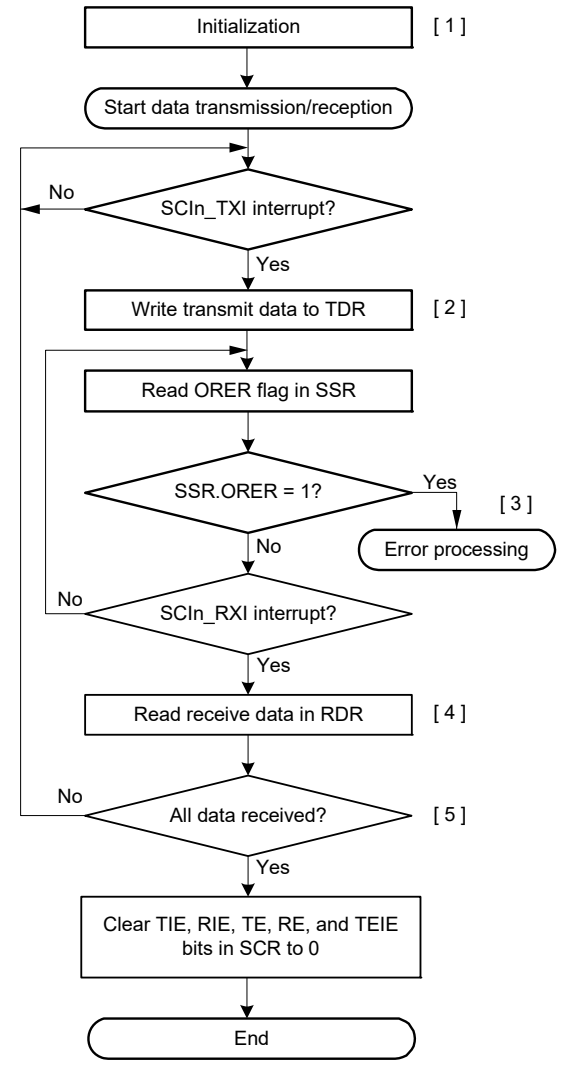
Figure 27.43 shows an example flow of simultaneous serial transmission and reception operations in clock synchronous mode. After initializing the SCI, use the following procedure for simultaneous serial data transmission and reception operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data transmission by verifying that the SSR.TEND flag is set to 1.
2. Initialize the SCR register and then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously with a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data reception.
2. Set the RIE and RE bits in the SCR register to 0, then check that the receive error flag ORER in the SSR register is 0.
3. Set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously with a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to TDR once in the SCIn_TXI interrupt request handling routine.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, perform the relevant error processing, then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Reading receive data:
Read the receive data in RDR once in the SCIn_RXI interrupt request handling routine.

[5] Serial transmission/reception continuation procedure:
To continue serial transmission and reception, before the MSB bit [7] of the current frame is received, finish reading the receive data in RDR by the SCIn_RXI interrupt. Also, before the MSB bit [7] of the current frame is transmitted, write data to TDR by the SCIn_TXI interrupt.
Transmit data can also be written to TDR by activating the DMAC or DTC by a transmit data empty interrupt (SCIn_TXI) request. Similarly, the RDR data can also be read by activating the DTC by a receive data full interrupt (SCIn_RXI) request.

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first set the TIE, RIE, TE, RE, and TEIE bits in SCR to 0, then set the TIE, RIE, TE, and RE bits to 1 simultaneously.

Figure 27.43 Example flow of simultaneous serial transmission and reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 27.44 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with FIFO selected.

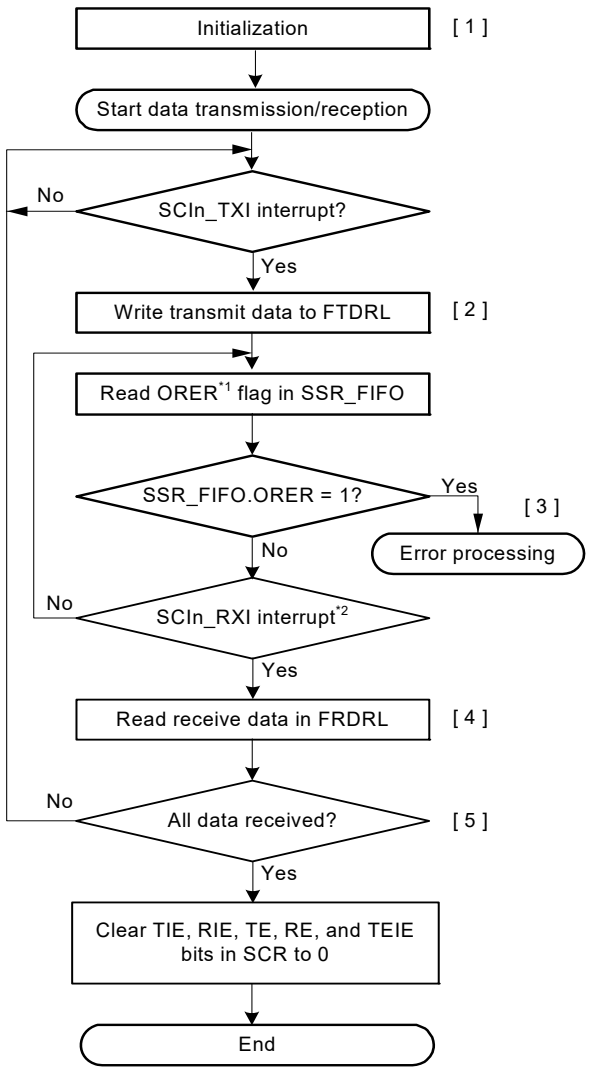
After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the transmission by verifying that the TEND flag in SSR_FIFO is set to 1.
2. Initialize the SCR register, then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously with a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the reception.
2. Set the RIE and RE bits to 0, then check that the receive error flag ORER in SSR_FIFO is 0.
3. Set the TIE, RIE, TE, and RE bits in SCR register to 1 simultaneously with a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to FTDRL in the SCIn_TXI interrupt request handling routine. The amount of transmit data that can be written is 16 bits, which is the number of stored transmit data in the FIFO.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, perform the relevant error processing, and then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Reading receive data:
The receive data stored in FRDRL register is read until the number of stored data is less than the FCR.RTRG value. Software can check readable data in FDR.R[4:0].

[5] Serial transmission/reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0. To continue serial transmission, before transmission of the current transmit data is finished, write the next transmit data to FTDRL in the SCIn_TXI interrupt handling routine and clear the SSR_FIFO.TDFE flag to 0.
Transmit data can also be written to FTDRL by activating the DMAC or DTC by a transmit FIFO data empty interrupt (SCIn_TXI) request. Similarly, the FRDRL data can also be read by activating the DMAC or DTC by a receive FIFO data full interrupt (SCIn_RXI) request. The RDF and TDFE flags are cleared automatically in this case.
Do not write to the RDF and TDFE flags.

Note 1. ORER can also read from FRDRH.ORER. To clear the ORER flag, write 0 to SSR_FIFO.ORER.
Note 2. The total receive data amount must be an integral multiple of the FIFO triggering number.

Figure 27.44 Example flow of simultaneous serial transmission and reception in clock synchronous mode with FIFO selected

27.6 Operation in Smart Card Interface Mode

The SCI supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards), as an extended function of the SCI.

Smart card interface mode can be selected using the appropriate register.

27.6.1 Example Connection

Figure 27.45 shows an example connection between a smart card (IC card) and the MCU.

Because the MCU communicates with an IC card using a single transmission line, interconnect the TXDn and RXDn pins and pull up the data transmission line to VCC using a resistor, as shown in Figure 27.45.

Setting the TE and RE bits in the SCR_SMCI register to 1 with an IC card disconnected enables closed-loop transmission or reception, allowing self-diagnosis. To supply an IC card with the clock pulses generated by the SCI, input the SCKn pin output to the CLK pin of an IC card. The output port of the MCU can be used to output a reset signal.

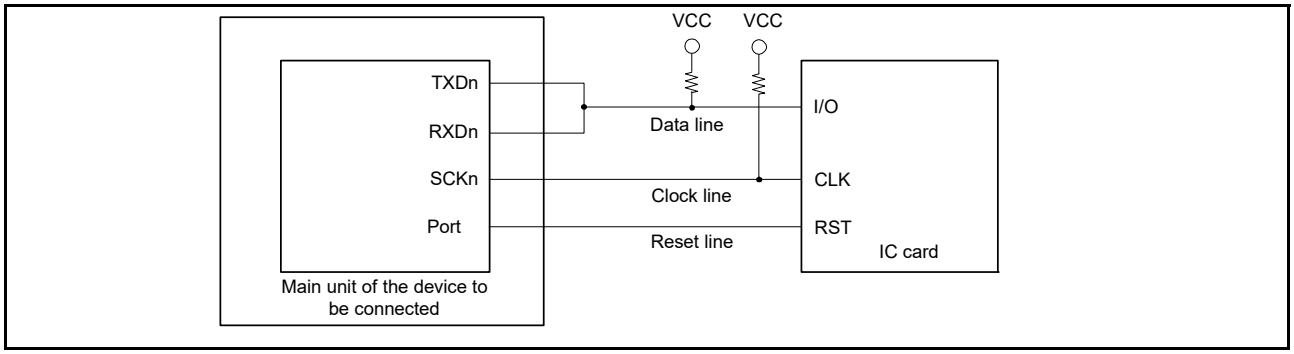


Figure 27.45 Example connection with a smart card (IC card)

27.6.2 Data Format (Except in Block Transfer Mode)

Figure 27.46 shows the data transfer formats in smart card interface mode.

The data transfer format is as follows:

- One frame consists of 8-bit data and a parity bit in asynchronous mode
- During transmission, a value of at least 2 ETUs (elementary time unit, which is the time required to transfer 1 bit) is set as a guard time from the end of the parity bit until the start of the next frame
- If a parity error is detected during reception, a low error signal is output for 1 ETU after 10.5 ETUs elapse from the start bit
- If an error signal is sampled during transmission, the same data is automatically retransmitted after at least 2 ETUs.

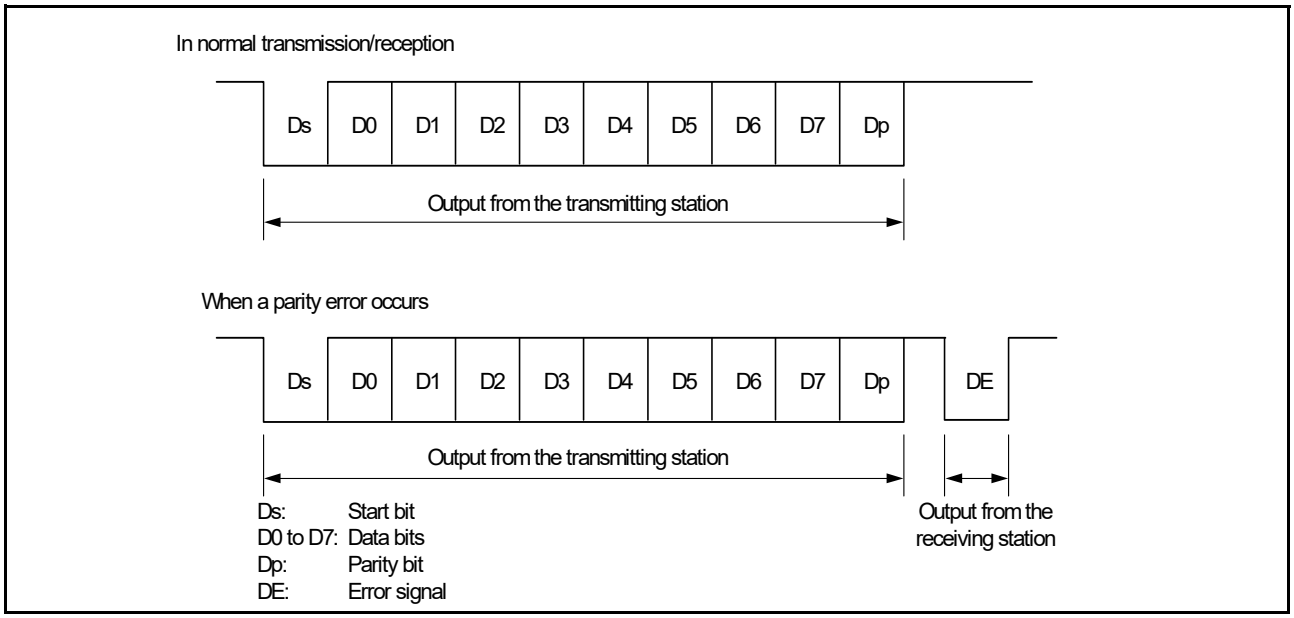


Figure 27.46 Data formats in smart card interface mode

For communication with IC cards of the direct convention type and inverse convention type, follow the procedures in this section.

(1) Direct convention type

For the direct convention type, logic levels 1 and 0 correspond to the Z and A states, respectively, and data is transferred with LSB-first for the start character, as shown in Figure 27.47. Therefore, data in the start character in Figure 27.47 is 3Bh.

When using the direct convention type, write 0 to both the SDIR and SINV bits in SCMR. Write 0 to the PM bit in SMR_SMCI to use even parity, which is recommended by the smart card standard.

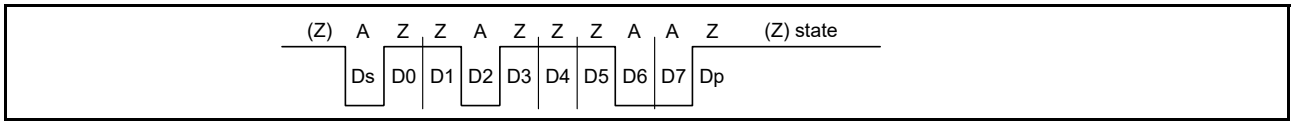


Figure 27.47 Direct convention with SDIR in SCMR = 0, SINV in SCMR = 0, and PM in SMR_SMCI = 0

(2) Inverse convention type

For the inverse convention type, logic levels 1 and 0 indicate the A and Z states respectively, and data is transferred with MSB-first as the start character, as shown in Figure 27.48. Therefore, data in the start character in Figure 27.48 is 3Fh.

When using the inverse convention type, write 1 to both the SCMR.SDIR and SCMR.SINV bits. The parity bit is at logic level 0 to produce even parity, which is required by the smart card standard, and corresponds to the Z state. Because the SINV bit only inverts data bits D7 to D0, write 1 to the PM bit in SMR_SMCI to invert the parity bit for both transmission and reception.

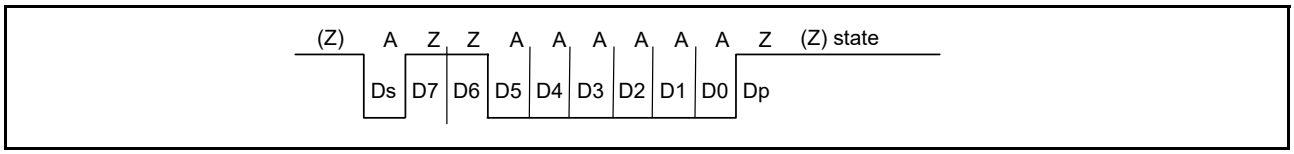


Figure 27.48 Inverse convention with SDIR in SCMR = 1, SINV in SCMR = 1, and PM in SMR_SMCI = 1

27.6.3 Block Transfer Mode

Block transfer mode differs from non-block transfer mode of the smart card interface mode as follows:

- If a parity error is detected during reception, no error signal is output. Because the PER flag in SSR_SMCI is set by error detection, clear the PER flag before receiving the parity bit of the next frame.
- During transmission, at least 1 ETU is set as a guard time from the end of the parity bit until the start of the next frame
- Because the same data is not retransmitted, the TEND flag in SSR_SMCI is set to 11.5 ETUs after transmission starts
- In block transfer mode, the ERS flag in SSR_SMCI indicates the error signal status as in non-block transfer mode of smart card interface mode, but the flag is read as 0 because no error signal is transferred.

27.6.4 Receive Data Sampling Timing and Reception Margin

Only the clock generated by the on-chip baud rate generator can be used as a transfer clock in smart card interface mode.

In this mode, the SCI can operate on a base clock with a frequency of 32, 64, 372, 256, 93, 128, 186, or 512 times the bit rate according to the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bit settings.

For data reception, the falling edge of the start bit is sampled with the base clock to perform synchronization.

Receive data is sampled on the 16th, 32nd, 186th, 128th, 46th, 64th, 93rd, and 256th rising edges of the base clock so that it can be latched at the middle of each bit as shown in Figure 27.49. The reception margin is determined by the following formula:

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F) \right| \times 100\ [\%]$$

M: Reception margin (%)

N: Ratio of bit rate to clock (N = 32, 64, 372, 256)

D: Duty cycle of clock (D = 0 to 1.0)

L: Frame length (L = 10)

F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5, and N = 372 in the specified formula, the reception margin is determined by the following formula:

M = {0.5 - 1/(2 × 372)} × 100 [%] = 49.866%

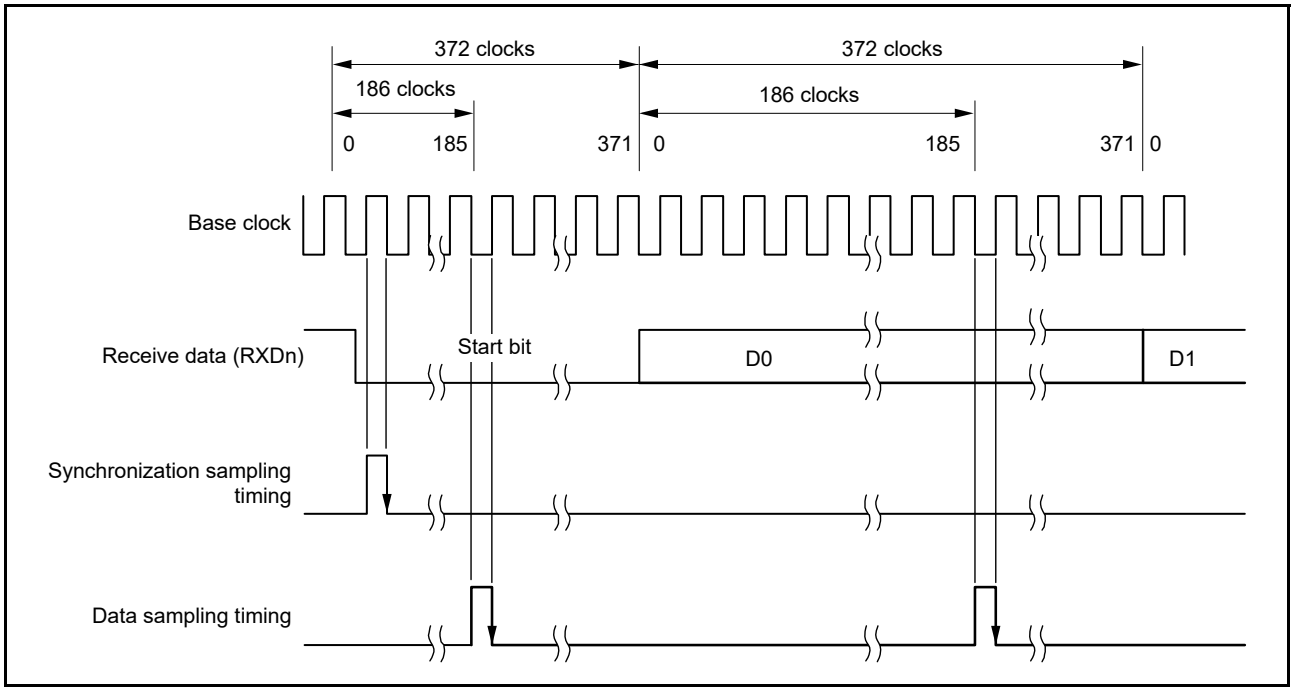


Figure 27.49 Receive data sampling timing in smart card interface mode when clock frequency is 372 times the bit rate

27.6.5 SCI Initialization

Before transmitting and receiving data, write the initial value 00h in the SCR_SMCI register and initialize the SCI using the example flow shown in Figure 27.50.

Be sure to set the initial value in the TIE, RIE, TE, RE, and TEIE bits in the SCR_SMCI register before switching from transmission to reception mode or from reception to transmission mode. When the SCR_SMCI.RE bit is set to 0, the RDR register is not initialized.

To change from reception mode to transmission mode, first check that the reception is complete, then initialize the SCI. At the end of initialization, set TE = 1 and RE = 0. Reception completion can be verified by reading the SCIn_RXI request, ORER, or PER flag in SSR_SMCI.

To change transmission mode to reception mode, first check that the transmission is complete, then initialize the SCI. At the end of the initialization, set TE = 0 and RE = 1. Transmission completion can be verified by reading the TEND flag in SSR_SMCI.

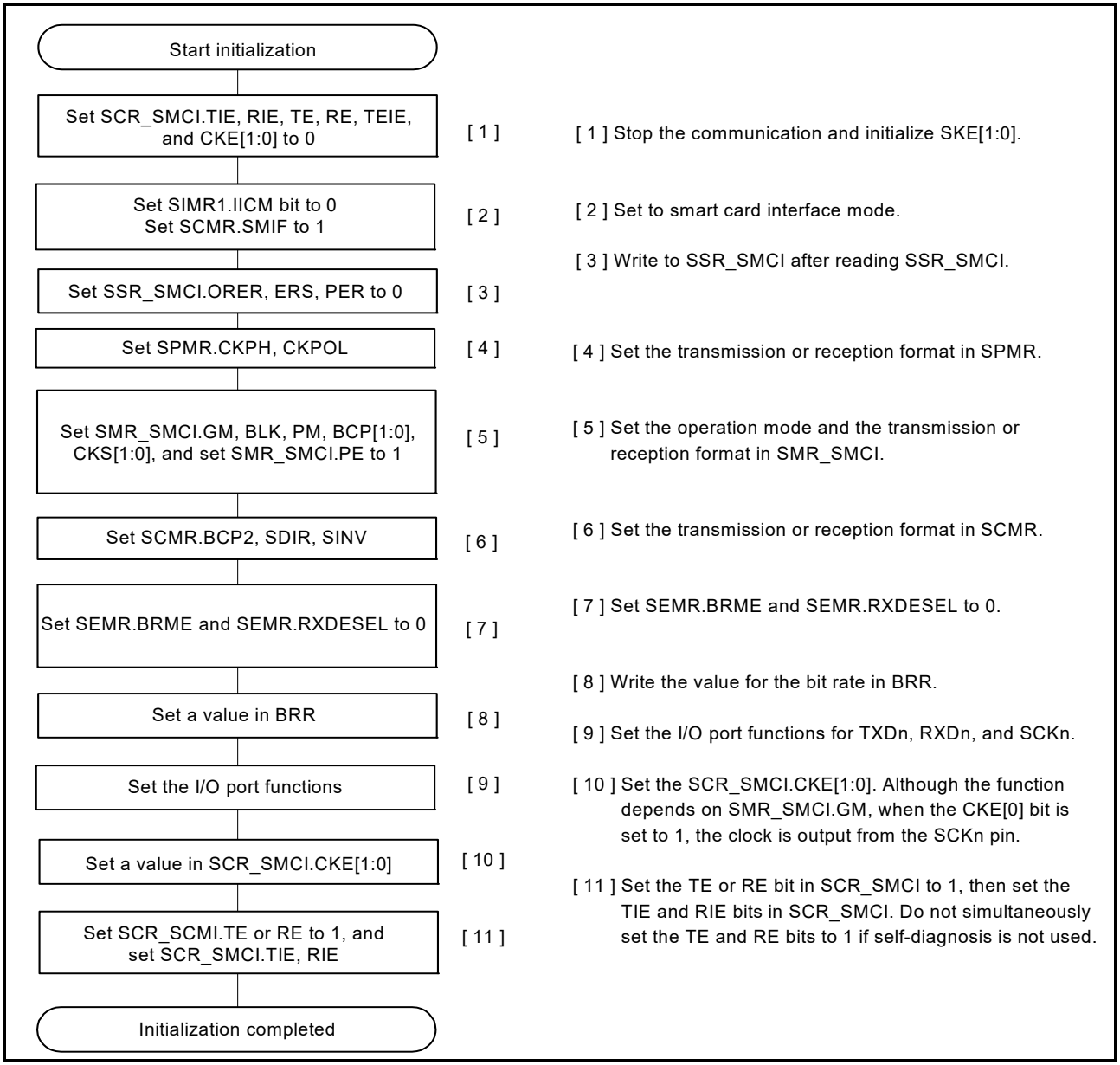


Figure 27.50 Example flow of SCI initialization in smart card interface mode

Figure 27.51 shows a timing diagram when data transmission is performed by transitioning to smart card interface mode according to the flow in Figure 27.50. Figure 27.51 shows when the GM bit in SMR_SMCI is set to 0. The timing in Figure 27.51 shows when the port is connected as SCKn and TXDn, the pins are Hi-Z because the CKE[0] bit in SCR_SMCI is 0.

Start the clock output to the SCK pin by setting the CKE[0] bit in SCR_SMCI to 1, then start data transmission by writing the transmit data after setting the TE bit in SCR_SMCI to 1. When the TE bit in SCR_SMCI changes from 0 to 1, there is a preamble period for one frame before data transmission starts. In smart card interface mode, the TXDn pin is Hi-Z when there is a preamble period. Pull-up or pull-down for the SCKn and TXDn pins is required outside the MCU.

In smart card interface mode, even when the TE and RE bits in SCR_SMCI are 0, the clock is continuously output if the clock output setting is used.

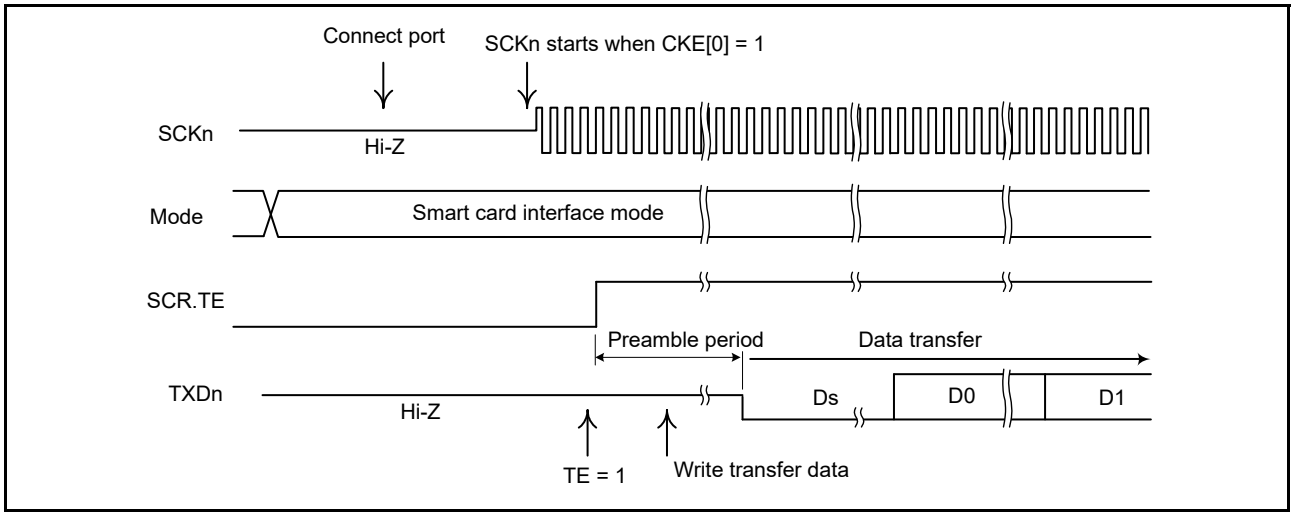


Figure 27.51 Example timing of data transmission in smart card interface mode

27.6.6 Serial Data Transmission (Except in Block Transfer Mode)

Serial data transmission in smart card interface mode (except in block transfer mode) is different from that in non-smart card interface mode, in that an error signal is sampled and data can be retransmitted in smart card mode. Figure 27.52 shows the data retransfer operation during transmission.

In Figure 27.52:

- [1] indicates when an error signal from the receiver end is sampled after 1-frame data is transmitted, the SSR_SMCI.ERS flag is set to 1. If the SCR_SMCI.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the ERS flag to 0 before the next parity bit is sampled.
- [2] indicates for a frame in which an error signal is received, the SSR_SMCI.TEND flag is not set. Data is retransferred from TDR to TSR, allowing automatic data retransmission.
- [3] indicates if no error signal is returned from the receiver, the ERS flag is not set to 1.
- [4] indicates the SCI determines that the transmission of 1-frame data, including the retransfer, is complete, and the TEND flag is set. If the SCR_SMCI.TIE bit is 1, an SCIn_TXI interrupt request is generated. Write transmit data to the TDR to start transmission of the next data.

Figure 27.54 shows an example flow of serial transmission. All the processing steps are automatically performed using an SCIn_TXI interrupt request to activate the DMAC or DTC.

When the SSR_SMCI.TEND flag is set to 1 in transmission and when the SCR_SMCI.TIE bit is 1, an SCIn_TXI interrupt request is generated.

The DMAC or DTC is activated by an SCIn_TXI interrupt request if the SCIn_TXI interrupt request is previously specified as a source of DMAC or DTC activation, allowing the transfer of transmit data. The TEND flag is automatically set to 0 when the DMAC or DTC transfers data.

If an error occurs, the SCI automatically retransmits the same data. During this retransmission, the TEND flag is kept at 0 and the DMAC or DTC is not activated. Therefore, the SCI and DMAC or DTC automatically transmit the specified number of bytes, including retransmission when an error occurs. Because the ERS flag is not automatically cleared, set the RIE bit to 1 to enable an SCIn_ERI interrupt request generation when an error occurs, and clear the ERS flag to 0.

When transmitting or receiving data using the DMAC or DTC, always enable the DMAC or DTC before setting the SCI.

For DMAC or DTC settings, see section 16, DMA Controller (DMAC) and section 17, Data Transfer Controller (DTC).

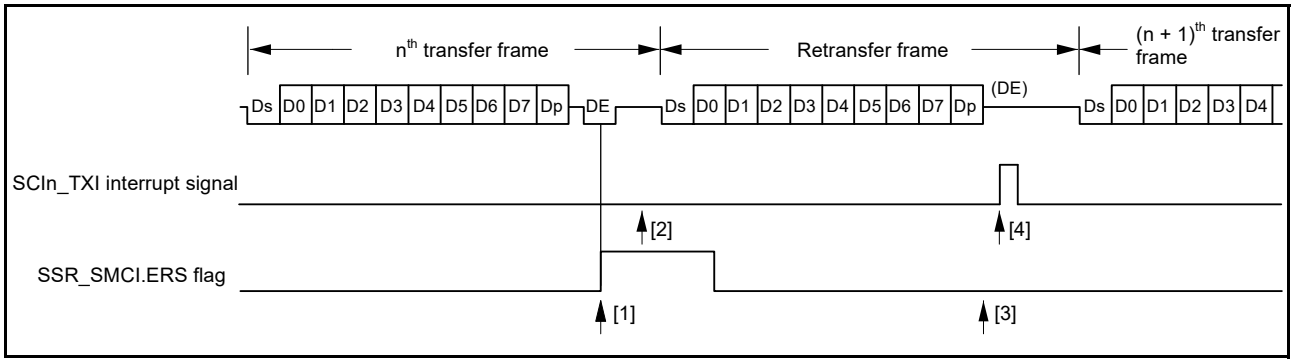


Figure 27.52 Data retransfer operation in SCI transmission mode

Note: The SSR_SMCI.TEND flag is set at different timings depending on the SMR_SMCI.GM bit setting.

Figure 27.53 shows the TEND flag generation timing.

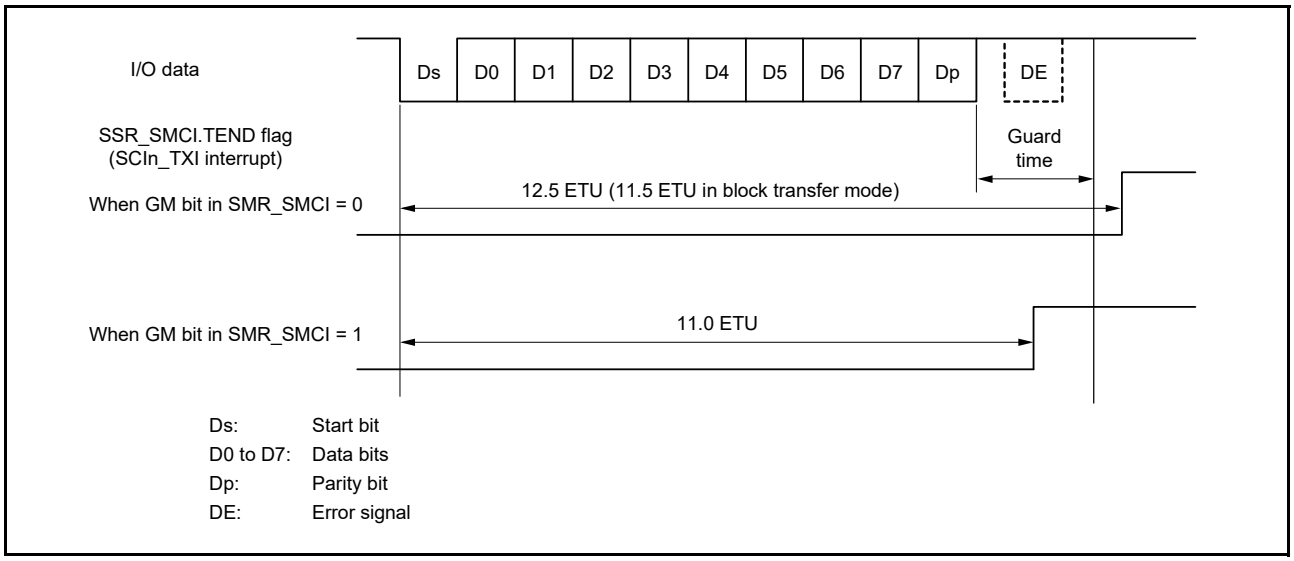


Figure 27.53 SSR.TEND flag generation timing during transmission

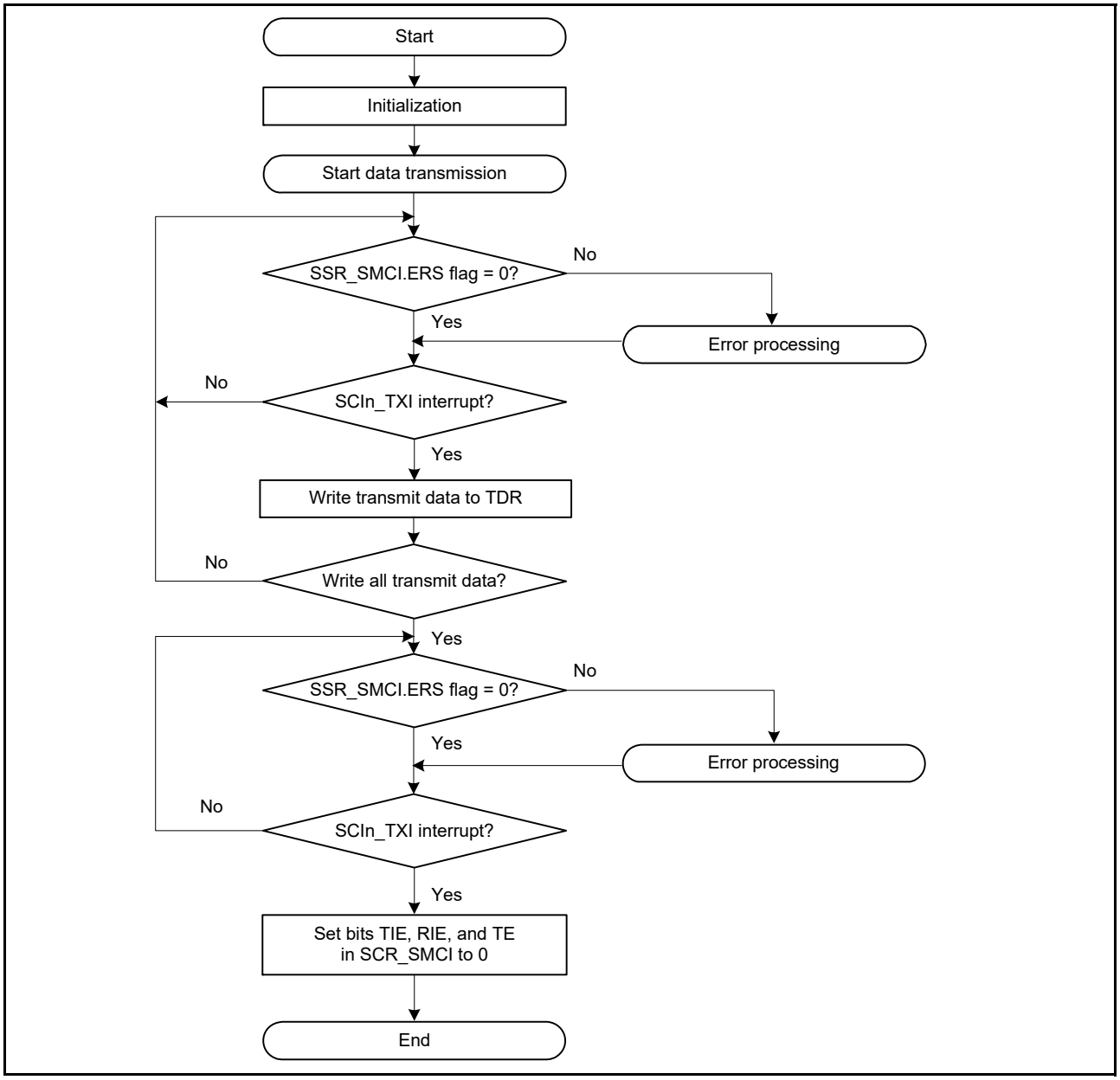


Figure 27.54 Example flow of smart card interface transmission

27.6.7 Serial Data Reception (Except in Block Transfer Mode)

Serial data reception in smart card interface mode is similar to that in non-smart card interface mode. Figure 27.55 shows the data retransfer operation in reception mode.

- [1] indicates if a parity error is detected in the receive data, the SSR_SMCI.PER flag is set to 1. When the SCR_SMCI.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the PER flag to 0 before the next parity bit is sampled.
- [2] indicates for a frame in which a parity error is detected, no SCIn_RXI interrupt is generated.
- [3] indicates when no parity error is detected, the SCR_SMCI.PER flag is not set to 1.
- [4] indicates the data is determined to be received successfully. When the SCR_SMCI.RIE bit is 1, an SCIn_RXI interrupt request is generated.

Figure 27.56 shows an example flow of serial data reception. All the processing steps are automatically performed using an SCIn_RXI interrupt request to activate the DMAC or DTC.

In reception, setting the RIE bit to 1 allows an SCIn_RXI interrupt request to be generated. The DMAC or DTC is activated by an SCIn_RXI interrupt request if the SCIn_RXI interrupt request is previously specified as a source of DMAC or DTC activation, allowing the transfer of receive data.

If an error occurs during reception and either the ORER or PER flag in SSR_SMCI is set to 1, a receive error interrupt (SCIn_ERI) request is generated. Clear the error flag after the error occurrence. If an error occurs, the DMAC or DTC is not activated and receive data is skipped. Therefore, the number of bytes of receive data specified in the DMAC or DTC is transferred.

If a parity error occurs and the PER flag is set to 1 during reception, the receive data is transferred to RDR, therefore allowing the data to be read.

When a reception is forced to terminate by setting SCR_SMCI.RE to 0 during operation, read the RDR register because the received data that is not yet read might be left in the RDR.

Note: For operations in block transfer mode, see section 27.3.9, Serial Data Reception in Asynchronous Mode.

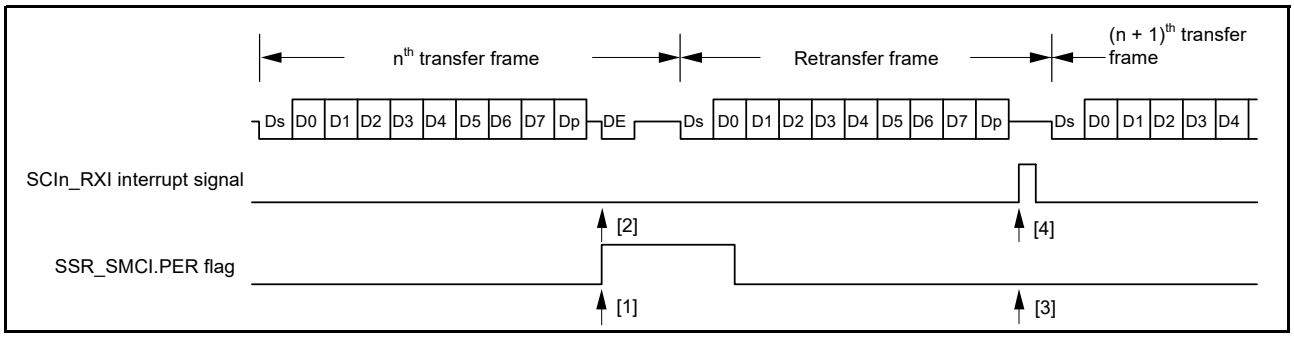


Figure 27.55 Data retransfer operation in SCI reception mode

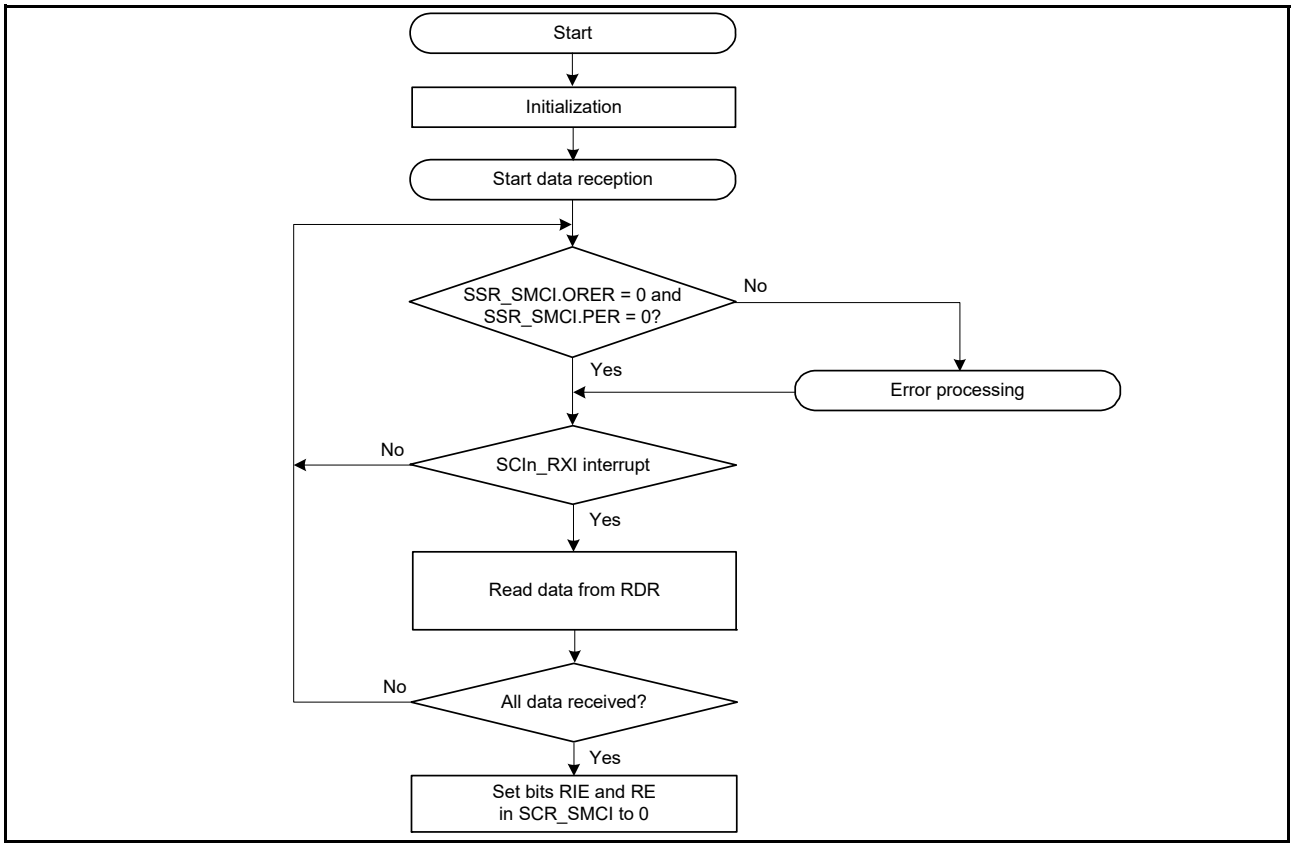


Figure 27.56 Example flow of smart card interface reception

27.6.8 Clock Output Control

When the GM bit in SMR_SMCI is set to 1, the clock output can be controlled by the CKE[1: 0] bits in SCR_SMCI. For details on the CKE[1:0] bits, see section 27.2.12, Serial Control Register for Smart Card Interface Mode (SCR_SMCI) (SCMR.SMIF = 1). When setting the clock output, the base clock described in section 27.6.4, Receive Data Sampling Timing and Reception Margin is output.

Figure 27.57 shows an example timing for the clock output control when the CKE[1] bit in SCR_SMCI is set to 0 and the CKE[0] bit in SCR_SMCI is controlled.

When the GM bit in SMR_SMCI is 0, output control by the CKE[0] bit in SCR_SMCI is immediately reflected in the SCK pin, so there is a possibility that pulses with an unintended width might be output from the SCK pin.

When the GM bit in SMR_SMCI is 1, the clock with the same pulse width as the base clock is output even if the CKE[0] bit in SCR_SMCI is changed.

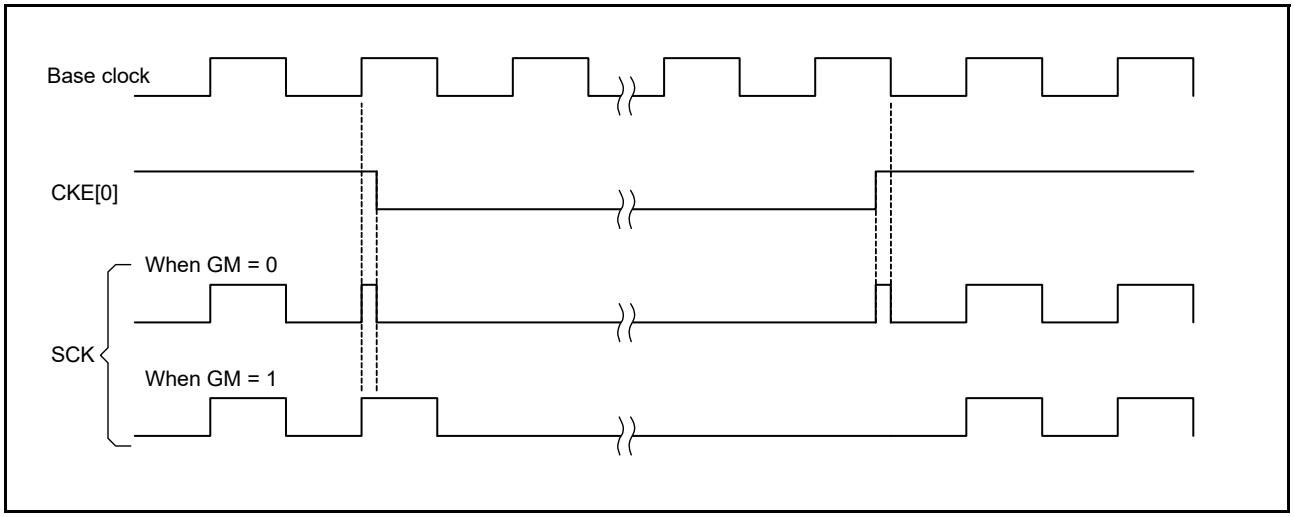


Figure 27.57 Clock output control

27.7 Operation in Simple IIC Mode

Simple I2C bus format is composed of 8 data bits and an acknowledge bit. By continuing into a slave-address frame after a start condition or restart condition, a master device can specify a slave device as a partner for communications. The currently specified slave device remains valid until a new slave device is specified or a stop condition is satisfied. The 8 data bits in all frames are transmitted in order from the MSB.

The I2C bus format and timing are shown in Figure 27.58 and Figure 27.59.

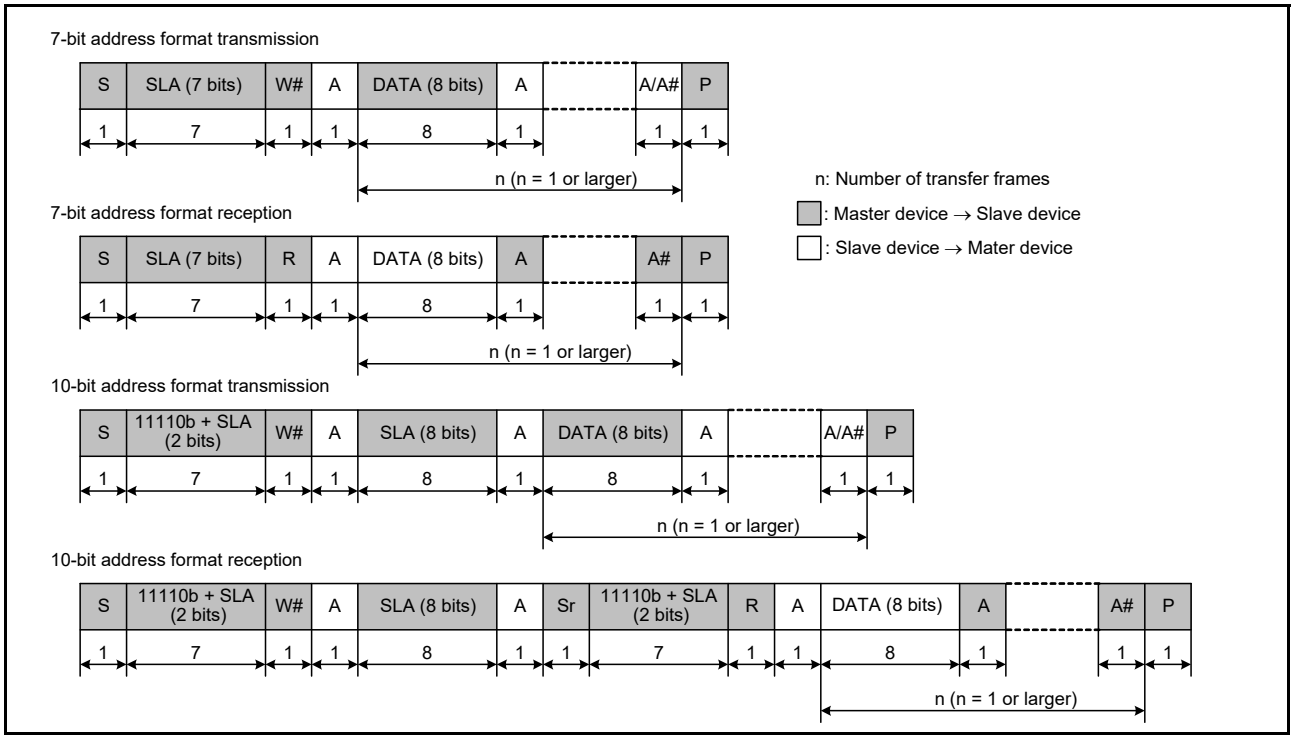


Figure 27.58 I²C bus format

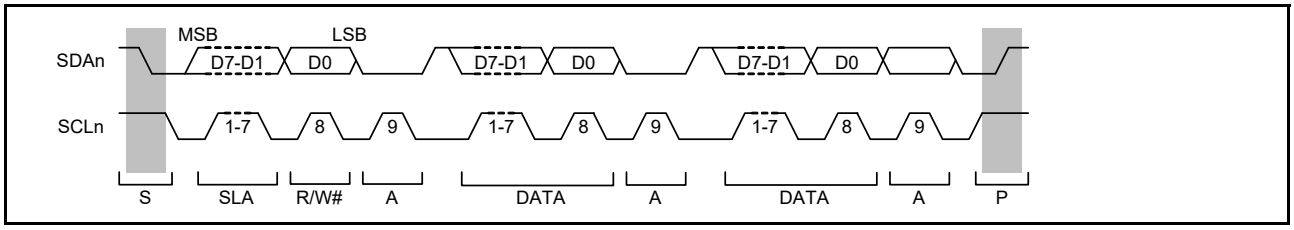


Figure 27.59 I²C bus timing when SLA is 7 bits

S: Indicates a start condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high.

SLA: Indicates a slave address, by which the master device selects a slave device.

R/W#: Indicates the direction of transfer (reception or transmission). The value 1 indicates transfer from the slave device to the master device and 0 indicates transfer from the master device to the slave device.

A/A#: Indicates an acknowledge bit. This is returned by the slave device for master transmission and by the master device for master reception. Return low indicates ACK and return high indicates NACK.

Sr: Indicates a restart condition when the master device changes the level on the SDAn line from high to low while the SCLn line is high and after the setup time elapses.

DATA: Indicates the data being received or transmitted.

P: Indicates a stop condition, when the master device changes the level on the SDAn line from low to high while the SCLn line is high.

27.7.1 Generation of Start, Restart, and Stop Conditions

Writing 1 to the SIMR3.IICSTAREQ bit causes the generation of a start condition. The generation of a start condition proceeds through the following operations:

- The level on the SDAn line falls (from high level to low level) and the SCLn line is kept in the released state
- The hold time for the start condition is set as half of a bit period at the bit rate determined by the BRR setting

- The level on the SCLn line falls (from high level to low level), the IICSTAREQ bit in SIMR3 is set to 0, and a start-condition generated interrupt is output.

Writing 1 to the IICRSTAREQ bit in SIMR3 causes the generation of a restart condition. The generation of a restart condition proceeds through the following operations:

- The SDAn line is released and the SCLn line is kept at a low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from low level to high level)
- When a high level is detected on the SCLn line, the setup time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SDAn line falls (from high level to low level)
- The hold time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from high level to low level), the SIMR3.IICRSTAREQ bit is set to 0, and a restart-condition generated interrupt is output.

Writing 1 to the SIMR3.IICSTPREQ bit causes the generation of a stop condition. The generation of a stop condition proceeds through the following operations:

- The level on the SDAn line falls (from high level to low level) and the SCLn line is kept at a low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from low level to high level)
- When a high level is detected on the SCLn line, the setup time for the stop condition is set as half of a bit period at the bit rate determined by the BRR setting
- The SDAn line is released (transition from low level to high level), the SIMR3.IICSTPREQ bit is set to 0, and a stop-condition generated interrupt is output.

Figure 27.60 shows the timing of operations in the generation of start, restart, and stop conditions.

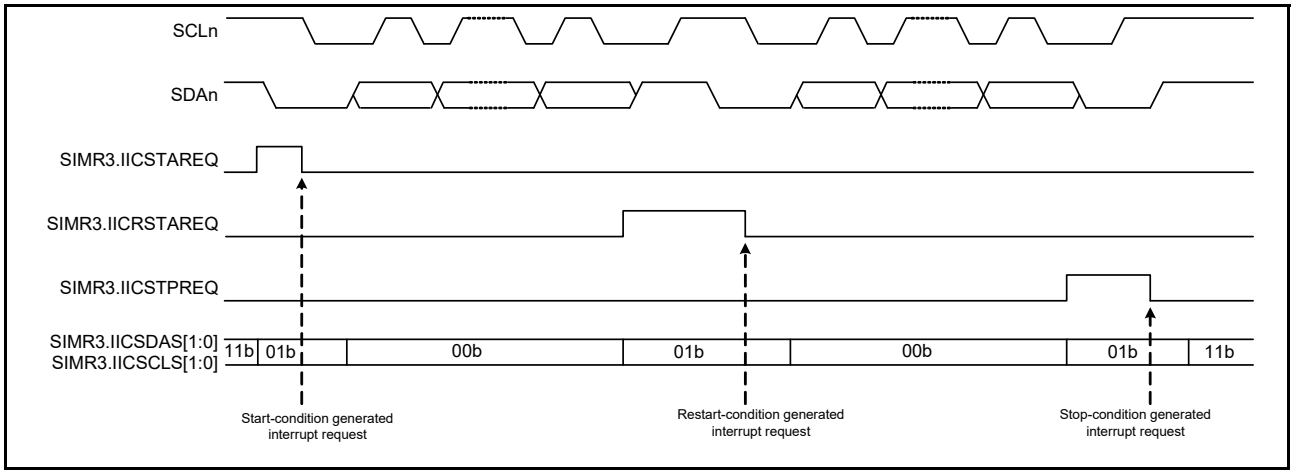


Figure 27.60 Timing of operations to generate start, restart, and stop conditions

27.7.2 Clock Synchronization

The SCLn line can be driven low if a wait is inserted by a slave device at the other side of the transfer. Setting the SIMR2.IICCSC bit to 1 allows clock synchronization control when a difference arises between the levels of the internal SCLn clock signal and the level being input on the SCLn pin.

When the SIMR2.IICCSC bit is set to 1, the level of the internal SCLn clock signal changes from low to high. Counting to determine the period at a high level stops while the low level is being input on the SCLn pin. Counting to determine the period at a high level starts after the input on the SCLn pin transitions to the high level.

The interval from the time until counting, to determine the period at high level that starts on the transition of the SCLn pin to the high level, is the total of the delay of SCLn output, delay for noise filtering of the input on the SCLn pin (2 or 3 cycles of sampling clock for the noise filter), and delay for internal processing (1 or 2 PCLKA cycles). The period at high level of the internal SCLn clock is extended even when other devices are not placing the low level on the SCLn line.

If the SIMR2.IICCSC bit is 1, synchronization is obtained for the transmission and reception of data by taking the logical AND of the input on the SCLn pin and the internal SCLn clock. If the SIMR2.IICCSC bit is 0, synchronization with the internal SCLn clock is obtained for the transmission and reception of data.

If a slave device inserts a wait period into the interval until the transition of the internal SCLn clock signal from the low to the high level after a request for the generation of a start, restart, or stop condition is issued, the time until generation is prolonged by that period.

If a slave device inserts a wait period after a transition of the internal SCLn clock signal from the low to the high level, although the generation-completed interrupt is issued without stopping the waiting period, generation of the condition itself is not guaranteed. Figure 27.61 shows an example of operation to synchronize the clocks.

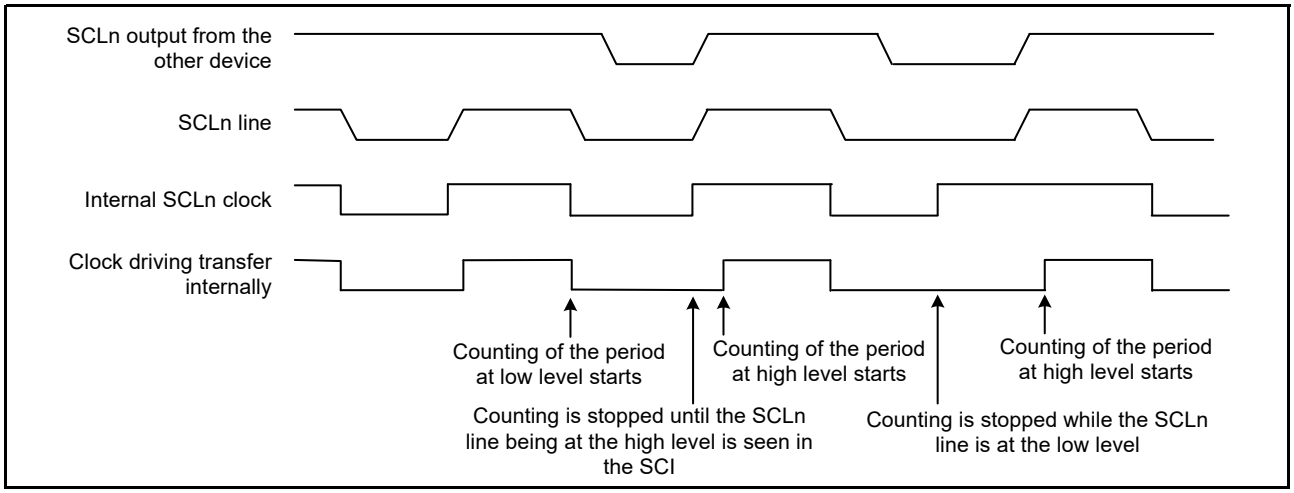


Figure 27.61 Example of operations for clock synchronization

27.7.3 SDA Output Delay

The SIMR1.IICDL[4:0] bits can be used to set a delay for the output on the SDAn pin relative to the falling edges of output on the SCLn pin. Delay settings from 0 to 31 are selectable. The delay settings represent periods of the associated numbers of cycles of the clock signal from the on-chip baud rate generator (derived by frequency-dividing the base clock, PCLKA, by the divisor selected in the SMR.CKS[1:0] bits). A delay for output on the SDAn pin applies to the start condition/restart condition/stop condition signal, 8-bit transmit data, and an acknowledge bit.

If the SDA output delay is shorter than the time required for the level on the SCLn pin to fall, the change of the output on the SDAn pin starts while the output level on the SCLn pin is falling, creating a possibility of erroneous operation of slave devices. Ensure that the settings for output delay on the SDAn pin specify a time period greater than the time that the output on the SCLn pin takes to fall (300 ns for IIC in standard mode and fast mode).

Figure 27.62 shows the timing of delays in SDA output.

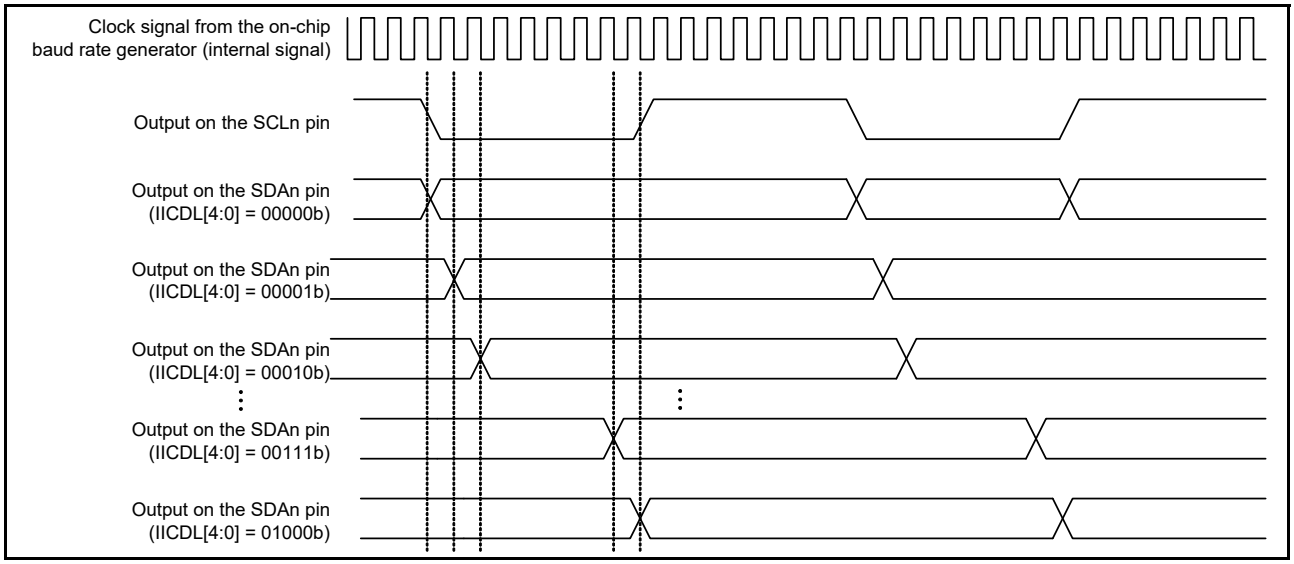


Figure 27.62 Timing of delays in SDA output

27.7.4 SCI Initialization in Simple IIC Mode

Before transferring data, write the initial value of 00h to SCR and initialize the interface as shown in the example in Figure 27.63. Before making any changes to the operating mode or transfer format, be sure to set SCR to its initial value. In simple IIC mode, the open-drain setting for the communication ports should be made on the port side.

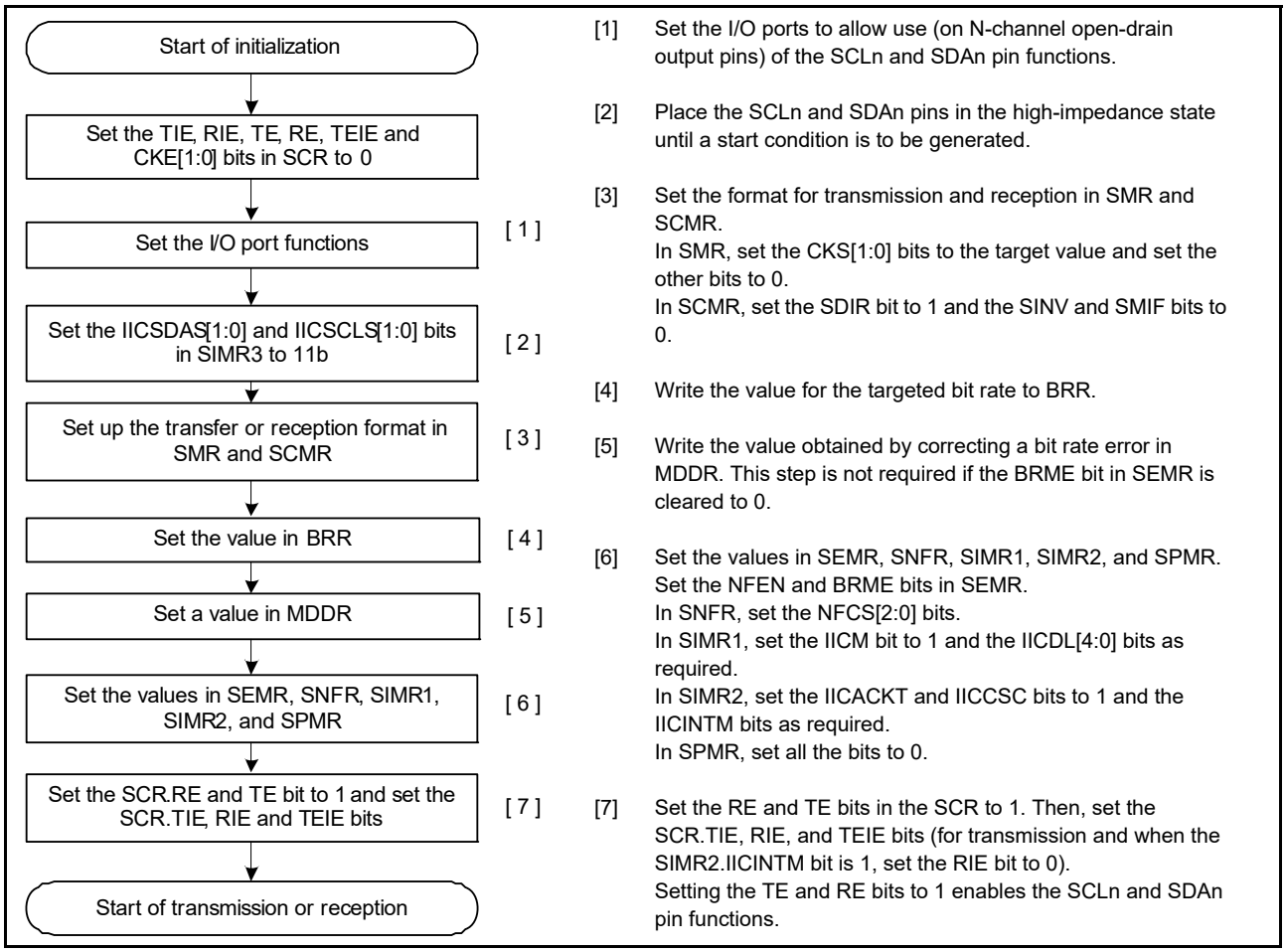


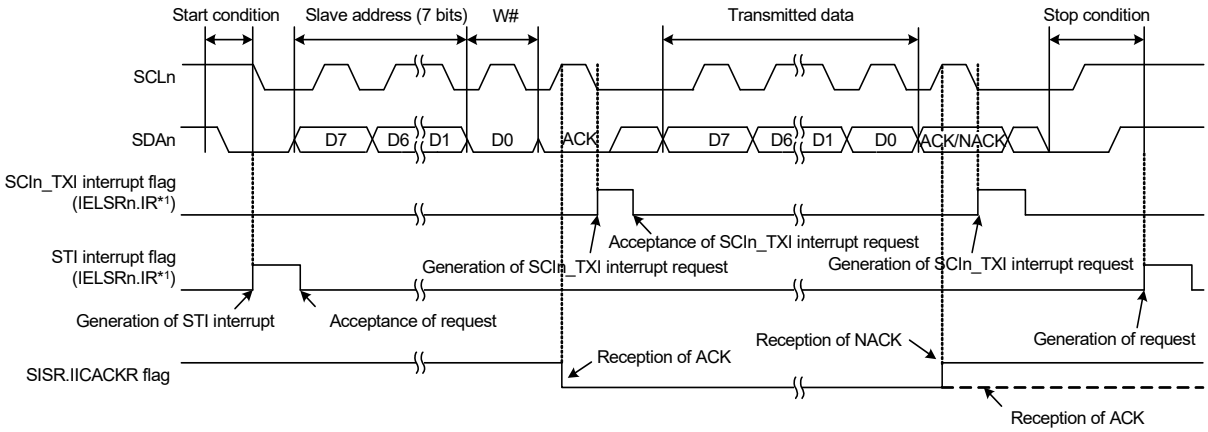
Figure 27.63 Example flow of SCI initialization in simple IIC mode

27.7.5 Operation in Master Transmission in Simple IIC Mode

Figure 27.64 and Figure 27.65 show examples of master transmission and Figure 27.66 shows an example flow of data transmission. The value of the SIMR2.IICINTM bit is assumed to be 1 (use reception and transmission interrupts) and the value of the SCR.RIE bit is assumed to be 0 (SCIn_RXI and SCIn_ERI interrupt requests are disabled). See Table 27.29 for more information on the STI interrupt.

When 10-bit slave addresses are in use, steps [3] and [4] in Figure 27.66 are repeated twice.

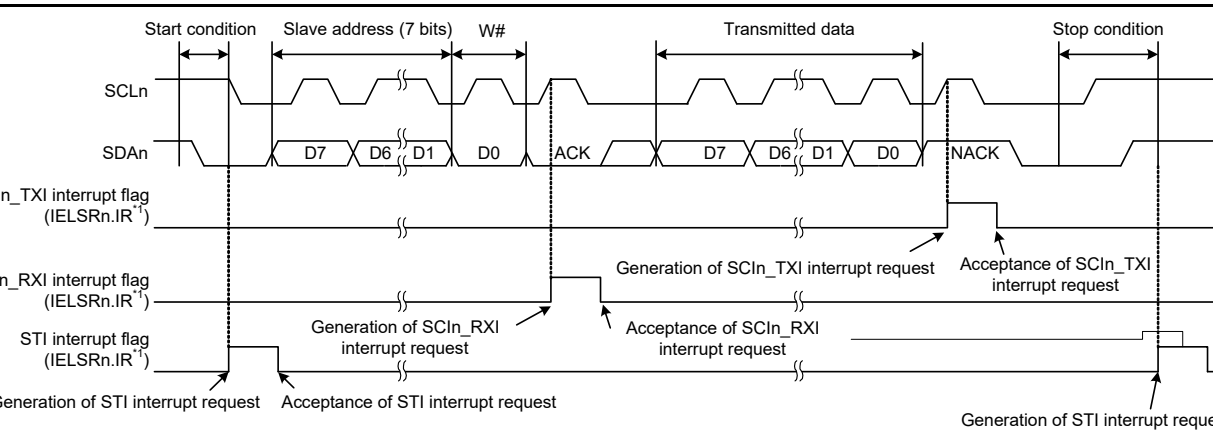
In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the timing of the SCIn_TXI interrupt request generation during clock synchronous transmission.



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

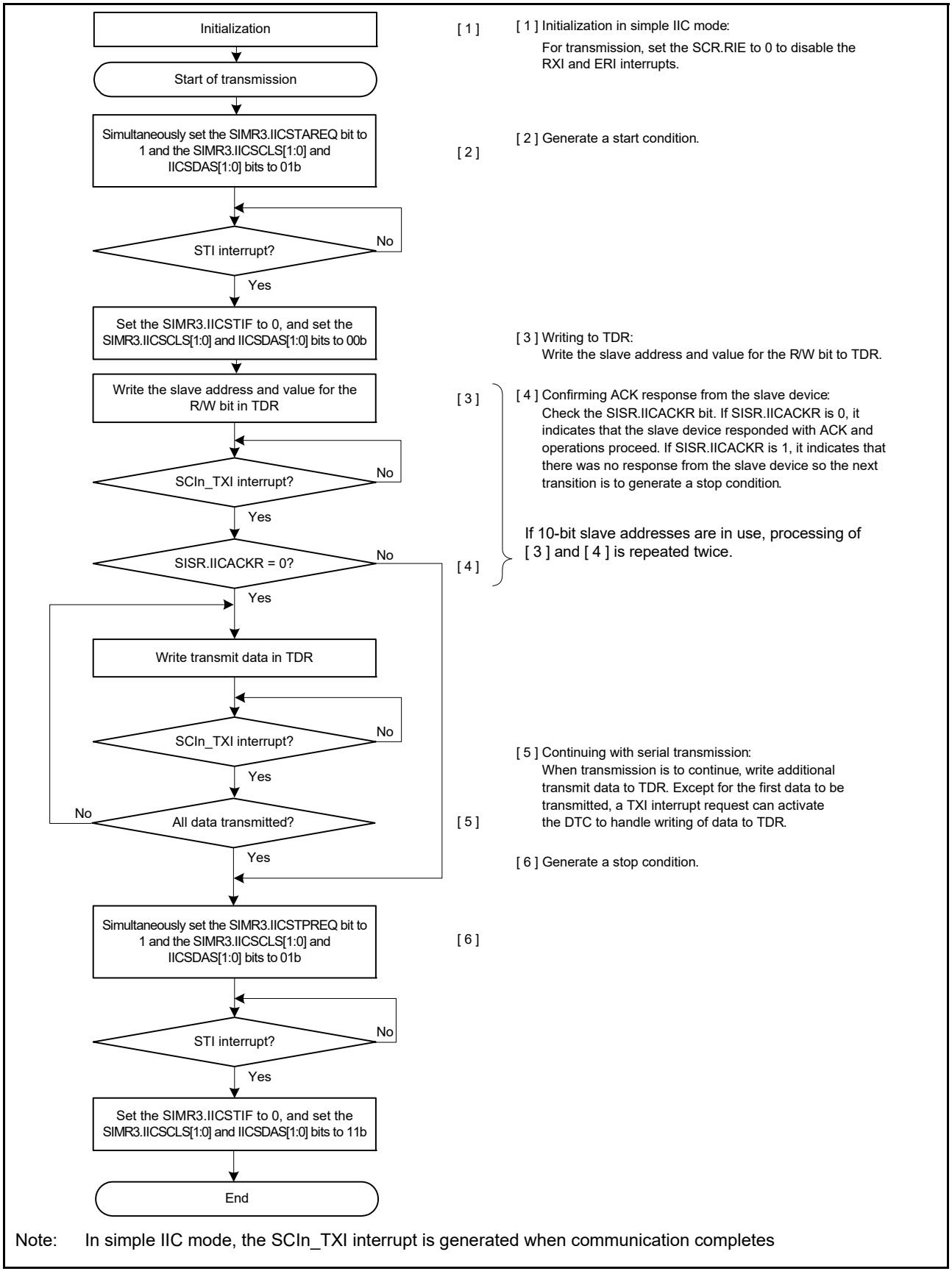
Figure 27.64 Example 1 operation for master transmission in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

When the SIMR2.IICINTM bit is set to 0, using ACK/NACK interrupts during master transmission, the DMAC or DTC is activated by the ACK interrupt as the trigger and the required number of data bytes are transmitted. When a NACK is received, error processing such as transmission stop and retransmission is performed using the NACK interrupt as the trigger.



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 27.65 Example 2 operation for master transmission in simple IIC mode with 7-bit slave addresses, ACK interrupts, and NACK interrupts



Note: In simple IIC mode, the SCIn_TXI interrupt is generated when communication completes

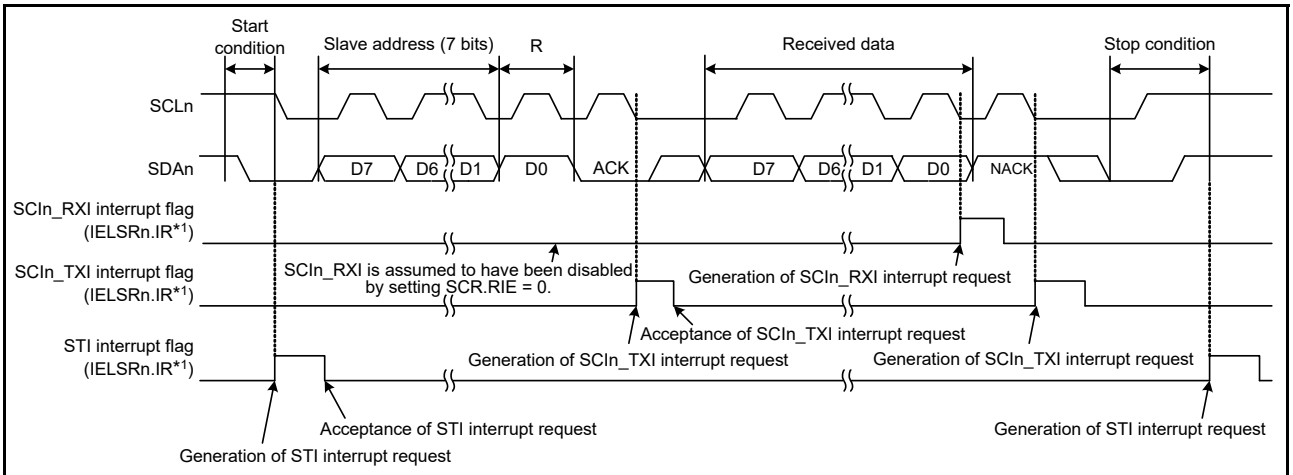
Figure 27.66 Example flow of master transmission in simple IIC mode with transmission interrupts and reception interrupts

27.7.6 Master Reception in Simple IIC Mode

Figure 27.67 shows an example of master reception operation in simple IIC mode and Figure 27.68 shows an example flow of master reception.

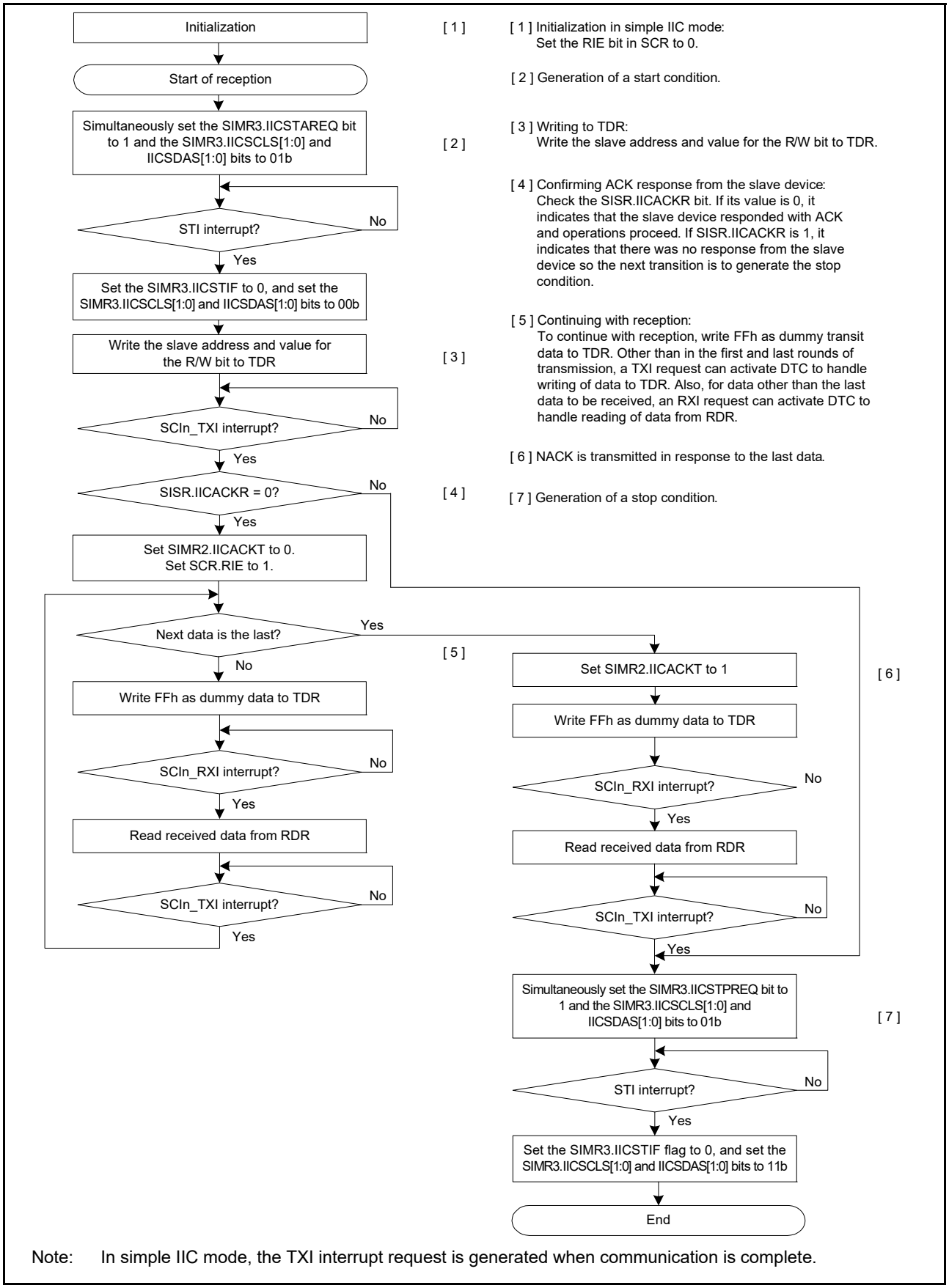
The value of the SIMR2.IICINTM bit is assumed to be 1, using reception and transmission interrupts.

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the timing of the SCIn_TXI interrupt request generation timing during clock synchronous transmission.



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 27.67 Example operation for master reception in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts



Note: In simple IIC mode, the TXI interrupt request is generated when communication is complete.

Figure 27.68 Example flow of master reception in simple IIC mode with transmission interrupts and reception interrupts

27.8 Operation in Simple SPI Mode

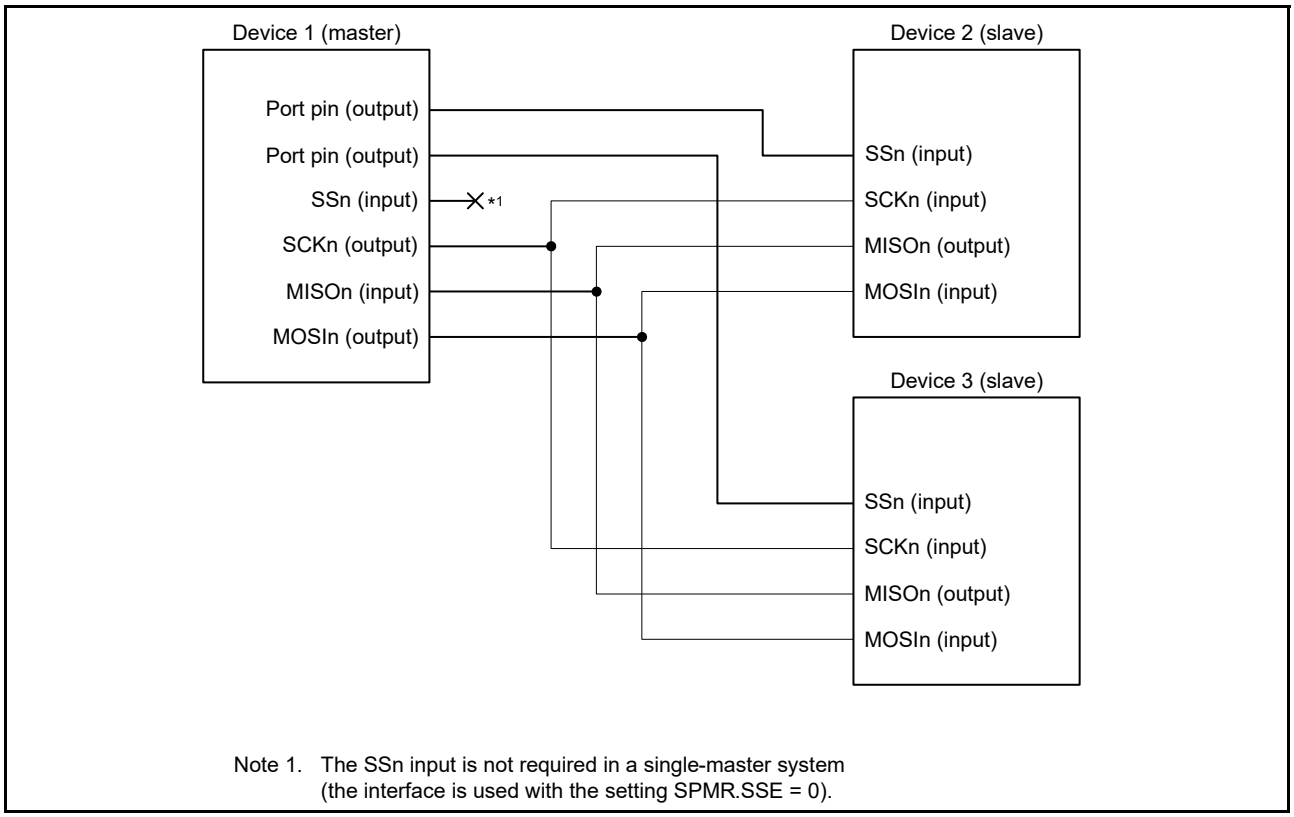
As an extended function, the SCI supports a simple SPI mode that handles transfer between one or multiple master devices and multiple slave devices.

To place the SCI in simple SPI mode, use the settings for clock synchronous mode (SCMR.SMIF = 0, SIMR1.IICM = 0, SMR.CM = 1) and set the SPMR.SSE bit to 1. When the configuration only has a single master, the SSn pin function on the master side is not required to connect the device used as the master in simple SPI mode. Therefore, set the SPMR.SSE bit to 0 in this case.

Figure 27.69 shows an example of connections in simple SPI mode. Use a general port pin to produce the SSn output signal from the master.

In simple SPI mode, data is transferred in synchronization with clock pulses in the same way as in clock synchronous mode. One character of transfer data consists of 8 bits of data, and parity bits cannot be appended. The data can be inverted by setting the SCMR.SINV bit to 1.

Because the receiver and transmitter are independent of each other within the SCI module, full-duplex communications are possible, with a common clock signal. Additionally, because both the transmitter and receiver have a buffered structure, it is possible to write the next transmit data while transmission is in progress and also read previously received data while reception is in progress. This enables continuous transfer.



Note 1. The SSn input is not required in a single-master system (the interface is used with the setting SPMR.SSE = 0).

Figure 27.69 Example connections using simple SPI mode in single master mode with SPMR.SSE bit = 0

27.8.1 States of Pins in Master and Slave Modes

The direction (input or output) of pins for the simple SPI mode interface differs according to whether the device is a master (SCR.CKE[1:0] = 00b or 01b and SPMR.MSS = 0) or slave (SCR.CKE[1:0] = 10b or 11b and SPMR.MSS = 1).

Table 27.25 lists the relationship between the pin states, mode, and input level on the SSn pin.

Table 27.25 Pin states by mode and input level on the SSn pin

Mode	Input on SSn pin	State of TXDn pin	State of RXDn pin	State of SCKn pin
Master mode*1	High level (transfer can proceed)	Output for data transmission*2	Input for received data	Clock output*3
	Low level (transfer cannot proceed)	High-impedance	Input for received data (but disabled)	High-impedance
Slave mode	High level (transfer cannot proceed)	Input for received data (but disabled)	High-impedance	Clock input (but disabled)
	Low level (transfer can proceed)	Input for received data	Output for data transmission	Clock input

Note 1. When there is only a single master (SPMR.SSE = 0), transfer is possible regardless of the input level on the SSn pin. This is equivalent to the input of a high level on the SSn pin. Because the SSn pin function is not required, the pin is available for other purposes.
Note 2. The MOSIn pin output is in a high-impedance state when serial transmission is disabled (SCR.TE = 0).
Note 3. The SCKn pin output is in a high-impedance state when serial transmission is disabled (SCR.TE and RE = 00b) in a multi-master configuration (SPMR.SSE = 1).

27.8.2 SS Function in Master Mode

Setting the SCR.CKE[1:0] bits to 00b and the SPMR.MSS bit to 0 selects master operation. The SSn pin is not used in single-master configurations (SPMR.SSE = 0), so transmission or reception can proceed regardless of the value of the SSn pin.

When the level on the SSn pin is high in a multi-master configuration (SPMR.SSE = 1), a master device outputs clock signals from the SCKn pin before starting transmission or reception to indicate that there are no other masters or another master is performing reception or transmission.

When the level on the SSn pin is low in a multi-master configuration (SPMR.SSE = 1), there are other masters, and this indicates that transmission or reception is in progress. The MOSIn output and SCKn pins are placed in a high-impedance state and starting transmission or reception is not possible. In addition, the value of the SPMR.MFF bit is 1, indicating a mode fault error. In a multi-master configuration, start error processing by reading the SPMR.MFF flag. Even if a mode fault error occurs while transmission or reception is in progress, transmission or reception does not stop, but the MOSIn and SCKn outputs are placed in the high-impedance state after completion of the transfer. Use a general port pin to produce the SS output signal from the master.

27.8.3 SS Function in Slave Mode

Setting the SCR.CKE[1:0] bits to 10b and the SPMR.MSS bit to 1 selects slave operation. When the level on the SSn pin is high, the MISOn output pin is in a high-impedance state and the clock input through the SCKn pin is ignored. When the level on the SSn pin is low, clock input through the SCKn pin is valid and transmission or reception can proceed.

If the input on the SSn pin changes from low to high during transmission or reception, the MISOn output pin is placed in a high-impedance state. Meanwhile, the internal processing for transmission or reception continues at the rate of the clock input through the SCKn pin until processing for the current transmitted or received character is complete, after which it stops, and the appropriate interrupt (SCIn_TXI, SCIn_RXI, or SCIn_TEI) is then generated.

27.8.4 Relationship between Clock and Transmit/Receive Data

The CKPOL and CKPH bits in the SPMR can be used to set up the clock for use in transmission and reception in four different ways. The relation between the clock signal and the transmission and reception of data is shown in Figure 27.70. The relation is the same for both master and slave operation. This is the same as when the level on the SSn pin is high.

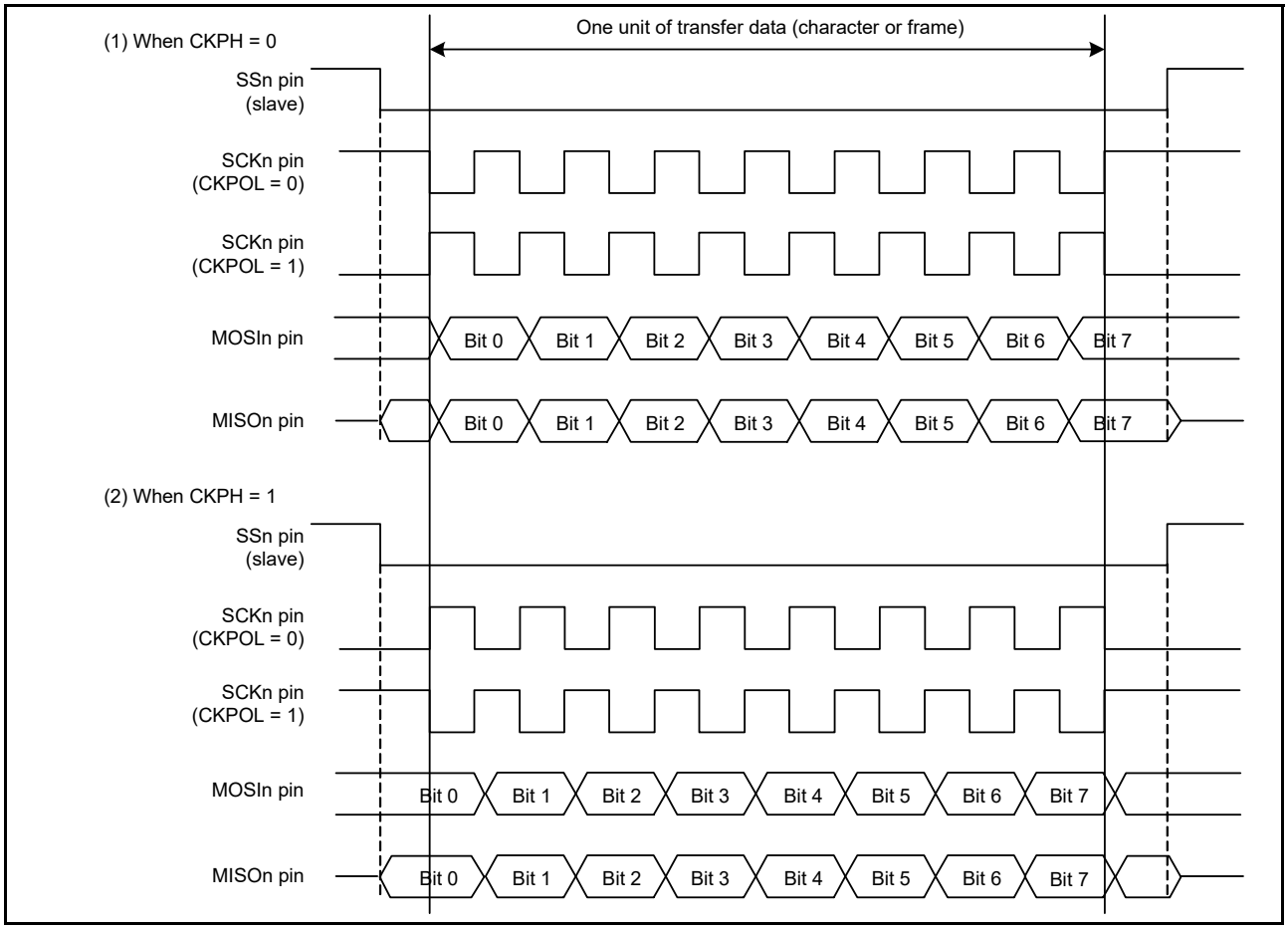


Figure 27.70 Relation between clock signal and transmit or receive data in simple SPI mode

27.8.5 SCI Initialization in Simple SPI Mode

Initialization in simple SPI mode is the same as in clock synchronous mode. See Figure 27.32 for an example initialization flow. The CKPOL and CKPH bits in the SPMR must be set to ensure that the selected clock signal configuration is suitable for both master and slave devices.

Always initialize the SCR register before making any changes to the operating mode or transfer format.

Note: Only the RE bit is set to 0. The SSR.ORER, FER, PER, and RDR flags are not initialized.

Changing the value of the TE bit from 1 to 0 or from 0 to 1 when the TIE bit in the SCR register is 1 at the same time, leads to the generation of a transmit data empty interrupt (SCIn_TXI).

27.8.6 Transmission and Reception of Serial Data in Simple SPI Mode

In master operation, ensure that the SSn pin of the slave device on the other side of the transfer is at a low level before starting the transfer and at a high level on completion of the transfer. Otherwise, the procedures are the same as in clock synchronous mode.

27.9 Bit Rate Modulation Function

Using the bit rate modulation function, the bit rate can be evenly corrected using the number specified in the MDDR register when PCLKA is selected in the CKS[1:0] bits in SMR/SMR_SMCI.

Figure 27.71 shows an example where PCLKA is selected in the CKS[1:0] bits in SMR/SMR_SMCI, the BRR bit is set to 0, and the MDDR is set to 160 in asynchronous mode. In this example, the cycle of the base clock is evenly corrected (256/160) and the bit rate is also corrected (160/256).

Note: Enabling an internal clock causes bias and expansion. Contraction is generated in the pulse width of the internal base clock.

Do not use this function in clock synchronous mode and in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).

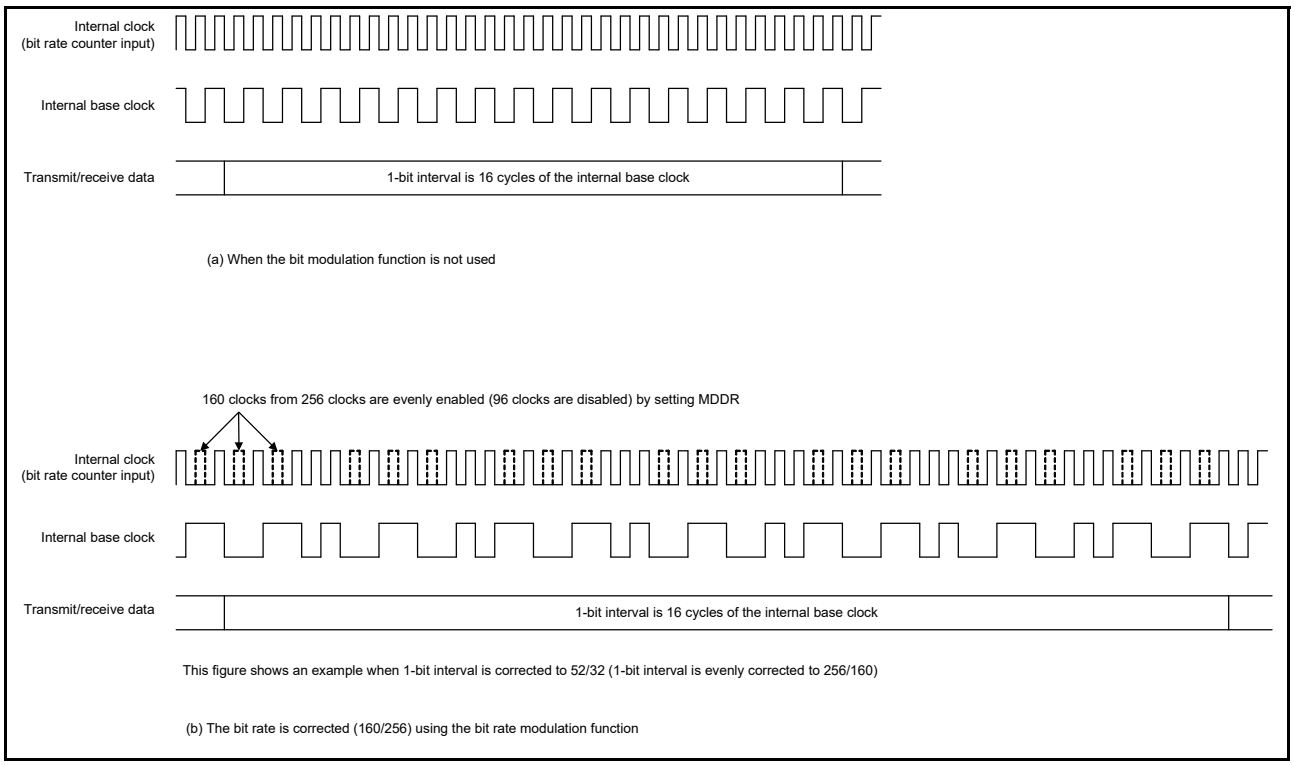


Figure 27.71 Example of internal base clock using bit rate modulation function

27.10 Interrupt Sources

27.10.1 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (non-FIFO selected)

If the conditions for an SCIn_TXI and SCIn_RXI interrupt are satisfied while the interrupt status flag in the ICU is 1, the ICU does not output the interrupt request but saves it internally, with a capacity for saving one request per source.

When the interrupt status flag in the ICU becomes 0, the interrupt request retained within the ICU is output. The internally retained interrupt request is automatically discarded when the actual interrupt is output. Clearing of the associated interrupt enable bit (the TIE or RIE bit in the SCR/SCR_SMCI) can also be used to discard an internally retained interrupt request.

27.10.2 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (FIFO selected)

When an interrupt status flag in the ICU is set to 1, the SCIn_TXI and SCIn_RXI interrupts do not output interrupt requests to the ICU. When an interrupt status flag of the ICU is set to 0, and if the conditions for SCIn_TXI and SCIn_RXI interrupts are satisfied, an interrupt request is generated.

27.10.3 Interrupts in Asynchronous, Clock Synchronous, and Simple SPI Modes

(1) Non-FIFO selected

Table 27.26 lists interrupt sources in asynchronous, clock synchronous, and simple SPI modes. A different interrupt vector can be assigned to each interrupt source. Individual interrupt sources can be enabled or disabled with the enable bits in the SCR register.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when transmit data is transferred from the TDR or TDRHL register*1 to the TSR register. An SCIn_TXI interrupt request can also be generated using a single instruction to set the SCR.TE and SCR.TIE bits to 1 simultaneously. An SCIn_TXI interrupt request can activate the DMAC or DTC to handle data transfer.

An SCIn_TXI interrupt request is not generated by setting the SCR.TE bit to 1 when SCR.TIE is 0 or by setting the SCR.TIE bit to 1 when the SCR.TE is 1.*2

When new data is not written by the time of transmission of the last bit of the current transmit data and SCR.TEIE is 1, the SSR.TEND flag sets to 1 and an SCIn_TEI interrupt request is generated. Additionally, when SCR.TE is 1, the SSR.TEND flag retains the value 1 until more transmit data are written to the TDR or TDRHL register*1, and setting SCR.TEIE to 1 leads to the generation of an SCIn_TEI interrupt request.

Writing data to the TDR or TDRHL register*1 leads to clearing of the SSR.TEND flag and, after a certain time, discarding of the SCIn_TEI interrupt request.

If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated when received data is stored in the RDR register. An SCIn_RXI interrupt request can activate the DMAC or DTC to handle data transfer.

Setting any of the ORER, FER, and PER flags in the SSR register to 1 while the SCR.RIE bit is 1 leads to the generation of an SCIn_ERI interrupt request. An SCIn_RXI interrupt request is not generated at this time. Clearing all three flags (ORER, FER, and PER) leads to discarding of the SCIn_ERI interrupt request.

(2) FIFO selected

Table 27.27 lists the interrupt sources in FIFO selected mode.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when the amount of stored data in the FTDRL register becomes equal to or less than the threshold value indicated in FCR.TTRG. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the SCR.TE and SCR.TIE bits to 1 simultaneously.

An SCIn_TXI interrupt request is not generated by setting SCR.TE to 1 when SCR.TIE is 0 or by setting SCR.TIE to 1 when SCR.TE is 1.

If SCR.TEIE is 1 and if the next data is not written to the FTDRL register by the time the last bit of the transmit data is sent, the SSR_FIFO.TEND flag is set to 1 and the SCIn_TEI interrupt request is generated.

If SCR.RIE is 1, the SCIn_RXI interrupt request is generated when the amount of stored data in the FRDRL register becomes equal to or greater than the threshold value indicated in FCR.RTRG. When RTRG is 0, an SCIn_RXI interrupt does not occur even when the amount of data in the receive FIFO is equal to 0.

If the SCR.RIE bit is 1, when the SSR_FIFO.ORER flag is set to 1 or data with a framing error or a parity error is stored in the FRDRL register, the SCIn_ERI interrupt request is generated. When the amount of data stored in the FRDRL register is at or above the threshold value, the SCIn_RXI interrupt request is also generated. The SCIn_ERI interrupt request can be canceled, in which case the SSR_FIFO.ORER, FER, and PER flags are all cleared.

Note 1. When asynchronous mode and 9-bit data length are selected.
Note 2. To temporarily prohibit the SCIn_TXI interrupts on transmission of the last of the data when a new round of transmission is to be started, after handling the transmission-completed interrupt, control the activation of the interrupt by using the interrupt request enable bit in the ICU rather than using the SCR.TIE bit. This approach can prevent the suppression of the SCIn_TXI interrupt requests in the transfer of new data.

Table 27.26 SCI interrupt sources with non-FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_ERI	Receive error*1	ORER, FER, PER, DFER, DPER	RIE	Not possible	Not possible
SCIn_RXI	Receive data full	RDRF	RIE	Possible	Possible
	Address match	DCMF	RIE	Possible	Possible
SCIn_AM	Address match	DCMF	-	Possible	Possible
SCIn_TXI	Transmit data empty	TDRE	TIE	Possible	Possible
SCIn_TEI	Transmit end	TEND	TEIE	Not possible	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous mode and simple SPI mode.

Table 27.27 SCI interrupt sources with FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_ERI	Receive error*1	ORER, FER, PER, DFER, DPER	RIE	Not possible	Not possible
		DR (when FCR.DRES = 1)	RIE	Not possible	Not possible
SCIn_RXI	Receive data full	RDF	RIE	Possible	Possible
	Receive data ready	DR (when FCR.DRES = 0)	RIE	Possible	Possible
	Address match	DCMF	RIE	Possible	Possible
SCIn_AM	Address match	DCMF	-	Possible	Possible
SCIn_TXI	Transmit data empty	TDFE	TIE	Possible	Possible
SCIn_TEI	Transmit end	TEND	TEIE	Not possible	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous mode and simple SPI mode.

27.10.4 Interrupts in Smart Card Interface Mode

Table 27.28 lists the interrupt sources in smart card interface mode. A transmit end interrupt (SCIn_TEI) request and an address match (SCIn_AM) request cannot be used in this mode.

Table 27.28 SCI Interrupt sources in smart card interface mode

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_ERI	Receive error or error signal detection	ORER, FER, ERS	RIE	Not possible	Not possible
SCIn_RXI	Receive data full	RDRF	RIE	Possible	Possible
SCIn_TXI	Transmit end	TEND	TIE	Possible	Possible

Data transmission or reception using the DMAC or DTC is also possible in smart card interface mode. In transmission, when the SSR_SMCI.TEND flag is set to 1, an SCIn_TXI interrupt request is generated. The SCIn_TXI interrupt request activates the DMAC or DTC, allowing the transfer of transmit data if the SCIn_TXI request is previously specified as a source for DMAC or DTC activation. The TEND flag is automatically set to 0 when the DMAC or DTC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During the retransmission, the TEND flag is kept at 0 and the DMAC or DTC is not activated. Therefore, the SCI and DMAC or DTC automatically transmit the specified number of bytes, including retransmission when errors occur. However, the SSR_SMCI.ERS flag is not automatically cleared to 0 at error occurrence. Therefore, the ERS flag must be cleared by previously setting the SCR_SMCI.RIE bit to 1 to enable an SCIn_ERI interrupt request to be generated at error occurrence.

When transmitting or receiving data using the DMAC or DTC, always enable the DMAC or DTC before setting the SCI. For DMAC or DTC settings, see section 16, DMA Controller (DMAC) and section 17, Data Transfer Controller (DTC).

In reception, an SCIn_RXI interrupt request is generated when receive data is set to RDR. The SCIn_RXI interrupt request activates the DMAC or DTC, allowing transfer of receive data if the SCIn_RXI request is previously specified as a source of DMAC or DTC activation. If an error occurs, the error flag is set. Therefore, the DMAC or DTC is not activated and an SCIn_ERI interrupt request is issued to the CPU instead. The error flag must be cleared.

27.10.5 Interrupts in Simple IIC Mode

Table 27.29 lists the interrupt sources in simple IIC mode. The STI interrupt is allocated to the transmit end interrupt (SCIn_TEI) request. The receive error interrupt (SCIn_ERI) and the address match (SCIn_AM) request cannot be used.

The DMAC or DTC can also be used to handle transfer in simple IIC mode.

When the SIMR2.IICINTM bit is 1:

- An SCIn_RXI request is generated on the falling edge of the SCLn signal for the 8th bit. If SCIn_RXI is previously

set up as an activation source for the DMAC or DTC, the SCIn_RXI request activates the DMAC or DTC to handle transfer of the received data.

- An SCIn_TXI request is generated on the falling edge of the SCLn signal for the 9th bit (acknowledge bit). If SCIn_TXI is previously set up as an activation source for the DMAC or DTC, the SCIn_TXI request activates the DMAC or DTC to handle transfer of the transmit data.

When the SIMR2.IICINTM bit is 0:

- An SCIn_RXI request (ACK detection) is generated if the input on the SDAn pin is low on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- An SCIn_TXI request (NACK detection) is generated if the input on the SDAn pin is high on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- If SCIn_RXI is previously set up as an activation source for the DMAC or DTC, the SCIn_RXI request activates the DMAC or DTC to handle the transfer of the received data.

If the DMAC or DTC is used for data transfer in reception or transmission, always set up and enable the DMAC or DTC before setting up the SCI.

When the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits in SIMR3 are used to generate a start condition, restart condition, or stop condition, the STI request is issued when generation is complete.

Table 27.29 SCI interrupt sources in simple IIC mode

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_RXI	Reception, ACK detection	-	RIE	Possible	Possible
SCIn_TXI	Transmission, NACK detection	-	TIE	Possible	Possible
STIn	Completion of generation of a start, restart, or stop condition	IICSTIF	TEIE	Not possible	Not possible

Note 1. Activation of the DTC is only possible when the SIMR2.IICINTM bit is 1 (use reception and transmission interrupts).

27.11 Event Linking

By using interrupt request signals as event signals, the SCI can provide linked operation through the Event Link Controller (ELC) for modules selected in advance.

Event signals can be output regardless of the values of the associated interrupt request enable bits.

(1) Error event output (receive error or error signal detected)

- Indicates abnormal termination because of a parity error during reception in asynchronous mode
- Indicates abnormal termination because of a framing error during reception in asynchronous mode
- Indicates abnormal termination because of an overrun error during reception
- Indicates detection of the error signal during transmission in smart card interface mode
- Indicates that when the SSR_FIFO.FER and PER flags are 0, and receive data less than the receive FIFO data trigger number is in the receive FIFO buffer, 15 ETUs elapse when FIFO is selected and the FCR.DRES bit is 1.

(2) Receive data full event output

- Indicates that ACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 8th bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode
- When the SIMR2.IICINTM bit is 1 during master transmission in simple IIC mode, set the ELC so that receive data full events are not used.

(a) Non-FIFO selected

- Indicates that received data is set in the Receive Data Register (RDR or RDRHL).

(b) FIFO selected

- Using this event output is prohibited.

(3) Transmit data empty event output

- Indicates that the SCR/SCR_SMCI.TE bit changed from 0 to 1
- Indicates that transmission is complete in smart card interface mode
- Indicates that NACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 9th-bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode.

(a) Non-FIFO selected

- Indicates that transmit data is transferred from the Transmit Data Register (TDR or TDRHL) to the Transmit Shift Register (TSR).

(b) FIFO selected

- Using this event output is prohibited.

(4) Transmit end event output

- Indicates the completion of transmission
- Indicates that the starting condition, restart condition, or stop condition is generated in simple IIC mode

Note: When FIFO is selected, using this event output is prohibited.

(5) Address match event output

- Indicates a match of the comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode.

27.12 Address Mismatch Event Output (SCI0_DCUF)

The address mismatch event output, SCI0_DCUF, indicates a mismatch of the comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode. This event can be used for snooze end request only.

27.13 Noise Cancellation Function

Figure 27.72 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of a 2-stage flip-flop circuit and a match detection circuit. When the input signals of the noise filter and the output signals of the 2-stage flip-flop circuits completely match, the matched level is an internal signal. Unless a match occurs, the previous value is retained. When the same level is retained for 3 cycles or longer on the sampling clock of the noise filter, it is considered as a valid receive signal. A change in pulse for 3 cycles or shorter is considered as noise and not as a receive signal.

When SEMR.ABCS = 0 and SEMR.ABCSE = 0, the cycle is 1/16 the period of 1 transfer bit.

When SEMR.ABCS = 1 and SEMR.ABCSE = 0, the cycle is 1/8 the period of 1 transfer bit.

When SEMR.ABCSE = 1, the cycle is 1/6 the period of 1 transfer bit.

In asynchronous mode, the noise cancellation function can be applied to the receive signal input on the RXDn pin. The receive level of the RXDn is sampled in the flip-flop circuit of the noise filter on the base clock of the asynchronous mode.

In simple IIC mode, the noise cancellation function can be used for each input on SDAn and SCLn. The sampling clock for the noise cancellation function is selected in the SNFR.NFCS[2:0] bit by dividing the baud rate generator source clock by 1, 2, 4, or 8.

If the base clock is stopped with the noise filter enabled and the base clock input is restarted again, the noise filter

operation resumes from the state where the clock was stopped. When SCR.TE and SCR.RE are set to 0 during base clock input, all of the noise filter flip-flop values are initialized to 1. Accordingly, if the input data is 1 when reception operation resumes, the function determines that a level match is detected and the result is an internal signal. When the level being input corresponds to 0, the initial output of the noise filter is retained until the level matches in 3 consecutive sampling cycles.

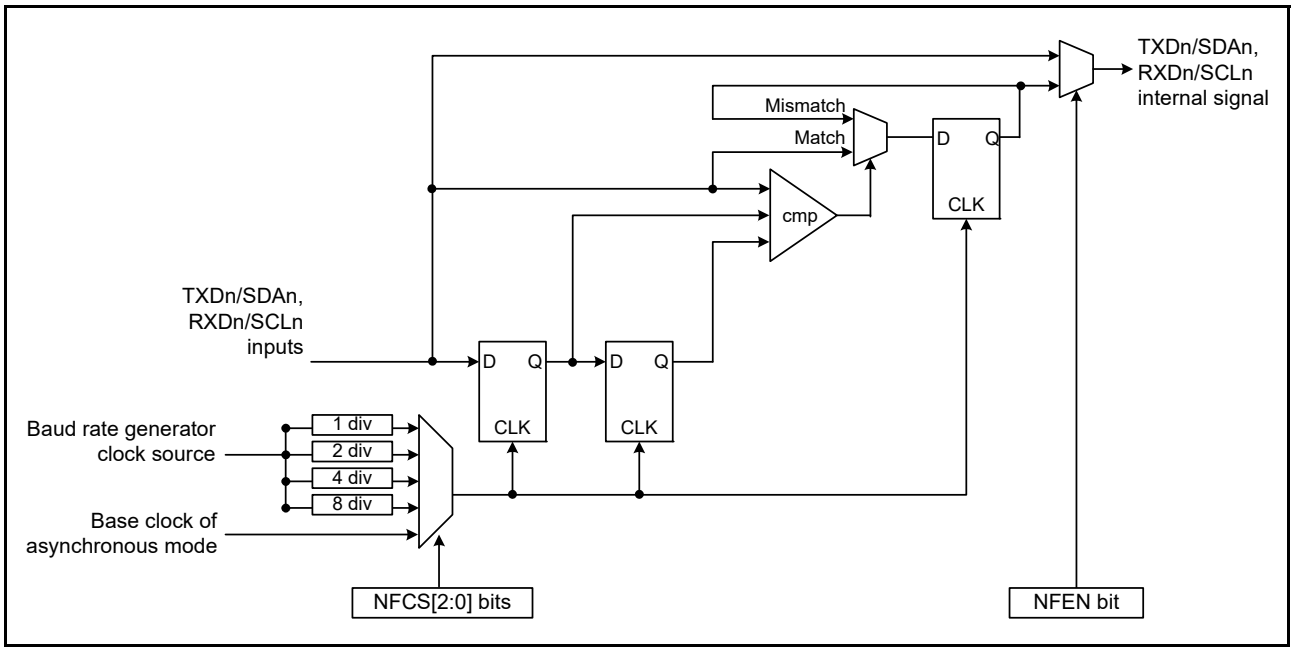


Figure 27.72 Digital noise filter circuit block diagram

27.14 Usage Notes

27.14.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable SCI operation. The SCI is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

27.14.2 SCI Operation during Low Power State

(1) Transmission

When setting the module to the stopped state or in transition to Software Standby, stop the operation (by setting the TIE, TE, and TEIE bits in the SCR/SCR_SMCI to 0) after switching the TXDn pin to the general I/O port pin function. When setting the I/O port as an SCI connection, the SPTR register can control the state of the TXDn pin. Setting the TE bit to 0 initializes the TSR register. The TEND bit in the SSR/SSR_SMCI is initialized to 1 with non-FIFO selected. The value is saved with FIFO selected. Depending on the port settings and the SPTR register settings, output pins might output the level before a transition to the low power state is made after release from the module-stop state or Software Standby mode. When transitions to these states are made during transmission, the transmitted data becomes indeterminate.

To transmit data in the same transmission mode after cancellation of the low power state:

1. Set the TE bit to 1.
2. Read SSR/SSR_FIFO/SSR_SMCI.
3. Write data to TDR sequentially to start data transmission.

To transmit data with a different transmission mode, initialize the SCI first.

Figure 27.73 shows an example flow of transition to Software Standby mode during transmission. Figure 27.74 and Figure 27.75 show the port pin states during transition to Software Standby mode.

Before specifying the module-stop state or making a transition to Software Standby mode from the transmission mode

using DTC transfer, stop the transmit operations (TE = 0). To start transmission after cancellation using the DTC, set the TE bit to 1. The SCIn_TXI interrupt flag is set to 1 and transmission starts using the DTC.

(2) Reception

(a) When address match function is not used as a wakeup condition

Before specifying the module-stop state or making a transition to Software Standby mode, stop the receive operations (RE = 0 in SCR/SCR_SMCI). If transition is made during data reception, the received data is invalid.

Figure 27.76 shows an example flow for transition to Software Standby mode during reception.

(b) When address match function is used as a wakeup condition

Before specifying the module-stop state or making a transition to Software Standby mode:

1. Set the operations after cancellation of the low power state.
2. Set CDR.CMPD and DCCR.DCME to 1.
3. Set the receive operations (RE = 1 in SCR/SCR_SMCI).
4. Set the module-stop state or Software Standby mode.

When the SCI transfers to the low power mode, if the receive data pin (RXD) is at the low level, set SEMR.RXDESEL to 0. When setting SEMR.RXDESEL to 1, there is a possibility that a start bit (falling edge of RXDn pin) cannot be detected on release of the low power mode.

Figure 27.77 shows an example flow of transition to Software Standby mode during reception with address match.

(c) When using SCI0 in Snooze mode

When using SCI0 in Snooze mode, some restrictions apply, including maximum bit rates. For details, see section 11, Low Power Modes.

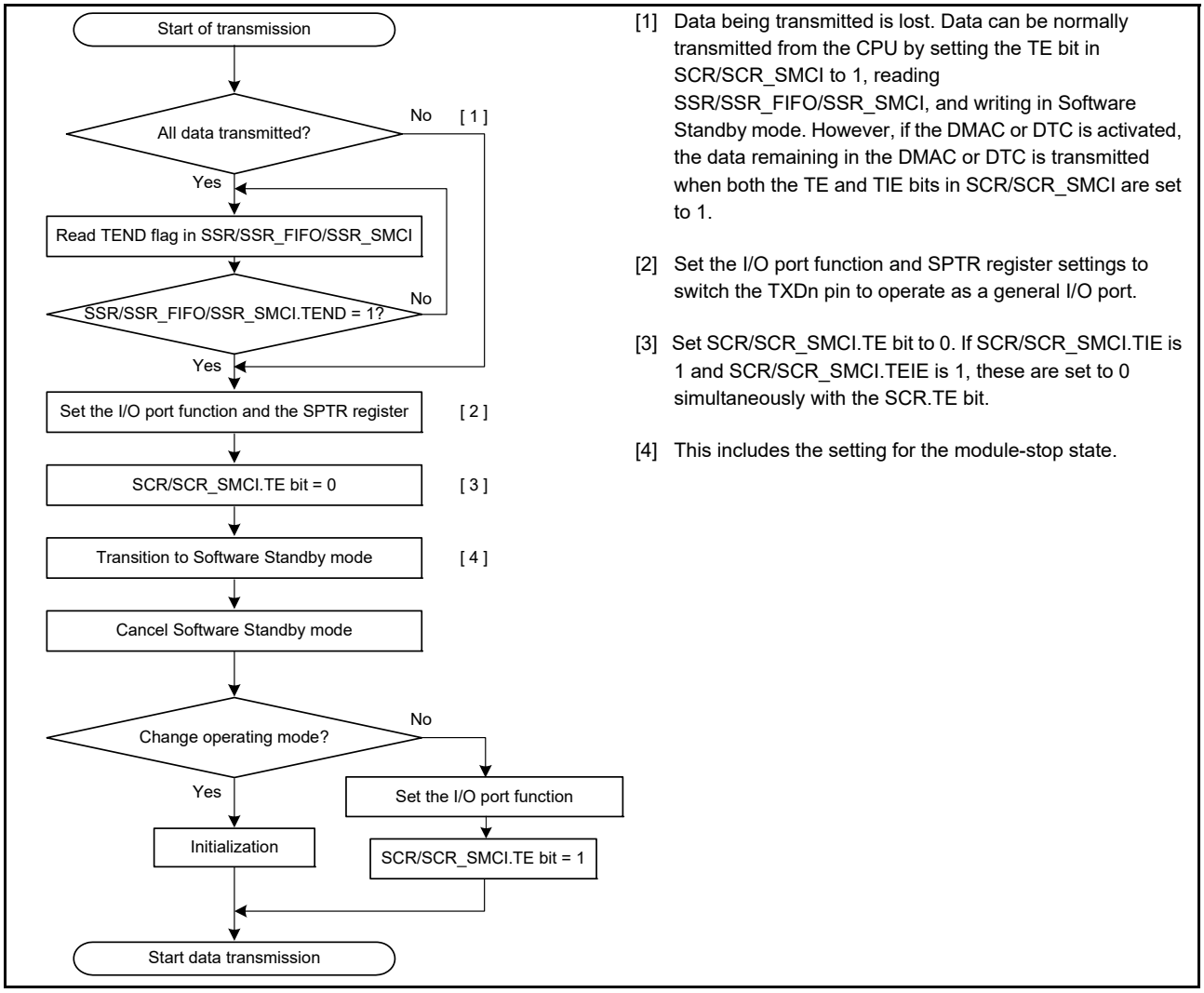


Figure 27.73 Example flow of transition to Software Standby mode during transmission

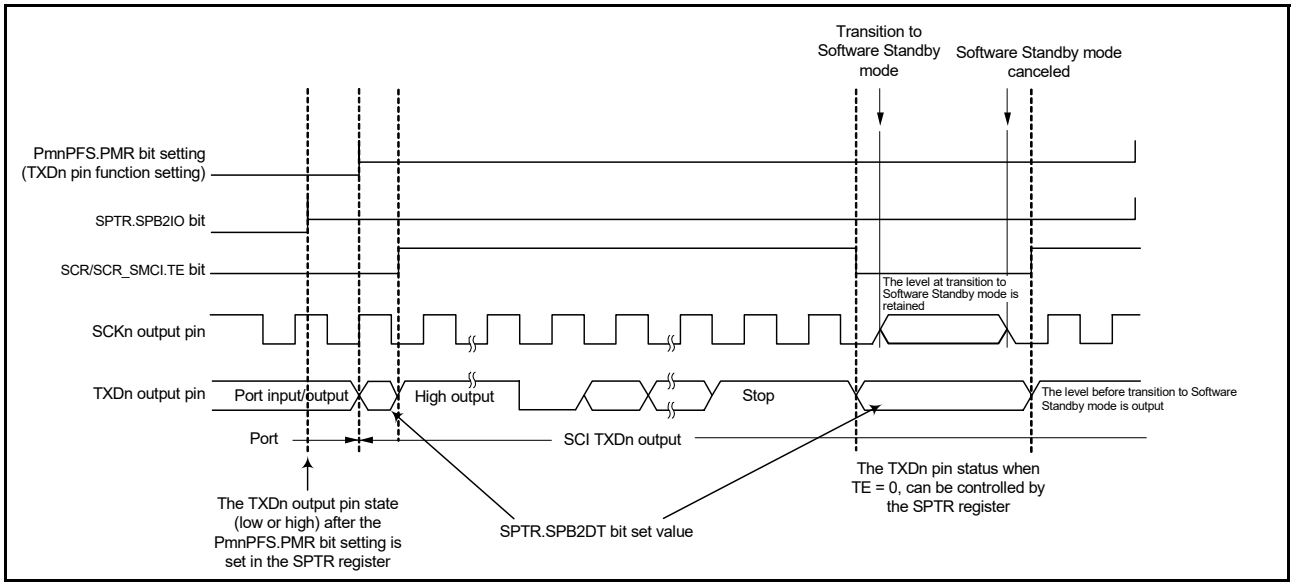


Figure 27.74 Port pin states during transition to Software Standby mode with internal clock and asynchronous transmission

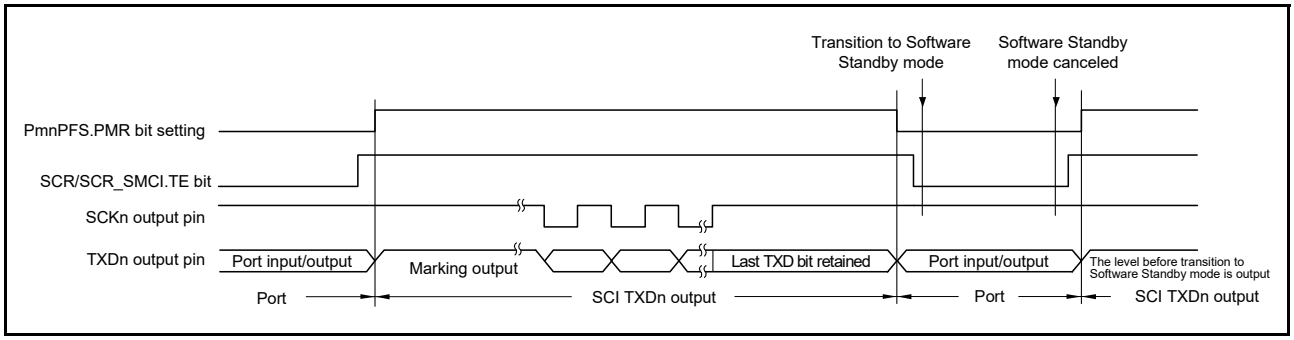


Figure 27.75 Port pin states during transition to Software Standby mode with internal clock and clock synchronous transmission

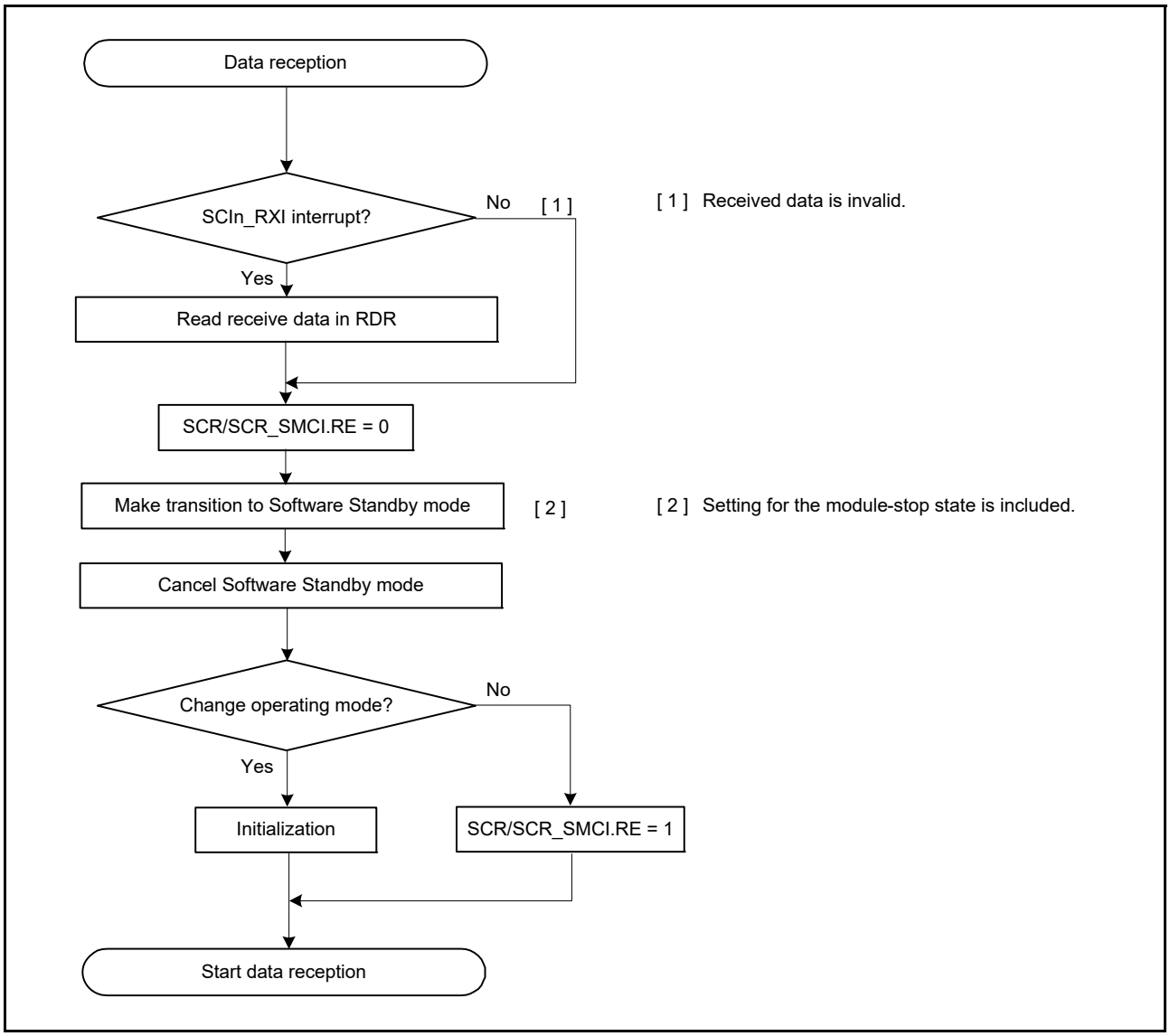


Figure 27.76 Example flow of transition to Software Standby mode during reception

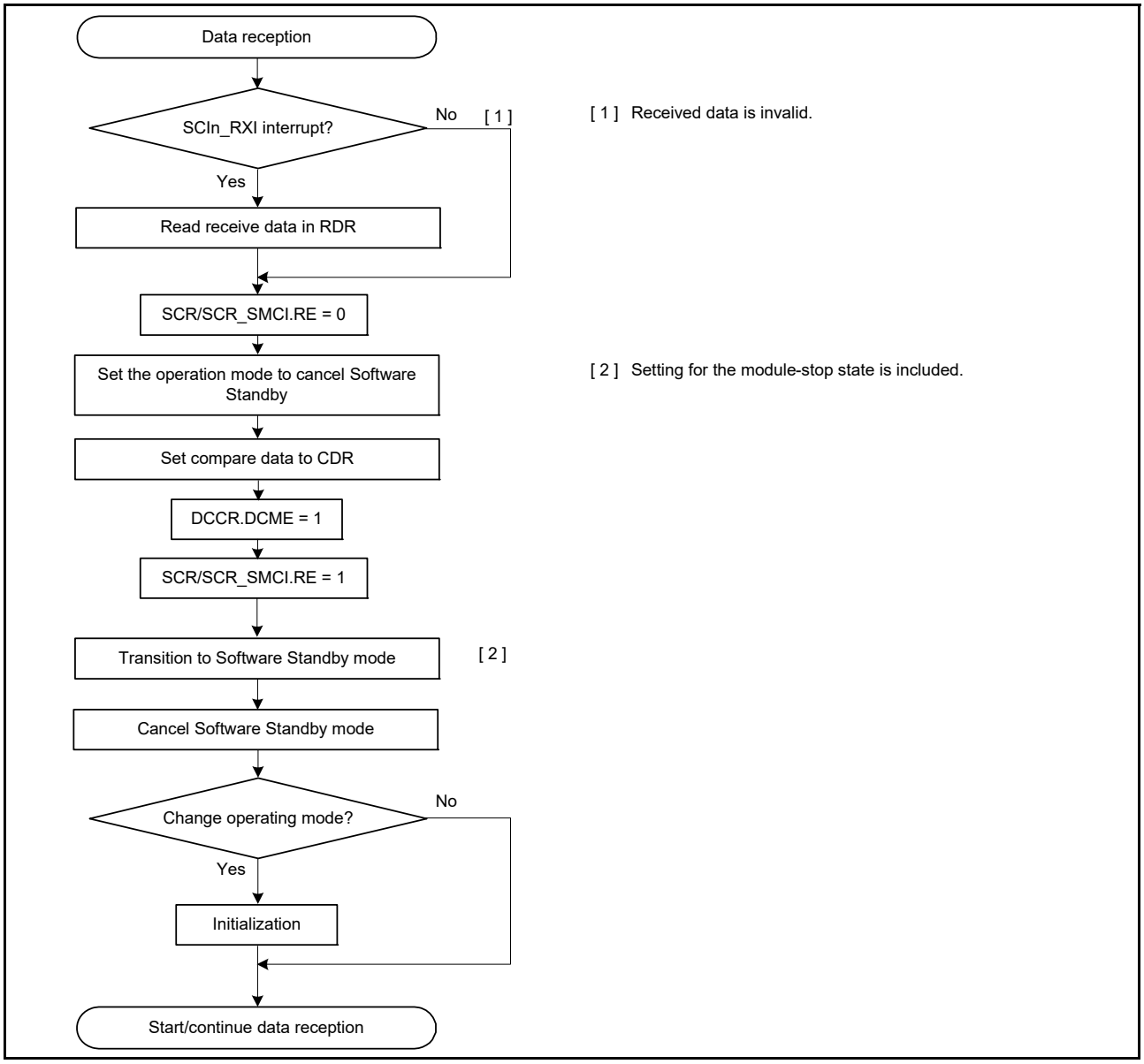


Figure 27.77 Example flow of transition to Software Standby mode during reception with address match

27.14.3 Break Detection and Processing

(1) Non-FIFO selected

When a framing error is detected, a break can be detected by reading the RXDn pin value directly. In a break, the input from the RXDn pin becomes all 0s, and the SSR.FER flag is set to 1 to indicate a framing error. The SSR.PER flag might also be set to 1 to indicate a parity error. The SCI continues the receive operation even after a break is received. Therefore, even if the FER flag is 0, indicating that no framing error occurred, it is set to 1 again. When the SEMR.RXDESEL bit is 1, the SCI sets the SSR.FER flag to 1 and stops the receiving operations until a start bit of the next data frame is detected. If the SSR.FER flag is set to 0, the SSR.FER flag retains 0 during the break.

When the RXDn pin is set to 1 and the break ends, detecting the beginning of the start bit on the first falling edge of the RXDn pin allows the SCI to start the receiving operation.

(2) FIFO selected

After a framing error is detected and when the SCI detects that continuous receive data is 0 for one frame, reception stops. When a framing error is detected, a break can be detected by reading the SPTR.RXDMON bit value. After the RXD signal is in the mark state and the break ends, data reception to the FRDRHL register resumes.

27.14.4 Mark State and Production of Breaks

When the SCR/SCR_SMCI.TE bit is 0, disabling serial transmission, the state of the TXDn pin can be set using the SPTR.SPB2IO and SPTR.SPB2DT bits. With this approach, a TXDn pin can be placed in the mark state to transmit a break.

Before setting the SCR/SCR_SMCI.TE bit to 1, enabling serial transmission, set the SPB2IO and SPB2DT bits to put the communication line in the mark state (the state of 1), and change the TxDn pin using the I/O port function. To output a break on data transmission, after setting the TXDn pin to output 0 by setting the SPB2IO and SPB2DT bits, change the TXDn pin using the I/O port function and set the SCR/SCR_SMCI.TE bit to 0. When the SCR/SCR_SMCI.TE bit is set to 0, the transmitter is initialized regardless of the current state of transmission.

27.14.5 Receive Error Flags and Transmit Operation in Clock Synchronous and Simple SPI Modes

Transmission cannot start when a receive error flag (ORER) in SSR/SSR_FIFO is set to 1, even if data is written to TDR or FTDRL*1. Be sure to set the receive error flags to 0 before starting transmission.

Note: The receive error flags cannot be set to 0 when serial reception is disabled by setting the RE bit in SCR/SCR_SMCI to 0.

Note 1. Do not use the FTDRH register in simple SPI mode.

27.14.6 Restrictions on Clock Synchronous Transmission in Clock Synchronous Mode and Simple SPI Mode

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Wait at least the following time from writing transmit data to TDR to the start of the external clock input:

1 PCLKA cycle + data output delay time for the slave (t_{DO}) + setup time for the master (t_{SU}).

See Figure 27.78.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock for bit [7]. See Figure 27.78.

When updating TDR after bit [7] starts to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock, bit [7] (D7) to 4 PCLKA cycles or longer. See Figure 27.78.

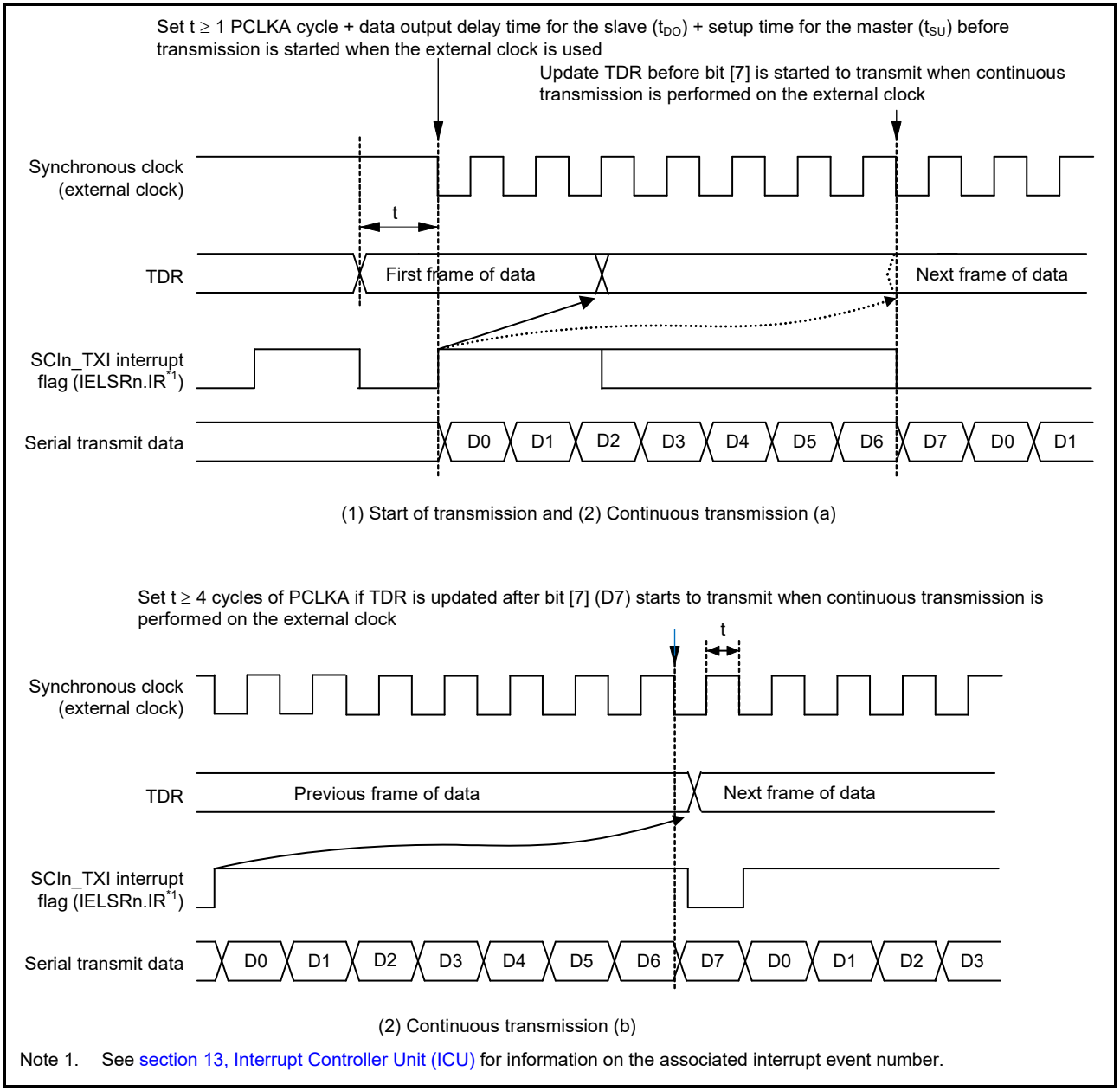


Figure 27.78 Restrictions on the use of external clock in clock synchronous transmission

27.14.7 Restrictions on Using DMAC or DTC

During transmission or reception operations using the DMAC or DTC, do not set transfer data for the DMAC/DTC.

(1) Writing data to TDR (FTDRHL)

(a) Non-FIFO selected

Data can be written to TDR and TDRHL. However, if new data is written to TDR or TDRHL when transmit data remains in TDR or TDRHL, the previous data in TDR and TDRHL is lost because it was not yet transferred to TSR. When using DMAC or DTC, be sure to write transmit data to TDR or TDRHL in the SCIn_TXI interrupt request handling routine.

(b) FIFO selected

It is possible to write data to the FTDRH and FTDRL registers when SCR.TE is 1. Confirm the amount of writable data using the FDR.T[4:0] bits.

(2) Reading data from RDR (FRDRHL)

When using the DMAC or DTC to read RDR and RDRHL, be sure to set the receive data full interrupt (SCIn_RXI) as the activation source of the relevant SCI channel.

27.14.8 Notes on Starting Transfer

When transfer starts while the Interrupt Status flag (IELSRn.IR) in the ICU is 1, follow the procedure in this section to clear interrupt requests before permitting operations (by setting the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit to 1).

For details on the Interrupt Status flag, see section 13, Interrupt Controller Unit (ICU).

1. Confirm that the transfer stopped (the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit is 0).
2. Set the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE) to 0.
3. Read the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE bit) to check that it is 0.
4. Set the Interrupt Status flag (IELSRn.IR) in the ICU to 0.

27.14.9 External Clock Input in Clock Synchronous Mode and Simple SPI Mode

In clock synchronous mode and simple SPI mode, the external clock (SCKn) must be input as follows:

High-pulse period, low-pulse period = 2 PCLKA cycles or more, period = 6 PCLKA cycles or more.

27.14.10 Limitations on Simple SPI Mode

(1) Master mode

- Use a resistor to pull up or pull down the clock line matching the initial settings for the transfer clock set in the SPMR.CKPH and CKPOL bits when the SPMR.SSE bit is 1. This prevents the clock line from being placed in the high-impedance state when the SCR.TE bit is set to 0 or unexpected edges from being generated on the clock line when the SCR.TE bit changes from 0 to 1. When the SPMR.SSE bit is 0 in single master mode, pulling up or pulling down the clock line is not required because the clock line is not placed in the high-impedance state even when the SCR.TE bit is set to 0.
- For the clock delay setting (SPMR.CKPH bit is 1), the receive data full interrupt (SCIn_RXI) is generated before the final clock edge on the SCKn pin, as indicated in Figure 27.79. If the TE and RE bits in the SCR register become 0 before the final edge of the clock signal on the SCKn pin, the SCKn pin is placed in the high-impedance state, so the width of the last clock pulse of the transfer clock is shortened. Additionally, an SCIn_RXI interrupt might lead to the input signal on the SSn pin of a connected slave going to the high level before the final edge of the clock signal on the SCKn pin, leading to incorrect operation of the slave.
- In a multi-master configuration, the SCKn pin output goes to high-impedance while the input on the SSn pin is at the low level if a mode fault error occurs while a character is being transferred, stopping supply of the clock signal to the connected slave. Reset the connected slave to avoid misaligned bits when transfer is restarted.

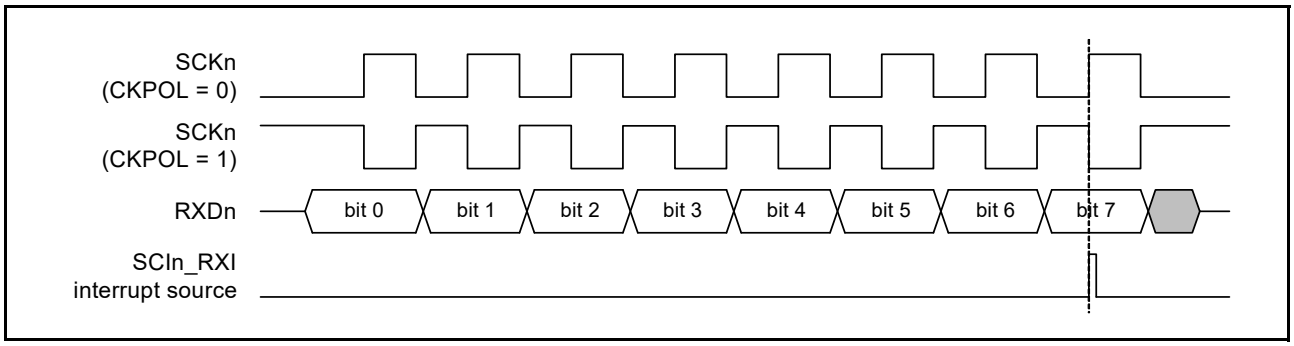


Figure 27.79 Timing of SCIn_RXI interrupt in simple SPI mode with clock delay

(2) Slave mode

- Wait at least the following time from writing transmit data in the TDR register to the start of the external clock input:
  1 PCLKA cycle + data output delay for the slave (t_{DO}) + setup time for the master (t_{SU}).
  Also, wait at least 5 PCLKA cycles from the input of the low level on the SSn pin to the start of the external clock input.
- Provide an external clock signal to the master for the data length for transfer
- Control the input on the SSn pin before the start and after the end of data transfer
- When the input level on the SSn pin changes from low to high while a character is being transferred, set the TE and RE bits in the SCR to 0 and, after restoring the settings, restart transfer of the first byte.

28. IrDA Interface

28.1 Overview

The IrDA interface sends and receives IrDA data communication waveforms in cooperation with SCI1, according to the IrDA (Infrared Data Association) standard 1.0.

Enabling the IrDA function using the IRE bit in the IRCR register allows the encoding and decoding of the TXD1 and RXD1 signals of the SCI1 to waveforms conforming to the IrDA standard 1.0 (IRTXD1 and IRRXD1 pins).

Connecting the waveforms to an infrared transmitter/receiver implements infrared data communication conforming to the IrDA standard 1.0 system.

With the IrDA standard 1.0 system, data transfer can be started at 9600 bps and the transfer rate can be changed whenever necessary. Because the IrDA interface cannot change the transfer rate automatically, the transfer rate must be changed through software.

Figure 28.1 shows the interaction between the IrDA interface and SCI1.

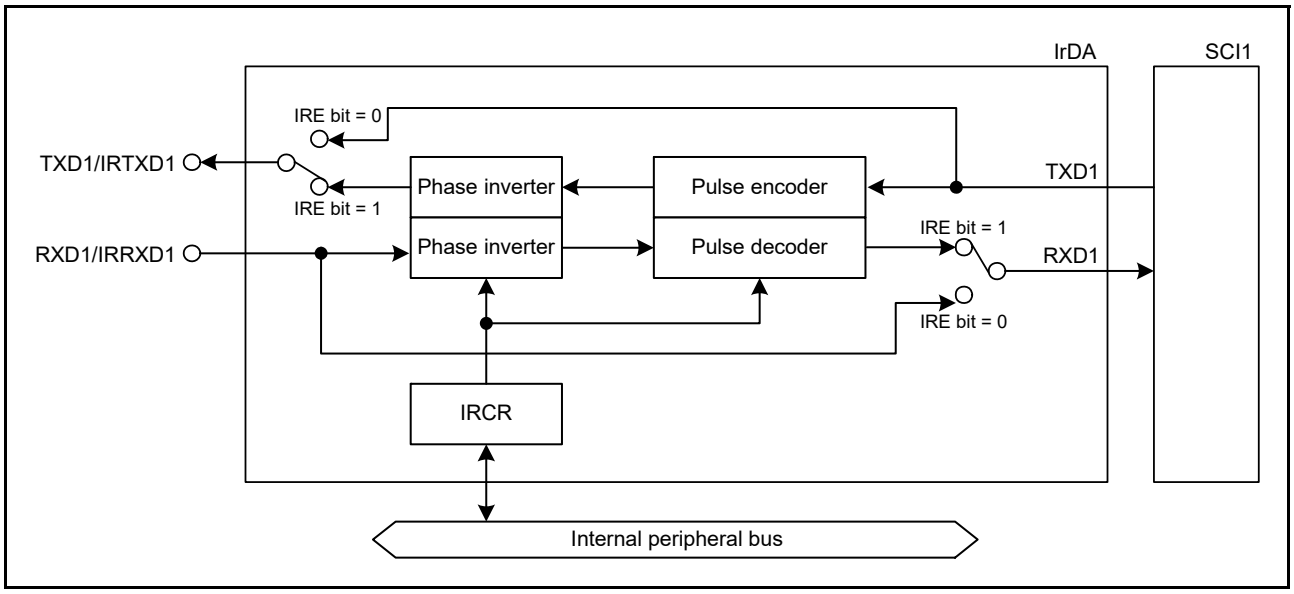


Figure 28.1 Interaction between the IrDA interface and SCI1

Table 28.1 IrDA interface I/O pins

Pin name	I/O	Function
IRTXD1	Output	Data to be transmitted
IRRXD1	Input	Received data

28.2 Register Descriptions

28.2.1 IrDA Control Register (IRCR)

Address(es): IRDA.IRCR 4007 0F00h

	b7	b6	b5	b4	b3	b2	b1	b0
	IRE	—	—	—	IRTXINV	IRRXINV	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	IRRXINV	IRRXD Polarity Switching	0: Use IRRXD input as received data as-is 1: Use IRRXD input as received data after the polarity is inverted.	R/W
b3	IRTXINV	IRTXD Polarity Switching	0: Output data to be transmitted to IRTXD as-is 1: Output data to be transmitted IRTXD after the polarity is inverted.	R/W
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	IRE	IrDA Enable	0: Use serial input/output pins for normal serial communication 1: Use serial input/output pins for IrDA data communication.	R/W

Note: The IRCR register values are retained in Sleep, Software Standby, and Deep Software Standby modes.

IRRXINV bit (IRRXD Polarity Switching)

The IRRXINV bit inverts the logic level of the IRRXD input. When inverted, the high-level pulse width is applied to the low-level pulse width.

IRTXINV bit (IRTXD Polarity Switching)

The IRTXINV bit inverts the logic level of the IRTXD output. When inverted, the high-level pulse width is applied to the low-level pulse width.

IRE bit (IrDA Enable)

The IRE bit configures the I/O pins for normal communication mode or IrDA data communication mode.

28.3 Operation

28.3.1 IrDA Interface Setup Procedure

To set up IrDA interface operation:

1. Set the associated pins to IRTXD1 and IRRXD1 in the Pin Function Control Register (PmnPFS.PSEL = 00101b) of the I/O ports function.
2. Specify the peripheral function in the Pin Function Control Register (PmnPFS.PMR = 1) of the I/O ports function.
3. Specify the IrDA function in the IRCR register.
4. Set the SCI1-related registers in the Serial Communications Interface (SCI).

28.3.2 Transmission

During transmission, the signals output from SCI1 (UART frames) are converted to IR frame data through the IrDA interface as shown in Figure 28.2. When the IRCR.IRTXINV bit is 0 and serial data is 0, high-level pulses with 3/16 the width of the bit rate (1-bit width period) are output (initial setting). The standard states that the minimum high-level pulse width must be 1.41 µs and the maximum high-level pulse width must be (3/16 + 2.5%) × bit rate or (3/16 × bit rate) + 1.08 µs. When the serial data is 1, no pulses are output.

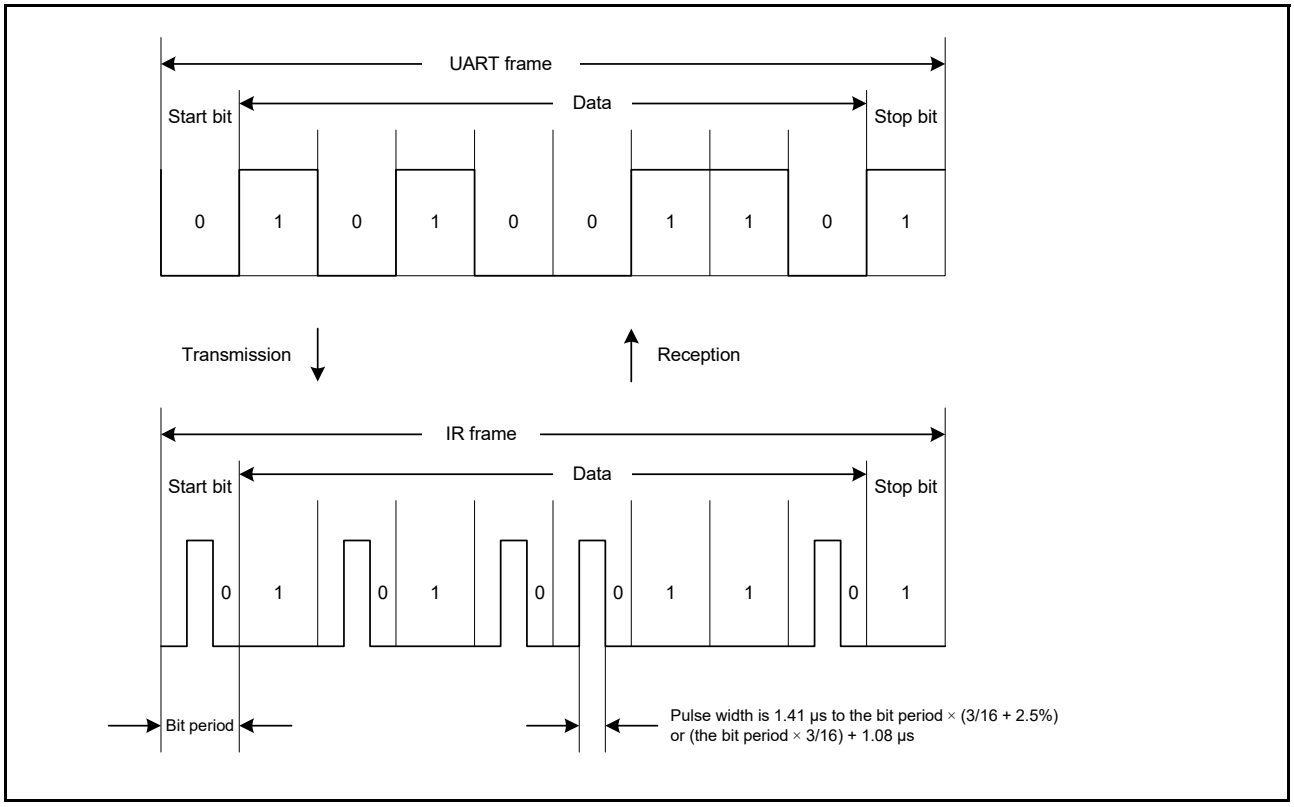


Figure 28.2 IrDA transmission and reception

28.3.3 Reception

During reception, IR frame data is converted to UART frame data through the IrDA interface and is input to SCI1.

Low-level data is input to SCI1 when the IRCR.IRRXINV bit is 0 and a high-level pulse is detected. High-level data is input to SCI1 when no pulse is detected for a 1-bit period.

28.4 Usage Notes

28.4.1 Settings for the Module-Stop State

IrDA operation can be enabled or disabled using the Module Stop Control Register. IrDA is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

28.4.2 Asynchronous Reference Clock for SCI1

The IrDA receives a clock with frequency 16 times the bit rate from SCI1 and operates in conjunction with SCI1.

When using the IrDA, set the SCI1.SEMR.ABCS bit to 0.

29. I2C Bus Interface (IIC)

29.1 Overview

The MCU has a 2-channel I2C Bus Interface (IIC) module that conforms with and provides a subset of the NXP I2C bus (Inter-Integrated Circuit) bus interface functions.

Table 29.1 lists the IIC specifications, Figure 29.1 shows a block diagram, and Figure 29.2 shows an example of I/O pin connections to external circuits, with an I2C bus configuration. Table 29.2 lists the I/O pins.

Table 29.1 IIC specifications (1 of 2)

Parameter	Specifications
Communications format	• I2C bus format or SMBus format • Master or slave mode selectable • Automatic securing of the setup times, hold times, and bus-free times for the transfer rate.
Transfer rate	Fast mode plus supported, up to 1 Mbps
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated • Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Configurable for up to three different slave addresses • 7-bit and 10-bit address formats supported, including simultaneous use • General call addresses, device ID addresses, and SMBus host addresses detectable.
Acknowledgment	• For transmission, automatic loading of the acknowledge bit. Transfer of the next transmit data can be automatically suspended on detection of a not-acknowledge bit. • For reception, automatic transmission of the acknowledge bit. If a wait between the 8th and 9th clock cycles is selected, software can control the value in the acknowledge field in response to the received value.
Wait function	During reception, the following wait periods are available by holding the SCL clock low: • Waiting between the 8th and 9th clock cycles • Waiting between the 9th clock cycle and the 1st clock cycle of the next transfer.
SDA output delay function	Output timing of transmitted data, including the acknowledge bit, can be delayed
Arbitration	• For multi-master operation: - SCL clock synchronization is possible when conflict occurs with the SCL signal from another master - When issuing the start condition creates conflict on the bus, loss of arbitration is detected by testing for mismatching between the internal signal for the SDA line and the level on the SDA line - In master operation, loss of arbitration is detected by testing for mismatching between the signal on the SDA line and the internal signal for the SDA line • Loss of arbitration because the start condition occurs while the bus is busy is detectable, to prevent the issuing of double start conditions • Loss of arbitration is detectable on transfer of a not-acknowledge bit because the internal signal for the SDA line and the level on the SDA line do not match • Loss of arbitration because mismatching of internal and line levels for data is detectable in slave transmission
Timeout function	Internal detection of long-interval stops of the SCL clock
Noise cancellation	• Digital noise filters for both the SCL and SDA signals • Programmable window for noise cancellation by the filters.
Interrupt sources	• Transfer error or event occurrence (arbitration detection, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end.
Module-stop function	Module-stop state can be set to reduce power consumption
IIC operating modes	• Master transmit • Master receive • Slave transmit • Slave receive.

Table 29.1 IIC specifications (2 of 2)

Parameter	Specifications
Event link function (output)	• Transfer error or event occurrence (arbitration detection, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end.
Wakeup function*1	CPU can return from Software Standby mode using a wakeup event

Note 1. This function is only available for IIC channel IIC0. IIC1 is not supported.

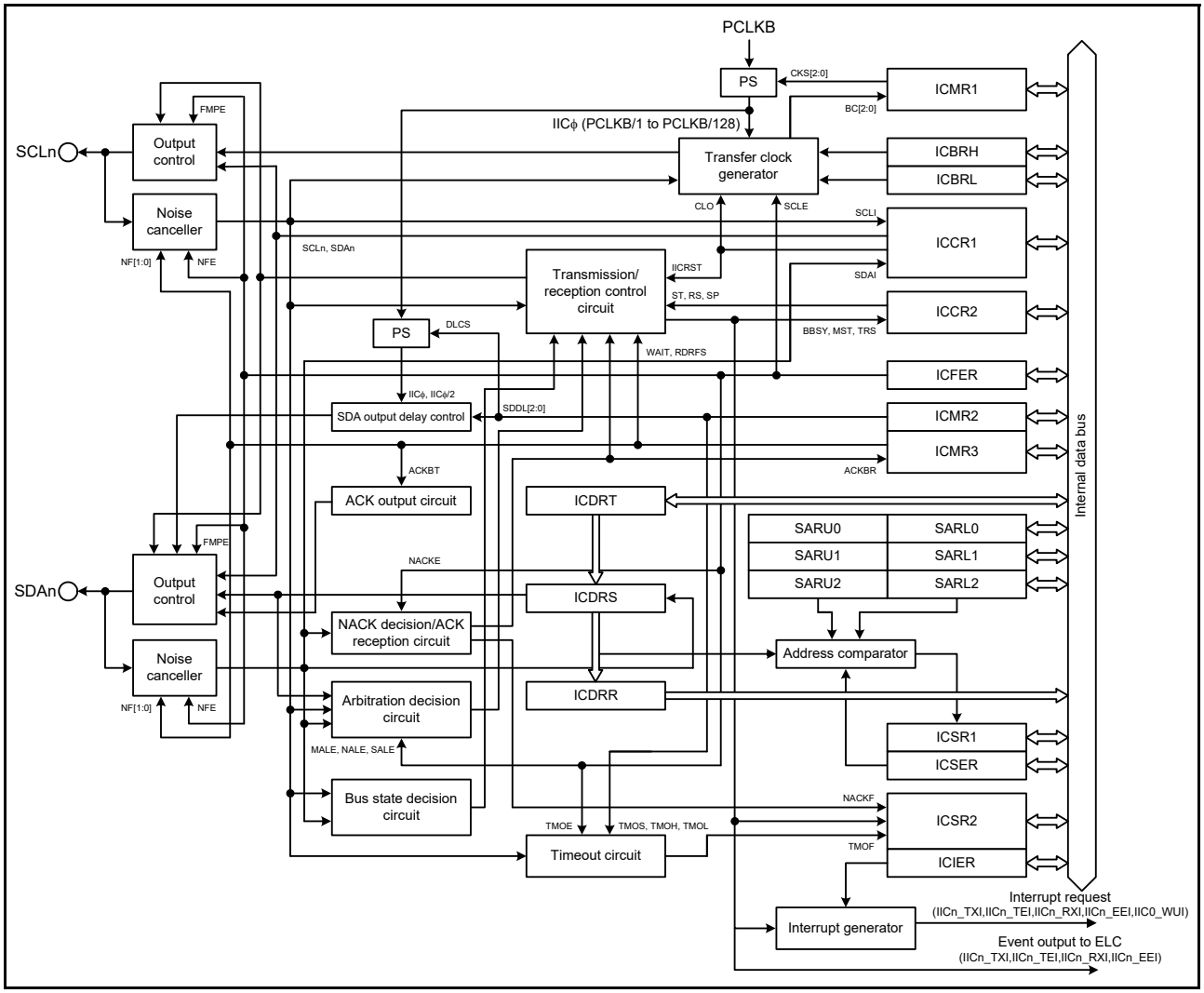


Figure 29.1 IIC block diagram

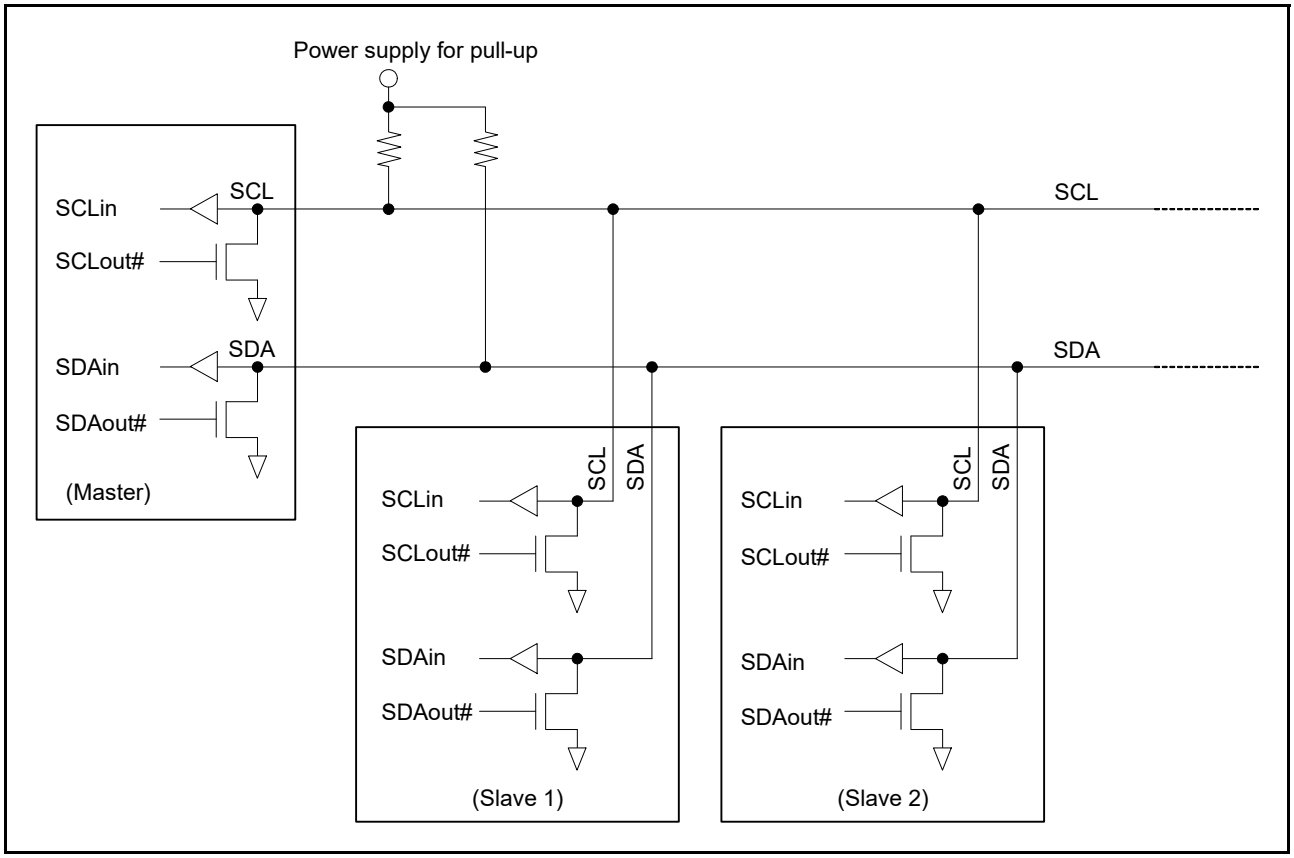


Figure 29.2 I/O pin connection to an external circuit (I2C bus configuration example)

The input level of the signals for IIC is CMOS when I2C bus is selected (ICMR3.SMBS = 0), or TTL when SMBus is selected (ICMR3.SMBS = 1).

Table 29.2 IIC I/O pins

Channel	Pin name	I/O	Function
IIC0	SCL0	I/O	IIC0 serial clock I/O pin
	SDA0	I/O	IIC0 serial data I/O pin
IIC1	SCL1	I/O	IIC1 serial clock I/O pin
	SDA1	I/O	IIC1 serial data I/O pin

29.2 Register Descriptions

29.2.1 I2C Bus Control Register 1 (ICCR1)

Address(es): IIC0.ICCR1 4005 3000h, IIC1.ICCR1 4005 3100h

	b7	b6	b5	b4	b3	b2	b1	b0
	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	SDAI	SDA Line Monitor	0: SDAn line is low 1: SDAn line is high.	R

Bit	Symbol	Bit name	Description	R/W
b1	SCLI	SCL Line Monitor	0: SCLn line is low 1: SCLn line is high.	R
b2	SDAO	SDA Output Control/Monitor	• Read: 0: IIC drives SDAn pin low 1: IIC releases SDAn pin. • Write: 0: IIC drives SDAn pin low 1: IIC releases SDAn pin.	R/W
b3	SCLO	SCL Output Control/Monitor	• Read: 0: IIC drives SCLn pin low 1: IIC releases SCLn pin. • Write: 0: IIC drives SCLn pin low 1: IIC releases SCLn pin. Use an external pull-up resistor to drive the signal high.	R/W
b4	SOWP	SCLO/SDAO Write Protect	0: Write enable SCLO and SDAO bits 1: Write protect SCLO and SDAO bits. This bit is read as 1.	R/W
b5	CLO	Extra SCL Clock Cycle Output	0: Do not output extra SCL clock cycle (default) 1: Output extra SCL clock cycle. This bit clears automatically after 1 clock cycle is output.	R/W
b6	IICRST	IIC-Bus Interface Internal Reset	0: Release IIC reset or internal reset 1: Initiate IIC reset or internal reset. This setting clears the bit counter and the SCLn/SDAn output latch.	R/W
b7	ICE	IIC-Bus Interface Enable	0: Disable (SCLn and SDAn pins in inactive state) 1: Enable (SCLn and SDAn pins in active state). Used in combination with the IICRST bit to select either IIC or internal reset.	R/W

SDAO bit (SDA Output Control/Monitor) and SCLO bit (SCL Output Control/Monitor)

The SDAO and SCLO bits directly control the SDAn and SCLn signals output from the IIC.

When writing to these bits, also write 0 to the SOWP bit. Setting these bits results in input to the IIC by the input buffer. When slave mode is selected, a start condition might be detected and the bus might be released, depending on the bit settings.

Do not rewrite these bits during a start condition, stop condition, restart condition, or during transmission, or reception. Operation after rewriting under the specified conditions is not guaranteed. When reading these bits, the state of signals output from the IIC can be read.

CLO bit (Extra SCL Clock Cycle Output)

The CLO bit allows output of an extra SCL clock cycle for debugging or error processing. Normally, set this bit to 0. Setting this bit to 1 in a normal communication state causes a communication error. For details on this function, see section 29.12.2, Extra SCL Clock Cycle Output Function.

IICRST bit (IIC-Bus Interface Internal Reset)

The IICRST bit initiates an internal state reset of the IIC. Setting this bit to 1 initiates an IIC reset or internal reset. Whether an IIC reset or internal reset is initiated is determined by setting this bit in combination with the ICE bit. Table 29.3 lists the IIC resets.

The IIC reset initializes all registers except ICCR1.ICE and ICCR1.IICRST bits, and internal states of the IIC. In addition to the internal states of the IIC, the internal reset initializes the following:

- Bit counter (ICMR1.BC[2:0] bits)
- I2C Bus Shift Register (ICDRS)
- I2C Bus Status Registers (ICSR1 and ICSR2)
- SDAO and SCLO Output Control/Monitor (ICCR1.SCLO and ICCR1.SDAO bits)
- I2C Bus Control Register 2 (except ICCR2.BBSY bit).

For the reset conditions of each register, see section 29.15, State of Registers when Issuing each Condition.

An internal reset initiated with the IICRST bit set to 1 during operation (with the ICE bit set to 1) resets the internal states of the IIC without initializing the port settings and the control and setting registers of the IIC. If the IIC hangs up in a low level output state, resetting the internal states cancels the low level output state and releases the bus with the SCLn pin and SDAn pin at high impedance.

Note: If an internal reset is initiated using the IICRST bit for a bus hang-up that occurs during communication with the master device in slave mode, the slave and master devices might enter different states, because the bit counter information differs. For this reason, do not initiate an internal reset in slave mode. Initiate recovery processing from the master device. If an internal reset is required because the IIC hangs with the SCLn line in a low level output state in slave mode, initiate an internal reset, then issue a restart condition from the master device, or issue a stop condition and resume communication from the start condition. If communication is restarted by initiating a reset solely in the slave device without issuing a start or restart condition from the master device, synchronization is lost because the master and slave devices operate asynchronously.

Table 29.3 IIC resets

IICRST	ICE	State	Specifications
1	0	IIC reset	Resets all registers except ICCR1.ICE and ICCR1.IICRST bits, and the internal states of the IIC
	1	Internal reset	Resets the following: • ICMR1.BC[2:0] bits • ICSR1, ICSR2, ICDRS registers • SDAO and SCLO Output Control/Monitor (ICCR1.SCLO and ICCR1.SDAO bits) • I2C Bus Control Register 2 (except ICCR2.BBSY bit) • Internal states of the IIC.

ICE bit (IIC-Bus Interface Enable)

The ICE bit selects the active or inactive state of the SCLn and SDAn pins. It can also be combined with the IICRST bit to initiate one of two types of resets. See Table 29.3 for the reset types.

Set the ICE bit to 1 when using the IIC. The SCLn and SDAn pins are placed in the active state when the ICE bit is set to 1. Set the ICE bit to 0 when the IIC is not used. The SCLn and SDAn pins are placed in the inactive state when the ICE bit is set to 0. Do not assign the SCLn or SDAn pin to the IIC when setting up the pin function control. Slave address comparison is performed if the pins are assigned to the IIC.

29.2.2 I2C Bus Control Register 2 (ICCR2)

Address(es): IIC0.ICCR2 4005 3001h, IIC1.ICCR2 4005 3101h

	b7	b6	b5	b4	b3	b2	b1	b0
	BBSY	MST	TRS	—	SP	RS	ST	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	ST	Start Condition Issuance Request	0: Do not issue a start condition request 1: Issue a start condition request.	R/W
b2	RS	Restart Condition Issuance Request	0: Do not issue a restart condition request 1: Issue a restart condition request.	R/W
b3	SP	Stop Condition Issuance Request	0: Do not issue a stop condition request 1: Issue a stop condition request.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	TRS	Transmit/Receive Mode	0: Receive mode 1: Transmit mode.	R/W*1

Bit	Symbol	Bit name	Description	R/W
b6	MST	Master/Slave Mode	0: Slave mode 1: Master mode.	R/W*1
b7	BBSY	Bus Busy Detection Flag	0: I2C bus released (bus free state) 1: I2C bus occupied (bus busy state).	R

Note 1. The MST and TRS bits can be written to when the ICMR1.MTWP bit is set to 1.

ST bit (Start Condition Issuance Request)

The ST bit requests transition to master mode and triggers a start condition.

When this bit is set to 1, a start condition is issued when the BBSY flag is set to 0 (bus free state). For details on issuing a start condition, see section 29.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the ST bit.

[Clearing conditions]

- When 0 is written to the ST bit
- When a start condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Only set the ST bit to 1 (start condition request) when the BBSY flag is set to 0 (bus free state). Arbitration might be lost if the ST bit is set to 1 when the BBSY flag is 1 (bus busy state).

RS bit (Restart Condition Issuance Request)

The RS bit requests that a restart condition be issued in master mode.

When this bit is set to 1 to request a restart condition, a restart condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on issuing a restart condition, see section 29.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the RS bit with the BBSY flag in ICCR2 set to 1.

[Clearing conditions]

- When 0 is written to the RS bit
- When a restart condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Do not set the RS bit to 1 while issuing a stop condition.
Note: If 1 (restart condition request) is written to the RS bit in slave mode, the restart condition is not issued, but the RS bit remains set to 1. If the operating mode changes to master mode without the bit being cleared, a restart condition might be issued.

SP bit (Stop Condition Issuance Request)

The SP bit requests that a stop condition be issued in master mode.

When this bit is set to 1, a stop condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on this function, see section 29.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the SP bit with both the BBSY flag and the MST bit in ICCR2 set to 1.

[Clearing conditions]

- When 0 is written to the SP bit
- When a stop condition is issued (a stop condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When a start condition and a restart condition are detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Writing to the SP bit is not possible when the BBSY flag is 0 (bus free state).
Note: Do not set the SP bit to 1 when a restart condition is being issued.

TRS bit (Transmit/Receive Mode)

The TRS bit indicates transmit or receive mode.

The IIC is in receive mode when the TRS bit is 0 and in transmit mode when the bit is 1. The combination of the TRS bit and the MST bit indicates the IIC operating mode.

The value of the TRS bit automatically changes to 1 for transmit mode or 0 for receive mode when a start condition is issued or detected and the R/W# bit is set. Although writing to the TRS bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not required during normal usage.

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When a restart condition is issued normally because of a restart condition request (when a restart condition is detected with the RS bit set to 1)
- When the R/W# bit appended to the slave address is set to 0 in master mode
- When the address received in slave mode matches the address enabled in ICSER, with the R/W# bit set to 1
- When 1 is written to the TRS bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When the R/W# bit appended to the slave address is set to 1 in master mode
- In slave mode, on a match between the received address and the address enabled in ICSER when the value of the received R/W# bit is 0, including when the received address is the general call address
- In slave mode, when a restart condition is detected (a start condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)
- When 0 is written to the TRS bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

MST bit (Master/Slave Mode)

The MST bit indicates master or slave mode. The IIC is in slave mode when the MST bit is set to 0 and is in master mode when the bit is set to 1. The combination of the MST bit and the TRS bit indicates the IIC operating mode.

The value of the MST bit automatically changes to 1 for master mode or 0 for slave mode when a start condition is issued, or when a stop condition is issued or detected. Although writing to the MST bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not required during normal usage.

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)

- When 1 is written to the MST bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 0 is written to the MST bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

BBSY flag (Bus Busy Detection Flag)

The BBSY flag indicates whether the I2C bus is occupied (bus busy state) or released (bus free state).

This flag is set to 1 when the SDAn line changes from high to low with the SCLn line is high, assuming that a start condition was issued.

This flag is set to 0 when the SDAn line changes from low to high with the SCLn line high, if the bus free time (ICBRL setting) start condition is not detected, assuming that a stop condition was issued.

[Setting condition]

- When a start condition is detected.

[Clearing conditions]

- When the bus free time (ICBRL register setting) start condition is not detected after detecting a stop condition
- When 1 is written to the IICRST bit in ICCR1 with the ICE bit in ICCR1 set to 0 (IIC reset).

29.2.3 I2C Bus Mode Register 1 (ICMR1)

Address(es): IIC0.ICMR1 4005 3002h, IIC1.ICMR1 4005 3102h

	b7	b6	b5	b4	b3	b2	b1	b0
	MTWP	CKS[2:0]			BCWP	BC[2:0]		
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	BC[2:0]	Bit Counter	b2 b0 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits.	R/W*1
b3	BCWP	BC Write Protect	0: Write enable BC[2:0] bits 1: Write protect BC[2:0] bits. This bit is read as 1.	R/W*1
b6 to b4	CKS[2:0]	Internal Reference Clock Select	Select the internal reference clock source (IICϕ) for the IIC. b6 b4 0 0 0: PCLKB clock 0 0 1: PCLKB/2 clock 0 1 0: PCLKB/4 clock 0 1 1: PCLKB/8 clock 1 0 0: PCLKB/16 clock 1 0 1: PCLKB/32 clock 1 1 0: PCLKB/64 clock 1 1 1: PCLKB/128 clock.	R/W
b7	MTWP	MST/TRS Write Protect	0: Write protect MST and TRS bits in ICCR2 1: Write enable MST and TRS bits in ICCR2.	R/W

Note 1. Rewrite the BC[2:0] bits and set the BCWP bit to 0 at the same time.

BC[2:0] bits (Bit Counter)

The BC[2:0] bits function as a counter that indicates the number of bits remaining to be transferred on detection of a rising edge on the SCLn line. Although BC[2:0] are read/write bits, it is not required to access these bits under normal conditions.

To write to these bits, specify the number of bits to be transferred plus one, for an additional acknowledge bit, between transferred frames when the SCLn line is at a low level.

The value in the BC[2:0] bits returns to 000b at the end of a data transfer, including the acknowledge bit, or when a start or restart condition is detected.

29.2.4 I2C Bus Mode Register 2 (ICMR2)

Address(es): IIC0.ICMR2 4005 3003h, IIC1.ICMR2 4005 3103h

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
Value after reset:	0	0	0	0	0	1	1	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOS	Timeout Detection Time Select	0: Select long mode 1: Select short mode.	R/W
b1	TMOL	Timeout L Count Control	0: Disable count while SCLn line is low 1: Enable count while SCLn line is low.	R/W
b2	TMOH	Timeout H Count Control	0: Disable count while SCLn line is high 1: Enable count while SCLn line is high.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	SDDL[2:0]	SDA Output Delay Counter	• When ICMR2.DLCS = 0 (IICϕ) b6 b4 0 0 0: No output delay 0 0 1: 1 IICϕ cycle 0 1 0: 2 IICϕ cycles 0 1 1: 3 IICϕ cycles 1 0 0: 4 IICϕ cycles 1 0 1: 5 IICϕ cycles 1 1 0: 6 IICϕ cycles 1 1 1: 7 IICϕ cycles. • When ICMR2.DLCS = 1 (IICϕ/2) b6 b4 0 0 0: No output delay 0 0 1: 1 or 2 IICϕ cycles 0 1 0: 3 or 4 IICϕ cycles 0 1 1: 5 or 6 IICϕ cycles 1 0 0: 7 or 8 IICϕ cycles 1 0 1: 9 or 10 IICϕ cycles 1 1 0: 11 or 12 IICϕ cycles 1 1 1: 13 or 14 IICϕ cycles.	R/W
b7	DLCS	SDA Output Delay Clock Source Select	0: Internal reference clock (IICϕ) selected as the clock source for SDA output delay counter 1: Internal reference clock divided by 2 (IICϕ/2) selected as the clock source for SDA output delay counter.*1	R/W

Note 1. The setting DLCS = 1 (IICϕ/2) is only valid when SCL is low. When SCL is high, the DLCS = 1 setting is invalid and the clock source becomes the internal reference clock (IICϕ).

TMOS bit (Timeout Detection Time Select)

The TMOS bit selects long or short mode for the timeout detection time when the timeout function is enabled (ICFER.TMOE = 1).

When this bit is set to 0, long mode is selected. When it is set to 1, short mode is selected.

In long mode, the timeout detection internal counter functions as a 16 bit-counter. In short mode, the counter functions as a 14-bit counter. While the SCLn line is in the state that enables this counter as specified in the TMOH and TMOL bits, the counter counts up in synchronization with the internal reference clock (IICϕ) as a count source.

For details on this function, see section 29.12.1, Timeout Function.

TMOL bit (Timeout L Count Control)

The TMOL bit enables or disables up-counting on the internal counter of the timeout function while the SCLn line is held low and the timeout function is enabled (ICFER.TMOE = 1).

TMOH bit (Timeout H Count Control)

The TMOH bit enables or disables up-counting on the internal counter of the timeout function while the SCLn line is held high and the timeout function is enabled (ICFER.TMOE = 1).

SDDL[2:0] bits (SDA Output Delay Counter)

The SDDL[2:0] bits can be used to delay the SDA output. This counter works with the clock source selected in the DLCS bit. The SDDL[2:0] setting can be used for all types of SDA output, including the transmission of the acknowledge bit.

Set the SDA output delay to meet the I2C bus standard for the data enable time/acknowledge enable time*1, or the SMBus standard, within [data hold time (300 ns or more + the SCL clock low-level period) - the data setup time (250 ns)]. If a value outside the standard is set, communication between the devices might malfunction or falsely indicate a start or stop condition, depending on the bus state.

For details on this function, see section 29.5, SDA Output Delay Function.

Note 1. Data enable time/acknowledge enable time
3,450 ns for up to 100 kbps: Standard mode (Sm)
900 ns for up to 400 kbps: Fast mode (Fm)
450 ns for up to 1 Mbps: Fast mode plus (Fm+).

29.2.5 I2C Bus Mode Register 3 (ICMR3)

Address(es): IIC0.ICMR3 4005 3004h, IIC1.ICMR3 4005 3104h

	b7	b6	b5	b4	b3	b2	b1	b0
	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	NF[1:0]	Noise Filter Stage Select	b1 b0 0 0: Filter out noise of up to 1 IICϕ cycle (single-stage filter) 0 1: Filter out noise of up to 2 IICϕ cycles (2-stage filter) 1 0: Filter out noise of up to 3 IICϕ cycles (3-stage filter) 1 1: Filter out noise of up to 4 IICϕ cycles (4-stage filter).	R/W
b2	ACKBR	Receive Acknowledge	0: 0: Received as the acknowledge bit (ACK reception) 1: 1: Received as the acknowledge bit (NACK reception).	R
b3	ACKBT	Transmit Acknowledge	0: Send 0 as the acknowledge bit (ACK transmission) 1: Send 1 as the acknowledge bit (NACK transmission).	R/W*1
b4	ACKWP	ACKBT Write Protect	0: Write protect ACKBT bit 1: Write enable ACKBT bit.	R/W*1
b5	RDRFS	RDRF Flag Set Timing Select	0: Set the RDRF flag on the rising edge of the 9th SCL clock cycle. The SCLn line is not held low on the falling edge of the 8th clock cycle 1: Set the RDRF flag on the rising edge of the 8th SCL clock cycle. The SCLn line is held low on the falling edge of the 8th clock cycle. Low-hold is released by writing to ACKBT.	R/W*2

Bit	Symbol	Bit name	Description	R/W
b6	WAIT	WAIT	0: No wait The period between 9th clock cycle and first clock cycle is not held low 1: Wait The period between 9th clock cycle and first clock cycle is held low. Low-hold is released by reading ICDRR.	R/W*2
b7	SMBS	SMBus/IIC-Bus Select	0: I2C bus selected 1: SMBus selected.	R/W

Note 1. Write to the ACKBT bit only when the ACKWP bit is 1. If the application writes 1 to both the ACKWP and ACKBT bits at the same time, the ACKBT bit is not set to 1.
Note 2. The WAIT and RDRFS bits are only valid in receive mode (invalid in transmit mode).

NF[1:0] bits (Noise Filter Stage Select)

The NF[1:0] bits select the number of stages in the digital noise filter.

For details on this function, see section 29.6, Digital Noise Filter Circuits.

Note: Set the noise range to be filtered out by the noise filter within a range less than the SCLn line high-level period or low-level period. If the noise range is set to a value of [SCL clock width: high-level period or low-level period, whichever is shorter] - [1.5 internal reference clock (IICϕ) cycles + analog noise filter: 120 ns (reference values)] or more, the SCL clock is regarded as noise by the noise filter function of the IIC, which might prevent the IIC from operating normally.

ACKBR bit (Receive Acknowledge)

The ACKBR bit stores the acknowledge bit information received from the receive device in transmit mode.

[Setting condition]

- When 1 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1.

[Clearing conditions]

- When 0 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (IIC reset).

ACKBT bit (Transmit Acknowledge)

The ACKBT bit sets the acknowledge bit to be sent in receive mode.

[Setting condition]

- When 1 is written to this bit with the ACKWP bit set to 1.

[Clearing conditions]

- When 0 is written to this bit with the ACKWP bit set to 1
- When stop condition request is detected with the SP bit in ICCR2 set to 1
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (IIC reset).

ACKWP bit (ACKBT Write Protect)

The ACKWP bit controls write enabling of the ACKBT bit.

RDRFS bit (RDRF Flag Set Timing Select)

The RDRFS bit selects the RDRF flag set timing in receive mode and also selects whether to hold the SCLn line low on the falling edge of the 8th SCL clock cycle.

When the RDRFS bit is 0, the SCLn line is not held low on the falling edge of the 8th SCL clock cycle, and the RDRF flag is set to 1 on the rising edge of the 9th SCL clock cycle.

When the RDRFS bit is 1, the RDRF flag is set to 1 on the rising edge of the 8th SCL clock cycle, and the SCLn line is held low on the falling edge of the 8th SCL clock cycle. The low-hold of the SCLn line is released by a write to the

ACKBT bit.

After data is received with this setting, the SCLn line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKBT = 0) or NACK (ACKBT = 1), based on the receive data.

WAIT bit (WAIT)

The WAIT bit controls whether to forcefully hold the period between the 9th SCL clock cycle and the 1st SCL clock cycle low until the receive data buffer (ICDRR) is completely read each time a single-byte data is received in receive mode.

When the WAIT bit is 0, the receive operation continues without holding the period between the 9th and the 1st SCL clock cycle low. When both the RDRFS and WAIT bits are 0, continuous receive operation is enabled with the double buffer.

When the WAIT bit is 1, the SCLn line is held low from the falling edge of the 9th clock cycle until the ICDRR value is read each time a single-byte data is received. This enables the receive operation in byte units.

Note: When the value of the WAIT bit is to be read, be sure to first read the ICDRR register first.

SMBS bit (SMBus/IIC-Bus Select)

Setting the SMBS bit to 1 selects the SMBus and enables the HOAE bit in ICSER.

29.2.6 I2C Bus Function Enable Register (ICFER)

Address(es): IIC0.ICFER 4005 3005h, IIC1.ICFER 4005 3105h

	b7	b6	b5	b4	b3	b2	b1	b0
	FMPE	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
Value after reset:	0	1	1	1	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOE	Timeout Function Enable	0: Timeout function disabled 1: Timeout function enabled.	R/W
b1	MALE	Master Arbitration-Lost Detection Enable	0: Master arbitration-lost detection disabled. Also disables automatic clearing of the MST and TRS bits in ICCR2 when arbitration is lost. 1: Master arbitration-lost detection enabled. Also enables automatic clearing of the MST and TRS bits in ICCR2 when arbitration is lost.	R/W
b2	NALE	NACK Transmission Arbitration-Lost Detection Enable	0: NACK transmission arbitration-lost detection disabled 1: NACK transmission arbitration-lost detection enabled.	R/W
b3	SALE	Slave Arbitration-Lost Detection Enable	0: Slave arbitration-lost detection disabled 1: Slave arbitration-lost detection enabled.	R/W
b4	NACKE	NACK Reception Transfer Suspension Enable	0: Transfer operation not suspended during NACK reception (transfer suspension disabled) 1: Transfer operation suspended during NACK reception (transfer suspension enabled).	R/W
b5	NFE	Digital Noise Filter Circuit Enable	0: No digital noise filter circuit used 1: A digital noise filter circuit used.	R/W
b6	SCLE	SCL Synchronous Circuit Enable	0: No SCL synchronous circuit used 1: An SCL synchronous circuit used.	R/W
b7	FMPE*1	Fast Mode Plus Enable	0:The Fast mode plus slope control circuit for the SCLn and SDAn pins not used 1: The Fast mode plus slope control circuit for the SCLn and SDAn pins used.	R/W

Note 1. The Fast Mode Plus Enable bit (FMPE) is supported only by IIC0 (SCL0-A, SDA0-A). Bit [7] is reserved in IIC1.

TMOE bit (Timeout Function Enable)

The TMOE bit enables or disables the timeout function.

For details on this function, see section 29.12.1, Timeout Function.

MALE bit (Master Arbitration-Lost Detection Enable)

The MALE bit specifies whether to use the arbitration-lost detection function in master mode. For normal operation, set this bit to 1.

NALE bit (NACK Transmission Arbitration-Lost Detection Enable)

The NALE bit specifies whether to cause loss of arbitration when ACK is detected during the transmission of NACK in receive mode, for example, when slaves with the same address exist on the bus, or when two or more masters select the same slave device simultaneously with a different number of receive bytes.

SALE bit (Slave Arbitration-Lost Detection Enable)

The SALE bit specifies whether to cause loss of arbitration when a value different from the value being transmitted is detected on the bus in slave transmit mode, for example, when slaves with the same address exist on the bus, or when a mismatch with the transmit data occurs because of noise.

NACKE bit (NACK Reception Transfer Suspension Enable)

The NACKE bit specifies whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. For normal operation, set this bit to 1.

When NACK is received with the NACKE bit set to 1, the next transfer operation is suspended. When the NACKE bit is 0, the next transfer operation continues regardless of the received acknowledge content.

For details, see section 29.9.2, NACK Reception Transfer Suspension Function.

SCLE bit (SCL Synchronous Circuit Enable)

The SCLE bit specifies whether to synchronize the SCL clock with the SCL input clock. For normal operation, set this bit to 1.

When the SCLE bit is set to 0 (no SCL synchronous circuit used), the IIC does not synchronize the SCL clock with the SCLn input clock. With this setting, the IIC outputs the SCL clock with the transfer rate set in ICBRH and ICBRL, regardless of the SCLn line state. For this reason, if the bus load of the I2C bus line is much larger than the specification value, or if the SCLn clock output overlaps in multiple masters, a short-cycle SCL clock that does not meet the specification might be output. When no SCL synchronous circuit is used, it also affects the issuing of the start, restart, and stop conditions, and the continuous output of extra SCL clock cycles.

Do not set the SCLE bit to 0 except when checking the output of the set transfer rate.

FMPE bit (Fast Mode Plus Enable)

The FMPE bit specifies whether to use a slope control circuit for Fast mode plus (Fm+).

When this bit is set to 1, a slope control circuit conforming to the I2C bus Fast mode plus (Fm+) standard (tof) is selected. When this bit is set to 0, a slope control circuit conforming to the I2C bus Standard mode (Sm) and Fast mode (Fm) standards (tof) is selected.

Set this bit to 1 when using transmission rates up to 1 Mbps (Fast mode plus (Fm+) standard). Set it to 0 when using other transmission rates (up to 100 kbps (Sm) or up to 400 kbps (Fm)) or for SMBus (10 to 100 kbps).

29.2.7 I2C Bus Status Enable Register (ICSER)

Address(es): IIC0.ICSER 4005 3006h, IIC1.ICSER 4005 3106h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
Value after reset:	0	0	0	0	1	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	SAR0E	Slave Address Register 0 Enable	0: Slave address in SARL0 and SARU0 disabled 1: Slave address in SARL0 and SARU0 enabled.	R/W
b1	SAR1E	Slave Address Register 1 Enable	0: Slave address in SARL1 and SARU1 disabled 1: Slave address in SARL1 and SARU1 enabled.	R/W
b2	SAR2E	Slave Address Register 2 Enable	0: Slave address in SARL2 and SARU2 disabled 1: Slave address in SARL2 and SARU2 enabled.	R/W
b3	GCAE	General Call Address Enable	0: General call address detection disabled 1: General call address detection enabled.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DIDE	Device ID Address Detection Enable	0: Device ID address detection disabled 1: Device ID address detection enabled.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOAE	Host Address Enable	0: Host address detection disabled 1: Host address detection enabled.	R/W

SARyE bit (Slave Address Register y Enable) (y = 0 to 2)

The SARyE bit enables or disables the received slave address and the slave address set in the SARLy and SARUy registers.

When this bit is set to 1, the slave address set in the SARLy and SARUy registers is enabled and is compared with the received slave address. When this bit is set to 0, the slave address set in SARLy and SARUy is disabled and is ignored even if it matches the received slave address.

GCAE bit (General Call Address Enable)

The GCAE bit specifies whether to ignore the general call address (0000 000b + 0 [W]: All 0) when it is received.

When this bit is set to 1, if the received slave address matches the general call address, the IIC recognizes the received slave address as the general call address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2), and performs the data receive operation. When this bit is set to 0, the received slave address is ignored even if it matches the general call address.

DIDE bit (Device ID Address Detection Enable)

The DIDE bit specifies whether to recognize and execute the device ID address when a device ID (1111 100b) is received in the first frame after a start or restart condition is detected.

When this bit is set to 1, if the received first frame matches the device ID, the IIC recognizes that the device ID address was received. When the next R/W# bit is 0 (W), the IIC recognizes the second and the subsequent frames as slave addresses and continues the receive operation. When this bit is set to 0, the IIC ignores the received first frame even if it matches the device ID address, and recognizes the first frame as a normal slave address.

For details, see section 29.7.3, Device ID Address Detection.

HOAE bit (Host Address Enable)

The HOAE bit specifies whether to ignore the received host address (0001 000b) when the SMBS bit in ICMR3 is 1.

When this bit is set to 1 while the SMBS bit in ICMR3 is 1, if the received slave address matches the host address, the IIC recognizes the received slave address as the host address independently of the slave addresses set in SARLy and

SARUy (y = 0 to 2), and performs the receive operation.

When the SMBS bit in ICMR3 or the HOAE bit is set to 0, the received slave address is ignored even if it matches the host address.

29.2.8 I2C Bus Interrupt Enable Register (ICIER)

Address(es): IIC0.ICIER 4005 3007h, IIC1.ICIER 4005 3107h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOIE	Timeout Interrupt Request Enable	0: Timeout interrupt (TMOIn) request disabled 1: Timeout interrupt (TMOIn) request enabled.	R/W
b1	ALIE	Arbitration-Lost Interrupt Request Enable	0: Arbitration-lost interrupt (ALIn) request disabled 1: Arbitration-lost interrupt (ALIn) request enabled.	R/W
b2	STIE	Start Condition Detection Interrupt Request Enable	0: Start condition detection interrupt (STIn) request disabled 1: Start condition detection interrupt (STIn) request enabled.	R/W
b3	SPIE	Stop Condition Detection Interrupt Request Enable	0: Stop condition detection interrupt (SPIn) request disabled 1: Stop condition detection interrupt (SPIn) request enabled.	R/W
b4	NAKIE	NACK Reception Interrupt Request Enable	0: NACK reception interrupt (NAKIn) request disabled 1: NACK reception interrupt (NAKIn) request enabled.	R/W
b5	RIE	Receive Data Full Interrupt Request Enable	0: Receive data full interrupt (IICn_RXI) request disabled 1: Receive data full interrupt (IICn_RXI) request enabled.	R/W
b6	TEIE	Transmit End Interrupt Request Enable	0: Transmit end interrupt (IICn_TEI) request disabled 1: Transmit end interrupt (IICn_TEI) request enabled.	R/W
b7	TIE	Transmit Data Empty Interrupt Request Enable	0: Transmit data empty interrupt (IICn_TXI) request disabled 1: Transmit data empty interrupt (IICn_TXI) request enabled.	R/W

TMOIE bit (Timeout Interrupt Request Enable)

The TMOIE bit enables or disables timeout interrupt (TMOIn) requests when the TMOF flag in ICSR2 is 1. To cancel a TMOI interrupt request, set the TMOF flag or the TMOIE bit to 0.

ALIE bit (Arbitration-Lost Interrupt Request Enable)

The ALIE bit enables or disables arbitration-lost interrupt (ALIn) requests when the AL flag in ICSR2 is 1. To cancel an ALI interrupt request, set the AL flag or the ALIE bit to 0.

STIE bit (Start Condition Detection Interrupt Request Enable)

The STIE bit enables or disables start condition detection interrupt (STIn) requests when the START flag in ICSR2 is 1. To cancel an STI interrupt request, set the START flag or the STIE bit to 0.

SPIE bit (Stop Condition Detection Interrupt Request Enable)

The SPIE bit enables or disables stop condition detection interrupt (SPIn) requests when the STOP flag in ICSR2 is 1. To cancel an SPI interrupt request, set the STOP flag or the SPIE bit to 0.

NAKIE bit (NACK Reception Interrupt Request Enable)

The NAKIE bit enables or disables NACK reception interrupt (NAKIn) requests when the NACKF flag in ICSR2 is 1. To cancel an NAKI interrupt request, set the NACKF flag or the NAKIE bit to 0.

RIE bit (Receive Data Full Interrupt Request Enable)

The RIE bit enables or disables receive data full interrupt (IICn_RXI) requests when the RDRF flag in ICSR2 is 1.

TEIE bit (Transmit End Interrupt Request Enable)

The TEIE bit enables or disables transmit end interrupt (IICn_TEI) requests when the TEND flag in ICSR2 is 1. To cancel an IICn_TEI interrupt request, set the TEND flag or the TEIE bit to 0.

TIE bit (Transmit Data Empty Interrupt Request Enable)

The TIE bit enables or disables transmit data empty interrupt (IICn_TXI) requests when the TDRE flag in ICSR2 is 1.

29.2.9 I2C Bus Status Register 1 (ICSR1)

Address(es): IIC0.ICSR1 4005 3008h, IIC1.ICSR1 4005 3108h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	AAS0	Slave Address 0 Detection Flag	0: Slave address 0 not detected 1: Slave address 0 detected.	R/(W) *1
b1	AAS1	Slave Address 1 Detection Flag	0: Slave address 1 not detected 1: Slave address 1 detected.	R/(W) *1
b2	AAS2	Slave Address 2 Detection Flag	0: Slave address 2 not detected 1: Slave address 2 detected.	R/(W) *1
b3	GCA	General Call Address Detection Flag	0: General call address not detected 1: General call address detected.	R/(W) *1
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DID	Device ID Address Detection Flag	0: Device ID command not detected 1: Device ID command detected. This bit is set to 1 when the first frame received immediately after a start condition is detected, matches a value of (device ID (1111 100b) + 0[W]).	R/(W) *1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOA	Host Address Detection Flag	0: Host address not detected 1: Host address detected. This bit is set to 1 when the received slave address matches the host address (0001 000b).	R/(W) *1

Note 1. Only 0 can be written to clear the flag.

AASy flag (Slave Address y Detection Flag) (y = 0 to 2)

The AASy flag indicates whether slave address y was detected.

[Setting conditions]

For 7-bit address format (SARUy.FS = 0):

- When the received slave address matches the SVA[6:0] value in SARLy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled). The AASy flag is set to 1 on the rising edge of the 9th SCL clock cycle in the frame.

For 10-bit address format: (SARUy.FS = 1):

- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy), and the subsequent address matches the SARLy value, with the SARyE bit in ICSER set to 1 (slave address y detection enabled). The AASy flag is set to 1 on the rising edge of the 9th SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the AASy flag after reading AASy = 1

- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

For 7-bit address format (SARUy.FS = 0):

- When the received slave address does not match the SVA[6:0] value in SARLy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled). The AASy flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.

For 10-bit address format (SARUy.FS = 1):

- When the received slave address does not match a value of 11110b + SVA[1:0] in SARUy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled). The AASy flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.
- When the received slave address matches a value of 11110b + SVA[1:0] in SARUy, and the subsequent address does not match the SARLy value, with the SARyE bit in ICSER set to 1 (slave address y detection enabled). The AASy flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.

GCA flag (General Call Address Detection Flag)

The GCA flag indicates whether the general call address was detected.

[Setting condition]

- When the received slave address matches the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection enabled). The GCA flag is set to 1 on the rising edge of the 9th SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the GCA flag after reading GCA = 1
- When a stop condition is detected
- When the received slave address does not match the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection enabled). The GCA flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

DID flag (Device ID Address Detection Flag)

The DID flag indicates whether the device ID address was detected.

[Setting condition]

- When the first frame received immediately after a start or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), with the DIDE bit in ICSER set to 1 (device ID address detection enabled). The DID flag is set to 1 on the rising edge of the 9th SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the DID flag after reading DID = 1
- When a stop condition is detected
- When the first frame received immediately after a start or restart condition is detected does not match a value of the device ID (1111 100b), with the DIDE bit in ICSER set to 1 (device ID address detection enabled). The DID flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.
- When the first frame received immediately after a start or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), and the second frame does not match any slave address from 0 to 2, with the DIDE bit in ICSER set to 1 (device ID address detection enabled). The DID flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

HOA flag (Host Address Detection Flag)

The HOA flag indicates whether the host address was detected.

[Setting condition]

- When the received slave address matches the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection enabled). The HOA flag is set to 1 on the rising edge of the 9th SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the HOA flag after reading HOA = 1
- When a stop condition is detected
- When the received slave address does not match the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection enabled). The HOA flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

29.2.10 I2C Bus Status Register 2 (ICSR2)

Address(es): IIC0.ICSR2 4005 3009h, IIC1.ICSR2 4005 3109h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOF	Timeout Detection Flag	0: Timeout not detected 1: Timeout detected.	R/(W)*1
b1	AL	Arbitration-Lost Flag	0: Arbitration not lost 1: Arbitration lost.	R/(W)*1
b2	START	Start Condition Detection Flag	0: Start condition not detected 1: Start condition detected.	R/(W)*1
b3	STOP	Stop Condition Detection Flag	0: Stop condition not detected 1: Stop condition detected.	R/(W)*1
b4	NACKF	NACK Detection Flag	0: NACK not detected 1: NACK detected.	R/(W)*1
b5	RDRF	Receive Data Full Flag	0: ICDRR contains no receive data 1: ICDRR contains receive data.	R/(W)*1
b6	TEND	Transmit End Flag	0: Data being transmitted 1: Data transmit complete.	R/(W)*1
b7	TDRE	Transmit Data Empty Flag	0: ICDRT contains transmit data 1: ICDRT contains no transmit data.	R

Note 1. Only 0 can be written to clear the flag.

TMOF flag (Timeout Detection Flag)

The TMOF flag is set to 1 when the IIC detects a timeout because the SCLn line state remains unchanged for the set period.

[Setting condition]

- When the SCLn line state remains unchanged for the period specified in the ICMR2.TMOH, TMOL, and TMOS bits while the ICFER.TMOE bit is 1 (timeout function enabled) in master or in slave mode and the received slave address matches.

[Clearing conditions]

- When 0 is written to the TMOF flag after reading TMOF = 1

- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

AL flag (Arbitration-Lost Flag)

The AL flag indicates that the bus mastership is lost in arbitration because of a bus conflict or because of some other reason, when a start condition was issued, or an address and data was transmitted.

The IIC monitors the level on the SDAn line during transmission. If the level on the line does not match the value of the bit being output, the IIC sets the AL flag to 1 to indicate that the bus is occupied by another device. The IIC can also set the AL flag to indicate the detection of arbitration loss during NACK transmission in master mode or during data transmission in slave mode.

[Setting conditions]

When master arbitration-lost detection is enabled (ICFER.MALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock, except for the ACK period during data transmission in master transmit mode
- When a start condition is detected while the ST bit in ICCR2 is 1 (start condition requested) or the internal SDA output state does not match the SDAn line level
- When the ST bit in ICCR2 is 1 (start condition requested), with the BBSY flag in ICCR2 set to 1.

When NACK arbitration-lost detection is enabled (ICFER.NALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock in the ACK period during NACK transmission in receive mode.

When slave arbitration-lost detection is enabled (ICFER.SALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock, except for the ACK period during data transmission in slave transmit mode.

[Clearing conditions]

- When 0 is written to the AL flag after reading AL = 1
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

Table 29.4 Relationship between arbitration-lost generation sources and arbitration-lost enable functions

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	Arbitration-lost generation source
1	×	×	1	Start condition issuance error	When internal SDA output state does not match SDAn line level when a start condition is detected while the ST bit in ICCR2 is 1
					When ST in ICCR2 is set to 1 while BBSY in ICCR2 is 1
			1	Transmit data mismatch	When transmit data (including slave address) does not match the bus state in master transmit mode
×	1	×	1	NACK transmission mismatch	When ACK is detected during transmission of NACK in master or slave receive mode
×	×	1	1	Transmit data mismatch	When transmit data does not match the bus state in slave transmit mode

×: Don't care

START flag (Start Condition Detection Flag)

The START flag indicates whether a start or restart condition is detected.

[Setting condition]

- When a start or restart condition is detected.

[Clearing conditions]

- When 0 is written to the START flag after reading START = 1

- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

STOP flag (Stop Condition Detection Flag)

The STOP flag indicates whether a stop condition is detected.

[Setting condition]

- When a stop condition is detected.

[Clearing conditions]

- When 0 is written to the STOP flag after reading STOP = 1
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

NACKF flag (NACK Detection Flag)

The NACKF flag indicates whether a NACK was detected.

[Setting condition]

- When acknowledge is not received (NACK received) from the receive device in transmit mode, with the NACKE bit in ICFER set to 1 (transfer suspension enabled).

[Clearing conditions]

- When 0 is written to the NACKF flag after reading NACKF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1, the IIC suspends data transmission and reception. Writing to ICDRT in transmit mode or reading from ICDRR in receive mode with the NACKF flag set to 1 does not enable data transmit or receive operation. To restart data transmission or reception, set the NACKF flag to 0.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates whether the IDCRR contains receive data.

[Setting conditions]

- When receive data is transferred from ICDRS to ICDRR. The RDRF flag is set to 1 on the rising edge of the 8th or 9th SCL clock cycle (selected in the RDRFS bit in ICMR3).
- When the received slave address matches after a start (or restart) condition is detected with the TRS bit in ICCR2 set to 0.

[Clearing conditions]

- When 0 is written to the RDRF flag after reading RDRF = 1
- When data is read from ICDRR
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

TEND flag (Transmit End Flag)

The TEND flag indicates whether data transmission is still being transmitted or is complete.

[Setting condition]

- On the rising edge of the 9th SCL clock cycle while the TDRE flag is 1.

[Clearing conditions]

- When 0 is written to the TEND flag after reading TEND = 1
- When data is written to ICDRT
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates whether the ICDRT contains transmit data.

[Setting conditions]

- When data is transferred from ICDRT to ICDRS and ICDRT becomes empty
- When the TRS bit in ICCR2 is set to 1
- When the received slave address matches while the TRS bit is 1.

[Clearing conditions]

- When data is written to ICDRT
- When the TRS bit in ICCR2 is set to 0
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1 while the NACKE bit in ICFER is 1, the IIC suspends data transmission and reception. In this case, if the TDRE flag is 0 (next transmit data written), data is transferred to the ICDRS register and the ICDRT register becomes empty on the rising edge of the 9th clock cycle, but the TDRE flag is not set to 1.

29.2.11 I2C Bus Wakeup Unit Register (ICWUR)

Address(es): IIC0.ICWUR 4005 3016h

	b7	b6	b5	b4	b3	b2	b1	b0
	WUE	WUIE	WUF	WUACK	—	—	—	WUAFA
Value after reset:	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	WUAFA	Wakeup Analog Filter Additional Selection	0: Do not add the wakeup analog filter 1: Add the wakeup analog filter.	R/W
b3 to b1	—	Reserved	These bit are read as 0. The write value should be 0.	R/W
b4	WUACK	ACK Bit for Wakeup Mode	Choice of four response modes in combination with ICCR1.IICRST and WUACK. See Table 29.5.	R/W
b5	WUF	Wakeup Event Occurrence Flag	0: Slave address not matching during wakeup 1: Slave address matching during wakeup.	R/W
b6	WUIE	Wakeup Interrupt Request Enable	0: Wakeup Interrupt Request (IIC0_WUI) disabled 1: Wakeup Interrupt Request (IIC0_WUI) enabled.	R/W
b7	WUE	Wakeup Function Enable	0: Wakeup function disabled 1: Wakeup function enabled.	R/W

Table 29.5 Wakeup mode

IICRST	WUACK	Operation mode	Description
0	0	Normal wakeup mode 1	ACK response on 9th SCL, and SCL low hold after 9th SCL
0	1	Normal wakeup mode 2	No ACK response immediately and SCL low hold between 8th and 9th SCL. SCL low-hold release and ACK response on 9th SCL.
1	0	Command recovery mode	ACK response on 9th SCL and no SCL low hold
1	1	EEP response mode	NACK response on 9th SCL and no SCL low hold

WUF flag (Wakeup Event Occurrence Flag)

The WUF flag indicates whether the slave address is matching during wakeup.

[Setting condition]

- When PCLKB is supplied after a slave-address match in the first 8th SCL low during wakeup mode.

[Clearing conditions]

- When 0 is written to the WUF flag after reading WUF = 1
- When ICE = 0 and IICRST = 1.

29.2.12 I2C-Bus Wakeup Unit Register 2 (ICWUR2)

Address(es): IIC0.ICWUR2 4005 3017h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	WUSYF	WUASYF	WUSEN
Value after reset:	1	1	1	1	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b0	WUSEN	Wakeup Function Synchronous Enable	0: IIC asynchronous operation enabled 1: IIC synchronous operation enabled.	R/W
b1	WUASYF	Wakeup Function Asynchronous Operation Status Flag	0: IIC synchronous operation enabled 1: IIC asynchronous operation enabled.	R
b2	WUSYF	Wakeup Function Synchronous Operation Status Flag	0: IIC asynchronous operation enabled 1: IIC synchronous operation enabled.	R
b7 to b3	—	Reserved	These bits are read as1. The write value should be 1.	R/W

WUSEN bit (Wakeup Function Synchronous Enable)

The WUSEN bit is used in combination with the WUASYF flag (or WUSYF flag) to switch between the PCLKB synchronous and asynchronous operation, when the wakeup effective function is enabled (ICWUR.WUE = 1).

The PCLKB operation switches from synchronous to asynchronous operation:

- When the ICCR2.BBSY flag is 0, if 0 is written to the WUSEN bit while the WUASYF flag is 0. The reception occurs independently of the operation of PCLKB (with PCLKB stopped) after it switches to the PCLKB asynchronous operation, on wakeup event detection.

The PCLKB operation switches from asynchronous to synchronous operation:

- When 1 is written to the WUSEN bit, with the WUASYF flag at 1, when a wakeup event is detected. After writing 1, the WUASYF flag immediately becomes 0.
- When the stop condition is detected with a wakeup event undetected.

WUASYF flag (Wakeup Function Asynchronous Operation Status Flag)

The WUASYF flag can place the IIC in PCLKB asynchronous operation when the wakeup effective function is enabled (ICWUR.WUE = 1).

[Setting condition]

- When the ICCR2.BBSY flag is 0, and WUSEN bit is set to 0 with the ICWUR.WUE bit set to 1.

[Clearing conditions]

- When 1 is written to the WUSEN bit after detecting a wakeup event with ICWUR.WUE bit set to 1
- When a stop condition is detected with WUSEN bit set to 1 before detecting the wakeup event with WUASY flag set to 1 with ICWUR.WUE bit set to 1
- When 1 is written to the WUSEN bit with the WUASYF flag set to 1, and a wakeup event is detected with ICWUR.WUE set to 1
- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)

- ICWUR.WUE = 0.

WUSYF flag (Wakeup Function Synchronous Operation Status Flag)

The WUSYF flag can place the IIC in PCLKB synchronous operation when the wakeup function is enabled (ICWUR.WUE = 1). When this flag is used, the WUASYF flag is reserved.

[Setting conditions]

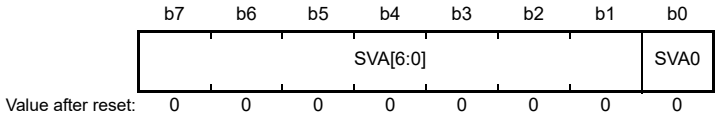
- When 1 is written to the WUSEN bit after detecting a wakeup event with ICWUR.WUE bit set to 1 and WUSYF flag set to 0
- When a stop condition is detected with WUSEN bit set to 1, before detecting a wakeup event with the WUSYF flag set to 0 and the ICWUR.WUE bit set to 1
- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

[Clearing condition]

- When the ICCR2.BBSY flag is 0 with the ICWUR.WUE bit set to 1, after writing 0 to the WUSEN bit.

29.2.13 Slave Address Register L y (SARLy) (y = 0 to 2)

Address(es): IIC0.SARL0 4005 300Ah, IIC1.SARL0 4005 310Ah, IIC0.SARL1 4005 300Ch, IIC1.SARL1 4005 310Ch, IIC0.SARL2 4005 300Eh, IIC1.SARL2 4005 310Eh



Bit	Symbol	Bit name	Description	R/W
b0	SVA0	10-Bit Address LSB	Slave address setting	R/W
b7 to b1	SVA[6:0]	7-Bit Address/10-Bit Address Lower Bits	Slave address setting	R/W

SVA0 bit (10-Bit Address LSB)

When the 10-bit address format is selected (SARUy.FS = 1), the SVA0 bit functions as the LSB of a 10-bit address and is combined with the SVA[6:0] bits to form the lower 8 bits of a 10-bit address.

This bit is valid when the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1. When the SARUy.FS or SARyE bit is 0, the setting in this bit is ignored.

SVA[6:0] bits (7-Bit Address/10-Bit Address Lower Bits)

When the 7-bit address format is selected (SARUy.FS = 0), the SVA[6:0] bits function as a 7-bit address. When the 10-bit address format is selected (SARUy.FS = 1), these bits combined with the SVA0 bit to form the lower 8 bits of a 10-bit address. When the SARyE bit in ICSER is 0, the setting in these bits is ignored.

29.2.14 Slave Address Register U y (SARUy) (y = 0 to 2)

Address(es): IIC0.SARU0 4005 300Bh, IIC1.SARU0 4005 310Bh, IIC0.SARU1 4005 300Dh, IIC1.SARU1 4005 310Dh, IIC0.SARU2 4005 300Fh, IIC1.SARU2 4005 310Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SVA[1:0]		FS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FS	7-Bit/10-Bit Address Format Select	0: Select 7-bit address format 1: Select 10-bit address format.	R/W
b2, b1	SVA[1:0]	10-Bit Address Upper Bits	Slave address setting	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FS bit (7-Bit/10-Bit Address Format Select)

The FS bit selects the 7-bit or 10-bit address format for the slave address y (in SARLy and SARUy).

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 0, the 7-bit address format is selected for slave address y, the SVA[6:0] setting in SARLy is valid, and the SVA[1:0] and SVA0 settings in SARLy are ignored.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, the 10-bit address format is selected for slave address y and the SVA[1:0] and SARLy settings are valid.

When the SARyE bit in ICSER is 0 (SARLy and SARUy disabled), the SARUy.FS bit is invalid.

SVA[1:0] bits (10-Bit Address Upper Bits)

When the 10-bit address format is selected (FS = 1), the SVA[1:0] bits function as the upper 2 bits of a 10-bit address.

These bits are valid when the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1. When the SARUy.FS or SARyE bit is 0, the setting of these bits is ignored.

29.2.15 I2C Bus Bit Rate Low-Level Register (ICBRL)

Address(es): IIC0.ICBRL 4005 3010h, IIC1.ICBRL 4005 3110h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRL[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	BRL[4:0]	Bit Rate Low-Level Period	Low-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

ICBRL is a 5-bit register that sets the low-level period of the SCL clock. ICBRL also generates the data setup time for automatic SCL low-hold operation, see section 29.9, Automatic Low-Hold Function for SCL.

BRL[4:0] bits (Bit Rate Low-Level Period)

The BRL[4:0] bits set the low-level period of the SCL clock. ICBRL counts the low-level period with the internal reference clock source (IICϕ) specified in the CKS[2:0] bits in ICMR1. When the IIC is used only in slave mode, the BRL[4:0] bits must be set to a value longer than the data setup time*1.

If the digital noise filter is enabled (NFE bit in ICFER is 1), set the BRL[4:0] bits to a value at least one greater than the

number of stages in the noise filter. For this number, see the description of the ICMR3.NF[1:0] bits.

Note 1. Data setup time ($t_{SU:DAT}$)
250 ns for up to 100 kbps: Standard mode (Sm)
100 ns for up to 400 kbps: Fast mode (Fm)
50 ns for up to 1 Mbps: Fast mode plus (Fm+)

29.2.16 I2C Bus Bit Rate High-Level Register (ICBRH)

Address(es): IIC0.ICBRH 4005 3011h, IIC1.ICBRH 4005 3111h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRH[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	BRH[4:0]	Bit Rate High-Level Period	High-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

ICBRH is a 5-bit register that sets the high-level period of the SCL clock. ICBRH is valid in master mode.

BRH[4:0] bits (Bit Rate High-Level Period)

The BRH[4:0] bits set the high-level period of the SCL clock. If the IIC is used only in slave mode, do not set the BRH[4:0] bits.

ICBRH counts the high-level period with the internal reference clock source (IICϕ) specified in the CKS[2:0] bits in ICMR1.

If the digital noise filter is enabled (NFE bit in ICFER is 1), set these bits to a value at least one greater than the number of stages in the noise filter. For this number, see the description of the ICMR3.NF[1:0] bits.

The IIC transfer rate and the SCL clock duty are calculated using the following expressions:

1. ICFER.SCLE = 0
Transfer rate = 1/{[(BRH + 1) + (BRL + 1)]/IICφ*1 + tr*2 + tf*2}
Duty cycle = {tr + [(BRH + 1)/IICφ]}/{tr + tf + [(BRH + 1) + (BRL + 1)]/IICφ}
2. ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] = 000b (IICφ = PCLKB)
Transfer rate = 1/{[(BRH + 3) + (BRL+ 3)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 3)/IICφ]}/{tr + tf + [(BRH + 3) + (BRL + 3)]/IICφ}
3. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] = 000b (IICφ = PCLKB)
Transfer rate = 1/{[(BRH + 3 + nf*3) + (BRL + 3 + nf)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 3 + nf)/IICφ]}/{tr + tf + [(BRH + 3 + nf) + (BRL + 3 + nf)]/IICφ}
4. ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] ≠ 000b
Transfer rate = 1/{[(BRH + 2) + (BRL + 2)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 2)/IICφ]}/{tr + tf + [(BRH + 2) + (BRL + 2)]/IICφ}
5. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] ≠ 000b
Transfer rate = 1/{[(BRH + 2 + nf) + (BRL + 2 + nf)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 2 + nf)/IICφ]}/{tr + tf + [(BRH + 2 + nf) + (BRL + 2 + nf)]/IICφ}

Note 1. IICφ = PCLKB × Division ratio.
Note 2. The SCLn line rise time (tr) and SCLn line fall time (tf) depend on the total bus line capacitance (Cb) and the pull-up resistor (Rp). For details, see the I2C bus standard from NXP Semiconductors.
Note 3. nf = Number of digital noise filter stages selected in the ICMR3.NF bit.

Table 29.6 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 0

Transfer rate (kbps)	CKS[2:0]	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	100b	14 (EEh)	17 (F1h)	60	—	(1)
400	010b	8 (E8h)	19 (F3h)	60	—	(1)
1000	000b	15 (EFh)	29 (FDh)	60	—	(1)

Table 29.7 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 1 and NFE = 0

Transfer rate (kbps)	CKS[2:0]	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	100b	13 (EDh)	16 (F0h)	60	—	(4)
400	010b	7 (E7h)	18 (F2h)	60	—	(4)
1000	000b	13 (EDh)	27 (FBh)	60	—	(2)

Table 29.8 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 1 and NFE = 1

Transfer rate (kbps)	CKS[2:0]	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	100b	11 (EBh)	14 (EEh)	60	01b	(5)
400	010b	5 (E5h)	16 (F0h)	60	01b	(5)
1000	000b	11 (EBh)	25 (F9h)	60	01b	(3)

29.2.17 I2C Bus Transmit Data Register (ICDRT)

Address(es): IIC0.ICDRT 4005 3012h, IIC1.ICDRT 4005 3112h

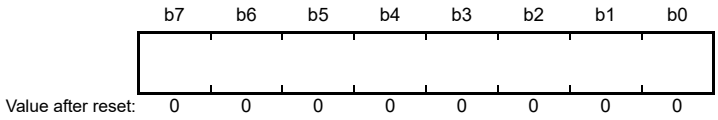
When ICDRT detects a space in the I2C Bus Shift Register (ICDRS), it transfers the transmit data that is written to ICDRT to ICDRS and starts transmitting data in transmit mode.

The double-buffer structure of ICDRT and ICDRS allows continuous transmit operation if the next transmit data is written to ICDRT while the ICDRS data is being transmitted.

ICDRT can always be read from and written to. Write transmit data to ICDRT when a transmit data empty interrupt (IICn_TXI) request is generated.

29.2.18 I2C Bus Receive Data Register (ICDRR)

Address(es): IIC0.ICDRR 4005 3013h, IIC1.ICDRR 4005 3113h

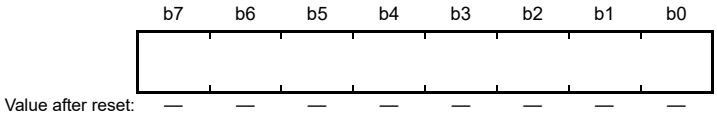


When 1 byte of data is received, the received data is transferred from the I2C Bus Shift Register (ICDRS) to ICDRR to enable the next data to be received.

The double-buffer structure of ICDRS and ICDRR allows continuous receive operation if the received data is read from ICDRR while ICDRS is receiving data. ICDRR cannot be written to. Read data from ICDRR when a receive data full interrupt (IICn_RXI) request is generated.

If ICDRR receives the next receive data before the current data is read from ICDRR while the RDRF flag in ICSR2 is 1, the IIC automatically holds the SCL clock low for 1 clock cycle before the RDRF flag is set to 1 again.

29.2.19 I2C Bus Shift Register (ICDRS)



ICDRS is an 8-bit shift register to transmit and receive data.

During transmission, transmit data is transferred from ICDRT to ICDRS and is sent from the SDAn pin. During reception, data is transferred from ICDRS to ICDRR after 1 byte of data is received. ICDRS cannot be accessed directly.

29.3 Operation

29.3.1 Communication Data Format

The I2C bus format consists of 8-bit data and 1-bit acknowledge. The frame following a start or restart condition is an address frame that specifies a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a stop condition is issued.

Figure 29.3 shows the I2C bus format, and Figure 29.4 shows the I2C bus timing.

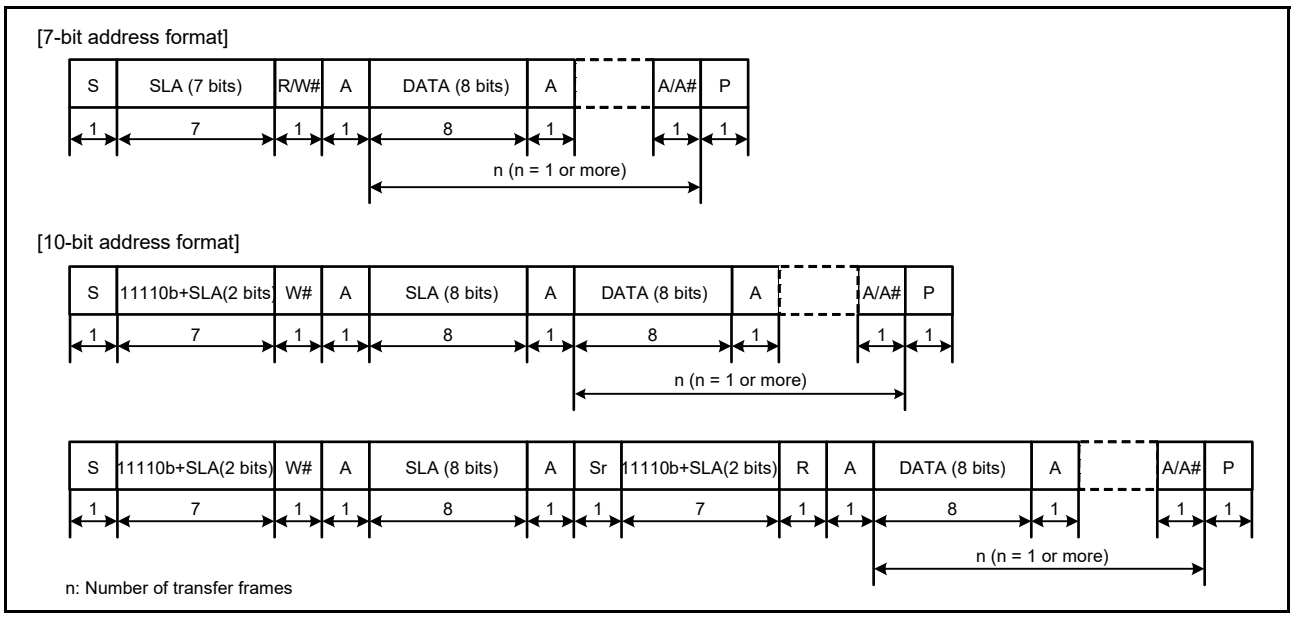


Figure 29.3 I2C bus format

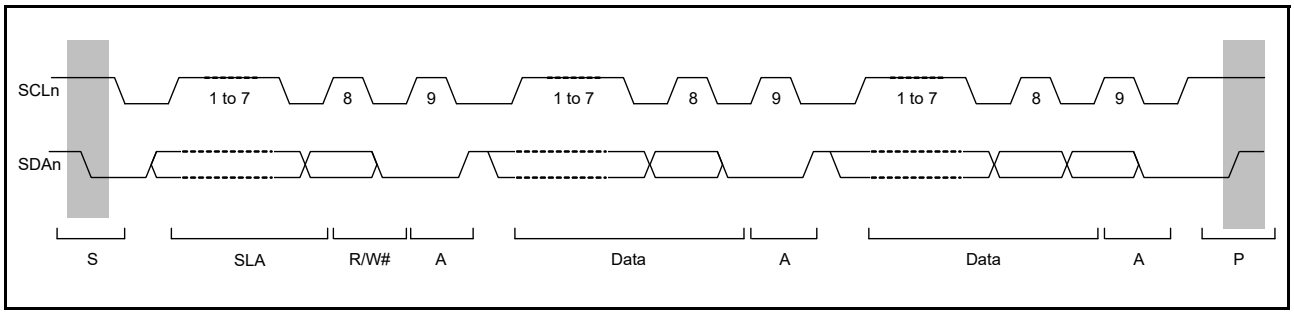


Figure 29.4 I2C bus timing (SLA = 7 bits)

S: Start condition. The master device drives the SDAn line low from high while the SCLn line is high.

SLA: Slave address, by which the master device selects a slave device

R/W#: Indicates the direction of data transfer: from the slave device to the master device when R/W# is 1, or from the master device to the slave device when R/W# is 0

A: Acknowledge. The receive device drives the SDAn line low. In master transmit mode, the slave device returns acknowledge. In master receive mode, the master device returns acknowledge.

A#: Not Acknowledge. The receive device drives the SDAn line high.

Sr: Restart condition. The master device drives the SDAn line low from the high after the setup time elapses with the SCLn line high.

DATA: Transmitted or received data

P: Stop condition. The master device drives the SDAn line high from low when the SCLn line is high.

29.3.2 Initial Settings

Before starting data transmission or reception, initialize the IIC using the procedure shown in Figure 29.5.

1. Set the ICCR1.ICE bit set to 0 to set the SCLn and SDAn pins to the inactive state.
2. Set the ICCR1.IICRST bit to 1 to initiate IIC reset.
3. Set the ICCR1.ICE bit to 1 to initiate internal reset, which initializes the flags and the internal state of the ICSR1 register.
4. Set the SARLy, SARUy, ICSER, ICMR1, ICBRH, and ICBRL registers (y = 0 to 2), and set the other registers as required. For initial IIC settings, see Figure 29.5.
5. When the required register settings are complete, set the ICCR1.IICRST bit to 0 to release the IIC reset.

Note: This procedure is not required if the IIC initialization is already complete.

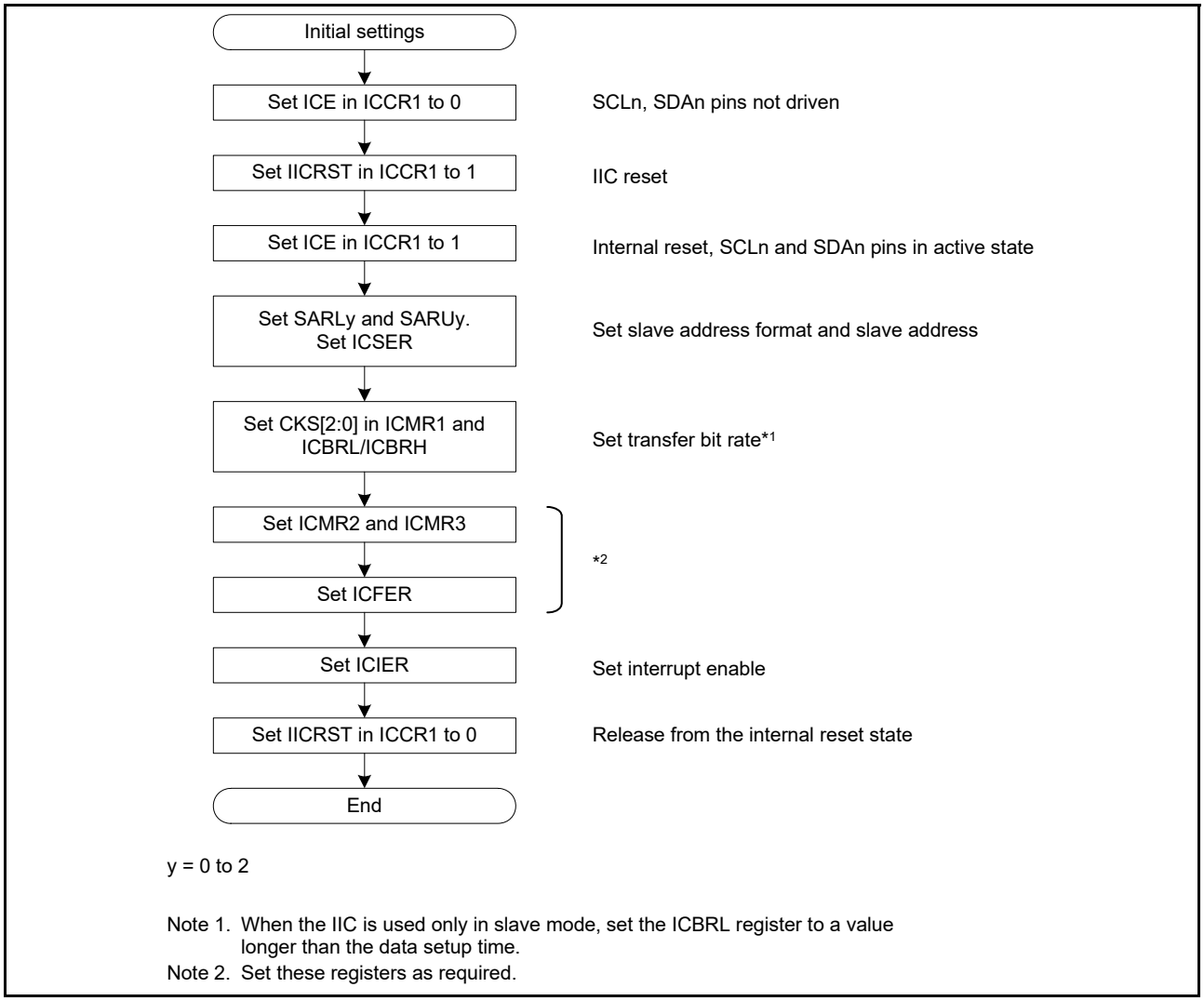


Figure 29.5 Example IIC initialization flow

29.3.3 Master Transmit Operation

In master transmit operation, the IIC outputs the SCL clock and transmit data signals as the master device, and the slave device returns the acknowledgments. Figure 29.6 shows an example of master transmission, and Figure 29.7 to Figure 29.9 show the operation timing in master transmission.

To set up and perform master transmission:

1. Initialize the IIC using the procedure in section 29.3.2, Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is open, then set the ST bit in ICCR2 to 1 (start condition request). On receiving the request, the IIC issues a start condition. At the same time, the BBSY and START flags in ICSR2 automatically set to 1 and the ST bit is automatically set to 0. If the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that the start condition requested by the ST bit has successfully completed, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to TRS = 1.
3. Check that the TDRE flag in ICSR2 is 1, then write the value for transmission (the slave address and the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag is automatically set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. After the byte containing the slave address and R/W# bit is transmitted, the value of the TRS bit automatically updates to select master transmit or master receive mode based on the value of the transmitted R/W# bit. If the value of the R/W# bit is 0, the IIC continues in master transmit mode. If the ICSR2.NACKF flag is 1, indicating that no slave device recognized the address or

there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
To transmit data with an address in the 10-bit format, start by writing 1111 0b, the two upper bits of the slave address, and W to ICDRT as the first address transmission. For the second address transmission, write the 8 lower bits of the slave address to ICDRT.

4. Check that the TDRE flag in ICSR2 is 1, then write the transmit data to the ICDRT register. The IIC automatically holds the SCLn line low until the transmit data is ready or a stop condition is issued.
5. After all bytes of transmit data are written to the ICDRT register, wait until the value in the TEND flag in ICSR2 returns to 1, then set the SP bit in ICCR2 to 1 (stop condition requested). On receiving a stop condition request, the IIC issues the stop condition. For details, see section 29.11.3, Issuing a Stop Condition.
6. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Additionally, the IIC automatically sets the TDRE and TEND flags to 0, and sets the STOP flag in ICSR2 to 1.
7. Check that the ICSR2.STOP flag is 1, then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

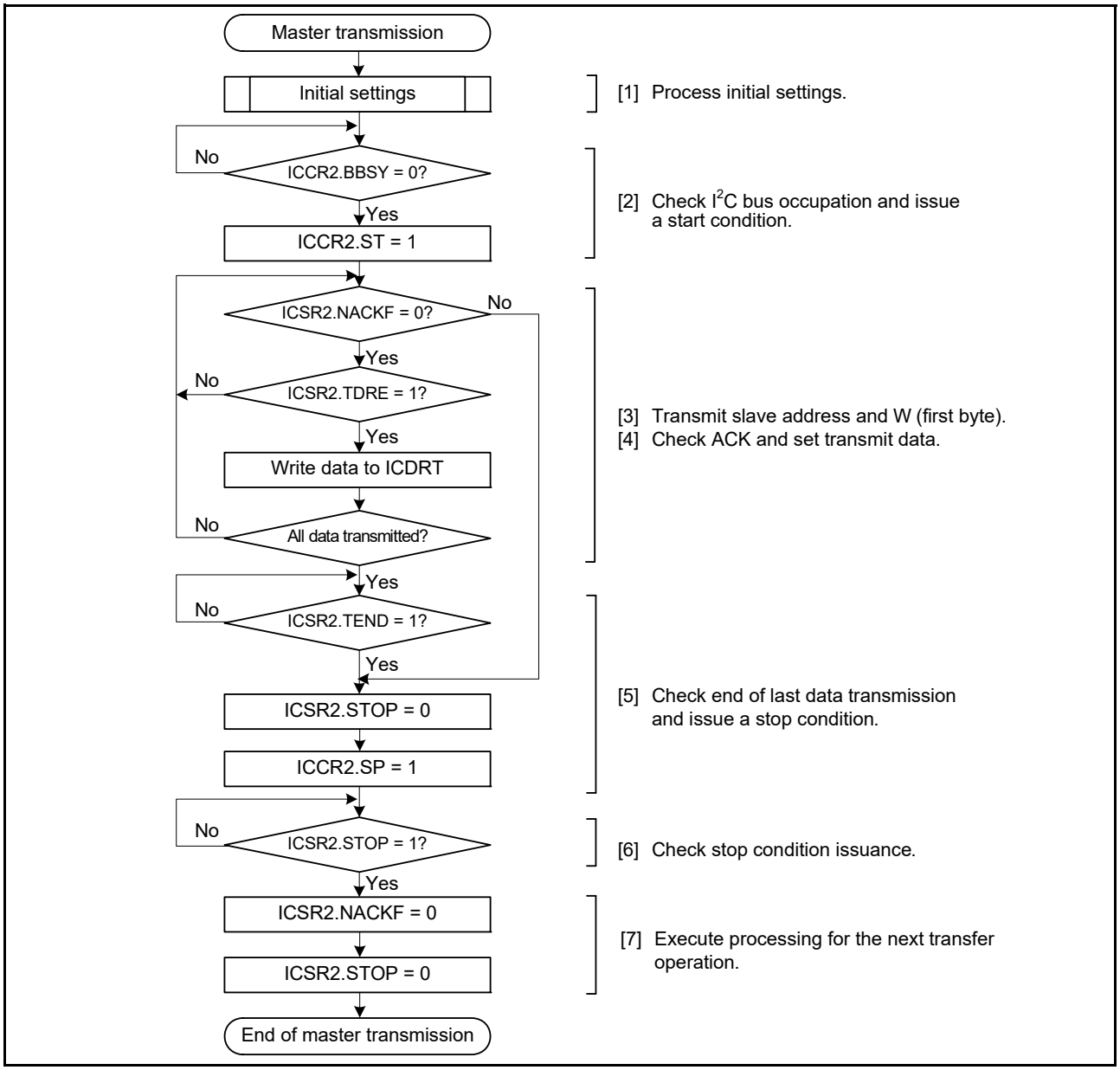


Figure 29.6 Example master transmission flow

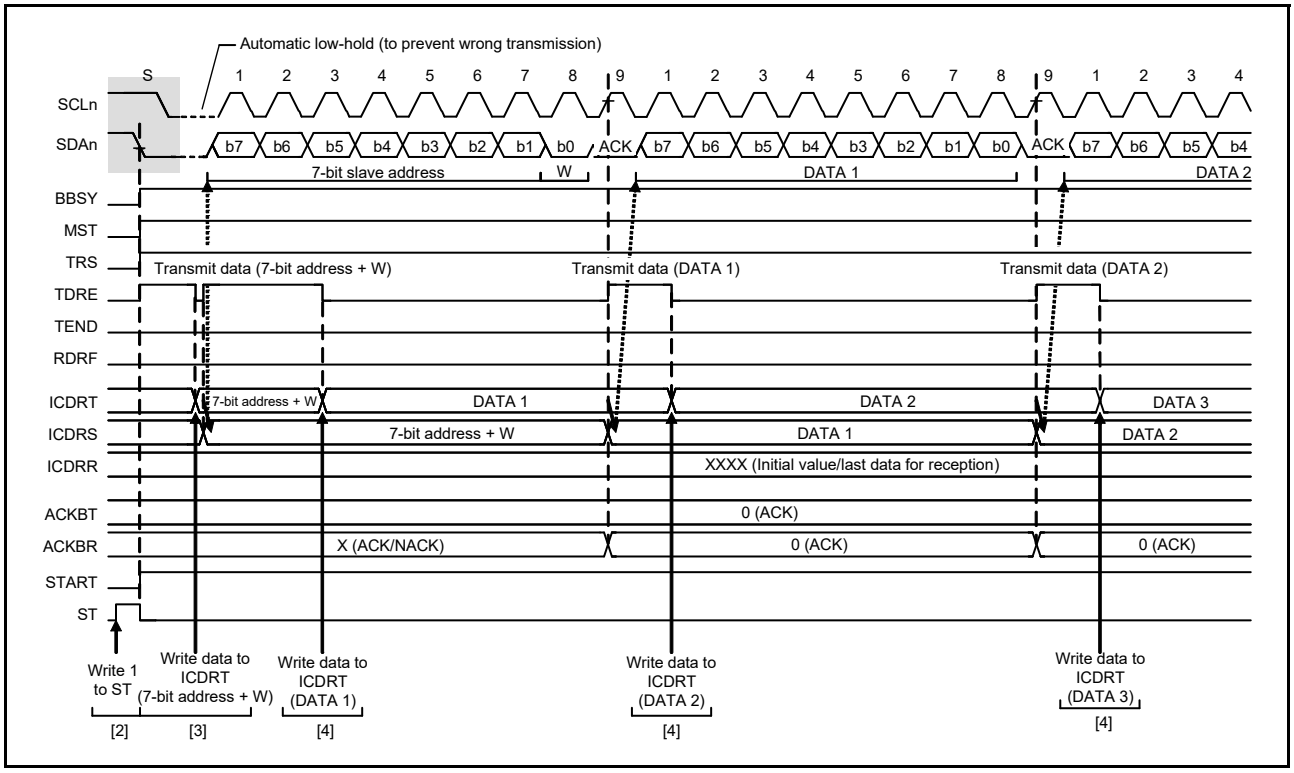


Figure 29.7 Master transmit operation timing (1) with 7-bit address format

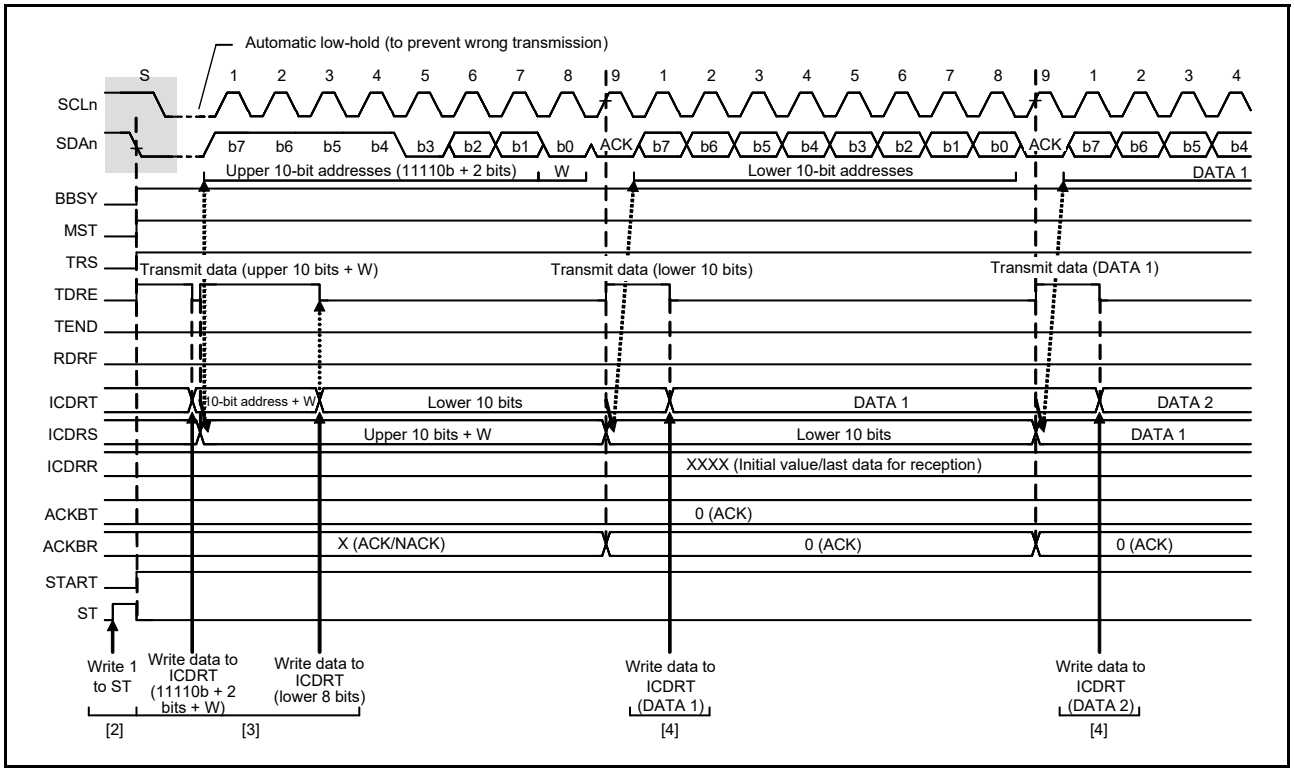


Figure 29.8 Master transmit operation timing (2) with 10-bit address format

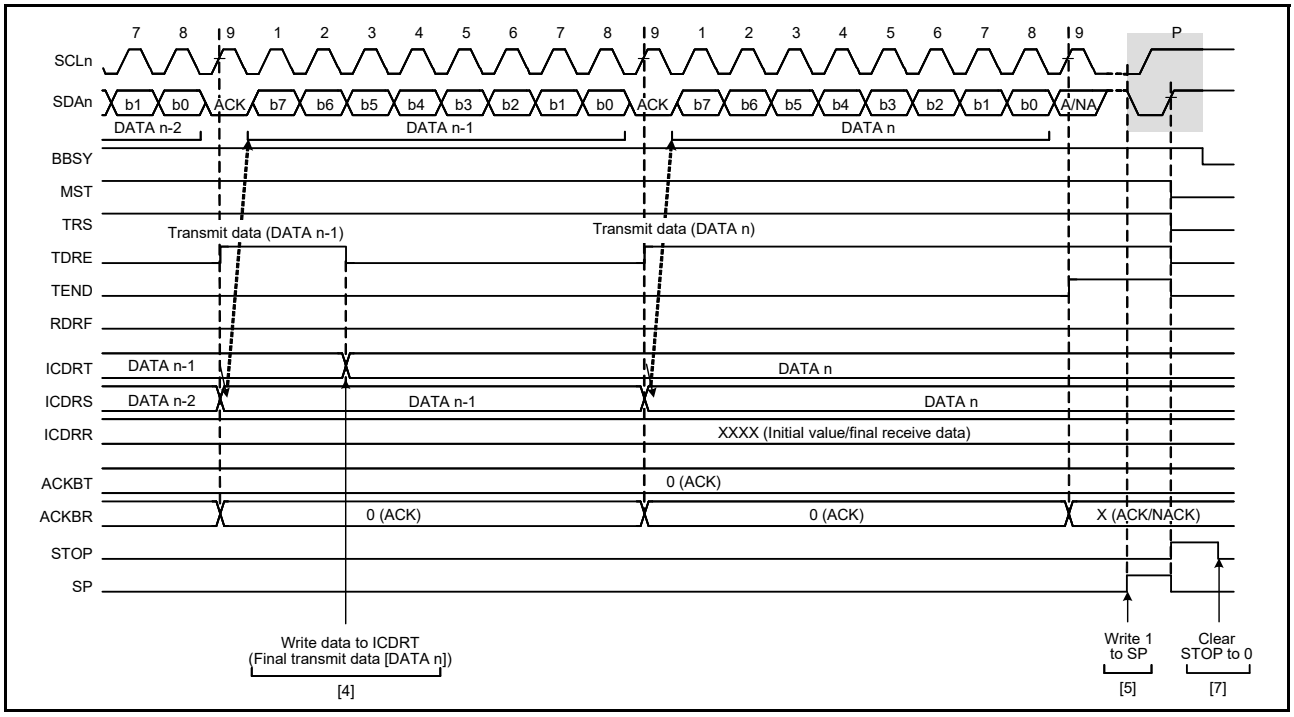


Figure 29.9 Master transmit operation timing (3)

29.3.4 Master Receive Operation

In master receive operation, the IIC as a master device outputs the SCL clock, receives data from the slave device, and returns acknowledgments. Because the IIC must start by sending a slave address to the associated slave device, the slave address part of the procedure is performed in master transmit mode, but the subsequent steps are in master receive mode.

Figure 29.10 and Figure 29.11 show examples of master reception (7-bit address format), and Figure 29.12 to Figure 29.14 show the operation timing in master reception.

To set up and perform master reception:

1. Initialize the IIC using the procedure in section 29.3.2, Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is open, then set the ST bit in ICCR2 to 1 to request the issue of a start condition. On receiving the request, the IIC issues a start condition. When the IIC detects the start condition, the BBSY and START flags in ICSR2 automatically set to 1, and the ST bit automatically sets to 0. If the start condition is detected and the levels for the SDA output and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that the start condition requested by the ST bit has successfully completed, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to TRS = 1.
3. Check that the TDRE flag in ICSR2 is 1, then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag is automatically set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. When the byte containing the slave address and R/W# bit is transmitted, the value of the ICCR2.TRS bit automatically updates to select transmit or receive mode based on the value of the transmitted R/W# bit. If the value of the R/W# bit is 1, the TRS bit is set to 0 on the rising edge of the 9th cycle of the SCL clock, placing the IIC in master receive mode. At this time, the TDRE flag is set to 0 and the ICSR2.RDRF flag is automatically set to 1.
   If the ICSR2.NACKF flag is 1, indicating that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
   For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a restart condition. After that, transmit 1111 0b, the two upper bits of the slave address, and the R bit to place the IIC in master receive mode.
4. Dummy read the ICDRR after confirming that the RDRF flag in ICSR2 is 1. Doing so causes the IIC to start output of the SCL clock and start data reception.

5. After 1 byte of data is received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the 8th or 9th cycle of the SCL clock, as selected in the RDRFS bit in ICMR3. Reading ICDRR produces the received data, and automatically sets the RDRF flag to 0. The value of the acknowledgment field received during the 9th cycle of the SCL clock is returned as the value set in the ICMR3.ACKBT bit. If the next byte to be received is the next to last byte, set the ICMR3.WAIT bit to 1 for wait insertion before reading ICDRR, containing the second byte from the last. In addition to enabling NACK output, even when interrupts or other operations result in delays in setting the ICMR3.ACKBT bit to 1 (NACK) in step (6), this fixes the SCLn line to low on the rising edge of the 9th clock cycle in reception of the last byte, which enables the issue of a stop condition.
6. When the ICMR3.RDRFS bit is 0, and the slave device must be notified that it is to end transfer for data reception after transfer of the next and final byte, set the ICMR3.ACKBT bit to 1 (NACK).
7. After reading the second-to-last byte from the ICDRR register, if the value of the ICSR2.RDRF flag is 1, write 1 to the SP bit in ICCR2 (to request stop condition), then read the last byte from ICDRR. When ICDRR is read, the IIC is released from the wait state and issues the stop condition after low-level output in the 9th clock cycle is complete or the SCLn line is released from the low-hold state.
8. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Additionally, detection of the stop condition sets the ICSR2.STOP flag to 1.
9. Check that the ICSR2.STOP flag is 1, then set the NACKF and STOP flags in ICSR2 to 0 for the next transfer operation.

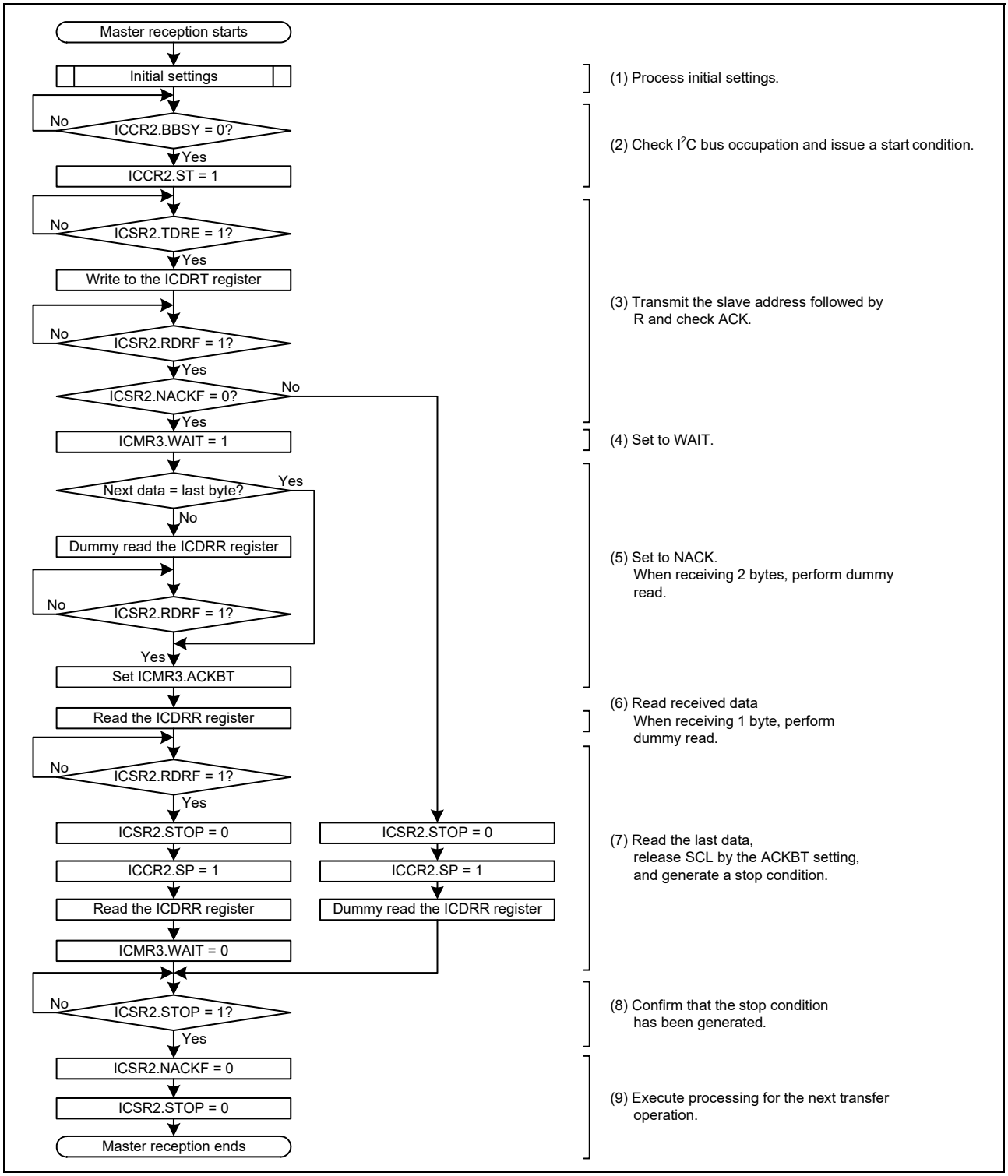


Figure 29.10 Example master reception flow with 7-bit address format, and 1 or 2 bytes

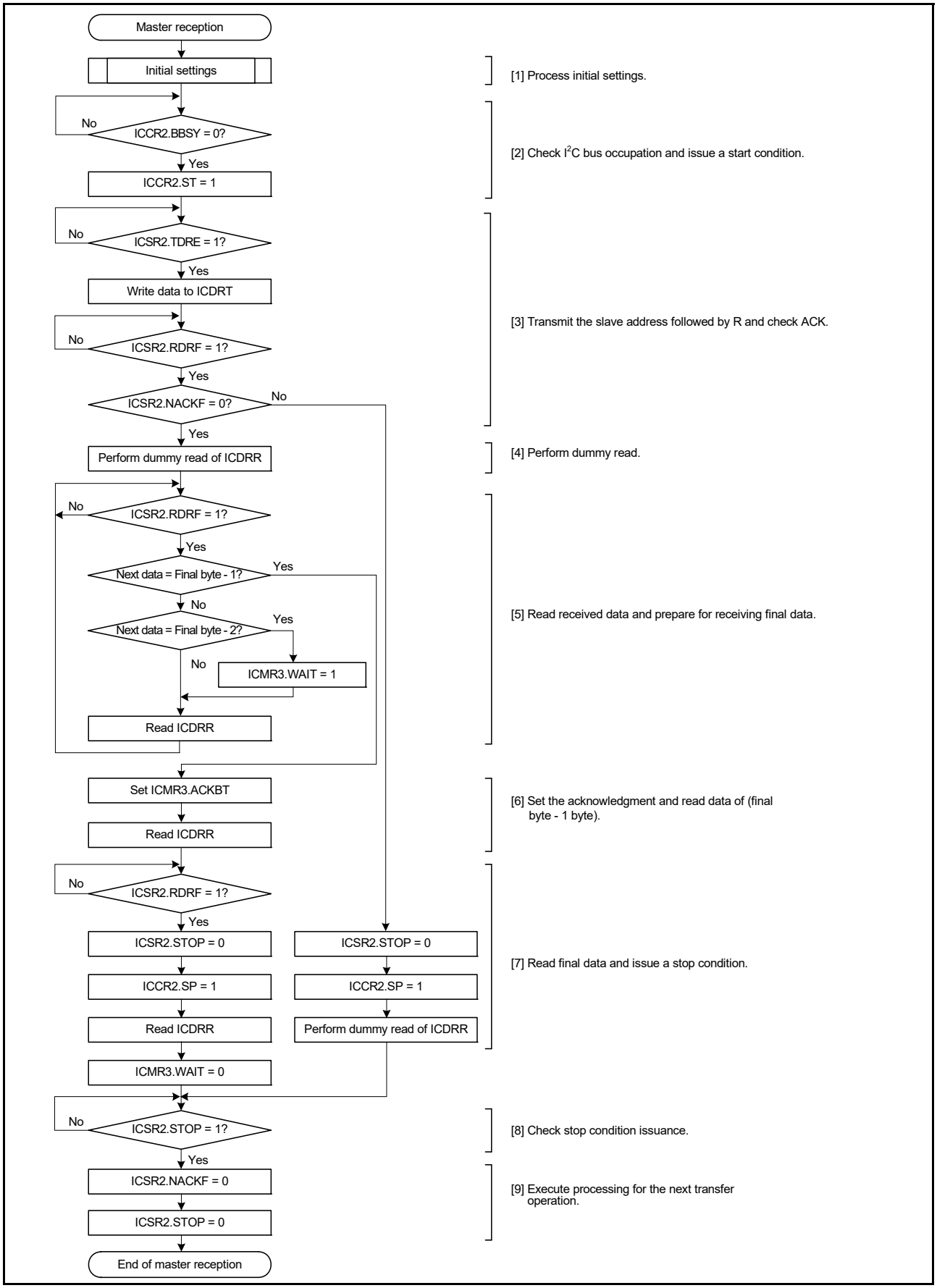


Figure 29.11 Example master reception flow with 7-bit address format and 3 or more bytes

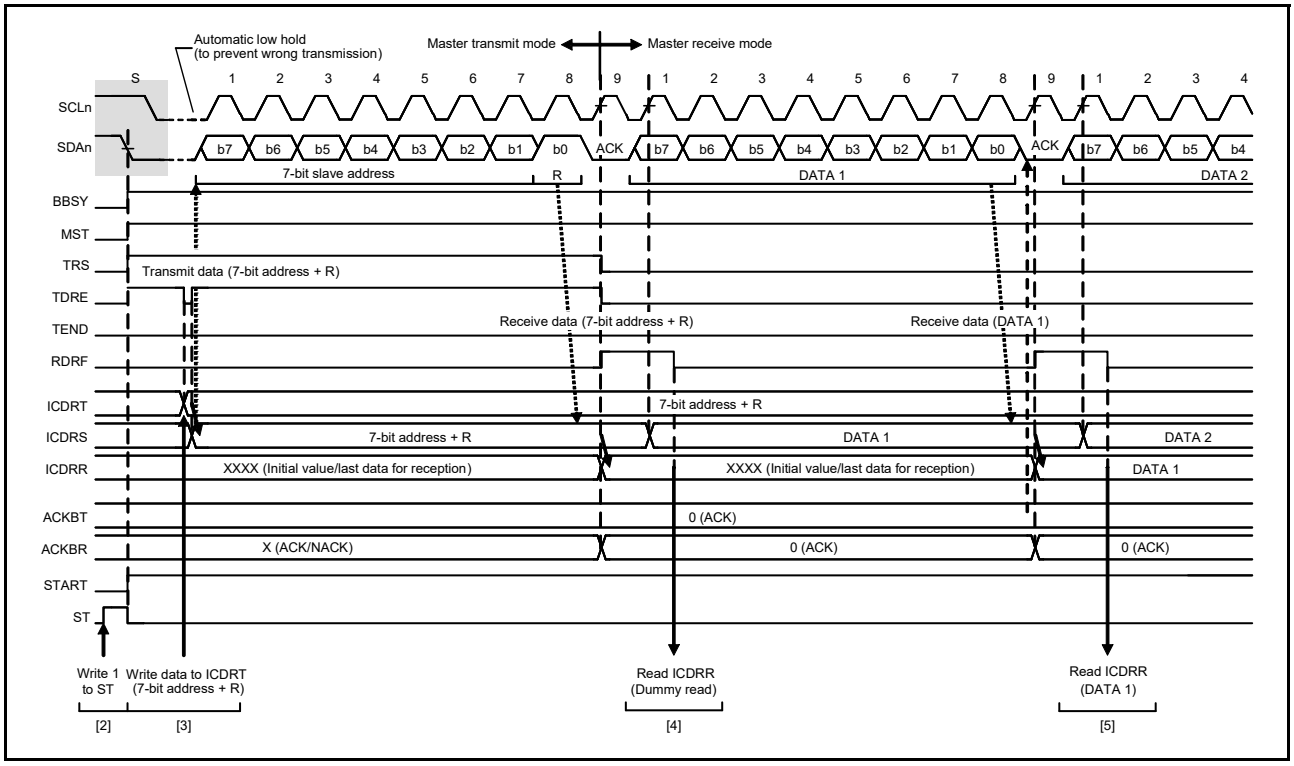


Figure 29.12 Master receive operation timing (1) with 7-bit address format, when RDRFS = 0

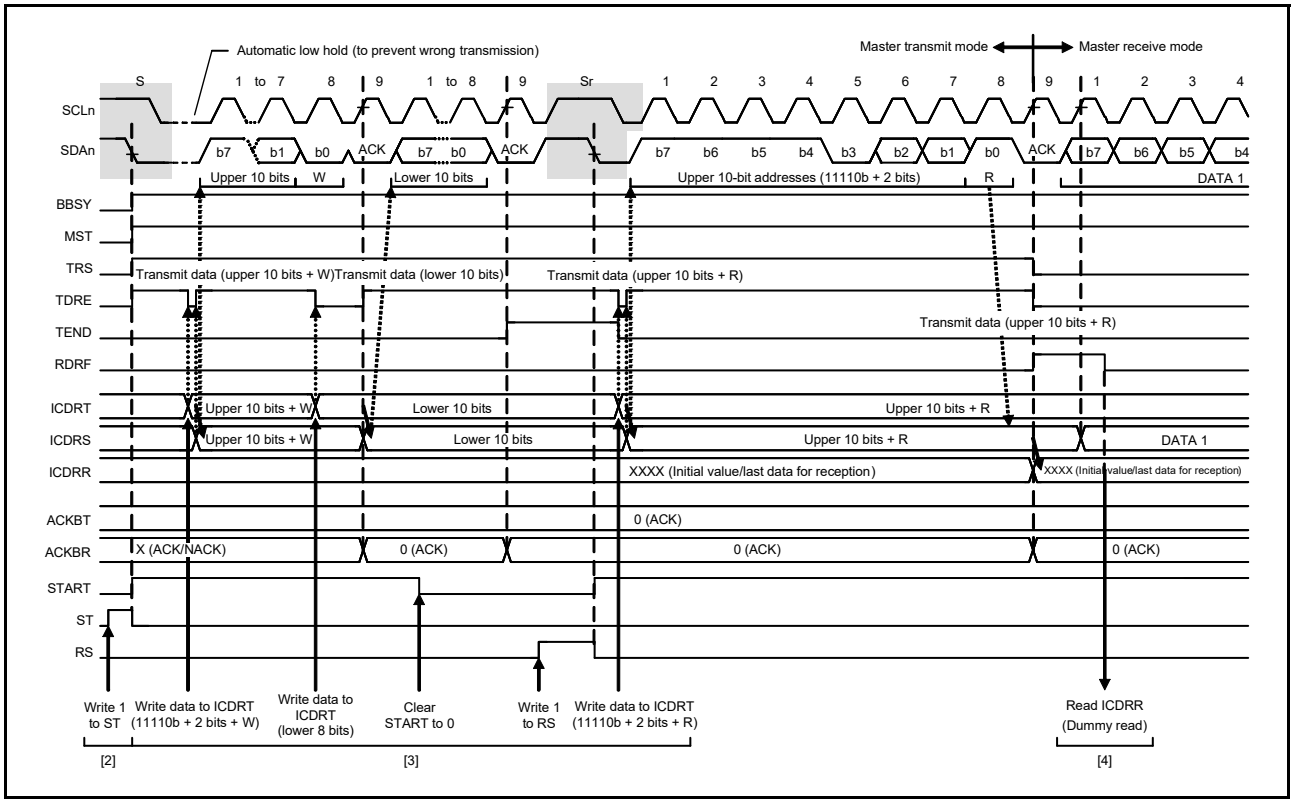


Figure 29.13 Master receive operation timing (2) with 10-bit address format, when RDRFS = 0

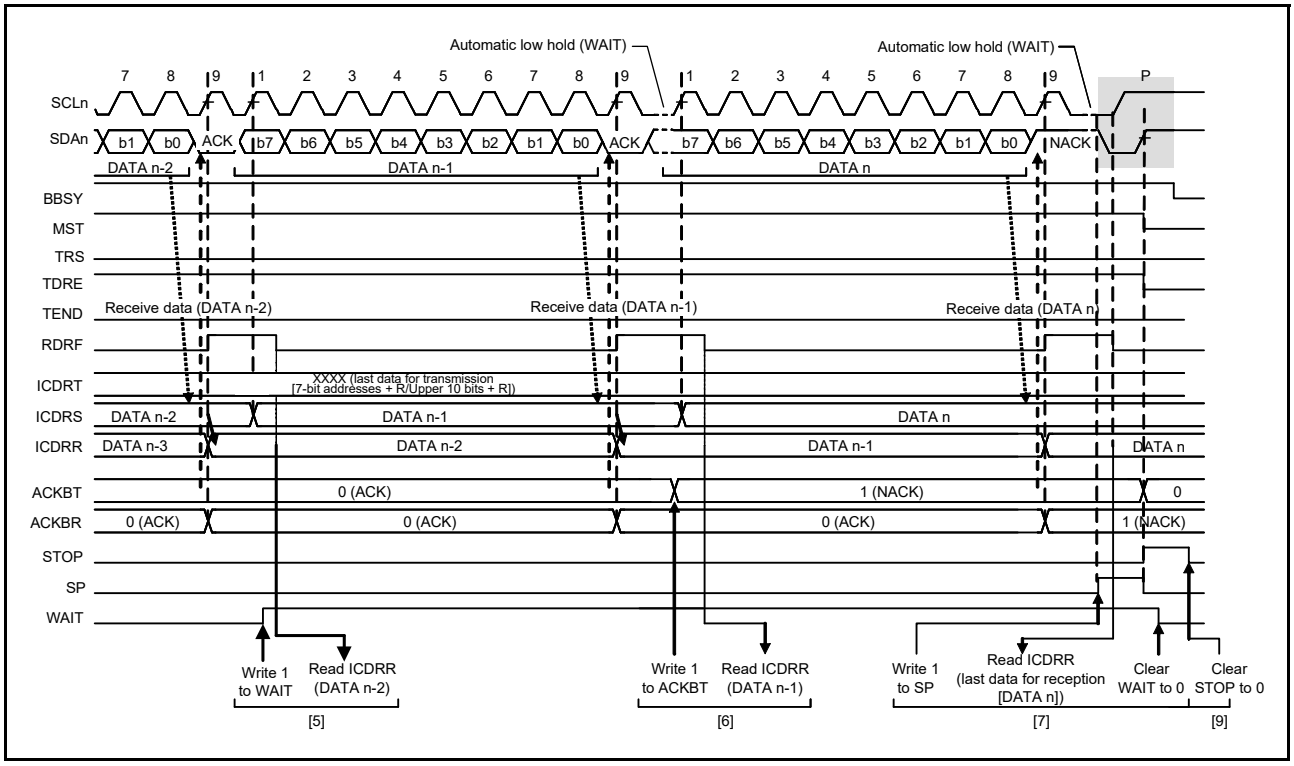


Figure 29.14 Master receive operation timing (3) when RDRFS = 0

29.3.5 Slave Transmit Operation

In slave transmit operation, the master device outputs the SCL clock, the IIC transmits data as a slave device, and the master device returns the acknowledgments.

Figure 29.15 shows an example of slave transmission, and Figure 29.16 and Figure 29.17 show the operation timing in slave transmission.

To set up and perform slave transmission:

1. Initialize the IIC using the procedure in section 29.3.2, Initial Settings.
   After the initialization, the IIC stays in the standby state until it receives a slave address that matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy (y = 0 to 2) flags to 1 on the rising edge of the 9th cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the 9th cycle of the SCL clock. If the value of the received R/W# bit is 1, the IIC automatically places itself in slave transmit mode by setting both the ICCR2.TRS bit and the ICSR2.TDRE flag to 1.
3. Check that the ICSR2.TEND flag is 1, then write the transmit data to the ICDRT register. If the IIC receives no acknowledge from the master device (receives an NACK signal) while the ICFER.NACKE bit is 1, the IIC suspends transfer of the next data.
4. Wait until the ICSR2.TEND flag is set to 1 while the ICSR2.TDRE flag is 1, after the ICSR2.NACKF flag is set to 1 or the last byte for transmission is written to the ICDRT register. When the ICSR2.NACKF flag or the TEND flag is 1, the IIC drives the SCLn line low on the 9th falling edge of the SCL clock.
5. When the NACKF or TEND flag in ICSR2 is 1, dummy read ICDRR to complete the processing. This releases the SCLn line.
6. On detecting the stop condition, the IIC automatically sets the ICSR1.HOA, GCA, and AASy (y = 0 to 2) flags, the TDRE and TEND flags in ICSR2, and the ICCR2.TRS bit to 0, and enters slave receive mode.
7. Check that the ICSR2.STOP flag is 1, then set the NACKF and STOP flags in ICSR2 to 0 for the next transfer operation.

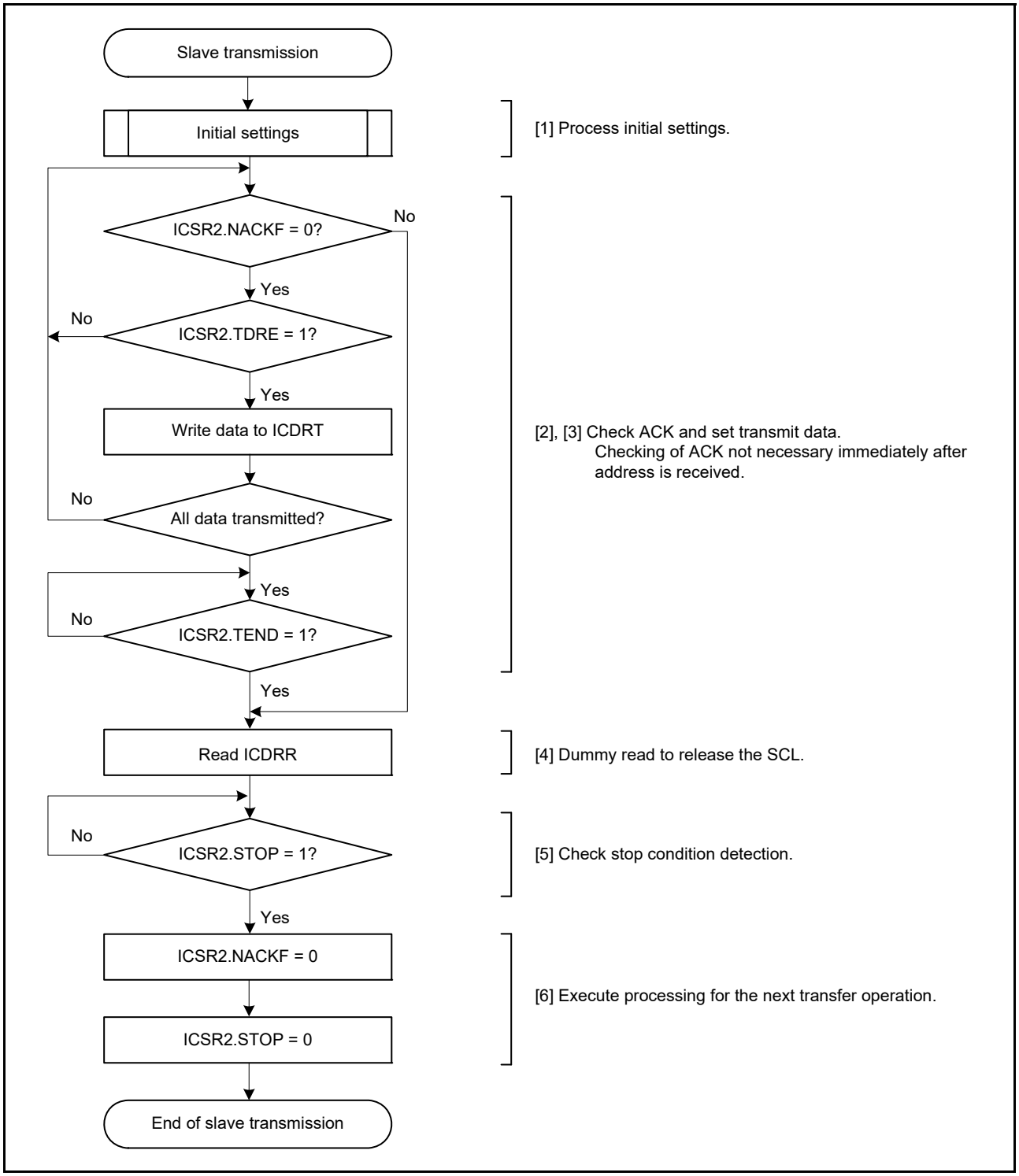


Figure 29.15 Example slave transmission flow

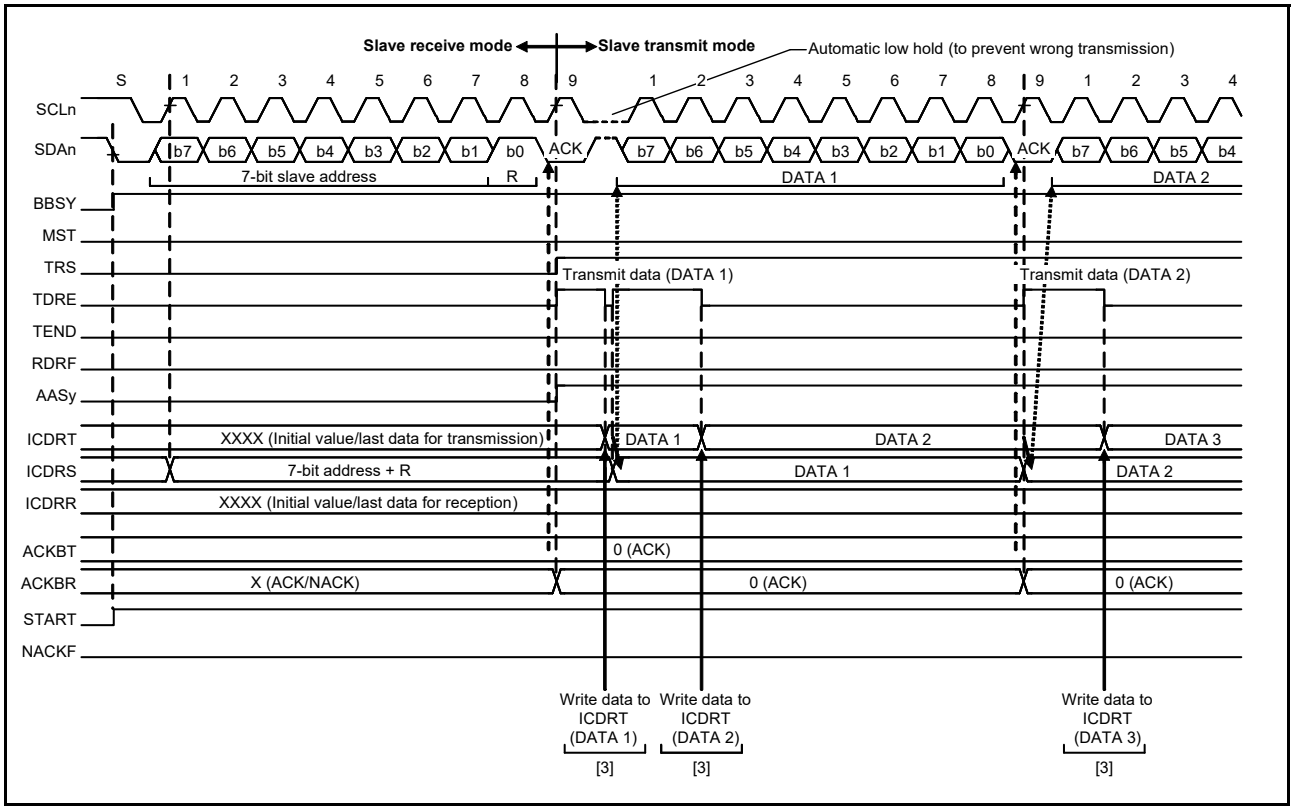


Figure 29.16 Slave transmit operation timing (1) with 7-bit address format

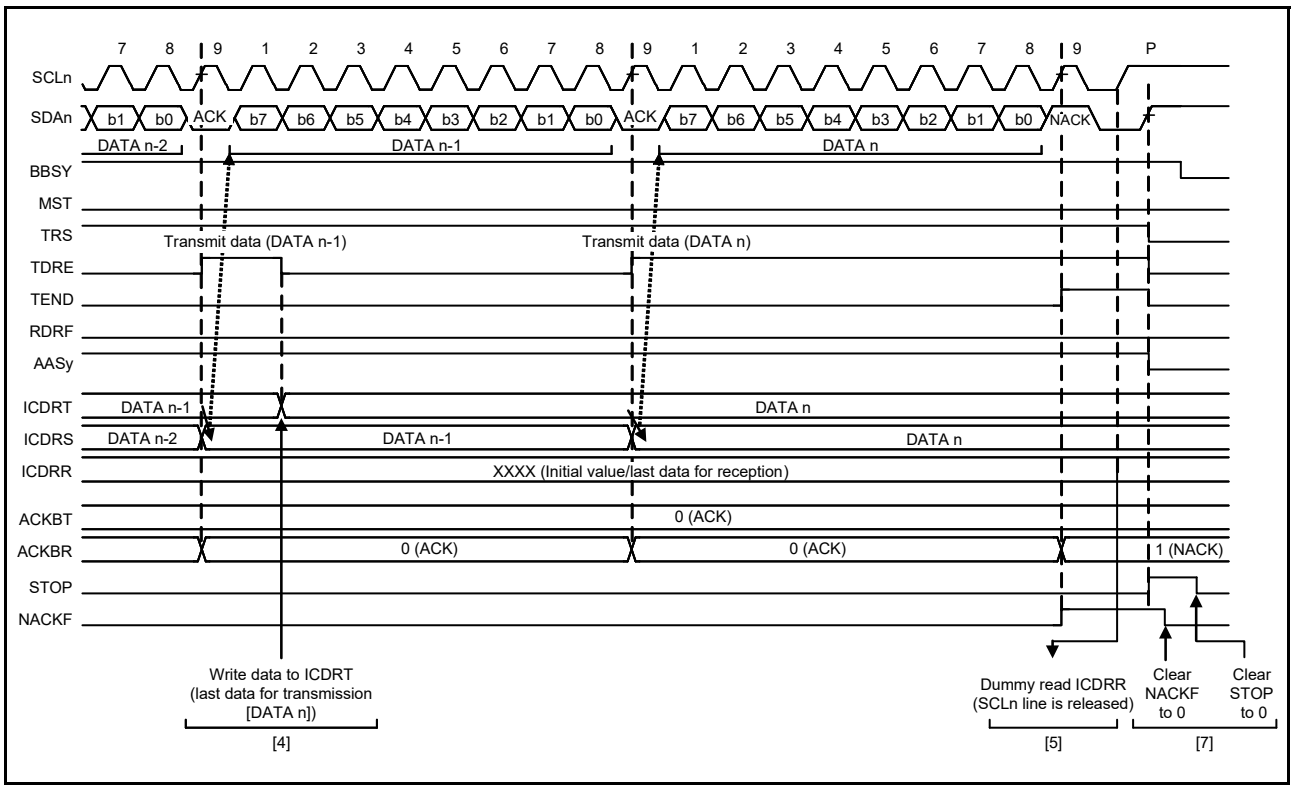


Figure 29.17 Slave transmit operation timing (2)

29.3.6 Slave Receive Operation

In a slave receive operation, the master device outputs the SCL clock and transmit data, and the IIC returns acknowledgments as a slave device.

Figure 29.18 shows an example of slave reception, and Figure 29.19 and Figure 29.20 show the operation timing in slave reception.

To set up and perform slave reception:

1. Initialize the IIC using the procedure in section 29.3.2, Initial Settings.
   After initialization, the IIC stays in the standby state until it receives a slave address that matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy (y = 0 to 2) flags to 1 on the rising edge of the 9th cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the 9th cycle of the SCL clock. If the value of the received R/W# bit is 0, the IIC continues to place itself in slave receive mode and sets the RDRF flag in ICSR2 to 1.
3. Check that the ICSR2.STOP flag is 0 and the ICSR2.RDRF flag is 1, and then dummy read the ICDRR register. The dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower 8 bits when the 10-bit address format is selected.
4. When ICDRR is read, the IIC automatically sets the ICSR2.RDRF flag to 0. If reading of ICDRR is delayed and the next byte is received while the RDRF flag is still set to 1, the IIC holds the SCLn line low until 1 SCL cycle before the point where RDRF must be set. In this case, reading ICDRR releases the SCLn line from being held at low. When the ICSR2.STOP flag is 1 and the ICSR2.RDRF flag is also 1, read ICDRR until all the data is completely received.
5. On detecting the stop condition, the IIC automatically set the ICSR1.HOA, GCA, and AASy (y = 0 to 2) flags in ICSR1 to 0.
6. Check that the ICSR2.STOP flag is 1, then set the ICSR2.STOP flag to 0 for the next transfer operation.

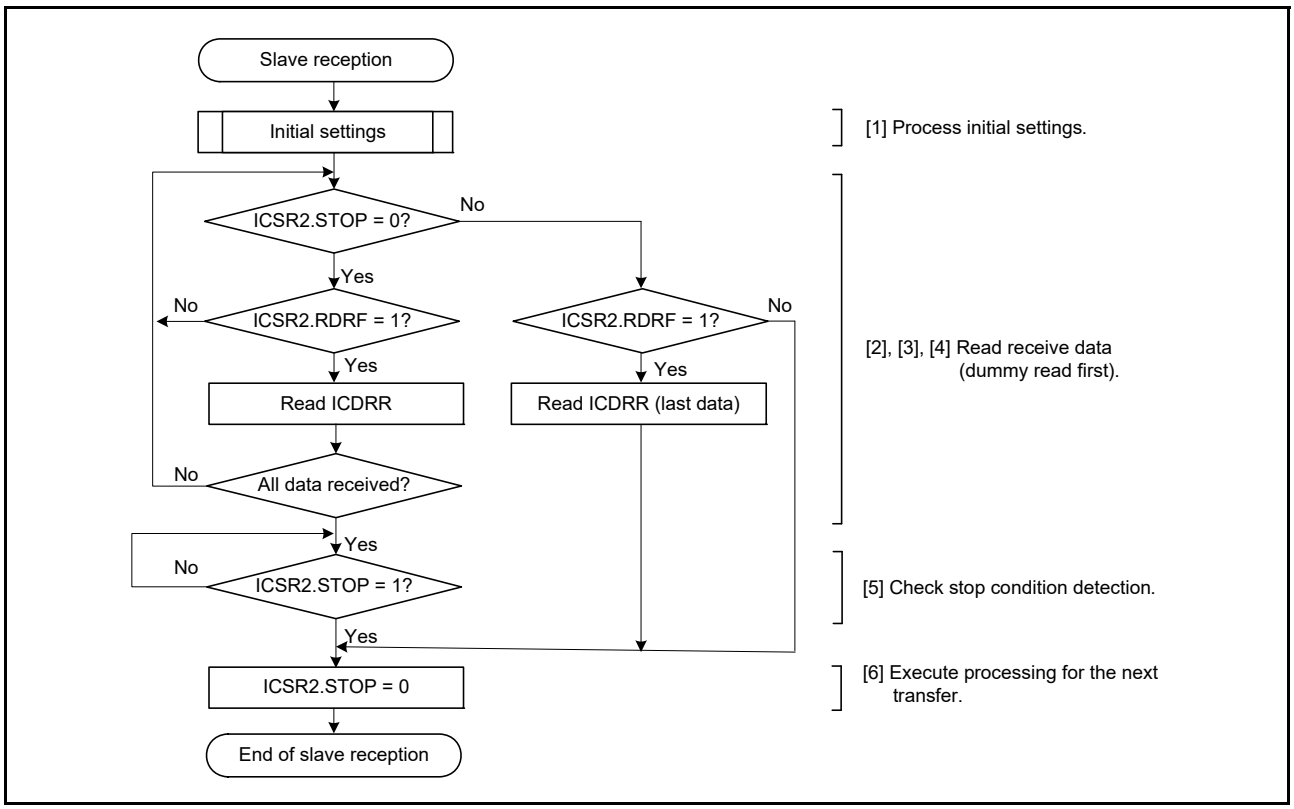


Figure 29.18 Example slave reception flow

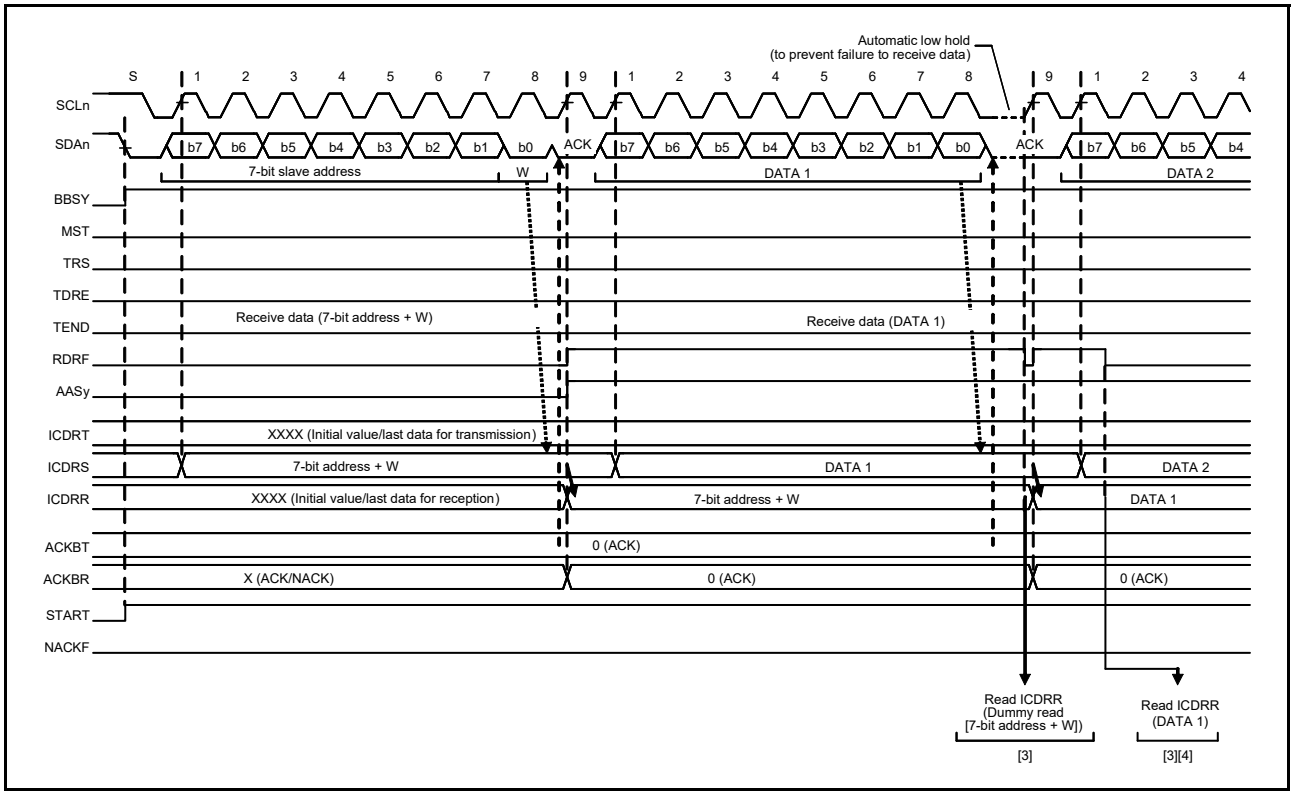


Figure 29.19 Slave receive operation timing (1) with 7-bit address format, when RDRFS = 0

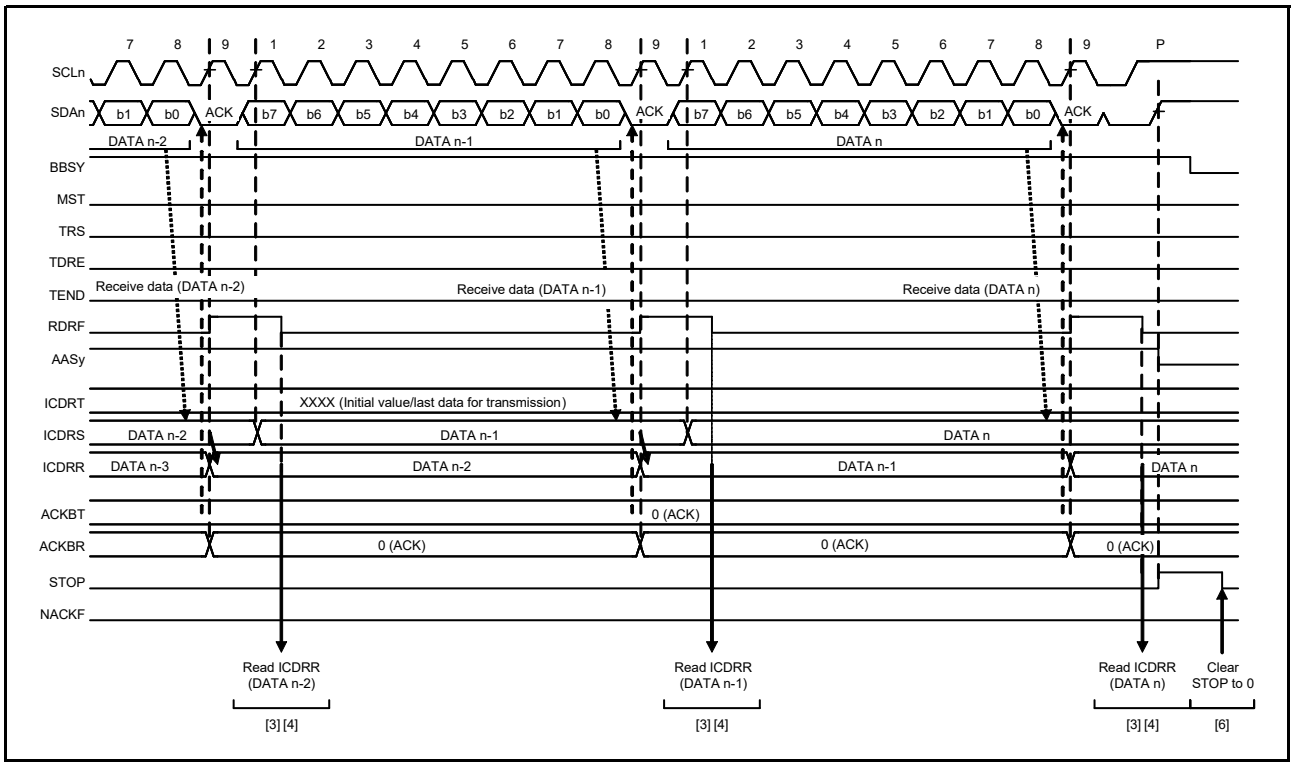


Figure 29.20 Slave receive operation timing (2) when RDRFS = 0

29.4 SCL Synchronization Circuit

To generate the SCL clock, the IIC starts counting the value for the high-level period specified in ICBRH when it detects a rising edge on the SCLn line, and drives the SCLn line low when it completes counting. When the IIC detects the falling edge of the SCLn line, it starts counting the value for the low-level period specified in ICBRL, and then stops driving the SCLn line (releases the line) when it completes counting. The IIC repeats this process to generate the SCL clock.

If multiple master devices are connected to the I2C bus, a collision of SCL signals might arise because of contention with another master device. In such cases, the master devices must synchronize their SCL signals. Because this synchronization of SCL signals must be bit-by-bit, IIC includes an SCL synchronization circuit to obtain bit-by-bit synchronization of the SCL clock signals by monitoring the SCLn line while in master mode.

When the IIC detects a rising edge on the SCLn line and starts counting the high-level period specified in ICBRH, and the level on the SCLn line falls because an SCL signal is being generated by another master device, the IIC performs the following:

1. Stops counting when it detects the falling edge.
2. Drives the level on the SCLn line low.
3. Starts counting the low-level period specified in ICBRL.

When the IIC finishes counting the low-level period, it stops driving the SCLn line low to release the line. If the low-level period of the SCL clock signal from the other master device is longer than the low-level period set in the IIC, the low-level period of the SCL signal is extended. When the low-level period for the other master device ends, the SCL signal rises because the SCLn line is released.

When the IIC finishes outputting the low-level period of the SCL clock, the SCLn line is released and the SCL clock rises. That is, when SCL signals from more than one master are contending, the high-level period of the SCL signal is synchronized with that of the clock with the narrower period, and the low-level period of the SCL signal is synchronized with that of the clock with the broader period. However, such synchronization of the SCL signal is only enabled when the SCLE bit in ICFER is set to 1.

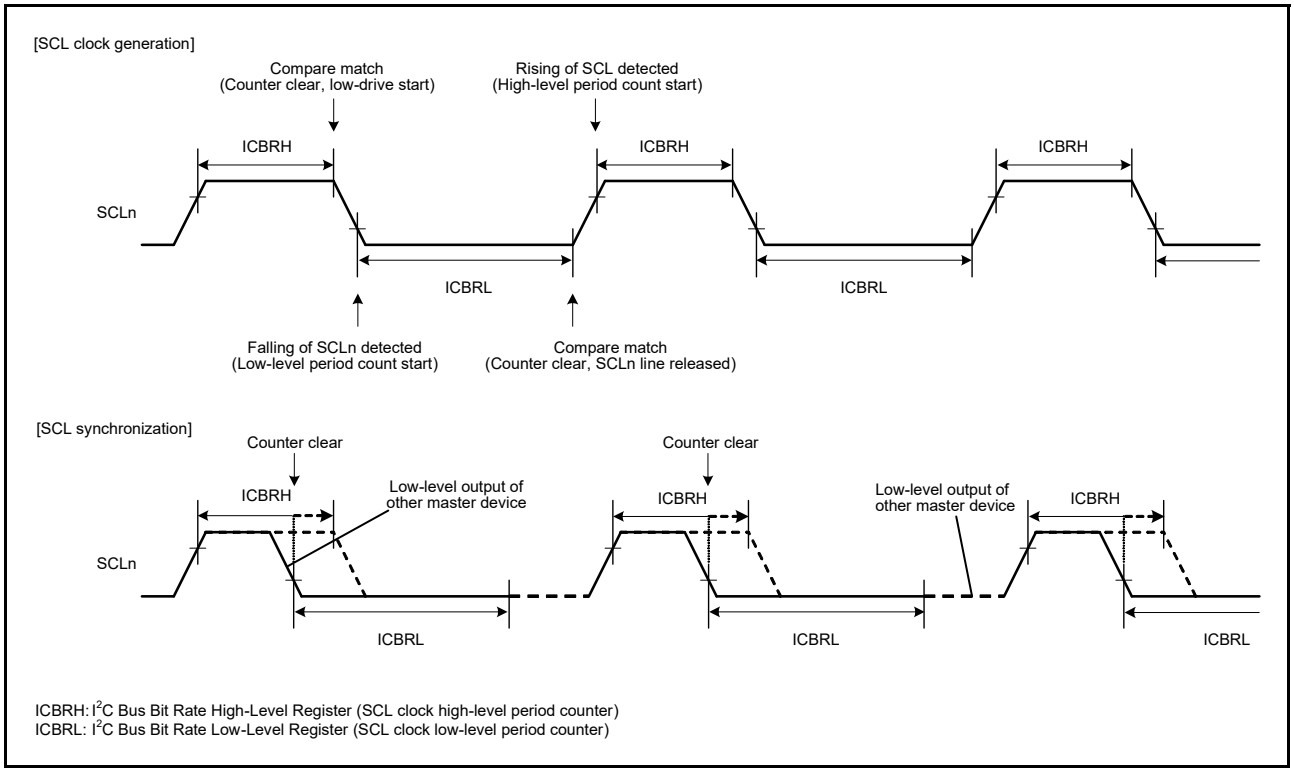


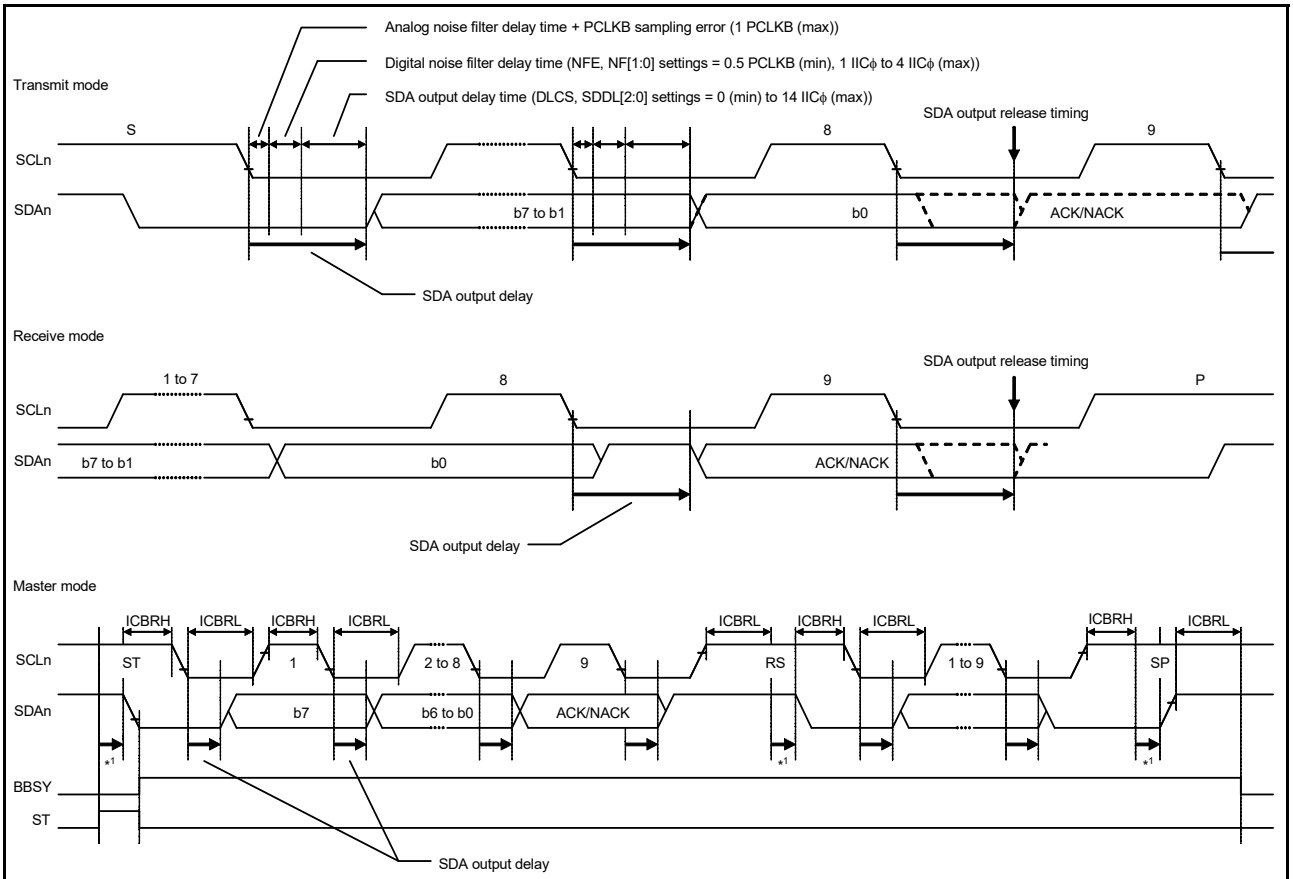
Figure 29.21 Generation and synchronization of SCL signal from the IIC

29.5 SDA Output Delay Function

The IIC module provides a function for delaying output on the SDA line. The delay can be applied to all outputs on the SDA line, including issuing of start, restart, and stop conditions, data, and the ACK and NACK signals.

With this function, SDA output is delayed from the detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval during which the SCL clock is low. This approach helps prevent erroneous operation of communication devices, with the aim of satisfying the 300-ns minimum data-hold time requirement of the SMBus specification. The output delay function is enabled by setting the SDDL[2:0] bits in ICMR2 to any value other than 000b, and disabled by setting the same bits to 000b.

When the SDA output delay function is enabled, for example, the DLCS bit in ICMR2 selects the clock source for the SDA output delay counter, either as the internal base clock (IICϕ) for the IIC module or as the internal base clock divided by two (IICϕ/2). The counter counts the number of cycles set in the SDDL[2:0] bits in ICMR2. When the delay count is reached, the IIC module places the required output (start, restart, or stop condition, data, or an ACK or NACK signal) on the SDA line.



Note 1. The output delay function is set by the DLCS and SDDL[2:0] bits when a start (ST), restart (RS), or stop (SP) condition is issued.

Figure 29.22 SDA output delay function

29.6 Digital Noise Filter Circuits

The internal circuitry sees the states of the SCLn and SDAn pins through analog and digital noise-filter circuits. Figure 29.23 shows a block diagram of the digital noise-filter circuit.

The on-chip digital noise-filter circuit of the IIC consists of four flip-flop circuit stages connected in series, and a match-detection circuit.

The number of valid stages in the digital noise filter is selected in the NF[1:0] bits in ICMR3. The selected number of valid stages determines the noise-filtering capability as a period from 1 to 4 IICϕ cycles.

The input signal to the SCLn pin (or SDAn pin) is sampled on falling edges of the IICϕ signal. When the input signal level matches the output level of the number of valid flip-flop circuit stages as selected in the NF[1:0] bits in ICMR3, the signal level is seen in the subsequent stage. If the signal levels do not match, the previous value is saved.

If the ratio between the frequency of the internal operating clock (PCLKB) and the transfer rate is small, for example, for a data transfer at 400 kbps with PCLKB at 4 MHz, the digital noise filter might lead to the elimination of the required signals as noise. In such cases, it is possible to disable the digital noise-filter circuit by setting the ICFER.NFE bit to 0, and use only the analog noise-filter circuit.

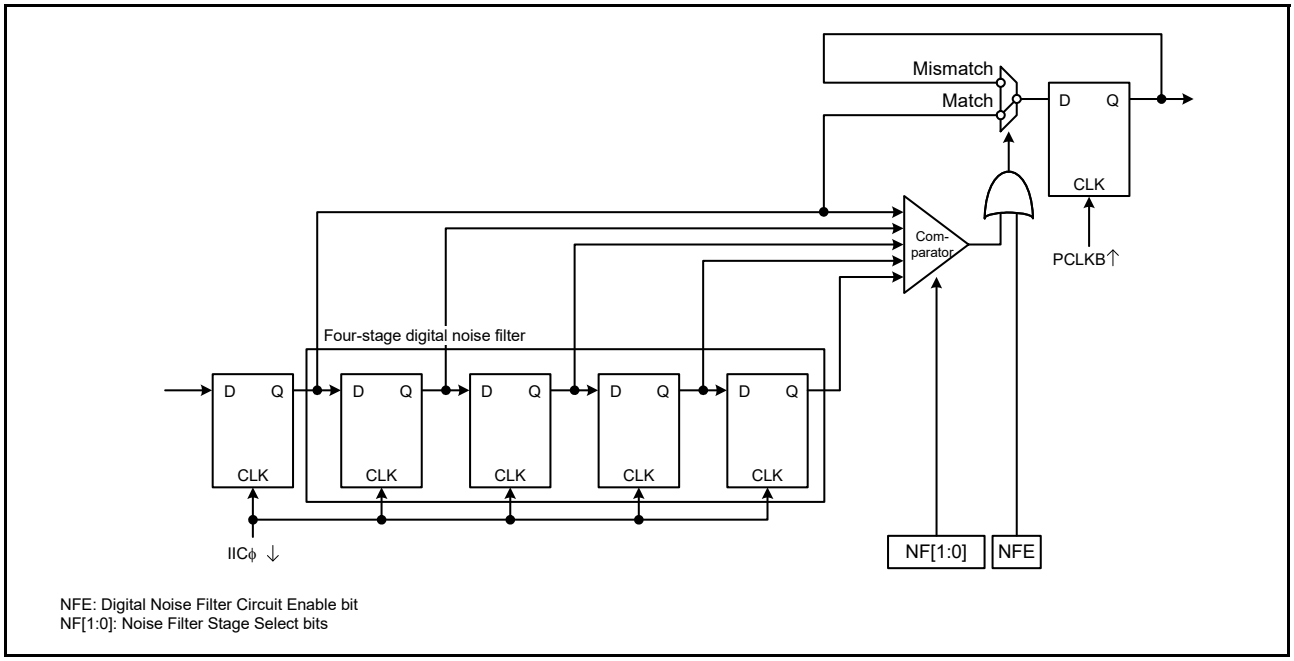


Figure 29.23 Digital noise-filter circuit block diagram

29.7 Address Match Detection

The IIC can set three unique slave addresses in addition to the general call address and host address. The slave addresses can be 7-bit or 10-bit slave addresses.

29.7.1 Slave-Address Match Detection

The IIC can set three unique slave addresses and has a slave address detection function for each unique slave address. When the SARyE bit (y = 0 to 2) in ICSER is set to 1, the slave addresses set in SARUy and SARLy (y = 0 to 2) can be detected.

When the IIC detects a match of the set slave address, the associated AASy (y = 0 to 2) flag in ICSR1 is set to 1 on the rising edge of the 9th SCL clock cycle, and the RDRF flag or TDRE flag in ICSR2 is set to 1 by the subsequent R/W# bit. This causes a receive data full interrupt (IICn_RXI) or transmit data empty interrupt (IICn_TXI) to be generated. The AASy flag identifies which slave address is specified.

Figure 29.24 to Figure 29.26 show the AASy flag set timing in three cases.

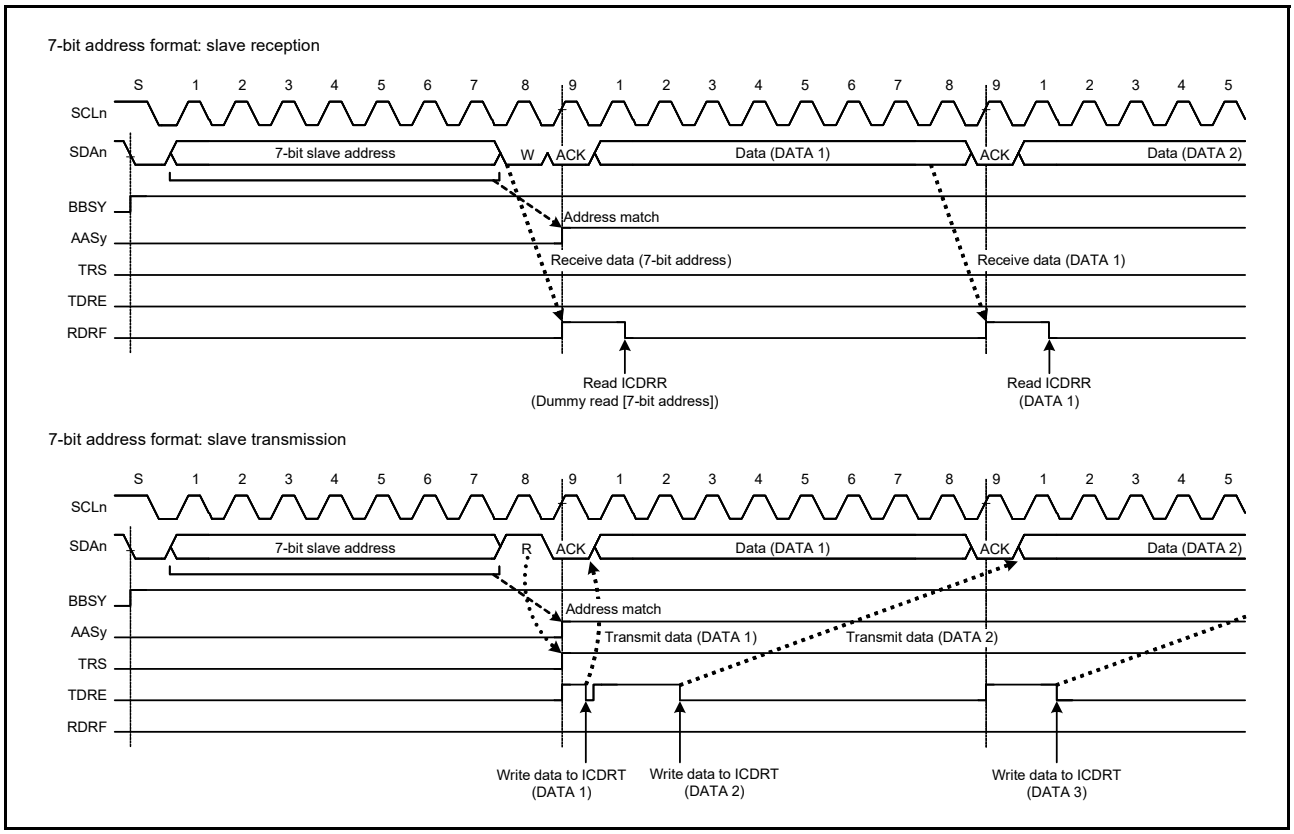


Figure 29.24 AASy flag set timing with 7-bit address format

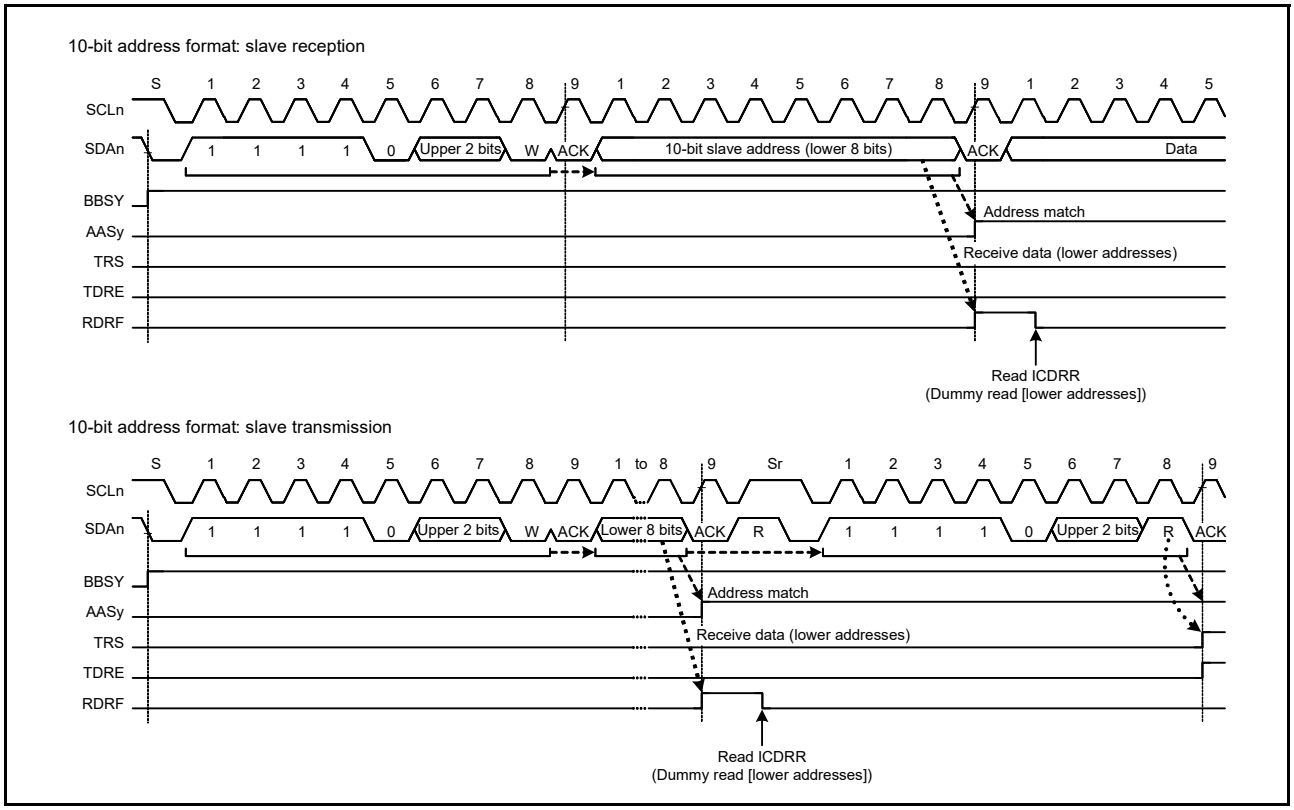


Figure 29.25 AASy flag set timing with 10-bit address format

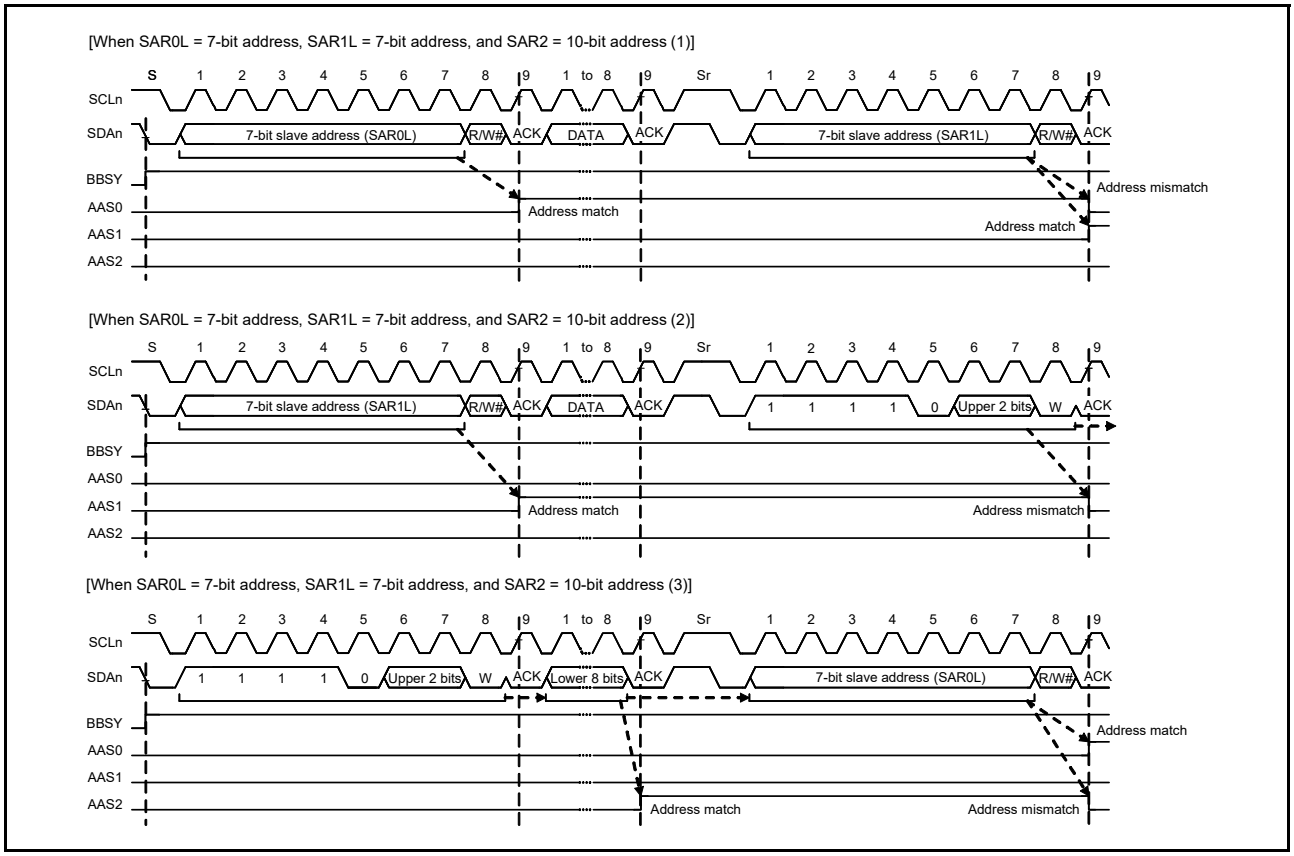


Figure 29.26 AASy flag set and clear timing with 7-bit and 10-bit address formats mixed

29.7.2 Detection of General Call Address

The IIC provides detection of the general call address (0000 000b + 0 [W]). General call address detection is enabled by setting the GCAE bit in ICSER to 1.

If the address received after a start or restart condition is issued is 0000 000b + 1[R] (start byte), the IIC recognizes this as the address of a slave device with an all-zero address, but not as the general call address.

When the IIC detects the general call address, both the GCA flag in ICSR1 and the RDRF flag in ICSR2 are set to 1 on the rising edge of the 9th cycle of the SCL clock. This leads to the generation of a receive data full interrupt (IICn_RXI). The value of the GCA flag can be checked to confirm that the general call address was transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

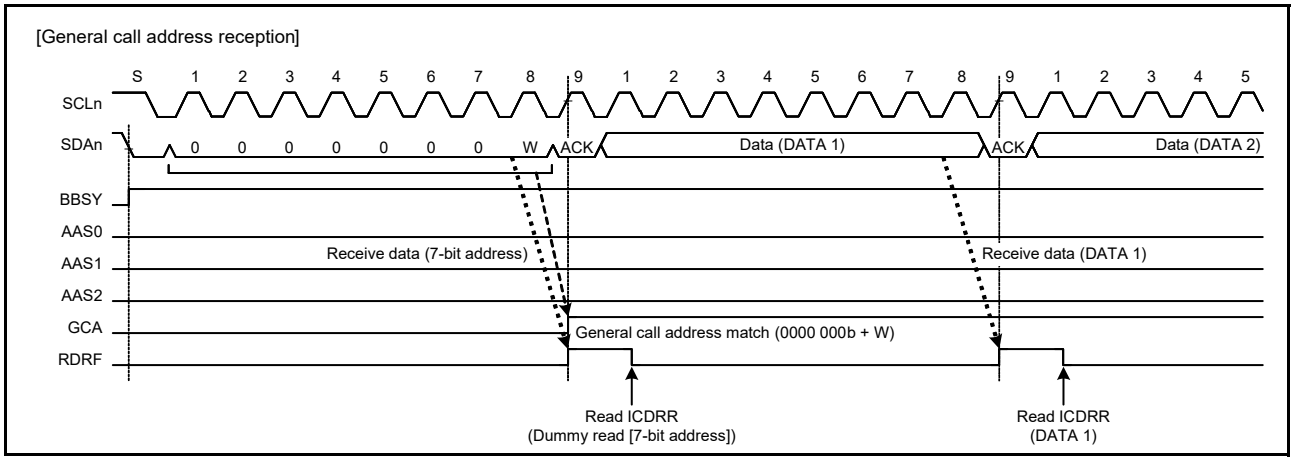


Figure 29.27 Timing of GCA flag setting during reception of general call address

29.7.3 Device ID Address Detection

The IIC module provides detection of the device ID address in compliance with the I2C bus specification, revision 03. When the IIC receives 1111 100b as the first byte after a start or restart condition is issued with the DIDE bit in ICSER set to 1, it recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the 8th SCL clock cycle when the subsequent R/W# bit is 0, then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the IIC sets the associated AASy (y = 0 to 2) flag in ICSR1 to 1.

When the first byte received after the issue of a start or restart condition matches the device ID address (1111 100b) again and the subsequent R/W# bit is 1, the IIC does not compare the second and subsequent bytes, and sets the ICSR2.TDRE flag to 1.

In the device ID address detection function, the IIC sets the DID flag to 0 if a match with the IIC slave address is not obtained, or a match with the device ID address is not obtained after a match with the IIC slave address, and a restart condition is detected. If the first byte after the detection of a start or restart condition matches the device ID address (1111 100b) and the R/W# bit is 0, the IIC sets the DID flag to 1 and compares the second and subsequent bytes with the slave address of IIC. If the R/W# bit is 1, the DID flag holds the previous value and the IIC does not compare the second and subsequent bytes. Therefore, the reception of a device ID address can be checked by reading the DID flag after confirming that TDRE = 1.

Additionally, prepare the device ID fields (3 bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device ID field as normal transmit data. For details on the information that must be included in device ID fields, contact NXP Semiconductors.

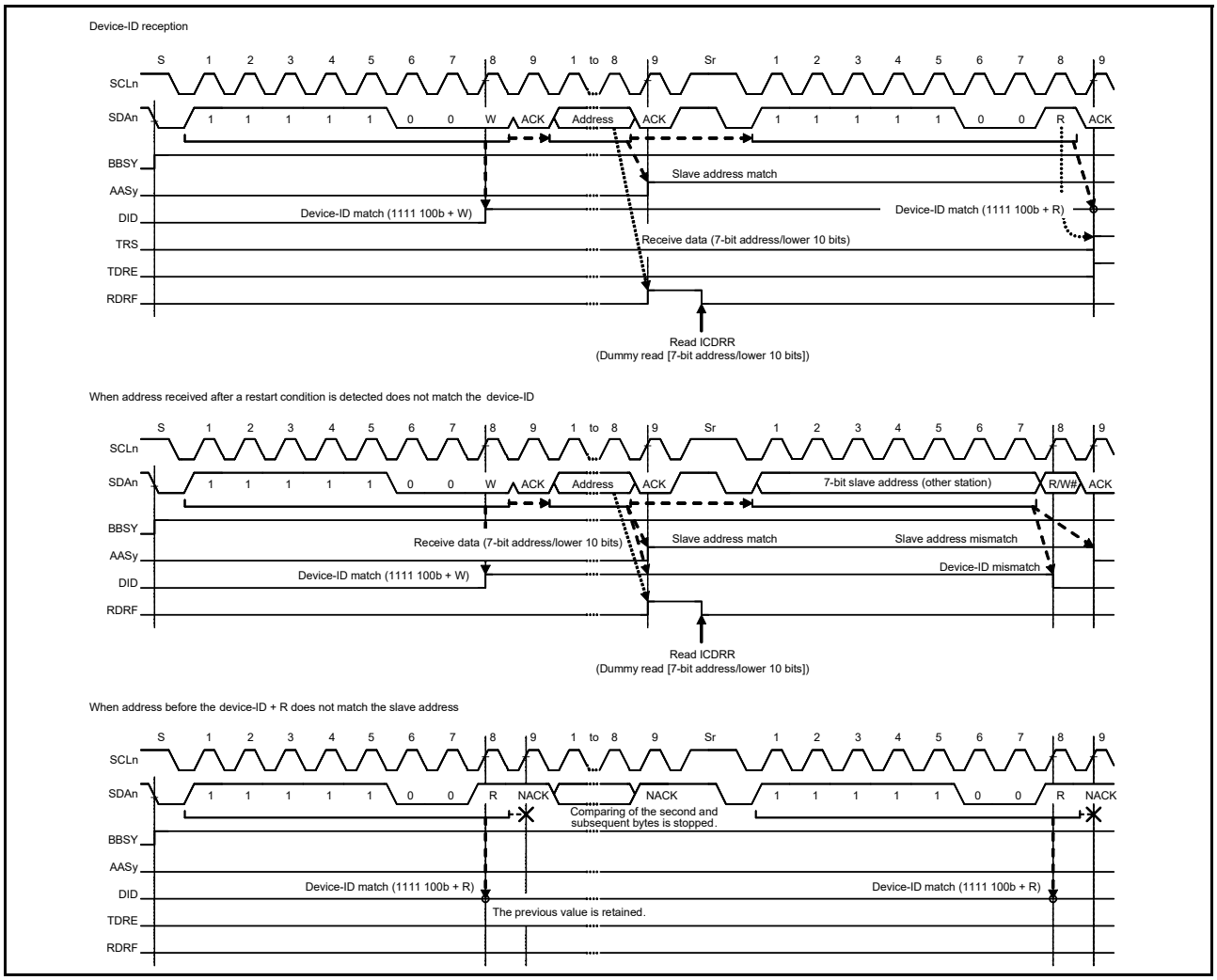


Figure 29.28 AASy and DID flag set and clear timing during reception of device ID

29.7.4 Host Address Detection

The IIC provides host address detection when operating in SMBus mode. When the HOAE bit in ICSER is set to 1 while the SMBS bit in ICMR3 is 1, the IIC can detect the host address (0001 000b) in slave receive mode (MST and TRS bits = 00b in ICCR2).

When the IIC detects the host address, the HOA flag in ICSR1 is set to 1 on the rising edge of the 9th SCL clock cycle. At the same time, the RDRF flag in ICSR2 is set to 1 when the R/W# bit is 0 (Wr bit). This causes a receive data full interrupt (IICn_RXI) to be generated. The HOA flag indicates that the host address was sent from another device.

If the bit following the host address (0001 000b) is a read bit (R/W# bit = 1), the IIC can also detect the host address. After the host address is detected, the IIC operates in the same manner as in normal slave operation.

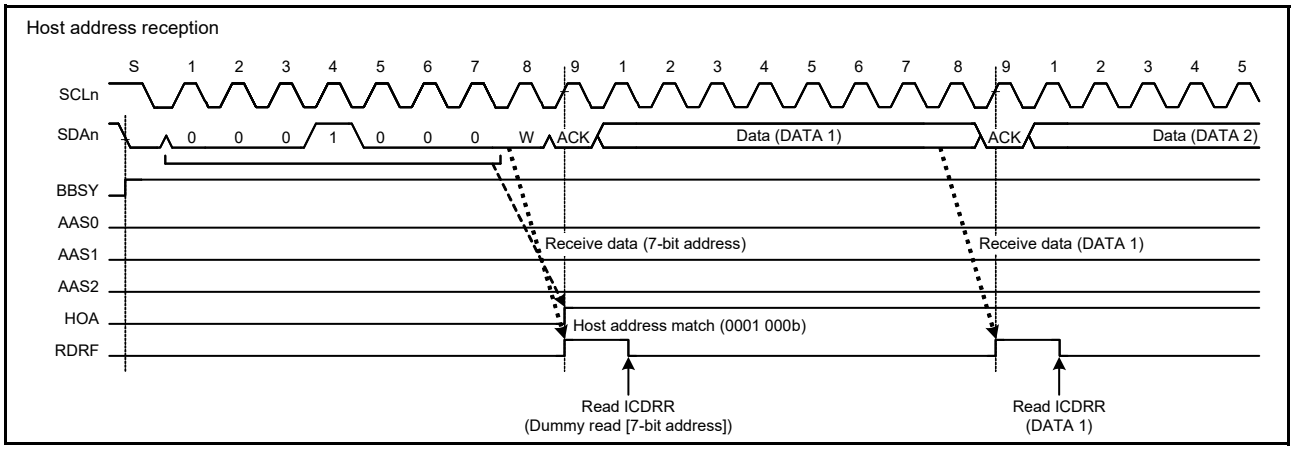


Figure 29.29 HOA flag set timing during reception of host address

29.8 Wakeup Function

The IIC provides a wakeup function that causes the MCU to transition from Software Standby mode to normal operation. The wakeup function enables the reception of data when the system clock is stopped, and generates a wakeup interrupt signal on a match of the slave address of the received data. This wakeup interrupt signal triggers the return to normal operation.

The wakeup function has four operation modes:

- Normal wakeup mode 1
- Normal wakeup mode 2
- Command recovery mode
- EEP response mode.

Table 29.9 describes the behavior in these modes.

Table 29.9 Wakeup operation modes

Operation mode	ACK response timing	ACK response before wakeup	SCL state during wakeup
Normal wakeup mode 1	Before wakeup	ACK	Fixed low
Normal wakeup mode 2	After wakeup	Before wakeup: no response After wakeup: ACK response	Fixed low
Command recovery mode	Before wakeup	ACK	Open
EEP response mode	Before wakeup	NACK	Open

Precautions on the use of the wakeup function

1. Disable the wakeup function (WUE = 0) after a wakeup interrupt triggers the transition from Software Standby mode to normal operation.

2. Do not change the content of the IIC registers while WUF = 0, even if the wakeup interrupt recovers the system clock. Specify the register settings after confirming that WUF = 1.
3. Set WUE = WUIE = 1 and MST = TRS = 0 (slave reception mode) before entering Software Standby mode.
4. Do not transition to Software Standby mode while BBSY = 1.
5. The wakeup function supports the 7-bit slave address of the slave address register SARL0, the general call address, and the host address. 10-bit slave addresses, SARL1 and SARL2, are not supported.
6. When the wakeup function is enabled, disable the interrupts selectable in the TIE, TEIE, RIE, NAKIE, SPIE, STIE, ALIE, and TMOIE bits in the ICIER register.
7. When the wakeup function is enabled, do not use the timeout function.
8. If the transition from Software Standby mode is triggered by an interrupt other than a wakeup interrupt, for example, the IRQn, the WUF flag is not set to 1. Follow the procedures shown in Figure 29.31 and Figure 29.36.

29.8.1 Normal Wakeup Mode 1

This section describes the behavior, timing, and an example operation in normal wakeup mode 1.

In normal wakeup mode 1, a wakeup interrupt triggered by the match of the slave address initiates the transition to normal operation as follows:

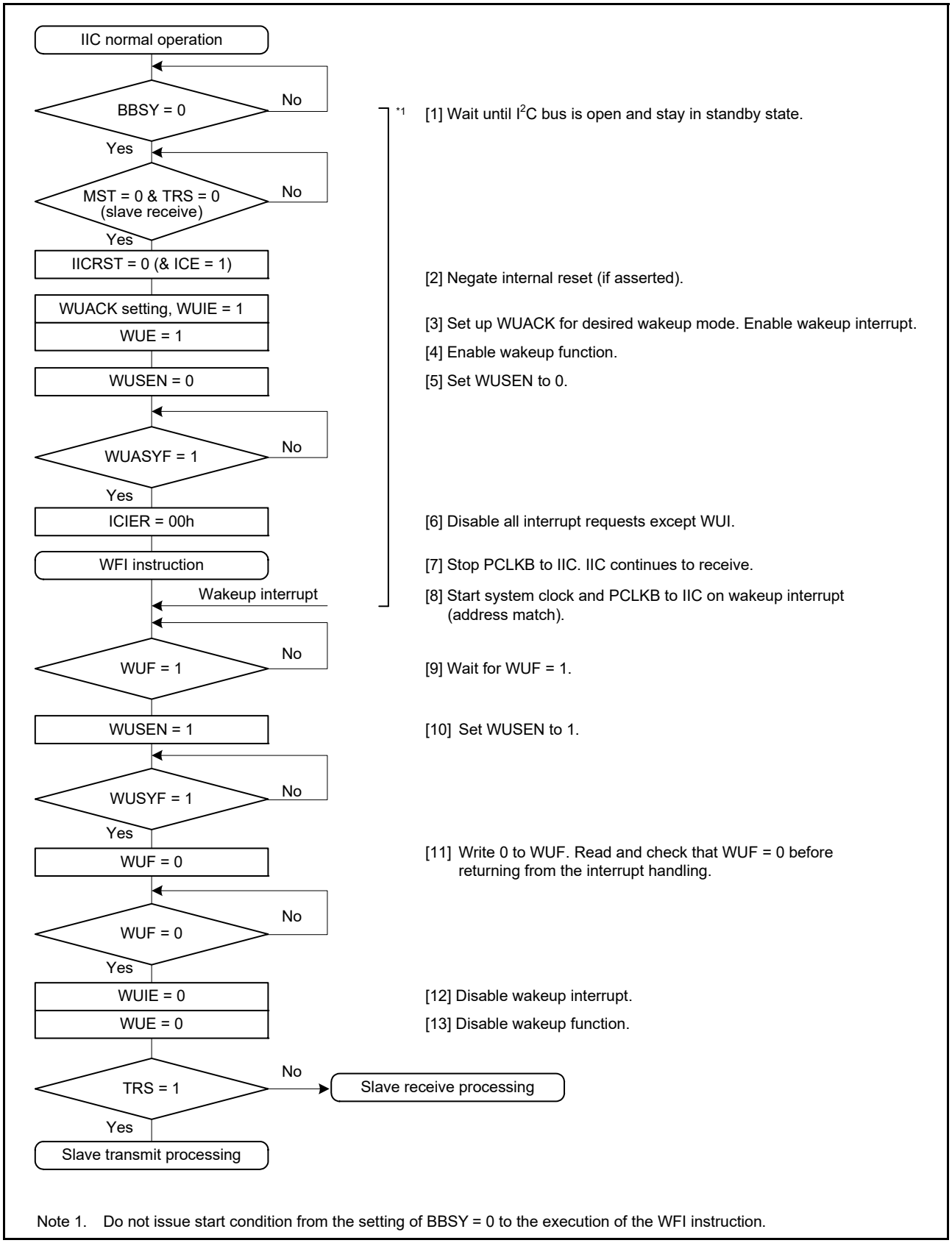
Before wakeup: ACK is sent in response to the data received with its own slave address of the IIC.
During wakeup: ACK response is made on the 9th clock cycle of SCL, after which SCL is held low*1.
After wakeup: Normal operation continues.

If the slave address does not match, the SCL line is not held low after the 9th clock cycle of SCL, and the slave operation continues.

Figure 29.30 shows an operation example, and Figure 29.32 shows the detailed timing.

Note 1. Between the 9th clock cycle and the 1st clock cycle during wakeup, WAIT = 1 is invalid.

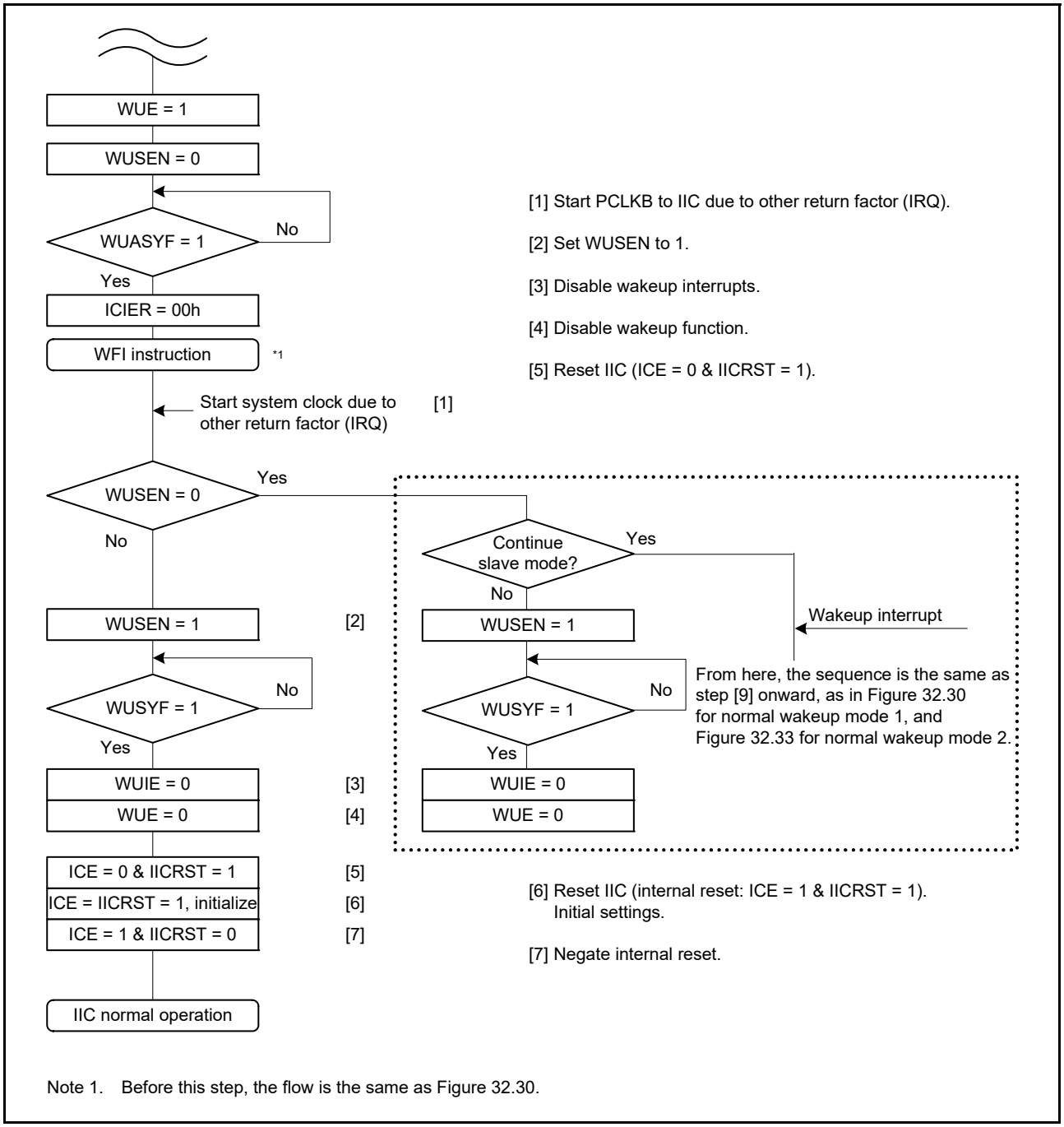
If the transition from Software Standby mode is triggered by an interrupt other than a wakeup interrupt, for example the IRQn, the WUF flag is not set to 1. Figure 29.31 shows an operation example.



Note 1. Do not issue start condition from the setting of BBSY = 0 to the execution of the WFI instruction.

Figure 29.30 Example operation of normal wakeup mode 1 when wakeup is triggered by a wakeup interrupt on match of the slave address

Note: See Precautions on the use of the wakeup function.



Note 1. Before this step, the flow is the same as Figure 32.30.

Figure 29.31 Example operation of normal wakeup modes 1 and 2 when wakeup is triggered by an interrupt other than IIC wakeup interrupt, for example, the IRQn

Note: For details on the IIC initial settings, see section 29.3.2, Initial Settings.

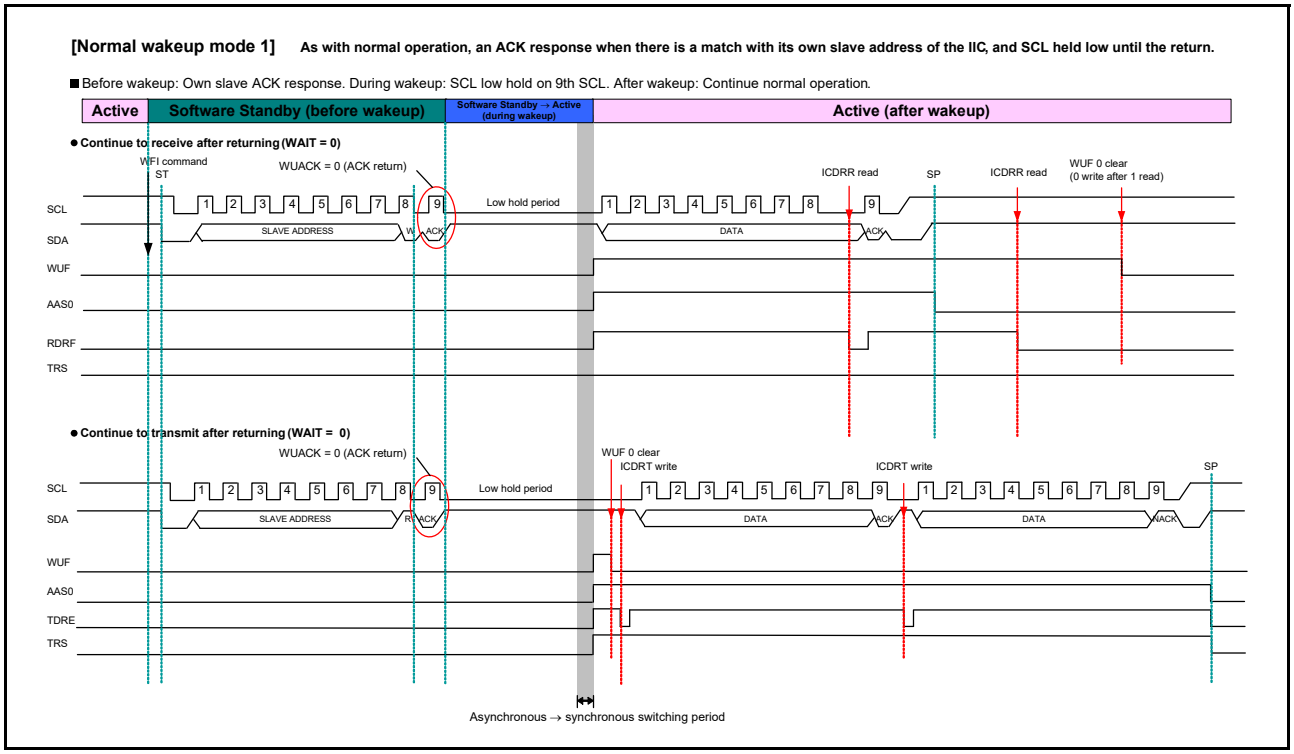


Figure 29.32 Timing of normal wakeup mode 1

29.8.2 Normal Wakeup Mode 2

This section describes the behavior, timing, and an example operation of normal wakeup mode 2.

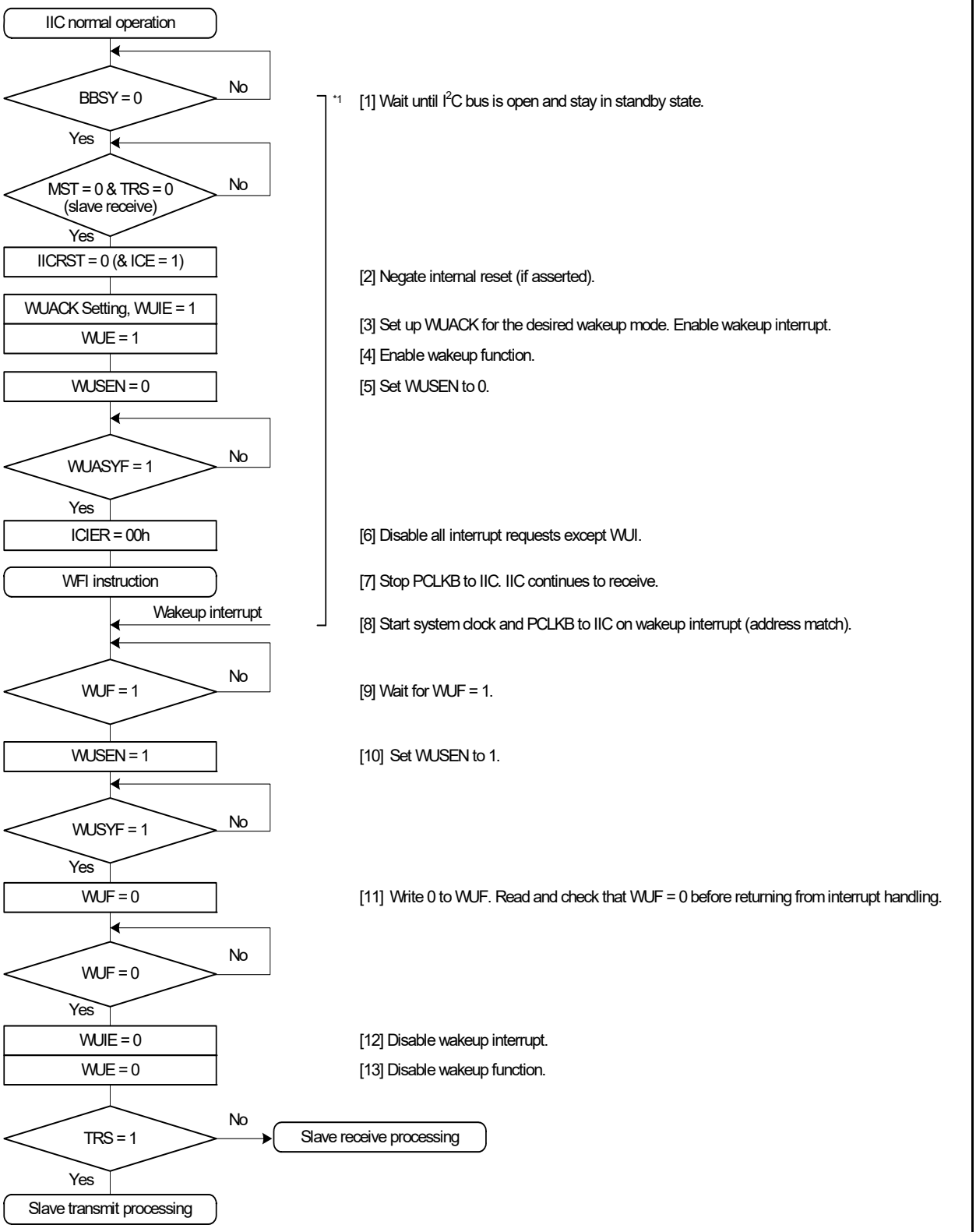
In normal wakeup mode 2, a wakeup interrupt triggered by a match of the slave address initiates the transition to normal operation as follows:

Before wakeup: No response to data received with its own slave address until the end of the 8th SCL cycle.
During wakeup: SCL line held low during the 8th and 9th clock cycles.
After wakeup: ACK returns on the 9th clock cycle of SCL, and normal operation continues.

If the slave address does not match, the SCL line is not held low after the 8th SCL clock cycle, and the slave operation continues.

Figure 29.33 shows an example operation, and Figure 29.34 shows the detailed timing.

If the transition from Software Standby mode is triggered by an interrupt other than a wakeup interrupt, such as the IRQn for example, the WUF flag is not set to 1. Figure 29.31 shows an operation example.



Note 1. Do not issue start condition from the setting of BBSY = 0 to the execution of the WFI instruction.

Figure 29.33 Example operation of normal wakeup mode 2 when wakeup is triggered by a wakeup interrupt on match of the slave address

Note: See Precautions on the use of the wakeup function.

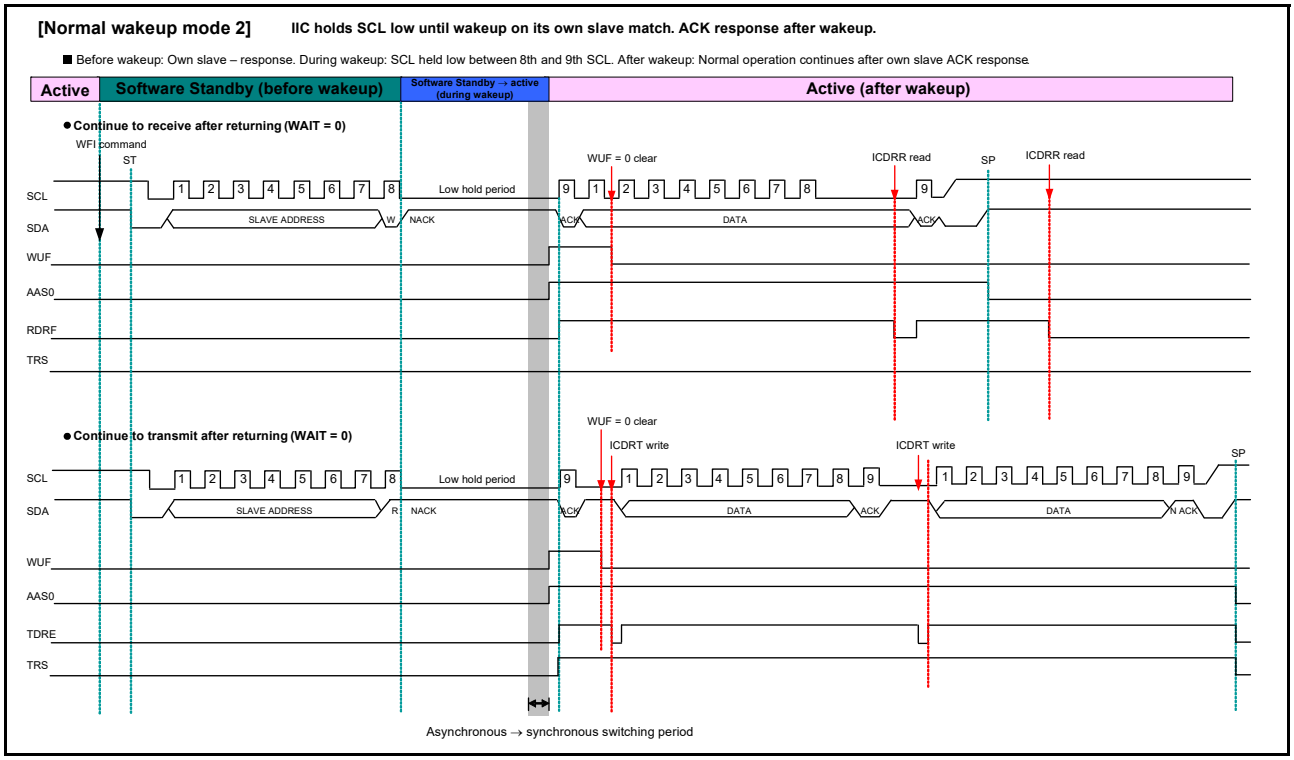


Figure 29.34 Timing of normal wakeup mode 2

29.8.3 Command Recovery Mode and EEP Response Mode (Special Wakeup Modes)

This section describes the behavior, timing, and an example operation in the command recovery and EEP response modes.

In the command recovery and EEP response modes, the SCL line is not held low during the wakeup period (after the rise of the 9th clock cycle of SCL). Therefore, other IIC devices can use the I2C bus during this period.

A wakeup interrupt triggered by a match of the slave address initiates the transition to normal operation as follows:

Before wakeup: In response to data received with its own slave address, the IIC returns ACK (command recovery mode) or NACK (EEP response mode).

During wakeup: The SCL line is not held low.

After wakeup: Normal operation continues after IIC initialization.

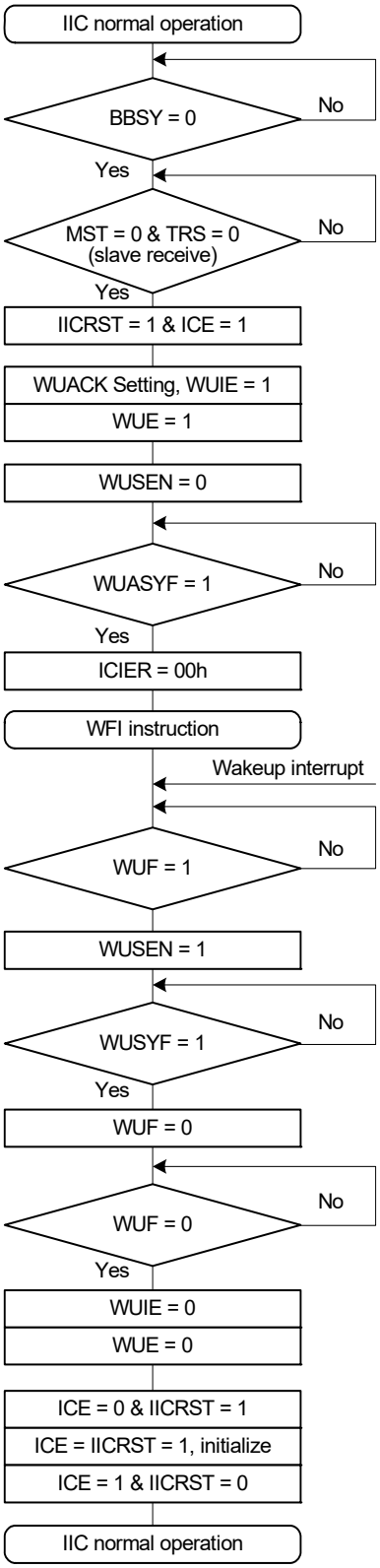
If the slave address does not match, the slave operation continues.

Note: Because the SCL line is not held low during wakeup, transmission or reception of the data that follows the slave address is not possible.

Note: The command recovery and EEP response modes are internal reset states (ICE = IICRST = 1). Therefore, the match of the slave address does not set the flags HOA, GCA, ASS0, ASS1, and ASS2 in the ICSR1 register.

Figure 29.35 shows an example of operation in command recovery and EEP response modes. Figure 29.37 shows the detailed timing.

If the transition from Software Standby mode is triggered by an interrupt other than a wakeup interrupt, for example the IRQn, the WUF flag is not set to 1. Figure 29.36 shows an operation example.



*1 [1] Wait until I2C bus is open and stay in standby state.

[2] Internal reset is asserted.

[3] Set up WUACK for the desired wakeup mode. Enable wakeup interrupt.

[4] Enable wakeup function.

[5] Set WUSEN to 0.

[6] Disable all interrupt requests except WUI.

[7] Stop PCLKB to IIC. IIC continues to receive.

[8] Start system clock and PCLKB to IIC on wakeup interrupt (address match).

[9] Wait for WUF = 1.

[10] Set WUSEN = 1.

[11] Write 0 to WUF. Read and check that WUF = 0 before returning from interrupt handling.

[12] Disable wakeup interrupt.

[13] Disable wakeup function.

[14] Reset IIC (ICE = 0 & IICRST = 1).

[15] Reset IIC (internal reset: ICE = 1 & IICRST = 1). Specify initial settings.

[16] Negate internal reset.

Note 1. Do not issue start condition from the setting of BBSY = 0 to the execution of the WFI instruction.

Figure 29.35 Example operation of command recovery and EEP response modes when wakeup is triggered by a wakeup interrupt on match of the slave address

Note: See Precautions on the use of the wakeup function.

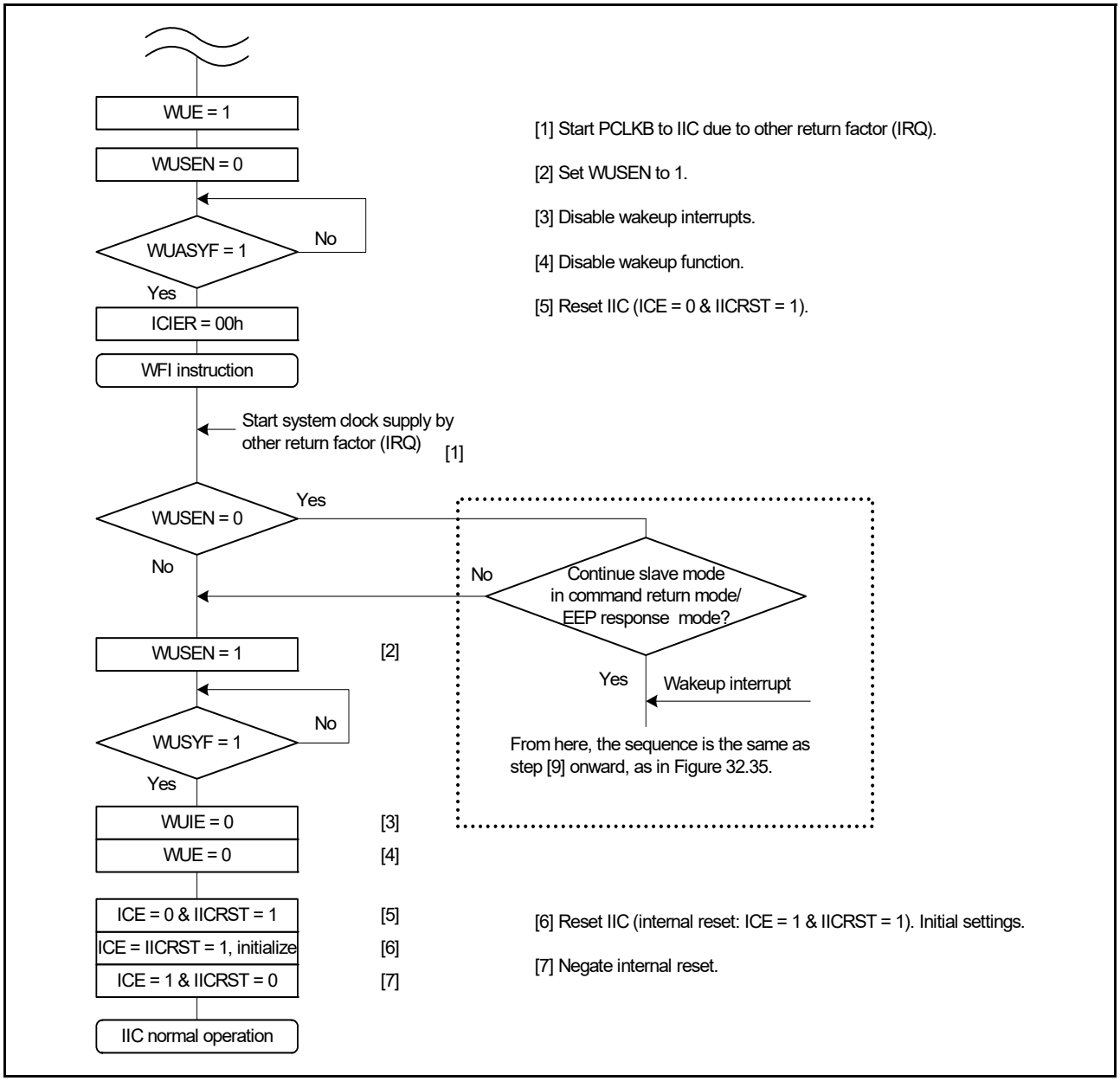


Figure 29.36 Example operation of command recovery mode and EEP response mode when wakeup is triggered by the interrupt other than IIC wakeup interrupt, for example, the IRQn

Note: For details on the IIC initial settings, see section 29.3.2, Initial Settings.

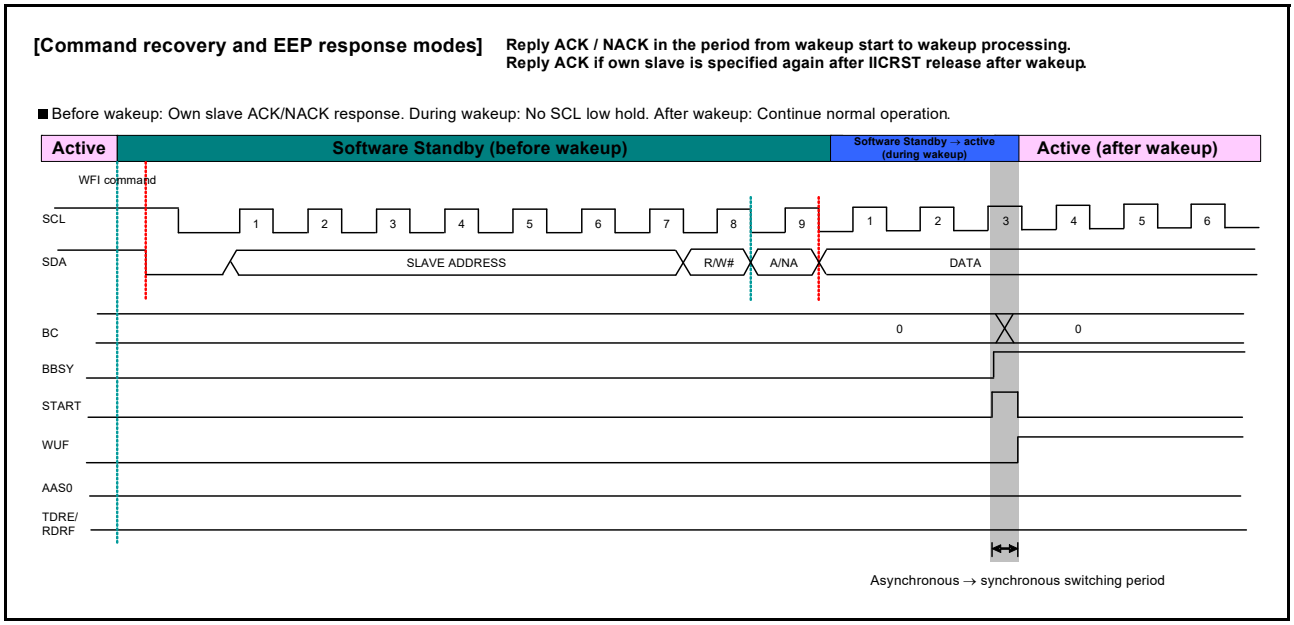


Figure 29.37 Timing of command recovery and EEP response modes

29.8.4 Precautions for WFI Instruction Execution

In the wakeup function examples shown in Figure 29.30, Figure 29.33, and Figure 29.35, make sure that the start condition is not issued during the period from the setting of BBSY = 0 to the execution of the WFI instruction.

When a start condition is issued during this period, NACK is returned after the reception of the first byte of the first data block. Detection of the start or restart condition then enables the wakeup function.

29.9 Automatic Low-Hold Function for SCL

29.9.1 Function to Prevent Wrong Transmission of Transmit Data

If the I2C Bus Shift Register (ICDRS) is empty when data has not been written to the I2C Bus Transmit Data Register (ICDRT) with the IIC in transmission mode (ICCR2.TRS bit = 1), the SCLn line is automatically held at the low level over the subsequent intervals. This low-hold period is extended until the transmit data is written, which prevents the unintended transmission of erroneous data.

Master transmit mode:

- Low-level interval after a start or restart condition is issued
- Low-level interval between the 9th clock cycle of one transfer and the 1st clock cycle of the next.

Slave transmit mode:

- Low-level interval between the 9th clock cycle of one transfer and the 1st clock cycle of the next.

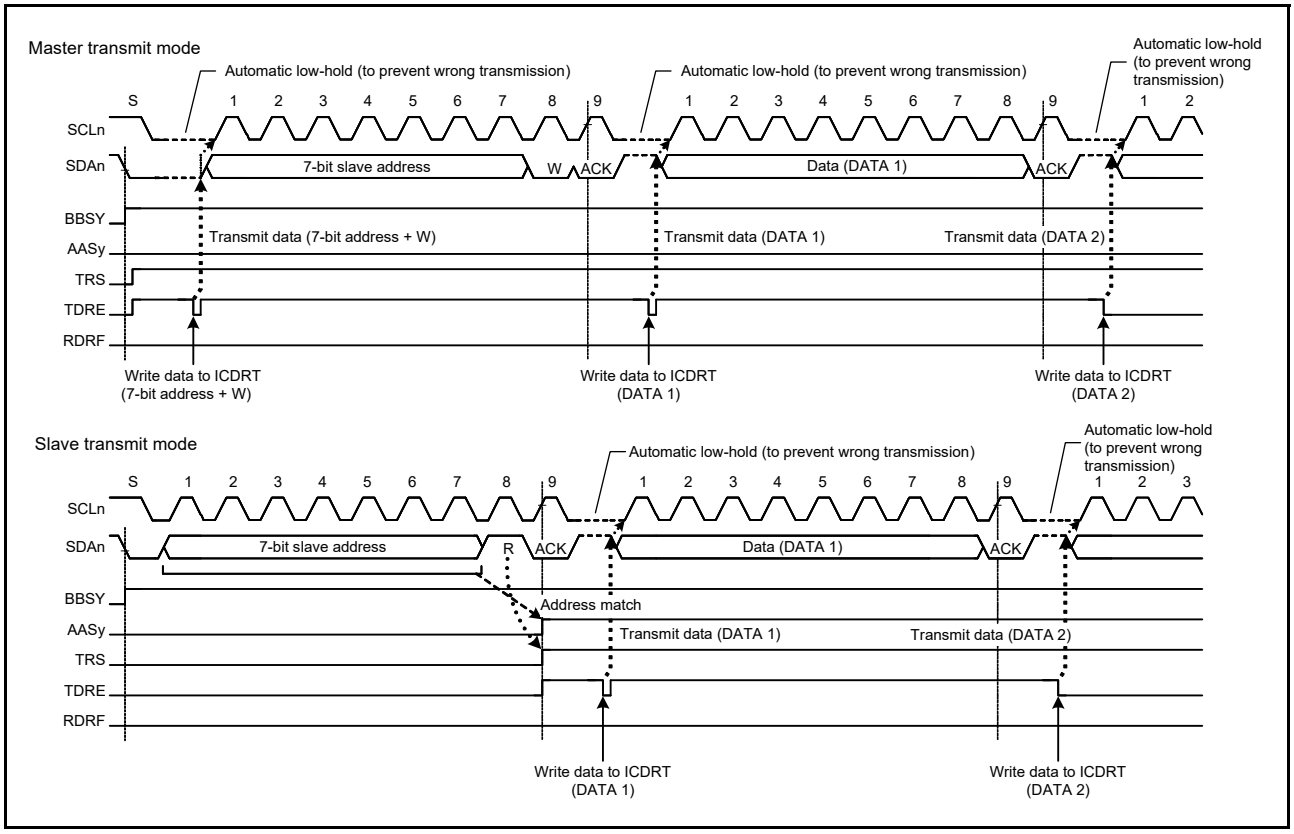


Figure 29.38 Automatic low-hold operation in transmit mode

29.9.2 NACK Reception Transfer Suspension Function

This function suspends transfer operation when NACK is received in transmit mode (ICCR2.TRS bit = 1). This function is enabled when the NACKE bit in ICFER is set to 1 (transfer suspension enabled). If the next transmit data is already written (TDRE flag = 0 in ICSR2) when NACK is received, the next data transmission on the falling edge of the 9th SCL clock cycle is automatically suspended. This prevents the SDAn line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is suspended by this function (NACKF = 1 in ICSR2), transmit and receive operations are discontinued. To restore transmit or receive operations, set the NACKF flag to 0. In master transmit mode, after issuing a restart or stop condition, set the NACKF flag to 0, then issue a start condition again.

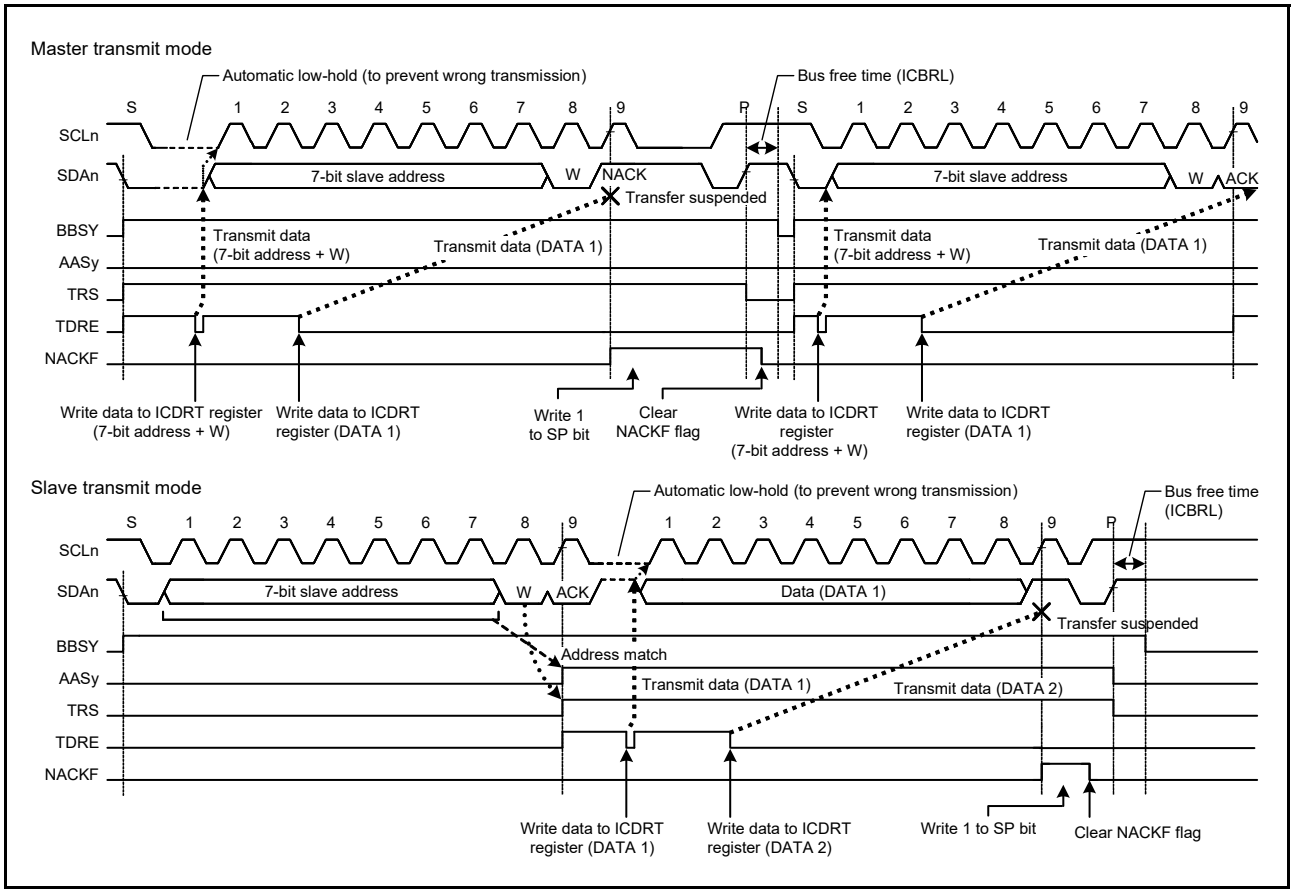


Figure 29.39 Suspension of data transfer when NACK is received (NACKE = 1)

29.9.3 Function to Prevent Failure to Receive Data

If response processing when receive data (ICDRR) read is delayed for a period of one transfer frame or more with receive data full (RDRF flag = 1 in ICSR2) in receive mode (TRS = 0 in ICCR2), the IIC holds the SCLn line low automatically immediately before the next data is received to prevent failure to receive data.

This function is also enabled even if the read processing of the final receive data is delayed and, in the meantime, the IIC slave address is designated after a stop condition is issued. This function does not interfere with other communication because the IIC does not hold the SCLn line low when a mismatch with its own slave address occurs after a stop condition is issued.

Periods in which the SCLn line is held low can be selected with a combination of the WAIT and RDRFS bits in ICMR3.

(1) 1-byte receive operation and automatic low-hold function using the WAIT bit

When the WAIT bit in ICMR3 is set to 1, the IIC performs a 1-byte receive operation using the WAIT bit function. Additionally, when the ICMR3.RDRFS bit is 0, the IIC automatically sends the ACKBT bit value in ICMR3 for the acknowledge bit in the period from the falling edge of the 8th SCL clock cycle to the falling edge of the 9th SCL clock cycle, and automatically holds the SCLn line low on the falling edge of the 9th SCL clock cycle using the WAIT bit function. This low-hold is released by reading data from ICDRR, which enables byte-wise receive operation.

The WAIT bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master receive mode or slave receive mode.

(2) 1-byte receive operation (ACK/NACK transmission control) and automatic low-hold function using the RDRFS bit

When the RDRFS bit in ICMR3 is set to 1, the IIC performs a 1-byte receive operation using the RDRFS bit function. When the RDRFS bit is set to 1, the RDRF (receive data full) flag in ICSR2 is set to 1 on the rising edge of the 8th SCL clock cycle, and the SCLn line is automatically held low on the falling edge of the 8th SCL clock cycle. This low-hold is released by writing a value to the ACKBT bit in ICMR3, but cannot be released by reading data from ICDRR, which enables receive operation through the ACK or NACK transmission control based on the data received in byte units.

The RDRFS bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master receive mode or slave receive mode.

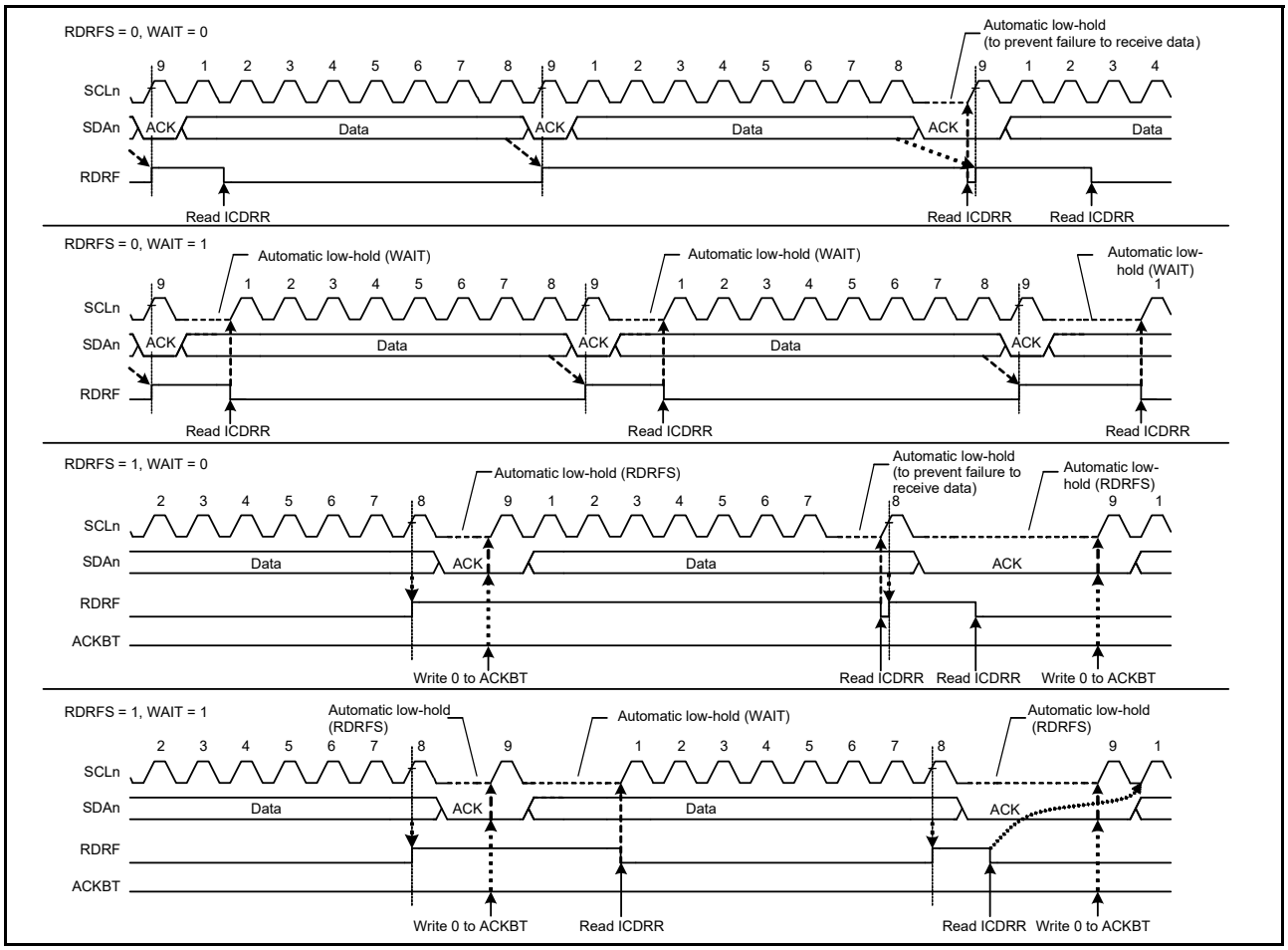


Figure 29.40 Automatic low-hold operation in receive mode using the RDRFS and WAIT bits

29.10 Arbitration-Lost Detection Functions

In addition to the normal arbitration-lost detection function defined by the I2C bus standard, the IIC provides functions to prevent double-issue of a start condition, detect arbitration-lost during the transmission of NACK, and detect arbitration-lost in slave transmit mode.

29.10.1 Master Arbitration-Lost Detection (MALE Bit)

The IIC drives the SDAn line low to issue a start condition. However, if the SDAn line was already driven low by another master device issuing a start condition, the IIC regards its own start condition as an error and considers this a loss in arbitration. Priority is given to transfer by the other master device. Similarly, if a request to issue a start condition is made by setting the ST bit in ICCR2 to 1 while the bus is busy (BBSY = 1 in ICCR2), the IIC regards this as a double-issuing-of-start-condition error and considers itself to have lost the arbitration. This prevents a failure of transfer resulting from a start condition issued while transfer is in progress.

When a start condition is issued successfully, if the transmit data including the address bits (internal SDA output level)

and the level on the SDAn line do not match (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state) and a low level is detected on the SDAn line, IIC loses the arbitration.

After a loss in arbitration of mastership, the IIC immediately enters slave receive mode. If a slave address, including the general call address, matches its own address at this time, the IIC continues in slave operation.

A loss in arbitration of mastership is detected when the following conditions are met while the MALE bit in ICFER is 1 (master arbitration-lost detection enabled).

[Master arbitration-lost conditions]

- Mismatching of the internal level for output on SDA and the level on the SDAn line after a start condition was issued by setting the ICCR2.ST bit to 1 while the BBSY flag in ICCR2 is set to 0 (erroneous issuing of a start condition)
- Setting of the ICCR2.ST bit to 1 (start condition double-issue error) while the BBSY flag is 1
- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDAn line in master transmit mode (MST and TRS bits = 11b in ICCR2).

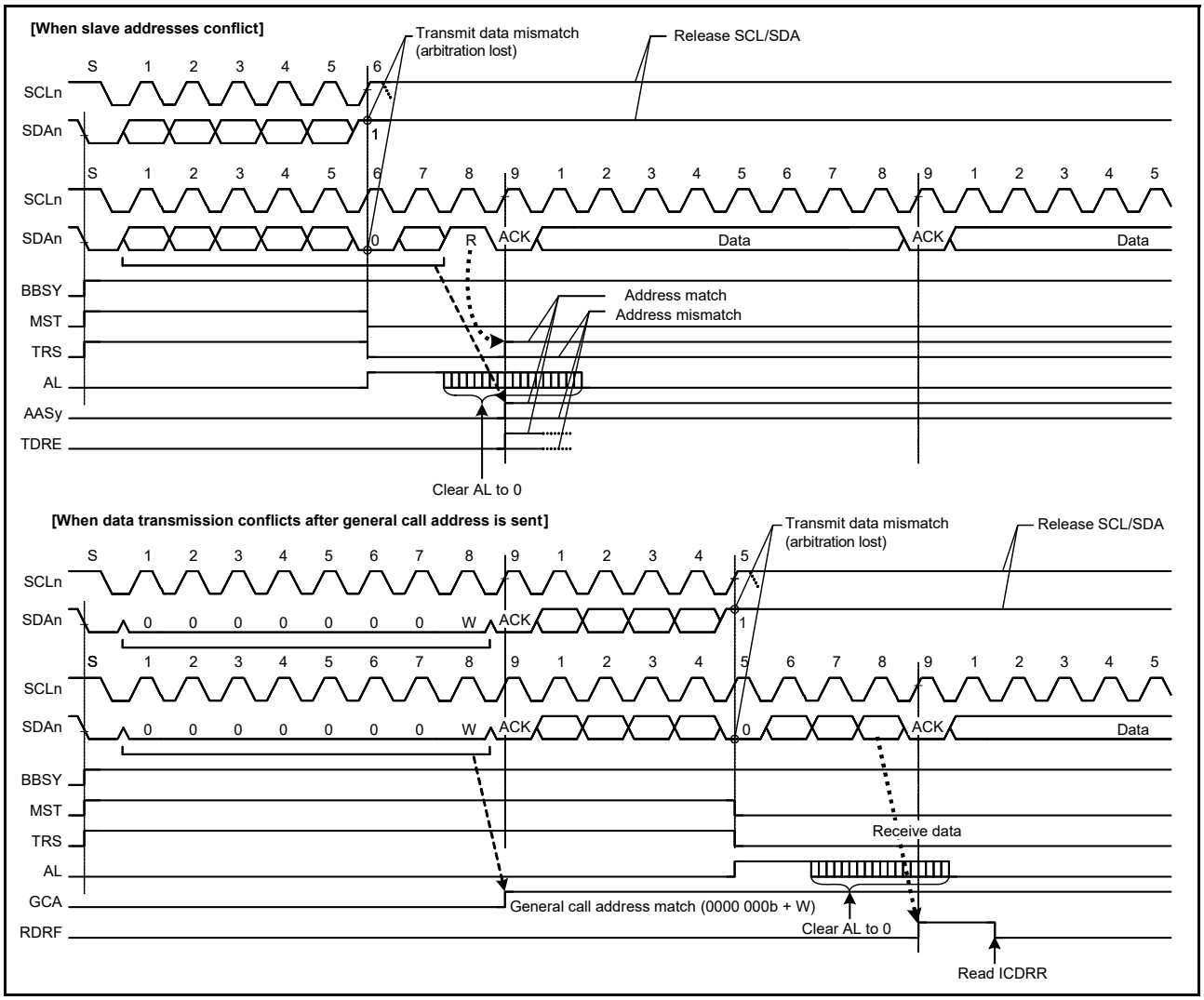


Figure 29.41 Examples of master arbitration-lost detection (MALE = 1)

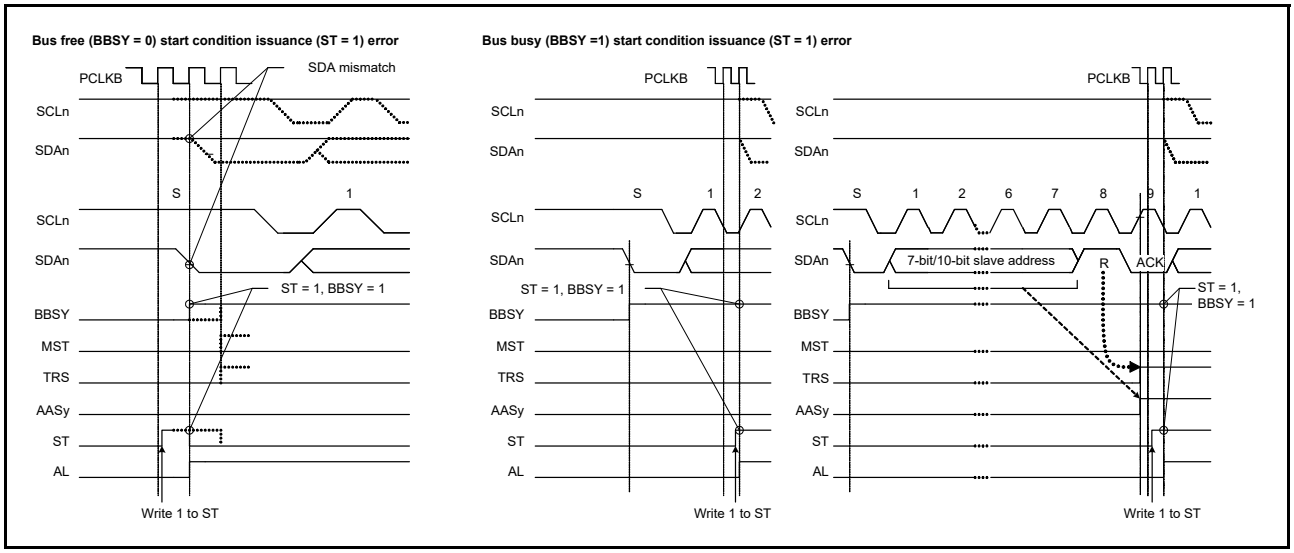


Figure 29.42 Arbitration-lost when start condition is issued (MALE = 1)

29.10.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit)

This function causes arbitration to be lost if the internal SDA output level does not match the level on the SDAn line during transmission of NACK in receive mode. Arbitration is lost because of a conflict between NACK and ACK transmissions when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such conflict occurs when multiple master devices send or receive the same information through a single slave device. Figure 29.43 shows an example of arbitration-lost detection during the transmission of NACK.

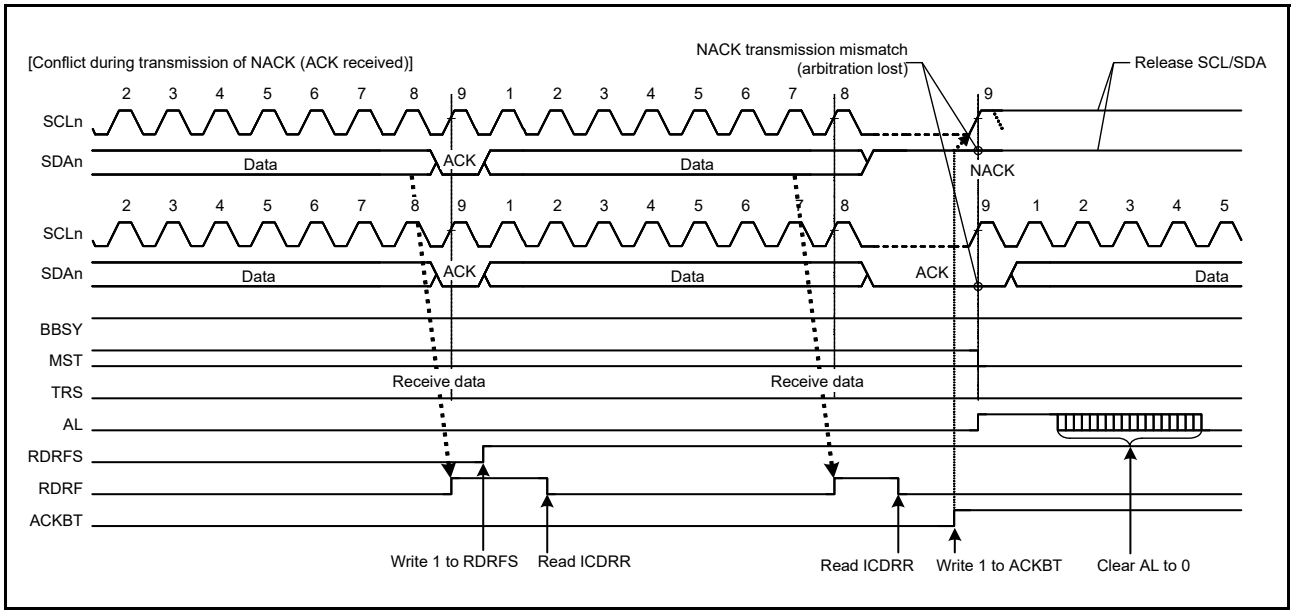


Figure 29.43 Example of arbitration-lost detection during transmission of NACK (NALE = 1)

The following description explains arbitration-lost detection using an example in which two master devices (master A and master B) and a single slave device are connected through the bus. In this example, master A receives 2 bytes of data from the slave device, and master B receives 4 bytes of data from the slave device.

If master A and master B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in either master A or B during access to the slave device. Therefore, both master A and master B recognize that they have obtained the bus mastership and operate as such. Master A sends NACK when it has received the 2 final bytes of data from the slave device. Meanwhile, master B sends ACK because it has not received the required 4 bytes of data.

The NACK transmission from master A and the ACK transmission from master B conflict. In general, if a conflict like

this occurs, master A cannot detect the ACK transmitted by master B and issues a stop condition. The stop condition issue conflicts with the SCL clock output of master B, which disrupts communication.

When the IIC receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost. If arbitration is lost during transmission of NACK, the IIC immediately cancels the slave match condition and enters slave receive mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

Similarly, in the ARP command processing of SMBus, the function to detect loss of arbitration during transmission of NACK is also available for eliminating the extra clock cycle processing, such as FFh transmission processing, which is required if the UDID (Unique Device Identifier) of the assigned address does not match in the Get UDID general processing after the Assign Address command.

The IIC detects arbitration-lost during transmission of NACK when the following condition is met with the NALE bit in ICFER set to 1 (arbitration-lost detection during NACK transmission enabled).

[Condition for arbitration-lost during NACK transmission]

- When the internal SDA output level does not match the SDAn line (ACK is received) during transmission of NACK (ACKBT bit = 1 in ICMR3).

29.10.3 Slave Arbitration-Lost Detection (SALE Bit)

This function causes arbitration to be lost if the transmit data (internal SDA output level) and the level on the SDAn line do not match in slave transmit mode. This arbitration-lost detection function is mainly used when transmitting a UDID (Unique Device Identifier) over an SMBus.

When the IIC loses slave arbitration, the IIC is immediately released from the slave-matched state and enters slave receive mode. This function can detect conflicts of data during transmission of UDIDs over an SMBus and eliminates subsequent redundant processing for the transmission of FFh.

The IIC detects slave arbitration-lost when the following condition is met with the SALE bit in ICFER set to 1 (slave arbitration-lost detection enabled).

[Condition for slave arbitration-lost]

- When transmit data excluding acknowledge (internal SDA output level) does not match the SDAn line in slave transmit mode (MST and TRS bits = 01b in ICCR2).

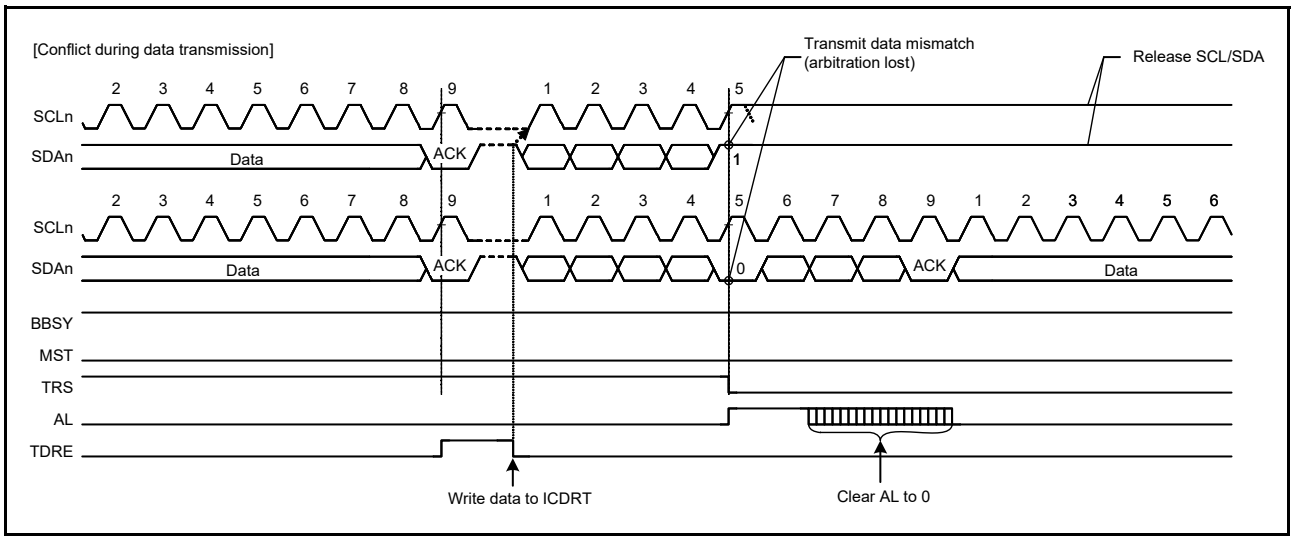


Figure 29.44 Example of slave arbitration-lost detection (SALE = 1)

29.11 Start, Restart, and Stop Condition Issuing Function

29.11.1 Issuing a Start Condition

The IIC issues a start condition when the ST bit in ICCR2 is set to 1.

When the ST bit is set to 1, a start condition request is made, and the IIC issues a start condition when the BBSY flag in ICCR2 is 0 (bus free state). When a start condition is issued normally, the IIC automatically shifts to the master transmit mode.

To issue a start condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure that the time set in ICBRH and the start condition hold time elapse.
3. Drive the SCLn line low (high level to low level).
4. Detect low level on the SCLn line and ensure the low-level period of the SCLn line set in ICBRL elapses.

29.11.2 Issuing a Restart Condition

The IIC issues a restart condition when the RS bit in ICCR2 is set to 1.

When the RS bit is set to 1, a restart condition request is made. The IIC issues a restart condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a restart condition:

1. Release the SDAn line.
2. Ensure the low-level period of the SCLn line set in ICBRL elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level on the SCLn line and ensure the time set in ICBRL and the restart condition setup time elapse.
5. Drive the SDAn line low (high level to low level).
6. Ensure the time set in ICBRH and the restart condition hold time elapse.
7. Drive the SCLn line low (high level to low level).
8. Detect a low level on the SCLn line and ensure the low-level period of the SCLn line set in ICBRL elapses.

Note: When issuing restart condition requests, write the slave address to ICDRT after confirming that ICCR2.RS = 0. Data written while ICCR2.RS = 1 is not forwarded because of the retransmission condition before the occurrence.

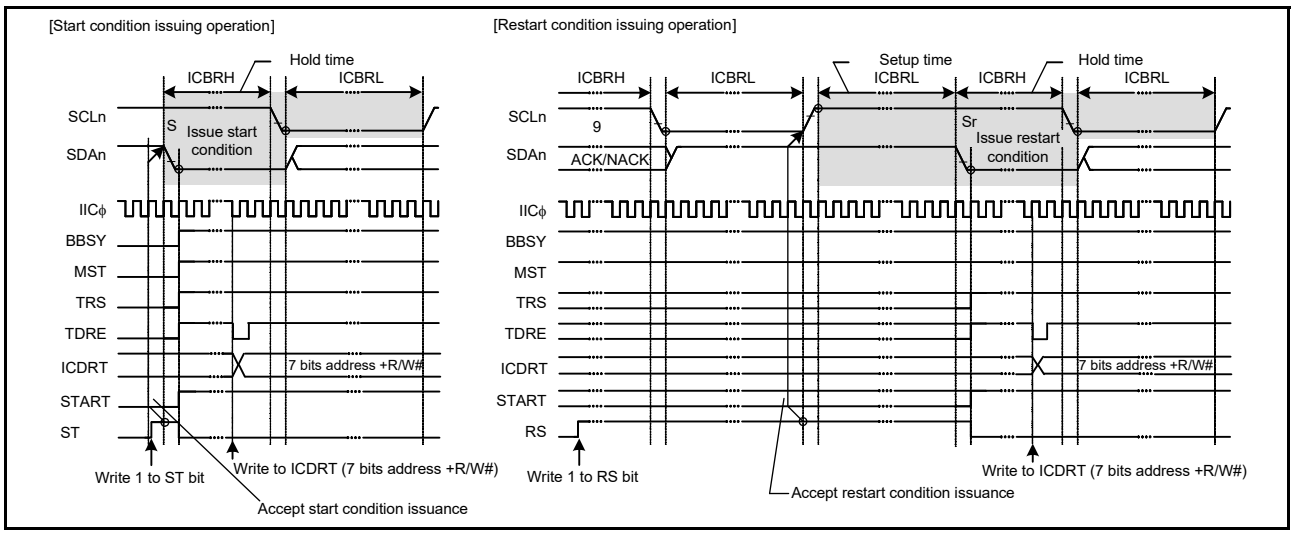


Figure 29.45 Start and restart condition issue timing using the ST and RS bits

Figure 29.46 shows the operation timing when a restart condition is issued after the master transmission.

To issue a restart condition after the master transmission:

1. Initialize the IIC using the procedure in section 29.3.2, Initial Settings.
2. Read the BBSY flag in IICR2 to check that the bus is open, and then set the ICCR2.ST bit to 1 (start condition request). On receiving the request, the IIC issues a start condition. At the same time, the BBSY and the START flags in ICSR2 are automatically set to 1 and the ST bit automatically sets to 0. If the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that a start condition is successfully issued as requested by the ST bit. The MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 when the TRS bit is set to 1.
3. Check that the TDRE flag in ICSR2 is 1, then write the value for transmission (the slave address and the R/W# bit) to the ICDRT register. After the transmit data is written to ICDRT, the TDRE flag is automatically set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag again sets to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRS bit is automatically updated to select master transmit or master receive mode according to the value of the transmitted R/W# bit. If the value of the R/W# bit is 0, the IIC continues in master transmit mode. If the ICSR2.NACKF flag is 1 at this time, indicating that no slave device recognized the address or there was an error in communications, write 1 to ICCR2.SP bit to issue a stop condition.

   To transmit data with an address in the 10-bit format, start by writing 1111 0b, the 2 upper bits of the slave address, and W to ICDRT as the first address transmission. Then, as the second address transmission, write the 8 lower bits of the slave address to the ICDRT register.
4. After confirming that the TDRE flag in ICSR2 is 1, write the data for transmission to the ICDRT register. The IIC automatically holds the SCLn line low until data for transmission is ready, and a restart or stop condition is issued.
5. After all bytes of data for transmission are written to the ICDRT register, wait until the value of the TEND flag in ICSR2 returns to 1. Then, after checking that the START flag in ICSR2 is 1, set the START flag in ICSR2 to 0.
6. Set the RS bit in ICCR2 to 1 (restart condition request). On receiving the request, the IIC issues a restart condition.
7. After checking that the START flag in ICSR2 is 1, write the value for transmission (the slave address and the R/W# bit) to the ICDRT register.

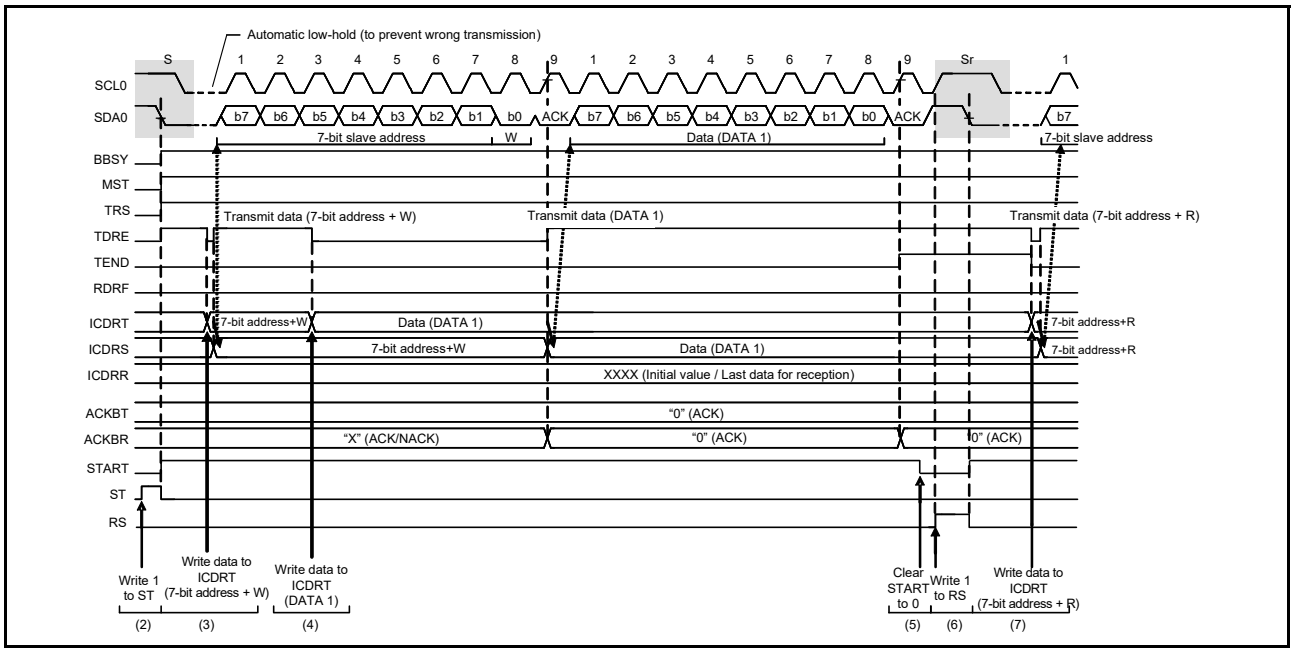


Figure 29.46 Restart condition issue timing after master transmission.

29.11.3 Issuing a Stop Condition

The IIC issues a stop condition when the SP bit in ICCR2 is set to 1.

When the SP bit is set to 1, a stop condition request is made. The IIC issues a stop condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a stop condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure that the low-level period of the SCLn line set in ICBRL elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level on the SCLn line and ensure that the time set in ICBRH and the stop condition setup time elapse.
5. Release the SDAn line (low level to high level).
6. Ensure the time set in ICBRL and the bus free time elapse.
7. Clear the BBSY flag to 0 to release the bus mastership.

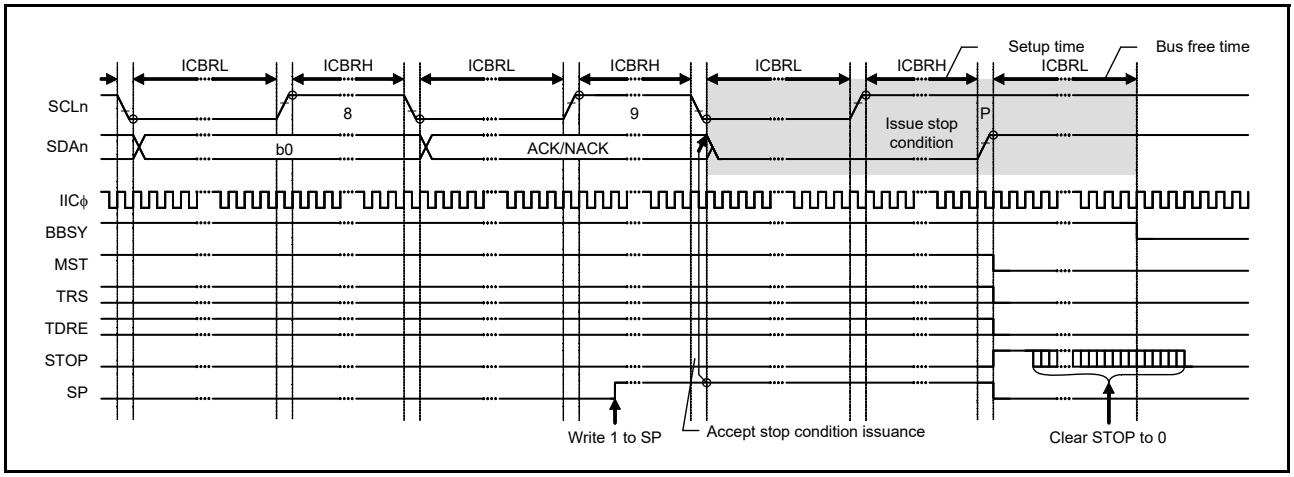


Figure 29.47 Stop condition issue timing using the SP bit

29.12 Bus Hanging

If the clock signals from the master and slave devices are out of synchronization because of noise or other factors, the I2C bus might hang with a fixed level on the SCLn line or SDAn line.

To manage bus hanging, the IIC has:

- A timeout function to detect hanging by monitoring the SCLn line
- A function for the output of an extra SCL clock cycle to release the bus from a hung state because of clock signals being out of synchronization
- An IIC reset function
- An internal reset function.

By checking the SCLO, SDAO, SCLI, and SDAI bits in ICCR1, it is possible to see whether the IIC or its communicating partner is placing the low level on the SCLn or SDAn lines.

29.12.1 Timeout Function

The timeout function can detect when the SCLn line is stuck longer than the predetermined time. The IIC can detect an abnormal bus state by monitoring that the SCLn line is stuck low or high for a predetermined time.

The timeout function monitors the SCLn line state and counts the low-level or high-level period using the internal counter. The timeout function resets the internal counter each time the SCLn line changes (rising or falling), but continues to count unless the SCLn line changes. If the internal counter overflows because no SCLn line changes, the IIC

can detect the timeout and report the bus hung state.

This timeout function is enabled when the ICFER.TMOE bit is 1. It detects a hung state when the SCLn line is stuck low or high during the following conditions:

- The bus is busy (ICCR2.BBSY flag is 1) in master mode (ICCR2.MST bit is 1)
- The IIC slave address is detected (ICSR1 register is not 00h) and the bus is busy (ICCR2.BBSY flag is 1) in slave mode (ICCR2.MST bit is 0)
- The bus is open (ICCR2.BBSY flag is 0) while a start condition is requested (ICCR2.ST bit is 1).

The internal counter of the timeout function uses the internal reference clock (IICϕ) set in the CKS[2:0] bits in ICMR1 as a count source. It functions as a 16-bit counter when long mode is selected (TMOS bit = 0 in ICMR2) or a 14-bit counter when short mode is selected (TMOS bit = 1).

The SCLn line level (low, high, or both levels) during which this counter is activated can be selected in the TMOH and TMOL bits in ICMR2. If both TMOL and TMOH bits are set to 0, the internal counter is disabled.

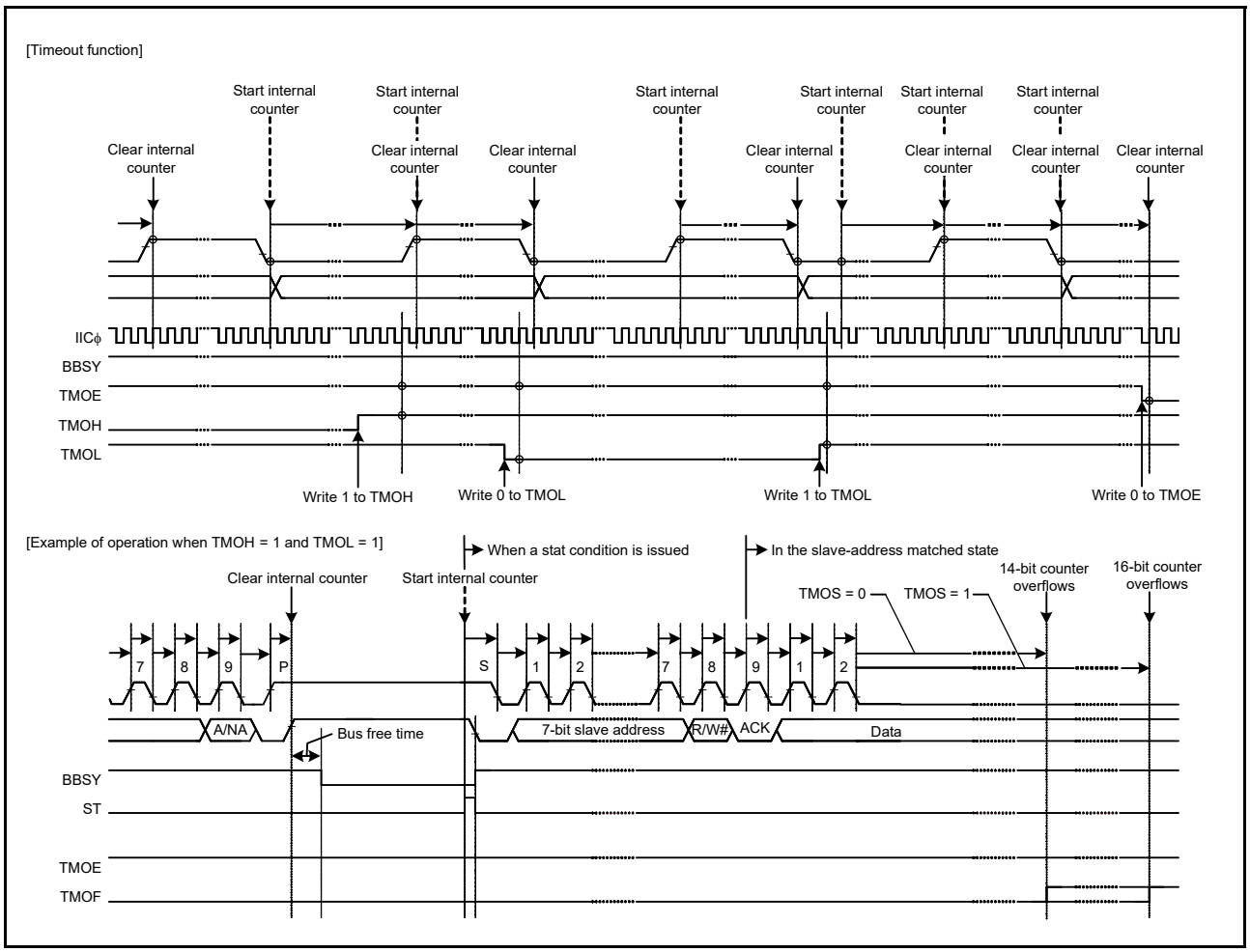


Figure 29.48 Timeout function using the TMOE, TMOS, TMOH, and TMOL bits

29.12.2 Extra SCL Clock Cycle Output Function

In master mode, this function outputs extra SCL clock cycles to release the SDAn line of the slave device from being held low because the master is out of synchronization with the slave device.

This function is mainly used in master mode to release the SDAn line of the slave device from being fixed low by including extra cycles of SCL output from the IIC. It uses single cycles of the SCL clock for a bus error where the IIC cannot issue a stop condition because the slave device is holding the SDAn line at the low level. Do not use this function in normal situations. Using it when communications are proceeding correctly leads to malfunctioning.

When the CLO bit in ICCR1 is set to 1 in master mode, a single cycle of the SCL clock at the transfer rate specified in the CKS[2:0] bits in ICMR1, the ICBRH, and ICBRL registers, is output as an extra clock cycle. After output of this single cycle of the SCL clock, the CLO bit is automatically set to 0. Therefore, more extra clock cycles can be output consecutively by writing 1 to the CLO bit after having read CLO = 0.

When the IIC module is in master mode and the slave device is holding the SDAn line low because synchronization with the slave device is lost due to the effects of noise, the output of a stop condition is not possible. This function can be used to output extra cycles of SCL one by one to make the slave device release the SDAn line from being held low, and recover the bus from an unusable state. Release of the SDAn line by the slave device can be monitored by reading the SDAI bit in ICCR1. After confirming the release of the SDAn line by the slave device, complete the communication by reissuing the stop condition.

Use this function with the MALE bit in ICFER set to 0 (master arbitration-lost detection disabled). If the MALE bit is set to 1 (enabled), arbitration is lost when the value of the SDAO bit in ICCR1 does not match the state of the SDAn line.

[Output conditions for using the CLO bit in ICCR1]

- When the bus is free (BBSY flag in ICCR2 = 0) or in master mode (MST bit = 1 and BBSY flag = 1 in ICCR2)
- When the communication device does not hold the SCLn line low.

Figure 29.49 shows the operation timing of the extra SCL clock cycle output function (CLO bit).

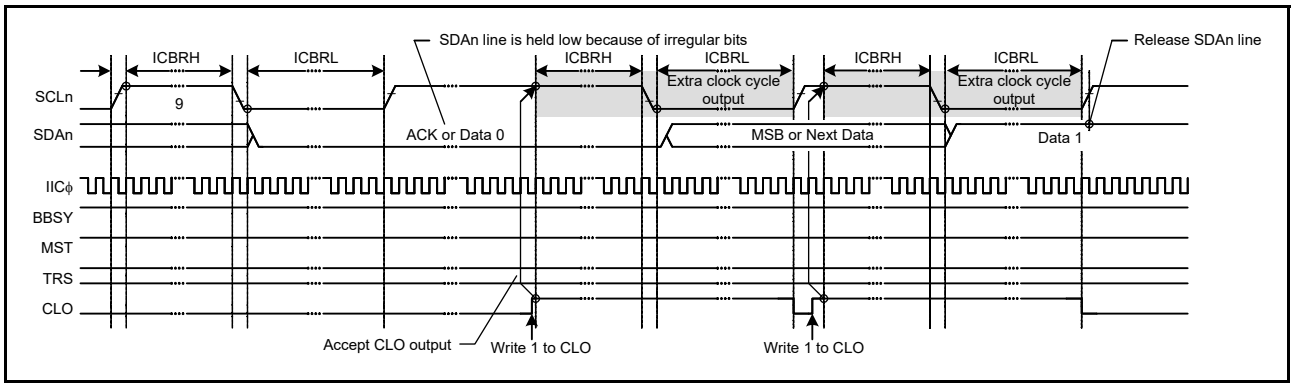


Figure 29.49 Extra SCL clock cycle output function using the CLO bit

29.12.3 IIC Reset and Internal Reset

The IIC module has two types of resets:

- IIC reset, which initializes all registers, including the BBSY flag in ICCR2
- Internal reset, which releases the IIC from the slave-address matched state and initializes the internal counter while saving other settings.

After issuing a reset, be sure to set the IICRST bit in ICCR1 to 0. Both types of resets are valid for release from bus-hung states, because both restore the output state of the SCLn and SDAn pins to the high-impedance state.

Issuing a reset during slave operation might lead to a loss of synchronization between the master device clock and the slave device clock, so avoid this when possible. In addition, monitoring of the bus state, such as for the presence of a start condition, is not possible during an IIC reset (ICE and IICRST bits = 01b in ICCR1).

For a detailed description of the IIC and internal resets, see section 29.15, State of Registers when Issuing each Condition.

29.13 SMBus Operation

The IIC supports data communication conforming to the SMBus Specification, version 2.0. To perform SMBus communication, set the SMBS bit in ICMR3 to 1. To use the transfer rate within a range of 10 kbps to 100 kbps of the SMBus standard, set the CKS[2:0] bits in ICMR1, the ICBRH, and ICBRL registers. In addition, specify the values in the DLCS bit in ICMR2 and the SDDL[2:0] bits in ICMR2 to meet the data hold time specification of 300 ns or more. When the IIC is used only as a slave device, the transfer rate setting is not required, but ICBRL must be set to a value longer than the data setup time (250 ns).

For the SMBus device default address (1100 001b), use one of the slave address registers L0 to L2 (SARL0, SARL1, and SARL2), and set the associated FS bit (7- or 10-bit address format select) in SARUy (y = 0 to 2) to 0 (7-bit address format).

When transmitting the UDID (Unique Device Identifier), set the SALE bit in ICFER to 1 to enable the slave arbitration-lost detection function.

29.13.1 SMBus Timeout Measurement

(1) Measuring slave device timeout

The following period (timeout interval: $T_{LOW:\ SEXT}$) must be measured for slave devices in SMBus communication:

- From start condition to stop condition.

To measure timeout for slave devices, measure the period from start condition detection to stop condition detection with the GPT using the IIC start condition detection interrupt (STIn) and stop condition detection interrupt (SPIn). The measured timeout period must be within the total clock low-level period [slave device] $T_{LOW:\ SEXT}$: 25 ms (maximum) of the SMBus standard.

If the time measured with the GPT exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the slave device must release the bus by writing 1 to the IICRST bit in ICCR1 to issue an internal reset of the IIC. When an internal reset is issued, the IIC stops driving the bus for the SCLn and SDAn pins and makes the SCLn/SDAn pin output high-impedance, which releases the bus.

(2) Measuring master device timeout

The following periods (timeout interval: $T_{LOW:\ MEXT}$) must be measured for master devices in SMBus communication:

- From start condition to acknowledge bit
- Between acknowledge bits
- From acknowledge bit to stop condition.

To measure timeout for master devices, measure these periods with the GPT using the IIC start condition detection interrupt (STIn), stop condition detection interrupt (SPIn), transmit end interrupt (IICn_TEI), or receive data full interrupt (IICn_RXI). The measured timeout period must be within the total clock low-level extended period (master device) $T_{LOW:\ MEXT}$: 10 ms (maximum) of the SMBus standard, and the total of all $T_{LOW:\ MEXT}$ values from the start condition to stop condition must be within $T_{LOW:\ SEXT}$: 25 ms (maximum).

For the ACK receive timing (rising edge of the 9th SCL clock cycle), monitor the TEND flag in ICSR2 in master transmit mode (master transmitter) and the RDRF flag in ICSR2 in master receive mode (master receiver). Perform byte-wise transmit operations in master transmit mode, and hold the RDRFS bit in ICMR3 at 0 until the byte immediately before the reception of the final byte in master receive mode. While the RDRFS bit is 0, the RDRF flag is set to 1 on the rising edge of the 9th SCL clock cycle.

If the period measured with GPT exceeds the total clock low-level extended period (master device), $T_{LOW:\ MEXT}$: 10 ms (maximum) of the SMBus standard or the total of measured periods exceeds the clock low-level detection timeout, $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the master device must stop the transaction by issuing a stop condition. In master transmit mode, immediately stop the transmit operation (stop writing data to ICDRT).

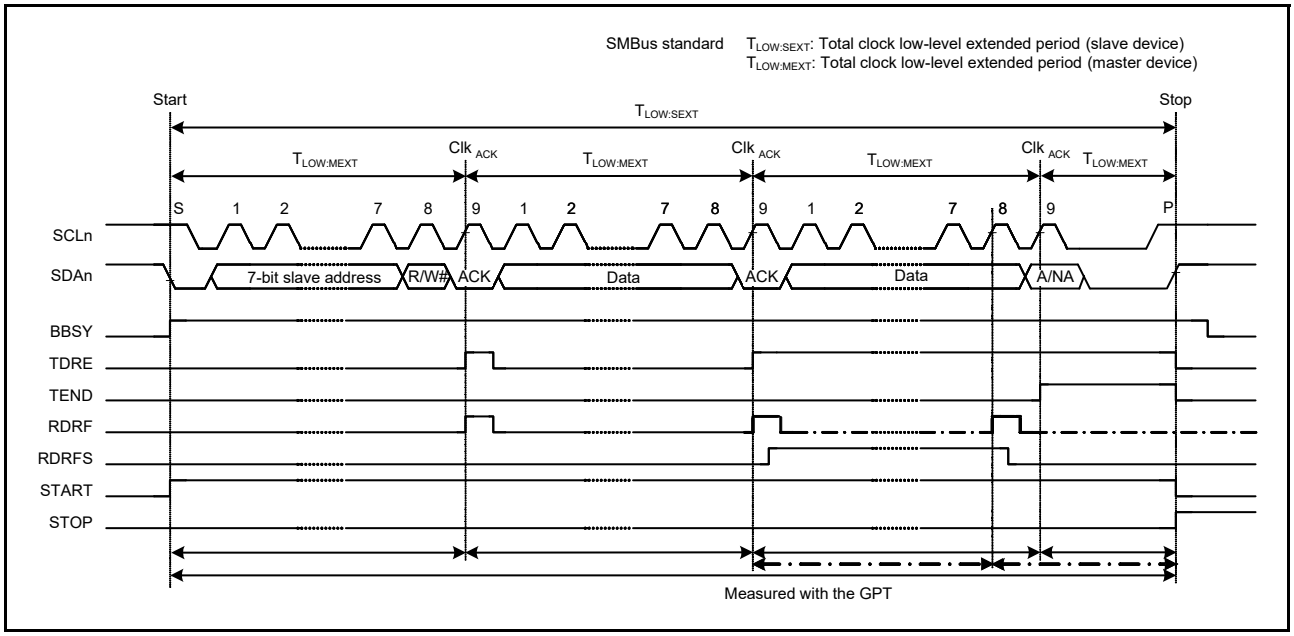


Figure 29.50 SMBus timeout measurement

29.13.2 Packet Error Code (PEC)

The MCU provides a CRC calculator that enables transmission of a Packet Error Code (PEC) or allows checking the received data in SMBus data communication. For the CRC-generating polynomials of the CRC calculator, see section 32, Cyclic Redundancy Check (CRC) Calculator.

In master transmit mode, the PEC data can be generated by writing all transmit data to the CRC Data Input Register (CRCDIR) in the CRC calculator.

In master receive mode, the PEC data can be checked by writing all receive data to CRCDIR in the CRC calculator and comparing the obtained value in the CRC Data Output Register (CRCDOR) with the received PEC data.

To send ACK or NACK based on the match or mismatch result when the final byte is received as a result of the PEC code check, set the RDRFS bit in ICMR3 to 1 before the rising edge of the 8th SCL clock cycle during reception of the final byte, and hold the SCLn line low on the falling edge of the 8th clock cycle.

29.13.3 SMBus Host Notification Protocol (Notify ARP Master Command)

In communications over an SMBus, a slave device can temporarily act as a master device to notify the SMBus host (or ARP master) of its own slave address, or to request its own slave address from the SMBus host.

For a product using the MCU to operate as an SMBus host or ARP master, the host address (0001 000b) sent from the slave device must be detected as a slave address, and so the IIC has a function for detecting the host address. To detect the host address as a slave address, set the SMBS bit in ICMR3 and the HOAE bit in ICSER to 1. Operation after the host address is detected is the same as normal slave operation.

29.14 Interrupt Sources

The IIC issues four types of interrupt requests:

- Transfer error or event generation (arbitration-lost, NACK detection, timeout detection, start or restart condition detection, and stop condition detection)
- Receive data full
- Transmit data empty
- Transmit end.

Table 29.10 lists details of the interrupt requests. The receive data full and transmit data empty interrupts can activate data transfer by the DTC or DMAC.

Table 29.10 Interrupt sources

Symbol	Interrupt source	Interrupt flag	DMAC/DTC activation	Interrupt condition
IICn_EEI*5	Transfer error or event generation	AL	Not possible	AL = 1, ALIE = 1
		NACKF		NACKF = 1, NAKIE = 1
		TMOF		TMOF = 1, TMOIE = 1
		START		START = 1, STIE = 1
		STOP		STOP = 1, SPIE = 1
IICn_RXI*2, *5	Receive data full	RDRF	Possible	RDRF = 1, RIE = 1
IICn_TXI*1, *5	Transmit data empty	TDRE	Possible	TDRE = 1, TIE = 1
IICn_TEI*3, *5	Transmit end	TEND	Not possible	TEND = 1, TEIE = 1
IIC0_WUI*4	Slave address match during wakeup function	WUF	Not possible	Slave address match Slave receive complete RWAK operation ASY0 = 1 WUIE = 1

Note: There is a delay between the execution of a write instruction for a peripheral module by the CPU and actual writing to the module. When an interrupt flag is cleared or masked, read the relevant flag again to check whether clearing or masking is complete, and then return from interrupt handling. Not doing so creates the possibility of repeated processing of the same interrupt.

Note 1. Because IICn_TXI is an edge-detected interrupt, it does not require clearing. Additionally, the TDRE flag in ICSR2 (condition for IICn_TXI) is automatically set to 0 when transmit data is written to ICDRT or a stop condition is detected (STOP flag = 1 in ICSR2).

Note 2. Because IICn_RXI is an edge-detected interrupt, it does not require clearing. Additionally, the RDRF flag in ICSR2 (condition for IICn_RXI) automatically is set to 0 when data is read from ICDRR.

Note 3. When using the IICn_TEI interrupt, clear the TEND flag in ICSR2 in the IICn_TEI interrupt handling. The TEND flag in ICSR2 automatically is set to 0 when transmit data is written to ICDRT or a stop condition is detected (STOP flag = 1 in ICSR2).

Note 4. Only channel 0 has a wakeup function, therefore IIC0_WUI is for channel 0 only.

Note 5. Channel number (n = 0, 1).

Clear or mask each flag during interrupt handling.

29.14.1 Buffer Operation for IICn_TXI and IICn_RXI Interrupts

If the conditions for generating an IICn_TXI or IICn_RXI interrupt are satisfied while the associated IR flag is 1, the interrupt request is not output for the ICU but is saved internally. One request per source can be saved internally.

An interrupt request that is saved within the ICU is output when the ICU.IELSRn.IR flag becomes 0. Internally saved interrupt requests are automatically cleared under normal conditions. They can also be cleared by writing 0 to the interrupt enable bit within the associated peripheral module.

29.15 State of Registers when Issuing each Condition

The IIC has two dedicated resets, IIC reset and internal reset. Table 29.11 lists the registers states when issuing each condition.

Table 29.11 Register states when issuing each condition (1 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICCR1	ICE, IICRST	Reset	Saved	Saved	Saved	Saved
	SCLO, SDAO		Reset	Reset		
	Others			Saved		
ICCR2	BBSY	Reset	Reset	Saved	Set	Saved
	ST			Reset	Saved	Saved
	TRS,MST				Set or saved	Reset
	Others				Reset	Reset or saved

Table 29.11 Register states when issuing each condition (2 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICMR1	BC[2:0]	Reset	Reset	Reset	Reset	Saved
	Others			Saved	Saved	
ICMR2		Reset	Reset	Saved	Saved	Saved
ICMR3		Reset	Reset	Saved	Saved	Saved
ICFER		Reset	Reset	Saved	Saved	Saved
ICSER		Reset	Reset	Saved	Saved	Saved
ICIER		Reset	Reset	Saved	Saved	Saved
ICSR1		Reset	Reset	Reset	Saved	Reset
ICSR2	TDRE, TEND	Reset	Reset	Reset	Saved	Reset
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		Reset	Reset	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		Reset	Reset	Saved	Saved	Saved
ICBRH, ICBRL		Reset	Reset	Saved	Saved	Saved
ICDRT		Reset	Reset	Saved	Saved	Saved
ICDRR		Reset	Reset	Saved	Saved	Saved
ICDRS		Reset	Reset	Reset	Saved	Saved
Timeout function		Reset	Reset	Operating	Operating	Operating
Bus free time measurement		Reset	Reset	Operating	Operating	Operating
ICWUR2	WUSEN	Reset	Reset	Saved	Saved	Saved
	Others					Saved, set, or reset

29.16 Event Link Output

IIC0 and IIC1 modules handle the event output for the Event Link Controller (ELC) for the following sources:

(1) Transfer error event

When a transfer error event occurs, the associated event signal can be output to another module by the ELC.

(2) Receive data full

When a receive data register becomes full, the associated event signal can be output to another module by the ELC.

(3) Transmit data empty

When a transmit data register becomes empty, the associated event signal can be output to another module by the ELC.

(4) Transmit end

On completion of the transfer, the associated event signal can be output to another module by the ELC.

29.16.1 Interrupt Handling and Event Linking

Each of the IIC interrupt types (see Table 29.10) has an enable bit to control enabling and disabling of the associated interrupt signal. An interrupt request signal is output to the CPU when an interrupt source condition is satisfied while the associated enable bit is set.

The associated event link output signals are sent to other modules as event signals by the ELC when the interrupt source conditions are satisfied, regardless of the interrupt enable bit settings. For details on interrupt sources, see Table 29.10.

29.17 Usage Notes

29.17.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable IIC operation. The IIC module is initially stopped after a reset. Releasing the module-stop state enables access to the registers.

For details on Module Stop Control Register B, see section 11, Low Power Modes.

29.17.2 Notes on Starting Transfer

If the IR flag associated with the IIC interrupt is 1 when the transfer is started (ICCR1.ICE bit = 1), follow the procedure in this section to clear the interrupts before enabling operations. Starting transfer with the IR flag set to 1 while the ICCR1.ICE bit is 1 leads to an interrupt request being internally saved after transfer starts, and this can lead to unexpected behavior of the IR flag.

To clear interrupts before starting transfer operation:

1. Confirm that the ICCR1.ICE bit is 0.
2. Set the relevant interrupt enable bits, such as ICIER.TIE to 0.
3. Read the relevant interrupt enable bits, such as ICIER.TIE, and confirm that the value is 0.
4. Set the IR flag to 0.

30. Controller Area Network (CAN) Module

30.1 Overview

The CAN module uses a message-based protocol to receive and transmit data between multiple slaves and masters in electromagnetically noisy applications. The module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. The CAN module requires an additional external CAN transceiver.

Table 30.1 lists the CAN specifications, and Figure 30.1 shows a block diagram.

Table 30.1 CAN specifications (1 of 2)

Parameter	Specifications
Data transfer rate	ISO11898-1-compliant for standard and extended frames
Bit rate	Programmable up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes, with two selectable mailbox modes • Normal mode: 32 mailboxes independently configurable for transmission or reception • FIFO mode: 24 mailboxes independently configurable for either transmission or reception, with remaining mailboxes used for receive (RX) and transmit (TX) 4-stage FIFOs.
Reception	• Support for data frame and remote frame reception • Reception ID format selectable to only standard ID, only extended ID, or mixed IDs • Programmable one-shot reception function • Selectable between overwrite mode (unread message overwritten) and overrun mode (unread message saved) • Reception complete interrupt independently enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one for every four mailboxes) • Masks independently enabled or disabled for each mailbox.
Transmission	• Support for data frame and remote frame transmission • Transmission ID format selectable to only standard ID, only extended ID, or mixed IDs • Programmable one-shot transmission function • Broadcast messaging function • Priority mode selectable based on message ID or mailbox number • Support for transmission request abort, with abort completion confirmable in status flag • Transmission complete interrupt independently enabled or disabled for each mailbox.
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state selectable to: • ISO11898-1 specification-compliant • Automatic invoking of CAN halt mode on bus-off entry • Automatic invoking of CAN halt mode on bus-off end • Transition to CAN halt mode through software • Transition to error-active state through software.
Error status monitoring	• Monitoring of CAN bus errors, including stuff error, form error, ACK error, 15-bit CRC error, bit error, and ACK delimiter error • Detection of transition to error states, including error-warning, error-passive, bus-off entry, and bus-off recovery • Support for reading of error counters.
Time stamping	• Time stamp function using a 16-bit counter • Reference clock selectable to 1-bit, 2-bit, 4-bit, and 8-bit time periods.
Interrupt function	Support for five interrupt sources: • Reception complete • Transmission complete • Receive FIFO • Transmit FIFO • Error interrupts.
CAN sleep mode	CAN clock stopped to reduce power consumption

Table 30.1 CAN specifications (2 of 2)

Parameter	Specifications
Software support unit	Three software support units: • Acceptance filter support • Mailbox search support, including receive mailbox search, transmit mailbox search, and message lost search • Channel search support.
CAN clock source	PCLKB or CANMCLK
Test mode	Three test modes available for evaluation purposes: • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback).
Module-stop function	Module-stop state can be set to reduce power consumption

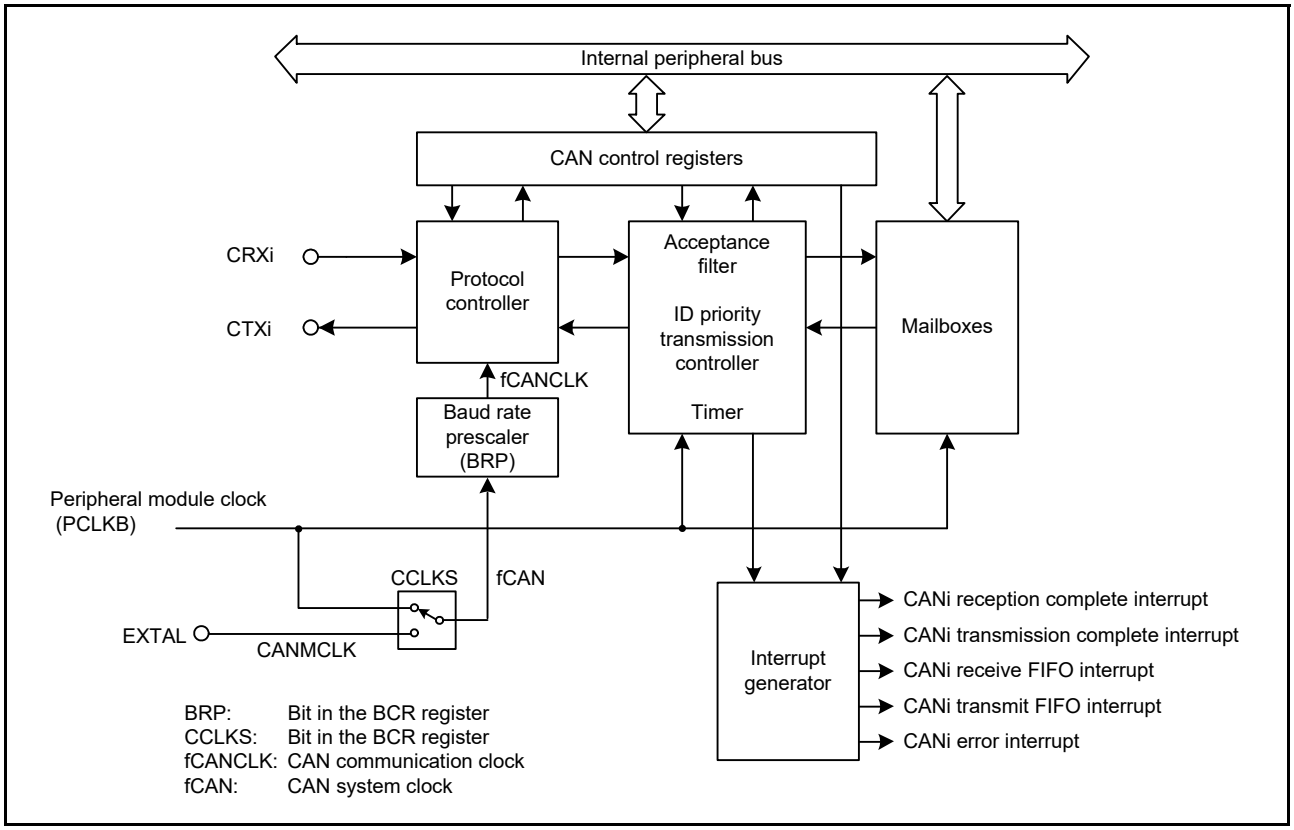


Figure 30.1 CAN module block diagram (i = 0)

The CAN module constitutes the following blocks:

- CAN input and output pins
  CRXi and CTXi, where i = 0
- Protocol controller
  Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, and error handling
- Mailboxes
  Consists of 32 mailboxes, which can be configured as either transmit or receive. Each mailbox has an individual ID, data length code (DLC), data field (8 bytes), and a time stamp.
- Acceptance filter
  Performs filtering of received messages using MKR0 to MKR7 registers for the filtering process
- Timer
  Used for the time stamp function. The timer value when a message is stored in the mailbox is written as the time stamp value.

- Interrupt generator for five types of interrupts:
  - CANi reception complete interrupt
  - CANi transmission complete interrupt
  - CANi receive FIFO interrupt
  - CANi transmit FIFO interrupt
  - CANi error interrupt.

Table 30.2 lists the CAN module pins. These pins are multiplexed with other signals on the MCU. For details, see section 19, I/O Ports.

Table 30.2 CAN module I/O pins

Pin name	I/O	Function
CRX0	Input	Data receive pin
CTX0	Output	Data transmit pin

30.2 Register Descriptions

30.2.1 Control Register (CTLR)

Address(es): CAN0.CTLR 4005 0840h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RBOC	BOM[1:0]		SLPM	CANM[1:0]		TSPS[1:0]		TSRC	TPM	MLM	IDFM[1:0]		MBM
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MBM	CAN Mailbox Mode Select*1	0: Normal mailbox mode 1: FIFO mailbox mode.	R/W
b2, b1	IDFM[1:0]	ID Format Mode Select *1	b2 b1 0 0: Standard ID mode All mailboxes, including FIFO mailboxes, handle only standard IDs 0 1: Extended ID mode All mailboxes, including FIFO mailboxes, handle only extended IDs 1 0: Mixed ID mode All mailboxes, including FIFO mailboxes, handle both standard and extended IDs. In normal mailbox mode, use the associated IDE bit to differentiate between standard and extended IDs. In FIFO mailbox mode, the associated IDE bits are used for mailboxes 0 to 23, the IDE bits in FIDCR0 and FIDCR1 are used for the receive FIFO, and the IDE bit associated with mailbox 24 is used for the transmit FIFO. 1 1: Setting prohibited.	R/W
b3	MLM	Message Lost Mode Select*1	0: Overwrite mode 1: Overrun mode.	R/W
b4	TPM	Transmission Priority Mode Select*1	0: ID priority transmit mode 1: Mailbox number priority transmit mode.	R/W
b5	TSRC	Time Stamp Counter Reset Command*4	0: Do not reset time stamp counter 1: Reset time stamp counter.*3	R/W
b7, b6	TSPS[1:0]	Time Stamp Prescaler Select*1	b7 b6 0 0: Every 1-bit time 0 1: Every 2-bit time 1 0: Every 4-bit time 1 1: Every 8-bit time.	R/W

Bit	Symbol	Bit name	Description	R/W
b9, b8	CANM[1:0]	CAN Operating Mode Select*5	b9 b8 0 0: CAN operation mode 0 1: CAN reset mode 1 0: CAN halt mode 1 1: CAN reset mode (forced transition).	R/W
b10	SLPM	CAN Sleep Mode*5,*6	0: Exit CAN sleep mode 1: Enter CAN sleep mode.	R/W
b12, b11	BOM[1:0]	Bus-Off Recovery Mode*1	b12 b11 0 0: Normal mode (ISO11898-1 specification compliant) 0 1: Enter CAN halt mode automatically on entering bus-off state 1 0: Enter CAN halt mode automatically at the end of bus-off state 1 1: Enter CAN halt mode during bus-off recovery period through a software request.	R/W
b13	RBOC	Forcible Return from Bus-Off*2	0: No return occurred 1: Forced return from bus-off state.*3	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Write to the BOM[1:0], TSPS[1:0], TPM, MLM, IDFM[1:0], and MBM bits in CAN reset mode.
Note 2. Set the RBOC bit to 1 in the bus-off state.
Note 3. This bit automatically sets to 0 after being set to 1. It should be read as 0.
Note 4. Set the TSRC bit to 1 in CAN operation mode.
Note 5. When the CANM[1:0] and SLPM bits are changed, check STR to ensure that the mode is switched. Do not change the CANM[1:0] bits or SLPM bit until the mode is switched.
Note 6. Write to the SLPM bit in CAN reset mode or CAN halt mode. When changing the SLPM bit, write 0 or 1 only to the SLPM bit.

MBM bit (CAN Mailbox Mode Select)

When the MBM bit is 0 (normal mailbox mode), mailboxes 0 to 31 are configured as transmit or receive mailboxes.

When the MBM bit is 1 (FIFO mailbox mode):

- Mailboxes 0 to 23 are configured as transmit or receive mailboxes
- Mailboxes 24 to 27 are configured as transmit FIFO
- Mailboxes 28 to 31 are configured as receive FIFO.

Transmit data is written into mailbox 24, a window mailbox for the transmit FIFO. Receive data is read from mailbox 28, a window mailbox for the receive FIFO.

Table 30.3 lists the mailbox configuration.

IDFM[1:0] bits (ID Format Mode Select)

The IDFM[1:0] bits specify the ID format.

MLM bit (Message Lost Mode Select*1)

The MLM bit specifies the operation when a new message is captured in an unread mailbox. Overwrite mode or overrun mode can be selected. All mailboxes, including the receive FIFO are set to either overwrite mode or overrun mode.

When the MLM bit is 0, all mailboxes are set to overwrite mode. Any new message received overwrites the pre-existing message.

When the MLM bit is 1, all mailboxes are set to overrun mode. Any new message received does not overwrite the pre-existing message, and the new message is discarded.

TPM bit (Transmission Priority Mode Select*1)

The TPM bit specifies the priority when transmitting messages.

The ID priority transmit mode or mailbox number transmit mode can be selected. All mailboxes are set for either ID priority transmission or mailbox number priority transmission.

When TPM is 0, ID priority transmit mode is selected and transmission priority is arbitrated, as defined in the CAN specification (ISO11898-1). In ID priority transmit mode, mailboxes 0 to 31 (in normal mailbox mode), and mailboxes 0 to 23 (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority.

Only the next message to be transmitted from the transmit FIFO is included in the transmission arbitration. If a FIFO message is currently being transmitted, the next pending message within the transmit FIFO is included in the transmission arbitration.

When TPM is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest mailbox number has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (0 to 23).

TSRC bit (Time Stamp Counter Reset Command*4)

The TSRC bit resets the time stamp counter. When this bit is set to 1, TSR is set to 0000h. This bit is automatically set to 0.

TSPS[1:0] bits (Time Stamp Prescaler Select*1)

The TSPS[1:0] bits select the prescaler for the time stamp. The reference clock for the time stamp can be selected to either 1-bit, 2-bit, 4-bit, or 8-bit time periods.

CANM[1:0] bits (CAN Operating Mode Select*5)

The CANM[1:0] bits select one of the following modes for the CAN module:

- CAN operation mode
- CAN reset mode
- CAN halt mode.

The CAN sleep mode is set in the SLPM bit. For details, see section 30.3, Operation Modes. When the CAN module enters CAN halt mode based on the BOM[1:0] setting, the CANM[1:0] bits are automatically set to 10b.

SLPM bit (CAN Sleep Mode)

When the SLPM bit is set to 1, the CAN module enters CAN sleep mode. When the SLPM bit is set to 0, the CAN module exits CAN sleep mode. For details, see section 30.3, Operation Modes.

BOM[1:0] bits (Bus-Off Recovery Mode*1)

The BOM[1:0] bits select bus-off recovery mode for the CAN module.

When the BOM[1:0] bits are 00b, the recovery from bus-off is compliant with the ISO11898-1 CAN specification. The CAN module recovers CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request occurs when recovering from bus-off.

When the BOM[1:0] bits are 01b and the CAN module reaches the bus-off state, the CANM[1:0] bits in CTLR are set to 10b to enter CAN halt mode. No bus-off recovery interrupt request occurs when recovering from bus-off, and TECR and RECR are set to 00h.

When the BOM[1:0] bits are 10b, the CANM[1:0] bits are set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters CAN halt mode after recovery from the bus-off state, and after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request occurs when recovering from bus-off, and TECR and RECR are set to 00h.

When the BOM[1:0] bits are 11b, the CAN module enters CAN halt mode by setting the CANM[1:0] bits to 10b while the CAN module is still in the bus-off state. No bus-off recovery interrupt request is generated when recovering from bus-off, and TECR and RECR are set to 00h. However, if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before the CANM[1:0] bits are set to 10b, a bus-off recovery interrupt request is generated.

If the CPU requests an entry to the CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when the BOM[1:0] bits are 01b, or at bus-off end when the BOM[1:0] bits are 10b), then the CPU request has higher priority.

RBOC bit (Forcible Return from Bus-Off*2)

When the RBOC bit is set to 1 in the bus-off state, the CAN module forcibly exits the bus-off state. This bit is automatically set to 0, and the error state changes from bus-off to error-active. When the RBOC bit is set to 1, RECR and TECR are set to 00h and the BOST bit in STR is set to 0, indicating that the CAN module is not in bus-off state. The other registers remain unchanged when RBOC is set to 1. No bus-off recovery interrupt request is generated by this

recovery from the bus-off state. Use the RBOC bit only when the BOM[1:0] bits are 00b (normal mode).

Table 30.3 Mailbox configuration

Mailbox	MBM bit = 0 (normal mailbox mode)	MBM bit = 1 (FIFO mailbox mode)*1 to *5
Mailboxes 0 to 23	Normal mailbox	Normal mailbox
Mailboxes 24 to 27		Transmit FIFO
Mailboxes 28 to 31		Receive FIFO

Note 1. The transmit FIFO is controlled by TFCR. The MCTL_TXj registers associated with mailboxes 24 to 27 are disabled. MCTL_TX24 to MCTL_TX27 cannot be used by the transmit FIFO.
Note 2. The receive FIFO is controlled by RFCR. The MCTL_RXj registers associated with mailboxes 28 to 31 are disabled. MCTL_RX28 to MCTL_RX31 cannot be used by the receive FIFO.
Note 3. See the MIER_FIFO register for information on the FIFO interrupts.
Note 4. The bits in MKIVLR associated with mailboxes 24 to 31 are disabled. Set these bits to 0.
Note 5. The transmit and receive FIFOs can be used for both data frames and remote frames.

30.2.2 Bit Configuration Register (BCR)

Address(es): CAN0.BCR 4005 0844h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TSEG1[3:0]				—	—	BRP[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SJW[1:0]		—	TSEG2[2:0]			—	—	—	—	—	—	—	CCLKS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CCLKS	CAN Clock Source Selection	0: PCLKB (generated by the PLL clock) 1: CANMCLK (generated by the main clock oscillator).	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	TSEG2[2:0]	Time Segment 2 Control	b10 b8 0 0 0: Setting prohibited 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	SJW[1:0]	Synchronization Jump Width Control	b13 b12 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25 to b16	BRP[9:0]	Baud Rate Prescaler Select*1	These bits set the frequency of the CAN communication clock (fCANCLK)	R/W
b27, b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit name	Description	R/W
b31 to b28	TSEG1[3:0]	Time Segment 1 Control	b31 b28 0 0 0 0: Setting prohibited 0 0 0 1: Setting prohibited 0 0 1 0: Setting prohibited 0 0 1 1: 4 Tq 0 1 0 0: 5 Tq 0 1 0 1: 6 Tq 0 1 1 0: 7 Tq 0 1 1 1: 8 Tq 1 0 0 0: 9 Tq 1 0 0 1: 10 Tq 1 0 1 0: 11 Tq 1 0 1 1: 12 Tq 1 1 0 0: 13 Tq 1 1 0 1: 14 Tq 1 1 1 0: 15 Tq 1 1 1 1: 16 Tq.	R/W

Tq: Time Quantum

Note 1. Do not select a value less than or equal to 1 while the SCKSCR.CKSEL[2:0] bits are 011b (selecting the main clock oscillator).

For details about setting the bit timing, see section 30.4, Data Transfer Rate Configuration. Set BCR before entering CAN halt mode or CAN operation mode from CAN reset mode. After the setting is made once, this register can be written to in CAN reset mode or CAN halt mode. A 32-bit read/write access must be performed carefully so as not to change bits [7:0].

CCLKS bit (CAN Clock Source Selection)

When the CCLKS bit is 0, the peripheral module clock (PCLKB) produced by the PLL frequency synthesizer is used as the CAN clock source (fCAN). When the CCLKS bit is 1, CANMCLK produced externally by the EXTAL pins is used as the CAN clock source (fCAN).

TSEG2[2:0] bits (Time Segment 2 Control)

The TSEG2[2:0] bits specify the length of the phase buffer segment 2 (PHASE_SEG2) with a Tq value. A value from 2 to 8 Tq can be set. Set a value smaller than that in the TSEG1[3:0] bits.

SJW[1:0] bits (Synchronization Jump Width Control)

The SJW[1:0] bits specify the synchronization jump width with a Tq value. A value from 1 to 4 Tq can be set. Set a value smaller than or equal to that in the TSEG2[2:0] bits.

BRP[9:0] bits (Baud Rate Prescaler Select*1)

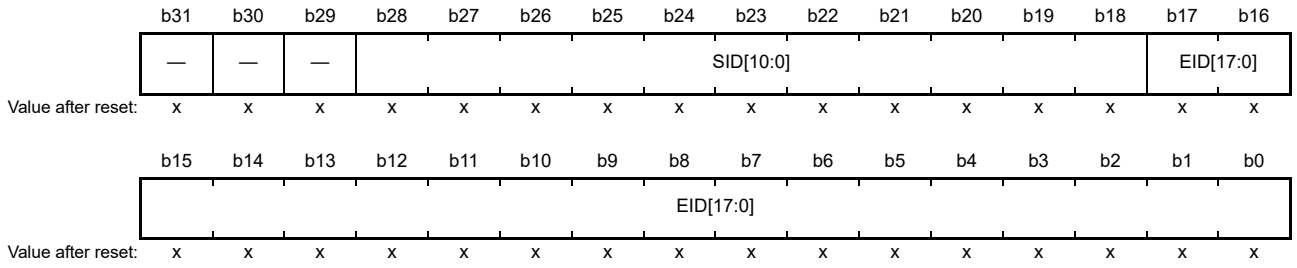
The BRP[9:0] bits set the frequency of the CAN communication clock (fCANCLK). The fCANCLK cycle is 1 Tq. If the setting is P (0 to 1023), the baud rate prescaler divides fCAN by P + 1.

TSEG1[3:0] bits (Time Segment 1 Control)

The TSEG1[3:0] bits specify the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1) with a time quantum (Tq) value. A value from 4 to 16 Tq can be set.

30.2.3 Mask Register k (MKRk) (k = 0 to 7)

Address(es): CAN0.MKR[0] 4005 0400h to CAN0.MKR[7] 4005 041Ch



x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID	0: Do not compare associated EID[17:0] bits 1: Compare associated EID[17:0] bits.	R/W
b28 to b18	SID[10:0]	Standard ID	0: Do not compare associated SID[10:0] bits 1: Compare associated SID[10:0] bits.	R/W
b31 to b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W

For the mask function in FIFO mailbox mode, see section 30.6, Acceptance Filtering and Masking Functions. Write to MKR0 to MKR7 in CAN reset mode or CAN halt mode.

EID[17:0] bits (Extended ID)

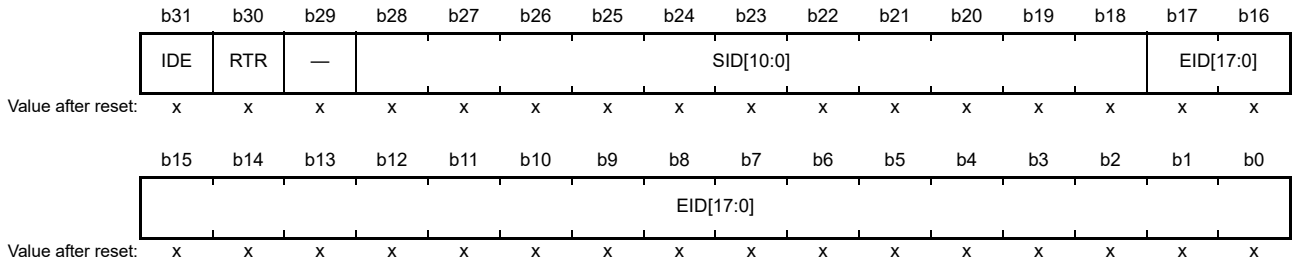
The EID[17:0] bits are the filter mask bits associated with the CAN extended ID bits. They are used to receive extended ID messages. When an EID[17:0] bit is set to 0, the received ID is not compared with the associated mailbox ID. When an EID[17:0] bit is set to 1, the received ID is compared with the associated mailbox ID.

SID[10:0] bits (Standard ID)

The SID[10:0] bits are the filter mask bits associated with the CAN standard ID bits. They are used to receive both standard ID and extended ID messages. When an SID[10:0] bit is set to 0, the received ID is not compared with the associated mailbox ID. When an SID[10:0] bit is set to 1, the received ID is compared with the associated mailbox ID.

30.2.4 FIFO Received ID Compare Registers 0 and 1 (FIDCR0 and FIDCR1)

Address(es): CAN0.FIDCR0 4005 0420h, CAN0.FIDCR1 4005 0424h



x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID	Extended ID of data and remote frames	R/W
b28 to b18	SID[10:0]	Standard ID	Standard ID of data and remote frames	R/W
b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b30	RTR	Remote Transmission Request	0: Data frame 1: Remote frame.	R/W

Bit	Symbol	Bit name	Description	R/W
b31	IDE	ID Extension*1	0: Standard ID 1: Extended ID.	R/W

Note 1. When the CTLR.IDFM[1:0] bits are any value other than 10b (mixed ID mode), the IDE bit should be written with 0 and read as 0.

FIDCR0 and FIDCR1 are enabled when the MBM bit in CTLR is set to 1 (FIFO mailbox mode). In this mode, the EID[17:0], SID[10:0], RTR, and IDE bits in mailbox 28 to mailbox 31 are disabled. Write to FIDCR0 and FIDCR1 in CAN reset mode or CAN halt mode. For information on using FIDCR0 and FIDCR1, see section 30.6, Acceptance Filtering and Masking Functions.

EID[17:0] bits (Extended ID)

The EID[17:0] bits set the extended ID of data and remote frames. These bits are used to receive extended ID messages.

SID[10:0] bits (Standard ID)

The SID[10:0] bits set the standard ID of data frames and remote frames. These bits are used to receive both standard ID and extended ID messages.

RTR bit (Remote Transmission Request)

The RTR bit sets the frame format to data frames or remote frames:

- When the RTR bits in both FIDCR0 and FIDCR1 registers are set to 0, only data frames are received
- When the RTR bits in both FIDCR0 and FIDCR1 registers are set to 1, only remote frames are received
- When the RTR bits in both FIDCR0 and FIDCR1 registers are set to different values, both data frames and remote frames are received.

IDE bit (ID Extension*1)

The IDE bit sets the ID format to standard ID or extended ID. The IDE bit is enabled when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode):

- When IDE bits in both FIDCR0 and FIDCR1 are set to 0, only standard ID frames are received
- When IDE bits in both FIDCR0 and FIDCR1 are set to 1, only extended ID frames are received
- When IDE bits in FIDCR0 and FIDCR1 are set to different values, both standard and extended ID frames are received.

30.2.5 Mask Invalid Register (MKIVLR)

Address(es): CAN0.MKIVLR 4005 0428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MB31 to MB0	Mask Invalid	0: Mask valid 1: Mask invalid.	R/W

Each bit in MKIVLR is associated with a mailbox of the same number. Bit [0] in MKIVLR corresponds to mailbox 0 (MB0), and bit [31] corresponds to mailbox 31 (MB31).

Note: Set bits [31:24] to 0 in FIFO mailbox mode.

When a bit is set to 1, the associated acceptance mask register becomes invalid for the associated mailbox. When a mask invalid bit is set to 1, a message is received by the associated mailbox only if the receive message ID matches the mailbox ID exactly. Write to MKIVLR in CAN reset or halt mode.

30.2.6 Mailbox Register j (MBj_ID, MBj_DL, MBj_Dm, MBj_TS) (j = 0 to 31; m = 0 to 7)

Table 30.4 lists the CANi mailbox memory mapping, and Table 30.5 lists the CAN data frame configuration. The value of the CANi mailbox after reset is undefined.

Write to MBj_ID, MBj_DL, MBj_Dm, and MBj_TS registers only when the related MCTL_TXj or MCTL_RXj register (j = 0 to 31) is 00h and the associated mailbox does not process an abort request. See Table 30.4 for details on register addresses.

Table 30.4 CAN mailbox memory mapping

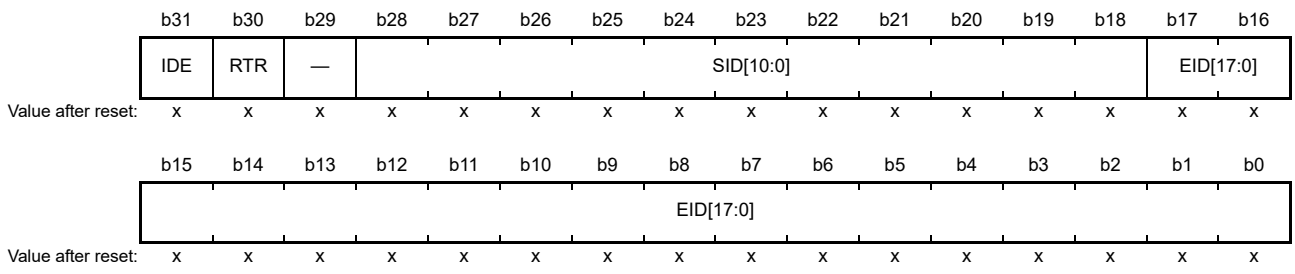
Address	Message content
CAN0	**Memory mapping**
4005 0200h + 16 × j + 0	IDE, RTR, SID10 to SID6
4005 0200h + 16 × j + 1	SID5 to SID0, EID17, EID16
4005 0200h + 16 × j + 2	EID15 to EID8
4005 0200h + 16 × j + 3	EID7 to EID0
4005 0200h + 16 × j + 4	-
4005 0200h + 16 × j + 5	Data length code (DLC[3:0])
4005 0200h + 16 × j + 6	Data byte 0
4005 0200h + 16 × j + 7	Data byte 1
4005 0200h + 16 × j + 8	Data byte 2
4005 0200h + 16 × j + 9	Data byte 3
4005 0200h + 16 × j + 10	Data byte 4
4005 0200h + 16 × j + 11	Data byte 5
4005 0200h + 16 × j + 12	Data byte 6
4005 0200h + 16 × j + 13	Data byte 7
4005 0200h + 16 × j + 14	Time stamp upper byte
4005 0200h + 16 × j + 15	Time stamp lower byte

Table 30.5 CAN data frame configuration

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC1	DATA0	DATA1	…	DATA7

The previous value of each mailbox is saved unless a new message is received.

Address(es): CAN0.MB0_ID 4005 0200h to CAN0.MB31_ID 4005 03F0h



x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID*1	Extended ID of data and remote frames	R/W
b28 to b18	SID[10:0]	Standard ID	Standard ID of data and remote frames	R/W
b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b30	RTR	Remote Transmission Request	0: Data frame 1: Remote frame.	R/W
b31	IDE	ID Extension*2	0: Standard ID 1: Extended ID.	R/W

Note 1. If the mailbox receives a standard ID message, the EID bits in the mailbox are undefined.
Note 2. The IDE bit is enabled when the CTLR.IDFM[1:0] bits are 10b (mixed ID mode). When the IDFM[1:0] bits are any value other than 10b, the IDE bit should be written with 0 and read as 0.

Address(es): CAN0.MB0_DL 4005 0204h to CAN0.MB31_DL 4005 03F4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	DLC[3:0]			
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DLC[3:0]	Data Length Code*1	b3 b0 0 0 0 0: Data length = 0 byte 0 0 0 1: Data length = 1 byte 0 0 1 0: Data length = 2 bytes 0 0 1 1: Data length = 3 bytes 0 1 0 0: Data length = 4 bytes 0 1 0 1: Data length = 5 bytes 0 1 1 0: Data length = 6 bytes 0 1 1 1: Data length = 7 bytes 1 x x x: Data length = 8 bytes.	R/W
b15 to b4	—	Reserved	The read value is undefined. The write value should be 0.	R/W

x: Don't care
Note 1. If the mailbox receives a message with data length (set in DLC[3:0]) of n bytes, where n is less than 8, the data in the DATAn to DATA7 registers in the mailbox is undefined. DATA0 to DATA7 are data registers for this mailbox. For example, if data length is 6 bytes (DLC[3:0] = 6h), the data in DATA6 and DATA7 registers is undefined.

Address(es): CAN0.MB0_D0 4005 0206h to CAN0.MB31_D0 4005 03F6h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA0							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D1 4005 0207h to CAN0.MB31_D1 4005 03F7h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA1							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D2 4005 0208h to CAN0.MB31_D2 4005 03F8h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA2							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D3 4005 0209h to CAN0.MB31_D3 4005 03F9h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA3							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D4 4005 020Ah to CAN0.MB31_D4 4005 03FAh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA4							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D5 4005 020Bh to CAN0.MB31_D5 4005 03FBh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA5							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D6 4005 020Ch to CAN0.MB31_D6 4005 03FCh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA6							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D7 4005 020Dh to CAN0.MB31_D7 4005 03FDh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA7							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DATA0 to DATA7	Data Bytes 0 to 7*1,*2	DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB-first, and transmission or reception starts from bit [7].	R/W

Note 1. If the mailbox receives a message with n bytes, where n is less than 8 bytes, the DATAn to DATA7 values in the mailbox are undefined.

Note 2. If the mailbox receives a remote frame, the previous values of DATA0 to DATA7 in the mailbox are saved.

Address(es): CAN0.MB0_TS 4005 020Eh to CAN0.MB31_TS 4005 03FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TSH[7:0]								TSL[7:0]							
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	TSL[7:0]	Time Stamp Lower Byte	The TSH[7:0] and TSL[7:0] bits store the counter value of the time stamp when received messages are stored in the mailbox.	R/W
b15 to b8	TSH[7:0]	Time Stamp Higher Byte		R/W

EID[17:0] bits (Extended ID*1)

The EID[17:0] bits set the extended ID of data frames and remote frames. These bits transmit or receive extended ID messages.

SID[10:0] bits (Standard ID)

The SID[10:0] bits set the standard ID of data frames and remote frames. These bits transmit or receive both standard ID and extended ID messages.

RTR bit (Remote Transmission Request)

The RTR bit sets the frame format to data frames or remote frames:

- The receive mailbox only receives frames with the format specified in the RTR bit
- The transmit mailbox transmits frames with the frame format specified in the RTR bit
- The receive FIFO mailbox receives the data frame, remote frame, or both frames as specified in the RTR bit in FIDCR0 and FIDCR1
- The transmit FIFO mailbox transmits the data frame or remote frame as specified in the RTR bit in the relevant transmit message.

IDE bit (ID Extension*2)

The IDE bit sets the ID format to standard ID or extended ID. The IDE bit is enabled when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode):

- The receive mailbox receives only the ID format specified in the IDE bit
- The transmit mailbox transmits with the ID format specified in the IDE bit
- The receive FIFO mailbox receives messages with the standard ID and extended ID settings specified in the IDE bit in FIDCR0 and FIDCR1
- The transmit FIFO mailbox transmits messages with the standard ID or extended ID settings specified in the IDE bit in the transmit message.

DLC[3:0] bits (Data Length Code*1)

The DLC[3:0] bits specify the data length to be transmitted in data frames. When a remote frame is used to request data, this field specifies the requested data length.

When a data frame is received, the received data length is stored in this field. When a remote frame is received, this field stores the requested data length.

30.2.7 Mailbox Interrupt Enable Register (MIER)

Address(es): CAN0.MIER 4005 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MB31 to MB0	Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled. Bit [31] is associated with mailbox 31 (MB31), and bit [0] with mailbox 0 (MB0).	R/W

The MIER register can enable interrupts for each mailbox independently. This register is available in normal mailbox mode. Do not access this register in FIFO mailbox mode.

Each bit is associated with a mailbox having the same number. These bits enable or disable transmission and reception complete interrupts for the associated mailboxes as follows:

- Bit [0] in MIER is associated with mailbox 0 (MB0)
- Bit [31] in MIER is associated with mailbox 31 (MB31).

Write to MIER only when the associated MCTL_TXj or MCTL_RXj register (j = 0 to 31) is 00h and the associated mailbox does not process a transmission or reception abort request.

30.2.8 Mailbox Interrupt Enable Register for FIFO Mailbox Mode (MIER_FIFO)

Address(es): CAN0.MIER_FIFO 4005 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	MB29	MB28	—	—	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b23 to b0	MB23 to MB0	Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled. Bit [23] corresponds to mailbox 23 (MB23), and bit [0] corresponds to mailbox 0 (MB0).	R/W
b24	MB24	Transmit FIFO Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b25	MB25	Transmit FIFO Interrupt Generation Timing Control	0: Generated every time transmission completes 1: Generated when the transmit FIFO empties on transmission completion.	R/W

Bit	Symbol	Bit name	Description	R/W
b27, b26	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b28	MB28	Receive FIFO Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b29	MB29	Receive FIFO Interrupt Generation Timing Control*1	0: Generated every time reception completes 1: Generated when the receive FIFO becomes a buffer warning*2 on reception completion.	R/W
b31, b30	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Note 1. No interrupt request occurs when the receive FIFO becomes a buffer warning because it is full.
Note 2. Buffer warning indicates a state in which the third message is stored in the receive FIFO.

The MIER_FIFO register can independently enable interrupts for each mailbox and FIFO. This register is available in FIFO mailbox mode. Do not access this register in normal mailbox mode.

The MB0 to MB23 bits are associated with the mailbox of the same number. These bits enable or disable transmission and reception complete interrupts for the associated mailboxes:

- Bit [0] in MIER_FIFO is associated with mailbox 0 (MB0)
- Bit [23] in MIER_FIFO is associated with mailbox 23 (MB23).

MB24, MB25, MB28, and MB29 specify whether the transmit and receive FIFO interrupts are enabled or disabled, and the timing when interrupt requests are generated.

Write to the MIER_FIFO register only when the associated MCTL_TXj or MCTL_RXj register (j = 0 to 31) is 00h and the associated mailbox does not process a transmission or reception abort request. In addition, change the bits in MIER_FIFO for the associated FIFO only when all the following conditions are true:

- The TFE bit in TFCR is 0 and the TFEST bit is 1
- The RFE bit in RFCR is 0 and the RFEST flag in RFCR is 1.

30.2.9 Message Control Register for Transmit (MCTL_TXj) (j = 0 to 31)

- Transmit mode (when the TRMREQ bit is 1 and the RECREQ bit is 0)

Address(es): CAN0.MCTL_TX[0] 4005 0820h to CAN0.MCTL_TX[31] 4005 083Fh,

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SENTDATA	Transmission Complete Flag*1,*2	0: Transmission not complete 1: Transmission complete.	R/W
b1	TRMACTIVE	Transmission-in-Progress Status Flag	0: Transmission pending or not requested 1: Transmission in progress.	R
b2	TRMABT	Transmission Abort Complete Flag*1,*2	0: Transmission started, transmission abort failed because transmission completed, or transmission abort not requested 1: Transmission abort complete.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0: Disable one-shot transmission 1: Enable one-shot transmission.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	RECREQ	Receive Mailbox Request *2,*3,*4,*5	0: Do not configure for reception 1: Configure for reception.	R/W
b7	TRMREQ	Transmit Mailbox Request *2,*4	0: Do not configure for transmission 1: Configure for transmission.	R/W

Note 1. Write 0 only. Writing 1 has no effect.
Note 2. When writing to bits in this register, write 1 to SENTDATA and TRMABT flags if these bits are not the write target.
Note 3. To enter one-shot transmit mode, write 1 to the ONESHOT bit at the same time as setting the TRMREQ bit to 1. To exit one-shot transmit mode, write 0 to the ONESHOT bit after the message is transmitted or aborted.
Note 4. Do not set both the RECREQ and TRMREQ bits to 1.
Note 5. When setting the RECREQ bit to 0, set the SENTDATA, TRMACTIVE, and TRMABT flags to 0 simultaneously.

MCTL_TXj sets mailbox j to transmit mode or receive mode. In transmit mode, MCTL_TXj also controls and indicates the transmission status. Do not access MCTL_TXj if mailbox j is in receive mode. Only write to MCTL_TXj in CAN operation or halt mode. Do not use MCTL_TX24 to MCTL_TX31 in FIFO mailbox mode.

SENTDATA flag (Transmission Complete Flag*1,*2)

The SENTDATA flag is set to 1 when data transmission from the associated mailbox is complete. This flag is set to 0 through a software write. To set this flag to 0, first set the TRMREQ bit to 0. The SENTDATA and TRMREQ flags cannot be set to 0 simultaneously. To transmit a new message from the associated mailbox, set the SENTDATA flag to 0.

TRMACTIVE flag (Transmission-in-Progress Status Flag)

The TRMACTIVE flag is set to 1 when the associated mailbox of the CAN module begins to transmit a message. It is set to 0 when the CAN module loses the CAN bus arbitration, when a CAN bus error occurs, or when data transmission completes.

TRMABT flag (Transmission Abort Complete Flag*1,*2)

The TRMABT flag is set to 1 in the following cases:

- Following a transmission abort request, when the transmission abort is complete before starting transmission
- Following a transmission abort request, when the CAN module detects CAN bus arbitration-lost or a CAN bus error
- In one-shot transmission mode (RECREQ = 0, TRMREQ = 1, and ONESHOT = 1), when the CAN module detects a CAN bus arbitration-lost or a CAN bus error.

The TRMABT flag is not set to 1 when data transmission is complete. The SENTDATA flag is set to 1 and the TRMABT flag is set to 0 through a software write.

ONESHOT bit (One-Shot Enable*2,*3)

When the ONESHOT bit is set to 1 in transmit mode (RECREQ = 0 and TRMREQ = 1), the CAN module transmits a message only one time. The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration-lost occurs. When transmission is complete, the SENTDATA flag is set to 1. If transmission does not complete because of a CAN bus error or CAN bus arbitration-lost error, the TRMABT flag is set to 1. Set the ONESHOT bit to 0 after the SENTDATA or TRMABT flag is set to 1.

RECREQ bit (Receive Mailbox Request)

The RECREQ bit selects the receive modes listed in Table 30.10.

When the RECREQ bit is set to 1, the associated mailbox is configured for reception of a data frame or remote frame.

When the RECREQ bit is set to 0, the associated mailbox is not configured for reception of a data frame or remote frame.

Due to hardware protection, the RECREQ bit cannot be set to 0 through a software write during the following period:

- Hardware protection is started from the acceptance filter processing (the beginning of the CRC field)
- Hardware protection is released:
  - For the mailbox that is specified to receive the incoming message, after the received data is stored in the mailbox or a CAN bus error occurs. This means that the maximum period of hardware protection is from the beginning of CRC field to the end of the 7th bit of EOF.
  - For the other mailboxes, after acceptance filter processing
  - If no mailbox is specified to receive the message, after acceptance filter processing.

When setting the RECREQ bit to 1, do not set the TRMREQ bit to 1. To change the configuration of a mailbox from transmission to reception, first abort the transmission, then set the SENTDATA and TRMABT flags to 0 before changing to reception.

Note: MCTL_TXj.RECREQ is the mirror bit of MCTL_RXj.RECREQ.

TRMREQ bit (Transmit Mailbox Request)

The TRMREQ bit selects the transmit modes listed in Table 30.10.

When the TRMREQ bit is set to 1, the associated mailbox is configured for transmission of a data frame or remote frame.

When the TRMREQ bit is set to 0, the associated mailbox is not configured for transmission of a data frame or remote frame.

If the TRMREQ bit is changed from 1 to 0 to cancel the associated transmission request, either the TRMABT or SENTDATA flag is set to 1. When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1. To change the configuration of a mailbox from reception to transmission, first abort the reception, then set the NEWDATA and MSGLOST flags to 0 before changing to transmission.

Note: MCTL_TXj.TRMREQ is the mirror bit of MCTL_RXj.TRMREQ.

30.2.10 Message Control Register for Receive (MCTL_RXj) (j = 0 to 31)

- Receive mode (when the TRMREQ bit is 0 and the RECREQ bit is 1)

Address(es): CAN0.MCTL_RX[0] 4005 0820h to CAN0.MCTL_RX[31] 4005 083Fh,

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NEWDATA	Reception Complete Flag*1,*2	0: No data received, or 0 was written to the flag 1: New message is being stored or was stored in the mailbox.	R/W
b1	INVALDATA	Reception-in-Progress Status Flag	0: Message valid 1: Message being updated.	R
b2	MSGLOST	Message Lost Flag*1,*2	0: Message not overwritten or overrun 1: Message overwritten or overrun.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0: Disable one-shot reception 1: Enable one-shot reception.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	RECREQ	Receive Mailbox Request *2,*3,*4,*5	0: Do not configure for reception 1: Configure for reception.	R/W
b7	TRMREQ	Transmit Mailbox Request *2,*4	0: Do not configure for transmission 1: Configure for transmission.	R/W

Note 1. Write 0 only. Writing 1 has no effect.
Note 2. When writing to bits in this register, write 1 to the NEWDATA and MSGLOST flags if they are not the write target.
Note 3. To enter one-shot receive mode, write 1 to the ONESHOT bit at the same time as setting the RECREQ bit to 1. To exit one-shot receive mode, write 0 to the ONESHOT bit after writing 0 to the RECREQ bit and confirming that it is 0.
Note 4. Do not set both the RECREQ and TRMREQ bits to 1.
Note 5. When setting the RECREQ bit to 0, set MSGLOST, NEWDATA, and RECREQ to 0 simultaneously.

MCTL_RXj sets mailbox j to transmit or receive mode. In receive mode, MCTL_RXj also controls and indicates the reception status.

Do not access MCTL_RXj if mailbox j is in transmit mode. Only write to the MCTL_RXj in CAN operation or halt mode. Do not use MCTL_RX24 to MCTL_RX31 registers in FIFO mailbox mode.

NEWDATA flag (Reception Complete Flag*1,*2)

The NEWDATA flag is set to 1 when a new message is being stored or was stored in the mailbox. Always set this bit to 1 simultaneously with the INVALDATA flag. The NEWDATA flag is set to 0 through a software write. The NEWDATA

flag cannot be set to 0 through a software write when the associated INVALDATA flag is 1.

INVALDATA flag (Reception-in-Progress Status Flag)

After the completion of a message reception, the INVALDATA flag is set to 1 while the received message is updated in the associated mailbox. The INVALDATA flag is set to 0 immediately after the message is stored. If the mailbox is read when the INVALDATA flag is 1, the data is undefined.

MSGLOST flag (Message Lost Flag*1,*2)

The MSGLOST flag is set to 1 when the mailbox is overwritten or overrun by a new received message while the NEWDATA flag is 1. The MSGLOST flag is set to 1 at the end of the 6th bit of EOF. The MSGLOST flag is set to 0 through a software write.

In both overwrite and overrun modes, the MSGLOST flag cannot be set to 0 through a software write during the 5 PCLKB cycles following the 6th bit of EOF.

ONESHOT bit (One-Shot Enable*2,*3)

When the ONESHOT bit is set to 1 in receive mode (RECREQ = 1 and TRMREQ = 0), the mailbox receives a message only one time. The mailbox does not behave as a receive mailbox after having received the message one time. The behavior of the NEWDATA and INVALDATA flags is the same as in normal receive mode. In one-shot receive mode, the MSGLOST flag is not set to 1. To set the ONESHOT bit to 0, first write 0 to the RECREQ bit and ensure that it is 0.

RECREQ bit (Receive Mailbox Request)

The RECREQ bit selects the receive modes listed in Table 30.10.

When the RECREQ bit is set to 1, the associated mailbox is configured for reception of a data frame or remote frame.

When the RECREQ bit is set to 0, the associated mailbox is not configured for reception of a data frame or remote frame.

Due to hardware protection, the RECREQ bit cannot be set to 0 through a software write during the following period:

- Hardware protection is started from the acceptance filter processing (the beginning of the CRC field)
- Hardware protection is released:
  - For the mailbox that is specified to receive the incoming message, after the received data is stored in the mailbox or a CAN bus error occurs. The maximum period of hardware protection is from the beginning of the CRC field to the end of the 7th bit of EOF.
  - For the other mailboxes, after the acceptance filter processing
  - If no mailbox is specified to receive the message, after acceptance filter processing.

When setting the RECREQ bit to 1, do not set the TRMREQ bit to 1. To change the configuration of a mailbox from transmission to reception, first abort the transmission, then set the SENTDATA and TRMABT flags to 0 before changing to reception.

Note: MCTL_RXj.RECREQ is the mirror bit of MCTL_TXj.RECREQ.

TRMREQ bit (Transmit Mailbox Request)

The TRMREQ bit selects the transmit modes listed in Table 30.10.

When the TRMREQ bit is set to 1, the associated mailbox is configured for transmission of a data frame or remote frame. When the TRMREQ bit is set to 0, the associated mailbox is not configured for transmission of a data frame or remote frame.

If the TRMREQ bit is changed from 1 to 0 to cancel the associated transmission request, either the TRMABT or the SENTDATA flag is set to 1. When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1. To change the configuration of a mailbox from reception to transmission, first abort the reception, and then set the NEWDATA and MSGLOST flags to 0 before changing to transmission.

Note: MCTL_RXj.TRMREQ is the mirror bit of MCTL_TXj.TRMREQ.

30.2.11 Receive FIFO Control Register (RFCR)

Address(es): CAN0.RFCR 4005 0848h

	b7	b6	b5	b4	b3	b2	b1	b0
	RFEST	RFWST	RFFST	RFMLF	RFUST[2:0]			RFE
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RFE	Receive FIFO Enable	0: Receive FIFO disabled 1: Receive FIFO enabled.	R/W
b3 to b1	RFUST[2:0]	Receive FIFO Unread Message Number Status	b3 b1 0 0 0: No unread message 0 0 1: 1 unread message 0 1 0: 2 unread messages 0 1 1: 3 unread messages 1 0 0: 4 unread messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved.	R
b4	RFMLF	Receive FIFO Message Lost Flag	0: Receive FIFO message not lost 1: Receive FIFO message lost.	R/W
b5	RFFST	Receive FIFO Full Status Flag	0: Receive FIFO not full 1: Receive FIFO full (4 unread messages).	R
b6	RFWST	Receive FIFO Buffer Warning Status Flag	0: Receive FIFO has no buffer warning 1: Receive FIFO has buffer warning (3 unread messages).	R
b7	RFEST	Receive FIFO Empty Status Flag	0: Unread message in receive FIFO 1: No unread message in receive FIFO.	R

Write to the RFCR register in CAN operation mode or halt mode.

RFE bit (Receive FIFO Enable)

When the RFE bit is set to 1, the receive FIFO is enabled.

When the RFE bit is set to 0, the receive FIFO is disabled for reception and becomes empty (RFEST = 1). Write 0 to the RFE bit simultaneously with the RFMLF flag setting.

Do not set this bit to 1 in normal mailbox mode (MBM bit in CTLR = 0). Due to hardware protection, the RFE bit cannot be set to 0 through a software write during the following period:

- Hardware protection is started from acceptance filter processing (the beginning of the CRC field)
- Hardware protection is released:
  - If the receive FIFO is specified to receive the incoming message, after the received data is stored in the receive FIFO or a CAN bus error occurs. The maximum period of hardware protection is from the beginning of the CRC field to the end of the 7th bit of EOF.
  - If the receive FIFO is not specified to receive the message, after acceptance filter processing.

RFUST[2:0] bits (Receive FIFO Unread Message Number Status)

The RFUST[2:0] bits indicate the number of unread messages in the receive FIFO. The value of the RFUST[2:0] bits is initialized to 000b when the RFE bit is set to 0.

RFMLF flag (Receive FIFO Message Lost Flag)

The RFMLF flag is set to 1 (receive FIFO message lost) when the receive FIFO receives a new message and is full. It is set to 1 at the end of the 6th bit of EOF.

The RFMLF flag is set to 0 through a software write (writing 1 has no effect). In both overwrite and overrun modes, if the receive FIFO is full and determined to have received a message, the RFMLF flag cannot be set to 0 (no receive FIFO

message lost) through a software write during 5 PCLKB cycles following the 6th bit of EOF, due to hardware protection.

RFFST flag (Receive FIFO Full Status Flag)

The RFFST flag is set to 1 (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. The RFFST flag is 0 (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. The flag is set to 0 when the RFE bit is 0.

RFWST flag (Receive FIFO Buffer Warning Status Flag)

The RFWST flag is set to 1 (receive FIFO buffer warning) when the number of unread messages in the receive FIFO is 3. The RFWST flag is 0 (no receive FIFO buffer warning) when the number of unread messages in the receive FIFO is less than 3 or equal to 4. The RFWST flag is set to 0 when the RFE bit is 0.

RFEST flag (Receive FIFO Empty Status Flag)

The RFEST flag is set to 1 (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is 0. The RFEST flag is set to 1 when the RFE bit is set to 0. The RFEST flag is set to 0 (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more.

Figure 30.2 shows the receive FIFO mailbox operation.

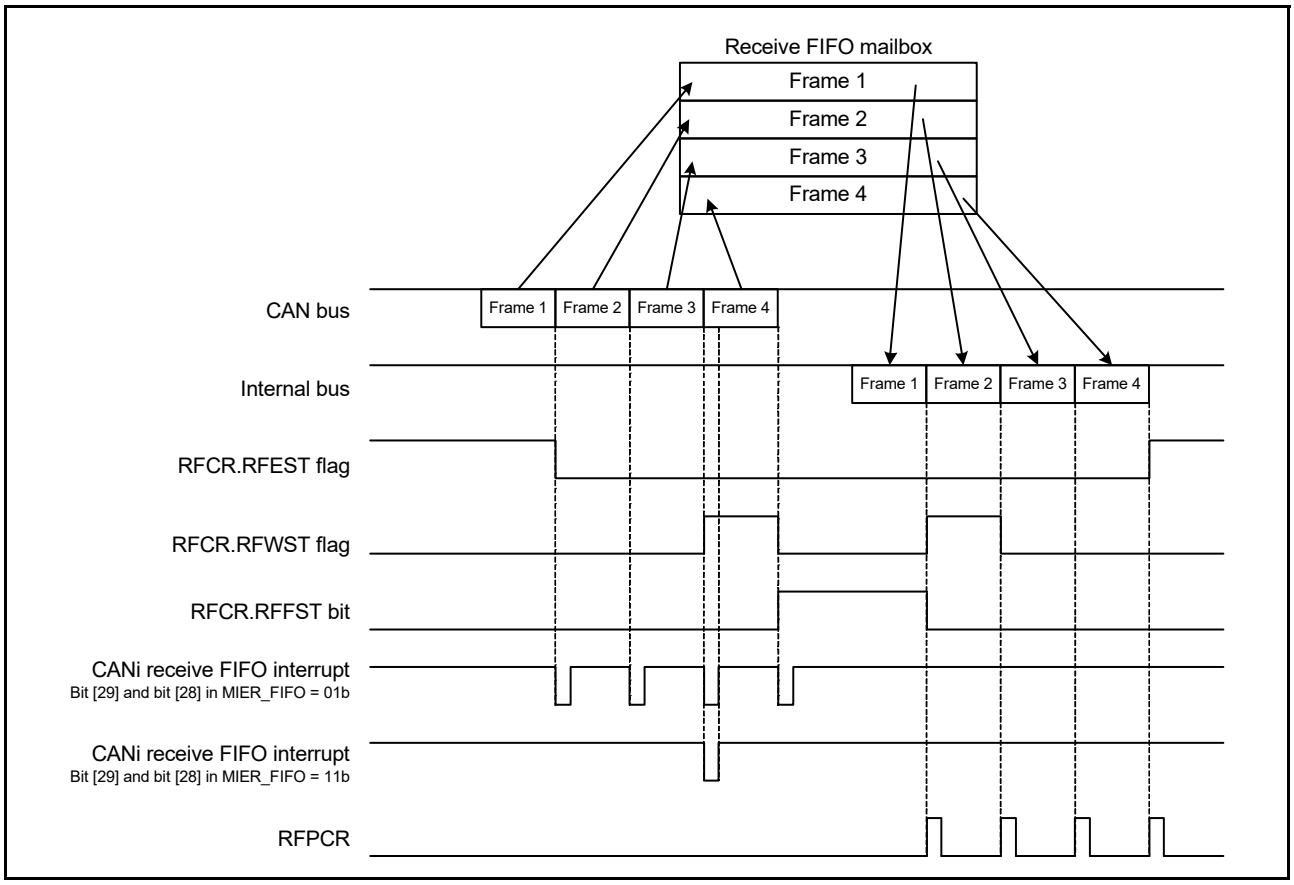


Figure 30.2 Receive FIFO mailbox operation with bits [29:28] in MIER_FIFO = 01b or 11b

30.2.12 Receive FIFO Pointer Control Register (RFPCR)

Address(es): CAN0.RFPCR 4005 0849h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	The CPU pointer for the receive FIFO is incremented by writing FFh to RFPCR	W

When the receive FIFO is not empty, write FFh to RFPCR through software to increment the CPU pointer to the next mailbox location. Do not write to RFPCR when the RFE bit in RFCR is 0 (receive FIFO disabled).

Both the CAN and CPU pointers are incremented when a new message is received and the RFFST flag is 1 (receive FIFO is full) in overwrite mode. When the RFMLF flag is 1 in this condition, the CPU pointer does not increment on a software write to RFPCR.

30.2.13 Transmit FIFO Control Register (TFCR)

Address(es): CAN0.TFCR 4005 084Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	TFEST	TFFST	—	—	TFUST[2:0]			TFE
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TFE	Transmit FIFO Enable	0: Transmit FIFO disabled 1: Transmit FIFO enabled.	R/W
b3 to b1	TFUST[2:0]	Transmit FIFO Unsent Message Number Status	b3 b1 0 0 0: 0 unsent messages 0 0 1: 1 unsent message 0 1 0: 2 unsent messages 0 1 1: 3 unsent messages 1 0 0: 4 unsent messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved.	R
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	TFFST	Transmit FIFO Full Status	0: Transmit FIFO is not full 1: Transmit FIFO is full (4 unsent messages).	R
b7	TFEST	Transmit FIFO Empty Status	0: Unsent message in transmit FIFO 1: No unsent message in transmit FIFO.	R

Write to the TFCR register in CAN operation mode or halt mode.

TFE bit (Transmit FIFO Enable)

When the TFE bit is set to 1, the transmit FIFO is enabled.

When the TFE bit is set to 0, the transmit FIFO becomes empty (TFEST = 1), and unsent messages in the transmit FIFO are lost in the following ways:

- Immediately if a message from the transmit FIFO is not scheduled for the next transmission or is already in transmission

- On completion of transmission, on a CAN bus error, a CAN bus arbitration-lost, or an entry to CAN halt mode, if a message from the transmit FIFO is scheduled for the next transmission or is already in transmission.

Before setting the TFE bit to 1 again, ensure that the TFEST bit is set to 1. After setting the TFE bit to 1, write transmit data to mailbox 24.

Do not set the TFE bit to 1 in normal mailbox mode (MBM bit in CTLR = 0).

TFUST[2:0] bits (Transmit FIFO Unsent Message Number Status)

The TFUST[2:0] bits indicate the number of unsent messages in the transmit FIFO. These bits are set to 000b after the TFE bit is set to 0 and transmission aborts or completes.

TFFST bit (Transmit FIFO Full Status)

The TFFST bit is set to 1 (transmit FIFO is full) when the number of unsent messages in the transmit FIFO is 4. The TFFST bit is set to 0 (transmit FIFO is not full) when the number of unsent messages in the transmit FIFO is less than 4. The TFFST bit is set to 0 when transmission from the transmit FIFO is aborted.

TFEST bit (Transmit FIFO Empty Status)

The TFEST bit is set to 1 (no message in transmit FIFO) when the number of unsent messages in the transmit FIFO is 0. The TFEST bit is set to 1 when transmission from the transmit FIFO is aborted. The TFEST bit is set to 0 (message in transmit FIFO) when the number of unsent messages in the transmit FIFO is not 0.

Figure 30.3 shows the transmit FIFO mailbox operation.

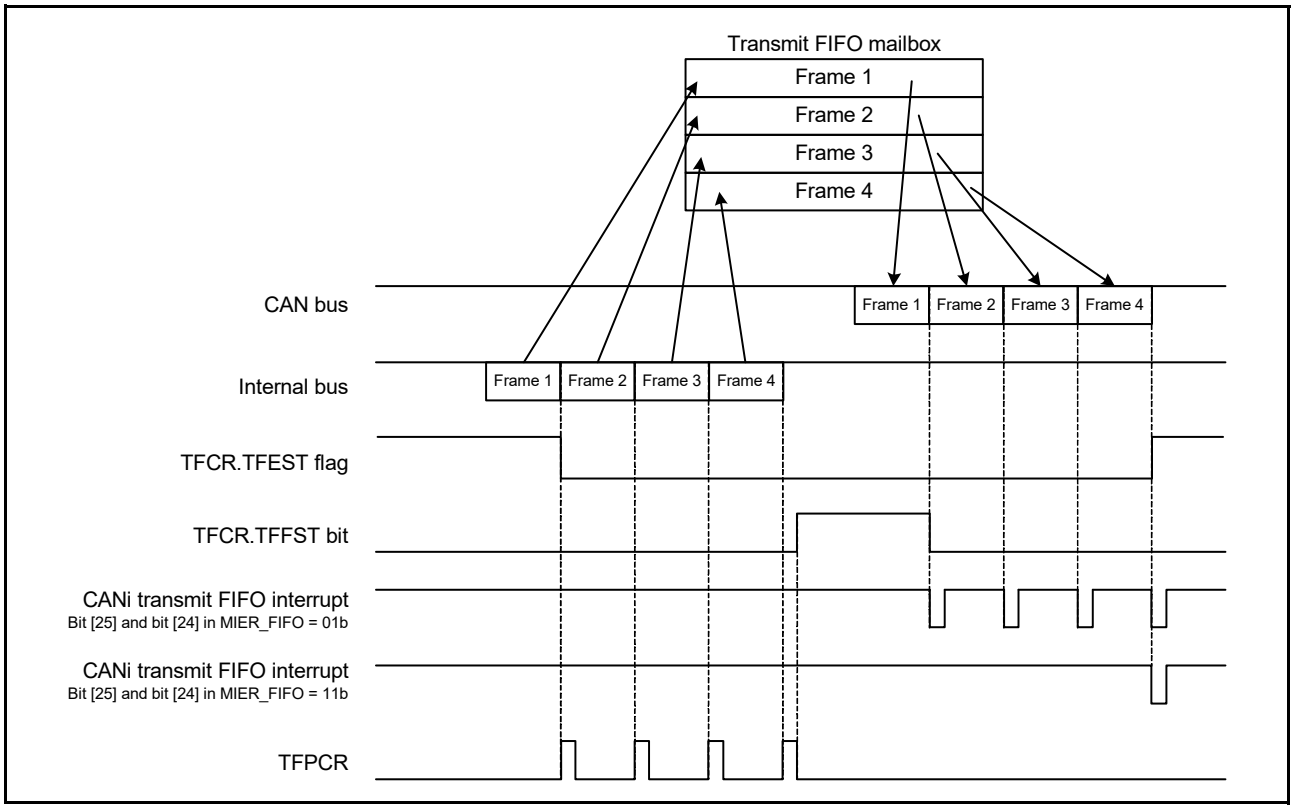


Figure 30.3 Transmit FIFO mailbox operation when bits [25:24] in MIER_FIFO = 01b or 11b

30.2.14 Transmit FIFO Pointer Control Register (TFPCR)

Address(es): CAN0.TFPCR 4005 084Bh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	The CPU pointer for the transmit FIFO is incremented by writing FFh to TFPCR	W

When the transmit FIFO is not full, write FFh to the TFPCR register through software to increment the CPU pointer for the transmit FIFO to the next mailbox location.

Do not write to TFPCR when the TFE bit in TFCR is 0 (transmit FIFO disabled).

30.2.15 Status Register (STR)

Address(es): CAN0.STR 4005 0842h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST	EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NDST	NEWDATA Status Flag	0: No mailbox with NEWDATA = 1 1: One or more mailboxes with NEWDATA = 1.	R
b1	SDST	SENTDATA Status Flag	0: No mailbox with SENTDATA = 1 1: One or more mailboxes with SENTDATA = 1.	R
b2	RFST	Receive FIFO Status Flag	0: Receive FIFO empty 1: Message in receive FIFO.	R
b3	TFST	Transmit FIFO Status Flag	0: Transmit FIFO full 1: Transmit FIFO not full.	R
b4	NMLST	Normal Mailbox Message Lost Status Flag	0: No mailbox with MSGLOST = 1 1: One or more mailboxes with MSGLOST = 1.	R
b5	FMLST	FIFO Mailbox Message Lost Status Flag	0: RFMLF = 0 1: RFMLF = 1.	R
b6	TABST	Transmission Abort Status Flag	0: No mailbox with TRMABT = 1 1: One or more mailboxes with TRMABT = 1.	R
b7	EST	Error Status Flag	0: No error occurred 1: Error occurred.	R
b8	RSTST	CAN Reset Status Flag	0: Not in CAN reset mode 1: In CAN reset mode.	R
b9	HLTST	CAN Halt Status Flag	0: Not in CAN halt mode 1: In CAN halt mode.	R
b10	SLPST	CAN Sleep Status Flag	0: Not in CAN sleep mode 1: In CAN sleep mode.	R
b11	EPST	Error-Passive Status Flag	0: Not in error-passive state 1: In error-passive state.	R
b12	BOST	Bus-Off Status Flag	0: Not in bus-off state 1: In bus-off state.	R

Bit	Symbol	Bit name	Description	R/W
b13	TRMST	Transmit Status Flag	0: Bus idle or reception in progress 1: Transmission in progress or in bus-off state.	R
b14	RECST	Receive Status Flag	0: Bus idle or transmission in progress 1: Reception in progress.	R
b15	—	Reserved	This bit is read as 0	R

NDST flag (NEWDATA Status Flag)

The NDST flag is set to 1 when at least one NEWDATA flag in MCTL_RXj (j = 0 to 31) registers is 1, regardless of the value of MIER or MIER_FIFO. The NDST flag is set to 0 when all NEWDATA flags are 0.

SDST flag (SENTDATA Status Flag)

The SDST flag is set to 1 when at least one SENTDATA flag in MCTL_TXj (j = 0 to 31) registers is 1, regardless of the value of MIER or MIER_FIFO. The SDST flag is set to 0 when all SENTDATA flags are 0.

RFST flag (Receive FIFO Status Flag)

The RFST flag is set to 1 when the receive FIFO is not empty. The RFST flag is set to 0 when the receive FIFO is empty or normal mailbox mode is selected.

TFST flag (Transmit FIFO Status Flag)

The TFST flag is set to 1 when the transmit FIFO is not full. The TFST flag is set to 0 when the transmit FIFO is full or normal mailbox mode is selected.

NMLST flag (Normal Mailbox Message Lost Status Flag)

The NMLST flag is set to 1 when at least one MSGLOST flag in MCTL_RXj (j = 0 to 31) registers is 1, regardless of the value of MIER or MIER_FIFO. The NMLST is set to 0 when all MSGLOST flags are 0.

FMLST flag (FIFO Mailbox Message Lost Status Flag)

The FMLST flag is set to 1 when the RFMLF flag in RFCR is 1, regardless of the value of MIER_FIFO. The FMLST flag is set to 0 when the RFMLF flag is 0.

TABST flag (Transmission Abort Status Flag)

The TABST flag is set to 1 when at least one TRMABT flag in MCTL_TXj (j = 0 to 31) registers is 1, regardless of the value of MIER or MIER_FIFO. The TABST flag is set to 0 when all TRMABT flags are 0.

EST flag (Error Status Flag)

The EST flag is set to 1 when at least one error is detected by EIFR, regardless of the value of EIER. The EST flag is set to 0 when no error is detected by EIFR.

RSTST flag (CAN Reset Status Flag)

The RSTST flag is set to 1 when the CAN module is in CAN reset mode. The RSTST flag is 0 when the CAN module is not in CAN reset mode. Even when the state changes from CAN reset mode to CAN sleep mode, the flag remains 1.

HLTST flag (CAN Halt Status Flag)

The HLTST flag is set to 1 when the CAN module is in CAN halt mode. The HLTST flag is set to 0 when the CAN module is not in CAN halt mode. Even when the state changes from CAN halt mode to CAN sleep mode, the flag remains 1.

SLPST flag (CAN Sleep Status Flag)

The SLPST flag is set to 1 when the CAN module is in CAN sleep mode. The SLPST flag is set to 0 when the CAN module is not in CAN sleep mode.

EPST flag (Error-Passive Status Flag)

The EPST flag is set to 1 when the value of TECR or RECR exceeds 127 and the CAN module is in an error-passive state ($128 \leq TEC < 256$ or $128 \leq REC < 256$). The EPST flag is set to 0 when the CAN module is not in the error-passive state.

BOST flag (Bus-Off Status Flag)

The BOST flag is set to 1 when the value in TECR exceeds 255 and the CAN module is in the bus-off state (TEC ≥ 256). The BOST flag is set to 0 when the CAN module is not in the bus-off state.

TRMST flag (Transmit Status Flag)

The TRMST flag is set to 1 when the CAN module performs as a transmitter node or is in the bus-off state. The TRMST flag is set to 0 when the CAN module performs as a receiver node or is in the bus-idle state.

RECST flag (Receive Status Flag)

The RECST flag is set to 1 when the CAN module performs as a receiver node. The RECST flag is set to 0 when the CAN module performs as a transmitter node or is in the bus-idle state.

30.2.16 Mailbox Search Mode Register (MSMR)

Address(es): CAN0.MSMR 4005 0853h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MBSM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	MBSM[1:0]	Mailbox Search Mode Select	b1 b0 0 0: Receive mailbox search mode 0 1: Transmit mailbox search mode 1 0: Message lost search mode 1 1: Channel search mode.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Write to the MSMR register in CAN operation mode or halt mode.

MBSM[1:0] bits (Mailbox Search Mode Select)

The MBSM[1:0] bits select the search mode for the mailbox search function.

When the MBSM[1:0] bits are 00b, receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA flag in MCTL_RXj (j = 0 to 31) registers for the normal mailbox, and the RFEST flag in RFCR.

When the MBSM[1:0] bits are 01b, transmit mailbox search mode is selected. In this mode, the search target is the SENTDATA flag in MCTL_TXj.

When the MBSM[1:0] bits are 10b, message lost search mode is selected. In this mode, the search targets are the MSGLOST flag in MCTL_RXj for the normal mailbox, and the RFMLF flag in RFCR.

When the MBSM[1:0] bits are 11b, channel search mode is selected. In this mode, the search target is CSSR. See section 30.2.18, Channel Search Support Register (CSSR).

30.2.17 Mailbox Search Status Register (MSSR)

Address(es): CAN0.MSSR 4005 0852h

	b7	b6	b5	b4	b3	b2	b1	b0
	SEST	—	—	MBNST[4:0]				
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	MBNST[4:0]	Search Result Mailbox Number Status	These bits output the smallest mailbox number that is found in each search mode selected in the MSMR register	R
b6, b5	—	Reserved	These bits are read as 0	R
b7	SEST	Search Result Status	0: Search result found 1: No search result.	R

MBNST[4:0] bits (Search Result Mailbox Number Status)

In all mailbox search modes, the MBNST[4:0] bits output the smallest mailbox number. In receive mailbox search mode, transmit mailbox search mode, and message lost search mode, the value of the mailbox (the search result to be output) is updated under the following conditions:

- When the associated NEWDATA, SENTDATA, or MSGLOST flag is set to 0 for a mailbox output by MBNST[4:0]
- When the associated NEWDATA, SENTDATA, or MSGLOST flag is set to 1 for a mailbox with a smaller number than that in MBNST[4:0].

If the MBSM[1:0] bits are set to 00b (receive mailbox search mode) or 10b (message lost search mode), the receive FIFO (mailbox 28) is output when it is not empty and there are no unread received messages and no lost messages in any of the normal mailboxes 0 to 23. If the MBSM[1:0] bits are set to 01b (transmit mailbox search mode), the transmit FIFO (mailbox 24) is not output. Table 30.6 lists the behavior of the MBNST[4:0] bits in FIFO mailbox mode.

In channel search mode, the MBNST[4:0] bits output the associated channel number. After MSSR is read by software, the next target channel number is output.

SEST bit (Search Result Status)

The SEST bit is set to 1 (no search result) when no associated mailbox is found after searching all mailboxes. For example, in transmit mailbox search mode, the SEST bit is set to 1 when no SENTDATA flag is 1 for any mailbox. The SEST bit is set to 0 when at least one SENTDATA flag is 1. When the SEST bit is 1, the value of the MBNST[4:0] bits is undefined.

Table 30.6 Behavior of MBNST[4:0] bits in FIFO mailbox mode

MBSM[1:0] bits	Mailbox 24 (transmit FIFO)	Mailbox 28 (receive FIFO)
00b	Mailbox 24 is not output	Mailbox 28 is output when no MCTL_RXj.NEWDATA flag for the normal mailboxes is set to 1 (new message is being stored or was stored in the mailbox) and the receive FIFO is not empty
01b		Mailbox 28 is not output
10b		Mailbox 28 is output when no MCTL_RXj.MSGLOST flag for the normal mailboxes is set to 1 (message is overwritten or overrun) and the RFCR.RFMLF flag is set to 1 (receive FIFO message lost) in the receive FIFO
11b		Mailbox 28 is not output

30.2.18 Channel Search Support Register (CSSR)

Address(es): CAN0.CSSR 4005 0851h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	When the value for the channel search is input, the channel number is output to MSSR	R/W

The bits that are set to 1 in the CSSR are encoded by an 8/3 encoder (the LSB position has the higher priority) and output to the MBNST[4:0] bits in MSSR. The MSSR register outputs the updated value whenever it is read by software.

Write to CSSR only when the MSMR.MBSM[1:0] bits are 11b (channel search mode). Write to CSSR in CAN operation mode or CAN halt mode.

Figure 30.4 shows the write and read operations of the CSSR and MSSR registers.

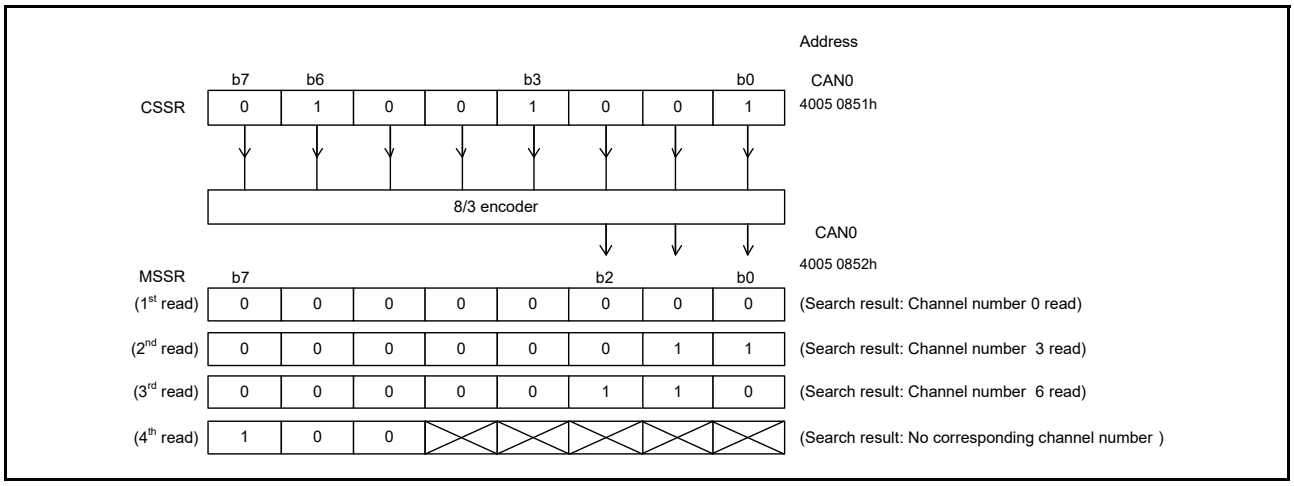


Figure 30.4 Write and read operations of the CSSR and MSSR registers

The value of CSSR is also updated whenever MSSR is read. On this read, the value prior to conversion by the 8/3 encoder can be read.

30.2.19 Acceptance Filter Support Register (AFSR)

Address(es): CAN0.AFSR 4005 0856h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b15 to b0	After the standard ID of a received message is written, the value converted for data table search can be read	R/W

Note: Write to AFSR in CAN operation mode or halt mode.

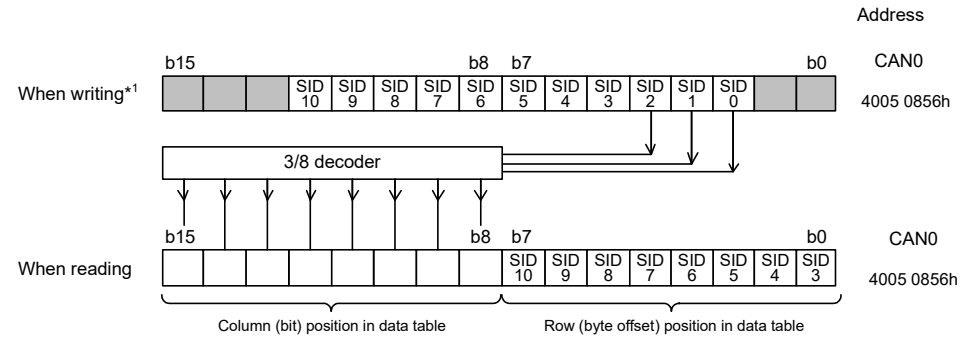
The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) searches. In the data table, all standard IDs that are created are set as valid or invalid in bit units. When AFSR is written with data in 16-bit units including the SID[10:0] bits in MBj_ID (j = 0 to 31), in which a received standard ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.

The ASU is enabled in the following cases:

- When the ID to be received cannot be masked by the acceptance filter.
  For example, if the IDs to be received are 078h, 087h, and 111h.
- When there are too many IDs to receive, and the software filtering time is expected to be shortened.

Note: The AFSR register cannot be set in CAN reset mode.

Figure 30.5 shows the write and read operations in the AFSR register.



Note 1. Write the same value as the 16-bit unit data, including the SID[10:0] bits in MBj_ID (j = 0 to 31).

Figure 30.5 Write and read operations in the AFSR register

30.2.20 Error Interrupt Enable Register (EIER)

Address(es): CAN0.EIER 4005 084Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BEIE	Bus Error Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b1	EWIE	Error-Warning Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b2	EPIE	Error-Passive Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b3	BOEIE	Bus-Off Entry Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b4	BORIE	Bus-Off Recovery Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b5	ORIE	Overrun Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b6	OLIE	Overload Frame Transmit Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b7	BLIE	Bus Lock Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W

The EIER register independently enables or disables the error interrupt for each error interrupt source. Write to EIER in CAN reset mode.

BEIE bit (Bus Error Interrupt Enable)

When the BEIE bit is 0, no error interrupt request occurs even if the BEIF flag in EIFR is 1. When the BEIE bit is 1, an error interrupt request occurs if the BEIF flag is set to 1.

EWIE bit (Error-Warning Interrupt Enable)

When the EWIE bit is 0, no error interrupt request occurs even if the EWIF flag in EIFR is 1. When the EWIE bit is 1, an error interrupt request is generated if the EWIF flag is set to 1.

EPIE bit (Error-Passive Interrupt Enable)

When the EPIE bit is 0, no error interrupt request occurs even if the EPIF flag in EIFR is 1. When the EPIE bit is 1, an error interrupt request occurs if the EPIF flag is set to 1.

BOEIE bit (Bus-Off Entry Interrupt Enable)

When the BOEIE bit is 0, no error interrupt request occurs even if the BOEIF flag in EIFR is 1. When the BOEIE bit is 1, an error interrupt request occurs if the BOEIF flag is set to 1.

BORIE bit (Bus-Off Recovery Interrupt Enable)

When the BORIE bit is 0, no error interrupt request occurs even if the BORIF flag in EIFR is 1. When the BORIE bit is 1, an error interrupt request occurs if the BORIF flag is set to 1.

ORIE bit (Overrun Interrupt Enable)

When the ORIE bit is 0, no error interrupt request occurs even if the ORIF flag in EIFR is 1. When the ORIE bit is 1, an error interrupt request occurs if the ORIF flag is set to 1.

OLIE bit (Overload Frame Transmit Interrupt Enable)

When the OLIE bit is 0, no error interrupt request occurs even if the OLIF flag in EIFR is 1. When the OLIE bit is 1, an error interrupt request occurs if the OLIF flag is set to 1.

BLIE bit (Bus Lock Interrupt Enable)

When the BLIE bit is 0, no error interrupt request occurs even if the BLIF flag in EIFR is 1. When the BLIE bit is 1, an error interrupt request occurs if the BLIF flag is set to 1.

30.2.21 Error Interrupt Factor Judge Register (EIFR)

Address(es): CAN0.EIFR 4005 084Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BEIF	Bus Error Detect Flag	0: No bus error detected 1: Bus error detected.	R/W
b1	EWIF	Error-Warning Detect Flag	0: No error-warning detected 1: Error-warning detected.	R/W
b2	EPIF	Error-Passive Detect Flag	0: No error-passive detected 1: Error-passive detected.	R/W
b3	BOEIF	Bus-Off Entry Detect Flag	0: No bus-off entry detected 1: Bus-off entry detected.	R/W
b4	BORIF	Bus-Off Recovery Detect Flag	0: No bus-off recovery detected 1: Bus-off recovery detected.	R/W

Bit	Symbol	Bit name	Description	R/W
b5	ORIF	Receive Overrun Detect Flag	0: No receive overrun detected 1: Receive overrun detected.	R/W
b6	OLIF	Overload Frame Transmission Detect Flag	0: No overload frame transmission detected 1: Overload frame transmission detected.	R/W
b7	BLIF	Bus Lock Detect Flag	0: No bus lock detected 1: Bus lock detected.	R/W

If an event associated with an EIFR flag occurs, the associated bit in EIFR is set to 1, regardless of the setting of EIER.

Clear the bits to 0 through a software write. If a bit is set to 1 at the same time that software clears it, the bit becomes 1. When setting a single bit to 0 in software, use the transfer instruction (MOV) to ensure that only the specified bit is set to 0 and the other bits are set to 1. Writing 1 has no effect to these bit values.

BEIF flag (Bus Error Detect Flag)

The BEIF flag is set to 1 when a bus error is detected.

EWIF flag (Error-Warning Detect Flag)

The EWIF flag is set to 1 when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95. This flag is set to 1 only when the REC or TEC value initially exceeds 95. If software writes 0 to this flag while the REC or TEC value remains greater than 95, the EWIF flag is not set to 1 until the REC or TEC value goes below 95, and then exceeds 95 again.

EPIF flag (Error-Passive Detect Flag)

The EPIF flag is set to 1 when the CAN error state becomes error-passive, while the REC or TEC value exceeds 127. This flag is set to 1 only when the REC or TEC value initially exceeds 127. If software writes 0 to this flag while REC or TEC remains greater than 127, the EPIF flag is not set to 1 until REC or TEC goes below 127, and then exceeds 127 again.

BOEIF flag (Bus-Off Entry Detect Flag)

The BOEIF flag is set to 1 when the CAN error state becomes bus-off, while the TEC value exceeds 255. This flag is also set to 1 when the BOM[1:0] bits in CTLR are 01b (automatic entry to CAN halt mode on bus-off entry) and the CAN module enters the bus-off state.

BORIF flag (Bus-Off Recovery Detect Flag)

The BORIF flag is set to 1 when the CAN module recovers from the bus-off state normally by detecting 11 consecutive recessive bits 128 times in the following conditions:

- When the BOM[1:0] bits in CTLR are 00b
- When the BOM[1:0] bits in CTLR are 10b
- When the BOM[1:0] bits in CTLR are 11b.

The BORIF flag is not set to 1 if the CAN module recovers from the bus-off state in the following conditions:

- When the CANM[1:0] bits in CTLR are set to 01b or 11b (CAN reset mode)
- When the RBOC bit in CTLR is set to 1 (forced return from bus-off)
- When the BOM[1:0] bits in CTLR are set to 01b
- When the BOM[1:0] bits in CTLR are set to 11b and the CANM[1:0] bits in CTLR are set to 10b (CAN halt mode) before normal recovery occurs.

Table 30.7 lists the behavior of the BOEIF and BORIF flags for each CTLR.BOM[1:0] bit setting.

Table 30.7 Behavior of BOEIF and BORIF flags for each CTLR.BOM[1:0] setting

BOM[1:0] bits	BOEIF flag	BORIF flag
00b	Set to 1 on entry to the bus-off state	Set to 1 on exit from the bus-off state
01b		Do not set to 1
10b		Set to 1 on exit from the bus-off state
11b		Set to 1 if normal bus-off recovery occurs before the CANM[1:0] bits are set to 10b (CAN halt mode)

ORIF flag (Receive Overrun Detect Flag)

The ORIF flag is set to 1 when a receive overrun occurs. This flag is not set to 1 in overwrite mode. In overwrite mode, a reception complete interrupt request occurs if an overwrite condition occurs and the ORIF flag is not set to 1.

In overrun mode with normal mailbox mode, if an overrun occurs in any of mailboxes 0 to 31, the ORIF flag is set to 1. In overrun mode with FIFO mailbox mode, if an overrun occurs in any of mailboxes 0 to 23 or the receive FIFO, this flag is set to 1.

OLIF flag (Overload Frame Transmission Detect Flag)

The OLIF flag is set to 1 if the transmitting condition of an overload frame is detected when the CAN module is transmitting or receiving.

BLIF flag (Bus Lock Detect Flag)

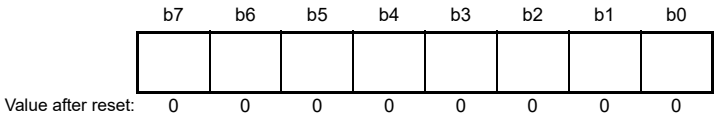
The BLIF flag is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.

After the BLIF flag is set to 1, 32 consecutive dominant bits are detected again in either of the following conditions:

- Recessive bits are detected after the BLIF flag changes to 0 from 1
- The CAN module enters CAN reset or halt mode and then enters CAN operation mode again, after the BLIF flag changes to 0 from 1.

30.2.22 Receive Error Count Register (RECR)

Address(es): CAN0.RECR 4005 084Eh



Bit	Description	R/W
b7 to b0	Receive error count function. RECR increments or decrements the counter value based on the error status of the CAN module during reception.	R

The RECR register indicates the value of the receive error counter. See the CAN specification (ISO11898-1) for the increment and decrement conditions of the receive error counter. The value of RECR in the bus-off state is undefined.

30.2.23 Transmit Error Count Register (TECR)

Address(es): CAN0.TECR 4005 084Fh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	Transmit error count function. TECR increments or decrements the counter value based on the error status of the CAN module during transmission.	R

The TECR register indicates the value of the transmit error counter. See the CAN specification (ISO11898-1) for the increment and decrement conditions of the transmit error counter. The value of TECR in the bus-off state is undefined.

30.2.24 Error Code Store Register (ECSR)

Address(es): CAN0.ECSR 4005 0850h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SEF	Stuff Error Flag*1,*2	0: No stuff error detected 1: Stuff error detected.	R/W
b1	FEF	Form Error Flag*1,*2	0: No form error detected 1: Form error detected.	R/W
b2	AEF	ACK Error Flag*1,*2	0: No ACK error detected 1: ACK error detected.	R/W
b3	CEF	CRC Error Flag*1,*2	0: No CRC error detected 1: CRC error detected.	R/W
b4	BE1F	Bit Error (recessive) Flag*1,*2	0: No bit error (recessive) detected 1: Bit error (recessive) detected.	R/W
b5	BE0F	Bit Error (dominant) Flag*1,*2	0: No bit error (dominant) detected 1: Bit error (dominant) detected.	R/W
b6	ADEF	ACK Delimiter Error Flag*1,*2	0: No ACK delimiter error detected 1: ACK delimiter error detected.	R/W
b7	EDPM	Error Display Mode Select*3,*4	0: Output first detected error code 1: Output accumulated error code.	R/W

Note 1. Writing 1 has no effect on these bit values.
Note 2. To write 0 to the SEF, FEF, AEF, CEF, BE1F, BE0F, and ADEF bits, use the transfer (MOV) instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
Note 3. Write to the EDPM bit in CAN reset mode or halt mode.
Note 4. If more than one error condition is detected simultaneously, all the related bits are set to 1.

ECSR indicates whether an error occurred on the CAN bus. See the CAN specification (ISO11898-1) for the conditions when each error occurs.

Clear all of the bits, except for EDPM, to 0 through a software write. If the ECSR bit is set to 1 by the CAN module at that same time that software writes 0 to it, the bit is set to 1.

SEF flag (Stuff Error Flag*1,*2)

The SEF flag is set to 1 when a stuff error is detected.

FEF flag (Form Error Flag*1,*2)

The FEF flag is set to 1 when a form error is detected.

AEF flag (ACK Error Flag*1,*2)

The AEF flag is set to 1 when an ACK error is detected.

CEF flag (CRC Error Flag*1,*2)

The CEF flag is set to 1 when a CRC error is detected.

BE1F flag (Bit Error (recessive) Flag*1,*2)

The BE1F flag is set to 1 when a recessive bit error is detected.

BE0F flag (Bit Error (dominant) Flag*1,*2)

The BE0F flag is set to 1 when a dominant bit error is detected.

ADEF flag (ACK Delimiter Error Flag*1,*2)

The ADEF flag is set to 1 when a form error is detected with the ACK delimiter during transmission.

EDPM bit (Error Display Mode Select*3,*4)

The EDPM bit selects the output mode of ECSR. When the EDPM bit is set to 0, ECSR outputs the first error code. When the EDPM bit is set to 1, ECSR outputs the accumulated error code.

30.2.25 Time Stamp Register (TSR)

Address(es): CAN0.TSR 4005 0854h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	R/W
b15 to b0	Free-running counter value for the time stamp function	R

Note: Read TSR in 16-bit units.

Reading the TSR register returns the current value of the 16-bit free-running time stamp counter. The time stamp counter reference clock is configured in the TSPS[1:0] bits in CTLR. The counter stops in CAN sleep mode and CAN halt mode, and is initialized in CAN reset mode. The time stamp counter value is stored in the TSL[7:0] and TSH[7:0] bits in the MBj_TS register when a received message is stored in a receive mailbox.

30.2.26 Test Control Register (TCR)

Address(es): CAN0.TCR 4005 0858h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TSTM[1:0]		TSTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSTE	CAN Test Mode Enable	0: CAN test mode disabled 1: CAN test mode enabled.	R/W
b2, b1	TSTM[1:0]	CAN Test Mode Select	b2 b1 0 0: Not CAN test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (external loopback) 1 1: Self-test mode 1 (internal loopback).	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TCR controls the CAN test mode. Write to TCR in CAN halt mode only.

(1) Listen-only mode

The CAN specification (ISO11898-1) recommends an optional bus monitoring mode. In listen-only mode, valid data frames and valid remote frames can be received. However, only recessive bits can be sent on the CAN bus. The ACK bit, overload flag, and active error flag cannot be sent. Listen-only mode can be used for baud rate detection. Do not request transmission from any mailboxes in listen-only mode.

Figure 30.6 shows the connection when listen-only mode is selected.

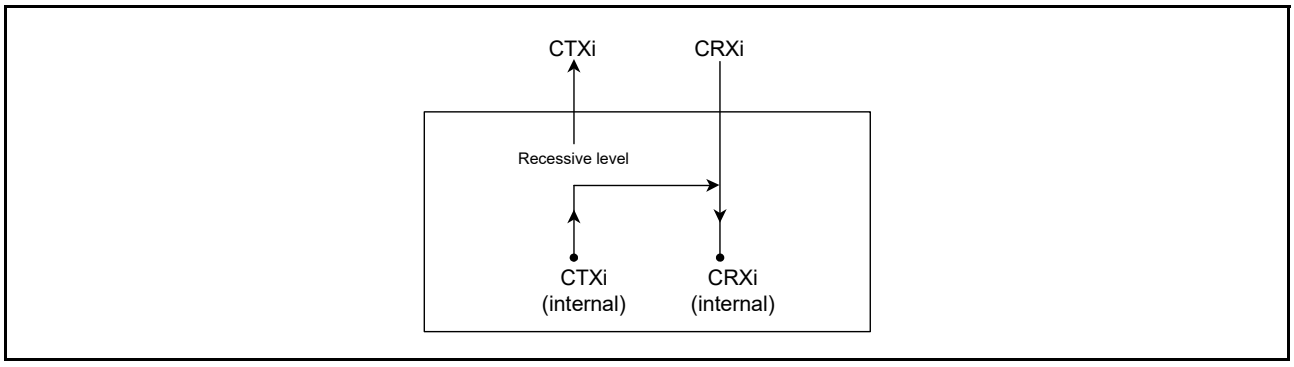


Figure 30.6 Connection when listen-only mode is selected (i = 0)

(2) Self-test mode 0 (external loopback)

Self-test mode 0 is provided for CAN transceiver tests. In this mode, the protocol module treats its own transmitted messages as those received by the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol module generates the ACK bit. Connect the CTXi and CRXi pins to the transceiver.

Figure 30.7 shows the connection when self-test mode 0 is selected.

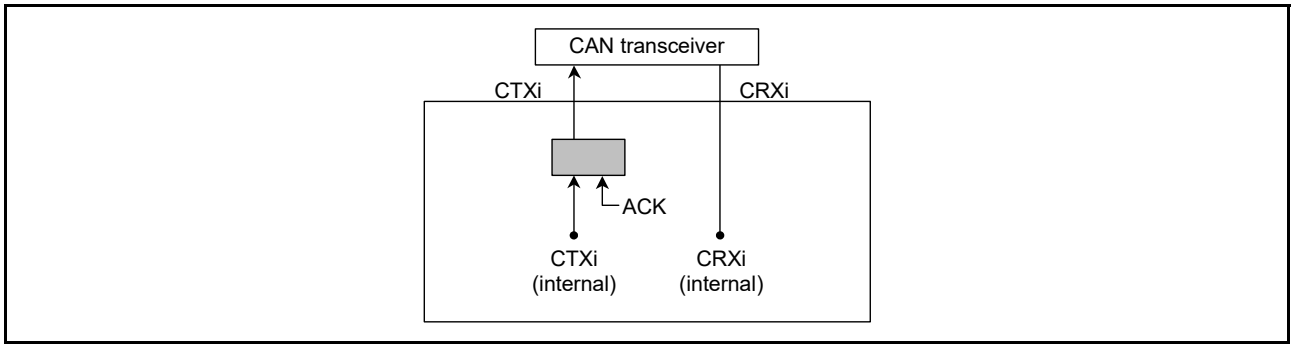


Figure 30.7 Connection when self-test mode 0 is selected (i = 0)

(3) Self-test mode 1 (internal loopback)

Self-test mode 1 is provided for self-test functions. In this mode, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

In self-test mode 1, the protocol controller performs an internal feedback from the internal CTXi pin to the internal CRXi pin. The input value of the external CRXi pin is ignored. The external CTXi pin outputs only recessive bits. The CTXi and CRXi pins are not required to be connected to the CAN bus or any external device.

Figure 30.8 shows the connection when self-test mode 1 is selected.

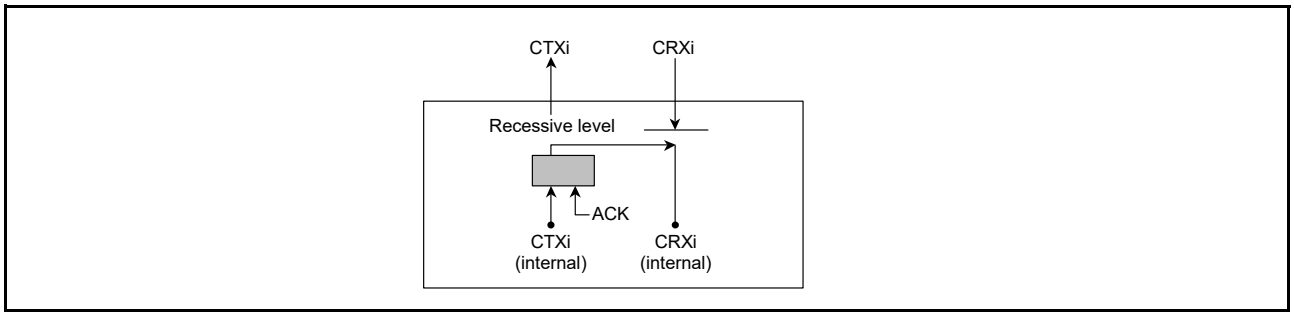


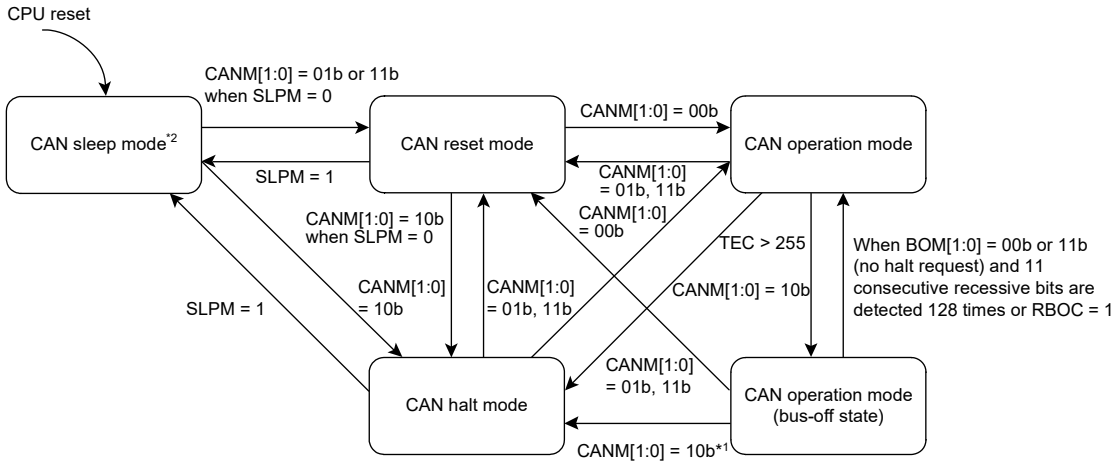
Figure 30.8 Connection when self-test mode 1 is selected (i = 0)

30.3 Operation Modes

The CAN module operation includes the following modes:

- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode.

Figure 30.9 shows the transitions between different operation modes.



CANM, SLPM, BOM, RBOC: Bits in CTLR

Note 1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the CTLR.BOM[1:0] bits.
When the CTLR.BOM[1:0] bits are 01b, the state transition occurs immediately after entering the bus-off state.
When the CTLR.BOM[1:0] bits are 10b, the state transition occurs at the end of the bus-off state.
When the CTLR.BOM[1:0] bits are 11b, the state transition occurs at the setting of the CTLR.CANM[1:0] bits to 10b (CAN halt mode).

Note 2. Change the CTLR.SLPM bit to set or cancel CAN sleep mode.

Figure 30.9 Transition between different operation modes

30.3.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration. When the CTLR.CANM[1:0] bits are set to 01b or 11b, the CAN module enters CAN reset mode. The STR.RSTST flag is then set to 1. Do not change the CTLR.CANM[1:0] bits until the RSTST flag is 1. Set the BCR register before exiting CAN reset mode to enter any other modes.

The following registers are initialized to their reset values after entering CAN reset mode, and their initial values are saved during CAN reset mode:

- MCTL_TXj and MCTL_RXj
- STR (except for the SLPST and TFST bits)
- EIFR
- RECR
- TECR
- TSR
- MSSR
- MSMR
- RFCR
- TFCR
- TCR
- ECSR (except for the EDPM bit).

The following registers retain their previous values even after entering CAN reset mode:

- CTLR
- STR (only the SLPST and TFST bits)
- MIER and MIER_FIFO

- EIER
- BCR
- CSSR
- ECSR (only the EDPM bit)
- MBj_ID, MBj_DL, MBj_Dm and MBj_TS
- MKRk
- FIDCR0 and FIDCR1
- MKIVLR
- AFSR
- RFPCR
- TFPCR.

30.3.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting. When the CTLR.CANM[1:0] bits are set to 10b, CAN halt mode is selected and the STR.HLTST bit is set to 1. Do not change the CTLR.CANM[1:0] bits until the HLTST bit is 1. See Table 30.8 for the state transition conditions when transmitting or receiving.

All registers except for the RSTST, HLTST, and SLPST bits in STR remain unchanged when the CAN enters CAN halt mode. Do not change CTLR (except for the CANM[1:0] and SLPM bits) and EIER in CAN halt mode. The BCR register can be changed in CAN halt mode only when listen-only mode is selected for automatic baud rate detection.

Table 30.8 Operation in CAN reset mode and CAN halt mode

Operation mode	Receiver	Transmitter	Bus-off
CAN reset mode (forced transition) CANM[1:0] = 11b	CAN module enters CAN reset mode without waiting for the end of message reception	CAN module enters CAN reset mode without waiting for the end of message transmission	CAN module enters CAN reset mode without waiting for the end of bus-off recovery
CAN reset mode CANM[1:0] = 01b	CAN module enters CAN reset mode without waiting for the end of message reception	CAN module enters CAN reset mode after waiting for the end of message transmission*1,*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception*2,*3	CAN module enters CAN halt mode after waiting for the end of message transmission*1,*4	• When the BOM[1:0] bits are 00b: A halt request from software is accepted only after bus-off recovery • When the BOM[1:0] bits are 01b: CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery, regardless of a halt request from software • When the BOM[1:0] bits are 10b: CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery, regardless of a halt request from software • When the BOM[1:0] bits are 11b: CAN module enters CAN halt mode without waiting for the end of bus-off recovery, if a halt is requested by software during bus-off.

BOM[1:0] bits: Bits in CTLR.

Note 1. If transmission of multiple messages is requested, a mode transition occurs on completion of the first transmission. If the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.

Note 2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF flag in EIFR.

Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module transitions to CAN halt mode.

Note 4. If a CAN bus error or arbitration-lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module transitions to the requested CAN mode.

30.3.3 CAN Sleep Mode

CAN sleep mode reduces power consumption by stopping the clock supply to the CAN module. After a reset from an MCU pin or a software reset, the CAN module starts from CAN sleep mode.

When the SLPM bit in CTLR is set to 1, the CAN module enters CAN sleep mode and the SLPST bit in STR is set to 1. Do not change the value of the SLPM bit until the SLPST bit is 1. The other registers remain unchanged when the CAN module enters CAN sleep mode.

Write to the SLPM bit in CAN reset mode and CAN halt mode. Do not change any registers (except for the SLPM bit) during CAN sleep mode. Read operation is still allowed.

When the SLPM bit is set to 0, the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

30.3.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication. When the CANM[1:0] bits in CTLR are set to 00b, the CAN module enters CAN operation mode. The RSTST and HLTST bits in STR are set to 0. Do not change the value of the CANM[1:0] bits until the RSTST and HLTST bits are 0.

If 11 consecutive recessive bits are detected after entering CAN operation mode:

- The CAN module becomes an active node on the network, which enables transmission and reception of CAN messages
- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

During CAN operation mode, the CAN module may be in one of the following three sub-modes, depending on the status of the CAN bus:

- Idle mode: No transmission or reception occurs
- Receive mode: A CAN message sent by another node is being received
- Transmit mode: A CAN message is being transmitted. The CAN module receives a message transmitted by the local node simultaneously when self-test mode 0 (TSTM[1:0] bits in TCR = 10b) or self-test mode 1 (TSTM[1:0] bits = 11b) is selected.

Figure 30.10 shows the sub-modes of CAN operation mode.

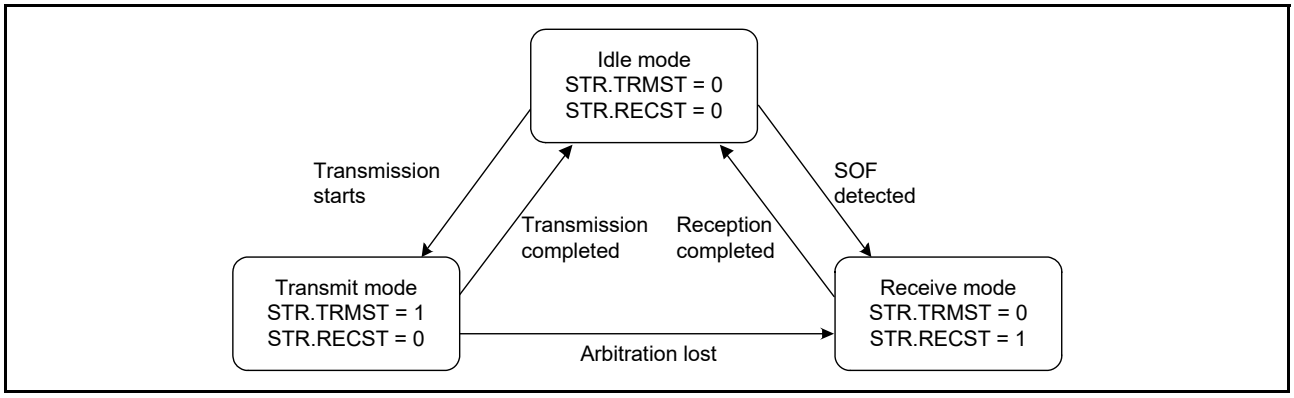


Figure 30.10 Sub-modes of CAN operation mode

30.3.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state based on the increment or decrement rules for the transmit or receive error counters, as defined in the CAN specifications.

The following cases apply when the CAN module is recovering from the bus-off state. When the CAN module is in the bus-off state, the values of the CAN module registers remain unchanged, except for those in STR, EIFR, RECR, TECR, and TSR.

(1) When CTLR.BOM[1:0] bits = 00b (normal mode)

The CAN module enters the error-active state after it completes recovery from the bus-off state and CAN communication is enabled. The BORIF flag in EIFR is set to 1 (bus-off recovery detected).

(2) When CTLR.RBOC bit = 1 (forced return from bus-off)

The CAN module enters the error-active state when it is in the bus-off state and the RBOC bit is 1. CAN communication is enabled again after 11b consecutive recessive bits are detected. The BORIF flag is not set to 1.

(3) When CTLR.BOM[1:0] bits = 01b (automatic transition to CAN halt mode on bus-off entry)

The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF flag is not set to 1.

(4) When CTLR.BOM[1:0] bits = 10b (automatic transition to CAN halt mode on bus-off end)

The CAN module enters CAN halt mode when it completes recovery from bus-off. The BORIF flag is set to 1.

(5) When CTLR.BOM[1:0] bits = 11b (automatic transition to CAN halt mode through software) and CTLR.CANM[1:0] bits = 10b (CAN halt mode) during bus-off state

The CAN module enters CAN halt mode when it is in the bus-off state and the CANM[1:0] bits are set to 10b (CAN halt mode). The BORIF flag is not set to 1. If the CANM[1:0] bits are not set to 10b during bus-off, the same behavior as (1) applies.

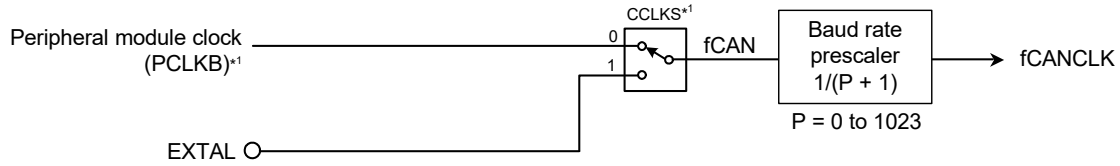
30.4 Data Transfer Rate Configuration

This section describes how to configure the data transfer rate.

30.4.1 Clock Setting

The CAN module has a CAN clock generator that can be set by the CCLKS and the BRP[9:0] bits in the BCR register.

Figure 30.11 shows a block diagram of the CAN clock generator.



CCLKS: Bit in the BCR register
fCAN: CAN system clock
P: Value selected in BRP[9:0] bits in BCR (P = 0 to 1023)
fCANCLK: CAN communication clock (fCANCLK = fCAN/(P + 1))

Note 1. See section 9, Clock Generation Circuit. When using the CAN module while the CCLKS bit is cleared to 0, PLL must be selected as the source of the peripheral module clock.

Figure 30.11 Block diagram of CAN clock generator

30.4.2 Bit Timing Setting

The bit timing consists of three segments as shown in Figure 30.12.

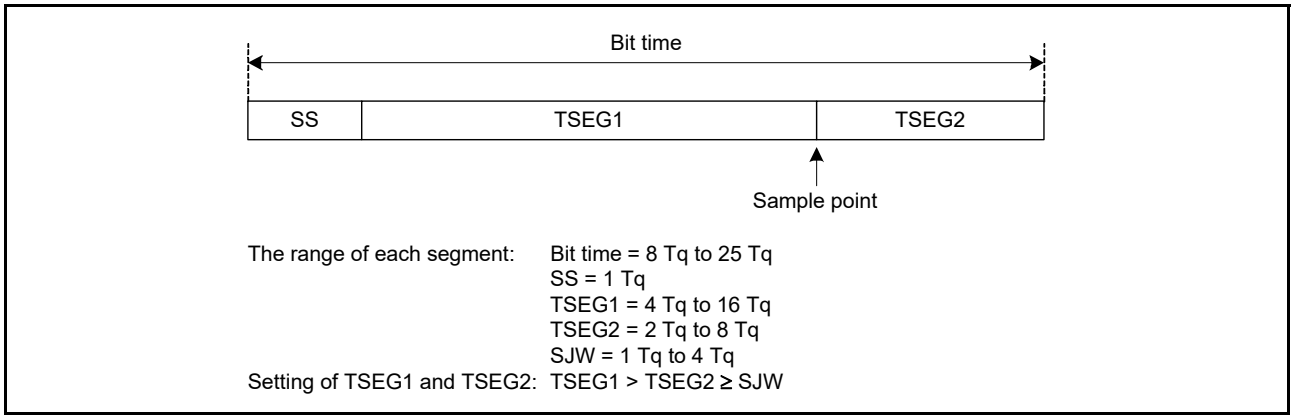


Figure 30.12 Bit timing

30.4.3 Data Transfer Rate

The data transfer rate depends on the division value of fCAN (CAN system clock), the division value of the baud rate prescaler, and the Tq count for 1 bit time.

$$\text{Data transfer rate (bps)} = \frac{\text{fCAN}}{\text{Baud rate prescaler division value}^{*1} \times \text{Tq count for 1 bit time}} = \frac{\text{fCANCLK}}{\text{Tq count for 1 bit time}}$$

Note 1. Division value of baud rate prescaler = P + 1 (P: 0 to 1023), where P is the BRP[9:0] setting in BCR.

Table 30.9 lists data transfer rate examples.

Table 30.9 Data transfer rate examples

fCAN	50 MHz		48 MHz		40 MHz		32 MHz	
Data transfer rate	**Tq count**	**P + 1**	**Tq count**	**P + 1**	**Tq count**	**P + 1**	**Tq count**	**P + 1**
1 Mbps	10 Tq 25 Tq	5 2	8 Tq 12 Tq 16 Tq	6 4 3	10 Tq 20 Tq	4 2	8 Tq 16 Tq	4 2
500 kbps	10 Tq 25 Tq	10 4	8 Tq 12 Tq 16 Tq	12 8 6	10 Tq 20 Tq	8 4	8 Tq 16 Tq	8 4
250 kbps	10 Tq 25 Tq	20 8	8 Tq 12 Tq 16 Tq	24 16 12	10 Tq 20 Tq	16 8	8 Tq 16 Tq	16 8
125 kbps	10 Tq 25 Tq	40 16	8 Tq 12 Tq 16 Tq	48 32 24	10 Tq 20 Tq	32 16	8 Tq 16 Tq	32 16
83.3 kbps	10 Tq 25 Tq	60 24	8 Tq 12 Tq 16 Tq	72 48 36	8 Tq 10 Tq 16 Tq 20 Tq	60 48 30 24	8 Tq 16 Tq	48 24
33.3 kbps	10 Tq 25 Tq	150 60	8 Tq 12 Tq 16 Tq	180 120 90	8 Tq 10 Tq 20 Tq	150 120 60	8 Tq 10 Tq 16 Tq 20 Tq	120 96 60 48

30.5 Mailbox and Mask Register Structure

Figure 30.13 shows the structure of the 32 mailbox registers MBj_ID, MBj_DL, MBj_Dm, and MBj_TS.

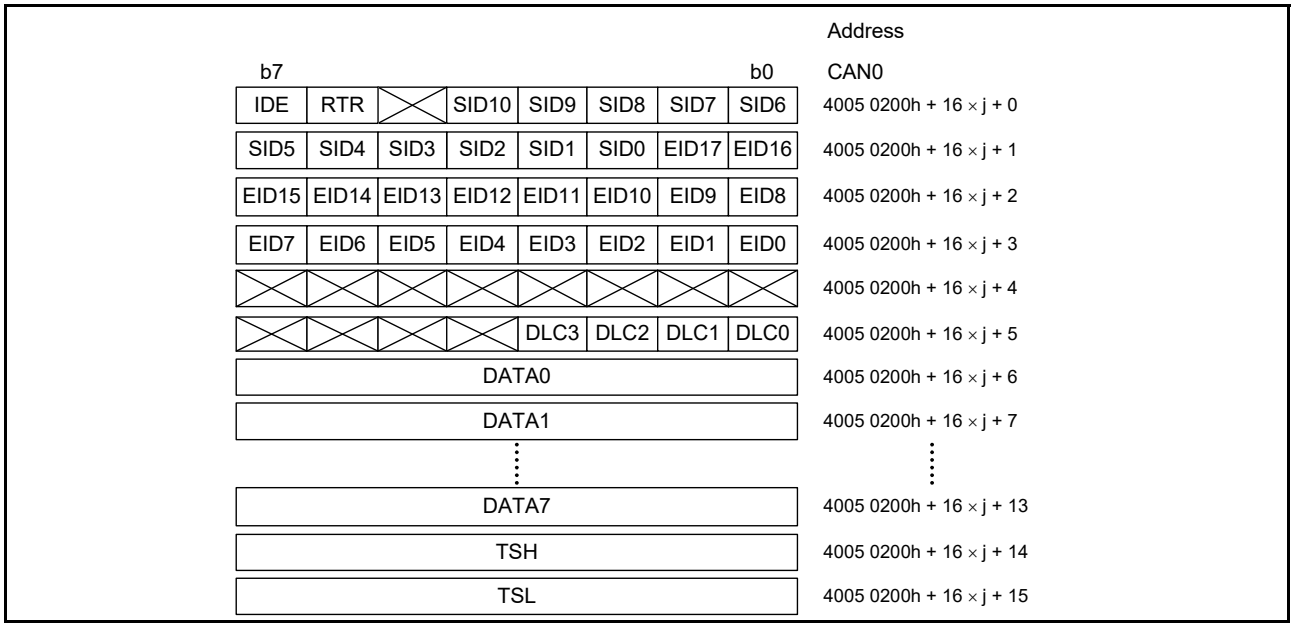


Figure 30.13 Structure of the mailbox registers (j = 0 to 31)

Figure 30.14 shows the structure of the eight mask registers MKRk.

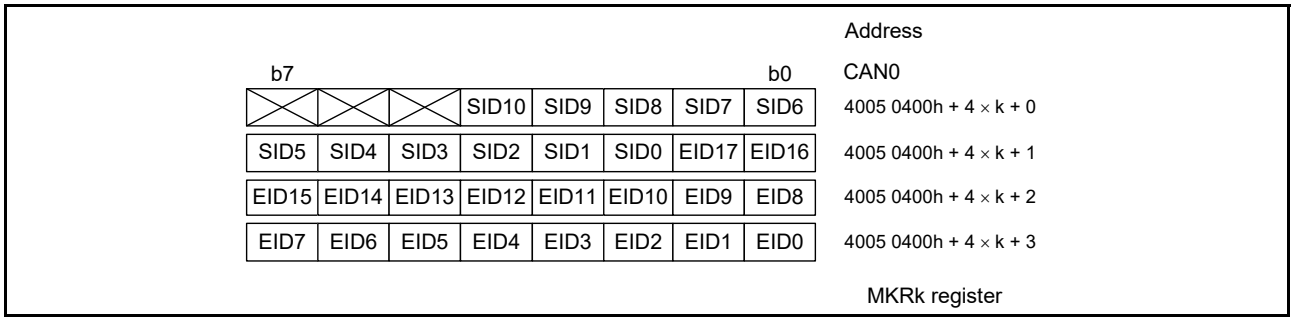


Figure 30.14 Structure of the MKRk registers (k = 0 to 7)

Figure 30.15 shows the structure of the two FIFO received ID compare registers, FIDCR0 and FIDCR1.

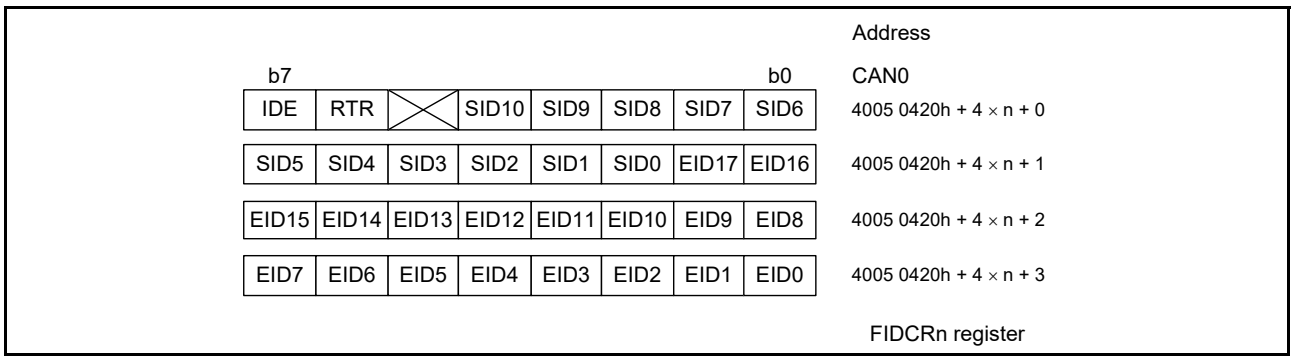


Figure 30.15 Structure of the FIDCRn registers (n = 0, 1)

30.6 Acceptance Filtering and Masking Functions

The acceptance filtering and masking functions allow you to select and receive messages with multiple IDs for mailboxes within a specified range.

The MKRk registers can mask the standard ID and the extended ID of 29 bits:

- MKR0 is the mask register for mailboxes 0 to 3
- MKR1 is the mask register for mailboxes 4 to 7
- MKR2 is the mask register for mailboxes 8 to 11
- MKR3 is the mask register for mailboxes 12 to 15
- MKR4 is the mask register for mailboxes 16 to 19
- MKR5 is the mask register for mailboxes 20 to 23
- MKR6 is the mask register for mailboxes 24 to 27 in normal mailbox mode and receive FIFO mailboxes 28 to 31 in FIFO mailbox mode
- MKR7 is the mask register for mailboxes 28 to 31 in normal mailbox mode and receive FIFO mailboxes 28 to 31 in FIFO mailbox mode.

MKIVLR disables acceptance filtering independently for each mailbox.

The IDE bit in MBj_ID register is valid when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode).

The RTR bit in MBj_ID register selects a data frame or remote frame.

In FIFO mailbox mode, normal mailboxes 0 to 23 use the associated register (MKR0 to MKR5) for acceptance filtering. The receive FIFO mailboxes 28 to 31 use two registers, MKR6 and MKR7, for acceptance filtering.

The receive FIFO uses two registers, FIDCR0 and FIDCR1, for ID comparison. The EID[17:0], SID[10:0], RTR, and IDE bits in mailbox 28 to mailbox 31 for the receive FIFO are disabled. As acceptance filtering depends on the result of two logic OR operations, two ranges of IDs can be received into the receive FIFO. The MKIVLR is disabled for the receive FIFO.

If different standard ID and extended ID values are set in the IDE bits in FIDCR0 and FIDCR1, both ID formats are received. If different data frame and remote frame values are set in the RTR bits in FIDCR0 and FIDCR1, both data and remote frames are received.

When a combination of two ranges of IDs is not required, set the same mask value and the same ID in both the FIFO ID and mask registers.

Figure 30.16 shows the associations between the mask registers and mailboxes. Figure 30.17 shows acceptance filtering.

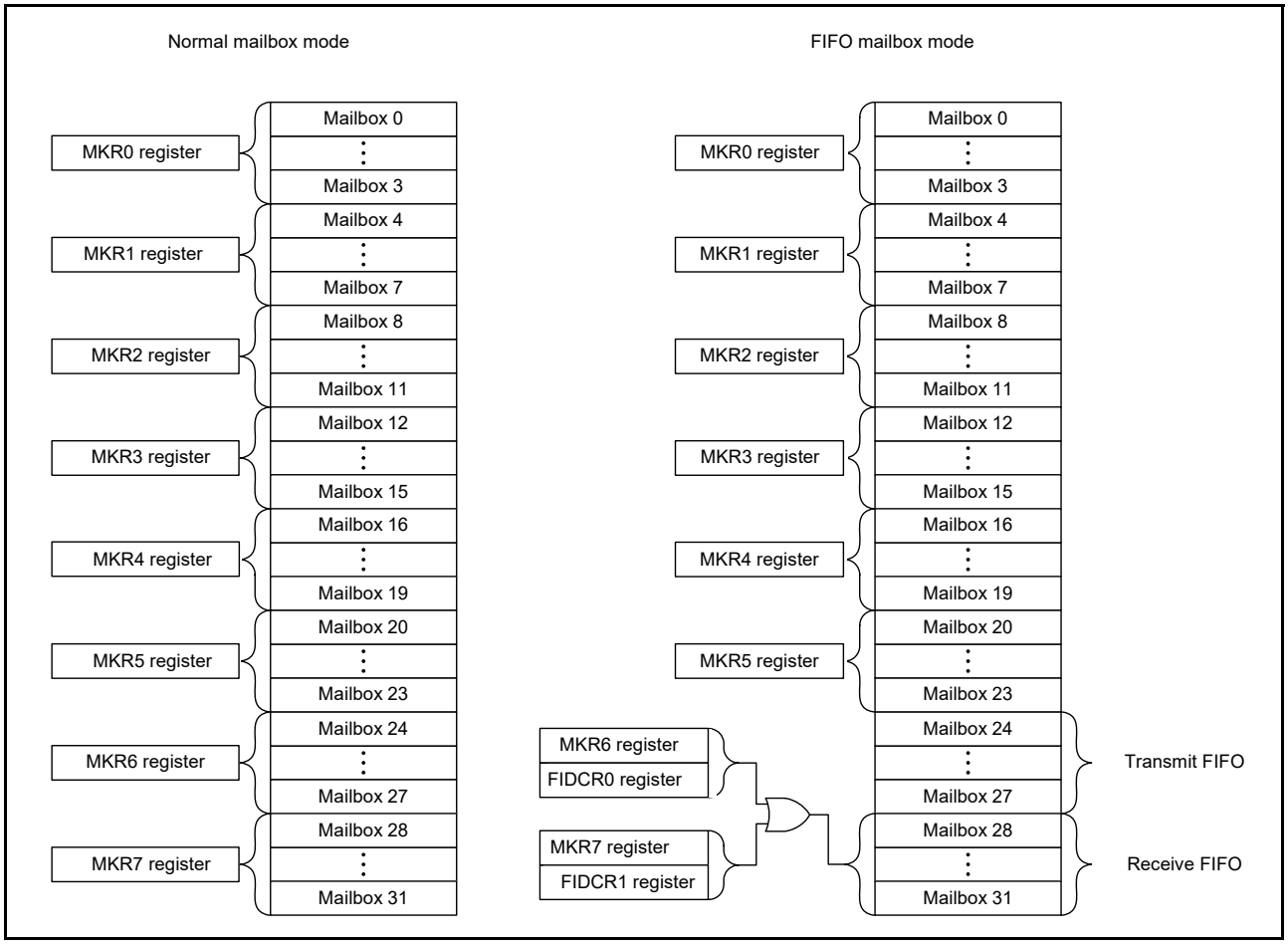
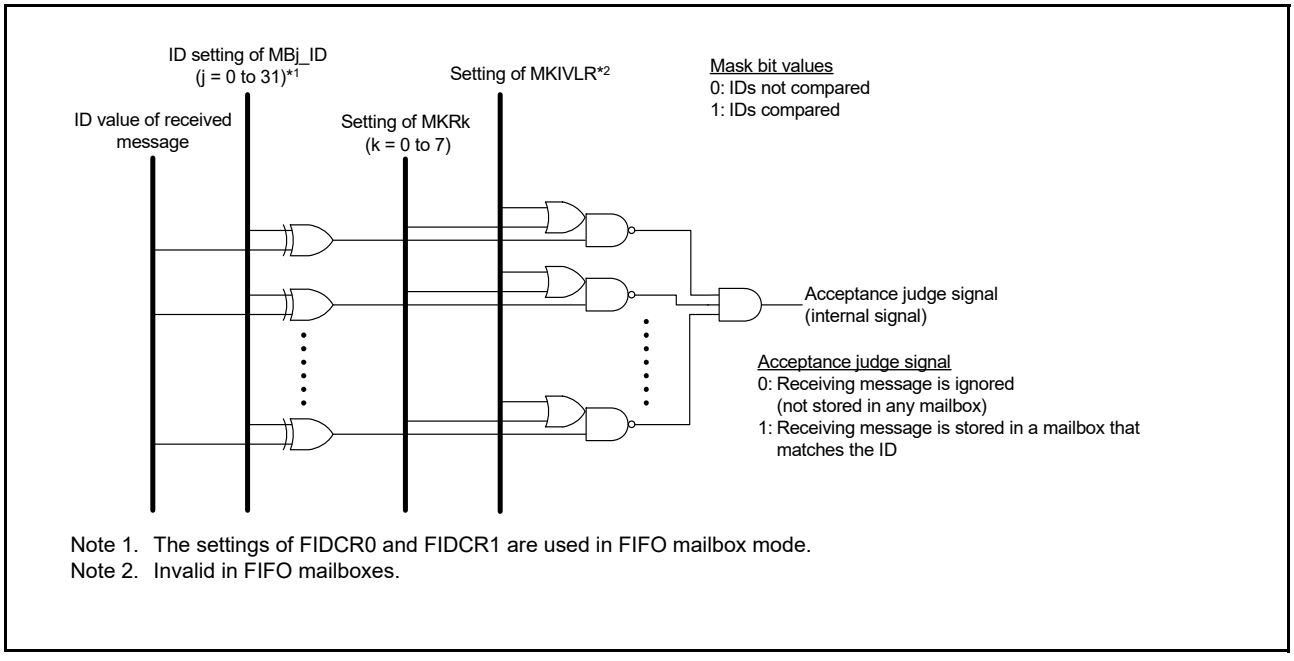


Figure 30.16 Associations between mask registers and mailboxes



Note 1. The settings of FIDCR0 and FIDCR1 are used in FIFO mailbox mode.
Note 2. Invalid in FIFO mailboxes.

Figure 30.17 Acceptance filtering

30.7 Reception and Transmission

Table 30.10 lists the CAN communication mode settings.

Table 30.10 Settings for CAN receive and transmit modes

MCTL_TXj.TRMREQ and MCTL_RXj.TRMREQ	MCTL_TXj.RECREQ and MCTL_RXj.RECREQ	MCTL_TXj.ONESHOT and MCTL_RXj.ONESHOT	Mailbox communication mode
0	0	0	Mailbox disabled or transmission aborted
0	0	1	Can be configured only when transmission or reception from a mailbox programmed in one-shot mode is aborted
0	1	0	Configured as a receive mailbox for a data frame or remote frame
0	1	1	Configured as a one-shot receive mailbox for a data frame or remote frame
1	0	0	Configured as a transmit mailbox for a data frame or remote frame
1	0	1	Configured as a one-shot transmit mailbox for a data frame or remote frame
1	1	0	Do not set
1	1	1	Do not set

j = 0 to 31

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox:

- Before configuring a mailbox, set MCTL_RXj to 00h
- A received message is stored in the first mailbox that matches the condition resulting from the receive mode settings and acceptance filtering. The matching mailbox with the smallest number takes priority for storing the received message.
- In CAN operation mode, the CAN module does not receive its own transmitted data even when the ID is a match. In self-test mode, however, the CAN module receives its own transmitted data and returns ACK.

When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox:

- Before configuring a mailbox, ensure that MCTL_TXj is 00h and that there is no pending abort process.

30.7.1 Reception

Figure 30.18 shows an operation example of data frame reception in overwrite mode.

The example shows the overwriting of the first message when the CAN module receives two consecutive CAN messages that match the receiving conditions in MCTL_RXj (j = 0 to 31).

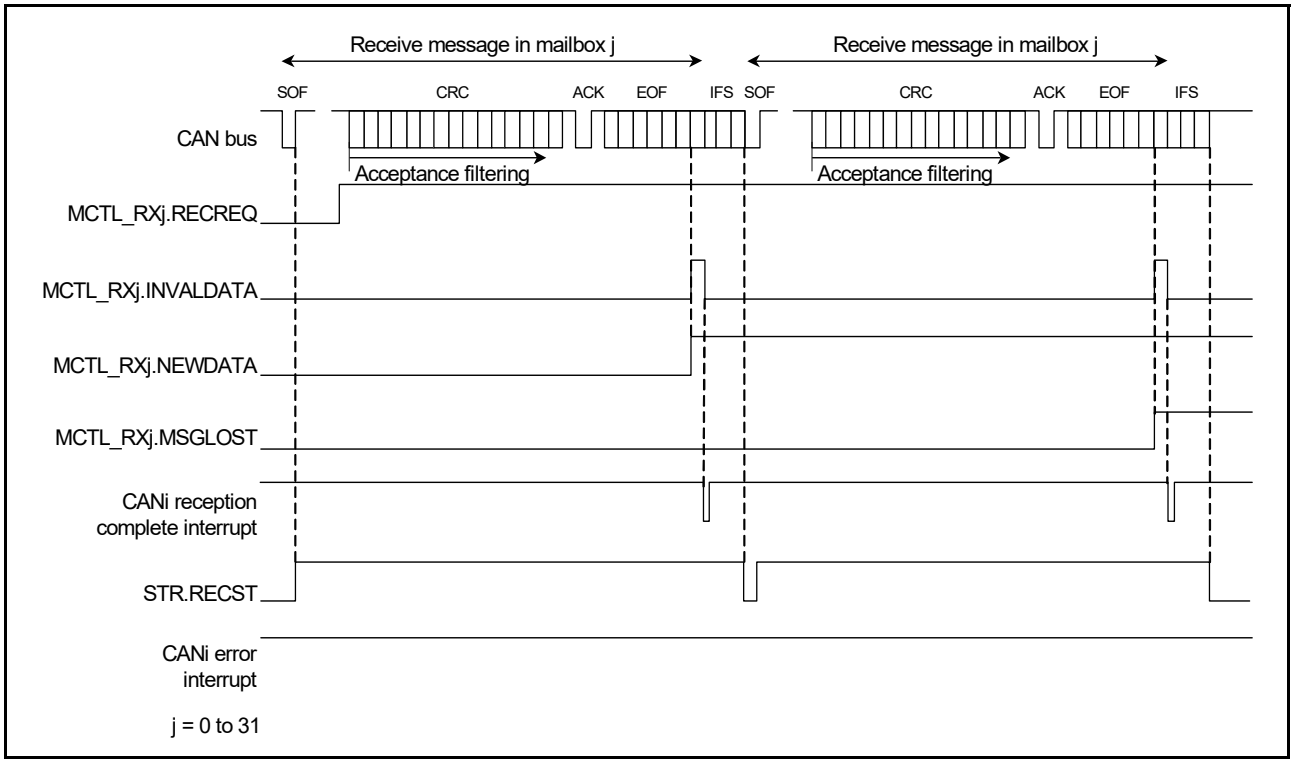


Figure 30.18 Operation example of data frame reception in overwrite mode

1. When an SOF is detected on the CAN bus, the RECST bit in STR is set to 1 (reception in progress) if the CAN module has no message ready to start transmission.
2. Acceptance filtering starts at the beginning of the CRC field to select the receive mailbox.
3. After a message is received, the NEWDATA flag in MCTL_RXj for the receive mailbox is set to 1 (new message is being stored or was stored to the mailbox). The INVALDATA flag in MCTL_RXj is set to 1 (message is updated) at the same time. The INVALDATA flag is set to 0 (message valid) again after the complete message is transferred to the mailbox.
4. When the interrupt enable bit in MIER for the receive mailbox is 1 (interrupt enabled), the INVALDATA flag is set to 0, triggering a CAN0 reception complete interrupt request.
5. After reading the message from the mailbox, the NEWDATA flag must be set to 0 by software.
6. In overwrite mode, if the next CAN message is received while the NEWDATA flag in MCTL_RXj is set to 1, the MSGLOST flag in MCTL_RXj is set to 1 (message was overwritten). The new received message is transferred to the mailbox. The CAN0 reception complete interrupt request is generated in the same as in step 4.

Figure 30.19 shows an operation example of data frame reception in overrun mode. The example shows the overrunning of the second message when the CAN module receives two consecutive CAN messages that match the receiving conditions in MCTL_RXj (j = 0 to 31).

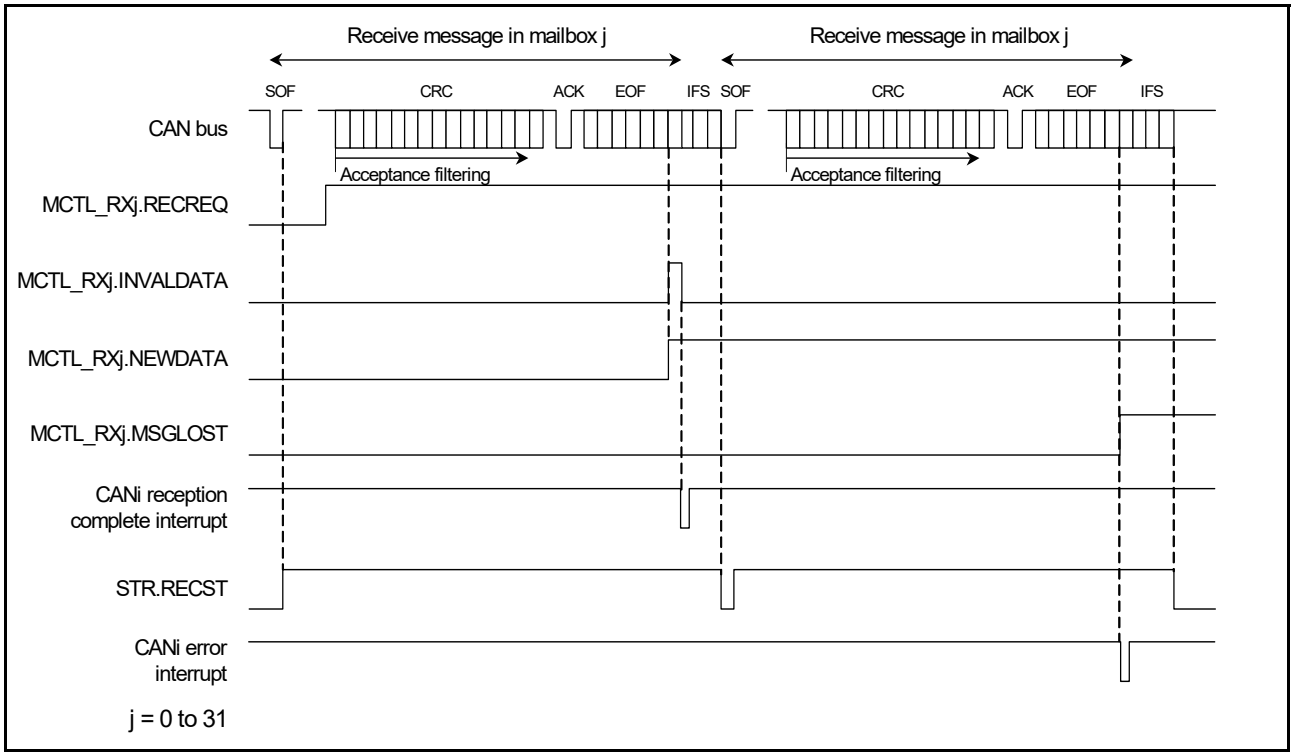


Figure 30.19 Operation example of data frame reception in overrun mode

Steps 1. to 5. are the same as in overwrite mode.

6. In overrun mode, if the next CAN message is received before the NEWDATA flag in MCTL_RXj is set to 0, the MSGLOST flag in MCTL_RXj is set to 1 (message overrun). The new received message is discarded and a CANi error interrupt request occurs if the associated interrupt enable bit in EIER is set to 1 (interrupt enabled).

30.7.2 Transmission

Figure 30.20 shows an example operation of data frame transmission.

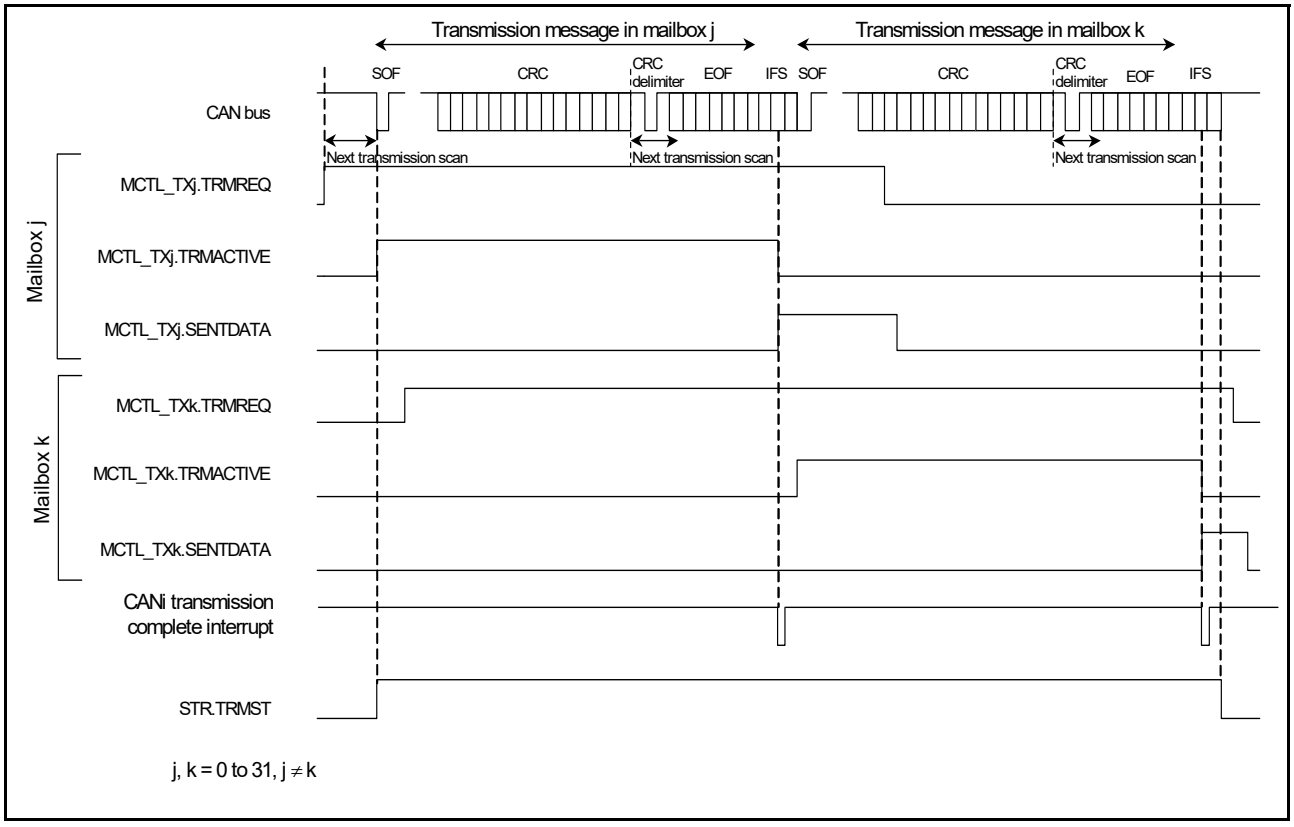


Figure 30.20 Operation example of data frame transmission

1. When a TRMREQ bit in MCTL_TXj (j = 0 to 31) is set to 1 (transmit mailbox) in the bus-idle state, mailbox scanning determines the highest-priority mailbox for transmission. When the transmit mailbox is determined, the TRMACTIVE flag in MCTL_TXj is set to 1 (from acceptance of transmission request to completion of transmission, or error/arbitration-lost), the TRMST bit in STR is set to 1 (transmission in progress), and the CAN module starts transmission.*1
2. If other TRMREQ bits are set, the transmission scanning starts with the CRC delimiter for the next transmission.
3. If transmission is complete without losing arbitration, the SENTDATA flag in MCTL_TXj is set to 1 (transmission complete) and the TRMACTIVE flag is set to 0 (transmission is pending or transmission is not requested). If the interrupt enable bit in MIER is 1 (interrupt enabled), the CANi transmission complete interrupt request is generated.
4. When requesting the next transmission from the same mailbox, set the SENTDATA flag and TRMREQ bit to 0, and then set the TRMREQ bit to 1 after checking that the SENTDATA flag and TRMREQ bit are set to 0.

Note 1. If arbitration is lost after the CAN module starts transmission, the TRMACTIVE flag is set to 0. Transmission scanning is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following arbitration-lost, transmission scanning is performed again to search for the highest-priority transmit mailbox from the start of the CRC delimiter.

30.8 Interrupts

The CAN module provides the following interrupts for each channel:

- CANi reception complete interrupt for mailboxes 0 to 31 (CANi_RXM)
- CANi transmission complete interrupt for mailboxes 0 to 31 (CANi_TXM)
- CANi receive FIFO interrupt (CANi_RXF)
- CANi transmit FIFO interrupt (CANi_TXF)
- CANi error interrupt (CANi_ERS).

Eight interrupt sources are available for the CANi error interrupts. Check the EIFR register to determine the interrupt sources:

- Bus error
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- Receive overrun
- Overload frame transmission
- Bus lock.

Table 30.11 lists the CAN interrupts.

Table 30.11 CAN interrupts

Module	Interrupt symbol	Interrupt source	Source flag
CANi i = 0	CANi_ERS	Bus lock detected	EIFR.BLIF
		Overload frame transmission detected	EIFR.OLIF
		Overrun detected	EIFR.ORIF
		Bus-off recovery detected	EIFR.BORIF
		Bus-off entry detected	EIFR.BOEIF
		Error-passive detected	EIFR.EPIF
		Error-warning detected	EIFR.EWIF
		Bus error detected	EIFR.BEIF
	CANi_RXF	Receive FIFO message received (MIER_FIFO.MB29 = 0)	RFCR.RFUST[2:0]
		Receive FIFO warning (MIER_FIFO.MB29 = 1)	
	CANi_TXF	Transmit FIFO message transmission completed (MIER_FIFO.MB25 = 0)	TFCR.TFUST[2:0]
		FIFO last message transmission completed (MIER_FIFO.MB25 = 1)	
	CANi_RXM	Mailbox 0 to 31 message received	MCTL_RX0.NEWDATA to MCTL_RX31.NEWDATA
	CANi_TXM	Mailbox 0 to 31 message transmission completed	MCTL_TX0.SENTDATA to MCTL_TX31.SENTDATA

30.9 Usage Notes

30.9.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable CAN operation. The CAN module is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

30.9.2 Settings for the Operating Clock

The settings for the operating clock can be made as follows:

- The following clock constraint must be satisfied for the CAN module when the CCLKS bit is 1:

  $fPCLKB \geq fCANMCLK$

- The source of the peripheral module clock must be PLL for the CAN module when the CCLKS bit is 0.

31. Serial Peripheral Interface (SPI)

31.1 Overview

The MCU provides two independent channels of the Serial Peripheral Interface (SPI). The SPI channels are capable of high-speed, full-duplex, synchronous serial communications with multiple processors and peripheral devices.

Table 31.1 lists the SPI specifications, and Figure 31.1 shows a block diagram.

In this section, *n* indicates A or B, and *i* indicates 0 or 1. A lower-case letter *i* in pin and signal names indicates a value from 0 to 3, and a lower-case letter *m* in SPI Command Register m (SPCMDm) indicates a value from 0 to 7.

Table 31.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	Two channels
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching.
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 128-bit transmit and receive buffers • Up to four frames transferrable in one round of transmission or reception (each frame consisting of up to 32 bits) • Byte swap operating function.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKA (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKA clock divided by 4 can be input as RSPCK (the maximum RSPCK frequency is that of PCLKA divided by 4) Width at high level: 2 PCLKA cycles Width at low level: 2 PCLKA cycles.
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • 128 bits for the transmit and receive buffers.
Error detection	• Mode fault error detection • Underrun error detection • Overrun error detection*1 • Parity error detection.
SSL control function	• Four SSL pins (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output • In multi-master mode, SSLn0 pin for input and SSLn1 to SSLn3 pins for either for output or unused • In slave mode, SSLn0 pin for input and SSLn1 to SSLn3 pins for unused • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity.
Control in master transfer	• Transfers of up to eight commands, each can be executed sequentially in looped execution • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity and phase, transfer data length, MSB- or LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • Transfers can be initiated by writing to the transmit buffer • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function.

Table 31.1 SPI specifications (2 of 2)

Parameter	Specifications
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • SPI error interrupt (mode-fault, overrun, parity error) • SPI idle interrupt (SPI idle) • Transmission-complete interrupt.
Event link function (output)	The following events can be output to the Event Link Controller (ELC): • Receive buffer full signal • Transmit buffer empty signal • Mode-fault, underrun, overrun, or parity error signal • SPI idle signal • Transmission-completed signal.
Other functions	• Switching between CMOS output and open-drain output • SPI initialization function • Loopback mode.
Module-stop function	Module-stop state can be set to reduce power consumption

Note 1. In master reception, when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped on overrun error detection.

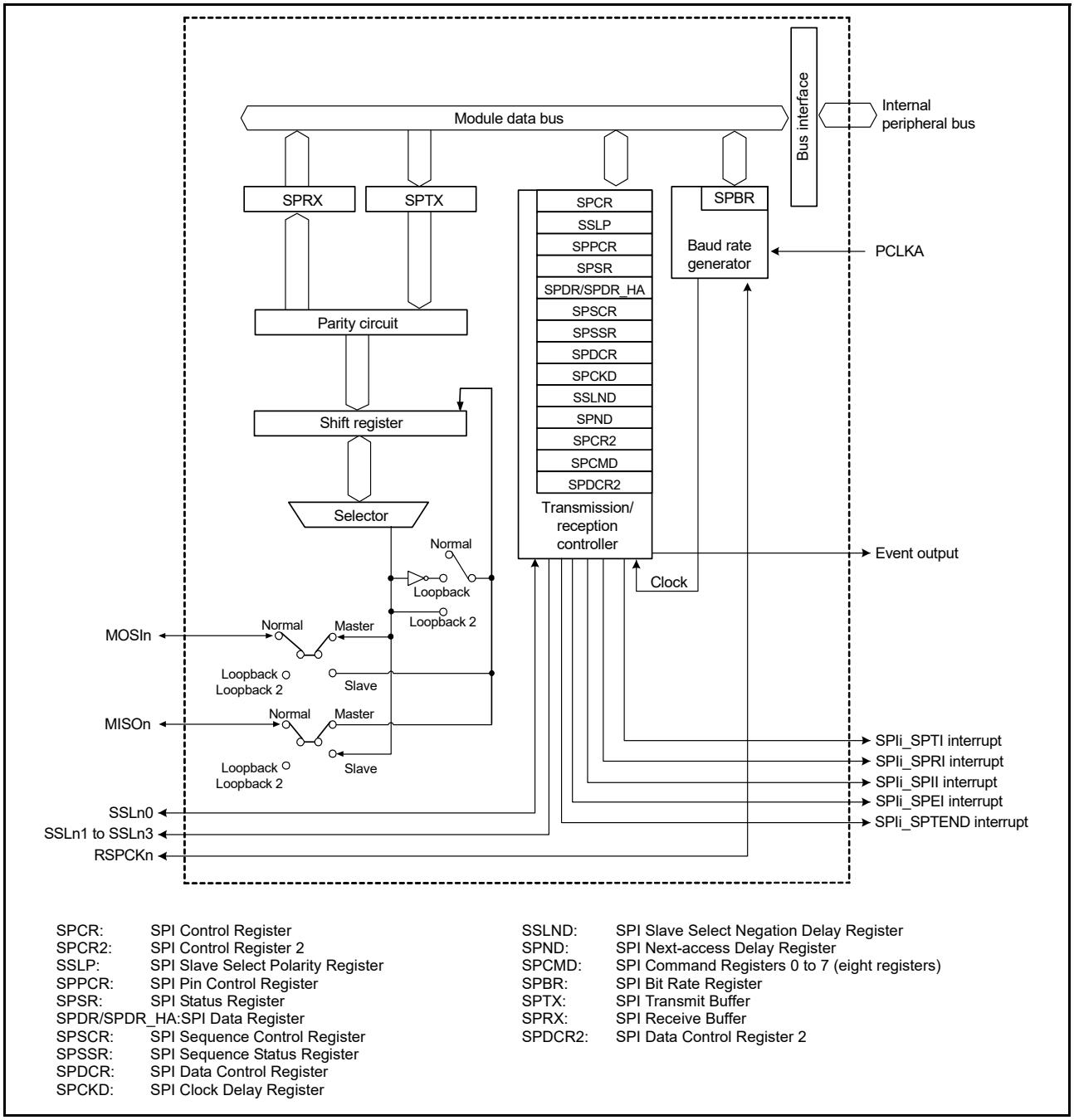


Figure 31.1 SPI block diagram

Table 31.2 lists the I/O pins used in the SPI. The SPI automatically switches the I/O direction of the SSLn0 pin. SSLn0 is an output when the SPI is a single master and an input when the SPI is a multi-master or a slave. The RSPCKn, MOSIn, and MISOn pins are automatically set as inputs or outputs based on the master or slave setting and the level input on the SSLn0 pin. For details, see section 31.3.2, Controlling the SPI Pins.

Table 31.2 SPI I/O pins

Channel	Pin name	I/O	Function
SPI0	RSPCKA	I/O	Clock input/output
	MOSIA	I/O	Master transmit data input/output
	MISOA	I/O	Slave transmit data input/output
	SSLA0	I/O	Slave selection input/output
	SSLA1	Output	Slave selection output
	SSLA2	Output	Slave selection output
	SSLA3	Output	Slave selection output
SPI1	RSPCKB	I/O	Clock input/output
	MOSIB	I/O	Master transmit data input/output
	MISOB	I/O	Slave transmit data input/output
	SSLB0	I/O	Slave selection input/output
	SSLB1	Output	Slave selection output
	SSLB2	Output	Slave selection output
	SSLB3	Output	Slave selection output

31.2 Register Descriptions

31.2.1 SPI Control Register (SPCR)

Address(es): SPI0.SPCR 4007 2000h, SPI1.SPCR 4007 2100h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPMS	SPI Mode Select	0: Select SPI operation (4-wire method) 1: Select clock synchronous operation (3-wire method).	R/W
b1	TXMD	Communications Operating Mode Select	0: Select full-duplex synchronous serial communications 1: Select serial communications with transmit-only.	R/W
b2	MODFEN	Mode Fault Error Detection Enable	0: Disable detection of mode fault errors 1: Enable detection of mode fault errors.	R/W
b3	MSTR	SPI Master/Slave Mode Select	0: Select slave mode 1: Select master mode.	R/W
b4	SPEIE	SPI Error Interrupt Enable	0: Disable SPI error interrupt requests 1: Enable SPI error interrupt requests.	R/W
b5	SPTIE	Transmit Buffer Empty Interrupt Enable	0: Disable transmit buffer empty interrupt requests 1: Enable transmit buffer empty interrupt requests.	R/W
b6	SPE	SPI Function Enable	0: Disable SPI function 1: Enable SPI function.	R/W
b7	SPRIE	SPI Receive Buffer Full Interrupt Enable	0: Disable SPI receive buffer full interrupt requests 1: Enable SPI receive buffer full interrupt requests.	R/W

If the SPCR.MSTR, SPCR.MODFEN, or SPCR.TXMD bit is changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

SPMS bit (SPI Mode Select)

The SPMS bit selects SPI operation (4-wire method) or clock synchronous operation (3-wire method).

The SSLn0 to SSLn3 pins are not used in clock synchronous operation. The RSPCKn, MOSIn, and MISOn pins handle communications. For clock synchronous operation in master mode (SPCR.MSTR = 1), the SPCMDm.CPHA bit can be set to either 0 or 1. For clock synchronous operation in slave mode (SPCR.MSTR = 0), set the CPHA bit to 1. Do not perform the operations if the CPHA bit is set to 0 when clock synchronous operation is in slave mode.

TXMD bit (Communications Operating Mode Select)

The TXMD bit selects full-duplex synchronous serial communications or transmit-only operations. When this bit is set to 1, the SPI only performs transmit operations and not receive operations (see section 31.3.6, Data Transfer Modes), and the receive buffer full interrupt requests cannot be used.

MODFEN bit (Mode Fault Error Detection Enable)

The MODFEN bit enables or disables the detection of mode fault errors (see section 31.3.8, Error Detection). In addition, the SPI determines the I/O direction of the SSLn0 to SSLn3 pins based on combinations of the MODFEN and MSTR bit settings (see section 31.3.2, Controlling the SPI Pins).

MSTR bit (SPI Master/Slave Mode Select)

The MSTR bit selects master or slave mode for the SPI. Based on the MSTR bit settings, the SPI determines the direction of the RSPCKn, MOSIn, MISOn, and SSLn0 to SSLn3 pins.

SPEIE bit (SPI Error Interrupt Enable)

The SPEIE bit enables or disables the generation of SPI error interrupt requests when one of the following occurs:

- The SPI detects a mode fault error or underrun error and sets the SPSR.MODF flag to 1
- The SPI detects an overrun error and sets the SPSR.OVRF flag to 1
- The SPI detects a parity error and sets the SPSR.PERF flag to 1.

For details, see section 31.3.8, Error Detection.

SPTIE bit (Transmit Buffer Empty Interrupt Enable)

The SPTIE bit enables or disables the generation of transmit buffer empty interrupt requests when the SPI detects that the transmit buffer is empty. To generate a transmit buffer empty interrupt request when transmission starts, set the SPE and SPTIE bits to 1 at the same time or set the SPE bit to 1 after setting the SPTIE bit to 1.

When the SPTIE bit is 1, transmit buffer interrupts are generated even when the SPI function is disabled (when the SPE bit is changed to 0).

SPE bit (SPI Function Enable)

The SPE bit enables or disables the SPI function. The SPE bit cannot be set to 1 when the SPSR.MODF flag is 1. For details, see section 31.3.8, Error Detection.

Setting the SPE bit to 0 disables the SPI function and initializes a part of the module function. For details, see section 31.3.9, Initializing the SPI. In addition, a transmit buffer empty interrupt request is generated when the SPE bit is changed from 0 to 1 or 1 to 0.

SPRIE bit (SPI Receive Buffer Full Interrupt Enable)

The SPRIE bit enables or disables the generation of an SPI receive buffer full interrupt request when the SPI detects a receive buffer full write after completion of a serial transfer.

31.2.2 SPI Slave Select Polarity Register (SSLP)

Address(es): SPI0.SSLP 4007 2001h, SPI1.SSLP 4007 2101h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSL0P	SSL0 Signal Polarity Setting	0: Set SSL0 signal to active-low 1: Set SSL0 signal to active-high.	R/W
b1	SSL1P	SSL1 Signal Polarity Setting	0: Set SSL1 signal to active-low 1: Set SSL1 signal to active-high.	R/W
b2	SSL2P	SSL2 Signal Polarity Setting	0: Set SSL2 signal to active-low 1: Set SSL2 signal to active-high.	R/W
b3	SSL3P	SSL3 Signal Polarity Setting	0: Set SSL3 signal to active-low 1: Set SSL3 signal to active-high.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the contents of SSLP are changed when the SPCR.SPE bit is 1, do not perform subsequent operations.

31.2.3 SPI Pin Control Register (SPPCR)

Address(es): SPI0.SPPCR 4007 2002h, SPI1.SPPCR 4007 2102h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPLP	SPI Loopback	0: Normal mode 1: Loopback mode, with data inverted for transmission.	R/W
b1	SPLP2	SPI Loopback 2	0: Normal mode 1: Loopback mode, with data not inverted for transmission.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	MOIFV	MOSI Idle Fixed Value	0: Set level output on the MOSIn pin during MOSI idling to low 1: Set level output on the MOSIn pin during MOSI idling to high.	R/W
b5	MOIFE	MOSI Idle Value Fixing Enable	0: Set MOSI output value to equal the final data from previous transfer 1: Set MOSI output value to equal value set in the MOIFV bit.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the contents of SPPCR are changed when the SPCR.SPE bit is 1, do not perform subsequent operations.

SPLP bit (SPI Loopback)

The SPLP bit selects the mode of the SPI pins. When this bit is set to 1, SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then connects the input path and output path for the shift register, establishing loopback mode.

SPLP2 bit (SPI Loopback 2)

The SPLP2 bit selects the mode of the SPI pins. When this bit is set to 1, SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then connects the input path and the output path for the shift register, establishing loopback mode 2.

MOIFV bit (MOSI Idle Fixed Value)

If the MOIFE bit is 1 in master mode, the MOIFV bit determines the MOSIn pin output value during the SSL negation period, including the SSL retention period during a burst transfer.

MOIFE bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIn output value when the SPI in master mode is in an SSL negation period, including the SSL retention period during a burst transfer. When the MOIFE bit is 0, the SPI outputs the last data from the previous serial transfer during the SSL negation period to the MOSIn pin. When the MOIFE bit is 1, the SPI outputs the fixed value set in the MOIFV bit to the MOSIn pin.

31.2.4 SPI Status Register (SPSR)

Address(es): SPI0.SPSR 4007 2003h, SPI1.SPSR 4007 2103h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRF	—	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
Value after reset:	0	0	1	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OVRF	Overrun Error Flag	0: No overrun error occurred 1: Overrun error occurred.	R/(W)*1
b1	IDLNF	SPI Idle Flag	0: SPI is in idle state 1: SPI is in transfer state.	R
b2	MODF	Mode Fault Error Flag	0: No mode fault or underrun error occurred 1: Mode fault error or underrun error occurred.	R/(W)*1
b3	PERF	Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*1
b4	UDRF	Underrun Error Flag	0: A mode fault error occurred (MODF = 1) 1: An underrun error occurred (MODF = 1). This bit is invalid when MODF is 0.	R/W*1,*2
b5	SPTEF	SPI Transmit Buffer Empty Flag	0: Data is in the transmit buffer 1: No data is in the transmit buffer.	R/(W)*3
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	SPRF	SPI Receive Buffer Full Flag	0: No valid data is in SPDR/SPDR_HA 1: Valid data is in SPDR/SPDR_HA.	R/(W)*3

Note 1. Only 0 can be written to clear the flag after reading 1.
Note 2. Clear the UDRF flag at the same time as the MODF flag.
Note 3. The write value should be 1.

OVRF flag (Overrun Error Flag)

The OVRF flag indicates the occurrence of an overrun error. In master mode (SPCR.MSTR = 1) and when the RSPCK clock auto-stop function is enabled (SPCR2.SCKASE = 1), an overrun error does not occur, and this flag is not set to 1. For details, see section 31.3.8.1, Overrun errors.

[Setting condition]

- When the next serial transfer ends while the SPCR.TXMD bit is 0 and the receive buffer is full.

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

IDLNF flag (SPI Idle Flag)

The IDLNF flag indicates the transfer status of the SPI.

[Setting conditions]

Master mode

- When conditions 1. and 2. in the master mode, in the clearing conditions, are not satisfied.

Slave mode

- When the SPCR.SPE bit is 1, enabling the SPI function.

[Clearing conditions]

Master mode

- When condition 1. or conditions 2., 3., and 4. are satisfied.

1. The SPCR.SPE bit is 0, indicating that the SPI is initialized.
2. The transmit buffer (SPTX) is empty, indicating that data for the next transfer is not set.
3. The SPSSR.SPCP[2:0] bits are 000b, indicating the beginning of sequence control.
4. The SPI internal sequencer is in the idle state, indicating that operations up to the next-access delay are complete.

Slave mode

- When condition 1. is satisfied.

MODF flag (Mode Fault Error Flag)

The MODF flag indicates the occurrence of a mode fault error or an underrun error. The UDRF flag indicates which error occurred.

[Setting conditions]

Multi-master mode

- When the input level of the SSLni pin changes to an active level while the SPCR.MSTR bit is 1 (master mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), triggering a mode fault error.

Slave mode

- When condition 1. or 2. is satisfied.

  1. The SSLni pin is negated before the RSPCK cycle required for data transfer ends while the SPCR.MSTR bit is 0 (slave mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), triggering a mode fault error.
  2. The serial transfer begins with the SPCR.MSTR bit set to 0 (slave mode), the SPCR.SPE bit set to 1, and the transmission data not prepared, triggering an underrun error.

The active level of the SSLni signal is determined by the SSLP.SSLiP bit (SSLi signal polarity setting).

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

PERF flag (Parity Error Flag)

The PERF flag indicates the occurrence of a parity error.

[Setting condition]

- When a serial transfer ends while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1, triggering a parity error.

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

UDRF flag (Underrun Error Flag)

The UDRF flag indicates the occurrence of an underrun error.

[Setting condition]

- When the serial transfer begins with the SPCR.MSTR bit set to 0 (slave mode), the SPCR.SPE bit set to 1, and the

transmission data not prepared, triggering an underrun error.

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

SPTEF flag (SPI Transmit Buffer Empty Flag)

The SPTEF flag indicates the status of the transmit buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting conditions]

- When condition 1. or 2. is satisfied.

  1. The SPCR.SPE bit is 0, indicating that the SPI is initialized.

  2. Transmit data is transferred from the transmit buffer to the shift register.

[Clearing condition]

- When data written to SPDR/SPDR_HA equals the number of frames set in the SPFC[1:0] bits in the SPI Data Control Register (SPDCR).

Data can only be written to SPDR/SPDR_HA when the SPTEF flag is 1. If data is written to the transmit buffer of SPDR/SPDR_HA when the SPTEF flag is 0, data in the transmit buffer is not updated.

SPRF flag (SPI Receive Buffer Full Flag)

The SPRF flag indicates the status of the receive buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting condition]

- When a serial transfer ends while the Communication Operating Mode Select bit (TXMD) in the SPI Control Register (SPCR) is 0, the SPRF flag is 0, and the SPI transfers the receive data from the shift register to SPDR/SPDR_HA. However, when the OVRF flag is 1, the SPRF flag does not change from 0 to 1.

[Clearing condition]

- When received data is read from SPDR/SPDR_HA.

31.2.5 SPI Data Register (SPDR/SPDR_HA)

Address(es): SPI0.SPDR 4007 2004h, SPI1.SPDR 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address(es): SPI0.SPDR_HA 4007 2004h, SPI1.SPDR_HA 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPDR/SPDR_HA is the interface with the buffers that hold data for transmission and reception by the SPI.

When accessing this register in words (SPLW = 1), access the SPDR register. When accessing it in halfwords (SPLW = 0), access the SPDR_HA register.

The transmit buffer (SPTX) and receive buffer (SPRX) are independent but are both mapped to SPDR/SPDR_HA. Figure 31.2 shows the configuration of the SPDR/SPDR_HA register.

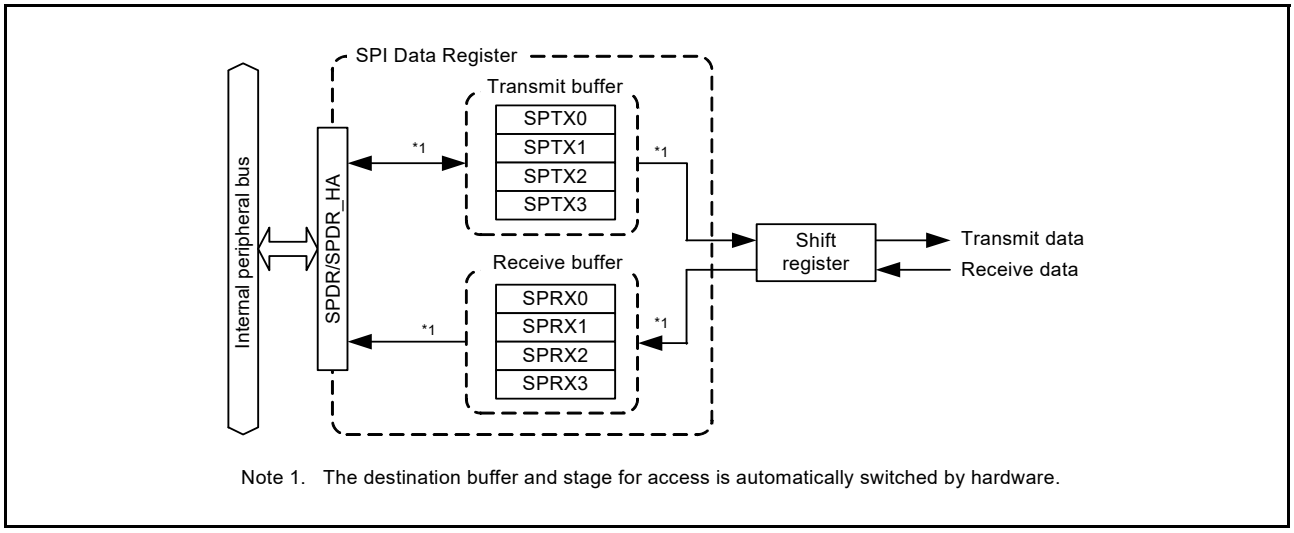


Figure 31.2 Configuration of SPDR/SPDR_HA

The transmit and receive buffers each have four stages. The number of stages to be used is selectable by the number of frames specification bits in the SPI Data Control Register (SPDCR.SPFC[1:0]). The eight stages of the buffer are all mapped to the single address of the SPDR/SPDR_HA register.

Data written to SPDR/SPDR_HA is written to a transmit-buffer stage (SPTXn) (n = 0 to 3) and then transmitted from the buffer. The receive buffer holds the received data on completion of reception. The receive buffer is not updated if an overrun is generated.

If the data length is not 32 bits, the bits not referred to in SPTXn (n = 0 to 3) are stored in the associated bits in SPRXn (n = 0 to 3). For example, if the data length is 9 bits, the received data is stored in the SPRXn[8:0] bits, and the SPTXn[31:9] bits are stored in the SPRXn[31:9] bits.

(1) Bus interface

SPDR/SPDR_HA is an interface with 32-bit wide transmit and receive buffers, each of which has four stages, for a total of 32 bytes. The 32 bytes are mapped to the 4-byte address space for SPDR/SPDR_HA. The unit of access for SPDR/SPDR_HA is selected by the SPI Word Access/Halfword Access Specification bit in the SPI Data Control Register (SPDCR.SPLW). SPDR can also be accessed with the access size specified by the SPI Byte Access bit in the SPI Data Control Register (SPDCR.SPBYT).

Flush the transmission data at the LSB end of the register, and store the received data at the LSB end.

The following sections describe the operations involved in writing to and reading from SPDR/SPDR_HA.

(a) Writing

Data written to SPDR/SPDR_HA is written to a transmit buffer (SPTXn). This is not affected by the value of the SPDCR.SPRDTD bit, unlike when reading from SPDR/SPDR_HA. The transmit buffer includes a transmit buffer write pointer that is automatically updated to reference the next stage each time data is written to SPDR/SPDR_HA.

Figure 31.3 shows the configuration of the bus interface with the transmit buffer when writing to SPDR/SPDR_HA.

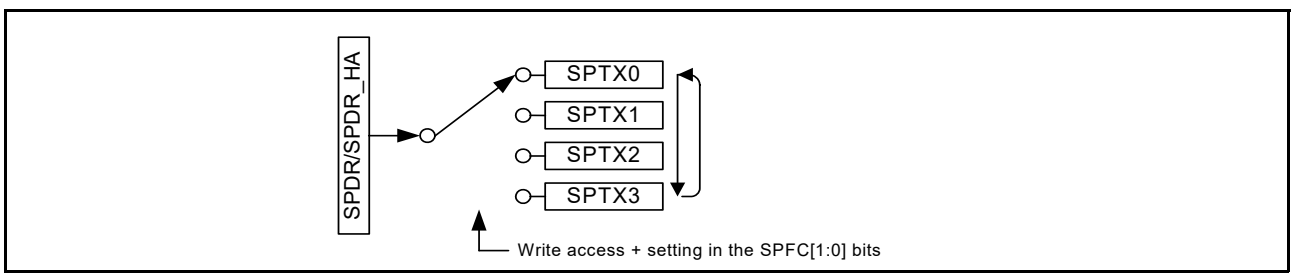


Figure 31.3 Configuration of SPDR/SPDR_HA for write access

The sequence for switching the transmit buffer write pointer changes with the setting of the number of frames specification bits in the SPI Data Control Register (SPDCR.SPFC[1:0]).

The relationship of the SPFC[1:0] setting and the sequence of pointer switching from SPTX0 to SPTX3 is as follows:

- When the SPFC[1:0] bits are 00b: SPTX0 → SPTX0 → SPTX0 → …
- When the SPFC[1:0] bits are 01b: SPTX0 → SPTX1 → SPTX0 → SPTX1 → …
- When the SPFC[1:0] bits are 10b: SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 → …
- When the SPFC[1:0] bits are 11b: SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → …

When 1 is written to the SPI Function Enable bit in the SPI Control Register (SPCR.SPE) while the bit is 0, SPTX0 is the destination for the next write.

When writing to the transmit buffer (SPTXn) after generation of the transmit buffer empty interrupt (when SPSR.SPTEF is 1), write the number of frames set in the SPI Data Control Register (SPDCR.SPFC[1:0]). Even when the specified number of frames is written to the transmit buffer (SPTXn), the value of the buffer is not updated after completion of the writing and before generation of the next transmit buffer empty interrupt (when SPTEF is 0).

(b) Reading

SPDR/SPDR_HA can be accessed to read the value of a receive buffer (SPRXn) or a transmit buffer (SPTXn). The setting in the SPI Receive/Transmit Data Select bit in the SPI Data Control Register (SPDCR.SPRDTD) selects whether reading is from the receive or transmit buffer.

The sequence of reading the SPDR/SPDR_HA register is controlled by the independent receive buffer and transmit buffer read pointers.

Figure 31.4 shows the configuration of a bus interface with the receive and transmit buffers for reading from SPDR/SPDR_HA.

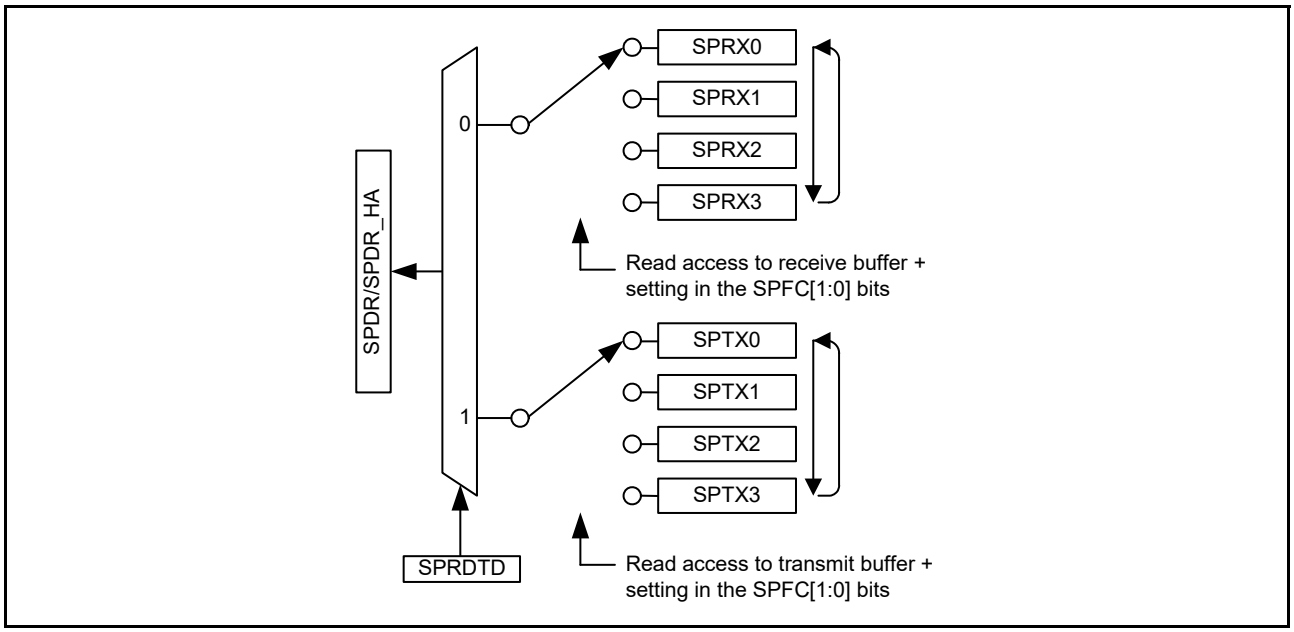


Figure 31.4 Configuration of SPDR/SPDR_HA for read access

Reading the receive buffer switches the receive buffer read pointer to the next buffer automatically. The switching sequence for the receive buffer read pointer is the same as that for the transmit buffer write pointer. However, when 1 is written to the SPI Function Enable bit in the SPI Control Register (SPCR.SPE) when the bit is 1, SPRX0 is referenced by the buffer read pointer for the next read.

The transmit buffer read pointer is updated when writing to SPDR/SPDR_HA, but is not updated when reading from the transmit buffer. When reading from the transmit buffer, the value most recently written to SPDR/SPDR_HA is read.

However, after a transmit buffer empty interrupt is generated, and the transmit buffer becomes full again, reading from

the transmit buffer returns all 0s after the completion of writing the number of frames of data specified in the SPDCR.SPFC[1:0] bits, until the next buffer empty interrupt is generated (when SPTEF is 0).

31.2.6 SPI Sequence Control Register (SPSCR)

Address(es): SPI0.SPSCR 4007 2008h, SPI1.SPSCR 4007 2108h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPSLN[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SPSLN[2:0]	SPI Sequence Length Specification	b2 b1 b0 Sequence Length — Referenced SPCMD0 to SPCMD7 (Number) 0 0 0: 1 — 0→0→… 0 0 1: 2 — 0→1→0→… 0 1 0: 3 — 0→1→2→0→… 0 1 1: 4 — 0→1→2→3→0→… 1 0 0: 5 — 0→1→2→3→4→0→… 1 0 1: 6 — 0→1→2→3→4→5→0→… 1 1 0: 7 — 0→1→2→3→4→5→6→0→… 1 1 1: 8 — 0→1→2→3→4→5→6→7→0→… The sequence length that is set in these bits determines the order in which the SPCMD0 to SPCMD07 registers are referenced. The setting defines the relationship between the sequence length and the SPCMD0 to SPCMD7 registers referenced by the SPI. In slave mode, the SPI references SPCMD0.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPSCR specifies the sequence length when the SPI operates in master mode. When changing the SPSCR.SPSLN[2:0] bits while both the SPCR.MSTR and SPCR.SPE bits are 1, always check that the SPSR.IDLNF flag is 0.

SPSLN[2:0] bits (SPI Sequence Length Specification)

The SPSLN[2:0] bits specify the sequence length when the SPI in master mode performs sequential operations. The SPI in master mode changes the SPCMD0 to SPCMD7 registers to be referenced, and the order in which they are referenced is based on this sequence length setting. In slave mode, SPCMD0 is referenced.

31.2.7 SPI Sequence Status Register (SPSSR)

Address(es): SPI0.SPSSR 4007 2009h, SPI1.SPSSR 4007 2109h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPECM[2:0]			—	SPCP[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SPCP[2:0]	SPI Command Pointer	b2 b1 b0 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7.	R
b3	—	Reserved	This bit is read as 0	R

Bit	Symbol	Bit name	Description	R/W
b6 to b4	SPECM[2:0]	SPI Error Command	b6 b4 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7.	R
b7	—	Reserved	This bit is read as 0	R

SPSSR indicates the sequence control status when the SPI operates in master mode. Any writes to SPSSR are ignored.

SPCP[2:0] bits (SPI Command Pointer)

The SPCP[2:0] bits indicate the SPCMDm register that is referenced to by the pointer during sequence control by the SPI. For the SPI sequence control, see section 31.3.10.1, Master mode operation.

SPECM[2:0] bits (SPI Error Command)

The SPECM[2:0] bits indicate the SPCMDm register that is specified in the SPCP[2:0] bits when an error is detected during sequence control by the SPI. The SPI updates the SPECM[2:0] bits only when an error is detected. If both the SPSR.OVRF and SPSR.MODF flags are 0 and there is no error, the values of the SPECM[2:0] bits have no meaning.

For the SPI error detection function, see section 31.3.8, Error Detection. For the SPI sequence control, see section 31.3.10.1, Master mode operation.

31.2.8 SPI Bit Rate Register (SPBR)

Address(es): SPI0.SPBR 4007 200Ah, SPI1.SPBR 4007 210Ah

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

SPBR sets the bit rate in master mode. If the contents of SPBR are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

When the SPI is in slave mode, the bit rate depends on the bit rate of the input clock, regardless of the settings in SPBR and the SPCMDm.BRDV[1:0] bits (bit rate division setting). Use bit rates that satisfy the electrical characteristics of the device.

The bit rate is determined by combination of the SPBR and SPCMDm.BRDV[1:0] settings in the SPI Command Register. The equation for calculating the bit rate is as follows:

$$\text{Bit rate} = \frac{f(\text{PCLKA})}{2 \times (n + 1) \times 2^{N}}$$

In the equation, n denotes an SPBR setting (0, 1, 2, …, 255), and N denotes a BRDV[1:0] setting (0, 1, 2, 3).

Table 31.3 lists examples of the relationship between the SPBR settings, BRDV[1:0] settings, and bit rates.

Table 31.3 Relationship between SPBR settings, BRDV[1:0] settings, and bit rates (1 of 2)

SPBR (n)	BRDV[1:0] bits (N)	Division ratio	Bit rate							
			PCLKA = 32 MHz	PCLKA = 36 MHz	PCLKA = 40 MHz	PCLKA = 50 MHz	PCLKA = 60 MHz	PCLKA = 80 MHz	PCLKA = 100 MHz	PCLKA = 120 MHz
0	0	2	16.0 Mbps	18.0 Mbps	20.0 Mbps	25.0 Mbps	30.0 Mbps	Not supported		
1	0	4	8.00 Mbps	9.00 Mbps	10.0 Mbps	12.5 Mbps	15.0 Mbps	20.0 Mbps	25.0 Mbps	30.0 Mbps

Table 31.3 Relationship between SPBR settings, BRDV[1:0] settings, and bit rates (2 of 2)

SPBR (n)	BRDV[1:0] bits (N)	Division ratio	Bit rate							
			PCLKA = 32 MHz	PCLKA = 36 MHz	PCLKA = 40 MHz	PCLKA = 50 MHz	PCLKA = 60 MHz	PCLKA = 80 MHz	PCLKA = 100 MHz	PCLKA = 120 MHz
2	0	6	5.33 Mbps	6.00 Mbps	6.67 Mbps	8.33 Mbps	10.0 Mbps	13.3 Mbps	16.7 Mbps	20.0 Mbps
3	0	8	4.00 Mbps	4.50 Mbps	5.00 Mbps	6.25 Mbps	7.50Mbps	10.0 Mbps	12.5 Mbps	15.0 Mbps
4	0	10	3.20 Mbps	3.60 Mbps	4.00 Mbps	5.00 Mbps	6.00 Mbps	8.00 Mbps	10.0 Mbps	12.0 Mbps
5	0	12	2.67 Mbps	3.00 Mbps	3.33 Mbps	4.16 Mbps	5.00 Mbps	6.67 Mbps	8.33 Mbps	10.0 Mbps
5	1	24	1.33 Mbps	1.50 Mbps	1.67 Mbps	2.08 Mbps	2.50 Mbps	3.33 Mbps	4.17 Mbps	5.00 Mbps
5	2	48	667 kbps	750 kbps	833 kbps	1.04 Mbps	1.25 Mbps	1.67 Mbps	2.08 Mbps	2.50 Mbps
5	3	96	333 kbps	375 kbps	417 kbps	521 kbps	625 kbps	833 kbps	1.04 Mbps	1.25 Mbps
255	3	4096	7.81 kbps	8.80 kbps	9.78 kbps	12.2 kbps	14.6 kbps	19.5 kbps	24.4 kbps	29.3 kbps

31.2.9 SPI Data Control Register (SPDCR)

Address(es): SPI0.SPDCR 4007 200Bh, SPI1.SPDCR 4007 210Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPBYT	SPLW	SPRDTD	—	—	SPFC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	SPFC[1:0]	Number of Frames Specification	b1 b0 0 0: 1 frame 0 1: 2 frames 1 0: 3 frames 1 1: 4 frames.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SPRDTD	SPI Receive/Transmit Data Select	0: Read SPDR/SPDR_HA values from the receive buffer 1: Read SPDR/SPDR_HA values from the transmit buffer, but only if the transmit buffer is empty.	R/W
b5	SPLW	SPI Word Access/Halfword Access Specification	0: Set SPDR_HA to valid for halfword access 1: Set SPDR to valid for word access.	R/W
b6	SPBYT	SPI Byte Access Specification	0: SPDR is accessed in halfword or word (SPLW is valid) 1: SPDR is accessed in byte (SPLW is invalid).	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Up to four frames can be transmitted or received in one round of transmission or reception. The amount of data in each transfer is controlled by the combination of the SPCMDm.SPB[3:0] bits, SPSCR.SPSLN[2:0] bits, and SPDCR.SPFC[1:0] bits.

When changing the SPDCR.SPFC[1:0] bits while the SPCR.SPE bit is 1, always check that the SPSR.IDLNF flag is 0.

SPFC[1:0] bits (Number of Frames Specification)

The SPFC[1:0] bits specify the number of frames that can be stored in SPDR/SPDR_HA per transfer activation. Up to four frames can be transmitted or received in one round of transmission or reception.

When the number of transmission data frames specified in the SPFC[1:0] bits is written to the SPDR/SPDR_HA register, the SPI clears the SPSR.SPTEF flag to 0 and begins transmitting. After that, when the number of transmission data frames specified in the SPFC[1:0] bits is transmitted to the shift register, the SPI generates the transmit buffer empty interrupt (SPSR.SPTEF is set to 1).

When the number of data frames specified in the SPFC[1:0] bits is received, the SPI generates a receive buffer full interrupt (SPSR.SPRF is set to 1).

Table 31.4 Settable combinations of the SPSLN[2:0] and SPFC[1:0] bits

Setting	SPSLN[2:0]	SPFC[1:0]	Number of frames in a single sequence	Number of frames at which transmit or receive buffer is filled
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD bit (SPI Receive/Transmit Data Select)

The SPRDTD bit selects whether the SPDR/SPDR_HA reads values from the receive buffer or from the transmit buffer.

If reading is from the transmit buffer, the last value written to the SPDR/SPDR_HA register is read. Read the transmit buffer before the writing of the number of frames set in the SPFC[1:0] bits is finished and after the generation of the transmit buffer empty interrupt (when SPSR.SPTEF is 1).

For details, see section 31.2.5, SPI Data Register (SPDR/SPDR_HA).

SPLW bit (SPI Word Access/Halfword Access Specification)

The SPLW bit specifies the access width for SPDR. Access to SPDR_HA in halfwords is valid when the SPLW bit is 0 and access to SPDR in words is valid when the SPLW bit is 1. Also, when the SPLW bit is 0, set the SPI data length setting bits, SPCMDm.SPB[3:0]), from 8 to 16 bits. Do not perform any operations when a data length of 20, 24, or 32 bits is specified.

SPBYT bit (SPI Byte Access Specification)

The SPBYT bit is used to set the data width of access to the SPI Data Register (SPDR). When SPBYT is 0, use word or half word access to SPDR. When SPBYT is 1 (SPLW is invalid), use byte access to SPDR.

When SPBYT is 1, set the SPI Data Length Setting (SPB[3:0]) bits in the SPI Command Register n (SPCMDn) to 0 bits. If SPB[3:0] are set to 9 to 16, 20, 24, or 32 bits, subsequent operation is not guaranteed.

31.2.10 SPI Clock Delay Register (SPCKD)

Address(es): SPI0.SPCKD 4007 200Ch, SPI1.SPCKD 4007 210Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SCKDL[2:0]	RSPCK Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPCKD specifies the RSPCK delay, the period from the beginning of SSLni signal assertion to RSPCK oscillation, when the SPCMDm.SCKDEN bit is 1. If the contents of SPCKD are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SCKDL[2:0] bits (RSPCK Delay Setting)

The SCKDL[2:0] bits specify an RSPCK delay value when the SPCMDm.SCKDEN bit is 1. When using the SPI in slave mode, set the SCKDL[2:0] bits to 000b.

31.2.11 SPI Slave Select Negation Delay Register (SSLND)

Address(es): SPI0.SSLND 4007 200Dh, SPI1.SSLND 4007 210Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SLNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SLNDL[2:0]	SSL Negation Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SSLND specifies the SSL negation delay, the period from the transmission of a final RSPCK edge to the negation of the SSLni signal during a serial transfer by the SPI in master mode. If the contents of SSLND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SLNDL[2:0] bits (SSL Negation Delay Setting)

The SLNDL[2:0] bits specify an SSL negation delay value when the SPI is in master mode. When using the SPI in slave mode, set the SLNDL[2:0] bits to 000b.

31.2.12 SPI Next-Access Delay Register (SPND)

Address(es): SPI0.SPND 4007 200Eh, SPI1.SPND 4007 210Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SPNDL[2:0]	SPI Next-Access Delay Setting	b2 b0 0 0 0: 1 RSPCK + 2 PCLKA 0 0 1: 2 RSPCK + 2 PCLKA 0 1 0: 3 RSPCK + 2 PCLKA 0 1 1: 4 RSPCK + 2 PCLKA 1 0 0: 5 RSPCK + 2 PCLKA 1 0 1: 6 RSPCK + 2 PCLKA 1 1 0: 7 RSPCK + 2 PCLKA 1 1 1: 8 RSPCK + 2 PCLKA.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPND specifies the next-access delay, the non-active period of the SSLni signal after termination of a serial transfer, when the SPCMDm.SPNDEN bit is 1. If the contents of SPND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SPNDL[2:0] bits (SPI Next-Access Delay Setting)

The SPNDL[2:0] bits specify a next-access delay when the SPCMDm.SPNDEN bit is 1. When using the SPI in slave mode, set the SPNDL[2:0] bits to 000b.

31.2.13 SPI Control Register 2 (SPCR2)

Address(es): SPI0.SPCR2 4007 200Fh, SPI1.SPCR2 4007 210Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPPE	Parity Enable	0: No parity bit added to transmit data and parity bit of receive data not checked 1: When SPCR.TXMD = 0, parity bit added to transmit data and parity bit of receive data checked When SPCR.TXMD = 1, parity bit added to transmit data but parity bit of receive data not checked.	R/W
b1	SPOE	Parity Mode	0: Even parity selected for transmission and reception 1: Odd parity selected for transmission and reception.	R/W
b2	SPIIE	SPI Idle Interrupt Enable	0: Idle interrupt requests disabled 1: Idle interrupt requests enabled.	R/W
b3	PTE	Parity Self-Testing	0: Self-diagnosis function of the parity circuit disabled 1: Self-diagnosis function of the parity circuit enabled.	R/W
b4	SCKASE	RSPCK Auto-Stop Function Enable	0: RSPCK auto-stop function disabled 1: RSPCK auto-stop function enabled.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the SPPE, SPOE, or SCKASE bit in SPCR2 is changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

SPPE bit (Parity Enable)

The SPPE bit enables or disables the parity function.

When the SPCR.TXMD bit is 0 and this bit is 1, the parity bit is added to transmit data and parity checking is performed for receive data.

When the SPCR.TXMD bit is 1 and this bit is 1, the parity bit is added to transmit data but parity checking is not performed for receive data.

SPOE bit (Parity Mode)

The SPOE bit specifies odd or even parity.

When even parity is set, parity bit addition is performed so that the total number of bits whose value is 1 in the transmit or receive character plus the parity bit is even. Similarly, when odd parity is set, parity bit addition is performed so that the total number of bits whose value is 1 in the transmit or receive character plus the parity bit is odd.

The SPOE bit is only valid when the SPPE bit is 1.

SPIIE bit (SPI Idle Interrupt Enable)

The SPIIE bit enables or disables the generation of SPI idle interrupt requests when an idle state is detected in the SPI and the SPSR.IDLNF flag is set to 0.

PTE bit (Parity Self-Testing)

The PTE bit enables self-diagnosis of the parity circuit to check whether the parity function is operating correctly.

SCKASE bit (RSPCK Auto-Stop Function Enable)

The SCKASE bit enables or disables the RSPCK auto-stop function. When this function is enabled, the RSPCK clock is stopped before an overrun error occurs, when data is received in master mode. For details, see section 31.3.8.1, Overrun errors.

31.2.14 SPI Command Registers 0 to 7 (SPCMD0 to SPCMD7)

Address(es): SPI0.SPCMD0 4007 2010h, SPI0.SPCMD1 4007 2012h, SPI0.SPCMD2 4007 2014h, SPI0.SPCMD3 4007 2016h, SPI0.SPCMD4 4007 2018h, SPI0.SPCMD5 4007 201Ah, SPI0.SPCMD6 4007 201Ch, SPI0.SPCMD7 4007 201Eh, SPI1.SPCMD0 4007 2110h, SPI1.SPCMD1 4007 2112h, SPI1.SPCMD2 4007 2114h, SPI1.SPCMD3 4007 2116h, SPI1.SPCMD4 4007 2118h, SPI1.SPCMD5 4007 211Ah, SPI1.SPCMD6 4007 211Ch, SPI1.SPCMD7 4007 211Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b0	CPHA	RSPCK Phase Setting	0: Select data sampling on leading edge, data change on trailing edge 1: Select data change on leading edge, data sampling on trailing edge.	R/W
b1	CPOL	RSPCK Polarity Setting	0: Set RSPCK low when idle 1: Set RSPCK high when idle.	R/W
b3, b2	BRDV[1:0]	Bit Rate Division Setting	b3 b2 0 0: Select the base bit rate 0 1: Select the base bit rate divided by 2 1 0: Select the base bit rate divided by 4 1 1: Select the base bit rate divided by 8.	R/W
b6 to b4	SSLA[2:0]	SSL Signal Assertion Setting	b6 b4 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 1 x x: Setting prohibited x: Don't care.	R/W

Bit	Symbol	Bit name	Description	R/W
b7	SSLKP	SSL Signal Level Keeping	0: Negate all SSL signals on completion of transfer 1: Keep the SSL signal level from the end of transfer until the beginning of the next access.	R/W
b11 to b8	SPB[3:0]	SPI Data Length Setting	b11 b8 0100 to 0111: 8 bits 1 0 0 0: 9 bits 1 0 0 1: 10 bits 1 0 1 0: 11 bits 1 0 1 1: 12 bits 1 1 0 0: 13 bits 1 1 0 1: 14 bits 1 1 1 0: 15 bits 1 1 1 1: 16 bits 0 0 0 0: 20 bits 0 0 0 1: 24 bits 0010, 0011: 32 bits.	R/W
b12	LSBF	SPI LSB First	0: MSB-first 1: LSB-first.	R/W
b13	SPNDEN	SPI Next-Access Delay Enable	0: Select next-access delay of 1 RSPCK + 2 PCLKA 1: Select next-access delay equal to the setting in the SPI Next-Access Delay Register (SPND).	R/W
b14	SLNDEN	SSL Negation Delay Setting Enable	0: Select SSL negation delay of 1 RSPCK 1: Select SSL negation delay equal to the setting in the SPI Slave Select Negation Delay register (SSLND).	R/W
b15	SCKDEN	RSPCK Delay Setting Enable	0: Select RSPCK delay of 1 RSPCK 1: Select RSPCK delay equal to the setting in the SPI Clock Delay register (SPCKD).	R/W

The SPCMDm registers specify the transfer format for the SPI in master mode. Each SPI channel has eight SPI Command registers (SPCMD0 to SPCMD7). Some of the bits in the SPCMD0 register are used to set the transfer mode for the SPI in slave mode. The SPI in master mode sequentially references the SPCMDm registers based on the settings in the SPSCR.SPSLN[2:0] bits and executes the serial transfer that is set in the referenced SPCMDm register.

Set the SPCMDm registers while the transmit buffer is empty (SPSR.SPTEF is 1 and the data for the next transfer is not set), and before the setting of the data to be transmitted when that SPCMDm register is referenced.

The SPCMDm register referenced by the SPI in master mode can be checked with the SPSSR.SPCP[2:0] bits. If the contents of SPCMDm are changed while the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1, do not perform subsequent operations.

CPHA bit (RSPCK Phase Setting)

The CPHA bit selects the RSPCK phase of the SPI in master or slave mode. Data communications between SPI modules require the same RSPCK phase setting between the modules.

CPOL bit (RSPCK Polarity Setting)

The CPOL bit selects the RSPCK polarity of the SPI in master or slave mode. Data communications between SPI modules require the same RSPCK polarity setting between the modules.

BRDV[1:0] bits (Bit Rate Division Setting)

The BRDV[1:0] bits determine the bit rate by combination of the settings in the BRDV[1:0] bits and the SPBR register (see section 31.2.8, SPI Bit Rate Register (SPBR)). The SPBR settings determine the base bit rate. The BRDV[1:0] settings select a bit rate obtained by dividing the base bit rate by 1, 2, 4, or 8. Different BRDV[1:0] bit settings can be specified in the SPCMDm registers, enabling the execution of serial transfers at a different bit rate for each command.

SSLA[2:0] bits (SSL Signal Assertion Setting)

The SSLA[2:0] bits control the SSLni signal assertion when the SPI performs serial transfers in master mode. When an SSLni signal is asserted, its polarity is determined by the value set in the associated SSLP. When the SSLA[2:0] bits are set to 000b in multi-master mode, serial transfers are performed with all the SSL signals in the negated state, as the SSLn0 pin acts as input. When using the SPI in slave mode, set the SSLA[2:0] bits to 000b.

SSLKP bit (SSL Signal Level Keeping)

When the SPI in master mode performs a serial transfer, the SSLKP bit specifies whether the SSLni signal level for the current command is to be kept or negated between the SSL negation associated with the current command and the SSL assertion timing associated with the next command.

Setting the SSLKP bit to 1 enables a burst transfer. For details, see (4) Burst transfers in section 31.3.10.1, Master mode operation. When using the SPI in slave mode, set the SSLKP bit to 0.

SPB[3:0] bits (SPI Data Length Setting)

The SPB[3:0] bits specify the transfer data length for the SPI in master or slave mode. When the SPLW bit is 0, set these bits from 8 to 16 bits.

LSBF bit (SPI LSB First)

The LSBF bit specifies the data format of the SPI in master or slave mode to MSB-first or LSB-first.

SPNDEN bit (SPI Next-Access Delay Enable)

The SPNDEN bit specifies the next-access delay, the period from the time the SPI in master mode terminates a serial transfer and sets the SSLni signal inactive until the SPI enables the SSLni signal assertion for the next access. If the SPNDEN bit is 0, the SPI sets the next-access delay to 1 RSPCK + 2 PCLKA. If the SPNDEN bit is 1, the SPI inserts a next-access delay in accordance with the SPND setting.

When using the SPI in slave mode, set the SPNDEN bit to 0.

SLNDEN bit (SSL Negation Delay Setting Enable)

The SLNDEN bit specifies the SSL negation delay, the period from the time the SPI in master mode stops RSPCK oscillation until the SPI sets the SSLni signal to inactive. If the SLNDEN bit is 0, the SPI sets the SSL negation delay to 1 RSPCK. If the SLNDEN bit is 1, the SPI negates the SSL signal at an SSL negation delay according to the SSLND setting.

When using the SPI in slave mode, set the SLNDEN bit to 0.

SCKDEN bit (RSPCK Delay Setting Enable)

The SCKDEN bit specifies the SPI clock delay, the period from the point when the SPI in master mode asserts the SSLni signal until the RSPCK starts oscillation (SPI clock delay). If the SCKDEN bit is 0, the SPI sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, the SPI starts the oscillation of RSPCK at an RSPCK delay according to the SPCKD setting.

When using the SPI in slave mode, set the SCKDEN bit to 0.

31.2.15 SPI Data Control Register 2 (SPDCR2)

Address(es): SPI0.SPDCR2 4007 2020h, SPI1.SPDCR2 4007 2120h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BYSW
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BYSW	Byte Swap Operating Mode Select	0: Byte swap off 1: Byte swap on.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPI Data Control Register 2 (SPDCR2) swaps the transmit or receive data in byte units. When transmit buffer data is copied to a shift register, it is swapped in byte units. When shift register data is copied to a receive buffer, it is swapped in byte units.

BYSW bit (Byte Swap Operating Mode Select)

The BYSW bit swaps the transmit or receive data in byte units. When byte access is valid (SPDCR.SPBYT = 1), byte swap is invalid. When byte swap is valid, parity function is invalid (SPCR2.SPPE bit = 0). The BYSW bit can only be changed when the SPCR.SPE bit is 0.

Data after byte swap is different depending on the data length (setting of SPCMD.SPB[3:0]).

At byte swap, the data length must be set to 32 bits or 16 bits. If data length is set to other values such as 8 to 15, 20, 24 bit length, byte swap is not guaranteed. Before swap and after swap (data length is 32 bits or 16 bits), the values are as shown:

- For data length of 32 bits (SPB[3:0] = 0010 or 0011)

  Before swap: [31:24] [23:16] [15:8] [7:0]

  After swap: [7:0] [15:8] [23:16] [31:24]

- For data length data of 16 bits (SPB[3:0] = 1111)

  Before swap: [31:24] [23:16]

  After swap: [23:16] [31:24].

In byte access mode (SPDCR.SPBT = 1), byte swap setting is invalid.

When byte swap is valid, set the parity function to invalid (SPCR2.SPPE = 0). When the parity function is set to valid, the behavior is not guaranteed.

31.3 Operation

In this section, the *serial transfer period* refers to the period from the beginning of driving valid data to the fetching of the final valid data.

31.3.1 Overview of SPI Operation

The SPI is capable of synchronous serial transfers in the following modes:

- Slave mode (SPI operation)
- Single-master mode (SPI operation)
- Multi-master mode (SPI operation)
- Slave mode (clock synchronous operation)
- Master mode (clock synchronous operation).

The SPI mode can be selected with the MSTR, MODFEN, and SPMS bits in SPCR. Table 31.5 lists the relationship between the SPI modes and SPCR settings, and a description of each mode.

Table 31.5 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn signal	Input	Output	Output/Hi-Z	Input	Output
MOSIn signal	Input	Output	Output/Hi-Z	Input	Output
MISOn signal	Output/Hi-Z	Input	Input	Output	Input
SSLn0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 signals	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1

Table 31.5 Relationship between SPCR settings and SPI modes (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
SSL polarity change function	Supported	Supported	Supported	-	-
Max transfer rate	PCLKA/4	PCLKA/2	PCLKA/2	PCLKA/4	PCLKA/2
Clock source	RSPCKn input	On-chip baud rate generator	On-chip baud rate generator	RSPCKn input	On-chip baud rate generator
Clock polarity	Two				
Clock phase	Two	Two	Two	One (CPHA = 1)	Two
First transfer bit	MSB/LSB				
Transfer data length	8 to 16, 20, 24, 32 bits				
Burst transfer	Possible (CPHA = 1)	Possible (CPHA = 0,1)	Possible (CPHA = 0,1)	-	-
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer trigger	SSL input active or RSPCK oscillation	Write to transmit buffer on generation of a transmit buffer empty interrupt request (SPTEF = 1)	Write to transmit buffer on generation of a transmit buffer empty interrupt request (SPTEF = 1)	RSPCK oscillation	Write to transmit buffer on generation of a transmit buffer empty interrupt request (SPTEF = 1)
Sequence control	Not supported	Supported	Supported	Not supported	Supported
Transmit buffer empty detection	Supported				
Receive buffer full detection	Supported*2				
Overrun error detection	Supported*2	Supported*2, *4	Supported*2, *4	Supported*2	Supported*2
Parity error detection	Supported*2,*3				
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported
Underrun error detection	Supported	Not supported	Not supported	Supported	Not supported

Note 1. This function is not supported in this mode.
Note 2. When the SPCR.TXMD bit is 1, detection of receiver buffer full, overrun error, and parity error is not performed.
Note 3. When the SPCR2.SPPE bit is 0, parity error detection is not performed.
Note 4. When the SPCR2.SCKASE bit is 1, overrun error detection does not proceed.

31.3.2 Controlling the SPI Pins

The SPI can switch pin states based on the MSTR, MODFEN, and SPMS bit settings in SPCR and the PmnPFS.NCODR bit for the I/O ports. Table 31.6 lists the relationship between the pin states and bit settings. Setting the PmnPFS.NCODR bit for an I/O port to 0 selects the CMOS output. Setting it to 1 selects the open-drain output. The I/O port settings must follow this relationship.

Table 31.6 Relationship between pin states and bit settings

Mode	Pin	Pin state*2	
		PmnPFS.NCODR bit for I/O ports = 0	PmnPFS.NCODR bit for I/O ports = 1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Slave mode (clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.
Note 2. SPI settings are not reflected in multiplexed pins for which the SPI function is not selected.
Note 3. When SSLn0 is at the active level, the pin state is Hi-Z.
Note 4. When SSLn0 is at the non-active level or the SPCR.SPE bit is 0, the pin state is Hi-Z.
Note 5. These pins are available for use as I/O port pins.

The SPI in single-master (SPI operation) or multi-master mode (SPI operation) determines the MOSI signal values during the SSL negation period (including the SSL retention period during a burst transfer) based on the MOIFE and MOIFV bit settings in SPPCR, as listed in Table 31.7.

Table 31.7 MOSI signal value determination during SSL negation period

MOIFE bit	MOIFV bit	MOSIn signal value during SSL negation period
0	0, 1	Final data from previous transfer
1	0	Low
1	1	High

31.3.3 SPI System Configuration Examples

31.3.3.1 Single master and single slave with the MCU as a master

Figure 31.5 shows a single-master and single-slave SPI system configuration example where the MCU is a master. In the single-master/single-slave configuration, the SSLn0 to SSLn3 outputs of the MCU (master) are not used. The SSL input of the SPI slave is fixed to the low level, and the SPI slave stays selected.*1

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

Note 1. In the transfer format used when the SPCMDm.CPHA bit is 0, the SSL signal for some slave devices cannot be fixed to an active level. In this case, always connect the SSLni output of the MCU to the SSL input of the slave device.

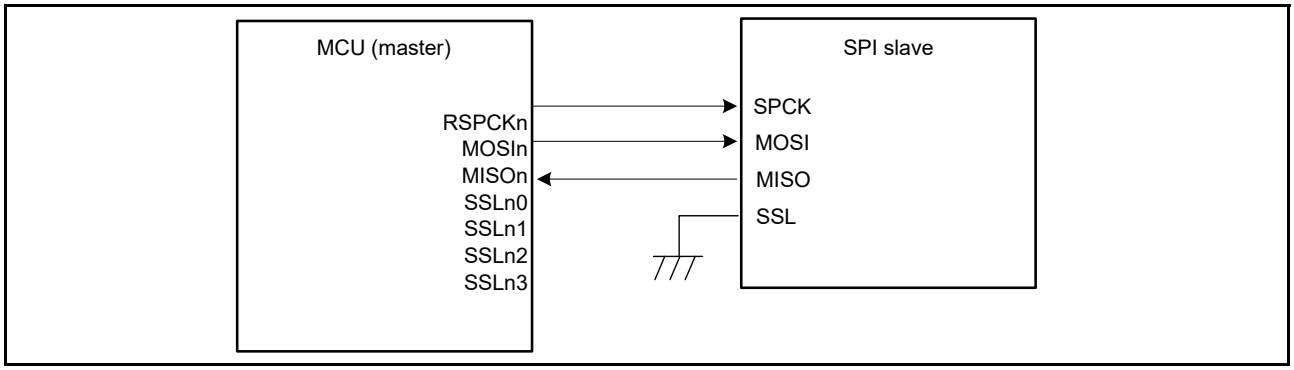


Figure 31.5 Single-master/single-slave configuration example with the MCU as a master

31.3.3.2 Single master and single slave with the MCU as a slave

Figure 31.6 shows a single-master and single-slave SPI system configuration example where the MCU is a slave. When the MCU operates as a slave, the SSLn0 pin is used as SSL input. The SPI master drives the RSPCK and MOSI signals. The MCU (slave) drives the MISOn signal.*1

In the single-slave configuration when the SPCMDm.CPHA bit is set to 1, the SSLn0 input of the MCU (slave) is fixed to the low level and the MCU (slave) stays selected. This enables serial transfer execution (Figure 31.7).

Note 1. When SSLn0 is at a non-active level, the pin state is Hi-Z.

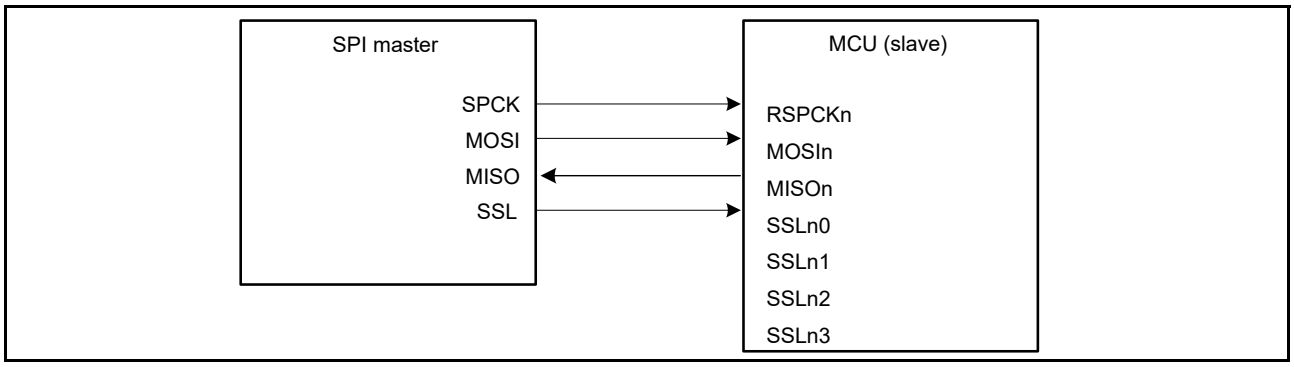


Figure 31.6 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 0

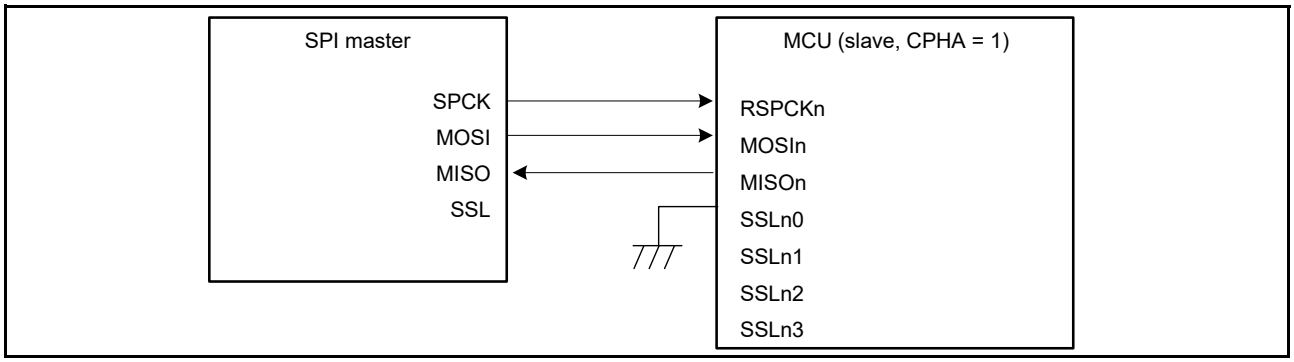


Figure 31.7 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 1

31.3.3.3 Single master and multi slave with the MCU as a master

Figure 31.8 shows a single-master and multi-slave SPI system configuration example where the MCU is a master. In the example, the SPI system includes the MCU (master) and four slaves (SPI slave 0 to SPI slave 3).

The RSPCKn and MOSIn outputs of the MCU (master) are connected to the RSPCK and MOSI inputs of SPI slave 0 to SPI slave 3. The MISO outputs of SPI slave 0 to SPI slave 3 are all connected to the MISOn input of the MCU (master). The SSLn0 to SSLn3 outputs of the MCU (master) are connected to the SSL inputs of SPI slave 0 to SPI slave 3, respectively.

The MCU (master) drives the RSPCKn, MOSIn, and SSLn0 to SSLn3 pins. Of the SPI slave 0 to SPI slave 3, the slave that receives low-level input into the SSL input drives the MISO signal.

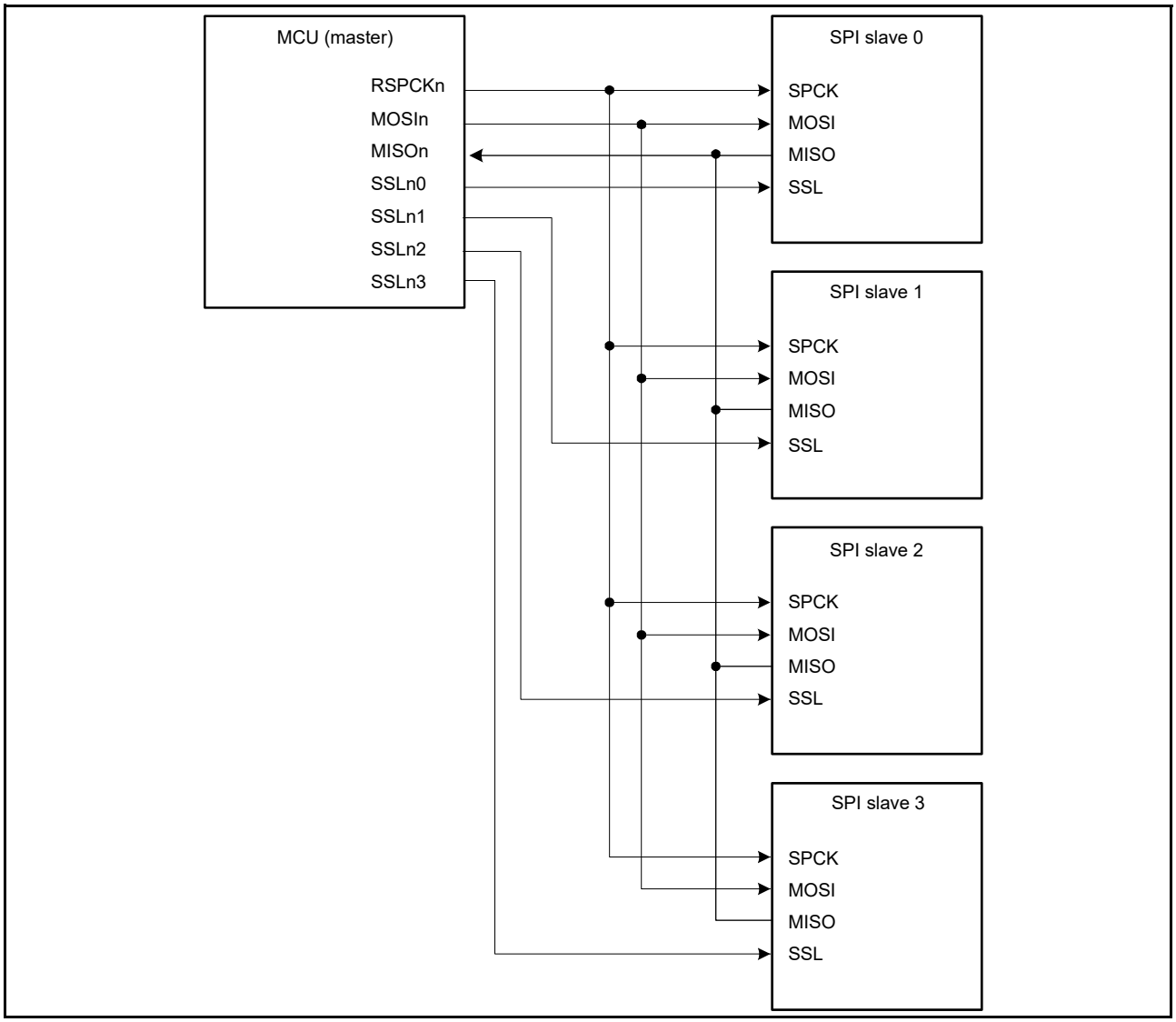


Figure 31.8 Single-master/multi-slave configuration example with the MCU as a a master

31.3.3.4 Single master and multi slave with the MCU as a slave

Figure 31.9 shows a single-master and multi-slave SPI system configuration example where the MCU is a slave. In this example, the SPI system includes an SPI master and two MCUs (slave X and slave Y).

The SPCK and MOSI outputs of the SPI master are connected to the RSPCKn and MOSIn inputs of the MCUs (slaves X and Y). The MISOn outputs of the MCUs (slave X and slave Y) are all connected to the MISO input of the SPI master. The SSLX and SSLY outputs of the SPI master are connected to the SSLn0 inputs of the MCUs (slave X and slave Y), respectively.

The SPI master drives the SPCK, MOSI, SSLX, and SSLY signals. Of the MCUs (slave X or slave Y), the slave that receives low-level input into the SSLn0 input drives the MISOn signal.

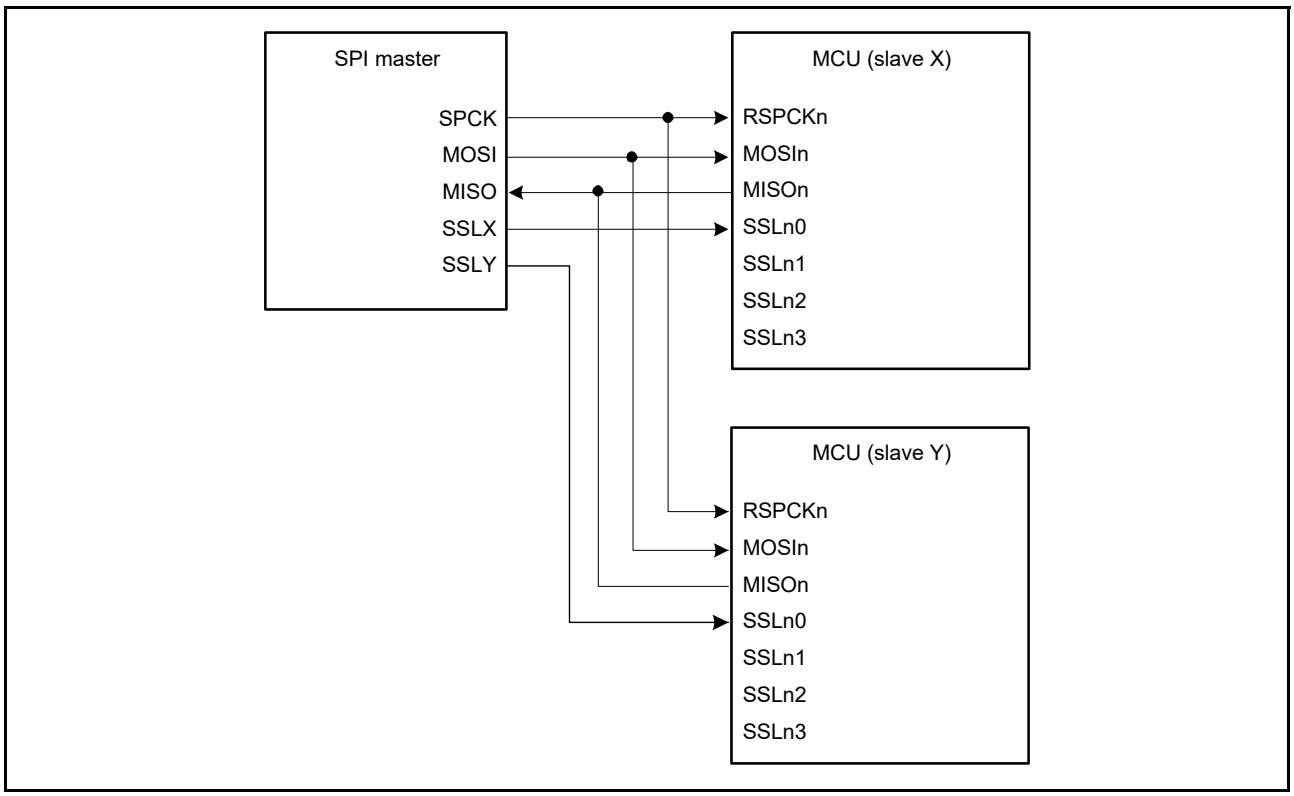


Figure 31.9 Single-master/multi-slave configuration example with the MCU as a slave

31.3.3.5 Multi master and multi slave with the MCU as a master

Figure 31.10 shows a multi-master/multi-slave SPI system configuration example where the MCU is a master. In this example, the SPI system includes two MCUs (master X and master Y) and two SPI slaves (SPI slave 1 and SPI slave 2).

The RSPCKn and MOSIn outputs of the MCUs (master X and master Y) are connected to the RSPCK and MOSI inputs of SPI slaves 1 and 2. The MISO outputs of SPI slaves 1 and 2 are connected to the MISOn inputs of the MCUs (master X and master Y). Any generic port Y output from the MCU (master X) is connected to the SSLn0 input of the MCU (master Y). Any generic port X output of the MCU (master Y) is connected to the SSLn0 input of the MCU (master X). The SSLn1 and SSLn2 outputs of the MCUs (master X and master Y) are connected to the SSL inputs of the SPI slaves 1 and 2. In this configuration example, because the system can be comprised solely of SSLn0 input, and SSLn1, SSLn2 outputs for slave connections, the SSLn3 output of the MCU is not required.

The MCU drives the RSPCKn, MOSIn, SSLn1, and SSLn2 signals when the SSLn0 input level is high. When the SSLn0 input level is low, the MCU detects a mode fault error, sets RSPCKn, MOSIn, SSLn1, and SSLn2 to Hi-Z, and releases the SPI bus directly to the other master. Of the SPI slaves 1 and 2, the slave that receives low-level input into the SSL input drives the MISO signal.

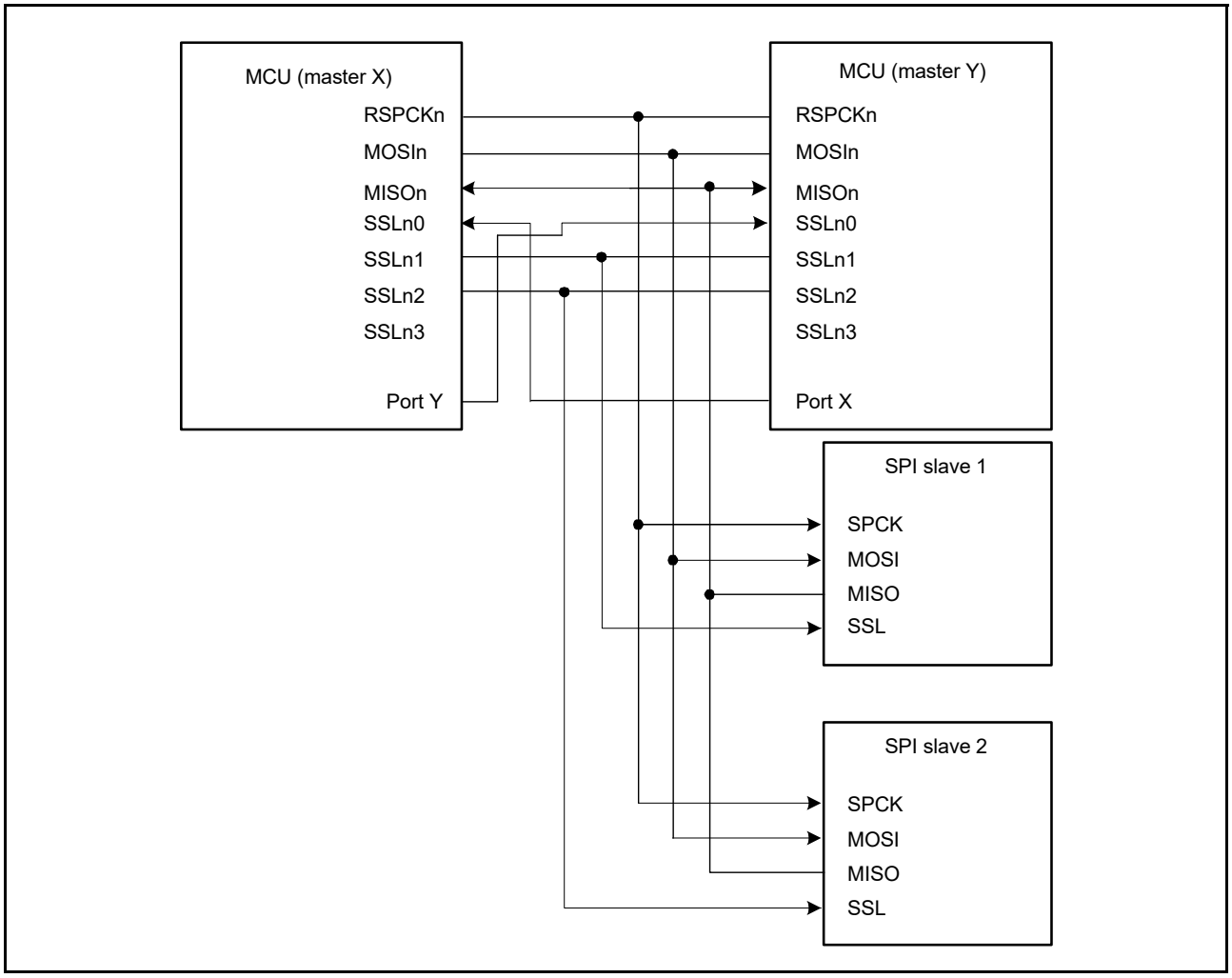


Figure 31.10 Multi-master/multi-slave configuration example with the MCU as a master

31.3.3.6 Master and slave in clock synchronous mode with the MCU as a master

Figure 31.11 shows a master and slave in clock synchronous mode where the MCU is a master. In this configuration, SSLn0 to SSLn3 of the MCU (master) are not used.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

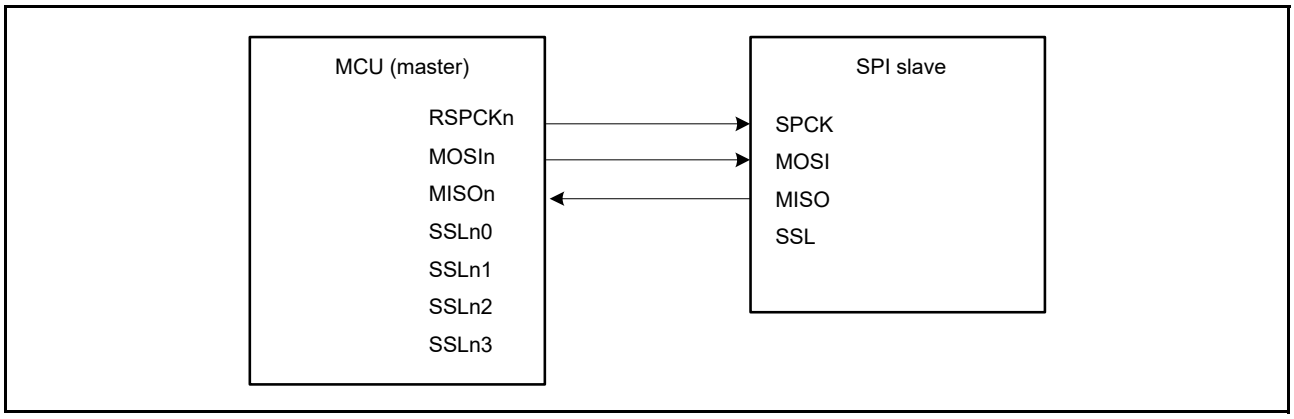


Figure 31.11 Configuration example of master/slave in clock synchronous mode with the MCU as a master

31.3.3.7 Master and slave in clock synchronous mode with the MCU as a slave

Figure 31.12 shows a master and slave in clock synchronous mode configuration where the MCU is a slave. When the MCU operates as a slave in clock synchronous mode, the MCU (slave) drives the MISOn signal and the SPI master drives the SPCK and MOSI signals. SSLn0 to SSLn3 of the MCU (slave) are not used.

The MCU (slave) can only execute serial transfer in the single-slave configuration when the SPCMDm.CPHA bit is set to 1.

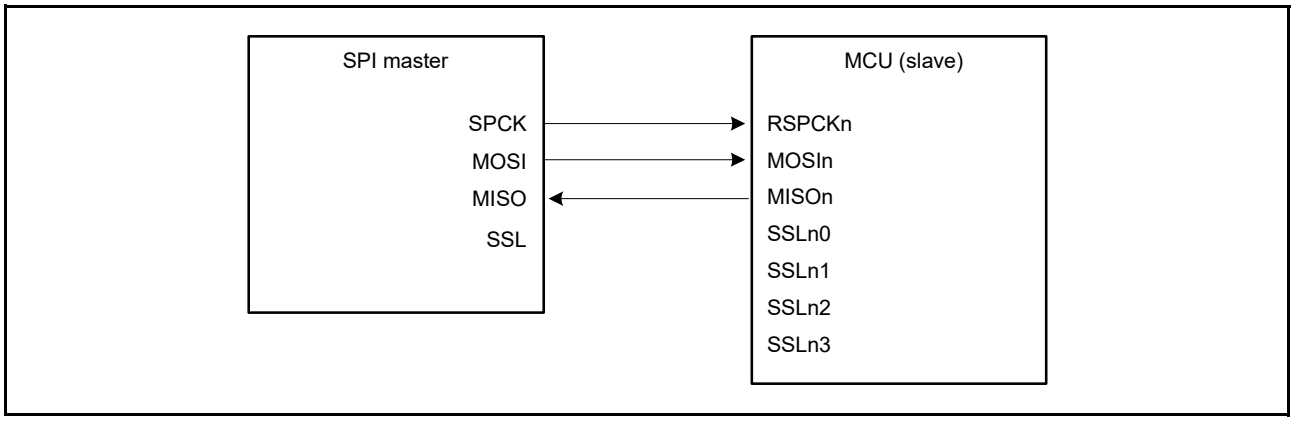


Figure 31.12 Configuration example of master and slave in clock synchronous mode with the MCU as a slave and CPHA = 1

31.3.4 Data Format

The data format of the SPI depends on the settings in the SPI Command Register m (SPCMDm) (m = 0 to 7) and the Parity Enable bit in SPI Control Register 2 (SPCR2.SPPE). Regardless of whether the ordering is MSB- or LSB-first, the SPI treats the range from the LSB bit in the SPI Data Register (SPDR/SPDR_HA) to the bit associated with the selected data length, as transfer data.

This section shows the format of one frame of data before or after transfer.

(a) Data format with parity disabled

When parity is disabled, transmission or reception of data proceeds with the bit length selected in the SPI data length setting bits in SPI Command Register m (SPCMDm.SPB[3:0]).

(b) Data format with parity enabled

When parity is enabled, transmission or reception of data proceeds with the bit length selected in the SPI data length setting bits in the SPI Command Register m (SPCMDm.SPB[3:0]). In this case, however, the last bit is a parity bit.

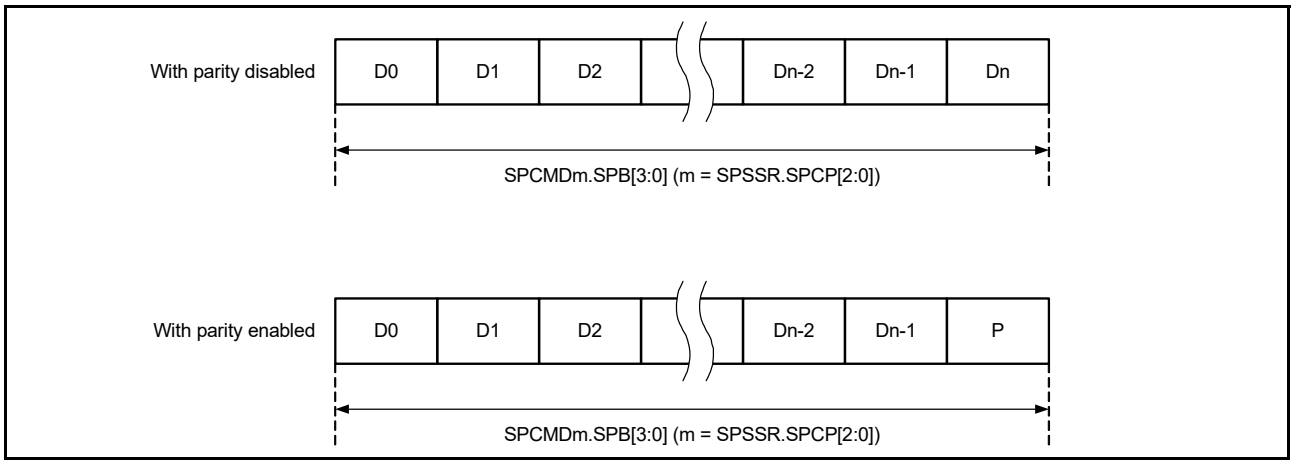


Figure 31.13 Data format with parity disabled and enabled

31.3.4.1 Operation when parity is disabled (SPCR2.SPPE = 0)

When parity is disabled, data for transmission is copied to the shift register with no pre-processing. This section describes the connection between the SPI Data Register (SPDR/SPDR_HA) and the shift register in terms of the combination of MSB- or LSB-first order and data length.

(1) MSB-first transfer with 32-bit data

Figure 31.14 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity disabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T31 to T30, and continuing to T00, in that order.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When R31 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

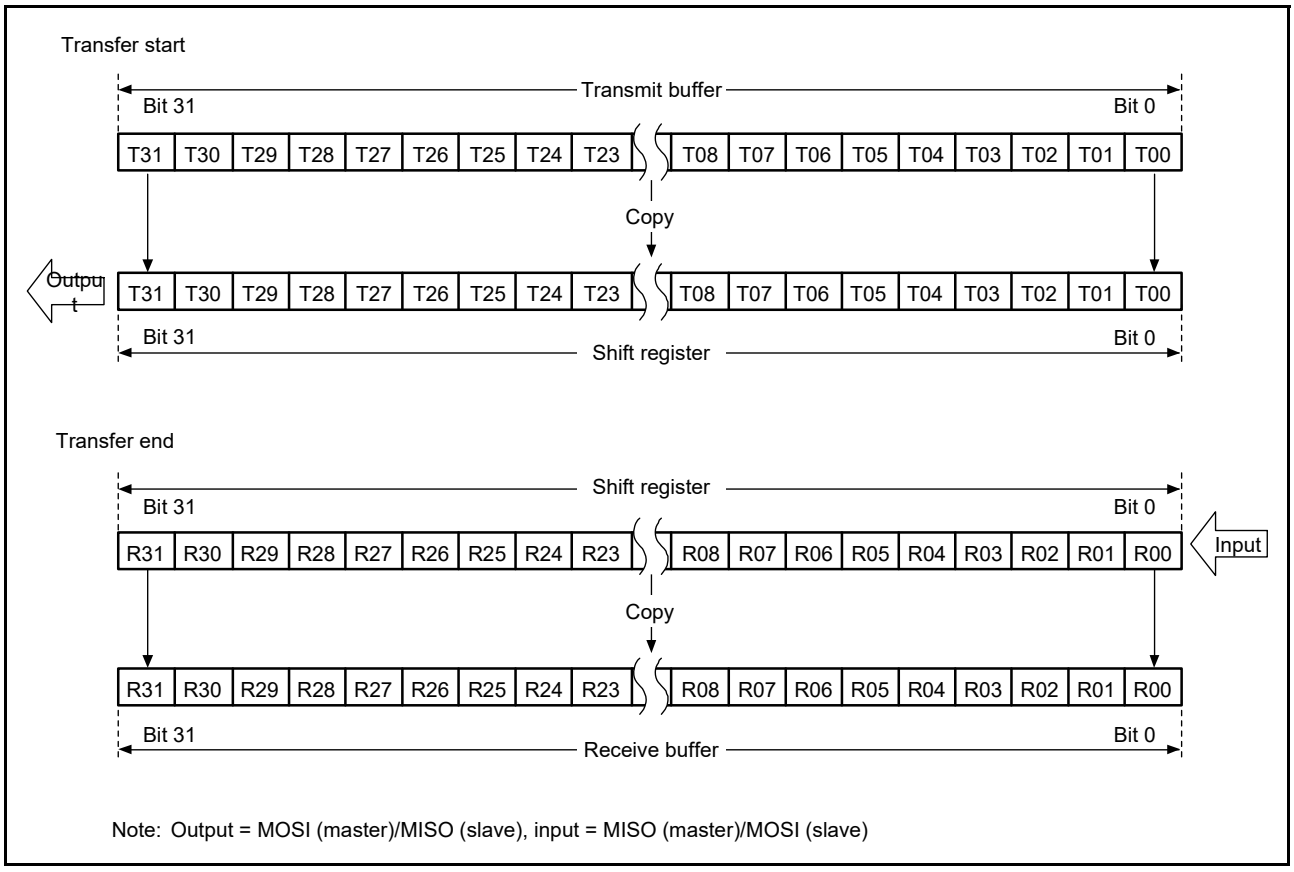


Figure 31.14 MSB-first transfer with 32-bit data and parity disabled

(2) MSB-first transfer with 24-bit data

Figure 31.15 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity disabled, an SPI data length of 24 bits, and MSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T23 to T22, and continuing to T00, in that order.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R23 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.

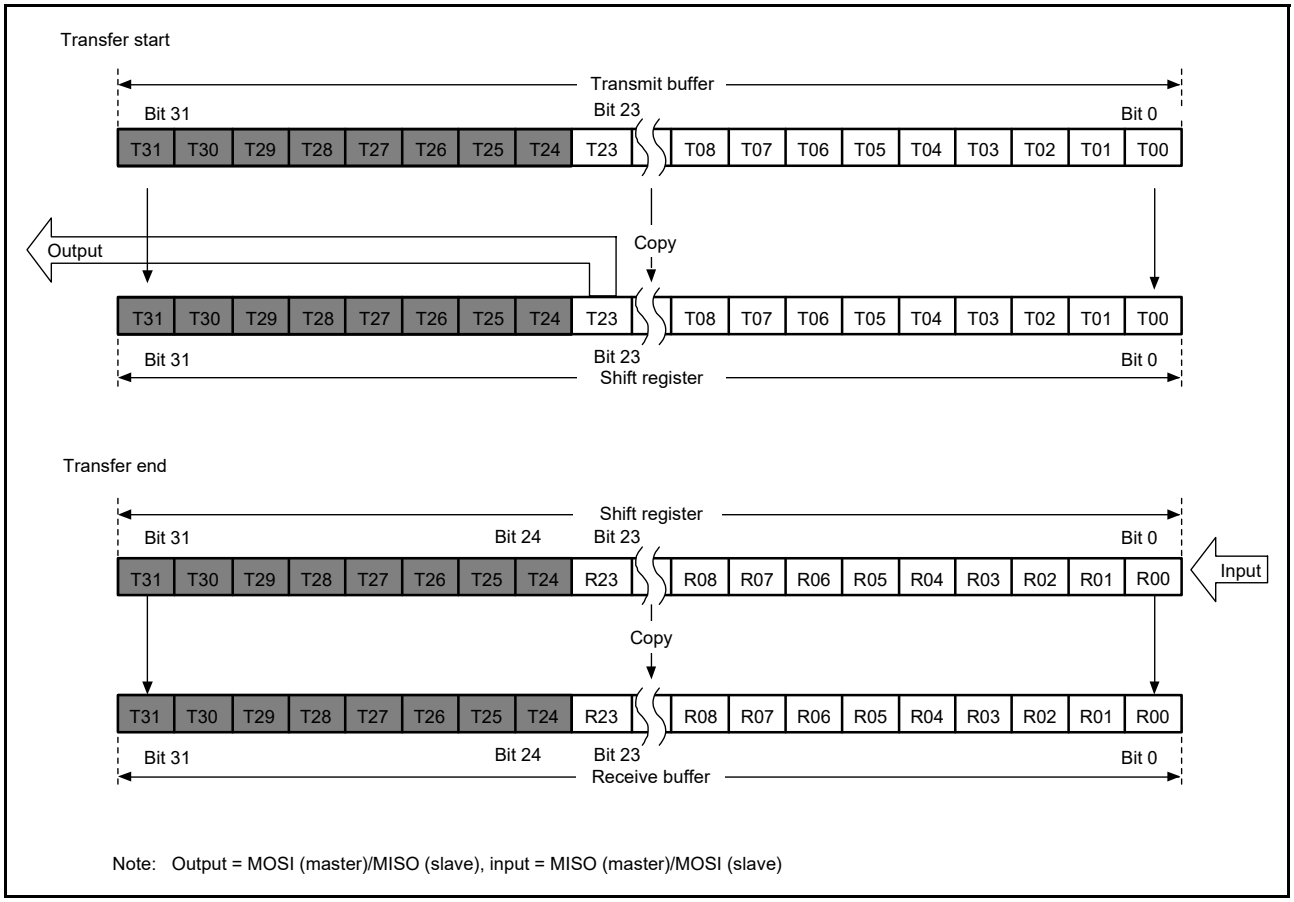


Figure 31.15 MSB-first transfer with 24-bit data and parity disabled

(3) LSB-first transfer with 32-bit data

Figure 31.16 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission is shifted out from the shift register from T00 to T01, and continuing to T3, in that order.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R00 to R31 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

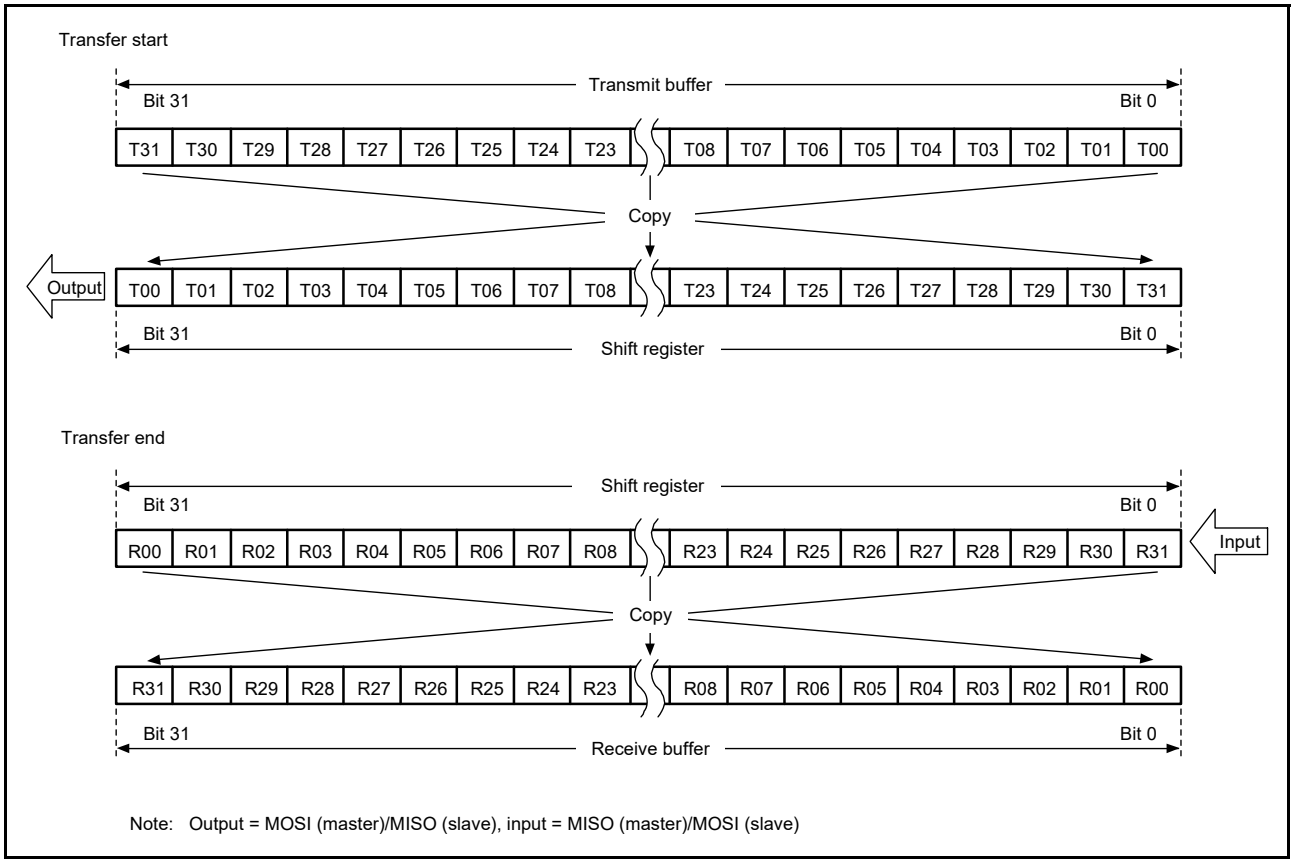


Figure 31.16 LSB-first transfer with 32-bit data and parity disabled

(4) LSB-first transfer with 24-bit data

Figure 31.17 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity disabled, an SPI data length of 24 bits, and LSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission is shifted out from the shift register from T00 to T01, and continuing to T23, in that order.

In reception, received data is shifted in bit-by-bit through bit [8] of the shift register. When the R00 to R23 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to the T31 to T24 bits at the time of transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.

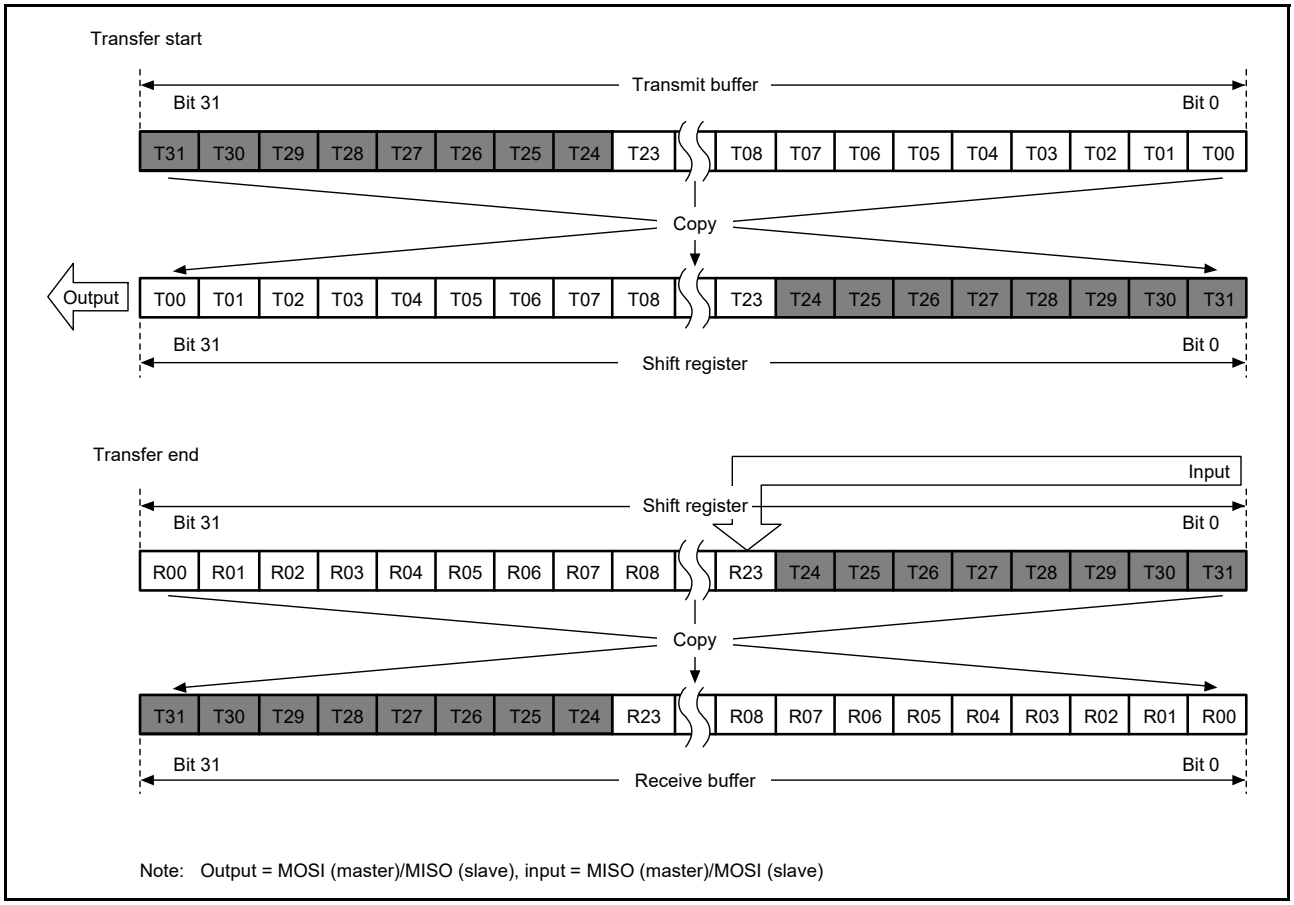


Figure 31.17 LSB-first transfer with 24-bit data and parity disabled

31.3.4.2 Operation when parity is enabled (SPCR2.SPPE = 1)

When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB-first transfer with 32-bit data

Figure 31.18 shows the transfer operation of the SPI Data Register (SPDR) and the shift register with parity enabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted in the order T31, T30, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R31 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, data from R31 to P is checked for parity.

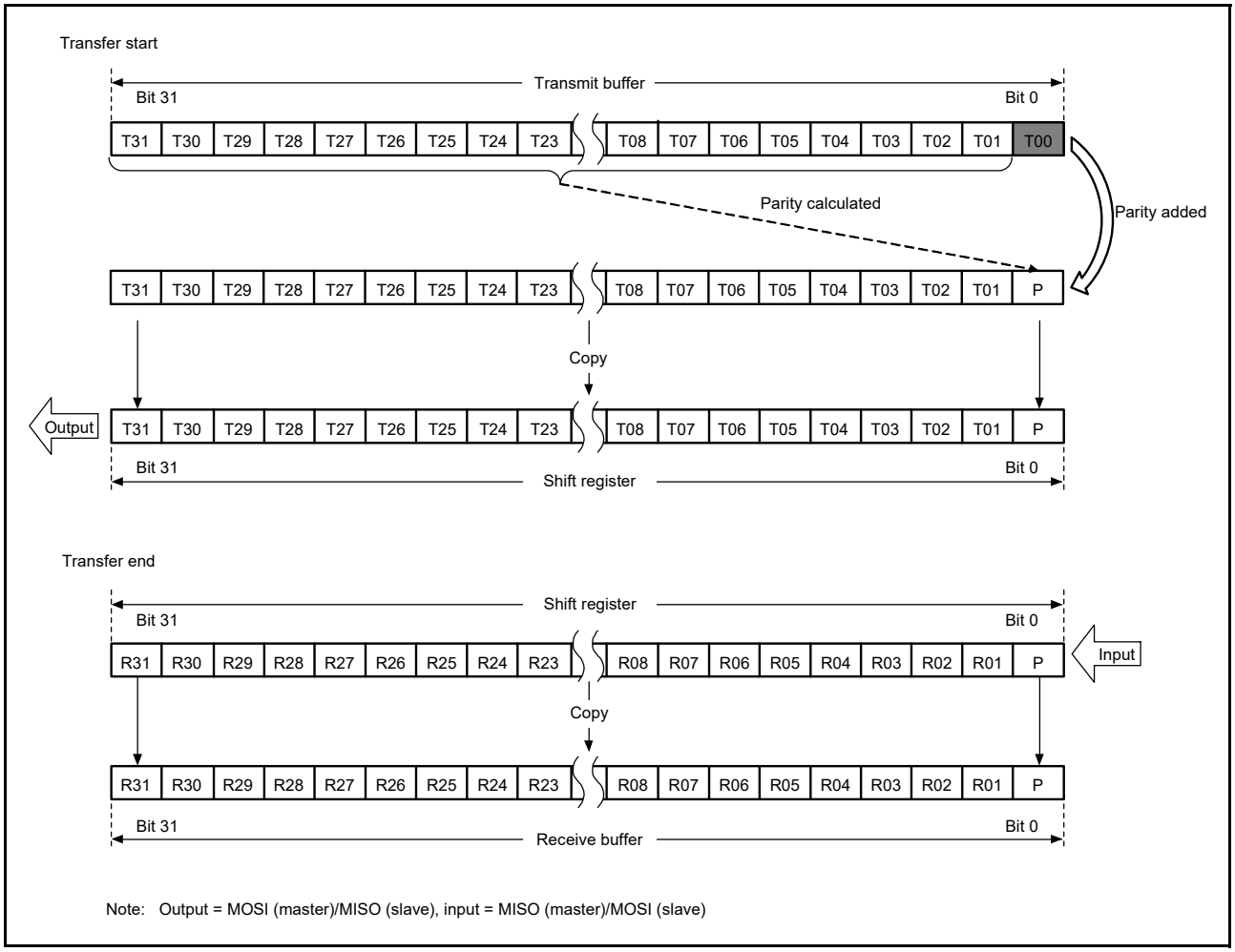


Figure 31.18 MSB-first transfer with 32-bit data and parity enabled

(2) MSB-first transfer with 24-bit data

Figure 31.19 shows the transfer operation of the SPI Data Register (SPDR) and the shift register with parity enabled, an SPI data length of 24 bits, and MSB-first selected.

In transmission, the value of the parity bits (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted in the order T23, T22, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R23 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. After data is copied to the shift register, data from R23 to P is checked for parity. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to the T31 to T24 bits at the time of transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.

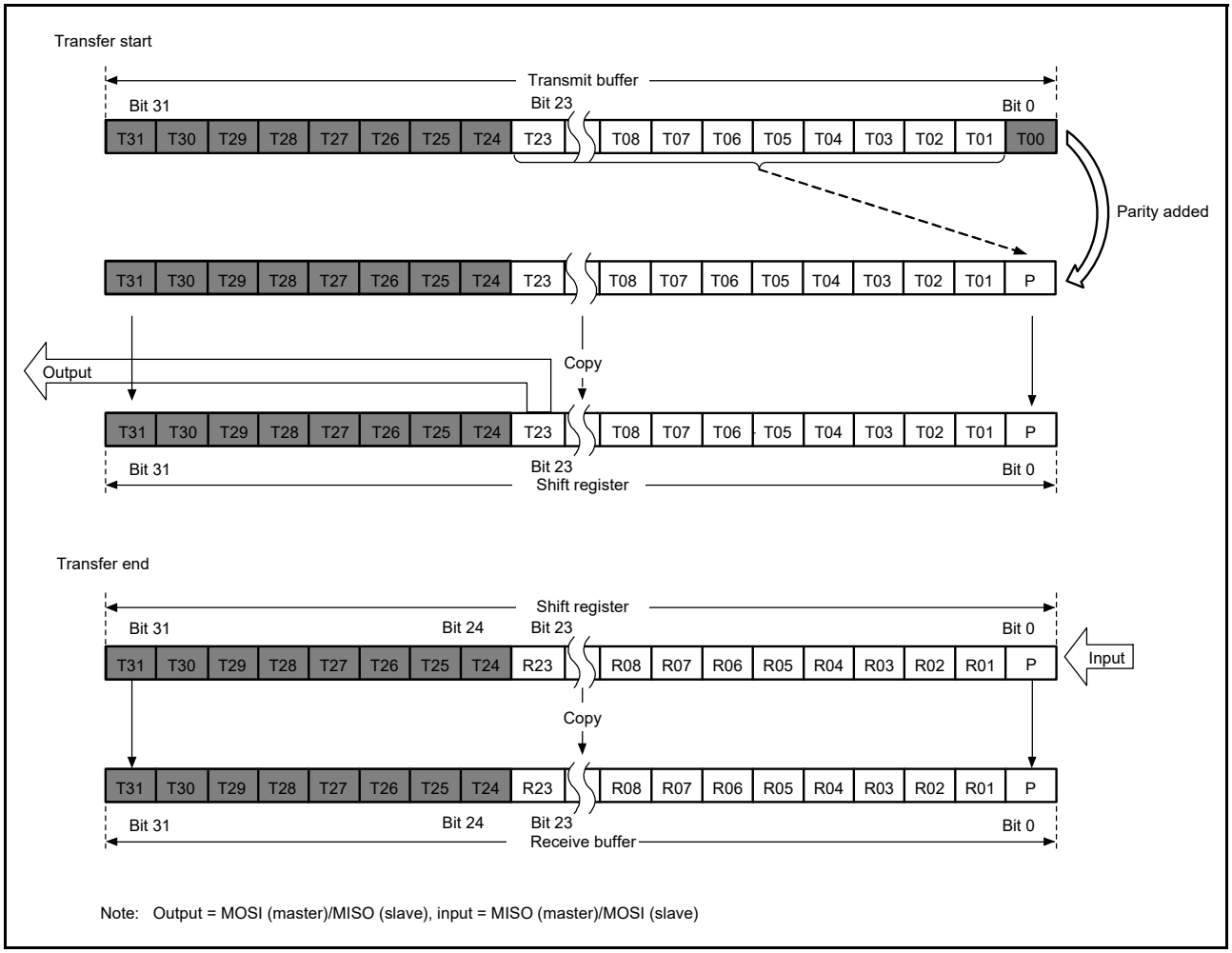


Figure 31.19 MSB-first transfer with 24-bit data and parity enabled

(3) LSB-first transfer with 32-bit data

Figure 31.20 shows the transfer operation of the SPI Data Register (SPDR) and the shift register with parity enabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from the T30 to T00 bits. This replaces the final bit, T31, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T30, and P.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. After data is copied to the shift register, the data from R00 to P is checked for parity.

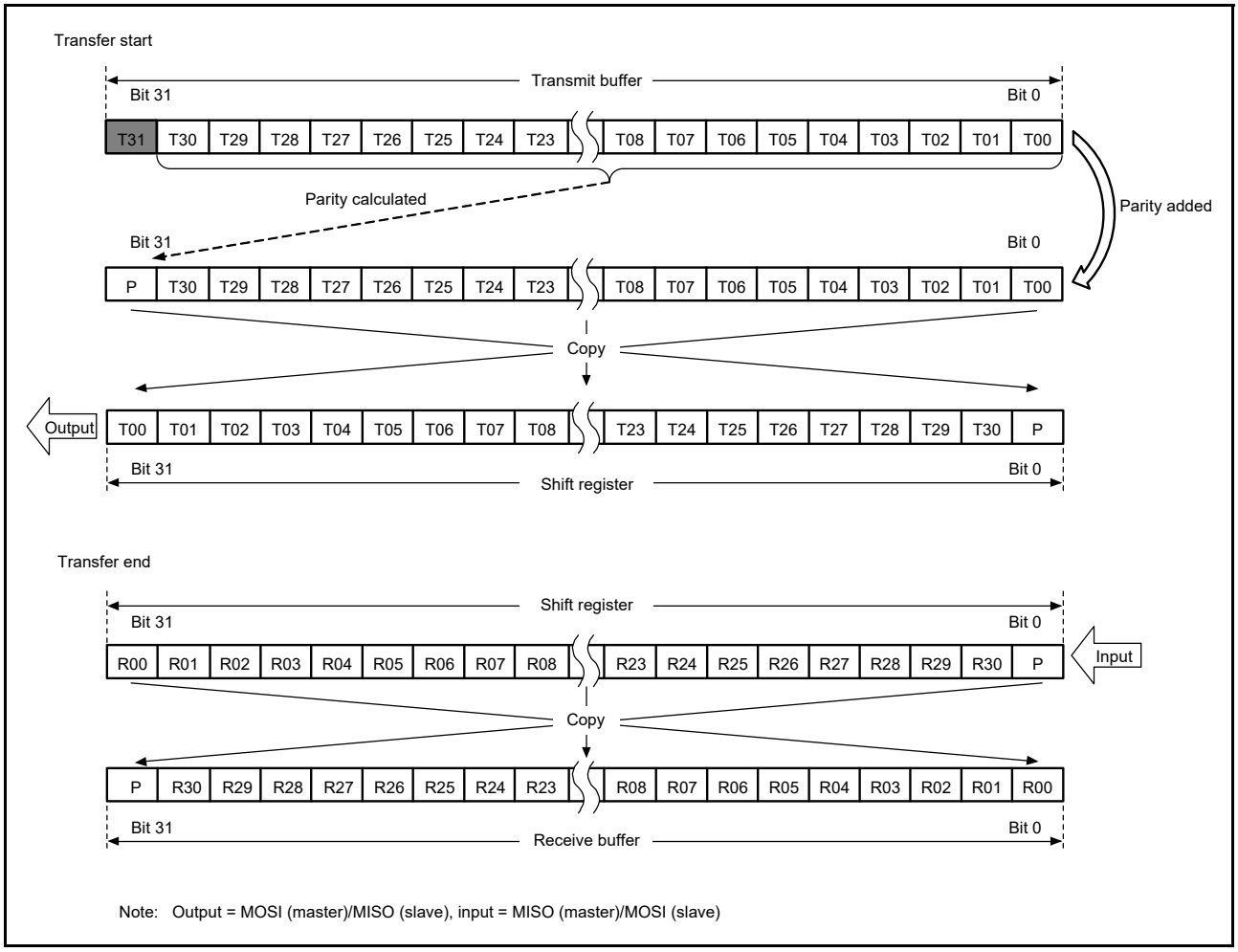


Figure 31.20 LSB-first transfer with 32-bit data and parity enabled

(4) LSB-first transfer with 24-bit data

Figure 31.21 shows the transfer operation of the SPI Data Register (SPDR) and the shift register with parity enabled, an SPI data length of 24 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from the T22 to T00 bits. This replaces the final bit, T23, and the whole is copied to the shift register. Data is transmitted in the order T00, T01, …, T22, and P.

In reception, received data is shifted in bit-by-bit through bit [8] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to the T31 to T24 bits at transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.

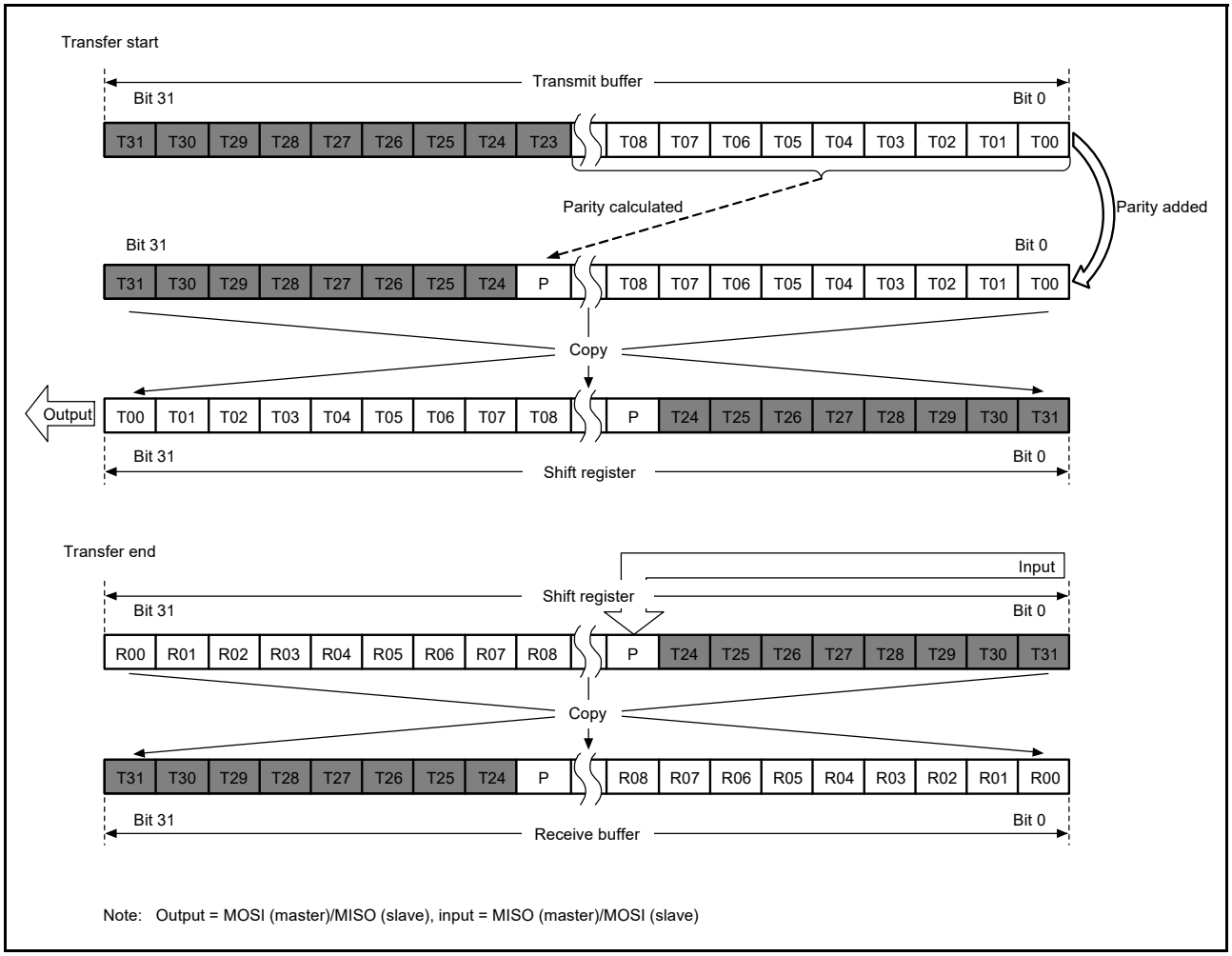


Figure 31.21 LSB-first transfer with 24-bit data and parity enabled

31.3.5 Transfer Format

31.3.5.1 Transfer format when CPHA = 0

Figure 31.22 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 0. Do not perform clock synchronous operation (SPCR.SPMS = 1) when the SPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In Figure 31.22, RSPCKn (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0, and RSPCKn (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI settings. For details, see section 31.3.2, Controlling the SPI Pins.

When the SPCMDm.CPHA bit is 0, the driving of valid data to the MOSIn and MISOn signals begins at an SSLni signal assertion. The first RSPCKn signal change that occurs after the SSLni signal assertion becomes the first transfer data fetch. After this, data is sampled every 1 RSPCK cycle. The change timing for the MOSIn and MISOn signals is 1/2 RSPCK cycles after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCK signal operation timing as it only affects the signal polarity.

t1 denotes the RSPCK delay, the period from an SSLni signal assertion to RSPCKn oscillation. t2 denotes the SSL negation delay, the period from the termination of RSPCKn oscillation to an SSLni signal negation. t3 denotes the next-access delay, the period in which SSLni signal assertion is suppressed for the next transfer after the end of the serial transfer. t1, t2, and t3 are controlled by a master device running on the SPI system. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 31.3.10.1, Master mode operation.

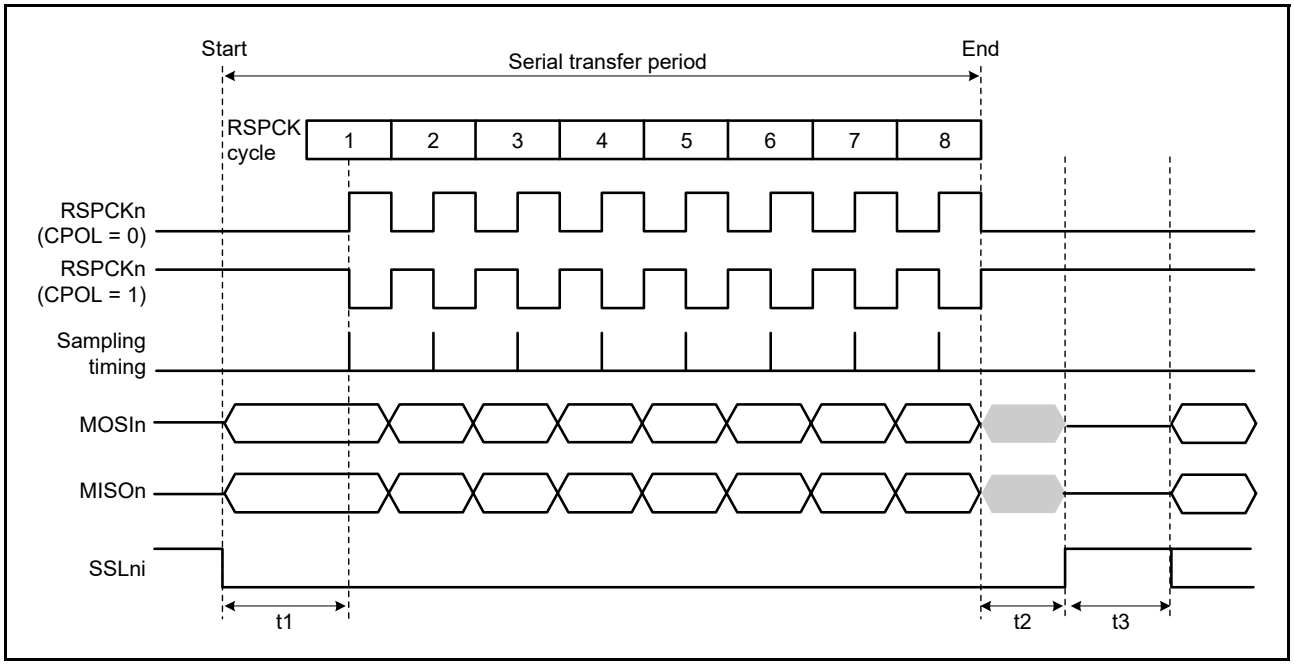


Figure 31.22 SPI transfer format when CPHA = 0

31.3.5.2 When CPHA = 1

Figure 31.23 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLni signals are not used, and only the three signals RSPCKn, MOSIn, and MISOn handle communications. In Figure 31.23, RSPCK (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0, and RSPCK (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI mode (master or slave). For details, see section 31.3.2, Controlling the SPI Pins.

When the SPCMDm.CPHA bit is 1, the driving of invalid data to the MISOn signal begins at an SSLni signal assertion. The output of valid data to the MOSIn and MISOn signals begins at the first RSPCKn signal change that occurs after the SSLni signal assertion. After this, data is updated every 1 RSPCK cycle. The transfer data fetch timing is 1/2 RSPCK cycles after the data update timing. The SPCMDm.CPOL bit setting does not affect the RSPCKn signal operation timing. It only affects the signal polarity.

t1, t2, and t3 are the same as those when CPHA = 0. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 31.3.10.1, Master mode operation.

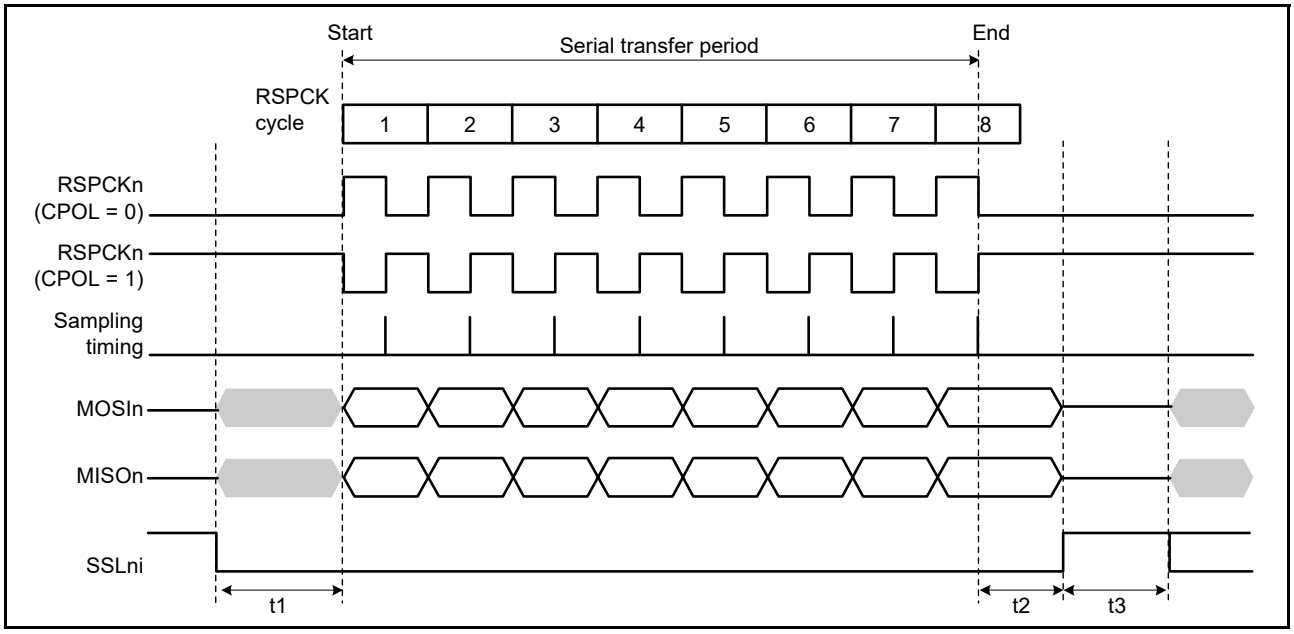


Figure 31.23 SPI transfer format when CPHA = 1

31.3.6 Data Transfer Modes

Full-duplex synchronous serial communications or transmit operations can only be selected in the Communications Operating Mode Select bit (SPCR.TXMD). The SPDR/SPDR_HA access shown in Figure 31.24 and Figure 31.25 indicate the condition of access to the register, where W denotes a write cycle.

31.3.6.1 Full-duplex synchronous serial communications (SPCR.TXMD = 0)

Figure 31.24 shows an example of operation where the Communications Operating Mode Select bit (SPCR.TXMD) is set to 0. In this example, the SPI performs an 8-bit serial transfer in which the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

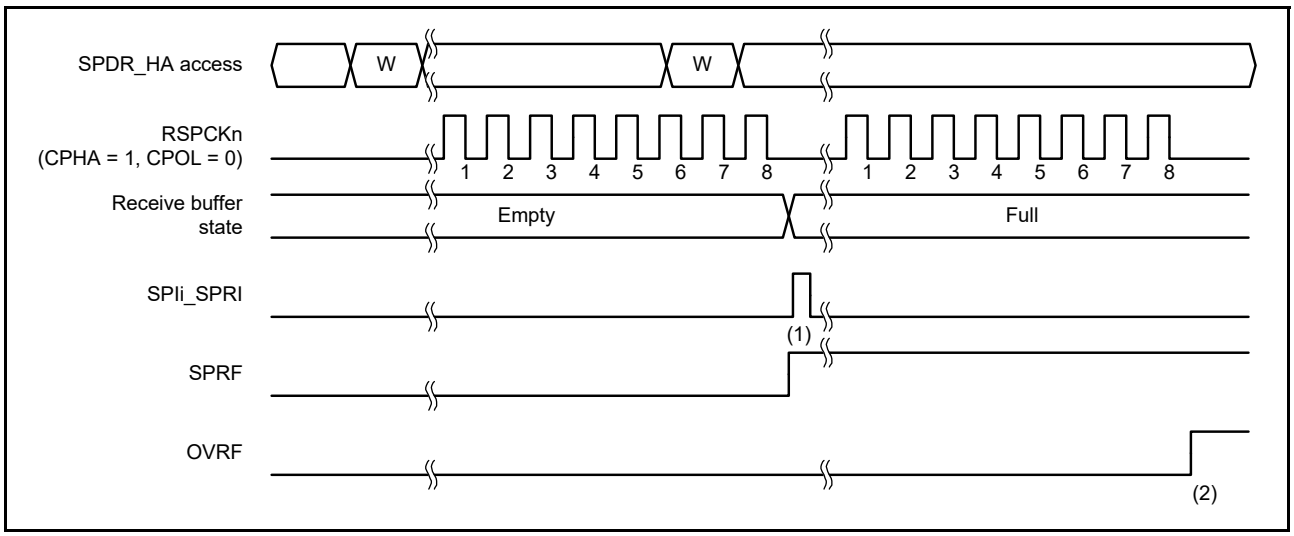


Figure 31.24 Operation example when SPCR.TXMD = 0

The operation of the flags at timings (1) and (2) in Figure 31.24 is as follows:

1. When a serial transfer ends with the SPDR_HA receive buffer empty, the SPI generates a receive buffer full interrupt request (SPIi_SPRI), the SPI sets the SPSR.SPRF flag to 1, and the received data is copied in the shift register to the receive buffer.

2. When a serial transfer ends with the SPDR_HA receive buffer holding data that was received in the previous serial transfer, the SPI sets the SPSR.OVRF flag to 1, and discards the received data in the shift register.

31.3.6.2 Transmit-only operations (SPCR.TXMD = 1)

Figure 31.25 shows an example of operation where the Communications Operating Mode Select bit (SPCR.TXMD) is set to 1. In this example, the SPI performs an 8-bit serial transfer in which the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

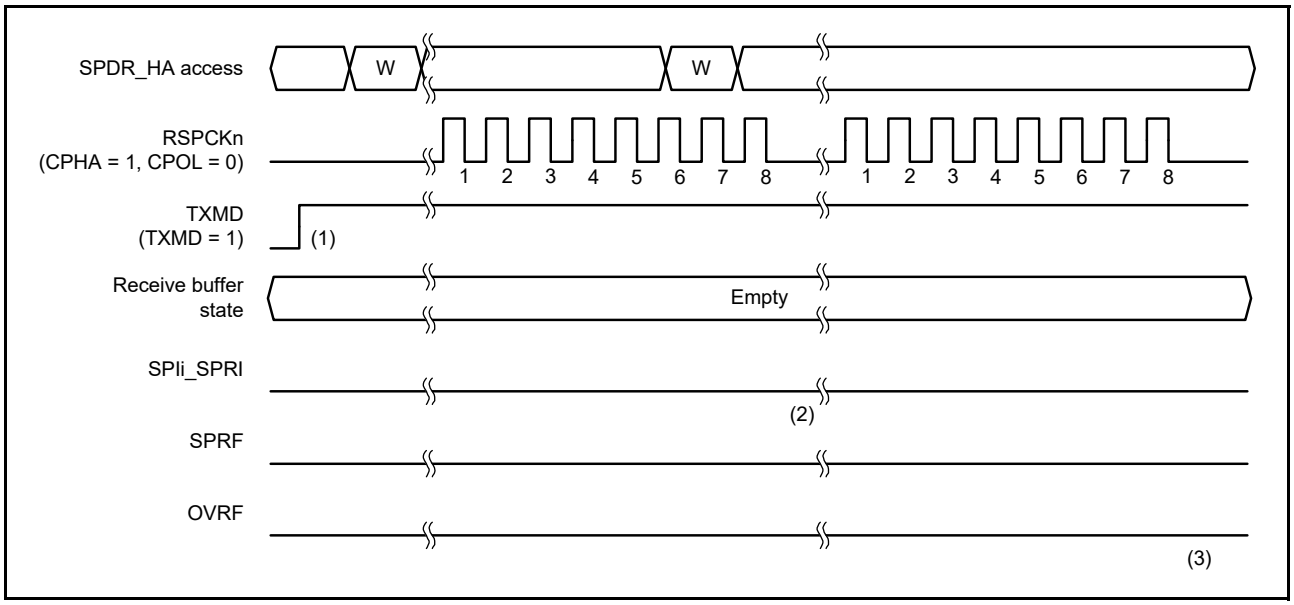


Figure 31.25 Operation example when SPCR.TXMD = 1

The operation of the flags at timings (1) to (3) in Figure 31.25 is as follows:

1. Make sure there is no data left in the receive buffer (SPSR.SPRF flag is 0) and the SPSR.OVRF flag is 0 before entering the transmit-only mode (SPCR.TXMD = 1).
2. When a serial transfer ends with the SPDR_HA receive buffer empty, if the transmit-only mode is selected (SPCR.TXMD = 1), the SPSR.SPRF flag remains 0, and the SPI does not copy the data in the shift register to the receive buffer.
3. Because the SPDR_HA receive buffer does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag remains 0, and the data in the shift register is not copied to the receive buffer.

In transmit-only mode (SPCR.TXMD = 1), the SPI transmits but does not receive data. Therefore, the SPSR.SPRF and SPSR.OVRF flags remain 0 at timings (1) to (3).

31.3.7 Transmit Buffer Empty and Receive Buffer Full Interrupts

Figure 31.26 and Figure 31.27 show operation examples of the transmit buffer empty interrupt (SPIi_SPTI) and the receive buffer full interrupt (SPIi_SPRI). The register accesses shown in these figures indicate the conditions of access to the SPDR_HA register, where W denotes a write cycle and R a read cycle. In Figure 31.26, the SPI performs an 8-bit serial transfer when SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 0, and the SPCMDm.CPOL bit is 0.

In Figure 31.27, the SPI performs an 8-bit serial transfer in which SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

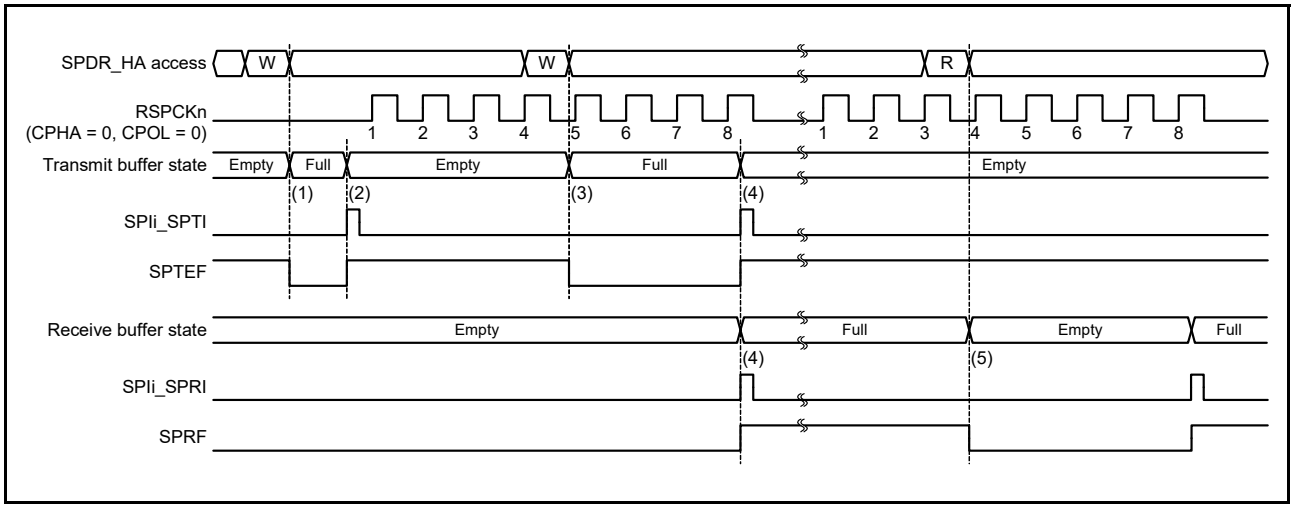


Figure 31.26 Operation example of SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 0 and CPOL = 0

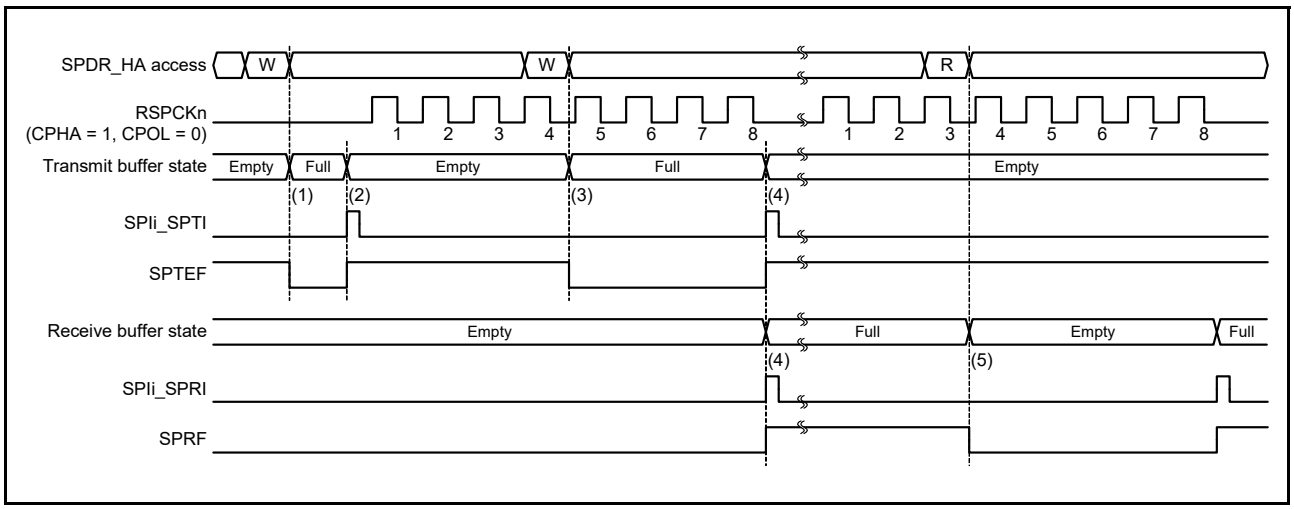


Figure 31.27 Operation example of SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 1 and CPOL = 0

The operation of the SPI at timings (1) to (5) in Figure 31.27 is as follows:

1. When transmit data is written to SPDR_HA with the transmit buffer of SPDR_HA empty and data for the next transfer not set, the SPI writes data to the transmit buffer and clears the SPSR.SPTEF flag to 0.
2. If the shift register is empty, the SPI copies the data in the transmit buffer to the shift register, generates a transmit buffer empty interrupt request (SPIi_SPTI), and sets the SPSR.SPTEF flag to 1. How a serial transfer is started depends on the SPI mode. For details, see section 31.3.10, SPI Operation, and section 31.3.11, Clock Synchronous Operation.
3. When transmit data is written to SPDR_HA either by the transmit buffer empty interrupt routine, or by the processing of the transmit buffer empty using the SPTEF flag, the SPI writes data to the transmit buffer and clears the SPTEF flag to 0. Because the data being transferred serially is stored in the shift register, the SPI does not copy the data in the transmit buffer to the shift register.
4. When the serial transfer ends with the SPDR_HA receive buffer empty, the SPI copies the receive data in the shift register to the receive buffer, generates a receive buffer full interrupt request (SPIi_SPRI), and sets the SPRF flag to 1. Because the shift register becomes empty on completion of the serial transfer, if the transmit buffer is full before the serial transfer ended, the SPI sets the SPTEF flag to 1 and copies data in the transmit buffer to the shift register. Even when received data is not copied from the shift register to the receive buffer in an overrun error status, on completion of the serial transfer, the SPI determines that the shift register is empty, so data transfer from the transmit buffer to the shift register is enabled.

5. When SPDR_HA is read either by the receive buffer full interrupt routine or by the processing of the receive buffer full interrupt using the SPRF flag, the receive data can be read.

If SPDR_HA is written to when the transmit buffer holds untransmitted data (SPTEF flag is 0), the SPI does not update data in the transmit buffer. When writing to SPDR_HA, make sure to use either a transmit buffer empty interrupt request or to process a transmit buffer empty interrupt using the SPTEF flag. To use a transmit buffer empty interrupt, set the SPTIE bit in SPCR to 1. If the SPI function is disabled (SPCR.SPE bit is 0), set the SPTIE bit to 0.

When serial transfer ends with the receive buffer full (SPRF flag is 1), the SPI does not copy data from the shift register to the receive buffer, and detects an overrun error (see section 31.3.8, Error Detection). To prevent a receive data overrun error, read the received data using a receive buffer full interrupt request before the next serial transfer ends. To use an SPI receive buffer full interrupt, set the SPCR.SPRIE bit to 1.

Transmission and reception interrupts or the associated IELSRn.IR flags in the ICU, where n is the interrupt vector number, can be used to confirm the states of the transmit and receive buffers. Similarly, the SPTEF and SPRF flags can be used to confirm the states of the transmit and receive buffers. See section 13, Interrupt Controller Unit (ICU) for the interrupt vector numbers.

31.3.8 Error Detection

In normal SPI serial transfer, data written to the SPDR/SPDR_HA transmit buffer is transmitted, and received data can be read from the receive buffer of SPDR/SPDR_HA. If access is made to SPDR/SPDR_HA, an abnormal transfer might occur, depending on the status of the transmit or receive buffer, or the status of the SPI at the beginning or end of the serial transfer.

If an abnormal transfer occurs, the SPI detects the event as an underrun error, overrun error, parity error, or mode fault error. Table 31.8 lists the relationship between non-normal transfer operations and the SPI error detection function.

Table 31.8 Relationship between non-normal transfer operations and SPI error detection function

Operation	Occurrence condition	SPI operation	Error detection
1	SPDR/SPDR_HA is written when the transmit buffer is full	• The contents of the transmit buffer are kept • Write data is missing.	None
2	SPDR/SPDR_HA is read when the receive buffer is empty	The contents of the receive buffer and previously received data are output	None
3	Serial transfer is started in slave mode when the SPI is not able to transmit data	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOA output signal is stopped • SPI function is disabled.	Underrun error
4	Serial transfer terminates when the receive buffer is full	• The contents of the receive buffer are kept • Receive data is missing.	Overrun error
5	An incorrect parity bit is received during full-duplex synchronous serial communications with the parity function enabled	The parity error flag is asserted	Parity error
6	The SSLn0 input signal is asserted when the serial transfer is idle in multi-master mode	• Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped • SPI function is disabled.	Mode fault error
7	The SSLn0 input signal is asserted during serial transfer in multi-master mode	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped • SPI function is disabled.	Mode fault error
8	The SSLn0 input signal is negated during serial transfer in slave mode	• Serial transfer is suspended • Missing transmit/receive data • Driving of the MISOn output signal is stopped • SPI function is disabled.	Mode fault error

In operation 1 described in Table 31.8, the SPI does not detect an error. To prevent data omission during writes to SPDR/SPDR_HA, the writes to SPDR/SPDR_HA must be executed using a transmit buffer empty interrupt request (when SPSR.SPTEF flag is 1). Similarly, the SPI does not detect an error in operation 2. To prevent extraneous data from

being read, SPDR/SPDR_HA reads must be executed using an SPI receive buffer full interrupt request (when SPSR.SPRF flag is 1).

For information on the other errors, see the following sections:

- Underrun errors, indicated in operation 3, see section 31.3.8.4, Underrun errors
- Overrun errors, indicated in operation 4, see section 31.3.8.1, Overrun errors
- Parity errors, indicated in operation 5, see section 31.3.8.2, Parity errors
- Mode fault error, indicated in operations 6 to 8, see section 31.3.8.3, Mode fault errors.

For the transmit and receive interrupts, see section 31.3.7, Transmit Buffer Empty and Receive Buffer Full Interrupts.

31.3.8.1 Overrun errors

If a serial transfer ends when the receive buffer of SPDR/SPDR_HA is full, the SPI detects an overrun error and sets the SPSR.OVRF flag to 1. When the OVRF flag is 1, the SPI does not copy data from the shift register to the receive buffer, so the data before the error occurrence is saved in the receive buffer. To set the OVRF flag to 0, write 0 to it after the CPU reads SPSR with the OVRF flag set to 1.

Figure 31.28 shows an example operation of the OVRF and SPRF flags. The SPSR and SPDR_HA accesses shown in Figure 31.28 indicate the condition of accesses to the register, where W denotes a write cycle and R a read cycle. In the example, the SPI performs an 8-bit serial transfer in which the SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

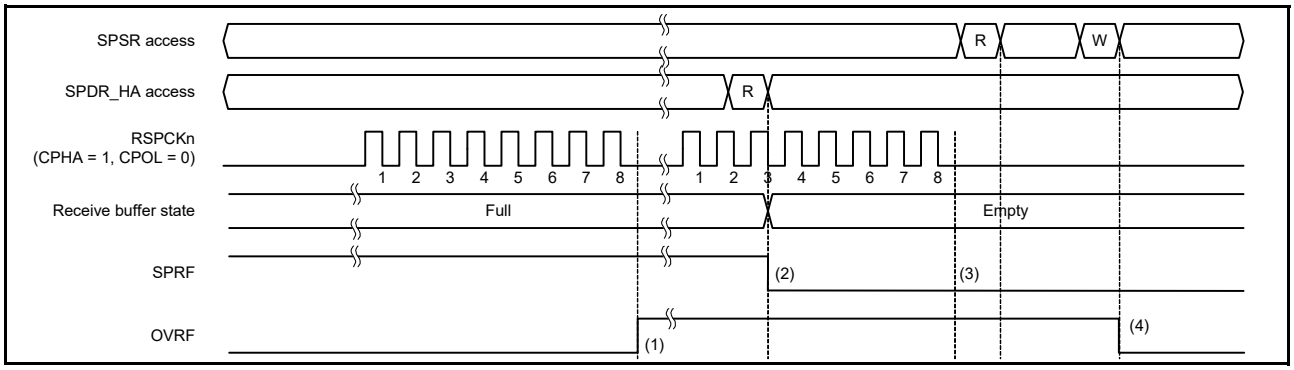


Figure 31.28 Operation example of OVRF and SPRF flags

The operation of the flags at timings (1) to (4) in Figure 31.28 is as follows:

1. If a serial transfer terminates with the SPRF flag set to 1 (receive buffer full), the SPI detects an overrun error, and sets the OVRF flag to 1. The SPI does not copy the data in the shift register to the receive buffer. Even when the SPPE bit is 1, parity errors are not detected. In master mode, the SPI copies the value of the SPCMDm pointer to the SPSSR.SPECM[2:0] bits.
2. When SPDR_HA is read, the SPI outputs the data in the receive buffer. The SPRF flag is then set to 0. The receive buffer becoming empty does not set the OVRF flag to 0.
3. If the serial transfer ends with the OVRF flag set to 1 (overrun error occurred), the SPI does not copy data in the shift register to the receive buffer (the SPRF flag is not set to 1). A receive buffer full interrupt is not generated. Even when the SPPE bit is 1, parity errors are not detected. In master mode, the SPI does not update the SPSSR.SPECM[2:0] bits. When an overrun error occurs and the SPI does not copy the received data from the shift register to the receive buffer, on termination of the serial transfer, the SPI determines that the shift register is empty. This enables data transfer from the transmit buffer to the shift register.
4. If 0 is written to the OVRF flag after SPSR is read when the OVRF flag is 1, the OVRF flag is set to 0.

The occurrence of an overrun can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. When executing a serial transfer, make sure that overrun errors are detected early, for instance, by reading SPSR immediately after SPDR_HA is read. In master mode, the value of the pointer to the SPCMDm register on the error occurrence can be checked by reading the SPSSR.SPECM[2:0] bits.

If an overrun error occurs and the OVRF flag is set to 1, normal reception operations cannot be performed until the OVRF flag is set to 0.

When the RSPCK auto-stop function is enabled in master mode, an overrun error does not occur. Figure 31.29 and Figure 31.30 show the clock stop waveform when a serial transfer continues while the receive buffer is full in master mode.

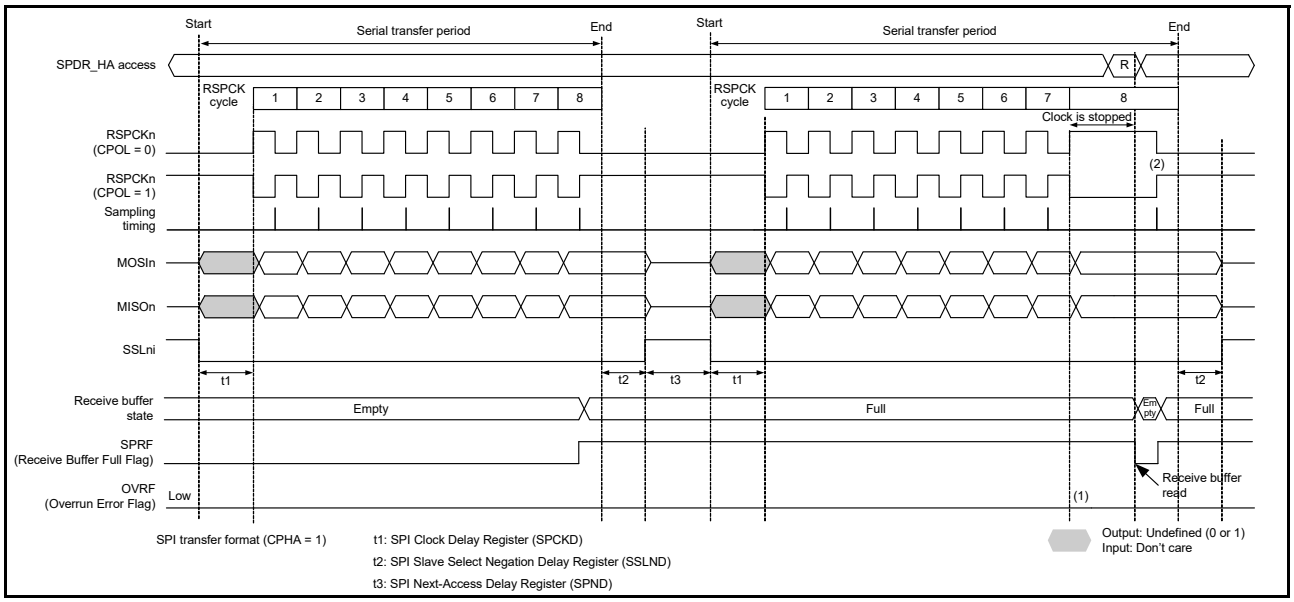


Figure 31.29 Clock stop waveform when serial transfer continues while receive buffer is full in master mode with CPHA = 1

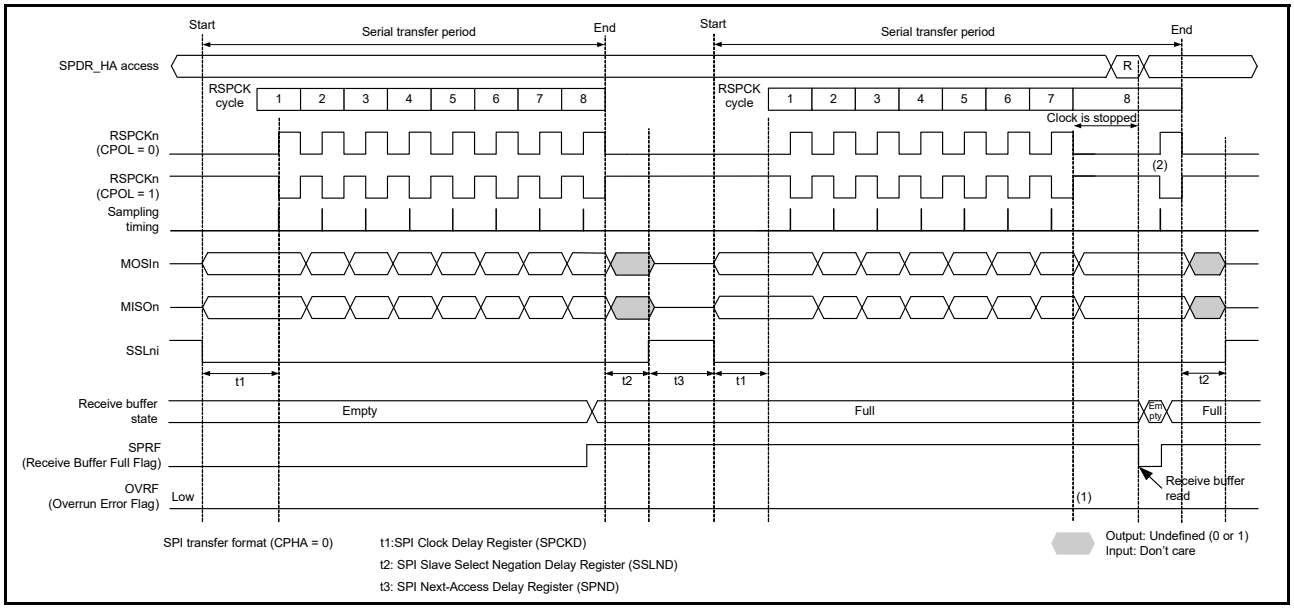


Figure 31.30 Clock stop waveform when serial transfer continues while receive buffer is full in master mode with CPHA = 0

The operation of the flags at timings (1) and (2) in Figure 31.29 and Figure 31.30 is as follows:

1. When the receive buffer is full, an overrun error does not occur because the RSPCK clock is stopped.
2. If SPDR_HA is read while the clock is stopped, data in the receive buffer can be read. The RSPCK clock restarts after reading the receive buffer (after SPSR.SPRF is set to 0).

31.3.8.2 Parity errors

When full-duplex synchronous serial communication is performed with the SPCR.TXMD bit set to 0 and the SPCR2.SPPE bit set to 1, the SPI checks for parity errors when serial transfer ends. On detecting a parity error in the received data, the SPI sets the SPSR.PERF flag to 1. Because the SPI does not copy data in the shift register to the receive buffer when the SPSR.OVRF flag is set to 1, parity error detection is not performed for the received data. To set the PERF flag to 0, write 0 to the PERF flag after the SPSR register is read with the PERF flag set to 1.

Figure 31.31 shows an example operation of the OVRF and PERF flags. The SPSR access shown in Figure 31.31 indicates the condition of access to the SPSR register, where W denotes a write cycle, and R a read cycle. In the example, full-duplex synchronous serial communication is performed while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1. The SPI performs an 8-bit serial transfer in which SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

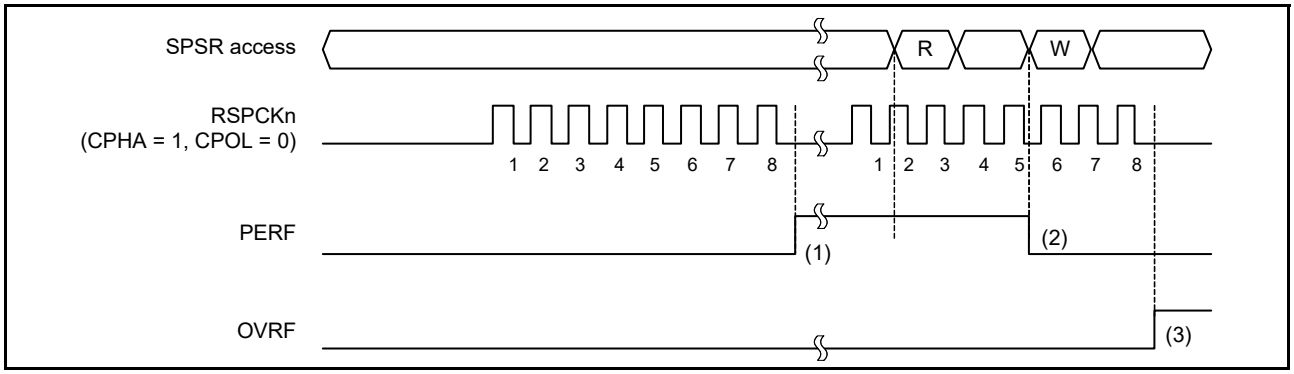


Figure 31.31 Operation example of the PERF flag

The operation of the flags at timings (1) to (3) in Figure 31.31 is as follows:

1. If a serial transfer terminates with the SPI not detecting an overrun error, the SPI copies the data in the shift register to the receive buffer. The SPI checks the received data at this time and sets the PERF flag to 1 if a parity error is detected. In master mode, the SPI copies the value of the SPCMDm pointer to the SPSSR.SPECM[2:0] bits.
2. If 0 is written to the PERF flag after the SPSR register is read when the PERF flag is 1, the PERF flag is set to 0.
3. When the SPI detects an overrun error and serial transfer is terminated, the data in the shift register is not copied to the receive buffer. The SPI does not perform parity error detection at this time.

Parity errors can be checked by reading the SPSR register or by using an SPI error interrupt and reading the SPSR register. When executing a serial transfer, make sure that parity errors are detected early, for instance by reading SPSR errors. When the SPI is in master mode, the pointer value to the SPCMDm register at the error occurrence can be checked by reading the SPSSR.SPECM[2:0] bits.

31.3.8.3 Mode fault errors

The SPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1. If the active level is input for the SSLn0 input signal of the SPI in multi-master mode, the SPI detects a mode fault error regardless of the status of the serial transfer, and sets the SPSR.MODF flag to 1. On detecting the mode fault error, the SPI copies the value of the SPCMDm pointer to the SPSSR.SPECM[2:0] bits. The active level of the SSLn0 signal is determined by the SSLP.SSL0P bit.

When the MSTR bit is 0, the SPI operates in slave mode. The SPI detects a mode fault error if the MODFEN bit of the SPI in slave mode is 1, and the SPMS bit is 0, and if the SSLn0 input signal is negated during the serial transfer period (from the time the driving of valid data is started to the time the final valid data is fetched).

On detecting a mode fault error, the SPI stops the driving of output signals and clears the SPCR.SPE bit to 0 (see section 31.3.9, Initializing the SPI). For multi-master configuration, detection of a mode fault error is used to stop the driving of output signals and the SPI function, which allows the master to be released.

The occurrence of a mode fault error can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting mode fault errors without using the SPI error interrupt requires polling of SPSR. When using

the SPI in master mode, the value of the pointer to the SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of a mode fault error, the MODF flag must be set to 0.

31.3.8.4 Underrun errors

When a serial transfer begins with the SPCR.MSTR bit set to 0 (slave mode), the SPCR.SPE bit is set to 1 and the transmission data not prepared, the SPI detects an underrun error. The SPI then sets the SPSR.MODF and SPSR.UDRF flags to 1. On detecting an underrun error, the SPI stops the driving of output signals and clears the SPCR.SPE bit to 0 (see section 31.3.9, Initializing the SPI).

The occurrence of an underrun error can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting underrun errors without using the SPI error interrupt requires polling of SPSR.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of an underrun error, the MODF flag must be set to 0.

31.3.9 Initializing the SPI

If 0 is written to the SPCR.SPE bit or if the SPI sets the SPE bit to 0 because it detected a mode fault error or an underrun error, the SPI disables the SPI function and initializes some of the module functions. When a system reset occurs, the SPI initializes all of the module functions. This section describes initialization by clearing of the SPCR.SPE bit, and by a system reset.

31.3.9.1 Initialization by clearing the SPE bit

When the SPCR.SPE bit is set to 0, the SPI initializes by:

- Suspending any serial transfer that is being executed
- Stopping the driving of output signals (Hi-Z) in slave mode
- Initializing the internal state of the SPI
- Initializing the transmit buffer of the SPI (SPSR.SPTEF flag is set to 1).

Initialization by clearing of the SPE bit does not initialize the control bits of the SPI. For this reason, the SPI can be started in the same transfer mode that is in use before initialization when the SPE bit is set to 1 again.

The SPRF, OVRF, MODF, PERF and UDRF flags in the SPSR register are not initialized, and the SPI Sequence Status Register (SPSSR) is not initialized. Therefore, even after the SPI is initialized, data from the receive buffer can be read to check the error status during an SPI transfer.

The transmit buffer is initialized to an empty state (SPSR.SPTEF flag is set to 1). Therefore, if the SPCR.SPTIE bit is set to 1 after SPI initialization, a transmit buffer empty interrupt is generated. When the SPI is initialized, to disable any transmit buffer empty interrupts, write 0 to the SPTIE bit simultaneously while writing 0 to the SPE bit.

31.3.9.2 Initialization by system reset

A system reset completely initializes the SPI by initializing all bits that control the SPI, the status bits, and the data registers, in addition to meeting the requirements described in section 31.3.9.1, Initialization by clearing the SPE bit.

31.3.10 SPI Operation

31.3.10.1 Master mode operation

The only difference between single-master mode and multi-master mode operation is the use of mode fault error detection (see section 31.3.8, Error Detection). In single-master mode, the SPI does not detect mode fault errors whereas in multi-master mode, it does. This section explains the operations that are common to both modes.

(1) Starting serial transfer

The SPI updates the data in the transmit buffer (SPTX) when data is written to the SPI Data Register (SPDR/SPDR_HA) with the SPI transmit buffer is empty, and data for the next transfer is not set (SPSR.SPTEF flag is 1). When the shift

register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR/SPDR_HA, the SPI copies data from the transmit buffer to the shift register and starts serial transfer. On copying transmit data to the shift register, the SPI changes the status of the shift register to full, and on termination of serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

The polarity of the SSLni output pins depends on the SSLP register settings. For details on the SPI transfer format, see section 31.3.5, Transfer Format.

(2) Terminating a serial transfer

Regardless of the SPCMDm.CPHA bit setting, the SPI terminates a serial transfer after transmitting an RSPCKn edge associated with the final sampling timing. If free space is available in the receive buffer (SPRX) (SPSR.SPRF flag is 0), on termination of the serial transfer, the SPI copies data from the shift register to the receive buffer of the SPDR/SPDR_HA register.

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[3:0] bit setting. The polarity of the SSLni output pin depends on the SSLP register settings. For details on the SPI transfer format, see section 31.3.5, Transfer Format.

(3) Sequence control

The transfer format used in master mode is determined by the SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers.

The SPSCR register determines the sequence configuration for serial transfers that the SPI executes in master mode. The following parameters are set in the SPCMDm register:

- SSLni pin output signal value
- MSB- or LSB-first
- Data length
- Some of the bit rate settings
- RSPCK polarity/phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced.

SPBR holds some of the bit rate settings, such as the SPI clock delay value (SPCKD), the SSL negation delay value (SSLND), and the next-access delay value (SPND).

Based on the sequence length assigned in SPSCR, the SPI makes up a sequence comprised of a part or all of the SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0, and incorporates the SPCMD0 settings into the transfer format at the beginning of serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command in the sequence, the SPI sets the pointer to SPCMD0 to execute the sequence repeatedly.

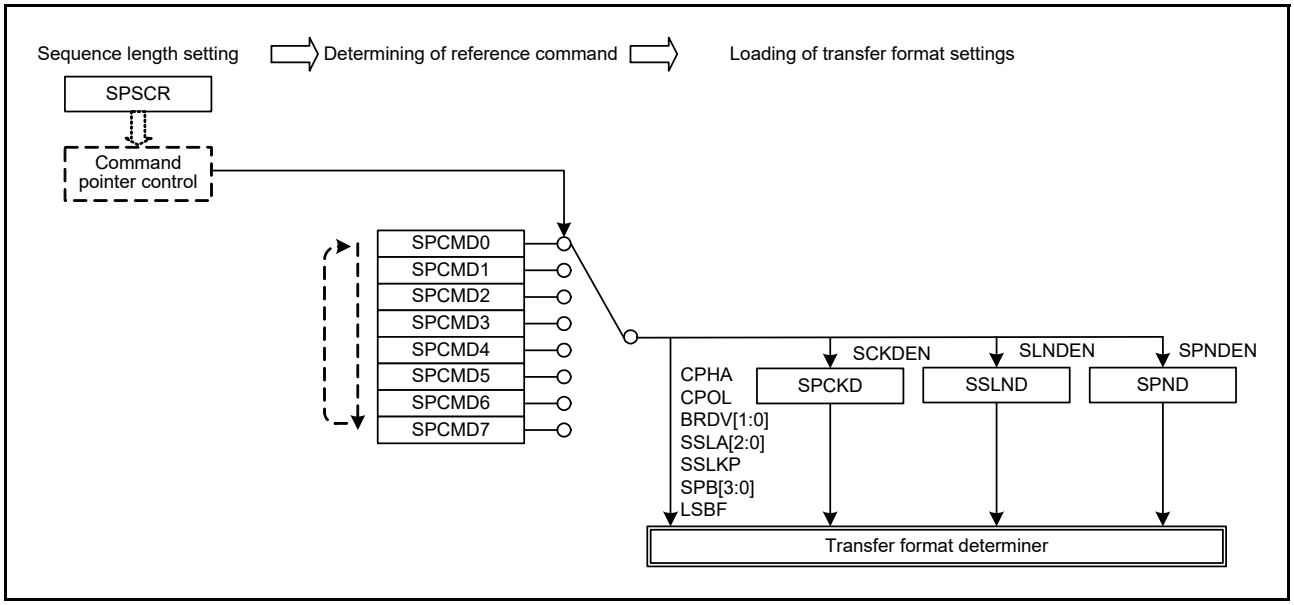


Figure 31.32 Procedure for determining serial transfer format in master mode

In this section, a frame is the combination of the SPDR/SPDR_HA data and the SPCMDm settings.

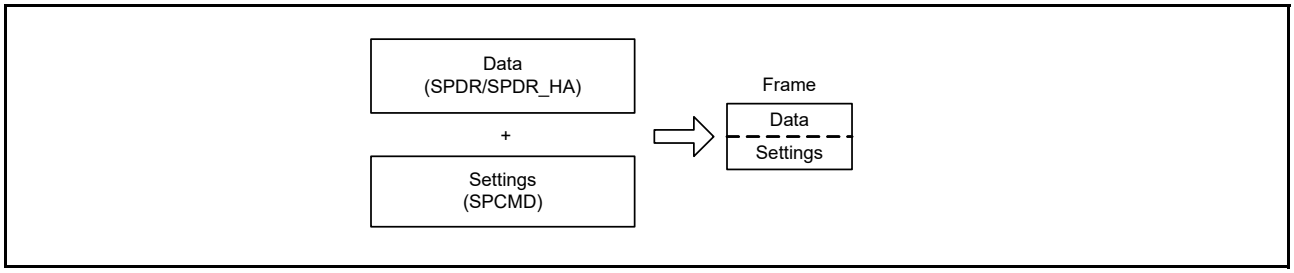


Figure 31.33 Conceptual diagram of frames

Figure 31.34 shows the relationship between the commands and the transmit and receive buffers in the sequence of operations specified by the settings in Table 31.4.

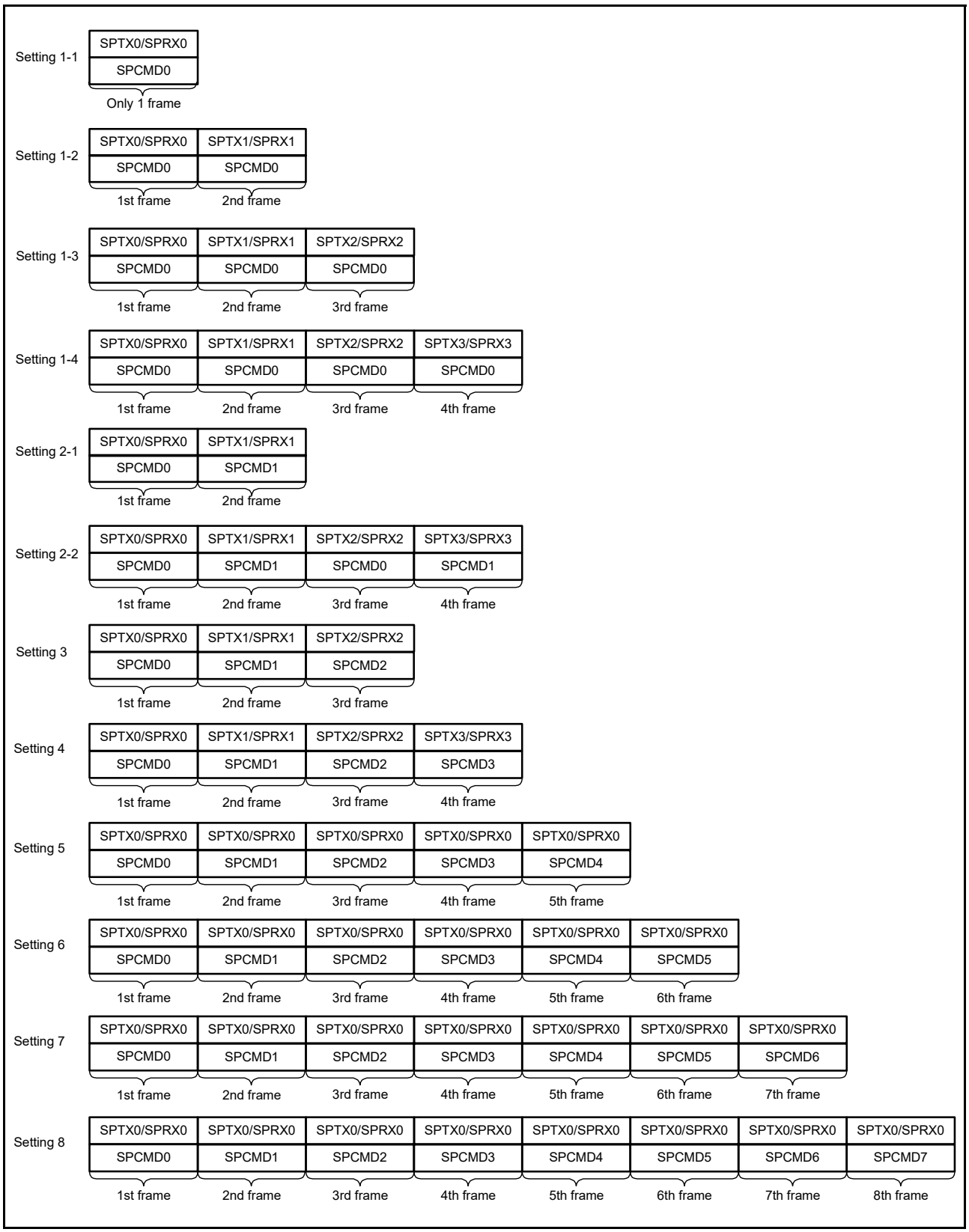


Figure 31.34 Relationship between SPI Command register and transmit and receive buffers in sequence operations

(4) Burst transfers

If the SPCMDm.SSLKP bit that the SPI references during the current serial transfer is 1, the SPI maintains the SSLni signal level during the serial transfer until the beginning of the SSLni signal assertion for the next serial transfer. If the SSLni signal level for the next serial transfer is the same as the SSLni signal level for the current serial transfer, the SPI can execute continuous serial transfers while keeping the SSLni signal assertion status (burst transfer).

Figure 31.35 shows an example of an SSLni signal operation for a burst transfer that is implemented using the SPCMD0 and SPCMD1 register settings. This section describes SPI operations (1) to (7) shown in Figure 31.35.

Note: The polarity of the SSLni output signal depends on the SSLP register settings.

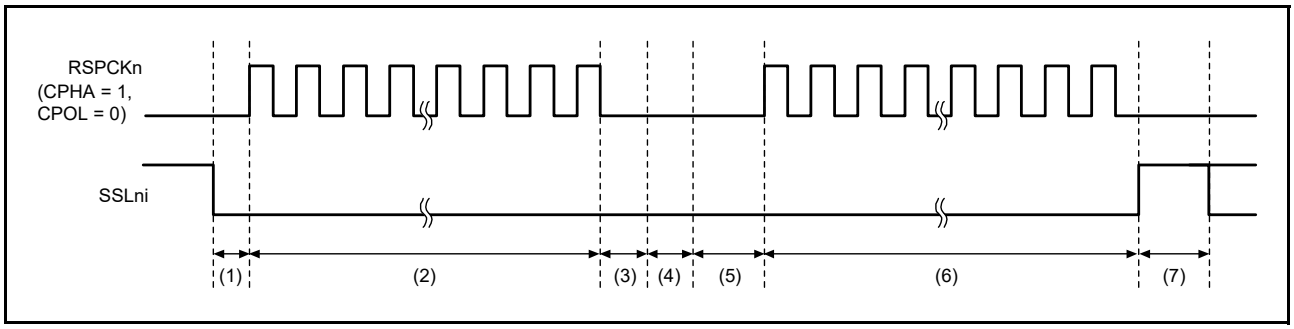


Figure 31.35 Example of burst transfer operation using the SSLKP bit

The SPI operation at timings (1) to (7) in Figure 31.35 is as follows:

1. Based on the SPCMD0 settings, the SPI asserts the SSLni signal and inserts RSPCK delays.
2. The SPI executes serial transfers according to the SPCMD0 settings.
3. The SPI inserts an SSL negation delay.
4. Because the SPCMD0.SSLKP bit is 1, the SPI keeps the SSLni signal value specified in SPCMD0. This period is sustained at a minimum for a period equal to the next-access delay in SPCMD0. If the shift register is empty after the passage of the minimum period, this period is sustained until the transmit data is stored in the shift register for the next transfer.
5. Based on the SPCMD1 settings, the SPI asserts the SSLni signal and inserts RSPCK delays.
6. The SPI executes serial transfers according to the SPCMD1 settings.
7. Because the SPCMD1.SSLKP bit is 0, the SPI negates the SSLni signal. In addition, a next-access delay is inserted according to SPCMD1.

If the SSLni signal output settings in the SPCMDm register where 1 is assigned to the SSLKP bit are different from the SSLni signal output settings in the SPCMDm register to be used in the next transfer, the SPI switches the SSLni signal status to SSLni signal assertion as shown in (5) in Figure 31.35. This corresponds to the command for the next transfer.

Note: If such an SSLni signal switching occurs, the slaves that drive the MISOn signal compete, and the collision of signal levels might occur.

The SPI in master mode references the SSLni signal operation within the module when the SSLKP bit is not used. When the SPCMDm.CPHA bit is 0, the SPI can accurately start serial transfers using the SSLni signal assertion for the next transfer that is detected internally.

(5) RSPCK delay (t1)

The RSPCK delay value of the SPI in master mode depends on the SPCMDm.SCKDEN bit setting and the SPCKD register setting. The SPI determines the SPCMDm register to be referenced during a serial transfer by pointer control, and determines the RSPCK delay value using the SPCMDm.SCKDEN bit and SPCKD, as listed in Table 31.9. For a definition of the RSPCK delay, see section 31.3.5, Transfer Format.

Table 31.9 Relationship between the SCKDEN bit, SPCKD register, and RSPCK delay

SPCMDm.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(6) SSL negation delay (t2)

The SSL negation delay value of the SPI in master mode depends on the SPCMDm.SLNDEN bit setting and the SSLND register setting. The SPI determines the SPCMDm register to be referenced by pointer control during a serial transfer, and determines the SSL negation delay by using the SPCMDm.SLNDEN bit and SSLND, as listed in Table 31.10. For a definition of the SSL negation delay, see section 31.3.5, Transfer Format.

Table 31.10 Relationship between the SLNDEN bit, SSLND, and SSL negation delay

SPCMDm.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL negation delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-access delay (t3)

The next-access delay value of the SPI in master mode depends on the SPCMDm.SPNDEN bit setting and the SPND register setting. The SPI determines the SPCMDm register to be referenced by pointer control during serial transfer, and determines a next-access delay during serial transfer using the SPCMDm.SPNDEN bit and SPND.SPNDL[2:0] bits, as listed in Table 31.11. For a definition of the next-access delay, see section 31.3.5, Transfer Format.

Table 31.11 Relationship between the SPNDEN bit, SPND bit, and next-access delay

SPCMDm.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLKA
1	000b	1 RSPCK + 2 PCLKA
	001b	2 RSPCK + 2 PCLKA
	010b	3 RSPCK + 2 PCLKA
	011b	4 RSPCK + 2 PCLKA
	100b	5 RSPCK + 2 PCLKA
	101b	6 RSPCK + 2 PCLKA
	110b	7 RSPCK + 2 PCLKA
	111b	8 RSPCK + 2 PCLKA

(8) Initialization flow

Figure 31.36 shows an example of SPI initialization flow when the SPI is in master mode. For information on how to set up the ICU, DMAC, and I/O ports, see the individual block descriptions.

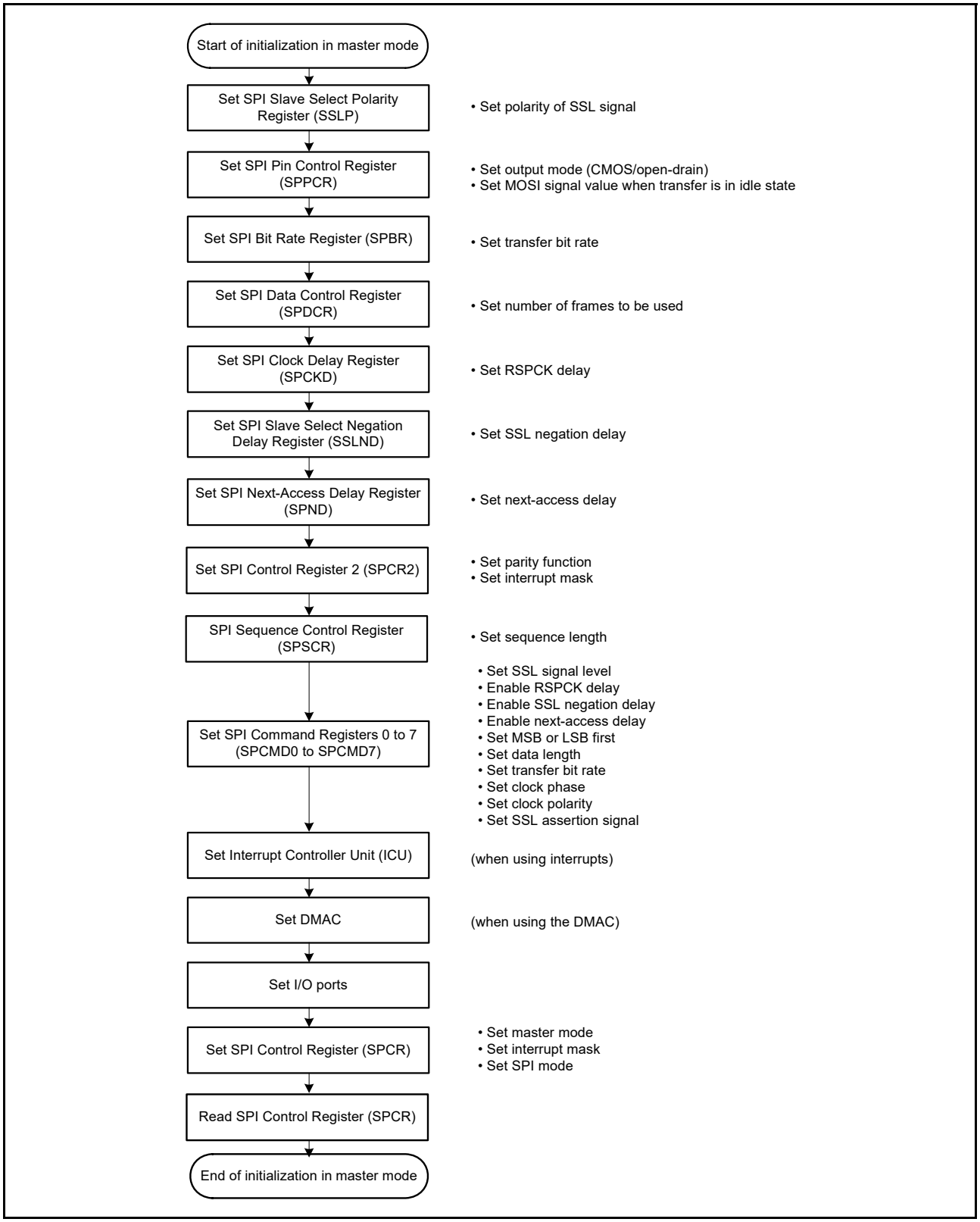


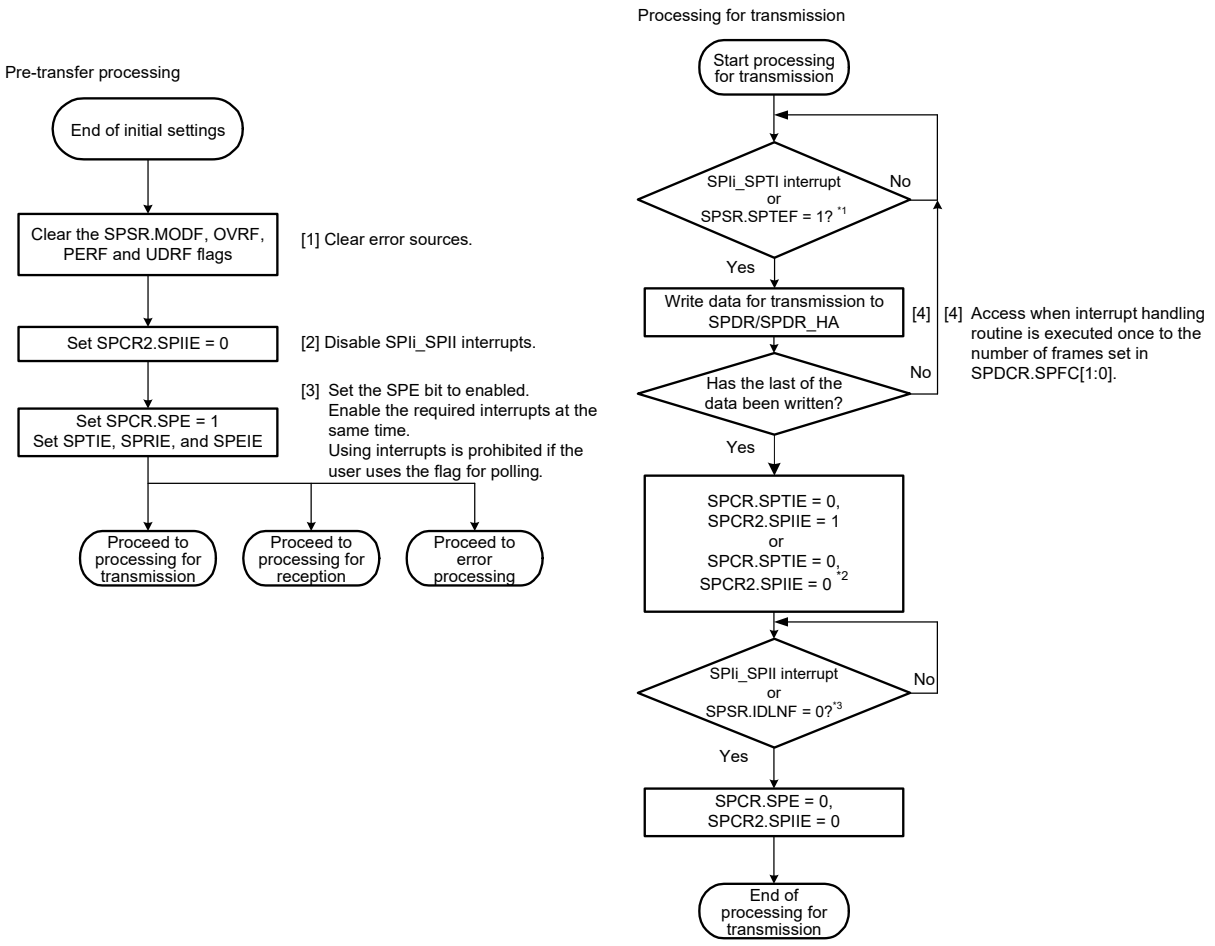
Figure 31.36 Example of initialization flow in master mode for SPI operation

(9) Software processing flow

Figure 31.37 to Figure 31.39 show examples of the software processing flow.

(a) Transmit processing flow

When transmitting data, with the SPIi_SPII interrupt enabled, the CPU is notified of the completion of data transmission after the last data write for transmission.



Note 1. Before writing data for transmission to SPDR/SPDR_HA, check the transmit buffer empty interrupt by reading the SPSR.SPTEF flag, if the flag for polling is used.
Note 2. Setting the idle interrupt is prohibited (SPCR2.SPIIE = 0), if the flag for polling is used.
Note 3. Wait more than 1 PCLKA after writing data for transmission to SPDE and before starting to poll PSR.IDLNF, if the flag for polling is used.

Figure 31.37 Transmission flow in master mode

(b) Receive processing flow

The SPI does not handle receive-only operations, so processing for transmission is required.

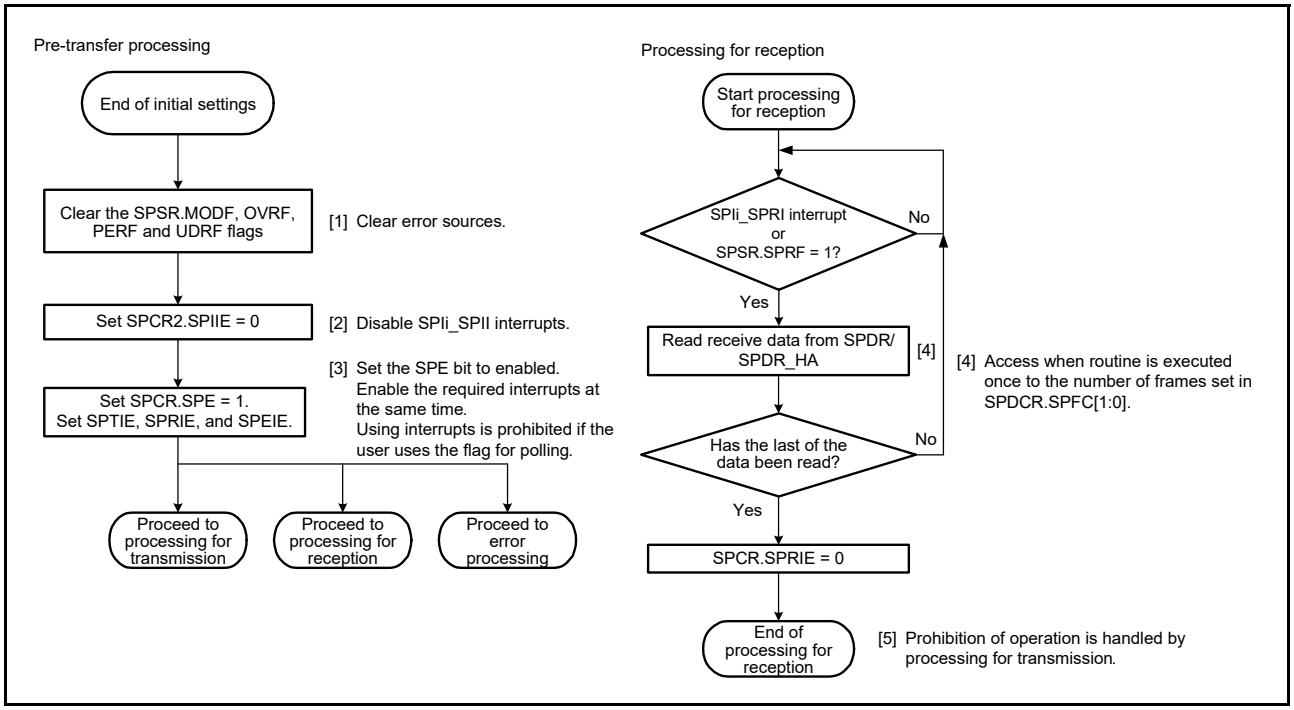


Figure 31.38 Reception flow in master mode

(c) Error processing flow

The SPI detects the following errors:

- Mode fault
- Underrun
- Overrun
- Parity.

When a mode fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. For errors from other sources, the SPCR.SPE bit is not cleared and operations for transmission and reception continue. Renesas recommends clearing the SPCR.SPE bit to stop operations for errors other than mode fault errors. Not doing so leads to updating of the SPSSR.SPECM[2:0] bits.

When an error is detected using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate a SPIi_SPTI or SPIi_SPRI interrupt request. If an SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.

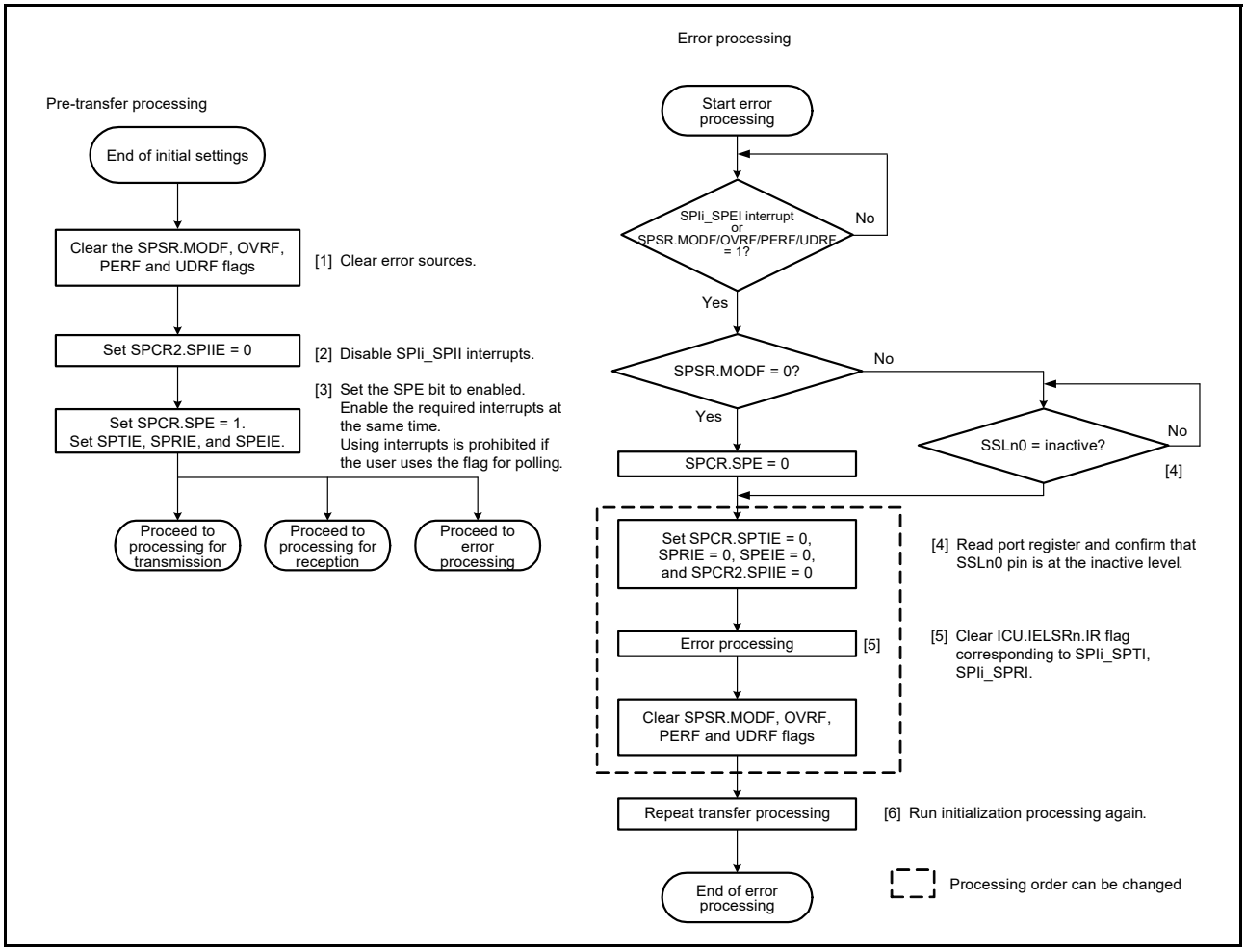


Figure 31.39 Error processing flow in master mode

31.3.10.2 Slave mode operation

(1) Starting a serial transfer

When the SPCMD0.CPHA bit is 0, if the SPI detects an SSLn0 input signal assertion, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLn0 input signal triggers the start of a serial transfer.

When the CPHA bit is 1, if the SPI detects the first RSPCKn edge in an SSLn0 signal asserted condition, it must drive valid data to the MISOn output signal. So, when the CPHA bit is 1, the first RSPCKn edge in an SSLn0 signal asserted condition triggers the start of a serial transfer.

Regardless of the CPHA bit setting, the SPI drives the MISOn output signal on SSLn0 signal assertion. The data that is output by the SPI is either valid or invalid, depending on the CPHA bit setting.

The polarity of the SSLn0 input signal depends on the SSLP.SSL0P setting. For details on the SPI transfer format, see section 31.3.5, Transfer Format.

(2) Terminating a serial transfer

Regardless of the SPCMD0.CPHA bit setting, the SPI terminates the serial transfer after detecting an RSPCKn edge associated with the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of a serial transfer, the SPI copies the received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty, regardless of the receive buffer state. A mode fault error occurs if the SPI detects an SSLn0 input signal negation from the beginning of the serial transfer to the end of the serial transfer (see section 31.3.8, Error Detection).

The final sampling timing changes depending on the bit length of the transfer data. In slave mode, the SPI data length is determined by the SPCMD0.SPB[3:0] bit setting. The polarity of the SSLn0 input signal is determined by the SSLP.SSL0P bit setting. For details on the SPI transfer format, see section 31.3.5, Transfer Format.

(3) Notes on single-slave operations

If the SPCMD0.CPHA bit is 0, the SPI starts serial transfers when it detects the assertion edge for an SSLn0 input signal. In the configuration example shown in Figure 31.7, if the SPI is in single-slave mode, the SSLn0 signal is fixed at an active state. Therefore, when the CPHA bit is set to 0, the SPI cannot correctly start a serial transfer. For the SPI to correctly execute transmit and receive operations in slave mode when the SSLn0 input signal is fixed at an active state, the CPHA bit must be set to 1. If the application requires setting the CPHA bit to 0, the SSLn0 input signal must not be fixed.

(4) Burst transfer

If the SPCMD0.CPHA bit is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSLn0 input signal. When the CPHA bit is 1, the serial transfer period is the period from the first RSPCKn edge to the sampling timing for the reception of the final bit in an SSLn0 signal active state. Even when the SSLn0 input signal remains at an active level, the SPI can accommodate burst transfers because it can detect the start of an access.

When the CPHA bit is 0, the second and subsequent serial transfers during burst transfer cannot be executed correctly.

(5) Initialization flow

Figure 31.40 shows an example of initialization flow for SPI operation when the SPI is in slave mode. For information on how to set up the ICU, DMAC, and I/O ports, see the individual block descriptions.

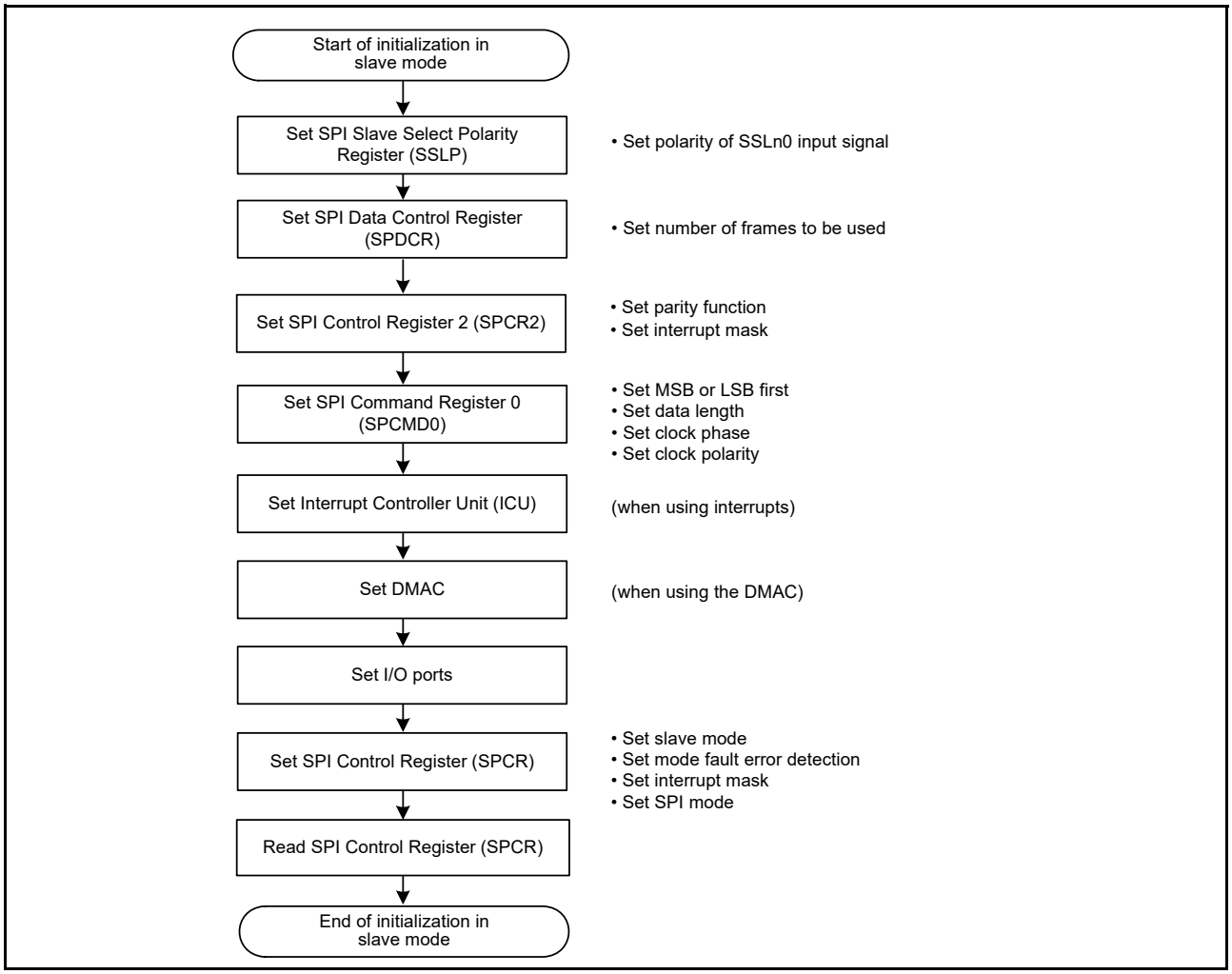
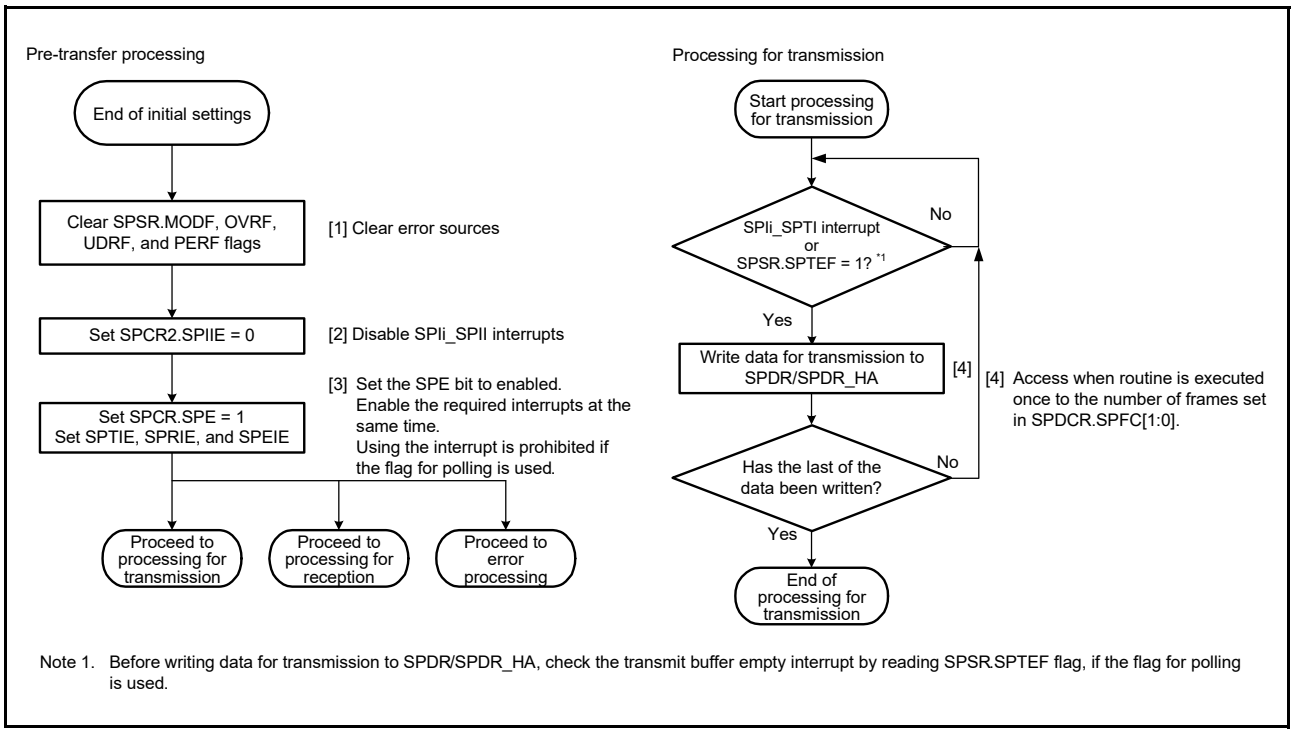


Figure 31.40 Example initialization flow in slave mode for SPI operation

(6) Software processing flow

Figure 31.41 to Figure 31.43 show examples of the software processing flow.

(a) Transmit processing flow



Note 1. Before writing data for transmission to SPDR/SPDR_HA, check the transmit buffer empty interrupt by reading SPSR.SPTEF flag, if the flag for polling is used.

Figure 31.41 Transmission flow in slave mode

(b) Receive processing flow

The SPI does not handle receive-only operations, so processing for transmission is required.

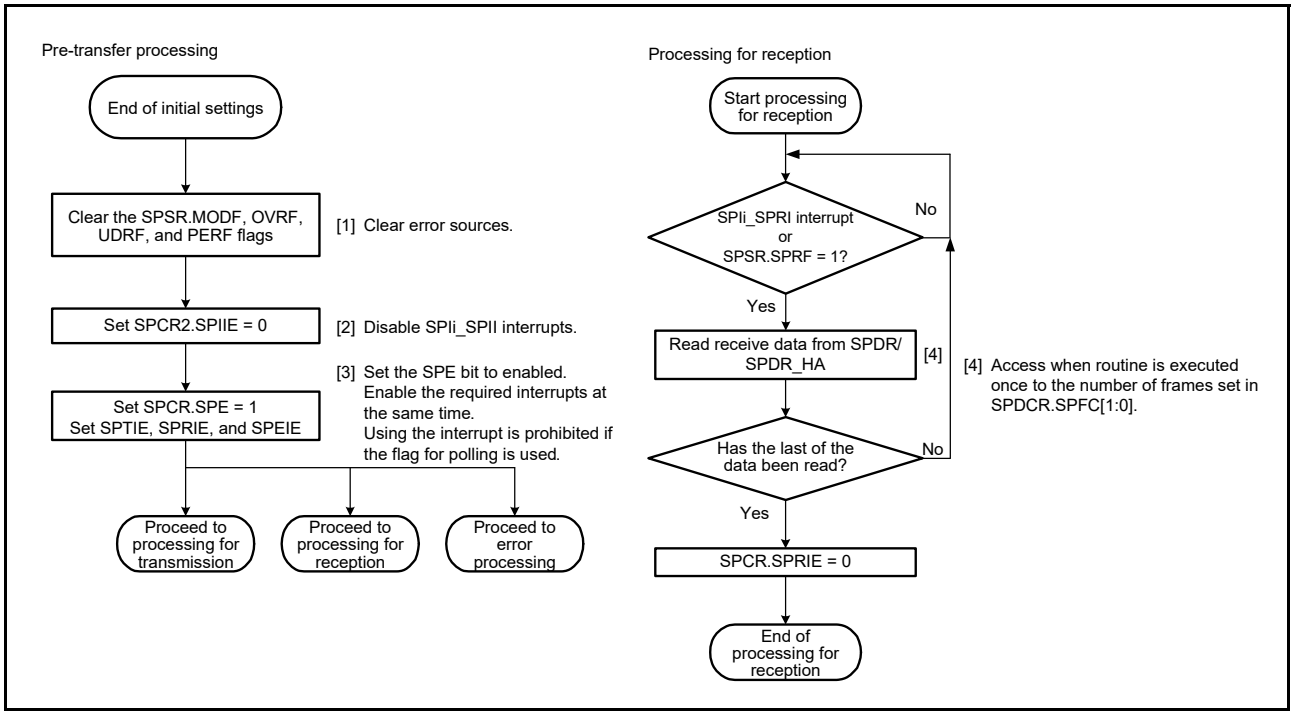


Figure 31.42 Reception flow in slave mode

(c) Error processing flow

In slave operation, even when a mode fault error is generated, the SPSR.MODF flag can be cleared regardless of the state of the SSLn0 pin.

When an error is detected by using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.

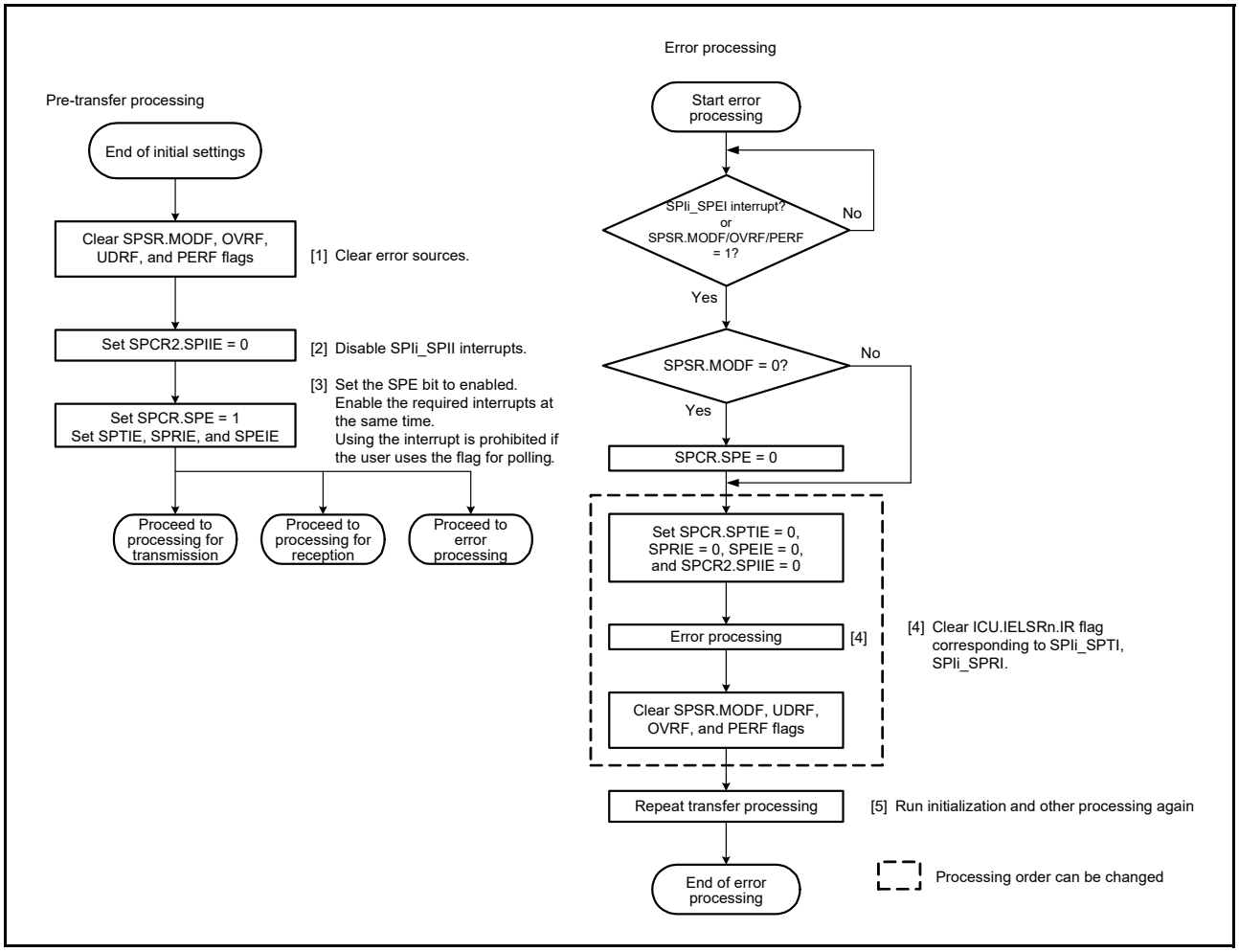


Figure 31.43 Error processing flow for slave mode

31.3.11 Clock Synchronous Operation

Setting the SPCR.SPMS bit to 1 selects clock synchronous operation of the SPI. In clock synchronous operation, the SSLni pin is not used, and the RSPCKn, MOSIn, and MISOn pins handle communication. All SSLni pins are available as I/O port pins.

Although clock synchronous operation does not require the use of the SSLni pin, operation of the module is the same as in SPI operation. In both master and slave operations, communications can be performed with the same flow as in SPI operation. However, mode fault errors are not detected because the SSLni pin is not used.

Additionally, do not perform operation if the clock synchronous operation is enabled when the SPCMDm.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).

31.3.11.1 Master mode operation

(1) Starting serial transfer

The SPI updates the data in the transmit buffer (SPTX) of SPDR/SPDR_HA when data is written to the SPDR/SPDR_HA register with the transmit buffer empty, the data for the next transfer not set and the SPSR.SPTEF flag is 1. When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR/SPDR_HA, the SPI copies data from the transmit buffer to the shift register and starts serial transmission. On copying transmit data to the shift register, the SPI changes the status of the shift register to full, and on termination of serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 31.3.5, Transfer Format.

(2) Terminating serial transfer

The SPI terminates the serial transfer after transmitting an RSPCKn edge associated with the sampling timing. If free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies data from the shift register to the receive buffer of the SPI Data Register (SPDR/SPDR_HA).

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[3:0] bit setting. Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 31.3.5, Transfer Format.

(3) Sequence control

The transfer format used in master mode is determined by the SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers. Although the SSLni signals are not output in clock synchronous operation, these settings are valid.

The SPSCR register determines the sequence configuration for serial transfers that are executed by the SPI in master mode. The following parameters are specified in the SPCMDm register:

- SSLni output signal value
- MSB- or LSB-first
- Data length
- Some of the bit rate settings
- RSPCKn polarity and phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced.

SPBR holds some of the bit rate settings such as the SPCKD (SPI clock delay), SSLND (SSL negation delay), and SPND (next-access delay).

Based on the sequence length that is assigned to SPSCR, the SPI makes up a sequence comprised of a part or all of SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in the SPCMD0 register, and incorporates the SPCMD0 register setting into the transfer format at the beginning of the serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command comprising the sequence, the SPI sets the pointer to the SPCMD0 register to execute the sequence repeatedly.

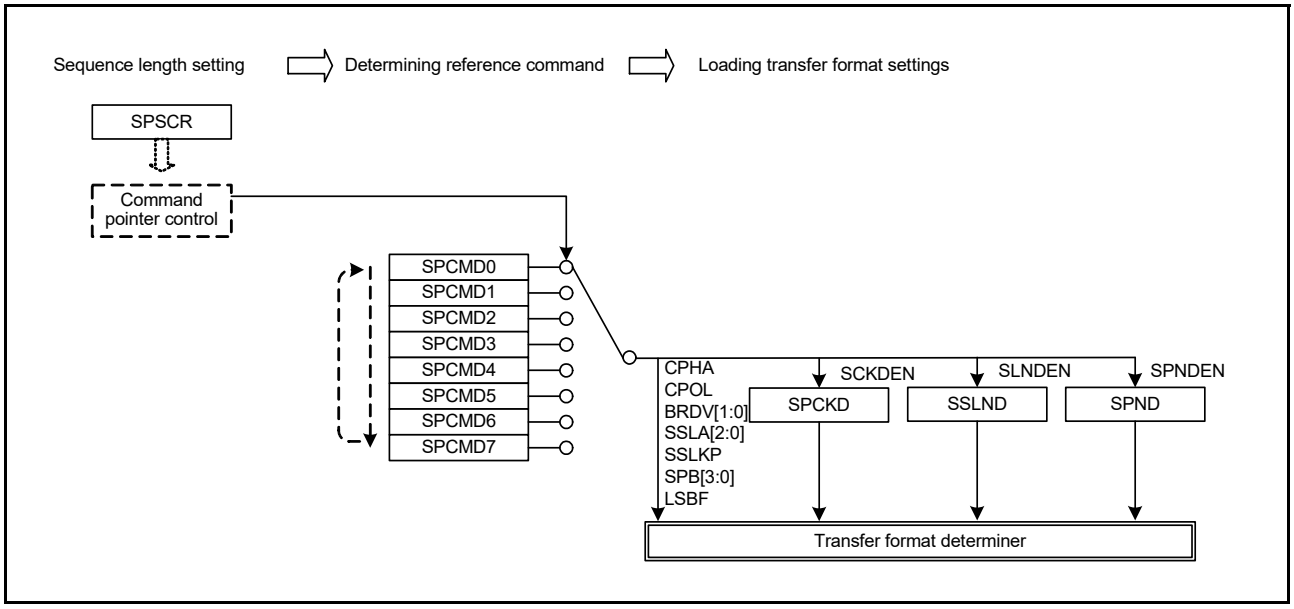


Figure 31.44 Procedure to determine the format of serial transmission in master mode

In this section, a frame is the combination of the SPDR/SPDR_HA data and SPCMDm settings.

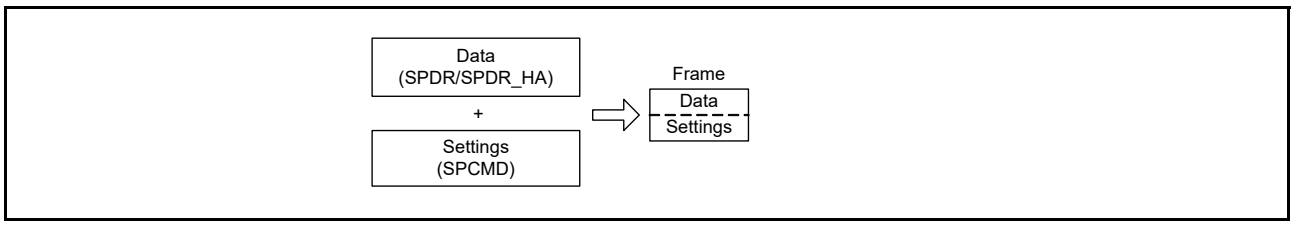


Figure 31.45 Conceptual diagram of frames

Figure 31.46 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings in Table 31.4.

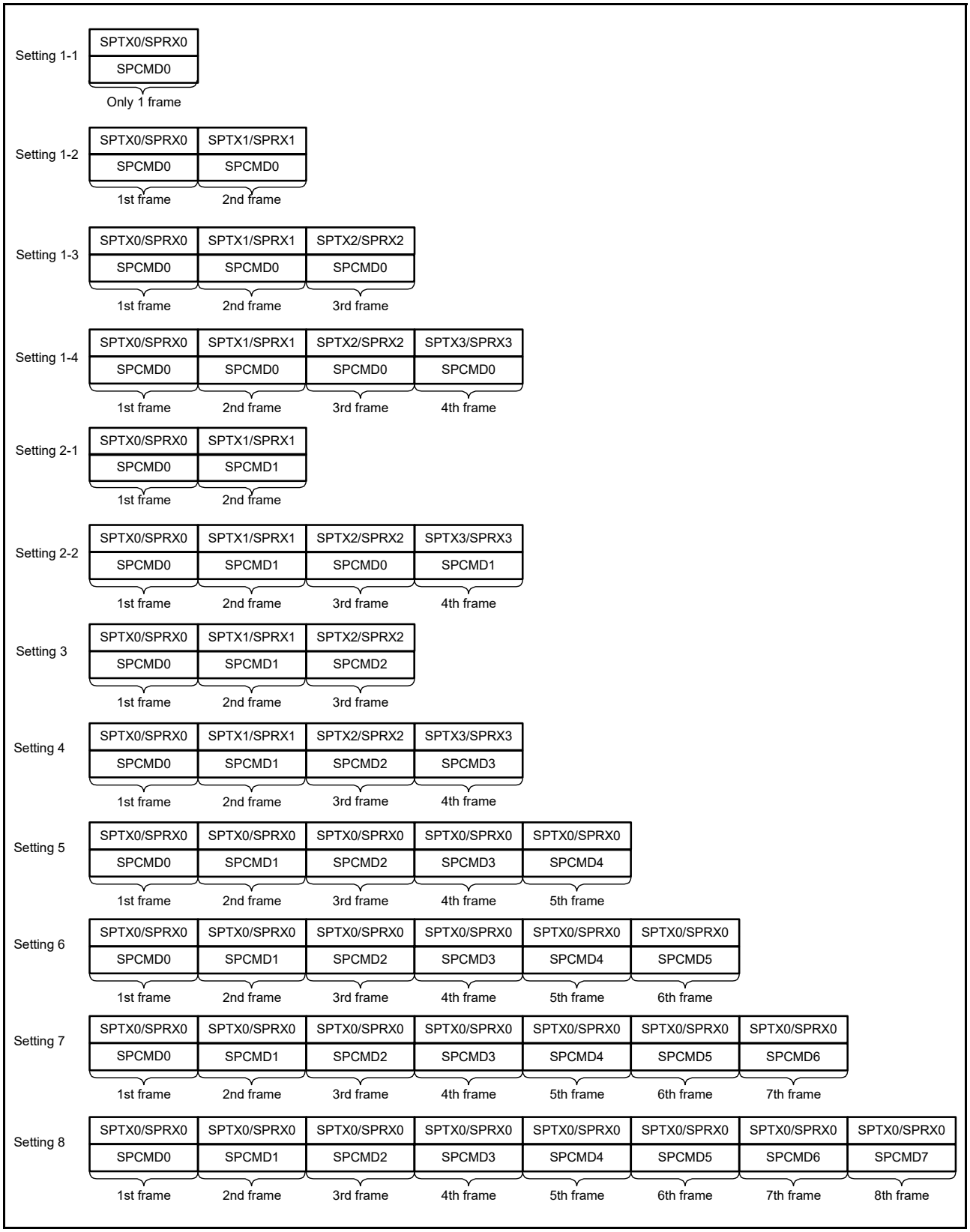


Figure 31.46 Relationship between the SPI Command register and the transmit and receive buffers in sequence operations

(4) Initialization flow

Figure 31.47 shows an example of initialization flow for clock synchronous operation when the SPI is used in master mode. For information on how to set up the ICU, DMAC, and I/O ports, see the descriptions given in the individual blocks.

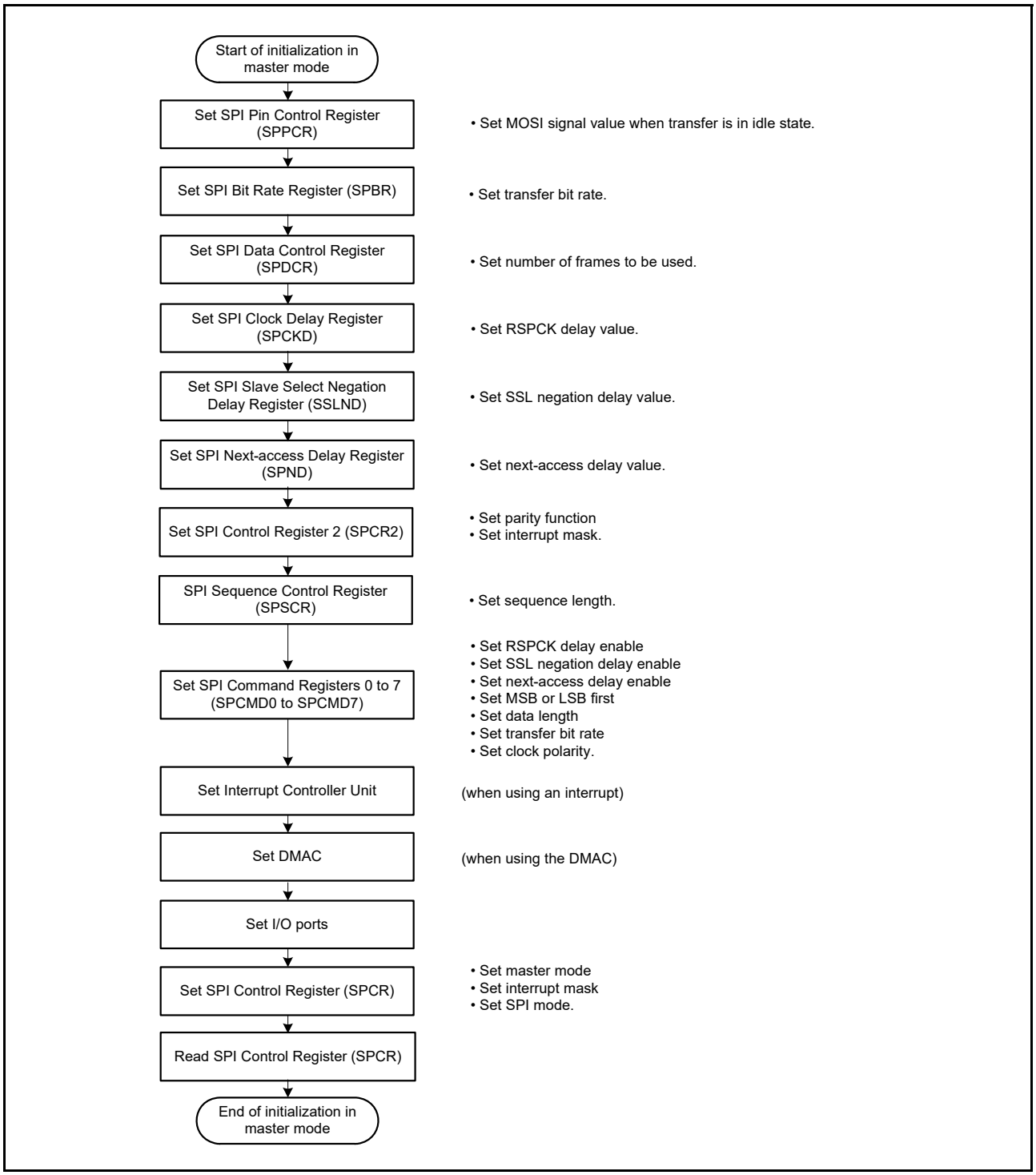


Figure 31.47 Example of initialization flow in master mode for clock synchronous operation

(5) Software processing flow

Software processing during clock synchronous master operation is the same as that for SPI master operation. For details, see section 31.3.10.1, (9) Software processing flow. Mode fault errors are not generated in clock synchronous operation.

31.3.11.2 Slave mode operation

(1) Starting serial transfer

When the SPCR.SPMS bit is 1, the first RSPCKn edge triggers the start of a serial transfer in the SPI, and the SPI drives the MISOn output signal. The SSLn0 input signal is not used in clock synchronous operation. For details on the SPI transfer format, see section 31.3.5, Transfer Format.

(2) Terminating serial transfer

The SPI terminates the serial transfer after detecting an RSPCKn edge associated with the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of a serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty regardless of the receive buffer.

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length is determined by the SPCMD0.SPB[3:0] bit setting. For details on the SPI transfer format, see section 31.3.5, Transfer Format.

(3) Initialization flow

Figure 31.48 shows an example of initialization flow for clock synchronous operation when the SPI is used in slave mode. For information on how to set up the ICU, DMAC, and I/O ports, see the descriptions given in the individual blocks.

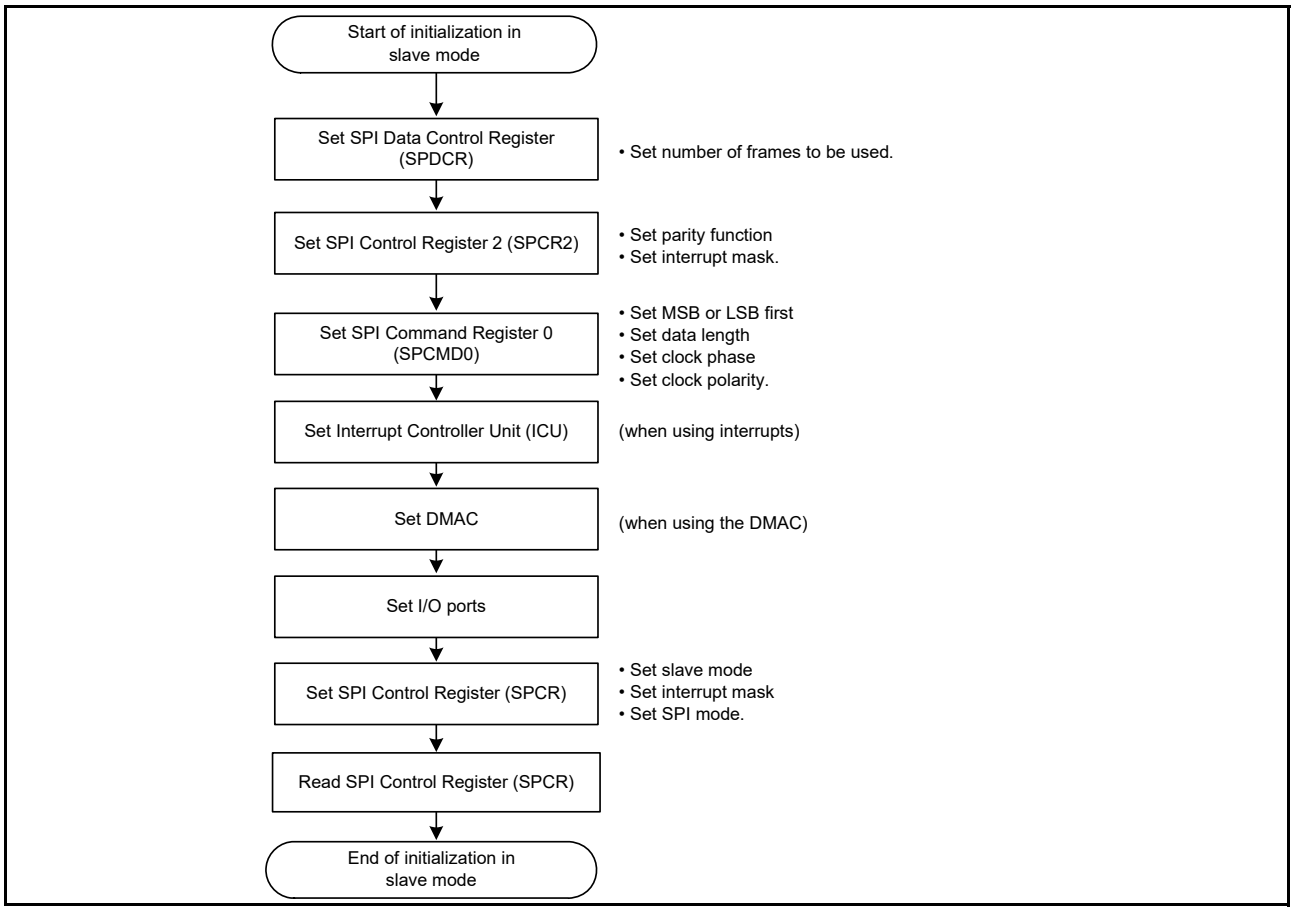


Figure 31.48 Example of initialization flow in slave mode for clock synchronous operation

(4) Software processing flow

Software processing during clock synchronous slave operation is the same as that for SPI slave operation. For details, see section 31.3.10.2, (6) Software processing flow.

Note: Mode fault errors are not generated in clock synchronous mode.

31.3.12 Loopback Mode

When 1 is written to the SPPCR.SPLP2 bit or SPPCR.SPLP bit, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, or between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input and output paths of the shift register, establishing a loopback mode. The SPI does not shut off the path between the MOSIn pin and the shift register if the SPCR.MSTR bit is 1, or between the MISOn pin and the shift register if the SPCR.MSTR bit is 0. When a serial transfer is executed in loopback mode, the transmit data for the SPI or the reversed transmit data becomes the received data for the SPI.

Table 31.12 lists the relationship between the SPLP2 and SPLP bits and the received data. Figure 31.49 shows the configuration of the shift register I/O paths when the SPI in master mode is set to loopback mode (SPPCR.SPLP2 = 1, SPPCR.SPLP = 0 or 1).

Table 31.12 SPLP2 and SPLP bit settings and received data

SPPCR.SPLP2 bit	SPPCR.SPLP bit	Received data
0	0	Input data from the MOSIn pin or MISOn pin
0	1	Inverted transmit data
1	0	Transmit data
1	1	Transmit data

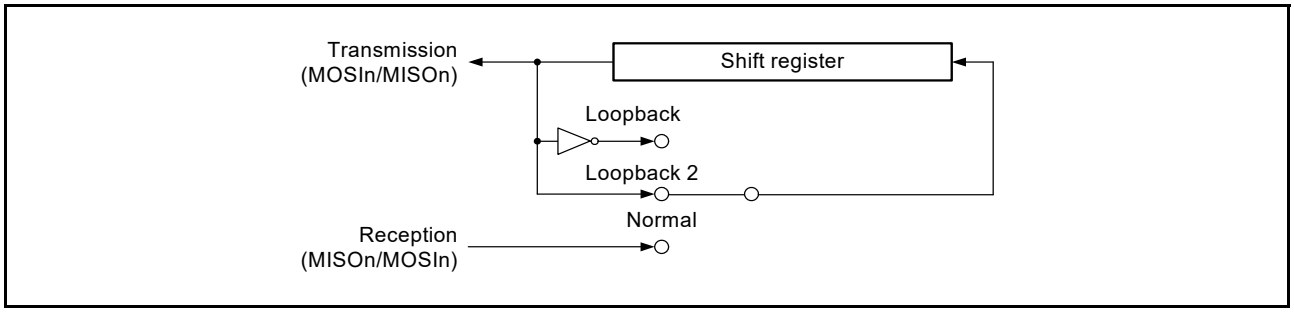


Figure 31.49 Configuration of Shift register I/O paths in loopback mode for master mode

31.3.13 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit used for transmit data and an error detecting unit used for received data. To detect defects in these units, the parity circuit performs self-diagnosis as shown in Figure 31.50.

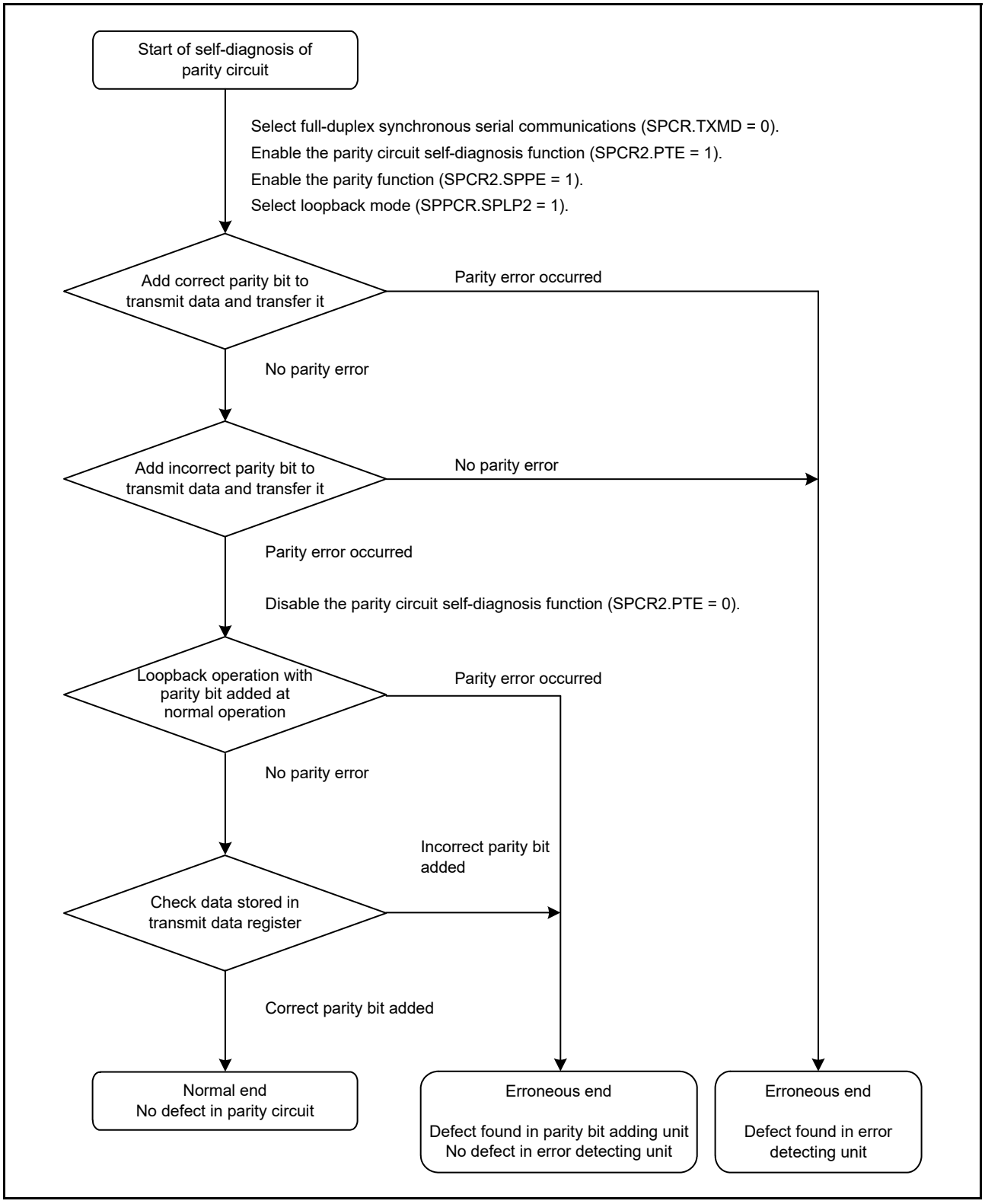


Figure 31.50 Self-diagnosis flow for parity circuit

31.3.14 Interrupt Sources

The SPI interrupt sources include:

- Receive buffer full
- Transmit buffer empty

- SPI error (mode-fault, underrun, overrun, or parity error)
- SPI idle
- Transmission-complete.

The DTC or DMAC can be activated by the receive buffer full or transmit buffer empty interrupt to perform data transfer.

Because the vector address for the SPIi_SPEI (SPI error interrupt) is allocated to interrupt requests on mode-fault, underrun, overrun, and parity errors, the actual interrupt source must be determined from the flags. Table 31.13 lists the interrupt sources for the SPI. An interrupt is generated on satisfaction of one of the interrupt conditions in Table 31.13. Clear the receive buffer full and transmit buffer empty sources through a data transfer.

When using the DTC or DMAC to perform data transmission and reception, you must first set up the DTC or DMAC to be in a transfer-enabled status before setting the SPI. For information on setting up the DTC or DMAC, see section 16, DMA Controller (DMAC), or section 17, Data Transfer Controller (DTC).

If the conditions for generating a transmit buffer empty or receive buffer full interrupt occur while the ICU.IELSRn.IR flag is 1, the interrupt is not output as a request for the ICU but is saved internally (the capacity for retention is one request per source). A saved interrupt request is output when the ICU.IELSRn.IR flag becomes 0. A saved interrupt request is automatically discarded when it is output as an actual interrupt request. The interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) for an internally saved interrupt request can also be set to 0.

Table 31.13 SPI interrupt sources

Interrupt source	Symbol	Interrupt condition	DMAC/DTC activation
Receive buffer full	SPIi_SPRI	The receive buffer becomes full (SPSR.SPRF flag is 1) while the SPCR.SPRIE bit is 1	Possible
Transmit buffer empty	SPIi_SPTI	The transmit buffer becomes empty (SPSR.SPTEF flag is 1) while the SPCR.SPTIE bit is 1	Possible
SPI errors (mode-fault, underrun, overrun, and parity error)	SPIi_SPEI	The SPSR.MODF, OVRF, PERF, or UDRF flag is set to 1 while the SPCR.SPEIE bit is 1	Impossible
SPI idle	SPIi_SPII	The SPSR.IDLNF flag is set to 0 while the SPCR2.SPIIE bit is 1	Impossible
Transmission-complete	SPIi_SPTEND	In master mode, an interrupt is generated when the IDLNF flag (SPI idle flag) changes from 1 to 0. In slave mode, an interrupt occurs on conditions shown in Table 31.15.	Impossible

31.4 Output to the Event Link Controller (ELC)

The ELC can produce the following event output signals:

- Receive buffer full event output
- Transmit buffer empty event output
- Mode-fault, underrun, overrun, or parity error event output
- SPI idle event output
- Transmission-completed event output.

The event link output signal is output regardless of the interrupt enable bit setting.

31.4.1 Receive Buffer Full Event Output

This event signal is output when received data is transferred from the shift register to the SPDR/SPDR_HA on completion of serial transfer.

31.4.2 Transmit Buffer Empty Event Output

This event signal is output when data for transmission is transferred from the transmit buffer to the shift register and when the value of the SPE bit changes from 0 to 1.

31.4.3 Mode-Fault, Underrun, Overrun, or Parity Error Event Output

This event signal is output when mode-fault, underrun, overrun, or parity error is detected. See section 31.5.4, Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output if using this event signal.

(1) Mode-fault

Table 31.14 lists the conditions for occurrence of a mode-fault event.

Table 31.14 Conditions for mode-fault occurrence

Condition	SPCR.MODFEN bit	SSLn0 pin	Remarks
• SPI operation (SPMS = 0) • Slave (SPCR.MSTR bit = 0)	1	Not active	Event is output only when the pin is deactivated during transmission

(2) Underrun

This event signal is output in response to an underrun when a serial transfer starts while the transmission data is not ready, and the SPCR.MSTR bit is 0, and the SPCR.SPE bit is 1. Under these conditions, the MODF and UDRF flags are set to 1.

(3) Overrun

This event signal is output in response to an overrun when a serial transfer completes while the receive buffer contains unread data and the SPCR.TXMD bit is 0. Under these conditions, the OVRF flag is set to 1.

(4) Parity error

This event signal is output in response to a parity error detected on completion of a serial transfer while the value of the TXMD bit in SPCR is 0 and the SPPE bit in SPCR2 is 1.

31.4.4 SPI Idle Event Output

(1) In master mode

In master mode, an event is output when the condition for setting the IDLNF flag (SPI idle flag) to 0 is satisfied.

(2) In slave mode

In slave mode, an event is output when the SPCR.SPE bit is set to 0 (SPI is initialized).

31.4.5 Transmission-Completed Event Output

During both SPI and clock synchronous operations in master mode, an event is output when the IDLNF flag (SPI idle flag) changes from 1 to 0. Table 31.15 lists the conditions for occurrence of a transmission-completed event in slave mode.

Table 31.15 Conditions for generation of transmission-completed event in slave mode

Mode of operation	Transmit buffer state	Shift register state	Others
SPI operation (SPMS = 0)	Empty	Empty	Negation of SSLn0 input
Clock synchronous operation (SPMS = 1)	Empty	Empty	Edge detection of the last RSPCKn

Whether the operation is in master mode or slave mode, an event is not output if 0 is written to the SPCR.SPE bit in transmission or the SPCR.SPE bit is cleared by the mode-fault error or underrun error.

31.5 Usage Notes

31.5.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable SPI operation. The SPI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details on the Module Stop Control Register B, see section 11, Low Power Modes.

31.5.2 Constraints on Low Power Functions

When using the module-stop function and entering a low power mode other than Sleep mode, set the SPCR.SPE bit to 0 before completing communication.

31.5.3 Constraints on Starting Transfer

If the ICU.IELSRn.IR flag is 1 when transfer starts, the interrupt request is internally saved, which can lead to unanticipated behavior of the ICU.IELSRn.IR flag.

To prevent this, use the following procedure to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1):

1. Confirm that the transfer stopped (SPCR.SPE is 0).
2. Set the associated interrupt enable bit (SPCR.SPTIE or SPCR.SPRIE) to 0.
3. Read the associated interrupt enable bit (SPCR.SPTIE or SPCR.SPRIE) and confirm that its value is 0.
4. Set the ICU.IELSRn.IR flag to 0.

31.5.4 Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output

Using the mode-fault, underrun, overrun, or parity error event is prohibited if the SPI is in multi-master mode (when the SPCR.SPMS bit is 0, the SPCR.MSTR bit is 1, and the SPCR.MODFEN bit is 1).

31.5.5 Constraints on SPRF/SPTEF Flags

If the polling flags, SPRF and SPTEF, are used, interrupt usage is prohibited, and you must set the SPCR.SPRIE and SPCR.SPTIE bits to 0. Either the interrupts or the flags can be used, but not both.

32. Cyclic Redundancy Check (CRC) Calculator

The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring of reads from and writes to specific addresses. This function is useful in applications that require the CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.

32.1 Overview

Table 32.1 lists the CRC calculator specifications, and Figure 32.1 shows a block diagram.

Table 32.1 CRC calculator specifications

Parameter	Specifications for 8-bit data	Specifications for 32-bit data
Data size	8-bit	32-bit
Data for CRC calculation*1	CRC code generated for data in 8n-bit units (where n is a whole number)	CRC code generated for data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on 8 bits in parallel	Operation executed on 32 bits in parallel
CRC generating polynomial	One of three generating polynomials that is selectable: [8-bit CRC] • $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT).	One of two generating polynomials that is selectable: [32-bit CRC] • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C).
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication	
Module-stop function	Module-stop state can be set to reduce power consumption	
CRC snoop	Monitor reads from and writes to a certain register address	-

Note 1. The circuit cannot divide data used in CRC calculations. Write data in 8-bit or 32-bit units.

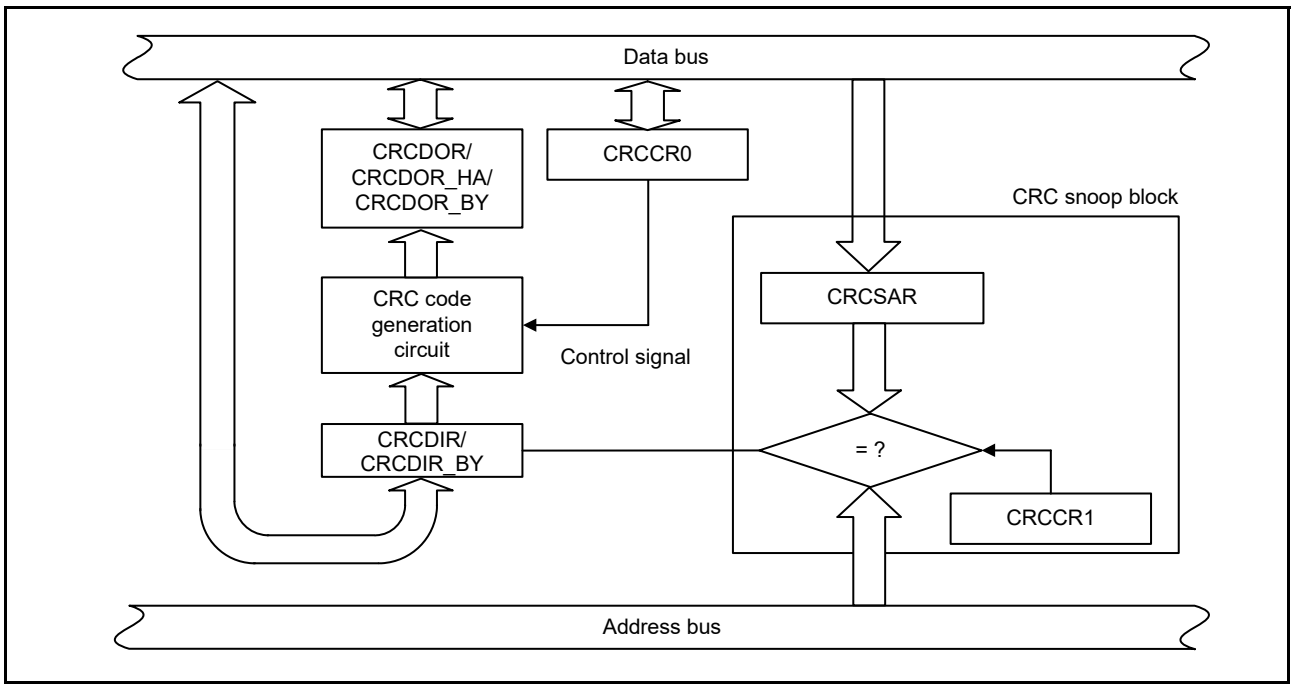


Figure 32.1 CRC calculator block diagram

32.2 Register Descriptions

32.2.1 CRC Control Register 0 (CRCCR0)

Address(es): CRC.CRCCR0 4007 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	DORCLR	LMS	—	—	—	GPS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	GPS[2:0]	CRC Generating Polynomial Switching	b2 b0 0 0: No calculation is executed 0 0: 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1: 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1: 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0: 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0: 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) Other: No calculation is executed.	R/W
b5 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	LMS	CRC Calculation Switching	0: Generate CRC for LSB-first communication 1: Generate CRC for MSB-first communication.	R/W
b7	DORCLR	CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear	1: Clear the CRCDOR/CRCDOR_HA/CRCDOR_BY register. This bit is read as 0.	W*1

Note 1. This bit must always be set to 1 when writing to this register.

GPS[2:0] bits (CRC Generating Polynomial Switching)

The GPS[2:0] bits select the CRC generating polynomial.

LMS bit (CRC Calculation Switching)

The LMS bit selects the bit order of generated CRC code. Transmit the lower byte of the CRC code first for LSB-first communication and the upper byte first for MSB-first communication. For details on transmitting and receiving CRC code, see section 32.3, Operation.

DORCLR bit (CRCDOR/CRCDOR_HA/CRCDOR_BY)

Write 1 to the DORCLR bit to set the CRCDOR/CRCDOR_HA/CRCDOR_BY register to 0000 0000h. This bit is read as 0. Only 1 can be written to it.

32.2.2 CRC Control Register 1 (CRCCR1)

Address(es): CRC.CRCCR1 4007 4001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CRCSEN	CRCSWR	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CRCSWR	Snoop-On-Write/Read Switch	0: Snoop-on-read 1: Snoop-on-write.	R/W

Bit	Symbol	Bit name	Description	R/W
b7	CRCSEN	Snoop Enable	0: Disabled 1: Enabled.	R/W

CRCSWR bit (Snoop-On-Write/Read Switch)

The CRCSWR bit selects the direction of access in the address monitoring function.

When this bit is set to 0 (initial value), the CRC snoop operation to read a specific register address is enabled. When the bit is set to 1, the CRC snoop operation to write to a specific register address is enabled.

CRCSEN bit (Snoop Enable)

When the CRCSEN bit is set to 1, the CRC snoop operation is enabled. When the bit is set to 0, CRC snoop operation is disabled.

32.2.3 CRC Data Input Register (CRCDIR/CRCDIR_BY)

Address(es): CRC.CRCDIR/CRCDIR_BY 4007 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCDIR is a 32-bit read/write register to write data for CRC-32 or CRC-32C calculation. CRCDIR_BY is an 8-bit read/write register to write data for CRC-8, CRC-16, or CRC-CCITT calculation.

32.2.4 CRC Data Output Register (CRCDOR/CRCDOR_HA/CRCDOR_BY)

Address(es): CRC.CRCDOR/CRCDOR_HA/CRCDOR_BY 4007 4008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCDOR is a 32-bit read/write register for CRC-32 or CRC-32C calculation. CRCDOR_HA is a 16-bit read/write register for CRC-16 or CRC-CCITT calculation. CRCDOR_BY is an 8-bit read/write register for CRC-8 calculation. Because its initial value is 0000 0000h, rewrite the CRCDOR/CRCDOR_HA/CRCDOR_BY register to perform the calculations using a value other than the initial value.

Data written to the CRCDIR/CRCDIR_BY register is CRC calculated and the result is stored in the CRCDOR/CRCDOR_HA/CRCDOR_BY register. If the CRC code is calculated following the transferred data and the result is 0000 0000h, there is no CRC error.

When an 8-bit CRC ($X^8 + X^2 + X + 1$ polynomial) is in use, the valid CRC code is obtained in CRCDOR_BY.

When a 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$ or $X^{16} + X^{12} + X^5 + 1$ polynomial) is in use, the valid CRC code is obtained in CRCDOR_HA.

32.2.5 Snoop Address Register (CRCSAR)

Address(es): CRC.CRCSAR 4007 400Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CRCSA[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CRCSA[13:0]	Register Snoop Address	These bits store the TDR or RDR address in the SCI module to snoop	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CRCSA[13:0] bits (Register Snoop Address)

The CRCSA[13:0] bits specify the lower 14 bits of the register address monitored by the CRC snoop operation.

Only the following addresses can be used for the CRCSA[13:0] bits:

- 4007 0003h: SCI0.TDR, 4007 0005h: SCI0.RDR
- 4007 0023h: SCI1.TDR, 4007 0025h: SCI1.RDR
- 4007 0043h: SCI2.TDR, 4007 0045h: SCI2.RDR
- 4007 0063h: SCI3.TDR, 4007 0065h: SCI3.RDR
- 4007 0083h: SCI4.TDR, 4007 0085h: SCI4.RDR
- 4007 0103h: SCI8.TDR, 4007 0105h: SCI8.RDR
- 4007 0123h: SCI9.TDR, 4007 0125h: SCI9.RDR
- 4007 000Fh: SCI0.FTDRL, 4007 0011h: SCI0.FRDRL
- 4007 002Fh: SCI1.FTDRL, 4007 0031h: SCI1.FRDRL
- 4007 004Fh: SCI2.FTDRL, 4007 0051h: SCI2.FRDRL
- 4007 006Fh: SCI3.FTDRL, 4007 0071h: SCI3.FRDRL
- 4007 008Fh: SCI4.FTDRL, 4007 0091h: SCI4.FRDRL
- 4007 010Fh: SCI8.FTDRL, 4007 0111h: SCI8.FRDRL
- 4007 012Fh: SCI9.FTDRL, 4007 0131h: SCI9.FRDRL.

32.3 Operation

32.3.1 Basic Operation

The CRC calculator generates CRC codes for use in LSB-first or MSB-first transfers.

The following examples illustrate CRC code generation for input data (F0h) using the 16-bit CRC-CCITT generating polynomial ($X^{16} + X^{12} + X^5 + 1$). In these examples, the value of the CRC Data Output Register (CRCDOR_HA) is cleared before CRC calculation.

When an 8-bit CRC (with the polynomial $X^8 + X^2 + X + 1$) is in use, the valid bits of the CRC code are obtained in CRCDOR_BY. When a 32-bit CRC is in use, the valid bits of the CRC code are obtained in CRCDOR.

Figure 32.2 and Figure 32.3 show the LSB-first and MSB-first data transmission examples respectively, and Figure 32.4 and Figure 32.5 show the LSB-first and MSB-first data reception examples.

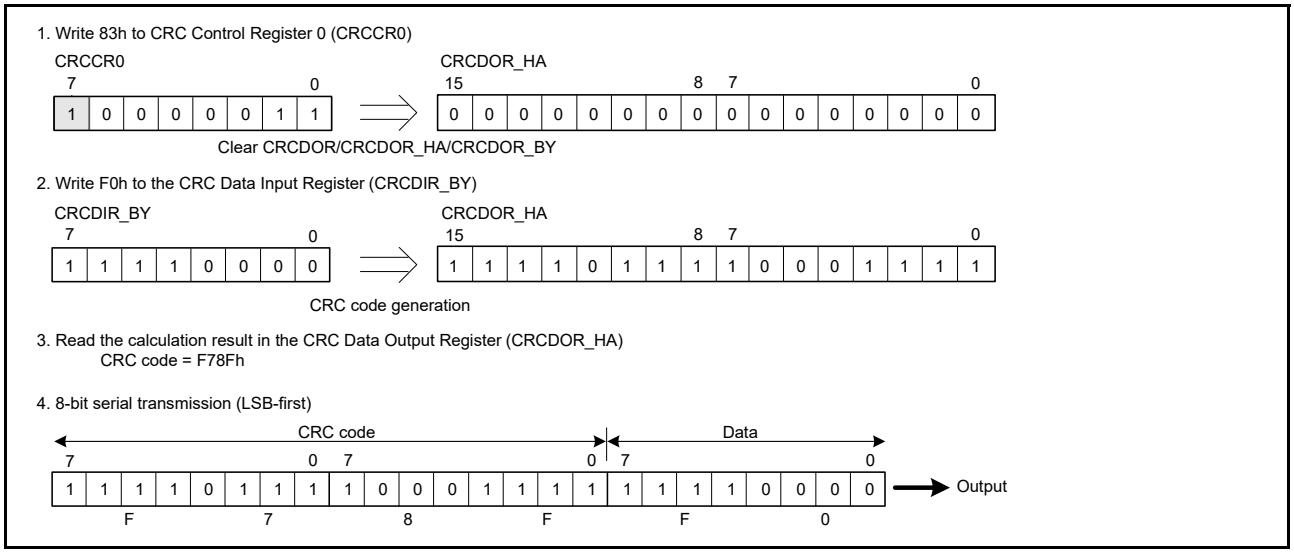


Figure 32.2 LSB-first data transmission

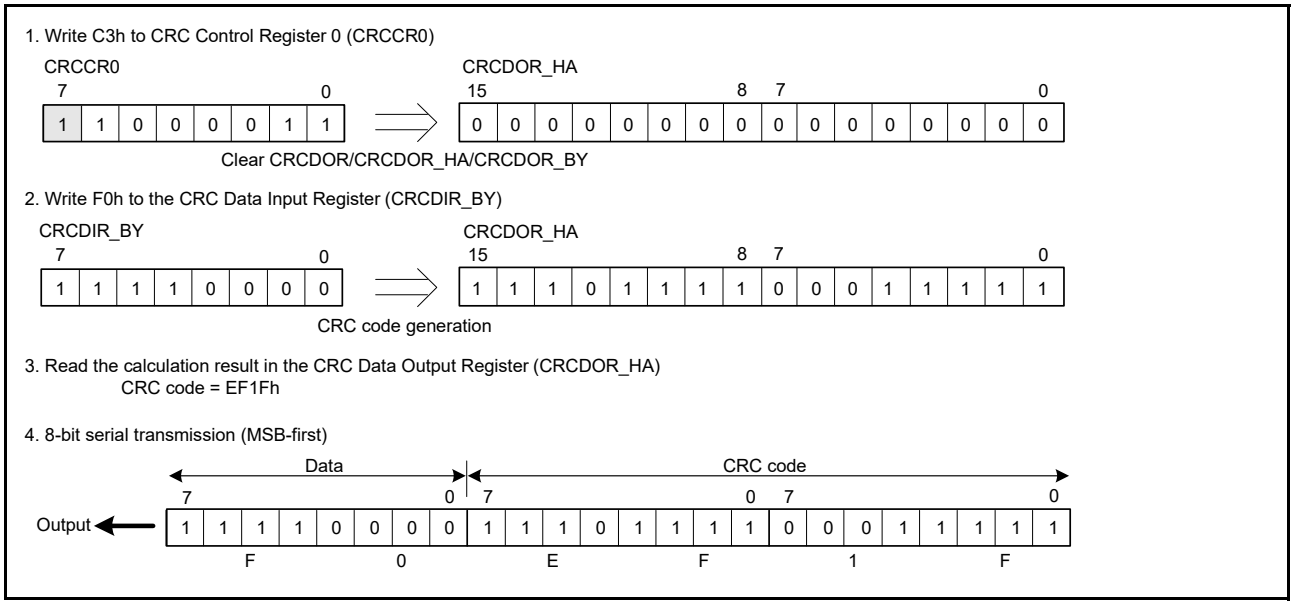


Figure 32.3 MSB-first data transmission

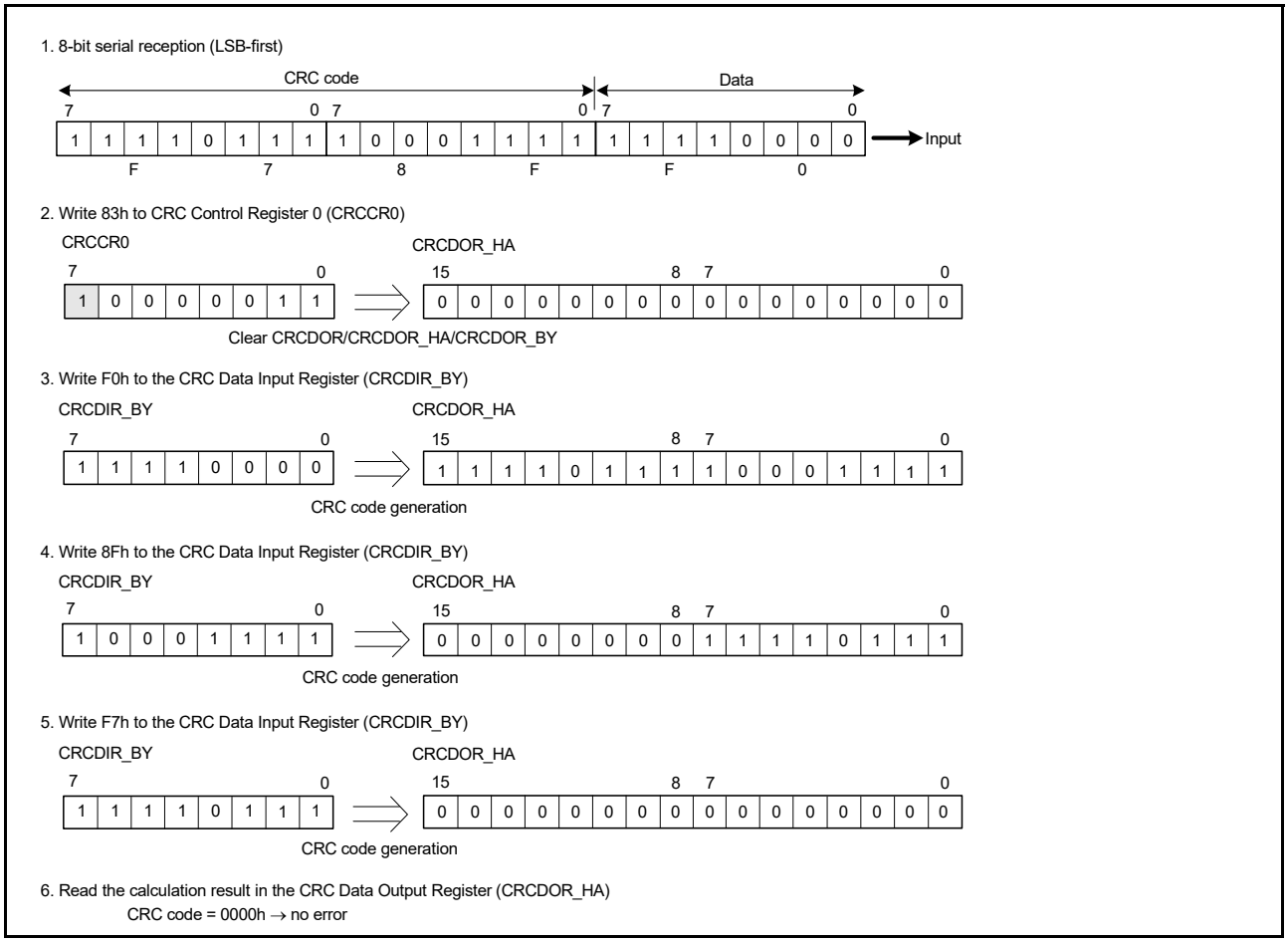


Figure 32.4 LSB-first data reception

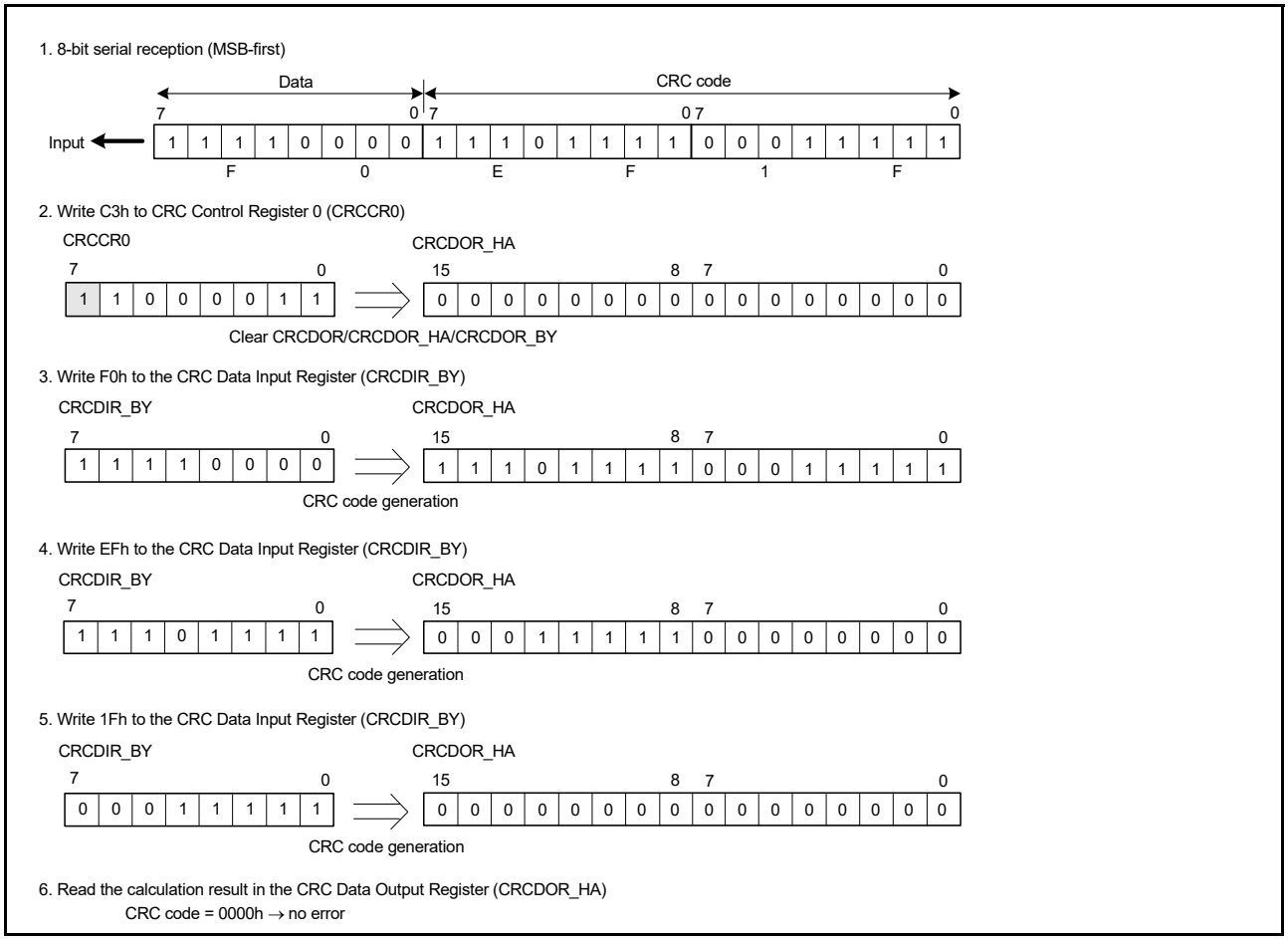


Figure 32.5 MSB-first data reception

32.3.2 CRC Snoop

The CRC snoop function monitors reads from and writes to a specific register address and performs CRC calculations on the data read from and written to the register address automatically. Because the CRC snoop recognizes writes to and reads from a specific register address as a trigger to automatically perform CRC calculations, there is no need to write data to the CRCDIR_BY register. All I/O register addresses specified in section 32.2.5, Snoop Address Register (CRCSAR) are subject to the CRC snoop. The CRC snoop is useful in monitoring writes to the serial transmit buffer, and reads from the serial receive buffer.

To use this function, write a target I/O register address to the CRCSA13 to CRCSA0 bits in the CRCSAR register, and set the CRCSEN bit in the CRCCR1 register to 1. Then, set the CRCSWR bit in the CRCCR1 register to 1 to enable snooping on the writes to the target address, or set the CRCSWR bit in the CRCCR1 register to 0 to enable snooping on the reads from the target address.

When both the CRCSEN and CRCSWR bits are set to 1, and data is written to a target I/O register address in a bus master module such as the CPU, DMAC, and DTC, the CRC calculator stores the data in the CRCDIR_BY register and performs CRC calculation. Similarly, when the CRCSEN bit is set to 1, CRCSWR bit is set to 0, and data is read from a target I/O register address in a bus master module such as the CPU, DMAC, and DTC, the CRC calculator stores the data in the CRCDIR_BY register and performs a CRC calculation.

CRC calculation is performed 1 byte at a time. When the target I/O register address is accessed in words (16 bits) or long words (32 bits), a CRC code is generated on the lower byte (1 byte) of data.

32.4 Usage Notes

32.4.1 Settings for the Module-Stop State

The Module Stop Control Register C (MSTPCRC) can enable or disable the operation of the CRC calculator. The CRC calculator is stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

32.4.2 Note on Transmission

The transmission sequence for the CRC code differs depending on whether transmission is LSB-first or MSB-first. Figure 32.6 shows an LSB-first and MSB-first data transmission.

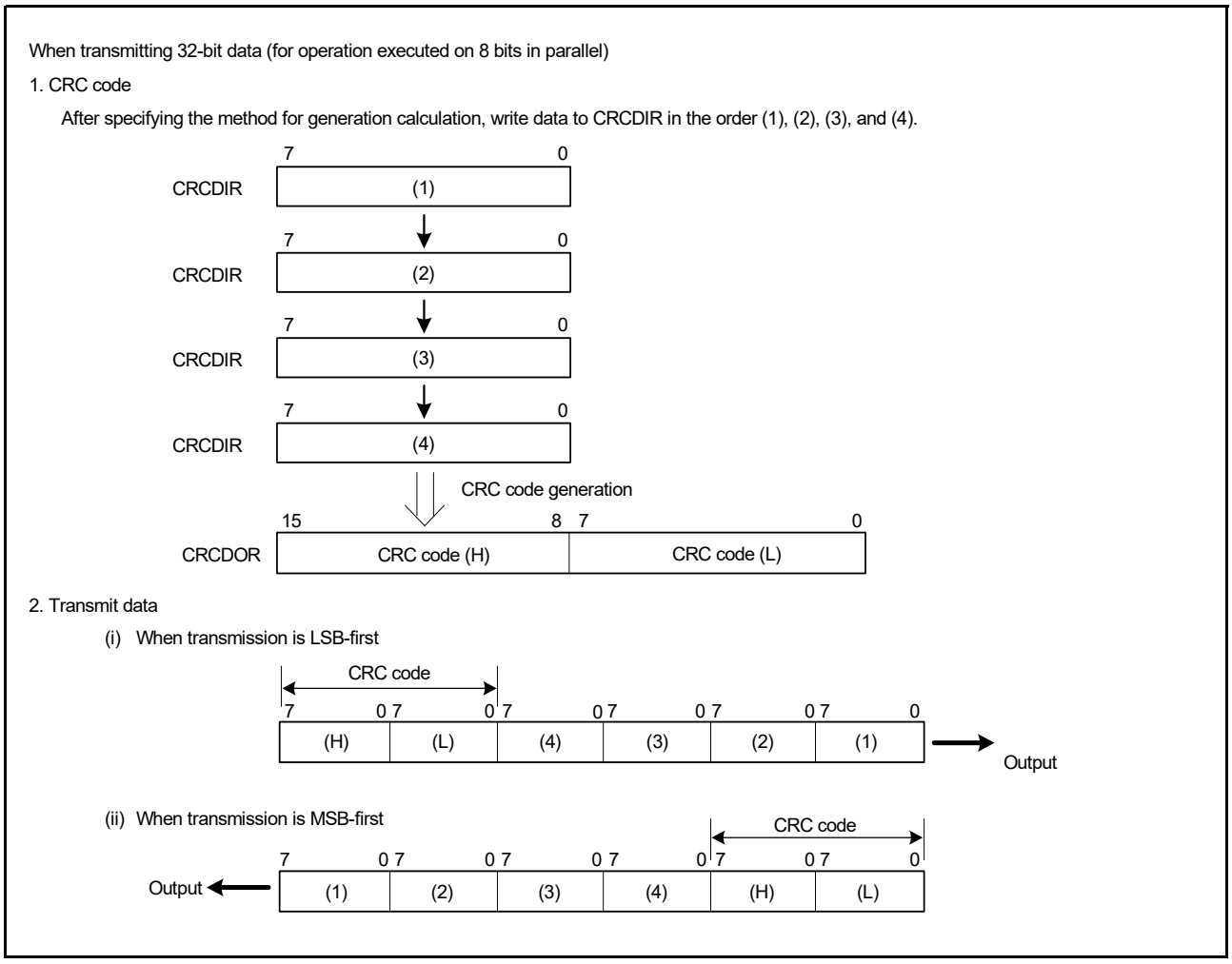


Figure 32.6 LSB-first and MSB-first data transmission

33. Boundary Scan

33.1 Overview

The boundary scan function provides a serial I/O interface based on the JTAG (Joint Test Action Group), IEEE Std. 1149.1, and IEEE Standard Test Access Port, and Boundary Scan Architecture.

Table 33.1 lists the boundary scan specifications, Figure 33.1 shows a block diagram, and Table 33.2 lists the I/O pins.

Table 33.1 Boundary scan specifications

Parameter	Specifications
Execution condition	Boundary scan must be executed when the RES pin is driven low
Test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode.

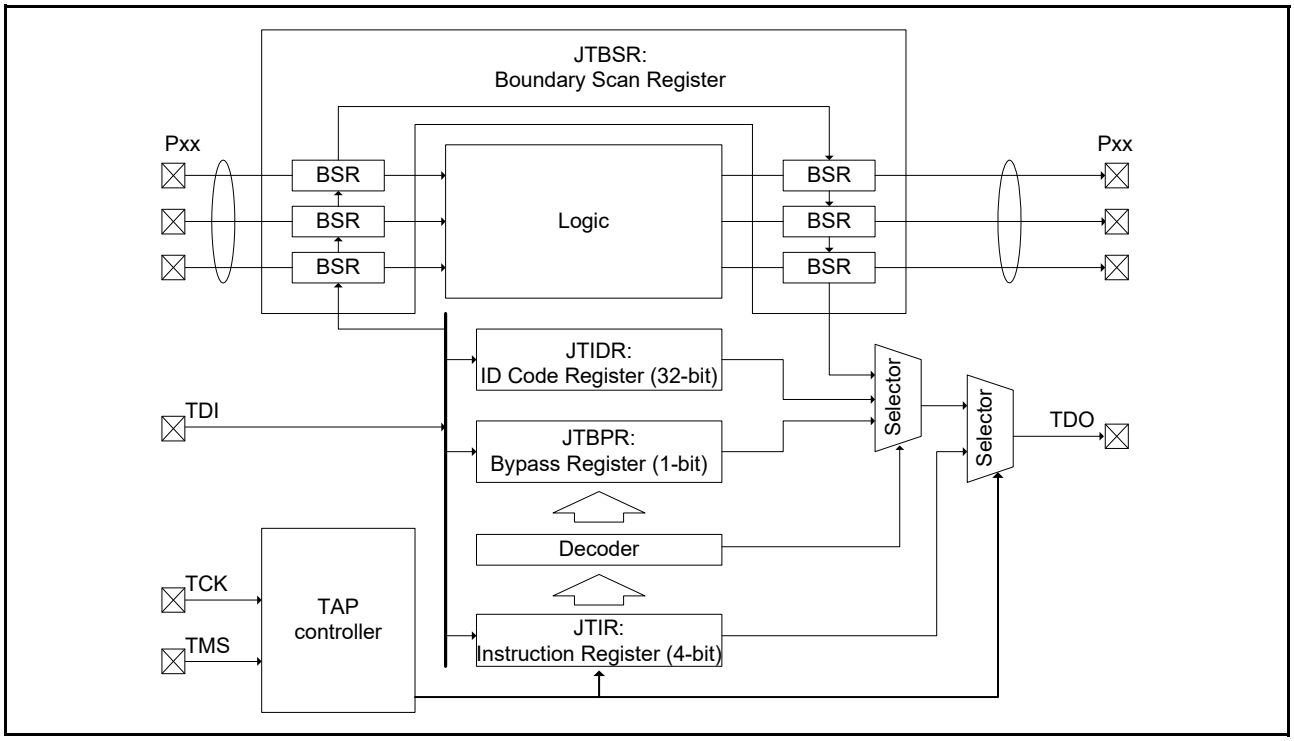


Figure 33.1 Boundary scan function block diagram

Table 33.2 Boundary scan I/O pins

Pin name	I/O	Description
TCK	Input	Test clock input pin. Clock signal for boundary scan. The input clock duty cycle is 50% when the boundary scan function is used.
TMS	Input	Test mode select pin
TDI	Input	Test data input pin
TDO	Output	Test data output pin

Note: This MCU does not support the TRST pin for the JTAG interface.

33.2 Register Descriptions

Table 33.3 lists the boundary scan registers.

Table 33.3 Boundary scan registers

Register name	Symbol	Value after reset
Instruction Register	JTIR	Eh
ID Code Register	JTIDR	083D 8447h
Bypass Register	JTBPR	Undefined
Boundary Scan Register	JTBSR	Undefined

Usage notes for the boundary scan registers:

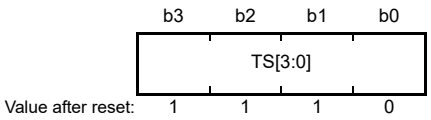
- Instructions can be input to the Instruction Register (JTIR) through the TDI pin by serial transfer
- The Bypass Register (JTBPR), which is a 1-bit register, is connected between the TDI and TDO pins in BYPASS mode
- The Boundary Scan Register (JTBSR), which is configured according to the BSDL description, is connected between the TDI and TDO pins when test data is being shifted in.

Table 33.4 shows the availability of serial transfer for the registers.

Table 33.4 Serial transfer for registers

Register name	Serial input	Serial output
Instruction Register (JTIR)	Available	Available
ID Code Register (JTIDR)	Available	Available
Bypass Register (JTBPR)	Available	Available
Boundary Scan Register (JTBSR)	Available	Available

33.2.1 Instruction Register (JTIR)



Bit	Symbol	Bit name	Description	R/W
b3 to b0	TS[3:0]	Test Bit Set	The command configuration for these bits is shown in Table 33.5	—

Table 33.5 Command configuration

TS3	TS2	TS1	TS0	Instruction
0	0	0	0	EXTEST
0	0	0	1	SAMPLE/PRELOAD
0	0	1	1	IDCODE (Renesas code)
0	1	0	1	CLAMP
0	1	1	0	HIGHZ
1	1	1	1	BYPASS
Other settings				Reserved

JTAG instructions can be transferred to the JTIR register by serial input from the TDI pin. The JTIR register is initialized when a power-on reset occurs, or when the TAP controller is in the Test-Logic-Reset state.

33.2.2 ID Code Register (JTIDR)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DID[31:0]															
Value after reset:	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DID[31:0]															
Value after reset:	1	0	0	0	0	1	0	0	0	1	0	0	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b31 to b0	DID[31:0]	Device ID	These bits store the fixed value that indicates the device IDCODE	—

JTIDR data is output from the TDO pin when the IDCODE instruction is executed. After a reset release, the IDCODE of JTIDR changes into the Arm® debug code. See the *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480F).

33.2.3 Bypass Register (JTBPR)

JTBPR is a 1-bit register and is connected between the TDI and TDO pins when the JTIR register is set to BYPASS mode. The JTBPR register cannot be read from or written to by the CPU.

33.2.4 Boundary Scan Register (JTBSR)

JTBSR is a shift register used for controlling the external input and output pins of the MCU, and is distributed across the pads. To apply the JTBSR register in boundary-scan testing, issue the EXTEST, SAMPLE/PRELOAD, CLAMP, and HIGHZ instructions. The BSDL file describes the associations between the JTBSR bits and the MCU pins. The value after reset is undefined.

33.3 Operation

During a reset, the JTAG ports, TCK, TMS, TDI, and TDO, are assigned as default pin functions. The TCK, TMS, and TDI pins are pulled up by the pull-up resistors. Boundary scan testing can be executed after the setup time elapses, when POR is negated, and RES is driven low.

33.3.1 TAP Controller

Figure 33.2 shows the state transition diagram of the TAP controller. All transitions are controlled by the TMS signal.

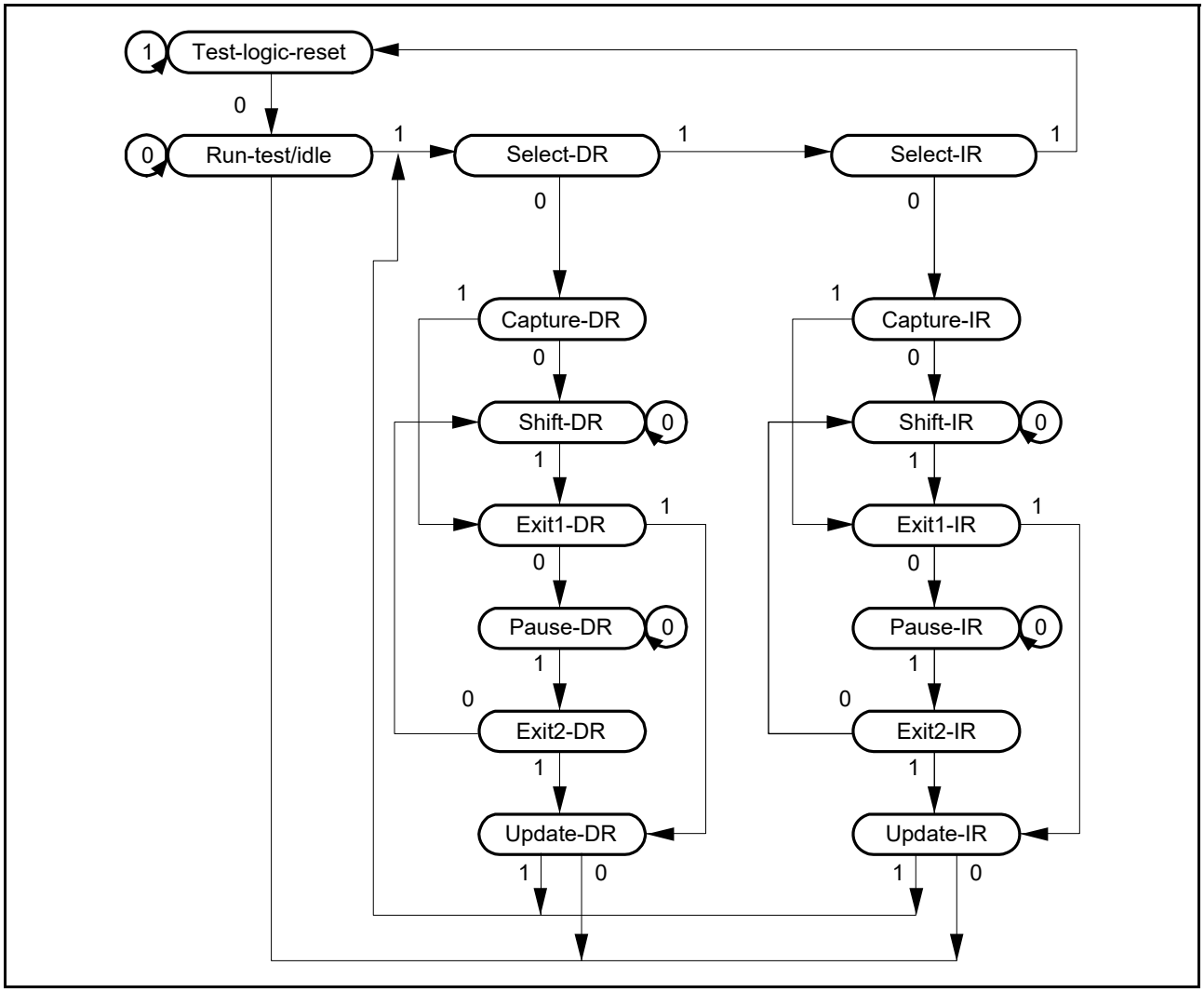


Figure 33.2 State transition diagram of TAP controller

33.3.2 Commands

(1) BYPASS

The BYPASS instruction drives the Bypass Register (JTBPR). This instruction shortens the shift path, facilitating the transfer of serial data to the other LSIs on a printed circuit board at higher speeds. While this instruction is being executed, the test circuit has no effect on the system circuits.

The Bypass Register (JTBPR) is connected between the TDI and TDO pins. Bypass operation is initiated from the Shift-DR operation. The TDO is low in the first clock cycle in the Shift-DR state. In the subsequent clock cycles, the TDI signal is output on the TDO pin.

(2) EXTEST

The EXTEST instruction is used to test external circuits when the MCU is installed on the printed circuit board. If this instruction is executed, the output pins are used to output test data (specified in the SAMPLE/PRELOAD instruction) from the Boundary Scan Register (JTBSR) to the print circuit board, and the input pins are used to input the test result.

(3) SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction is used to input data from the internal circuits of the MCU to the Boundary Scan Register (JTBSR), output data from the scan path, and reload the data to the scan path. While this instruction is executed, the input signals are directly input to the MCU and output signals are also directly output to the external circuits. The MCU system circuit is not affected by this instruction.

In SAMPLE operation, the Boundary Scan Register (JTBSR) latches a snapshot of the data transferred from the input pins to the internal circuit, or data transferred from the internal circuit to the output pins. The latched data is read from the scan path. The JTBSR register latches the data snapshot on the rising edge of the TCK pin in the Capture-DR state. The data snapshot is only transferred from the internal circuit to the output pins during a reset.

In PRELOAD operation, the initial value is written from the scan path to the parallel output latch of the Boundary Scan Register (JTBSR) prior to the EXTEST instruction execution. If EXTEST is executed without executing this PRELOAD operation, undefined values are output from the beginning of the EXTEST sequence to the end (transfer to the output latch). In the EXTEST instruction, output parallel latches are always output to the output pins.

(4) IDCODE

When the IDCODE instruction is selected, the ID Code Register (JTIDR) value is output to the TDO pin in the Shift-DR state of the TAP controller. In this case, the JTIDR register value is output LSB-first. During this instruction execution, the test circuit does not affect the system circuit.

(5) CLAMP

When the CLAMP instruction is selected, the output pins output the Boundary Scan Register (JTBSR) value that was specified in the SAMPLE/PRELOAD instruction in advance. While the CLAMP instruction is selected, the status of the JTBSR register is maintained regardless of the TAP controller state.

The Bypass Register (JTBPR) is connected between the TDI and TDO pins, leading to the same operation as when the BYPASS instruction is selected.

(6) HIGHZ

When the HIGHZ instruction is selected, all output pins enter a high-impedance state. While the HIGHZ instruction is selected, the status of Boundary Scan Register (JTBSR) is maintained regardless of the state of the TAP controller.

The Bypass Register (JTBPR) is connected between the TDI and TDO pins, leading to the same operation as when the BYPASS instruction is selected.

33.4 Usage Notes

The boundary scan function is subject to the following constraints:

- The boundary scan must be executed when the RES pin is driven low
- Serial data input/output is in LSB order, as shown in Figure 33.3.

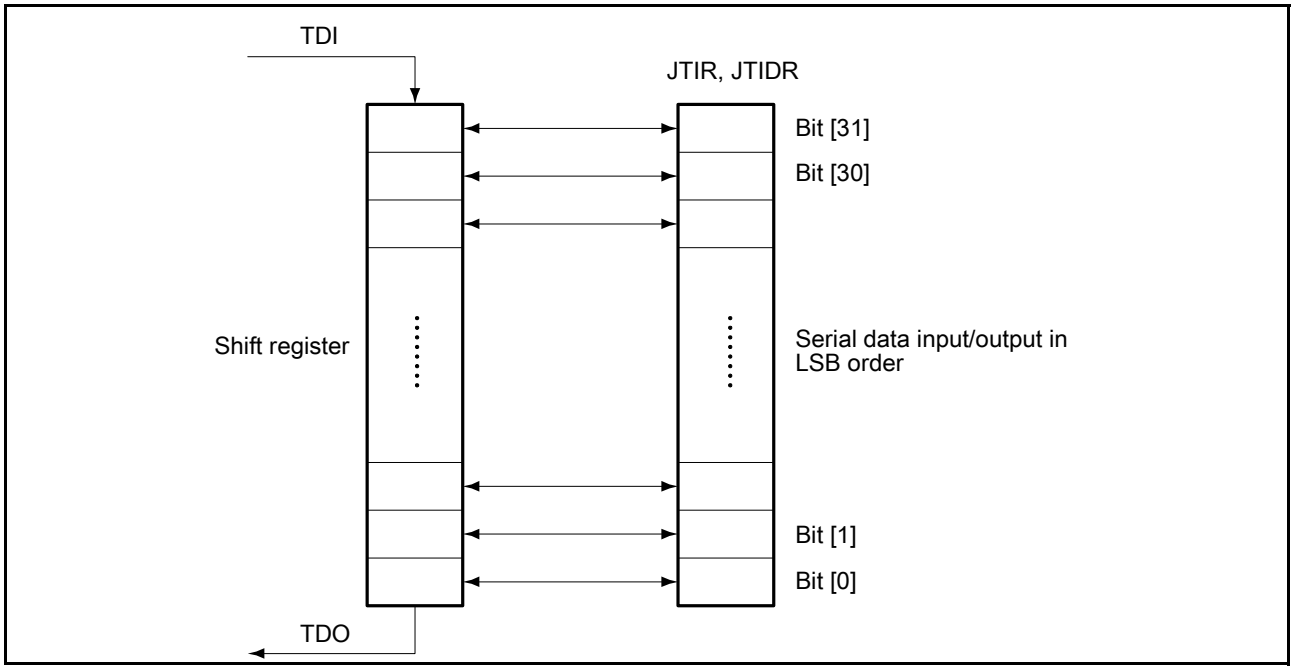


Figure 33.3 Serial data input/output

The following pins cannot be boundary-scanned:

- Power supply pins (VCC, VCL, VCL0, VSS, AVCC0, and AVSS0)
- Analog reference pins (VREFH0, VREFL0, VREFH, and VREFL)
- Clock pins (EXTAL, XTAL, XCIN, and XCOUT)
- Reset signal (RES)
- Boundary-scan pins (TCK, TMS, TDI, and TDO).

34. Secure Cryptographic Engine (SCE7)

34.1 Overview

The MCU incorporates a Secure Cryptographic Engine (SCE7) module to provide security functions. The module consists of an access management circuit, encryption engine, and random number generator.

Table 34.1 shows the SCE7 specifications and Figure 34.1 shows a block diagram.

Table 34.1 SCE7 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE7.
Encryption engine	Advanced Encryption Standard (AES): Compliant with NIST FIPS PUB 197 algorithm • Key sizes: 128, 192, or 256 bits • Block size: 128 bits • Chaining modes ECB, CBC, CTR: Compliant with NIST SP 800-38A GCM: Compliant with NIST SP 800-38D XTS: Compliant with NIST SP 800-38E. GCTR • Throughput for 128-bit data 11 PCLKB cycles for 128-bit key 15 PCLKB cycles for 256-bit key. AES-GCM • AES-GCM is realized by combining AES-GCTR and GHASH. Triple Data Encryption Standard (3DES) • 192-bit key length • Operates on a fixed 8-byte block of data • Used in legacy Secure Socket Layer (SSL) and Transport Layer Security (TLS) protocols. • Throughput for 64-bit data 16 PCLKB cycles for 56-bit key. Alleged RC4 (ARC4) • 2048-bit key length • Throughput for 128-bit data 16 PCLKB cycles for 2048-bit key.
Generation of random numbers	128-bit true random number generator
Signature generation and verification	RSA • Support for 1024-bit and 2048-bit key sizes • Signature generation, signature verification, public-key encryption, private-key decryption. DSA • Support for DSA key sizes: • (1024-bit, 160-bit) • (2048-bit, 224-bit) • (2048-bit, 256-bit). • Signature generation, signature verification. ECC • Support for curve P-192, P-224, P-256, and P-384 • Signature generation, signature verification • Scalar multiplication.
Message digest computation	HASH • SHA1, SHA224, SHA256, and MD5.
Unique ID	• An ID unique to the MCU (unique ID) is accessible from the access management circuit through the dedicated bus • Combining the unique ID with the key generation information prevents illicit copying of data to another MCU.

Table 34.1 SCE7 specifications (2 of 2)

Parameter	Specifications
Privileged mode	• The privileged mode signal is connected to the access management circuit and is used to limit control of the SCE7 module to privileged mode only.
Low power consumption	Setting of the module-stop state is possible

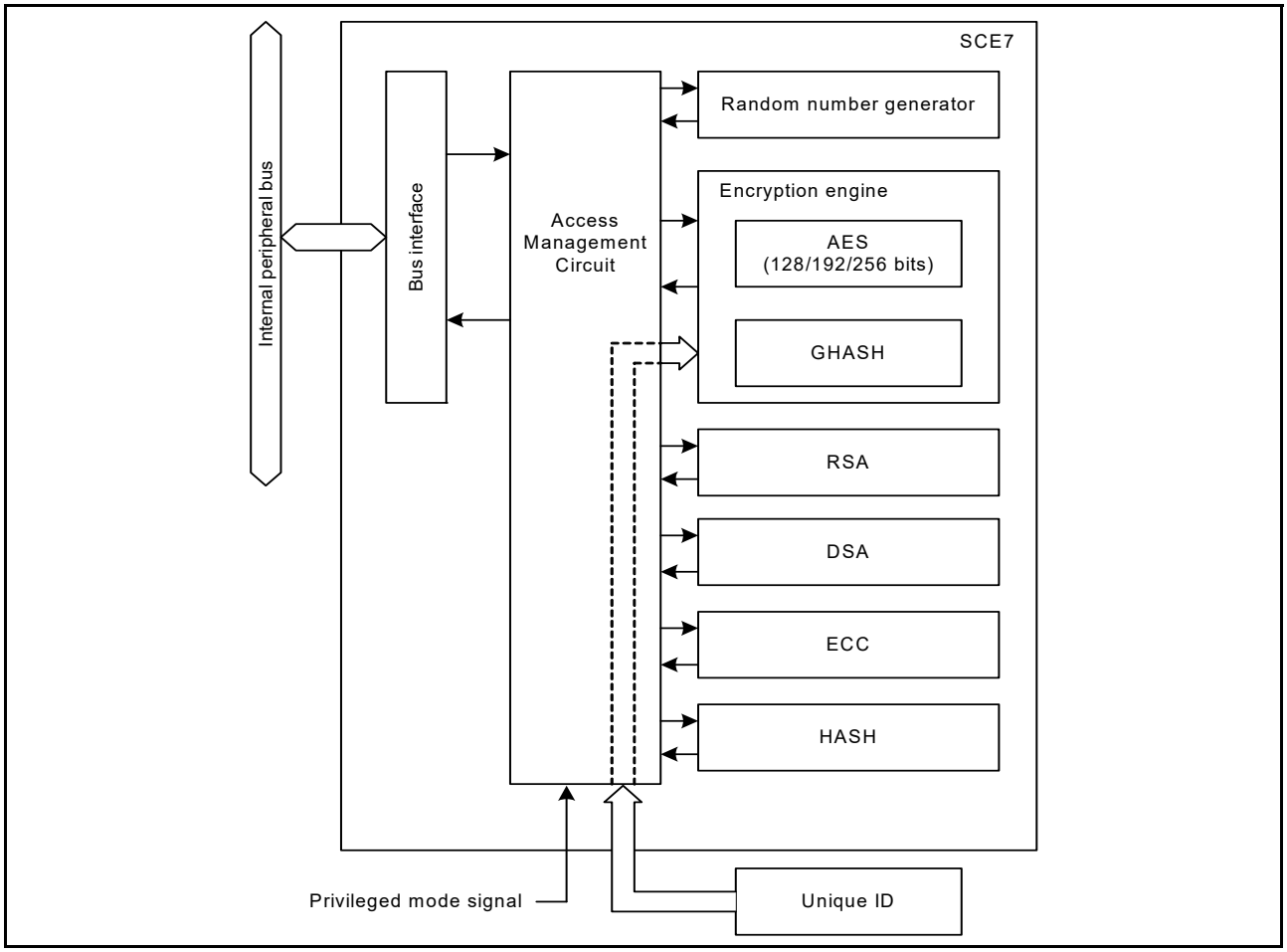


Figure 34.1 SCE7 block diagram

34.2 Operation

34.2.1 Encryption Engine

The encryption engine performs the following operation in hardware, see Figure 34.2:

- Plaintext to ciphertext encryption
- Ciphertext to plaintext decryption.

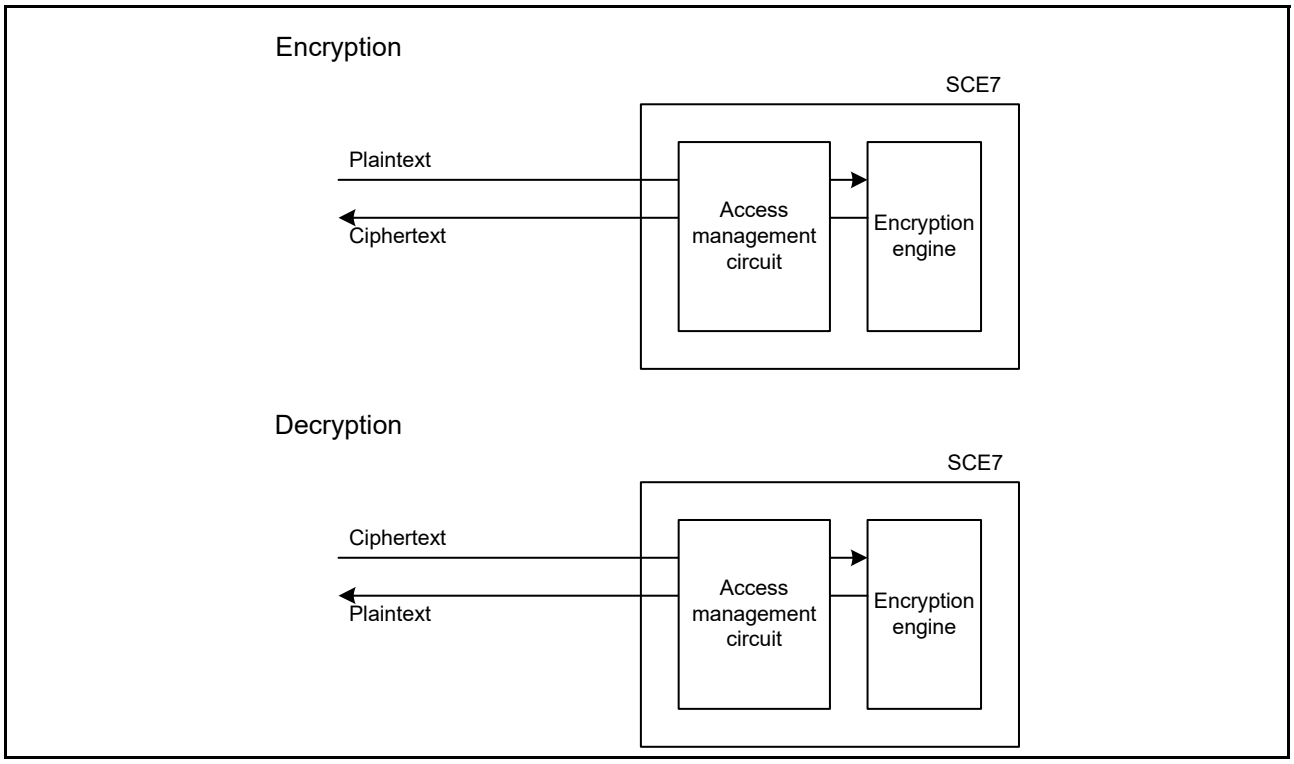


Figure 34.2 Encryption and decryption processes by encryption engine

34.2.2 Encryption and Decryption

To encrypt or decrypt data:

1. Input the data to encrypt or decrypt in the SCE7.
   The SCE7 converts the plaintext data to ciphertext or ciphertext data to plaintext.
2. Read the converted data.

The encryption engine has an input buffer and an output buffer, enabling encryption/decryption to proceed in parallel with data input/output. Figure 34.3 shows the encryption and decryption engine timing.

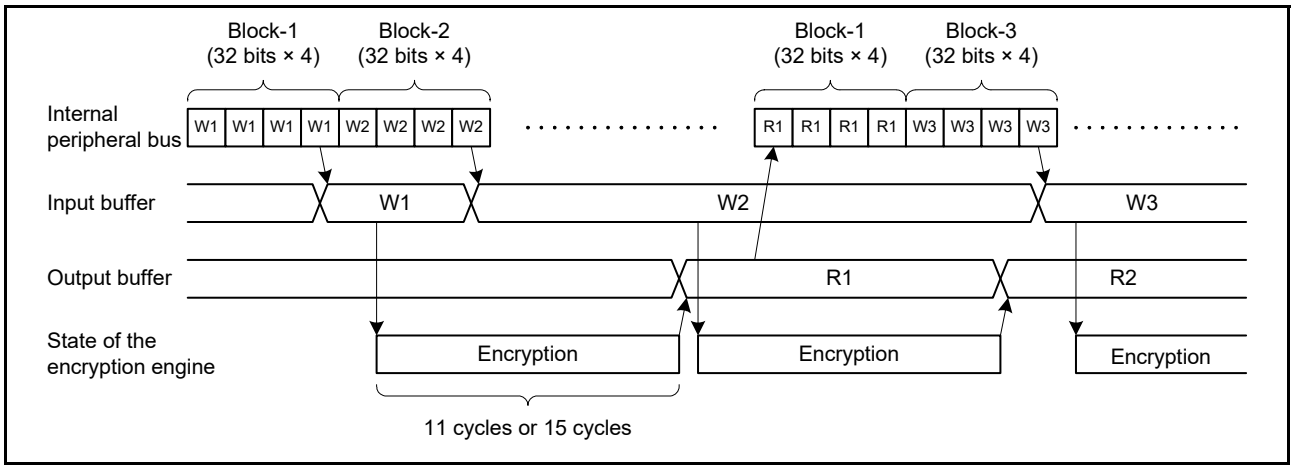


Figure 34.3 Encryption and decryption timing (AES)

34.3 Usage Notes

34.3.1 Software Standby Mode

When Software Standby mode is entered while the encryption engine is processing, proper processing cannot be resumed after exiting Software Standby mode. Software Standby mode should therefore be entered while the encryption engine is not running.

34.3.2 Settings for the Module-Stop Function

SCE7 operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The SCE7 module is initially stopped after reset. Releasing the module-stop state enables access to the registers.

35. 12-Bit A/D Converter (ADC12)

35.1 Overview

The MCU provides two 12-bit successive approximation A/D converter (ADC12) units. In unit 0, up to 11 analog input channels are selectable. In unit 1, up to eight analog input channels, temperature sensor output, and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-, 10-, and 8-bit conversion, making it possible to optimize the trade-off between speed and resolution in generating a digital value.

ADC12 features include:

- 11 channels (unit 0), 8 channels (unit 1)
- PCLKB = 60 MHz (maximum)
- PCLKC = 60 MHz (maximum)
- Analog channels: AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020 (unit 0), AN100 to AN102, AN105 to AN107, AN116, AN117 (unit 1)
- Resolution: 12-bit, 10-bit, 8-bit
- Dedicated sample-and-hold circuit embedded
- Programmable Gain Amplifier embedded.

The ADC12 supports the following operating modes:

- Single scan mode for converting analog inputs of arbitrarily selected channels in ascending order of channel number
- Continuous scan mode for sequentially converting analog inputs of arbitrarily selected channels continuously in ascending order of channel number
- Group scan mode for arbitrarily dividing the analog inputs of channels into two groups (A and B) and converting the analog input of the selected channel for each group in ascending order of channel number.

In group scan mode, you can start group A and group B A/D conversion at different times by individually selecting their scan start conditions. In addition, when a priority control operation for group A is set, ADC12 accepts group A scan starting during group B A/D conversion, suspending group B conversion. This allows you to assign higher priority to A/D conversion start for group A.

In double trigger mode, the analog input of an arbitrarily selected channel is converted in single scan mode or group scan mode (group A), and the data converted by the first and second A/D conversion start triggers are stored in different registers, providing duplexing of A/D-converted data.

Self-diagnosis is performed once at the beginning of each scan, and one of the three voltage values generated in ADC12 is A/D-converted.

The temperature sensor output and internal reference voltage are selectable at the same time as the analog input of the channel. A/D conversion is performed first for the analog input of the channel, next for the temperature sensor output, and then for the internal reference voltage.

The ADC12 provides a compare function (window A and window B). This compare function specifies the upper reference value for window A and lower reference value for window B, and outputs an interrupt request when the A/D-converted value of the selected channel meets the comparison conditions.

Table 35.1 lists the ADC12 specifications, Table 35.2 list the functions, and Table 35.3 lists the I/O pins. Figure 35.1 shows a block diagram of ADC12 unit 0, and Figure 35.2 shows a block diagram of ADC12 unit 1.

Table 35.1 ADC12 specifications (1 of 3)

Parameter	Specifications
Number of units	Two units, 0 and 1
Input channels	• Unit 0: Up to 11 channels • Unit 1: Up to 8 channels.

Table 35.1 ADC12 specifications (2 of 3)

Parameter	Specifications
Extended analog function	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method
Resolution	12 bits, selectable to 12-bit, 10-bit, or 8-bit conversion
Conversion time	0.4 µs/channel, when A/D conversion clock PCLKC (ADCLK) is operating at 60 MHz. See Table 43.27 and Table 43.28 about the condition.
A/D conversion clock	Peripheral module clock PCLKB*1 and A/D conversion clock PCLKC (ADCLK)*1 can be set with the following division ratios: PCLKB to PCLKC (ADCLK) frequency ratios = 1:1, 2:1, 4:1, 8:1, 1:2, 1:4
Data registers	• 19 registers for analog input (11 for unit 0, 8 for unit 1), one for A/D-converted data duplication in double trigger mode in each unit, and two for A/D-converted data duplication in extended operation in double trigger mode in each unit • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • A/D conversion results are stored in A/D data registers • 8-, 10-, and 12-bit accuracy output for A/D conversion results • A/D-converted value addition mode, in which the sum of all A/D conversion results are stored in the A/D data registers as the conversion accuracy bit count + 2 bits.*4 • Double trigger mode (selectable in single scan and group scan modes): The first unit of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second unit is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register provided for the associated trigger.
Operating modes	• Single scan mode: - A/D conversion is performed only once on the analog inputs of arbitrarily selected channels, the temperature sensor output, and the internal reference voltage. • Continuous scan mode: - A/D conversion is performed repeatedly on the analog inputs of arbitrarily selected channels, the temperature sensor output, and the internal reference voltage. • Group scan mode: -A/D conversion is performed only once on the analog inputs of arbitrarily selected channels divided into group A and group B, the temperature sensor output, and the internal reference voltage -The scan start conditions can be independently selected for group A and group B, allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): -If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B stops and A/D conversion is processed on group A. -Restart (rescan) of group B conversion after completion of group A conversion can be set.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger from the Event Link Controller (ELC) • Asynchronous trigger from the external trigger pins, ADTRG0 (unit 0) and ADTRG1 (unit 1).
Functions	• Dedicated sample-and-hold function with optional constant sampling and 3 channels in units 0 and 1 • Variable sampling state count • Self-diagnosis of ADC12 • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge and precharge functions) • Double trigger mode (duplication of A/D conversion data) • Switching function for 8-, 10-, and 12-bit conversion*2 • Automatic clear function for A/D data registers • Digital comparison of values in the comparison and data registers, and between values in the data registers.
Programmable gain amplifier	• Amplification of analog input signals to enable A/D conversion, with 3 channels in units 0 and 1 • Compatible with single end input and pseudo-differential input.
Interrupt sources and ELC events	• ADC12i_ADI: A/D scan end interrupt • ADC12i_GBADI: A/D scan end interrupt for group B • ADC12i_CMPAI: window A compare match • ADC12i_CMPBI: window B compare match • ADC12i_WCMPM: compare match • ADC12i_WCMPUM: compare mismatch.

Table 35.1 ADC12 specifications (3 of 3)

Parameter	Specifications
ELC interface	Scan can be started by a trigger from the ELC
Bus interface	Bus clock synchronized with peripheral clock (PCLKB), maximum frequency = 60 MHz
Reference voltage	• Unit 0: - VREFH0 is the high potential reference voltage - VREFL0 is the low potential reference voltage. • Unit 1: - VREFH is the high potential reference voltage - VREFL is the low potential reference voltage.
Module-stop function	Module-stop state can be set to reduce power consumption*3

i = 0 for unit 0, and i = 1 for unit 1.

Note 1. Peripheral module clock PCLKB is specified in the SCKDIVCR.PCKB[2:0] bits, and A/D conversion clock ADCLK in the SCKDIVCR.PCKC[2:0] bits in units 0 and 1.
Note 2. Changing the A/D conversion accuracy also changes the A/D conversion time. For details, see section 35.3.6, Analog Input Sampling and Scan Conversion Time.
Note 3. For details, see section 11, Low Power Modes.
Note 4. The number of extended bits for addition varies with the A/D conversion accuracy and the number of addition times. A 2-bit extension is up to 4 times conversion (3 times addition) when the A/D conversion accuracy is 8, 10, or 12 bits. A 4-bit extension is 16 times conversion (15 times addition) when the A/D conversion accuracy is 12 bits.

Table 35.2 ADC12 functions

Parameter			Unit 0 (ADC120)	Unit 1 (ADC121)
Analog input channel			AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020 Internal reference voltage Temperature sensor output	AN100 to AN102, AN105 to AN107, AN116, AN117 Internal reference voltage Temperature sensor output
Conditions for A/D conversion start	Software	Software trigger	Enabled	Enabled
	External trigger	Trigger input pin	ADTRG0	ADTRG1
	Synchronous trigger (trigger from ELC)	ELC trigger	ELC_AD00, ELC_AD01	ELC_AD10, ELC_AD11
Channel-dedicated sample-and-hold function	Target channel		AN000 to AN002	AN100 to AN102
Programmable gain amplifier	Target channel		AN000 to AN002	AN100 to AN102
	Pseudo-differential input pin		PGAVSS000	PGAVSS100
Interrupt			ADC120_ADI ADC120_GBADI ADC120_CMPAI ADC120_CMPBI	ADC121_ADI ADC121_GBADI ADC121_CMPAI ADC121_CMPBI
Output to ELC			ADC120_ADI ADC120_WCMPM ADC120_WCMPUM	ADC121_ADI ADC121_WCMPM ADC121_WCMPUM
Module-stop function settings*1, *2			MSTPCRD.MSTPD16 bit	MSTPCRD.MSTPD15 bit

Note 1. For details, see section 11, Low Power Modes.
Note 2. Wait for 1 µs or longer to start A/D conversion after release from the module-stop state.

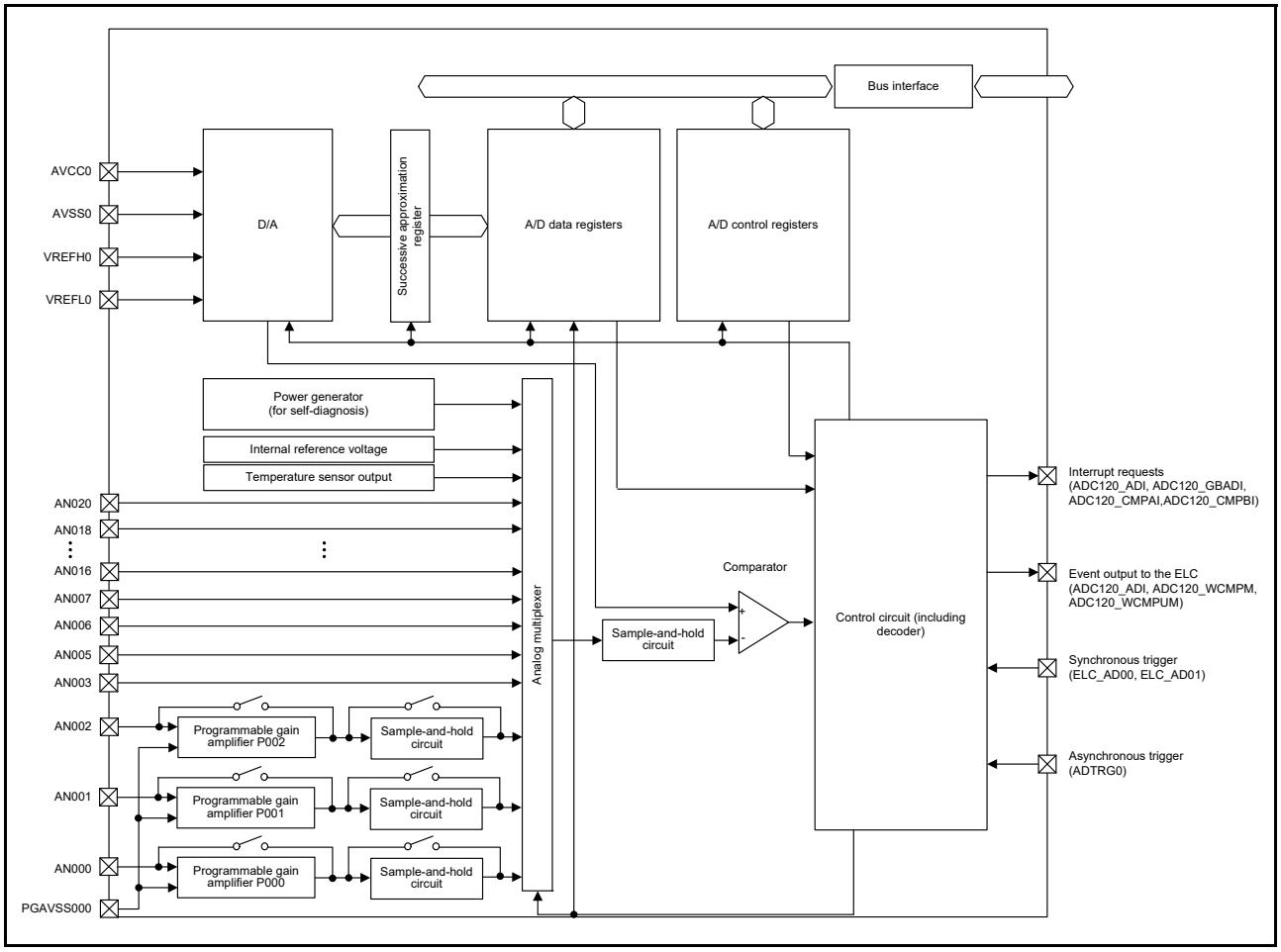


Figure 35.1 ADC12 unit 0 block diagram

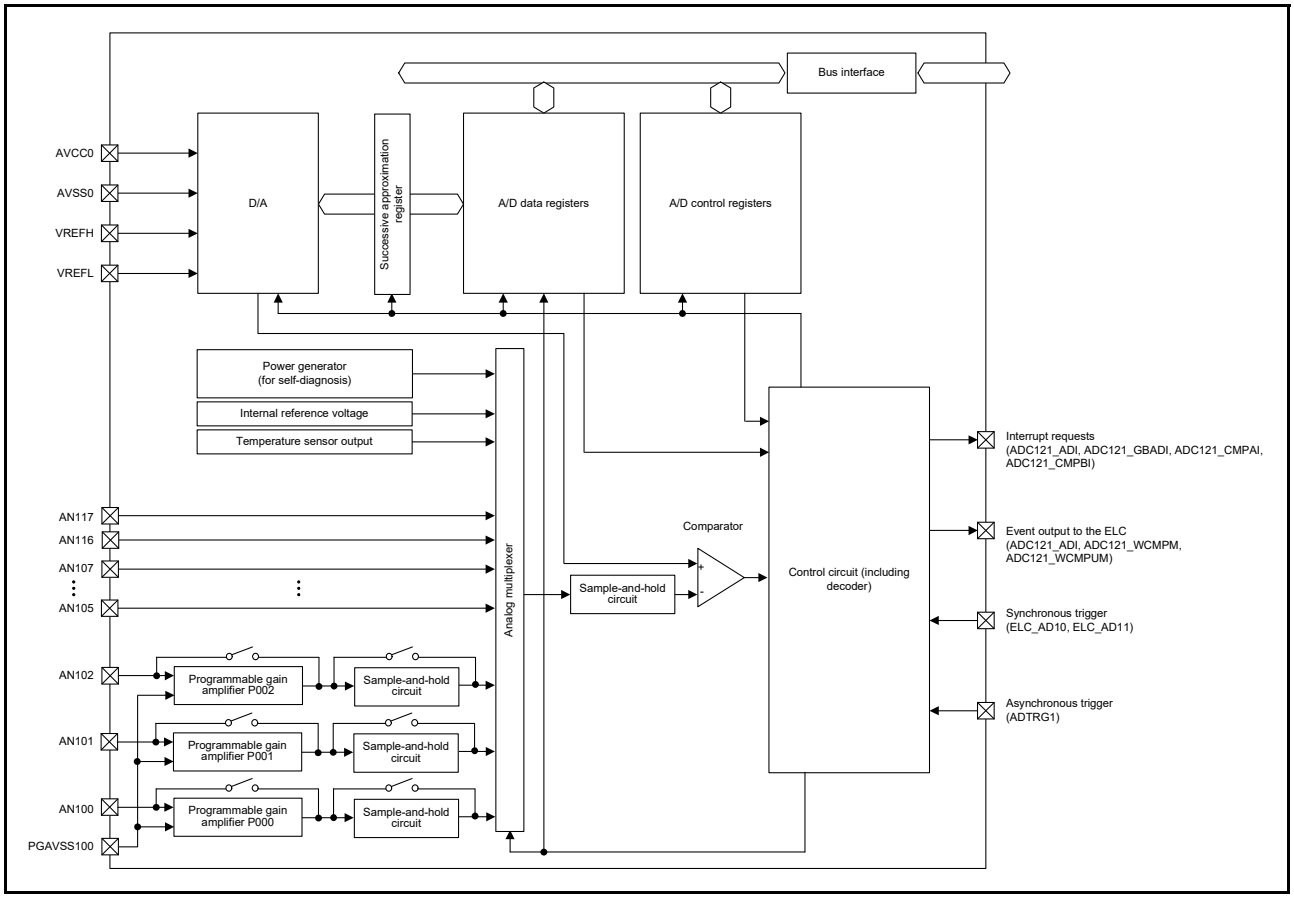


Figure 35.2 ADC12 unit 1 block diagram

Table 35.3 ADC12 I/O pins

Unit	Pin name	I/O	Function
Unit 0	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin
	AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020	Input	Analog input pins 0 to 3, 5 to 7, 16 to 18, and 20
	ADTRG0	Input	External trigger input pin for starting A/D conversion, active low
	PGAVSS000	Input	Pseudo-differential input pin
Unit 1	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH	Input	Reference power supply pin for ADC12 unit 1 and DAC
	VRELF	Input	Reference power supply ground pin for ADC12 unit 1 and DAC
	AN100 to AN102, AN105 to AN107, AN116, AN117	Input	Analog input pins 0 to 2, 5 to 7, 16, and 17
	ADTRG1	Input	External trigger input pin for starting A/D conversion, active low
	PGAVSS100	Input	Pseudo-differential input pin

35.2 Register Descriptions

35.2.1 A/D Data Registers y (ADDRy), A/D Data Duplexing Register (ADDBLDR), A/D Data Duplexing Register A (ADDBLDRA), A/D Data Duplexing Register B (ADDBLDRB), A/D Temperature Sensor Data Register (ADTSDR), A/D Internal Reference Voltage Data Register (ADOCDR)

The data registers include:

- ADDRy registers (y = 0 to 3, 5 to 7, 16 to 18, 20 in unit 0, and y = 0 to 2, 5 to 7, 16, 17 in unit 1): 16-bit read-only registers for storing the A/D conversion results
- ADDBLDR register: 16-bit read-only register for storing the A/D conversion results in response to the second trigger in double trigger mode
- ADDBLDRA and ADDBLDRB registers: 16-bit read-only registers for storing the A/D conversion results in response to the respective triggers during extended operation in double trigger mode
- ADTSDR register: 16-bit read-only register for storing the A/D conversion result of the temperature sensor output
- ADOCDR register: 16-bit read-only register for storing the A/D result of the internal reference voltage.

The following conditions determine the formats for data in the preceding registers:

- The setting in the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right setting)
- The setting in the A/D Conversion Accuracy Specify bits (ADCER.ADPRC[1:0]) (8-, 10-, or 12-bit setting).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

The data formats for each condition are as follows:

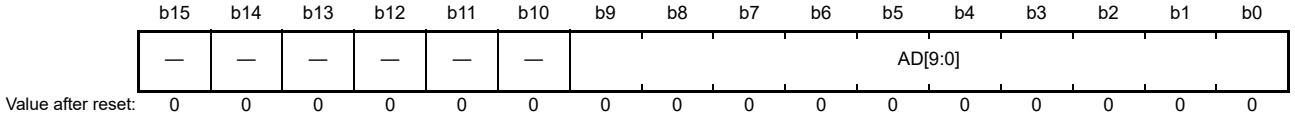
Settings for flush-right data with 12-bit accuracy

Address(es): ADC120.ADDR0 4005 C020h to ADC120.ADDR3 4005 C026h, ADC120.ADDR5 4005 C02Ah to ADC120.ADDR7 4005 C02Eh, ADC120.ADDR16 4005 C040h to ADC120.ADDR18 4005 C044h, ADC120.ADDR20 4005 C048h, ADC120.ADDBLDR 4005 C018h, ADC120.ADDBLDRA 4005 C084h, ADC120.ADDBLDRB 4005 C086h, ADC120.ADTSDR 4005 C01Ah, ADC120.ADOCDR 4005 C01Ch, ADC121.ADDR0 4005 C220h to ADC121.ADDR2 4005 C224h, ADC121.ADDR5 4005 C22Ah to ADC121.ADDR7 4005 C22Eh, ADC121.ADDR16 4005 C240h, ADC121.ADDR17 4005 C242h, ADC121.ADDBLDR 4005 C218h, ADC121.ADDBLDRA 4005 C284h, ADC121.ADDBLDRB 4005 C286h, ADC121.ADTSDR 4005 C21Ah, ADC121.ADOCDR 4005 C21Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

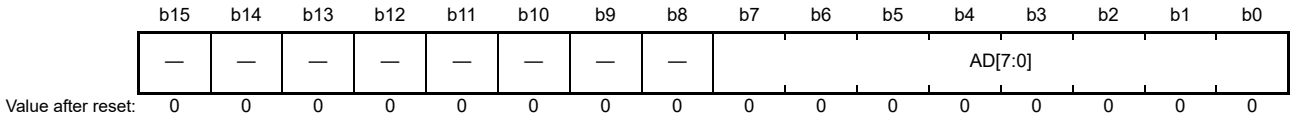
Bit	Symbol	Bit name	Description	R/W
b11 to b0	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R
b15 to b12	—	Reserved	These bits are read as 0	R

Settings for flush-right data with 10-bit accuracy



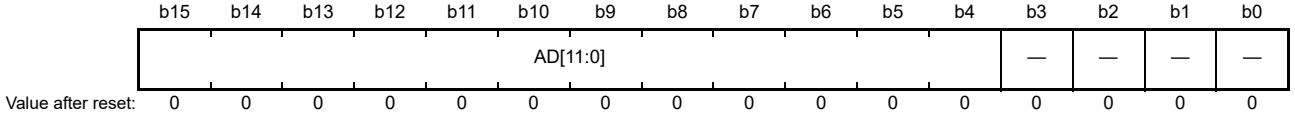
Bit	Symbol	Bit name	Description	R/W
b9 to b0	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value	R
b15 to b10	—	Reserved	These bits are read as 0	R

Settings for flush-right data with 8-bit accuracy



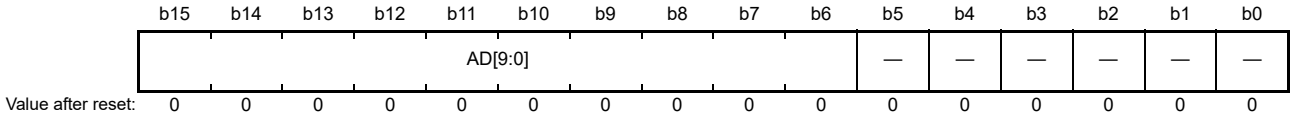
Bit	Symbol	Bit name	Description	R/W
b7 to b0	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value	R
b15 to b8	—	Reserved	These bits are read as 0	R

Settings for flush-left data with 12-bit accuracy



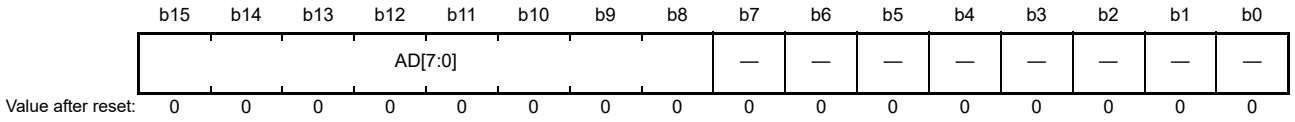
Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0	R
b15 to b4	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R

Settings for flush-left data with 10-bit accuracy



Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0	R
b15 to b6	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value	R

Settings for flush-left data with 8-bit accuracy



Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0	R
b15 to b8	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value	R

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in A/D-converted value addition mode. When A/D-converted value average mode is selected, this register indicates the mean of the A/D-converted values on the specified channel. The value is stored in the A/D data register based on the setting in the A/D Data Register Format Select bit in the same way as in normal A/D conversion.

(3) When A/D-converted value addition mode is selected

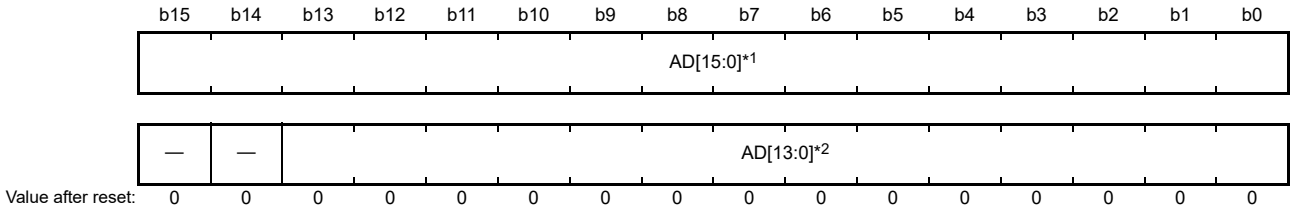
For 8-, 10-, or 12-bit accuracy (ADPRC bit setting), 1, 2, 3 or 4 times can be selected for A/D-converted value addition. 16 times can also be selected for addition mode, but only with 12-bit accuracy selected. In addition mode, this register indicates the value that is obtained by adding the A/D-converted values on a specific channel. The conversion results sum is retained in the A/D data register as a 2-bit-extended value of the conversion accuracy specified. The value is stored in the A/D data register based on the setting in the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

When converting 1, 2, 3, or 4 times in addition mode with 8-, 10-, or 12-bit accuracy specified, the conversion result is stored in the A/D data register as a 2-bit-extended value with the specified accuracy.

When converting 16 times in addition mode with 12-bit accuracy specified, the conversion result is stored in the A/D data register as a 4-bit-extended value with the specified accuracy.

The data formats for each condition are as follows.

Settings for flush-right data with 12-bit accuracy in A/D-converted value addition mode



Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]*1	Added Value 15 to 0	16-bit sum of A/D conversion results	R

Bit	Symbol	Bit name	Description	R/W
b13 to b0	AD[13:0]*2	Added Value 13 to 0	14-bit sum of A/D conversion results	R
b15, b14	—	Reserved	These bits are read as 0	R

Note 1. Used when 16 conversion times is specified in A/D-converted value addition mode.
Note 2. Used when 1, 2, 3, or 4 conversion times is specified in A/D-converted value addition mode.

Settings for flush-right data with 10-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	AD[11:0]	Added Value 11 to 0	12-bit sum of A/D conversion results	R
b15 to b12	—	Reserved	These bits are read as 0	R

Settings for flush-right data with 8-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	AD[9:0]	Added Value 9 to 0	10-bit sum of A/D conversion results	R
b15 to b10	—	Reserved	These bits are read as 0	R

Settings for flush-left data with 12-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[15:0]*1															
	AD[13:0]*2														—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]*1	Added Value 15 to 0	16-bit sum of A/D conversion results	R

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0	R
b15 to b2	AD[13:0]*2	Added Value 13 o 0	14-bit sum of A/D conversion results	R

Note 1. Used when 16 conversion times is selected in A/D-converted value addition mode.
Note 2. Used when 1, 2, 3, or 4 conversion times is selected in A/D-converted value addition mode.

Settings for flush-left data with 10-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0	R
b15 to b4	AD[11:0]	Added Value 11 to 0	12-bit sum of A/D conversion results	R

Settings for flush-left data with 8-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0	R
b15 to b6	AD[9:0]	Added Value 9 to 0	10-bit sum of A/D conversion results	R

35.2.2 A/D Self-Diagnosis Data Register (ADRD)

ADRD is a 16-bit read-only register that holds the A/D conversion results based on the self-diagnosis of the ADC12. In addition to the AD[11:0] bits indicating the A/D-converted value, it includes the Self-diagnosis Status (DIAGST) bit.

The following conditions determine the formats for data in this register:

- Setting in the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right setting)
- Setting in the A/D Conversion Accuracy Specify bits (ADCER.ADPRC[1:0]) (8-, 10-, or 12-bit setting).

The A/D-converted value addition and average modes cannot be applied to the A/D self-diagnosis function. For details on self-diagnosis, see section 35.2.11, A/D Control Extended Register (ADCER).

This section describes the data formats for each condition.

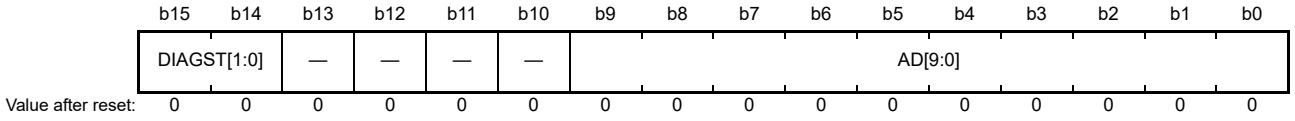
Settings for flush-right data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R
b13, b12	—	Reserved	These bits are read as 0	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis was executed using the 0 V voltage 1 0: Self-diagnosis was executed using the reference power supply*1 voltage x 1/2 1 1: Self-diagnosis was executed using the reference power supply*1 voltage. For details on self-diagnosis, see section 35.2.11, A/D Control Extended Register (ADCER).	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

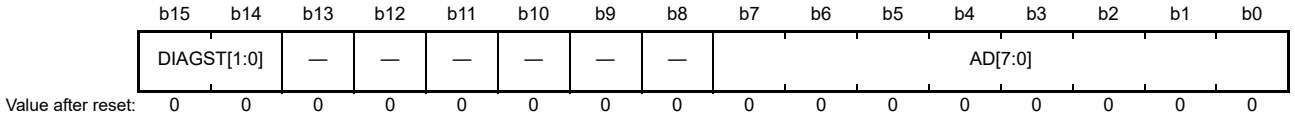
Settings for flush-right data with 10-bit accuracy



Bit	Symbol	Bit name	Description	R/W
b9 to b0	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value	R
b13 to b10	—	Reserved	These bits are read as 0	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis executed using the 0 V voltage 1 0: Self-diagnosis executed using the reference power supply*1 voltage x 1/2 1 1: Self-diagnosis executed using the reference power supply*1 voltage For details on self-diagnosis, see section 35.2.11, A/D Control Extended Register (ADCER).	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

Settings for flush-right data with 8-bit accuracy



Bit	Symbol	Bit name	Description	R/W
b7 to b0	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value	R
b13 to b8	—	Reserved	These bits are read as 0	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis executed using the 0 V voltage 1 0: Self-diagnosis executed using the reference power supply*1 voltage x 1/2 1 1: Self-diagnosis executed using the reference power supply*1 voltage. For details on self-diagnosis, see section 35.2.11, A/D Control Extended Register (ADCER).	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

Settings for flush-left data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis executed using the voltage of 0 V 1 0: Self-diagnosis executed using the voltage of reference power supply*1 × 1/2 1 1: Self-diagnosis executed using the voltage of reference power supply*1. For details on self-diagnosis, see section 35.2.11, A/D Control Extended Register (ADCER).	R
b3, b2	—	Reserved	These bits are read as 0	R
b15 to b4	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

Settings for flush-left data with 10-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis executed using the 0 V voltage 1 0: Self-diagnosis executed using the reference power supply*1 × 1/2 voltage 1 1: Self-diagnosis executed using the reference power supply*1 voltage. For details on self-diagnosis, see section 35.2.11, A/D Control Extended Register (ADCER).	R
b5 to b2	—	Reserved	These bits are read as 0	R
b15 to b6	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

Settings for flush-left data with 8-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[7:0]								—	—	—	—	—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis executed using the 0 V voltage 1 0: Self-diagnosis executed using the reference power supply*1 × 1/2 voltage 1 1: Self-diagnosis executed using the reference power supply*1 voltage. For details on self-diagnosis, see section 35.2.11, A/D Control Extended Register (ADCER).	R
b7 to b2	—	Reserved	These bits are read as 0	R
b15 to b8	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

35.2.3 A/D Control Register (ADCSR)

Address(es): ADC120.ADCSR 4005 C000h, ADC121.ADCSR 4005 C200h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS[1:0]		—			TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DBLANS[4:0]	Double Trigger Channel Select	These bits select one analog input channel for double-triggered operation. The setting is only valid in double trigger mode.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	GBADIE	Group B Scan End Interrupt and ELC Event Enable	0: Disable ADC12i_GBADI interrupt generation on group B scan completion 1: Enable ADC12i_GBADI interrupt generation on group B scan completion. Group B scan only works in group scan mode.	R/W
b7	DBLE	Double Trigger Mode Select	0: Deselect double trigger mode 1: Select double trigger mode.	R/W
b8	EXTRG	Trigger Select*1	0: Start A/D conversion by a synchronous trigger (ELC) 1: Start A/D conversion by the asynchronous trigger (ADTRGi).	R/W
b9	TRGE	Trigger Start Enable	0: Disable A/D conversion to be started by the synchronous or asynchronous trigger 1: Enable A/D conversion to be started by the synchronous or asynchronous trigger.	R/W
b12 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14, b13	ADCS[1:0]	Scan Mode Select	b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited.	R/W
b15	ADST	A/D Conversion Start	0: Stop A/D conversion process 1: Start A/D conversion process.	R/W

i = 0 for unit 0, and i = 1 for unit 1.

Note 1. To start A/D conversion using an external pin (asynchronous trigger):
After a high-level signal is input to the external pin (ADTRG0 in unit 0; ADTRG1 in unit 1), write 1 to both the TRGE and EXTRG bits in ADCSR and drive the external pin signals low. With these settings, the scan conversion process starts on detection of the falling edge of ADTRG0 in unit 0 and ADTRG1 in unit 1. For this configuration, the pulse width of the low-level input must be at least 1.5 PCLKB clock cycles.

DBLANS[4:0] bits (Double Trigger Channel Select)

The DBLANS[4:0] bits select one of the channels for A/D conversion data duplication in double trigger mode. The A/D conversion results from the specified analog input channel are stored in A/D Data Register y when conversion is started by the first trigger, and in the A/D Data Duplexing Register when started by the second trigger. Table 35.4 shows the channel selection settings for double-triggered operation.

A/D-converted value addition/average mode can be set with double trigger mode for the channel selected in the DBLANS[4:0] bits by using the ADADS0 and ADADS1 registers. In double trigger mode, the channels selected in the ADANSA0 and ADANSA1 registers are invalid, and the channel selected in the DBLANS[4:0] bits is A/D-converted instead.

When double trigger mode is used in group scan mode, double-trigger control is only applied to group A and not to group B. This means that multi-channel analog input, temperature sensor output, and internal reference voltage can be selected for group B even in double trigger mode.

Only set the DBLANS[4:0] bits while the ADST bit is 0. Do not set them at the same time that you write 1 to the ADST bit.

To enter A/D-converted value addition/average mode when in double trigger mode, set the channel selected in the DBLANS[4:0] bits in the ADANSA0 and ADANSA1 registers.

Table 35.4 Relationship between DBLANS bit settings and double-trigger enabled channels

Unit 0		Unit 1	
DBLANS[4:0]	Duplication channel	DBLANS[4:0]	Duplication channel
00000	AN000	00000	AN100
00001	AN001	00001	AN101
00010	AN002	00010	AN102
00011	AN003	00011	-
00100	-	00100	-
00101	AN005	00101	AN105
00110	AN006	00110	AN106
00111	AN007	00111	AN107

Unit 0		Unit 1	
DBLANS[4:0]	Duplication channel	DBLANS[4:0]	Duplication channel
10000	AN016	10000	AN116
10001	AN017	10001	AN117
10010	AN018	10010	-
10011	-	10011	-
10100	AN020	10100	-

Note: A/D-converted data from the self-diagnosis function, temperature sensor output, and internal reference voltage cannot be used in double trigger mode.
Settings other than those listed in Table 35.4 are prohibited.

GBADIE bit (Group B Scan End Interrupt and ELC Event Enable)

The GBADIE bit enables or disables group B scan end interrupt (ADC12i_GBADI (i = 0, 1)) in group scan mode.

DBLE bit (Double Trigger Mode Select)

The DBLE bit selects or deselects double trigger mode. Double trigger mode can only be operated by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits.

Double-trigger operation is as follows:

1. The ADC12i_ADI (i = 0, 1) interrupt is not output on completion of the first conversion but on completion of the second conversion.
2. The A/D conversion results from the duplication channel (selected in DBLANS[4:0]) started by the first trigger are stored in A/D Data Register y and those started by the second trigger are stored in the A/D Data Duplexing Register.

When DBLE is set, selecting double trigger mode, the channels specified in the ADANSA0 and ADANSA1 registers are invalid. Double trigger mode is deselected by setting DBLE to 0. Setting DBLE to 1 again enables the same double-trigger operation described in 1. and 2. for first time scanning with the first trigger.

Do not select double trigger mode in continuous scan mode. Additionally, do not select double trigger mode for conversion of the temperature sensor output or internal reference voltage except for group B scan in group scan mode. Software triggering cannot be set in double trigger mode. Always clear the ADST bit to 0 before setting the DBLE bit. In other words, do not set the DBLE bit at that same time as writing 1 to the ADST bit.

EXTRG bit (Trigger Select)

The EXTRG bit selects the synchronous or asynchronous trigger as the trigger for starting A/D conversion.

TRGE bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous and asynchronous triggers. In group scan mode, set this bit to 1.

ADCS[1:0] bits (Scan Mode Select)

The ADCS[1:0] bits select the scan mode.

In single scan mode, A/D conversion is performed for the analog inputs, up to a maximum of 11 channels in unit 0 and 8 channels in unit 1, and selected in the ADANSA0 and ADANSA1 registers in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, the scan conversion stops. When the temperature sensor output or internal reference voltage is selected, A/D conversion of the designated analog input channels is followed by A/D conversion of the temperature sensor output and the internal reference voltage, in that order.

In continuous scan mode, while the ADCSR.ADST bit is 1, A/D conversion is performed for the analog inputs selected in the ADANSA0 and ADANSA1 registers in ascending order of channel number, and when 1 cycle of A/D conversion completes for all the selected channels, A/D conversion is repeated from the first channel. If the ADCSR.ADST bit is set to 0 during continuous scan, A/D conversion stops even if scanning is in progress. When the temperature sensor output or internal reference voltage is selected, A/D conversion of the designated analog input channels is followed by A/D conversion of the temperature sensor output and the internal reference voltage, in that order.

In group scan mode, scanning is started by the synchronous trigger (ELC) selected in the TRSA[5:0] bits in ADSTRGR. A/D conversion is performed on the group A analog inputs, up to the maximum channels selected in the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops. On the same trigger, A/D conversion is also performed on the group B analog inputs, up to the maximum channels selected in the ADANSB0 and ADANSB1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops. If the conversion processes in group A and group B occur at the same time, those conversions cannot be controlled separately. In this case, set the Group A Priority Control Setting bit (ADGSPCR.PGS) in the A/D Group Scan Priority Control Register (ADGSPCR) to 1 to give priority to group A conversion. When the temperature sensor output or internal reference voltage is selected, A/D conversion of the designated analog input channels is followed by A/D conversion of the temperature sensor output and the internal reference voltage, in that order.

In group scan mode, select different channels and triggers for group A and group B. Clear the ADST bit to 0 before setting the ADCS[1:0] bits. In other words, do not set the ADCS[1:0] bits at the same time as writing 1 to the ADST bit.

Table 35.5 Selectable targets for A/D conversion depending on scan and double trigger mode settings

Scan mode setting	Double trigger mode setting	Targets for A/D conversion				
		Self-diagnosis	Analog input (including group A)	Analog input (group B)	Temperature sensor output	Internal reference voltage
Single scan	DBLE = 0	✓	✓	-	✓	✓
	DBLE = 1	-	✓ (1 ch only)	-	-	-
Continuous scan	DBLE = 0	✓	✓	-	✓	✓
	DBLE = 1	-	-	-	-	-
Group scan	DBLE = 0	✓	✓	✓	✓	✓
	DBLE = 1	-	✓ (1 ch only)	✓	✓	✓

✓: Selectable. -: Not selectable.

ADST bit (A/D Conversion Start)

The ADST bit starts or stops the A/D conversion process. Before setting the ADST bit to 1, set the A/D conversion clock, conversion mode, and analog input for the conversion target.

[Setting conditions]

- 1 is written by software
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits is detected when ADCSR.EXTRG is 0 and ADCSR.TRGE is 1
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits is detected when ADCSR.TRGE is set to 1 in group scan mode
- The asynchronous trigger is detected when the ADCSR.TRGE and ADCSR.EXTRG bits are set to 1 and the ADSTRGR.TRSA[5:0] bits are set to 000000b
- When group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1, and A/D conversion of group B starts.

[Clearing conditions]

- 0 is written by software
- The A/D conversion of all the selected channels, the temperature sensor output or the internal reference voltage completes in single scan mode
- Group A scan completes in group scan mode
- Group B scan completes in group scan mode
- When group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1, and a scanning of group B completes.

Note: When group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 1.

Note: When group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 0. When forcing A/D conversion to terminate, follow the procedure for clearing the ADST bit.

Note: If the single scan continuous function is used (ADGSPCR.GBRP = 1) when the group priority operation mode is enabled (ADCSR.ADCS[1:0] = 01b and ADGSPCR.PGS = 1), the ADST bit is retained to 1.

35.2.4 A/D Channel Select Register A0 (ADANSA0)

Address(es): ADC120.ADANSA0 4005 C004h, ADC121.ADANSA0 4005 C204h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ANSA07	ANSA06	ANSA05	—	ANSA03	ANSA02	ANSA01	ANSA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	ANSA03 to ANSA00	A/D Conversion Channels Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7 to b5	ANSA07 to ANSA05	A/D Conversion Channels Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSAn bits (n = 00 to 03, 05 to 07) (A/D Conversion Channels Select)

The ADANSA0.ANSAn bits select or deselect the analog input channels for A/D conversion for AN000 to AN003, AN005 to AN007 (unit 0) and AN100 to AN102, AN105 to AN107 (unit 1). The channels and the number of channels can be set arbitrarily. In unit 0, the ANSA00 bit is associated with AN000 and the ANSA07 bit with AN007. In unit 1, the ANSA00 bit is associated with AN100 and the ANSA07 bit with AN107.

In double trigger mode, the channel selected in the ADANSA0 register is invalid, and the channel selected in the ADCSR.DBLANS[4:0] bits is selected in group A instead.

In group scan mode, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1). Only set the ADANSA0 register while the ADCSR.ADST bit is 0.

35.2.5 A/D Channel Select Register A1 (ADANSA1)

Address(es): ADC120.ADANSA1 4005 C006h, ADC121.ADANSA1 4005 C206h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ANSA20	—	ANSA18	ANSA17	ANSA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	ANSA18 to ANSA16	A/D Conversion Channels Select	0: Do not select associated input channel 1: Select associated input channel	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ANSA20	A/D Conversion Channel Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSAn bits (n = 16 to 18, 20) (A/D Conversion Channels Select)

The ADANSA1.ANSAn bits select or deselect the analog input channels for A/D conversion for AN016 to AN018, AN020 (unit 0) and AN116, AN117 (unit 1). The channels and the number of channels can be set arbitrarily. In unit 0, the ANSA16 bit is associated with AN016 and the ANSA20 bit with AN020. In unit 1, the ANSA16 bit is associated with AN116 and the ANSA17 bit with AN117.

In double trigger mode, the ANSA1[15:0] bits are invalid, and the channel selected in the ADCSR.DBLANS[15:0] bits is selected in group A instead.

In group scan mode, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1). Only set the ADANSA1 register while the ADCSR.ADST bit is 0.

35.2.6 A/D Channel Select Register B0 (ADANSB0)

Address(es): ADC120.ADANSB0 4005 C014h, ADC121.ADANSB0 4005 C214h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ANSB07	ANSB06	ANSB05	—	ANSB03	ANSB02	ANSB01	ANSB00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	ANSB03 to ANSB00	A/D Conversion Channels Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7 to b5	ANSB07 to ANSB05	A/D Conversion Channels Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSBn bits (n = 00 to 03, 05 to 07) (A/D Conversion Channels Select)

The ADANSB0.ANSBn bits select the analog input channels for A/D conversion for AN000 to AN003, AN005 to AN007 (unit 0) and AN100 to AN102, AN105 to AN107 (unit 1) in group B in group scan mode. The ADANSB0 register is only used for group scan mode, not for any other modes. Exclude the channels specified in group A (the channels associated with group A, selected in the ADANSA0 and ADANSA1 registers and the ADCSR.DBLANS[4:0] bits in double trigger mode), both the selected channels and the number of channels to be set.

In unit 0, the ANSB00 bit is associated with AN000 and the ANSB07 bit with AN007. In unit 1, the ANSB00 bit is associated with AN100 and the ANSB07 bit with AN107. Only set the ADANSB0 register while the ADCSR.ADST bit is 0.

35.2.7 A/D Channel Select Register B1 (ADANSB1)

Address(es): ADC120.ADANSB1 4005 C016h, ADC121.ADANSB1 4005 C216h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ANSB20	—	ANSB18	ANSB17	ANSB16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	ANSB18 to ANSB16	A/D Conversion Channels Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ANSB20	A/D Conversion Channel Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSBn bits (n = 16 to 18, 20) (A/D Conversion Channels Select)

The ADANSB1.ANSBn bits select the analog input channels for A/D conversion for AN016 to AN018, AN020 (unit 0) and AN116, AN117 (unit 1) in group B in group scan mode. The ADANSB1 register is only used for group scan mode, not for any other modes. Exclude the channels specified in group A (the channels associated with group A, selected in the ADANSA0 and ADANSA1 registers and the ADCSR.DBLANS[4:0] bits in double trigger mode), both the selected channels and the number of channels to be set.

In unit 0, the ANSB16 bit is associated with AN016 and the ANSB20 bit with AN020. In unit 1, the ANSB16 bit is associated with AN116 and the ANSB17 bit with AN117. Only set the ADANSB1 register bits while the ADST bit is 0.

35.2.8 A/D-Converted Value Addition/Average Channel Select Register 0 (ADADS0)

Address(es): ADC120.ADADS0 4005 C008h, ADC121.ADADS0 4005 C208h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ADS07	ADS06	ADS05	—	ADS03	ADS02	ADS01	ADS00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	ADS03 to ADS00	A/D-Converted Value Addition/Average Channel Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7 to b5	ADS07 to ADS05	A/D-Converted Value Addition/Average Channel Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSn bits (n = 00 to 03, 05 to 07) (A/D-Converted Value Addition/Average Channel Select)

When the ADSn bit with the same number as the A/D-converted channel selected in the ANSAn bits (n = 00 to 03, 05 to 07) in ADANSA0, or the ADCSR.DBLANS[4:0] bits and the ANSBn bits (n = 00 to 03, 05 to 07) in ADANSB0 is set to 1, A/D conversion of the analog input of the selected channels is performed successively 1 to 16 times, as specified in the ADC[2:0] bits in ADADC. When the ADADC.AVEE bit is 0, the value obtained by addition is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register. For A/D-converted channels for which addition or average mode is not selected, a normal one-time conversion is executed, and the conversion result is stored in the A/D data register.

In unit 0, the ADS00 bit is associated with AN000 and the ADS07 bit with AN007. In unit 1, the ADS00 bit is associated with AN100 and the ADS07 bit with AN107.

Only set the ADADS0 register bits while the ADCSR.ADST bit is 0.

35.2.9 A/D-Converted Value Addition/Average Channel Select Register 1 (ADADS1)

Address(es): ADC120.ADADS1 4005 C00Ah, ADC121.ADADS1 4005 C20Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ADS20	—	ADS18	ADS17	ADS16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	ADS18 to ADS16	A/D-Converted Value Addition/Average Channel Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ADS20	A/D-Converted Value Addition/Average Channel Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSn bits (n = 16 to 18, 20) (A/D-Converted Value Addition/Average Channel Select)

When the ADSn bit with the same number as the A/D-converted channel selected in the ANSAn bits (n = 16 to 18, 20) in ADANSA1 or the ADCSR.DBLANS[4:0] and ANSBn bits (n = 16 to 18, 20) in ADANSB1 is set to 1, A/D conversion

of the analog input of the selected channels is performed successively 1 to 16 times, as specified in the ADC[2:0] bits in ADADC. When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register. For A/D-converted channels for which addition/average mode is not selected, a normal one-time conversion is executed and the conversion result is stored in the A/D data register.

In unit 0, the ADS16 bit is associated with AN016 and the ADS20 bit with AN020. In unit 1, the ADS16 bit is associated with AN116 and the ADS17 bit with AN117. Only set the ADADS1 register while the ADCSR.ADST bit is 0.

Figure 35.3 shows a scanning operation sequence in which both the ADADS0.ADS02 and ADS07 bits are set to 1.

In this example, addition mode is selected (ADADS.AVEE = 0), the time conversion is set to 4 (ADADC.ADC[1:0] = 11b), and the AN000 to AN003 and AN005 to AN007 channels are selected (ADANSA0.ANSA0[15:0] = 00EFh) in continuous scan mode (ADCSR.ADCS[1:0] = 10b). The conversion process begins with AN000. The AN002 conversion is performed successively 4 times, and the added (integrated) value is returned to A/D data register ADDR2. Next, the AN003 conversion process starts. The AN007 conversion is performed successively 4 times and the added (integrated) value is returned to A/D data register, ADDR7. After conversion of AN007, the conversion operation is once again performed in the same sequence from AN000.

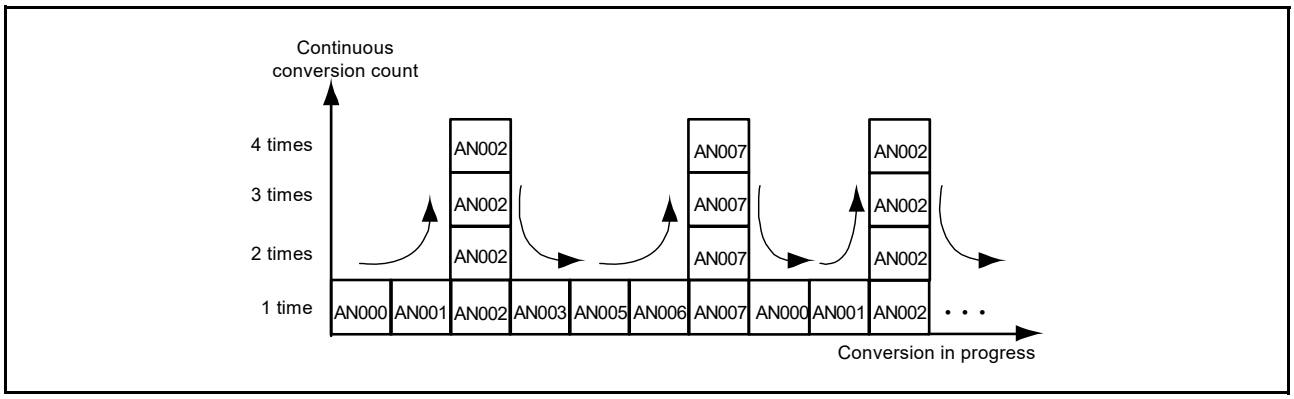


Figure 35.3 Scan conversion sequence with ADADC.ADC[2:0] = 011b, ADADS0.ADS02 = 1, and ADS07 = 1

35.2.10 A/D-Converted Value Addition/Average Count Select Register (ADADC)

Address(es): ADC120.ADADC 4005 C00Ch, ADC121.ADADC 4005 C20Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	AVEE	—	—	—	—	ADC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	ADC[2:0]	Count Select	b2 b0 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2 time conversion (one addition) 0 1 0: 3-time conversion (two additions) 0 1 1: 4 time conversion (three additions) 1 0 1: 16-time conversion (15 additions). Other settings are prohibited.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	AVEE	Average Mode Enable	0: Disable average mode*1 1: Enable average mode.*2	R/W

Note 1. When average mode is deselected by setting the ADADC.AVEE bit to 0, set addition count to 1, 2, 3, 4 or 16-time conversion. 16-time conversion can only be used with 12-bit accuracy selected.

Note 2. When average mode is selected by setting the ADADC.AVEE bit to 1, set the addition count to 1-, 2-, or 4-time conversion. Do not set the addition count to 3- or 16-time conversion (ADC[2:0] = 010b or 101b).

ADC[2:0] bits (Count Select)

The ADC[2:0] bits set the count for all channels for which A/D conversion and addition/average mode are selected, including the channels selected in double trigger mode in the ADCSR.DBLANS[4:0] bits. The count also applies to A/D conversion of temperature sensor output and internal reference voltage.

When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the count to 3-time conversion (ADADC.ADC[2:0] = 010b). Additionally, the combination of 16-time conversion (ADADC.ADC[2:0] = 101b) with a conversion accuracy setting of 8 or 10 bits (ADCER.ADPRC[1:0] = 10b or 01b) is a prohibited setting, as described in section 35.2.1.

Only set the ADC[2:0] bits while the ADCSR.ADST bit is 0. When self-diagnosis is executed (ADCER.DIAGM = 1), do not set the ADC[2:0] bits to any value other than 000b. When the conversion accuracy is 8 or 10 bits (ADCER.ADPRC[1:0] = 10b or 01b), do not set the ADC[2:0] bits to 101b.

AVEE bit (Average Mode Enable)

The AVEE bit selects addition or average mode for all channels for which A/D conversion and addition/average mode are selected, including the channels selected in double trigger mode in the ADCSR.DBLANS[4:0] bits, temperature sensor output, and internal reference voltage.

When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the addition count to 3-time conversion (ADADC.ADC[2:0] = 010b).

Only set the AVEE bits while the ADCSR.ADST bit is 0.

35.2.11 A/D Control Extended Register (ADCER)

Address(es): ADC120.ADCER 4005 C00Eh, ADC121.ADCER 4005 C20Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2, b1	ADPRC[1:0]	A/D Conversion Accuracy Specify	b2 b1 0 0: 12-bit accuracy 0 1: 10-bit accuracy 1 0: 8-bit accuracy 1 1: Setting prohibited.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	ACE	A/D Data Register Automatic Clearing Enable	0: Disable automatic clearing 1: Enable automatic clearing.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	DIAGVAL[1:0]	Self-Diagnosis Conversion Voltage Select	b9 b8 0 0: Setting prohibited when self-diagnosis is enabled 0 1: 0 V 1 0: Reference power supply voltage*1 x 1/2 1 1: Reference power supply voltage.*1	R/W
b10	DIAGLD	Self-Diagnosis Mode Select	0: Select rotation mode for self-diagnosis voltage 1: Select mixed mode for self-diagnosis voltage.	R/W
b11	DIAGM	Self-Diagnosis Enable	0: Disable ADC12 self-diagnosis 1: Enable ADC12 self-diagnosis.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	ADRFMT	A/D Data Register Format Select	0: Select flush-right for the A/D data register format 1: Select flush-left for the A/D data register format.	R/W

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

ADPRC[1:0] bits (A/D Conversion Accuracy Specify)

The ADPRC[1:0] bits set the A/D conversion accuracy to 8-, 10-, or 12-bit accuracy. Changing the A/D conversion accuracy also changes the bit width of valid data stored in the result register and the A/D conversion time. For details, see section 35.3.6, Analog Input Sampling and Scan Conversion Time.

Only set the ADPRC[1:0] bits while the ADCSR.ADST bit is 0.

ACE bit (A/D Data Register Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (all 0s) of ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, or ADOCDR after any of these registers is read by the CPU, DTC, or DMAC. Automatic clearing of the A/D data registers enables detection of failures that do not update the A/D data registers.

DIAGVAL[1:0] bits (Self-Diagnosis Conversion Voltage Select)

The DIAGVAL[1:0] bits select the voltage value used in self-diagnosis fixed voltage mode. For details, see the ADCER.DIAGLD bit description.

Do not execute self-diagnosis by setting the ADCER.DIAGLD bit to 1 when the ADCER.DIAGVAL[1:0] bits are set to 00b.

DIAGLD bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated, or fixed voltage is used in self-diagnosis. Setting this bit to 0 allows conversion of the voltages in rotation mode where 0 V, the reference power supply × 1/2, and the reference power supply are converted, in that order. After reset, when the self-diagnosis voltage rotation mode is selected, self-diagnosis is executed from 0 V. The fixed voltage specified in the ADCER.DIAGVAL[1:0] bits is converted when self-diagnosis fixed voltage mode is selected. In self-diagnosis voltage rotation mode, the self-diagnosis voltage value does not return to 0 when scan conversion completes. When scan conversion restarts, rotation starts at the voltage value following the previous value. If fixed mode is switched to rotation mode, rotation starts at the fixed voltage value.

Only set the DIAGLD bit while the ADCSR.ADST bit is 0.

DIAGM bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis. Self-diagnosis is used to detect a failure of the ADC12. In self-diagnosis mode, one of the internally generated voltage values (0, the reference power supply × 1/2, or the reference power supply) is converted. When conversion completes, information on the converted voltage and the conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). ADRD can be read by software to determine whether the conversion result falls within the normal range (normal) or not (abnormal). Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. When the double trigger mode is set (ADCSR.DBLE = 1), always deselect self-diagnosis (DIAGM = 0). When self-diagnosis is selected in group scan mode, self-diagnosis is executed separately on group A and group B.

Only set the DIAGM bit while the ADCSR.ADST bit is 0.

ADRFMT bit (A/D Data Register Format Select)

The ADRFMT bit specifies flush-right or flush-left for the data to be stored in ADDRy, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR, ADCMPDR0/1, ADWINLLB, ADWINULB, or ADRD.

Only set the ADRFMT bit when the ADCSR.ADST bit is 0.

35.2.12 A/D Conversion Start Trigger Select Register (ADSTRGR)

Address(es): ADC120.ADSTRGR 4005 C010h, ADC121.ADSTRGR 4005 C210h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	TRSB[5:0]	A/D Conversion Start Trigger Select for Group B	These bits specify the A/D conversion start trigger for group B in group scan mode	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	TRSA[5:0]	A/D Conversion Start Trigger Select	These bits specify the A/D conversion start trigger in single scan mode and continuous mode. In group scan mode, the A/D conversion start trigger for group A is selected.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TRSB[5:0] bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[5:0] bits select the trigger to start scanning of the analog input selected in group B. The TRSB[5:0] bits must only be set in group scan mode and are not used in any other scan mode. For the scan conversion start trigger for group B, setting a software trigger or an asynchronous trigger is prohibited. In group scan mode, set the TRSB[5:0] bits to a value other than 000000b, and set the ADCSR.TRGE bit to 1.

When group A is given priority in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows group B to continuously operate in single scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[5:0] bits to 3Fh. The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (t_{SCAN}). If the issuance period is less than t_{SCAN}, A/D conversion by the trigger might have no effect.

When the trigger from a module operated at 120 MHz (GPT) is selected as an A/D conversion start trigger, a delay for synchronization processing occurs. For details, see section 35.3.6, Analog Input Sampling and Scan Conversion Time.

Table 35.6 lists the A/D conversion startup sources selected in the TRSB[5:0] bits.

TRSA[5:0] bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion in single scan mode and continuous scan mode. In group scan mode, the trigger to start scanning of the analog input selected in group A is selected. When scanning is executed in group scan mode or double trigger mode, setting a software trigger or an asynchronous trigger is prohibited.

When using a synchronous trigger (ELC) as the A/D conversion start source, set the TRGE bit in ADCSR to 1 and the EXTRG bit in ADCSR to 0.

When using the asynchronous trigger (ADTRGn), set the TRGE bit in ADCSR to 1 and the EXTRG bit in ADCSR to 1.

The software trigger (ADCSR.ADST) is enabled regardless of the settings in the ADCSR.TRGE bit, the ADCSR.EXTRG bit, or the TRSA[5:0] bits. The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (t_{SCAN}). If the issuance period is less than t_{SCAN}, A/D conversion by the trigger might have no effect.

When the trigger from a module operated at 120 MHz (GPT) is selected as an A/D conversion start trigger, a delay period for synchronization processing occurs. For details, see section 35.3.6, Analog Input Sampling and Scan Conversion Time.

Table 35.7 lists the A/D conversion start sources selected in the TRSA[5:0] bits.

Table 35.6 Selection of A/D conversion start sources in the TRSB[5:0] bits

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
Trigger source deselected state		1	1	1	1	1	1
ELC_ADC00 (unit 0), ELC_ADC10 (unit 1)	ELC	0	0	1	0	0	1
ELC_ADC01 (unit 0), ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	0
ELC_ADC00/ELC_ADC01 (unit 0) ELC_ADC10/ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	1

Table 35.7 Selection of A/D activation sources in the TRSA[5:0] bits

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
Trigger source deselected state		1	1	1	1	1	1
ADTRGn	Input pin for the trigger	0	0	0	0	0	0
ELC_ADC00 (unit 0), ELC_ADC10 (unit 1)	ELC	0	0	1	0	0	1
ELC_ADC01 (unit 0), ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	0
ELC_ADC00/ELC_ADC01 (unit 0) ELC_ADC10/ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	1

35.2.13 A/D Conversion Extended Input Control Register (ADEXICR)

Address(es): ADC120.ADEXICR 4005 C012h, ADC121.ADEXICR 4005 C212h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	OCSB	TSSB	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSSAD	Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select	0: Do not select addition/average mode for temperature sensor output 1: Select addition/average mode for temperature sensor output.	R/W
b1	OCSAD	Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select	0: Do not select addition/average mode for internal reference voltage 1: Select addition/average mode for internal reference voltage.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TSSA	Temperature Sensor Output A/D Conversion Select	0: Disable A/D conversion of temperature sensor output 1: Enable A/D conversion of temperature sensor output.	R/W
b9	OCSA	Internal Reference Voltage A/D Conversion Select	0: Disable A/D conversion of internal reference voltage 1: Enable A/D conversion of internal reference voltage.	R/W
b10	TSSB	Temperature Sensor Output A/D Conversion Select for group B	Selection for group B in group scan mode: 0: Disable A/D conversion of temperature sensor output 1: Enable A/D conversion of temperature sensor output.	R/W

Bit	Symbol	Bit name	Description	R/W
b11	OCSB	Internal Reference Voltage A/D Conversion Select for group B	Selection for group B in group scan mode: 0: Disable A/D conversion of internal reference voltage 1: Enable A/D conversion of internal reference voltage.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TSSAD bit (Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select)

When the TSSAD bit is set to 1, A/D conversion of the temperature sensor output is selected and performed successively for the number of times specified in the ADC[2:0] bits in ADADC. The maximum addition count depends on the conversion accuracy, see section 35.2.1. When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D Temperature sensor Data Register (ADTSDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADTSDR.

Only set the TSSAD bit while the ADCSR.ADST bit is 0.

OCSAD bit (Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select)

When the OCSAD bit is set to 1, A/D conversion of the internal reference voltage is selected and performed successively the number of times specified in the ADC[2:0] bits in ADADC. The maximum addition count differs depending on the conversion accuracy as described in section 35.2.1. When the ADADC.AVEE bit is 0, the value obtained by addition is returned to the A/D Internal Reference Voltage Data Register (ADOCDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADOCDR.

Only set the OCSAD bit while the ADCSR.ADST bit is 0.

TSSA bit (Temperature Sensor Output A/D Conversion Select)

The TSSA bit selects A/D conversion of the temperature sensor output for group A in single scan mode, continuous scan mode, or group scan mode. When A/D conversion of the temperature sensor output is selected and performed, set the ADCSR.DBLE bit to 0.

Only set the TSSA bit when the ADCSR.ADST bit is 0.

OCSA bit (Internal Reference Voltage A/D Conversion Select)

The OCSA bit selects A/D conversion of the internal reference voltage for group A in single scan mode, continuous scan mode, or group scan mode. When A/D conversion of the internal reference voltage is selected and performed, set the ADCSR.DBLE bit to 0.

Only set the OCSA bit while the ADCSR.ADST bit is 0. In addition, wait for 400 ns or more after the OCSA bit is set to 1 before starting A/D conversion.

TSSB bit (Temperature Sensor Output A/D Conversion Select for group B)

The TSSB bit selects A/D conversion of the temperature sensor output for group B in group scan mode.

Only set the TSSB bit while the ADCSR.ADST bit is 0. Do not set the TSSB bit to 1 while the TSSA bit is 1.

OCSB bit (Internal Reference Voltage A/D Conversion Select for group B)

The OCSB bit selects A/D conversion of the internal reference voltage for group B in group scan mode.

Only set the OCSB bit while the ADCSR.ADST bit is 0. Do not set the OCSB bit to 1 while the OCSA bit is 1. In addition, start the A/D conversion after waiting for 400 ns or more after the OCSB bit is set to 1.

35.2.14 A/D Sampling State Register n (ADSSTRn) (n = 00 to 03, 05 to 07, L, T, O)

Address(es): ADC120.ADSSTR00 4005 C0E0h to ADC120.ADSSTR03 4005 C0E3h, ADC120.ADSSTR05 4005 C0E5h to ADC120.ADSSTR07 4005 C0E7h, ADC120.ADSSTRL 4005 C0DDh, ADC120.ADSSTRT 4005 C0DEh, ADC120.ADSSTRO 4005 C0DFh, ADC121.ADSSTR00 4005 C2E0h to ADC121.ADSSTR02 4005 C2E2h, ADC121.ADSSTR05 4005 C2E5h to ADC121.ADSSTR07 4005 C2E7h, ADC121.ADSSTRL 4005 C2DDh, ADC121.ADSSTRT 4005 C2DEh, ADC121.ADSSTRO 4005 C2DFh

	b7	b6	b5	b4	b3	b2	b1	b0
	SST[7:0]							
Value after reset:	0	0	0	0	1	0	1	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	SST[7:0]	Sampling Time Setting	These bits set the sampling time in the range from 5 to 255 states	R/W

The ADSSTRn register sets the sampling time for analog input. If one state is 1 ADCLK (A/D conversion clock) cycle and the ADCLK clock is 60 MHz, one state is 16.7 ns. The initial value is 11 states.

The sampling time can be adjusted if the impedance of the analog input signal source is too high to secure sufficient sampling time, or if the ADCLK clock is slow.

Only set the SST[7:0] bits while the ADCSR.ADST bit is 0.

The lower limit of the sampling time setting depends on the frequency ratio, as follows:

- If the frequency ratio of PCLKB to PCLKC(ADCLK) = 1:1, 2:1, 4:1, or 8:1, the sampling time must be set to a value of more than 5 states
- If the frequency ratio of PCLKB to PCLKC(ADCLK) = 1:2 or 1:4, the sampling time must be set to a value of more than 6 states.

Table 35.8 shows the relationship between the A/D Sampling State Register and the associated channels. For details, see section 35.3.6, Analog Input Sampling and Scan Conversion Time.

Table 35.8 Relationship between A/D Sampling State Register and associated channels

	Associated channels	
Bit name	Unit 0	Unit 1
ADSSTR00.SST[7:0] bits*1	AN000	AN100
ADSSTR01.SST[7:0] bits	AN001	AN101
ADSSTR02.SST[7:0] bits	AN002	AN102
ADSSTR03.SST[7:0] bits	AN003	-
ADSSTR05.SST[7:0] bits	AN005	AN105
ADSSTR06.SST[7:0] bits	AN006	AN106
ADSSTR07.SST[7:0] bits	AN007	AN107
ADSSTRL.SST[7:0] bits	AN016 to AN018 and AN020	AN116 and AN117
ADSSTRT.SST[7:0] bits	Temperature sensor output	Temperature sensor output
ADSSTRO.SST[7:0] bits	Internal reference voltage	Internal reference voltage

Note 1. When the self-diagnosis function is selected, the sampling time set in the ADSSTR00.SST[7:0] bits is applied.

35.2.15 A/D Sample and Hold Circuit Control Register (ADSHCR)

Address(es): ADC120.ADSHCR 4005 C066h, ADC121.ADSHCR 4005 C266h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SHANS[2:0]			SSTSH[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	SSTSH[7:0]	Channel-Dedicated Sample-and-Hold Circuit Sampling Time Setting	Sampling time (4 to 255 states)	R/W
b10 to b8	SHANS[2:0]	Channel-Dedicated Sample-and-Hold Circuit Bypass Select	Select whether to use or bypass channel-dedicated sample-and-hold circuits for AN000 to AN002 (unit 0) and AN100 to AN102 (unit 1). 0: Bypass the circuits 1: Use the circuits.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SSTSH[7:0] bits (Channel-Dedicated Sample-and-Hold Circuit Sampling Time Setting)

The SSTSH[7:0] bits set the sampling time for the channel-dedicated sample-and-hold circuits. If one state is 1 ADCLK (A/D conversion clock) cycle and the ADCLK clock is 60 MHz, one state is 16.7 ns. The initial value is 24 states. The sampling time can be adjusted if the impedance of the analog input signal source is too high to secure sufficient sampling time, or if the ADCLK clock is slow.

Only set the SSTSH[7:0] bits while the ADCSR.ADST bit is 0. The sampling time must be set to a value that is 4 states or more and 255 or less.

SHANS[2:0] bits (Channel-Dedicated Sample-and-Hold Circuit Bypass Select)

The SHANS[2:0] bits select whether to use or bypass the channel-dedicated sample-and-hold circuits for AN000 to AN002 (unit 0) and AN100 to AN102 (unit 1). In unit 0, the SHANS[0] bit is associated with AN000, the SHANS[1] bit with AN001, and the SHANS[2] bit with AN002. In unit 1, the SHANS[0] bit is associated with AN100, the SHANS[1] bit with AN101, and the SHANS[2] bit with AN102.

If any channel from AN000 to AN002 (unit 0) or AN100 to AD102 (unit 1) is selected for group B while operation is in group scan mode under group A priority control, use this setting to bypass the dedicated sample-and-hold circuit of the channel.

Only set the SHANS[2:0] bits while the ADCSR.ADST bit is 0 and the ADSHMSR.SHMD bit is 0.

35.2.16 A/D Sample and Hold Operation Mode Selection Register (ADSHMSR)

Address(es): ADC120.ADSHMSR 4005 C07Ch, ADC121.ADSHMSR 4005 C27Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SHMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SHMD	Sampling Operation Selection	0: Disable continuous sampling function 1: Enable continuous sampling function.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SHMD bit (Sampling Operation Selection)

Setting SHMD to 1 enables the constant sampling function of the channel-dedicated sample-and-hold selected in the ADSHCR.SHANS[2:0] bits. Only set the SHMD bit while the ADCSR.ADST bit is 0.

When the sampling function is enabled, the sample-and-hold circuit operates sampling while the ADC12 is not operating, and operates holding while the ADC12 is operating.

Note: The ADCSR.ADST bit must become 1 after 400 ns or more elapses after the SHMD bit is set to 1 (when the permissible signal source impedance is 1 kΩ). The sampling period of the sample-and-hold circuit must be 400 ns or more (when the permissible signal source impedance is 1 kΩ).

35.2.17 A/D Disconnection Detection Control Register (ADDISCR)

Address(es): ADC120.ADDISCR 4005 C07Ah, ADC121.ADDISCR 4005 C27Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PCHG	ADNDIS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	ADNDIS[3:0]	Disconnection Detection Assist Setting	b3 b0 0 0 0 0: Disconnection detection assist function is disabled 0 0 0 1: Setting prohibited Others : Number of states for the discharge or precharge period.	R/W
b4	PCHG	Precharge/discharge select	0: Discharge 1: Precharge.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ADDISCR register selects either precharge or discharge, and the period of precharge or discharge for the A/D disconnection detection assist function.

Only set the ADDISCR register when the ADCSR.ADST bit is 0.

If any of the following functions are used, the disconnection detection assist function should be disabled:

- Temperature sensor
- Internal reference voltage
- A/D self-diagnosis
- Programmable gain amplifier without bypass enabled.

ADNDIS[3:0] bits (Disconnection Detection Assist Setting)

The ADNDIS[3:0] bits specify the period of precharge or discharge. When ADNDIS[3:0] = 0000b, the disconnection detection assist function is disabled. Setting the ADNDIS[3:0] bits to 0001b is prohibited. Except when ADNDIS[3:0] = 0000b or 0001b, the specified value indicates the number of states for the period of precharge or discharge. When the ADNDIS[3:0] bits are set to any values other than 0000b or 0001b, the disconnection detection assistance function is enabled.

PCHG bit (Precharge/discharge select)

Setting the PCHG bit to 1 selects precharge and setting the PCHG bit to 0 selects discharge.

35.2.18 A/D Group Scan Priority Control Register (ADGSPCR)

Address(es): ADC120.ADGSPCR 4005 C080h, ADC121.ADGSPCR 4005 C280h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PGS	Group A Priority Control Setting*1	0: Operate without group A priority control 1: Operate with group A priority control.	R/W
b1	GBRSCN	Group B Restart Setting	This bit is enabled only when PGS = 1. It is reserved when PGS = 0. 0: Do not restart group B scanning after it is stopped by group A priority control 1: Restart group B scanning after it is stopped by group A priority control.	R/W
b14 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	GBRP	Group B Single Scan Continuous Start*2	This bit is enabled only when PGS = 1. It is reserved when PGS = 0. 0: Do not continuously activate single scan for group B 1: Continuously activate single scan for group B.	R/W

Note 1. The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting PGS to 1. Operation is not guaranteed if these bits are set to any other value.

Note 2. When the GBRP bit is set to 1, single scan is performed continuously for group B regardless of the setting in the GBRSCN bit.

PGS bit (Group A Priority Control Setting)

Set the PGS bit to 1 to give priority to operation on group A. The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting the PGS bit to 1. Operation is not guaranteed if the bits are set to any other value.

When the PGS bit is set to 0, a clear operation must be performed by software as described in section 35.6.2, Constraints on Stopping A/D Conversion. When the PGS bit is set to 1, use the settings described in section 35.3.4.3, Operation with group A priority control.

GBRSCN bit (Group B Restart Setting)

The GBRSCN bit controls the restarting of scan operation on group B when operation on group A is given priority. If a scan operation on group B is stopped by a group A trigger input with the GBRSCN bit set to 1, the scan operation is restarted on completion of group A conversion. Also, if a group B trigger is input during A/D conversion on group A, the scan operation on group B is restarted on completion of group A conversion.

When the GBRSCN bit is set to 0, trigger inputs during A/D conversion are ignored. Only set the GBRSCN bit while the ADCSR.ADST bit is 0.

The setting in the GBRSCN bit is valid when the PGS bit is 1.

GBRP bit (Group B Single Scan Continuous Start)

The GBRP bit performs a single scan operation continuously on group B. Setting the GBRP bit to 1 starts a single scan on group B. On completion of the scan, another single scan on group B starts automatically. If a group B conversion stops because of an operation on group A, the group A operation takes priority, and single scan on group B restarts automatically on completion of the group A conversion.

Disable group B trigger input before setting the GBRP bit to 1. Setting the GBRP bit to 1 invalidates the setting in the GBRSCN bit. Only set the GBRP bit while the ADCSR.ADST is 0.

The setting in the GBRP bit is valid when the PGS bit is 1.

35.2.19 A/D Compare Function Control Register (ADCMPCR)

Address(es): ADC120.ADCMPCR 4005 C090h, ADC121.ADCMPCR 4005 C290h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CMPAB[1:0]	Window A/B Composite Conditions Setting	b1 b0 0 0: Output ADC12i_WCMPM when window A OR window B comparison conditions are met. Otherwise, output ADC12i_WCMPUM 0 1: Output ADC12i_WCMPM when window A EXOR window B comparison conditions are met. Otherwise, output ADC12i_WCMPUM 1 0: Output ADC12i_WCMPM when window A AND window B comparison conditions are met. Otherwise, output ADC12i_WCMPUM 1 1: Setting prohibited. These bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1).	R/W
b8 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	CMPBE	Compare Window B Operation Enable	0: Disable compare window B operation. Disable ADC12i_WCMPM and ADC12i_WCMPUM outputs. 1: Enable compare window B operation.	R/W
b10	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11	CMPAE	Compare Window A Operation Enable	0: Disable compare window A operation. Disable ADC12i_WCMPM and ADC12i_WCMPUM outputs. 1: Enable compare window A operation.	R/W
b12	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13	CMPBIE	Compare B Interrupt Enable	0: Disable ADC12i_CMPBI interrupt when comparison conditions (window B) are met 1: Enable ADC12i_CMPBI interrupt when comparison conditions (window B) are met.	R/W
b14	WCMPE	Window Function Setting	0: Disable window function. Window A and window B operate as a comparator to compare the single value on the lower side with the A/D conversion result. 1: Enable window function. Window A and window B operate as a comparator to compare the two values on the upper and lower sides with the A/D conversion result.	R/W
b15	CMPAIE	Compare A Interrupt Enable	0: Disable ADC12i_CMPAI interrupt when comparison conditions (window A) are met 1: Enable ADC12i_CMPAI interrupt when comparison conditions (window A) are met.	R/W

Note: i = 0: unit 0, i = 1: unit 1.

CMPAB[1:0] bits (Window A/B Composite Conditions Setting)

The CMPAB[1:0] bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1) in single scan mode. These bits specify the compare function match/mismatch event output conditions and monitoring conditions of ADWINMON.MONCONB.

Only set the CMPAB[1:0] bits when the ADCSR.ADST bit is 0.

CMPBE bit (Compare Window B Operation Enable)

The CMPBE bit enables or disables the compare window B operation. Set the CMPBE bit when the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D Channel Select Registers A0, A1, B0, and B1 (ADANSA0, ADANSA1, ADANSB0, and ADANSB1)
- OCSB, TSSB, OCSA, or TSSA bits in the A/D Conversion Extended Input Control Register (ADEXICR)
- CMPCHB[5:0] bits in the Window B Channel Select Register (ADCMPBNSR).

CMPAE bit (Compare Window A Operation Enable)

The CMPAE bit enables or disables the compare window A operation. Set the CMPAE bit when the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D Channel Select Registers A0, A1, B0, and B1 (ADANSA0, ADANSA1, ADANSB0, and ADANSB1)
- OCSB, TSSB, OCSA, or TSSA bits in the A/D Conversion Extended Input Control Register (ADEXICR)
- Window A Channel Select Registers 0 and 1 (ADCMPANSR0 and ADCMPANSR1)
- Window A Extended Input Select Register (ADCMPANSER).

CMPBIE bit (Compare B Interrupt Enable)

The CMPBIE bit enables or disables the ADC12i_CMPBI (i = 0, 1) interrupt output when the comparison conditions (window B) are met.

WCMPE bit (Window Function Setting)

The WCMPE bit enables or disables the window function. Set the WCMPE bit when the ADCSR.ADST bit is 0.

CMPAIE bit (Compare A Interrupt Enable)

The CMPAIE bit enables or disables the ADC12i_CMPAI (i = 0, 1) interrupt output when the comparison conditions (window A) are met.

35.2.20 A/D Compare Function Window A Channel Select Register 0 (ADCMPANSR0)

Address(es): ADC120.ADCMPANSR0 4005 C094h, ADC121.ADCMPANSR0 4005 C294h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMPCHA07	CMPCHA06	CMPCHA05	—	CMPCHA03	CMPCHA02	CMPCHA01	CMPCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CMPCHA03 to CMPCHA00	Compare Window A Channel Select	0: Disable compare function for associated input channel 1: Enable compare function for associated input channel. In unit 0, bit 3 (CMPCHA03) is associated with to AN003 and bit 0 (CMPCHA00) with AN000. In unit 1, bit 2 (CMPCHA02) is associated with AN102 and bit 0 (CMPCHA00) with AN100.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7 to b5	CMPCHA07 to CMPCHA05	Compare Window A Channel Select	0: Disable compare function for associated input channel 1: Enable compare function for associated input channel. In unit 0, bit 7 (CMPCHA07) is associated with to AN007 and bit 5 (CMPCHA05) with AN005. In unit 1, bit 7 (CMPCHA07) is associated with AN107 and bit 5 (CMPCHA05) with AN105.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPCHAn bits (n = 00 to 03, 05 to 07) (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel

selected in the ADANSA0.ANSAn bits (n = 00 to 03, 05 to 07) and the ADANSB0.ANSBn bits (n = 00 to 03, 05 to 07).

Set the CMPCHAn bits while the ADCSR.ADST bit is 0.

35.2.21 A/D Compare Function Window A Channel Select Register 1 (ADCMPANSR1)

Address(es): ADC120.ADCMPANSR1 4005 C096h, ADC121.ADCMPANSR1 4005 C296h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPCHA20	—	CMPCHA18	CMPCHA17	CMPCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CMPCHA18 to CMPCHA16	Compare Window A Channel Select	0: Disable compare function for associated input channel 1: Enable compare function for associated input channel. In unit 0, bit 2 (CMPCHA18) is associated with AN018, and bit 0 (CMPCHA16) with AN016. In unit 1, bit 1 (CMPCHA17) is associated with AN117 and bit 0 (CMPCHA16) with AN116.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	CMPCHA20	Compare Window A Channel Select	0: Disable compare function for associated input channel 1: Enable compare function for associated input channel. In unit 0, bit 4 (CMPCHA20) is associated with AN020. In unit 1, bit 4 (CMPCHA20) is not associated.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPCHAn bits (n = 16 to 18, 20) (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel selected in the ADANSA1.ANSAn bits (n = 16 to 18, 20) and the ADANSB1.ANSBn bits (n = 16 to 18, 20).

Set the CMPCHAn bits while the ADCSR.ADST bit is 0.

35.2.22 A/D Compare Function Window A Extended Input Select Register (ADCMPANSER)

Address(es): ADC120.ADCMPANSER 4005 C092h, ADC121.ADCMPANSER 4005 C292h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPOCA	CMPTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPTSA	Temperature Sensor Output Compare Select	0: Exclude the temperature sensor output from the compare window A target range 1: Include the temperature sensor output in the compare window A target range.	R/W
b1	CMPOCA	Internal Reference Voltage Compare Select	0: Exclude the internal reference voltage from the compare window A target range. 1: Include the internal reference voltage in the compare window A target range.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPTSA bit (Temperature Sensor Output Compare Select)

The compare window A function is enabled by setting the CMPTSA bit to 1 while the ADEXICR.TSSA bit or the

ADEXICR.TSSB bit is 1. Only set the CMPTSA bit when the ADCSR.ADST bit is 0.

CMPOCA bit (Internal Reference Voltage Compare Select)

The compare window A function is enabled by setting the CMPOCA bit to 1 while the ADEXICR.OCSA bit or the ADEXICR.OCSB bit is 1. Only set the CMPOCA bit when the ADCSR.ADST bit is 0.

35.2.23 A/D Compare Function Window A Comparison Condition Setting Register 0 (ADCMPLR0)

Address(es): ADC120.ADCMPLR0 4005 C098h, ADC121.ADCMPLR0 4005 C298h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMPLCHA07	CMPLCHA06	CMPLCHA05	—	CMPLCHA03	CMPLCHA02	CMPLCHA01	CMPLCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CMPLCHA03 to CMPLCHA00	Compare Window A Comparison Condition Select	These bits set comparison conditions for channels to which window A comparison conditions are applied, selected from AN000 to AN003 (unit 0), and AN100 to AN102 (unit 1). Comparison conditions are shown in Figure 35.4. • When window function is disabled (ADCMPCR.WCMPE = 0): 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1): 0: A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7 to b5	CMPLCHA07 to CMPLCHA05	Compare Window A Comparison Condition Select	These bits set comparison conditions for channels to which window A comparison conditions are applied, selected from AN005 to AN007 (unit 0), and AN105 to AN107 (unit 1). Comparison conditions are shown in Figure 35.4. • When the window function is disabled (ADCMPCR.WCMPE = 0): 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When the window function is enabled (ADCMPCR.WCMPE = 1): 0: A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPLCHAn bits (n = 00 to 03, 05 to 07) (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels to which window A comparison conditions are applied, selected from AN000 to AN003, AN005 to AN007 (unit 0) and AN100 to AN102, AN105 to AN107 (unit 1). These bits can be set for each analog input to be compared. In unit 0, CMPLCHA00 is associated with AN000 and CMPLCHA07 with AN007. In unit 1, CMPLCHA00 is associated with AN100 and CMPLCHA07 with AN107. When the comparison result of each analog input meets the set condition, the ADCMPSR0.CMPSTCHAn flag is set to 1, and a compare interrupt (ADC12i_CMPAI (i = 0, 1)) is generated.

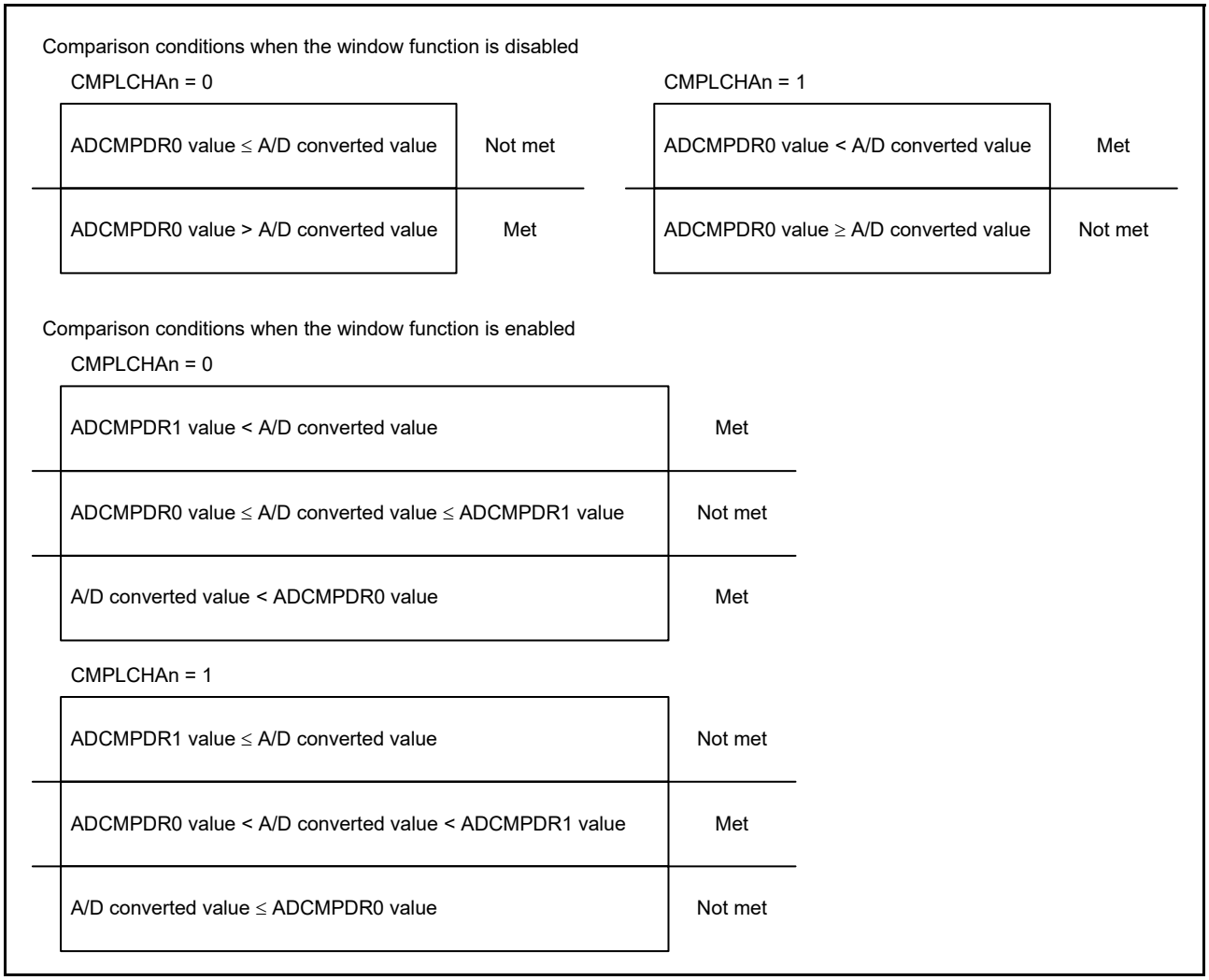


Figure 35.4 Explanation of comparison conditions for compare function window A

35.2.24 A/D Compare Function Window A Comparison Condition Setting Register 1 (ADCMPLR1)

Address(es): ADC120.ADCMPLR1 4005 C09Ah, ADC121.ADCMPLR1 4005 C29Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPLCHA20	—	CMPLCHA18	CMPLCHA17	CMPLCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CMPLCHA18 to CMPLCHA16	Compare Window A Comparison Condition Select	These bits set comparison conditions for channels to which window A comparison conditions are applied, selected from AN016 to AN018 (unit 0) and AN116, AN117 (unit 1). Comparison conditions are shown in Figure 35.4. • When window function is disabled (ADCMPCR.WCMPE = 0) 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1) 0: A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	CMPLCHA20	Compare Window A Comparison Condition Select	This bit sets comparison condition for channels to which window A comparison condition is applied, selected as AN020 (unit 0). Comparison condition is shown in Figure 35.4. • When window function is disabled (ADCMPCR.WCMPE = 0) 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1) 0: A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPLCHAn bits (n = 16 to 18, 20) (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels to which window A comparison conditions are applied, selected from AN016 to AN018, AN020 (unit 0) and AN116, AN117 (unit 1). These bits can be set for each analog input to be compared. In unit 0, CMPLCHA16 is associated with AN016, and CMPLCHA20 with AN020. In unit 1, CMPLCHA16 is associated with AN116, and CMPLCHA17 with AN117. When the comparison result of each analog input meets the set condition, the ADCMPSR1.CMPSTCHAn flag is set to 1 and a compare interrupt (ADC12i_CMPAI (i = 0, 1)) is generated.

35.2.25 A/D Compare Function Window A Extended Input Comparison Condition Setting Register (ADCMPLER)

Address(es): ADC120.ADCMPLER 4005 C093h, ADC121.ADCMPLER 4005 C293h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPLOCA	CMPLTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPLTSA	Compare Window A Temperature Sensor Output Comparison Condition Select	Comparison conditions are shown in Figure 35.4. • When window function is disabled (ADCMPCR.WCMPE = 0) 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1) 0: A/D-converted value < ADCMPDR0 value, or A/D-converted value > ADCMPDR1 value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W.
b1	CMPLOCA	Compare Window A Internal Reference Voltage Comparison Condition Select	Comparison conditions are shown in Figure 35.4. • When window function is disabled (ADCMPCR.WCMPE = 0) 0: ADCMPDR0 register value > A/D-converted value 1: ADCMPDR0 register value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1) 0: A/D-converted value < ADCMPDR0 register value, or A/D-converted value > ADCMPDR1 register value 1: ADCMPDR0 register value < A/D-converted value < ADCMPDR1 register value.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R

CMPLTSA bit (Compare Window A Temperature Sensor Output Comparison Condition Select)

The CMPLTSA bit specifies comparison conditions when the temperature sensor output is the target for the window A comparison condition. When the temperature sensor output comparison result meets the set condition, the ADCMPSER.CMPSTTSA flag is set to 1 and a compare interrupt (ADC12i_CMPAI (i = 0, 1)) is generated.

CMPLOCA bit (Compare Window A Internal Reference Voltage Comparison Condition Select)

The CMPLOCA bit specifies comparison conditions when the internal reference voltage is the target for the window A comparison condition. When the internal reference voltage comparison result meets the set condition, the ADCMPSER.CMPSTOCA flag is set to 1 and a compare interrupt (ADC12i_CMPAI) is generated.

35.2.26 A/D Compare Function Window A Lower-Side Level Setting Register (ADCMPDR0), A/D Compare Function Window A Upper-Side Level Setting Register (ADCMPDR1), A/D Compare Function Window B Lower-Side Level Setting Register (ADWINLLB), A/D Compare Function Window B Upper-Side Level Setting Register (ADWINULB)

Address(es): ADC120.ADCMPDR0 4005 C09Ch, ADC120.ADCMPDR1 4005 C09Eh, ADC120.ADWINLLB 4005 C0A8h, ADC120.ADWINULB 4005 C0AAh, ADC121.ADCMPDR0 4005 C29Ch, ADC121.ADCMPDR1 4005 C29Eh, ADC121.ADWINLLB 4005 C2A8h, ADC121.ADWINULB 4005 C2AAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	—	Reference value	R/W

The ADCMPDRy (y = 0, 1) register specifies the reference data when the compare window A function is used. ADCMPDR0 sets the lower reference for window A, and ADCMPDR1 sets the upper reference for window A.

ADWINULB and ADWINLLB specify the reference data when the compare window B function is used. ADWINLLB sets the lower reference for window B, and ADWINULB sets the upper reference for window B. The ADCMPDRy, ADWINULB, and ADWINLLB are read/write registers.

ADCMPDRy, ADWINULB, and ADWINLLB can be written to, even during A/D conversion. The reference data can be dynamically changed by rewriting the register values during A/D conversion.

Set these registers so that the upper reference is not less than the lower reference (ADCMPDR1 ≥ ADCMPDR0 and ADWINULB ≥ ADWINLLB). ADCMPDR1 and ADWINULB are not used when the window function is disabled.

Note: The lower and upper references are changed when each register is written. For example, when the upper reference value changed and the lower reference value are changed, the MCU compares the upper reference (after a rewrite), and the lower reference (before a rewrite) with the A/D conversion result. See Figure 35.5. If the comparison during the rewriting of these two references is erroneous, then rewrite these reference values when both ADCSR.ADST and the associated compare window operation enable bit (ADCMPCR.CMPAE or ADCMPCR.CMPBE) are 0.

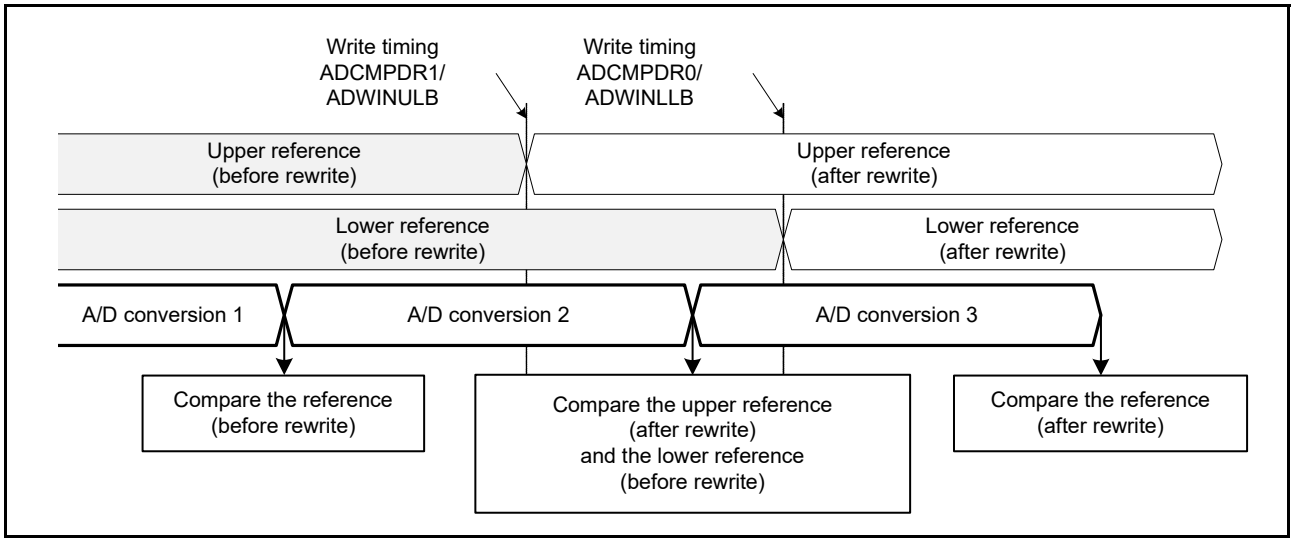


Figure 35.5 Comparison between upper and lower references before and after a rewrite

The ADCMPDRy, ADWINLLB, and ADWINULB registers use different formats depending on the following conditions:

- The value in the A/D Data Register Format Select bit (flush-right or flush-left)
- The value in the A/D Conversion Accuracy Specify bit (12-bit, 10-bit, or 8-bit)
- The value in the A/D-Converted Value Addition/Average Channel Select bits (A/D-converted value addition mode selected or not selected).

The data formats for each condition are described in this section.

(1) When A/D-converted value addition mode is not selected

- Flush-right data with 12-bit accuracy: Lower 12 bits ([11:0]) are valid
- Flush-right data with 10-bit accuracy: Lower 10 bits ([9:0]) are valid
- Flush-right data with 8-bit accuracy: Lower 8 bits ([7:0]) are valid
- Flush-left data with 12-bit accuracy: Upper 12 bits ([15:4]) are valid
- Flush-left data with 10-bit accuracy: Upper 10 bits ([15:6]) are valid
- Flush-left data with 8-bit accuracy: Upper 8 bits ([15:8]) are valid.

(2) When A/D-converted value addition mode is selected

- Flush-right data with 12-bit accuracy: Lower 14 bits ([13:0]) are valid
- Flush-right data with 10-bit accuracy: Lower 12 bits ([11:0]) are valid
- Flush-right data with 8-bit accuracy: Lower 10 bits ([9:0]) are valid
- Flush-left data with 12-bit accuracy: Upper 14 bits ([15:2]) are valid
- Flush-left data with 10-bit accuracy: Upper 12 bits ([15:4]) are valid
- Flush-left data with 8-bit accuracy: Upper 10 bits ([15:6]) are valid.

35.2.27 A/D Compare Function Window A Channel Status Register 0 (ADCMPSR0)

Address(es): ADC120.ADCMPSR0 4005 C0A0h, ADC121.ADCMPSR0 4005 C2A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMPSTCHA07	CMPSTCHA06	CMPSTCHA05	—	CMPSTCHA03	CMPSTCHA02	CMPSTCHA01	CMPSTCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CMPSTCHA03 to CMPSTCHA00	Compare Window A Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1b), these bits indicate the comparison result of the channels to which window A comparison conditions are applied, selected from AN000 to AN003 (unit 0) and AN100 to AN102 (unit 1). 0: Comparison conditions are not met 1: Comparison conditions are met.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7 to b5	CMPSTCHA07 to CMPSTCHA05	Compare Window A Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1b), these bits indicate the comparison result of the channels to which window A comparison conditions are applied, selected from AN005 to AN007 (unit 0) and AN105 to AN107 (unit 1). 0: Comparison conditions are not met 1: Comparison conditions are met.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTCHAn flags (n = 00 to 03, 05 to 07) (Compare Window A Flag)

The CMPSTCHAn flags indicate the comparison results for channels to which window A comparison conditions are applied, selected from AN000 to AN003, AN005 to AN007 (unit 0), and AN100 to AN102, AN105 to AN107 (unit 1). When a comparison condition set in ADCMPLR0.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn flag is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI (i = 0, 1)) is generated when this flag is set to 1. In unit 0, CMPSTCHA00 is associated with AN000, and CMPSTCHA07 with AN007. In unit 1, CMPSTCHA00 is associated with AN100, and CMPSTCHA07 with AN107.

Writing 1 to the CMPSTCHAn flags is invalid.

[Setting condition]

- The condition set in ADCMPLR0.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

35.2.28 A/D Compare Function Window A Channel Status Register1 (ADCMPSR1)

Address(es): ADC120.ADCMPSR1 4005 C0A2h, ADC121.ADCMPSR1 4005 C2A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPSTCHA20	—	CMPSTCHA18	CMPSTCHA17	CMPSTCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CMPSTCHA18 to CMPSTCHA16	Compare Window A Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1), these bits indicate the comparison result of the channels to which window A comparison conditions are applied, selected from AN016 to AN018 (unit 0) and AN116, AN117 (unit 1). 0: Comparison conditions are not met 1: Comparison conditions are met.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	CMPSTCHA20	Compare Window A Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1b), this bit indicates the comparison result of the channel to which window A comparison condition is applied, selected AN020(unit 0). 0: Comparison conditions are not met 1: Comparison conditions are met.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTCHAn flags (n = 16 to 18, 20) (Compare Window A Flag)

The CMPSTCHAn flags indicate the comparison results for channels to which window A comparison conditions are applied, selected from AN016 to AN018, AN020 (unit 0), and AN116, AN117 (unit 1). When the comparison condition set in ADCMPLR1.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn flag is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI (i = 0, 1)) is generated when this flag is set to 1. In unit 0, CMPSTCHA16 is associated with AN016, and CMPSTCHA20 with AN020. In unit 1, CMPSTCHA16 is associated with AN116, and CMPSTCHA17 with AN117.

Writing 1 to the CMPSTCHAn flags is invalid.

[Setting condition]

- The condition set in ADCMPLR1.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

35.2.29 A/D Compare Function Window A Extended Input Channel Status Register (ADCMPSER)

Address(es): ADC120.ADCMPSER 4005 C0A4h, ADC121.ADCMPSER 4005 C2A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPSTTSA	Compare Window A Temperature Sensor Output Compare Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the temperature sensor output comparison result. 0: Comparison conditions are not met 1: Comparison conditions are met.	R/W
b1	CMPSTOCA	Compare Window A Internal Reference Voltage Compare Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the internal reference voltage comparison result. 0: Comparison conditions are not met 1: Comparison conditions are met.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTTSA flag (Compare Window A Temperature Sensor Output Compare Flag)

The CMPSTTSA flag indicates the temperature sensor output comparison result. When the comparison condition set in ADCMPLER.CMPLTSA is met at the end of A/D conversion, this flag is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI (i = 0, 1)) is generated when this flag is set to 1.

Writing 1 to the CMPSTTSA flag is invalid.

[Setting condition]

- The condition set in ADCMPLER.CMPLTSA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

CMPSTOCA flag (Compare Window A Internal Reference Voltage Compare Flag)

The CMPSTOCA flag indicates the internal reference voltage comparison result. When the comparison condition set in ADCMPLER.CMPLOCA is met at the end of A/D conversion, this flag is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI) is generated when this flag is set to 1.

Writing 1 to the CMPSTOCA flag is invalid.

[Setting condition]

- The condition set in ADCMPLER.CMPLOCA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

35.2.30 A/D Compare Function Window B Channel Select Register (ADCMPBNSR)

Address(es): ADC120.ADCMPBNSR 4005 C0A6h, ADC121.ADCMPBNSR 4005 C2A6h

	b7	b6	b5	b4	b3	b2	b1	b0
	CMPLB	—	CMPCHB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	CMPCHB[5:0]	Compare Window B Channel Select	These bits select channels to be compared with the compare window B conditions. The maximum channel is AN020 in unit 0 and AN117 in unit 1. b5 b0 Unit 0 Unit 1 0 0 0 0 0 0: AN000 AN100 0 0 0 0 0 1: AN001 AN101 0 0 0 0 1 0: AN002 AN102 0 0 0 0 1 1: AN003 — 0 0 0 1 0 1: AN005 AN105 0 0 0 1 1 0: AN006 AN106 0 0 0 1 1 1: AN007 AN107 0 1 0 0 0 0: AN016 AN116 0 1 0 0 0 1: AN017 AN117 0 1 0 0 1 0: AN018 — 0 1 0 1 0 0: AN020 — 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage 1 1 1 1 1 1: Do no select. Other settings are prohibited.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	CMPLB	Compare Window B Comparison Condition Setting	This bit sets comparison conditions for the channels for window B. The comparison conditions are shown in Figure 35.6. • When window function is disabled (ADCMPCR.WCMPE = 0) 0: CMPLLB value > A/D-converted value 1: CMPLLB value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1) 0: A/D-converted value < CMPLLB value, or CMPULB value < A/D-converted value 1: CMPLLB value < A/D-converted value < CMPULB value.	R/W

CMPCHB[5:0] bits (Compare Window B Channel Select)

The CMPCHB[5:0] bits specify the channels to be compared with the compare window B conditions from AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020 (unit 0), AN100 to AN102, AN105 to AN107, AN116, AN117 (unit 1), the temperature sensor, and the internal reference voltage. The compare window B function is enabled by specifying the hexadecimal number of the A/D conversion channel selected in the following bits:

Unit 0

- ADANSA0.ANSA00 to ANSA03 bits
- ADANSA0.ANSA05 to ANSA07 bits
- ADANSA1.ANSA16 toANSA018, ANSA20 bits
- ADANSB0.ANSB00 to ANSB03 bits
- ADANSB0.ANSB05 to ANSB07 bits
- ADANSB1.ANSB16 to ANSB18, ANSB20 bits.

Unit 1

- ADANSA0.ANSA00 to ANSA02 bits

- ADANSA0.ANSA05 to ANSA07 bits
- ADANSA1.ANSA16, ANSA17 bits
- ADANSB0.ANSB00 to ANSB02 bits
- ADANSB0.ANSB05 to ANSB07 bits
- ADANSB1.ANSB16, ANSB17 bits.

Set the CMPCHB[5:0] bits while the ADCSR.ADST bit is 0.

CMPLB bit (Compare Window B Comparison Condition Setting)

The CMPLB bit specifies the comparison conditions for the channels for window B. When the comparison result of an analog input meets the set condition, the associated ADCMPBSR.CMPSTB flag is set to 1, and a compare interrupt request (ADC12i_CMPBI (i = 0, 1)) is generated.

Compare conditions when the window function is disabled

CMPLB = 0		CMPLB = 1	
ADWINLLB value ≤ A/D converted value	Not met	ADWINLLB value < A/D converted value	Met
ADWINLLB value > A/D converted value	Met	ADWINLLB value ≥ A/D converted value	Not met

Compare conditions when the window function is enabled

CMPLB = 0

A/D converted value > ADWINULB value	Met
ADWINLLB value ≤ A/D converted value ≤ ADWINULB value	Not met
A/D converted value < ADWINLLB value	Met

CMPLB = 1

A/D converted value ≥ ADWINULB value	Not met
ADWINLLB value <A/D converted value < ADWINULB value	Met
A/D converted value ≤ ADWINLLB value	Not met

Figure 35.6 Explanation of compare conditions for compare function for window B

35.2.31 A/D Compare Function Window B Status Register (ADCMPBSR)

Address(es): ADC120.ADCMPBSR 4005 C0ACh, ADC121.ADCMPBSR 4005 C2ACh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPSTB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPSTB	Compare Window B Flag	When window B operation is enabled (ADCMPCR.CMPBE = 1), this bit indicates the comparison result of the channels to which window B comparison conditions are applied, selected from AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020 (unit 0), AN100 to AN102, AN105 to AN107, and AN116, AN117 (unit 1), temperature sensor output, and internal reference voltage. 0: Comparison conditions are not met 1: Comparison conditions are met.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTB flag (Compare Window B Flag)

The CMPSTB flag indicates the comparison result of the channels to which window B comparison conditions are applied, selected from AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020 (unit 0), AN100 to AN102, AN105 to AN107, AN116, AN117 (unit 1), the temperature sensor, and the internal reference voltage. When the comparison condition set in ADCMPBNSR.CMPLB is met at the end of A/D conversion, this flag is set to 1. When the ADCMPCR.CMPBIE bit is 1, a compare interrupt request (ADC12i_CMPBI (i = 0, 1)) is generated when this flag is set to 1.

Writing 1 to the CMPSTB flag is invalid.

[Setting condition]

- The condition set in ADCMPBNSR.CMPLB is met when ADCMPCR.CMPBE = 1.

[Clearing condition]

- Writing 0 after reading 1.

35.2.32 A/D Compare Function Window A/B Status Monitor Register (ADWINMON)

Address(es): ADC120.ADWINMON 4005 C08Ch, ADC121.ADWINMON 4005 C28Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MONCOMB	Combination Result Monitor	This bit indicates the combination result. This bit is valid when both window A and window B operations are enabled. 0: Window A/B composite conditions are not met 1: Window A/B composite conditions are met.	R
b3 to b1	—	Reserved	These bits are read as 0	R
b4	MONCMPA	Comparison Result Monitor A	0: Window A comparison conditions are not met 1: Window A comparison conditions are met.	R
b5	MONCMPB	Comparison Result Monitor B	0: Window B comparison conditions are not met 1: Window B comparison conditions are met.	R

Bit	Symbol	Bit name	Description	R/W
b7, b6	—	Reserved	These bits are read as 0	R

MONCOMB bit (Combination Result Monitor)

The read-only MONCOMB bit indicates the combined result of comparison condition results A and B based on the combination condition set in the ADCMPCR.CMPAB[1:0] bits.

[Setting condition]

- The combined result meets the combination condition set in the ADCMPCR.CMPAB[1:0] bits when ADCMPCR.CMPAE = 1 and ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The combined result does not meet the combination condition set in the ADCMPCR.CMPAB[1:0] bits
- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA bit (Comparison Result Monitor A)

The read-only MONCMPA bit is read as 1 when the A/D-converted value of the window A target channel meets the condition set in the ADCMPLR0/ADCMPLR1 and ADCMPLER registers. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in ADCMPLR0.CMPLCHAn when ADCMPCR.CMPAE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in ADCMPLR0.CMPLCHAn when ADCMPCR.CMPAE = 1
- ADCMPCR.CMPAE = 0 (automatically cleared when the ADCMPCR.CMPAE value changes from 1 to 0).

MONCMPB bit (Comparison Result Monitor B)

The read-only MONCMPB bit is read as 1 when the A/D-converted value of the window B target channel meets the condition set in the ADCMPBNSR.CMPLB bit. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1
- ADCMPCR.CMPBE = 0 (automatically cleared when the ADCMPCR.CMPBE value changes from 1 to 0).

35.2.33 A/D Programmable Gain Amplifier Control Register (ADPGACR)

Address(es): ADC120.ADPGACR 4005 C1A0h, ADC121.ADPGACR 4005 C3A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	P002GEN	P002ENAMP	P002SEL1	P002SEL0	P001GEN	P001ENAMP	P001SEL1	P001SEL0	P000GEN	P000ENAMP	P000SEL1	P000SEL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	P000SEL0	PGA P000 Amplifier Bypass Enable	0: Do not output the signal in a path bypassing the PGA amplifier 1: Output the signal in a path bypassing the PGA amplifier.	R/W
b1	P000SEL1	PGA P000 Amplifier Transit Enable	0: Do not output the signal in a path through the PGA amplifier 1: Output the signal in a path through the PGA amplifier.	R/W

Bit	Symbol	Bit name	Description	R/W
b2	P000ENAMP	PGA P000 Amplifier Enable	0: Do not use the PGA amplifier 1: Use the PGA amplifier.	R/W
b3	P000GEN	PGA P000 Gain Setting Enable	0: Disable gain setting 1: Enable gain setting.	R/W
b4	P001SEL0	PGA P001 Amplifier Bypass Enable	0: Do not output the signal in a path bypassing the PGA amplifier 1: Output the signal in a path bypassing the PGA amplifier.	R/W
b5	P001SEL1	PGA P001 Amplifier Transit Enable	0: Do not output the signal in a path through the PGA amplifier 1: Output the signal in a path through the PGA amplifier.	R/W
b6	P001ENAMP	PGA P001 Amplifier Enable	0: Do not use the PGA amplifier 1: Use the PGA amplifier.	R/W
b7	P001GEN	PGA P001 Gain Setting Enable	0: Disable gain setting 1: Enable gain setting.	R/W
b8	P002SEL0	PGA P002 Amplifier Bypass Enable	0: Do not output the signal in a path bypassing the PGA amplifier 1: Output the signal in a path bypassing the PGA amplifier.	R/W
b9	P002SEL1	PGA P002 Amplifier Transit Enable	0: Do not output the signal in a path through the PGA amplifier 1: Output the signal in a path through the PGA amplifier.	R/W
b10	P002ENAMP	PGA P002 Amplifier Enable	0: Do not use the PGA amplifier 1: Use the PGA amplifier.	R/W
b11	P002GEN	PGA P002 Gain Setting Enable	0: Disable gain setting 1: Enable gain setting.	R/W
b12	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b14, b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

Note: See section 35.3.12, Programmable Gain Amplifiers, for details on setting these bits.

PnSEL0 bit (PGA Pn Amplifier Bypass Enable) (n = 000 to 002)

The PnSEL0 bit selects whether to output the signal in a path that bypasses the amplifier in the PGA for each programmable gain amplifier Pn.

PnSEL1 bit (PGA Pn Amplifier Transit Enable) (n = 000 to 002)

The PnSEL1 bit selects whether to output the signal in a path through the amplifier in the PGA for each programmable gain amplifier Pn.

PnENAMP bit (PGA Pn Amplifier Enable) (n = 000 to 002)

The PnENAMP bit selects whether to use the amplifier in the PGA for each programmable gain amplifier Pn.

PnGEN bit (PGA Pn Input Resistance Side Gain Selection Signal Enable) (n = 000 to 002)

The PnGEN bit enables or disables the gain setting for each programmable gain amplifier Pn.

35.2.34 A/D Programmable Gain Amplifier Gain Setting Register 0 (ADPGAGS0)

Address(es): ADC120.ADPGAGS0 4005 C1A2h, ADC121.ADPGAGS0 4005 C3A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	P002GAIN[3:0]				P001GAIN[3:0]				P000GAIN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	P000GAIN[3:0]	PGA P000 Gain Setting	• When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0)	R/W
b7 to b4	P001GAIN[3:0]	PGA P001 Gain Setting	0 0 0 0: × 2.000	R/W
b11 to b8	P002GAIN[3:0]	PGA P002 Gain Setting	0 0 0 1: × 2.500 0 0 1 0: × 2.667 0 0 1 1: × 2.857 0 1 0 0: × 3.077 0 1 0 1: × 3.333 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 1 0 0 1: × 5.000 1 0 1 0: × 5.714 1 0 1 1: × 6.667 1 1 0 0: × 8.000 1 1 0 1: × 10.000 1 1 1 0: × 13.333. • When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1 0 0 0 1: × 1.500 0 1 0 1: × 2.333 1 0 0 1: × 4.000 1 0 1 1: × 5.667. Other settings are prohibited.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. For details on setting these bits, see section 35.3.12, Programmable Gain Amplifiers.

PnGAIN[3:0] bits (PGA Pn Gain Setting) (n = 000 to 002)

The PnGAIN[3:0] bits specify the gain of each PGA amplifier Pn. For pseudo-differential inputs (ADPGADCR0.PnDEN = 1 and ADPGACR.PnGEN = 1), these bits set the gain in combination with ADPGADCR0.PnDG[1:0].

35.2.35 A/D Programmable Gain Amplifier Pseudo-Differential Input Control Register (ADPGADCR0)

Address(es): ADC120.ADPGADCR0 4005 C1B0h, ADC121.ADPGADCR0 4005 C3B0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	P002DEN	—	P002DG[1:0]		P001DEN	—	P001DG[1:0]		P000DEN	—	P000DG[1:0]	
Value after reset:	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	P000DG[1:0]	P000 Pseudo-Differential Input Gain Setting	When these bits are used, set {P000DEN, P000GEN} to 11b. b1 b0 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	P000DEN	P000 Pseudo-Differential Input Enable	0: Disable pseudo-differential input 1: Enable pseudo-differential input.	R/W
b5, b4	P001DG[1:0]	P001 Pseudo-Differential Input Gain Setting	When these bits are used, set {P001DEN, P001GEN} to 11b. b5 b4 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	P001DEN	P001 Pseudo-Differential Input Enable	0: Disable pseudo-differential input 1: Enable pseudo-differential input.	R/W
b9, b8	P002DG[1:0]	P002 Pseudo-Differential Input Gain Setting	When these bits are used, set {P002DEN, P002GEN} to 11b. b9 b8 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667.	R/W
b10	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11	P002DEN	P002 Pseudo-Differential Input Enable	0: Disable pseudo-differential input 1: Enable pseudo-differential input.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: For details on setting these bits, see section 35.3.12, Programmable Gain Amplifiers.

PnDG[1:0] bits (Pn Pseudo-Differential Input Gain Setting) (n = 000 to 002)

The PnDG[1:0] bits specify the gain of each PGA amplifier Pn when pseudo-differential inputs are used. These bits are only valid when the PnDEN bit is 1 and the PnGEN bit is 1.

To use the PGA for pseudo-differential inputs, set the ADPGADCR0.PnDG[1:0] bits in conjunction with the ADPGAGS0.PnGAIN[3:0] bits.

Example: To set the gain to × 1.5 using P000 for pseudo-differential input, set:
ADPGAGS0.P000GAIN[3:0] = 0001b
ADPGADCR0.P000DG[1:0] = 00b.

PnDEN bit (Pn Pseudo-Differential Input Enable) (n = 000 to 002)

The PnDEN bit enables or disables pseudo-differential inputs for each PGA amplifier Pn.

35.3 Operation

35.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.

Scan conversion is performed in three operating modes:

- Single scan mode
- Continuous scan mode
- Group scan mode.

In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until the ADCSR.ADST bit is cleared to 0 from 1 by software. In group scan mode, the selected channels in group A and the selected channels in group B are scanned once after scan starts in response to the respective synchronous trigger (ELC).

In single scan mode and continuous scan mode, A/D conversion is performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. In group scan mode, A/D conversion is performed for the ANn channels in group A selected in the ADANSA0 and ADANSA1 registers first, and then for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.

When self-diagnosis is selected, it is executed once at the beginning of each scan, and one of the three voltages generated internally in the ADC12 is converted.

The temperature sensor output and internal reference voltage can be selected at the same time as the analog input of the channels, and A/D conversion is performed on the analog input of channels, temperature sensor output, and internal reference voltage, in that order.

Double trigger mode can be used with single scan mode or group scan mode. With double trigger mode enabled (ADCSR.DBLE = 1), A/D conversion data of a channel selected in the ADCSR.DBLANS[4:0] bits is duplicated only if the conversion is started by the synchronous trigger (ELC) selected in the TRSA[5:0] bits in ADSTRGR. Only group A in group scan mode can use the double trigger mode.

The extended operation of double trigger mode means the A/D conversion operation is generated from the synchronous trigger combination. This trigger combination is selected in ADSTRGR.TRSA[5:0] in double trigger mode. ELC_AD00 and ELC_AD01 are associated with unit 0. ELC_AD10 and ELC_AD11 are associated with unit 1.

In the extended operation of double trigger mode, in addition to normal double-trigger operation, A/D conversion data from the ELC_AD00 (unit 0) and ELC_AD10 (unit 1) triggers is stored in the A/D Data Duplexing Register A (ADDBLDRA), and A/D conversion data from the ELC_AD01 (unit 0) and ELC_AD11 (unit 1) triggers is stored in the A/D Data Duplexing Register B (ADDBLDRB). In the extended operation of double trigger mode, when a combination of triggers occurs at the same time, the data duplexing register settings for the specified triggers do not work, and A/D conversion data is stored in the A/D Data Duplexing Register B (ADDBLDRB).

When one synchronous trigger is input during the A/D conversion started by another synchronous trigger, the subsequent trigger is input when the other A/D conversion is canceled.

When any of the AN000 to AN002 (unit 0), and AN100 to AN102 (unit 1) channels are set as a channel-dedicated sample-and-hold circuit in the SHANS[2:0] bits in ADSHCR, the target analog input specified is sampled and held before the first A/D conversion of each scan.

35.3.2 Single Scan Mode

35.3.2.1 Basic operation without channel-dedicated sample-and-hold circuits

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels. as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input, A/D conversion is performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.

2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (without register setting).
4. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then the ADC12 enters a wait state.

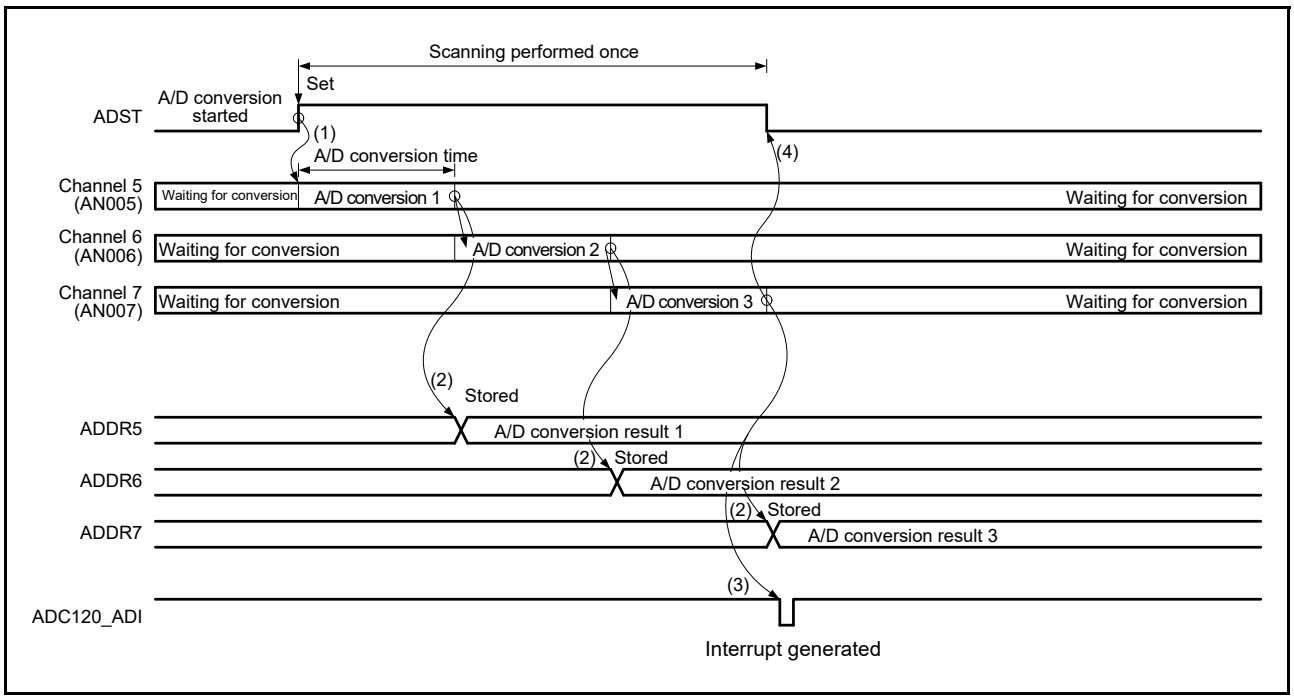


Figure 35.7 Example of basic operation in single scan mode when AN005 to AN007 are selected

35.3.2.2 Basic operation with channel-dedicated sample-and-hold circuits and continuous sampling disabled

When the channel-dedicated sample-and-hold circuit is used, sample-and-hold operation is first performed, and then A/D conversion is performed once on the analog input of all the specified channels. The channels whose dedicated sample-and-hold circuit is to be used can be selected in the SHANS[2:0] bits in ADSHCR.

The operation is as follows:

1. Analog input sampling of all channels whose dedicated sample-and-hold circuit is to be used starts when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After sample-and-hold operation, A/D conversion is performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
5. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then, the ADC12 enters a wait state.

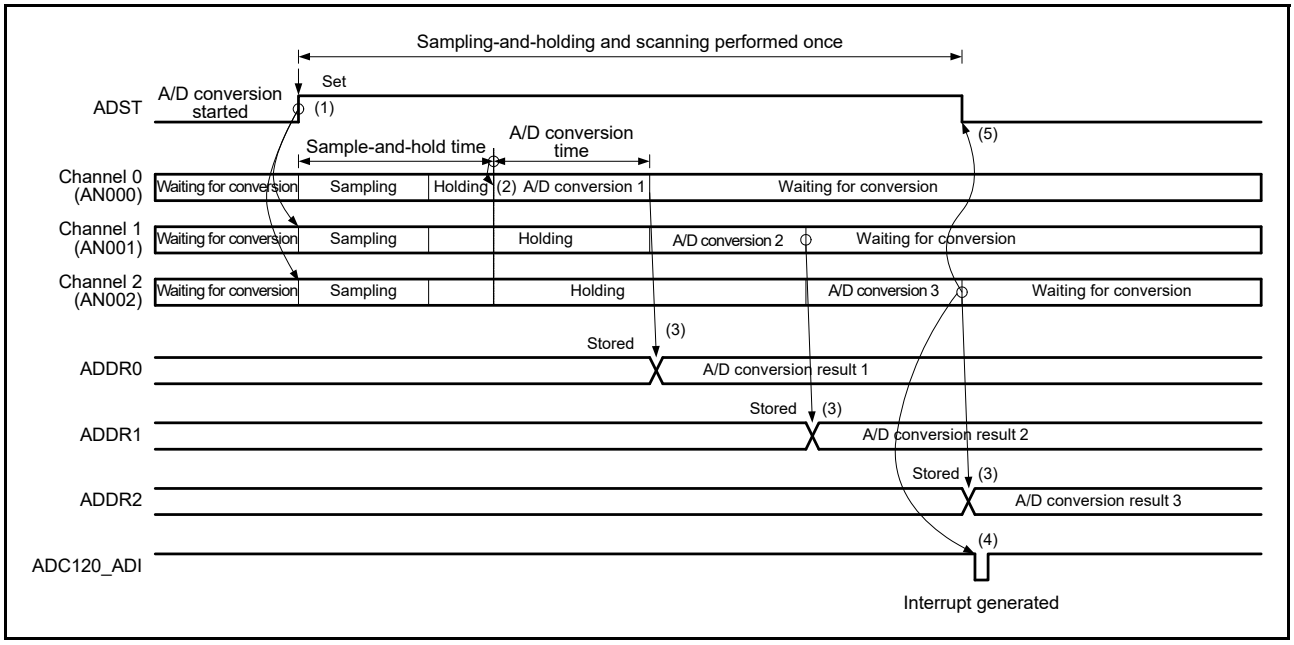


Figure 35.8 Example of operation in single scan mode when the channel-dedicated sample-and-hold circuits are used and AN000 to AN002 are selected

35.3.2.3 Basic operation with channel-dedicated sample-and-hold circuits and continuous sampling enabled

When a channel-dedicated sample-and-hold circuit is used while continuous sampling is enabled, sample-and-hold operation is performed first, followed by A/D conversion once on the analog inputs of all selected channels. The ADSHCR.SHANS[2:0] bits specify the channels for which the channel-dedicated sample-and-hold circuits are to be used.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
5. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (without register setting).
6. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then, the ADC12 enters a wait state. If this is followed by single scanning, set the continuous sampling time for the sample-and-hold circuits to at least 400 ns (when the permissible signal source impedance is 1 kΩ).
7. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.

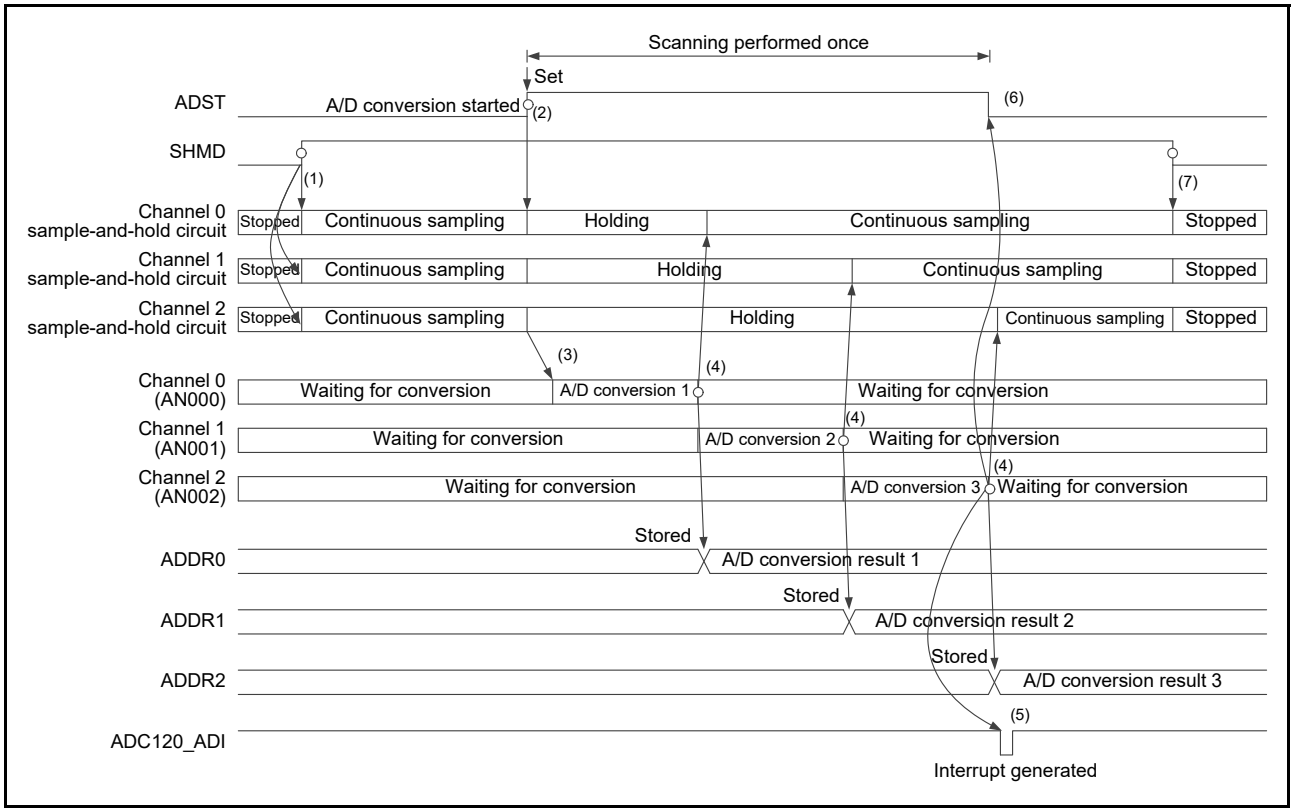


Figure 35.9 Example of operation in single scan mode when channel-dedicated sample-and-hold circuits are used, AN000 to AN002 are selected, and continuous sampling is enabled

35.3.2.4 Channel selection and self-diagnosis without channel-dedicated sample-and-hold circuits

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage VREFH0 (unit 0) or VREFH (unit 1) (× 0, × 1/2, or × 1) supplied to the ADC12, and then A/D conversion is performed once on the analog input of the specified channels.

The operation is as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
5. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then, the ADC12 enters a wait state.

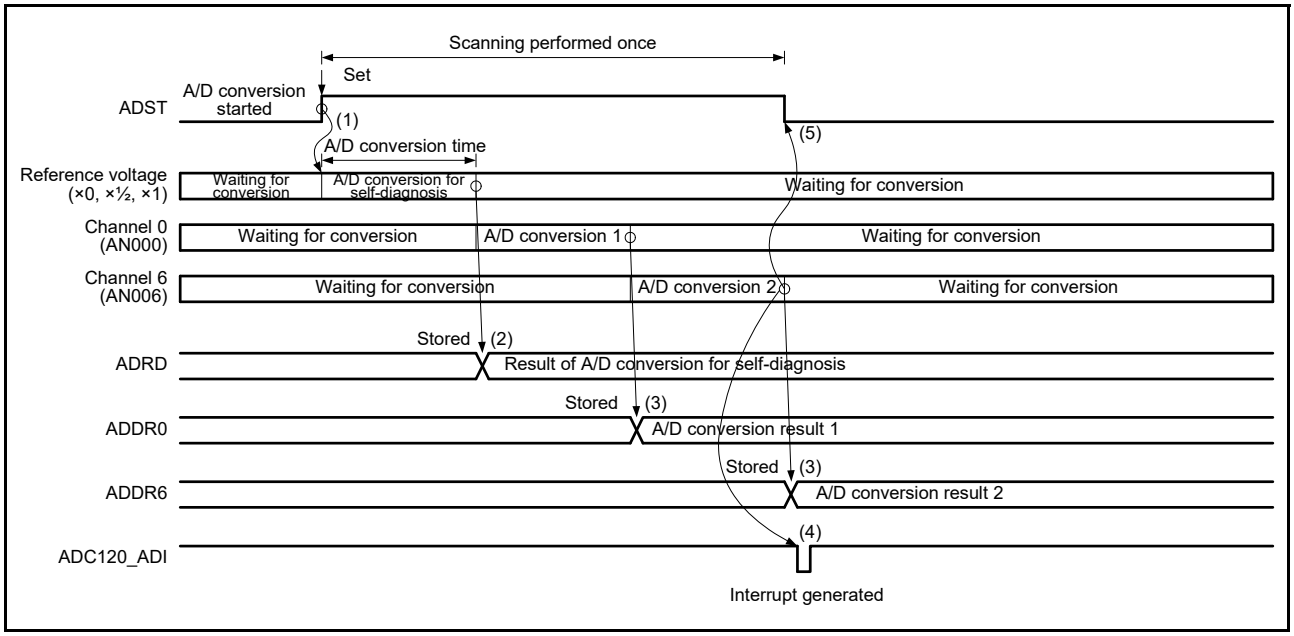


Figure 35.10 Example of basic operation in single scan mode when AN000 and AN006 are selected with self-diagnosis

35.3.2.5 Channel selection and self-diagnosis with channel-dedicated sample-and-hold circuits and continuous sampling disabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used while continuous sampling is disabled, the sample-and-hold operation is performed first, and then A/D conversion is performed once for the reference voltage VREFH0 (unit 0) or VREFH (unit 1) (×0, ×1/2, or ×1) supplied to the ADC12. After that, A/D conversion is performed only once on the analog input of the selected channels.

The operation is as follows:

1. Analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After sample-and-hold operation, A/D conversion for self-diagnosis starts.
3. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
5. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (without register setting).
6. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then, the ADC12 enters a wait state.

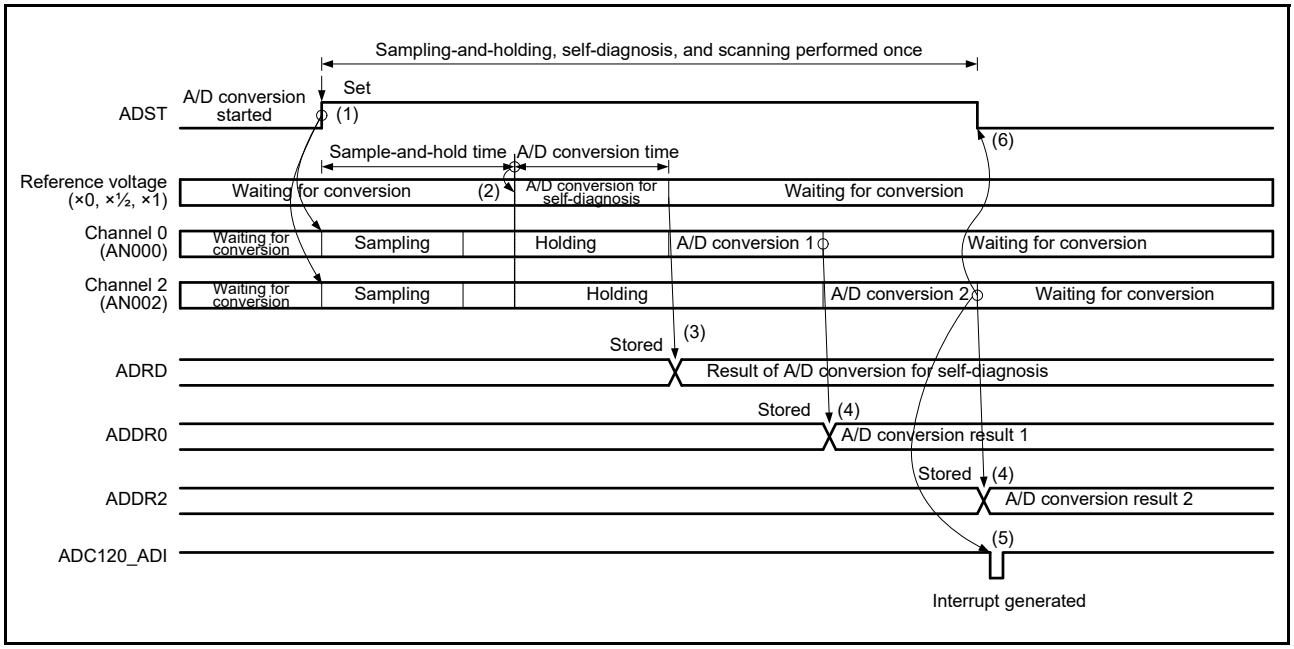


Figure 35.11 Example of operation in single scan mode when channel-dedicated sample-and-hold circuits are used, AN000 and AN002 are selected with self-diagnosis, and continuous sampling is disabled

35.3.2.6 Channel selection and self-diagnosis with channel-dedicated sample-and-hold circuits and continuous sampling enabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used while continuous sampling is enabled, sample-and-hold operations are performed first, and this is followed by A/D conversion of the reference voltage VREFH0 (unit 0) or VREFH (unit 1) supplied to the ADC12. After that, A/D conversion is performed only once on the analog input of the selected channels.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger. Set the ADCSR.ADST bit to 1 after at least 400 ns (when the permissible signal source impedance is 1 kΩ) elapse after the ADSHMSR.SHMD bit is set to 1.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion for self-diagnosis starts.
4. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
6. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (without register setting).
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then, the ADC12 enters a wait state. If this is followed by single scanning, set the continuous sampling time for the sample-and-hold circuits to at least 400 ns (when the permissible signal source impedance is 1 kΩ).
8. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.

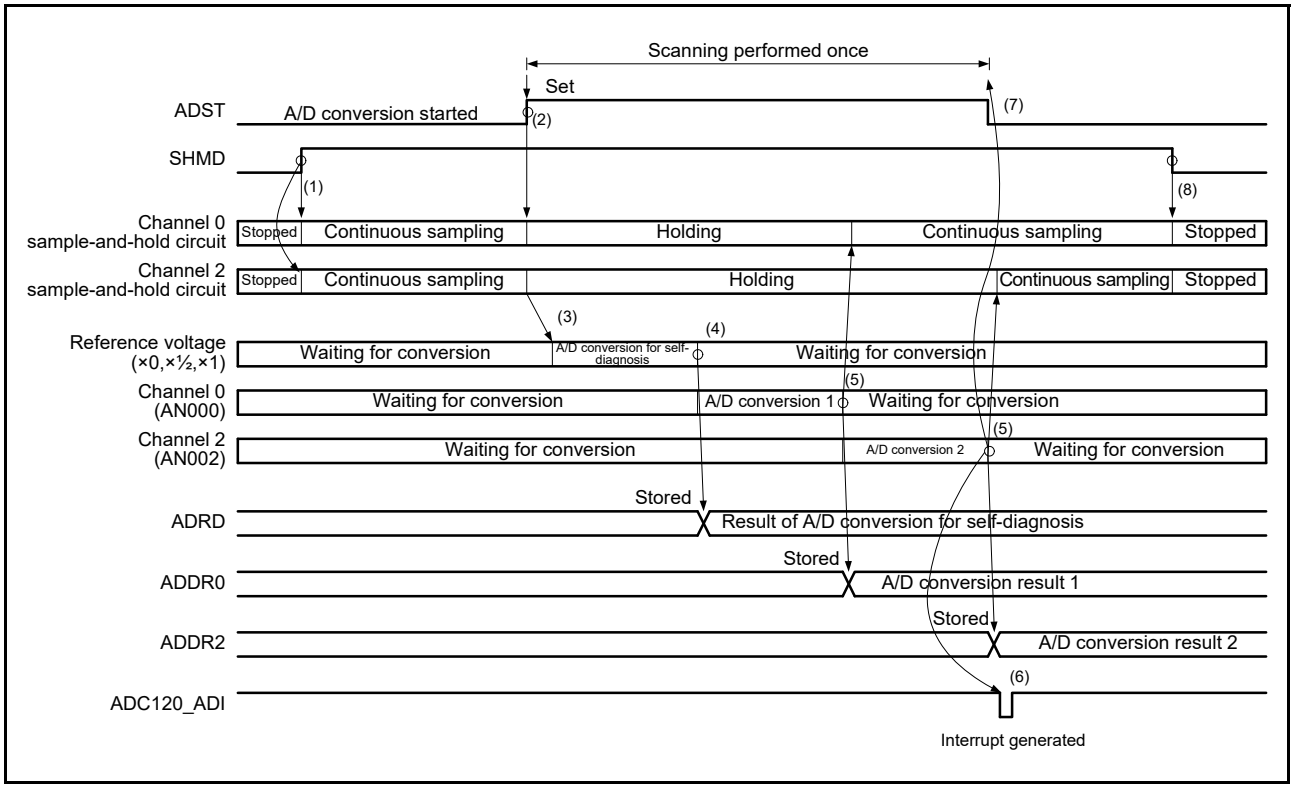


Figure 35.12 Example of operation in single scan mode when channel-dedicated sample-and-hold circuits are used, AN000 to AN002 are selected with self-diagnosis, and continuous sampling is enabled

35.3.2.7 A/D conversion of temperature sensor output or internal reference voltage

When the channels and temperature sensor output or internal reference voltage are selected at the same time, A/D conversion is first performed on the analog input of the selected channels, and then A/D conversion is performed once on the temperature sensor output or internal reference voltage. When both temperature sensor output and internal reference voltage are selected, A/D conversion of the temperature sensor output and internal reference voltage is performed, in that order. With the channels deselected, selecting only the temperature sensor output or internal reference voltage is also possible.

The operation is as follows:

1. When a software trigger, synchronous trigger (ELC), or asynchronous trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. On completion of A/D conversion on the channels, the result is stored in the associated A/D Data Register y (ADDRy), and then A/D conversion of the temperature sensor output starts.
3. On completion of A/D conversion of the temperature sensor output, the result is stored in the associated A/D Temperature Sensor Data Register (ADTSDR), and then A/D conversion of the internal reference voltage starts.
4. On completion of A/D conversion of the internal reference voltage, the result is stored in the associated A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC12i_ADI (i = 0, 1) interrupt request is generated (without register setting).
5. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 on completion of A/D conversion. Then, the ADC12 enters a wait state.

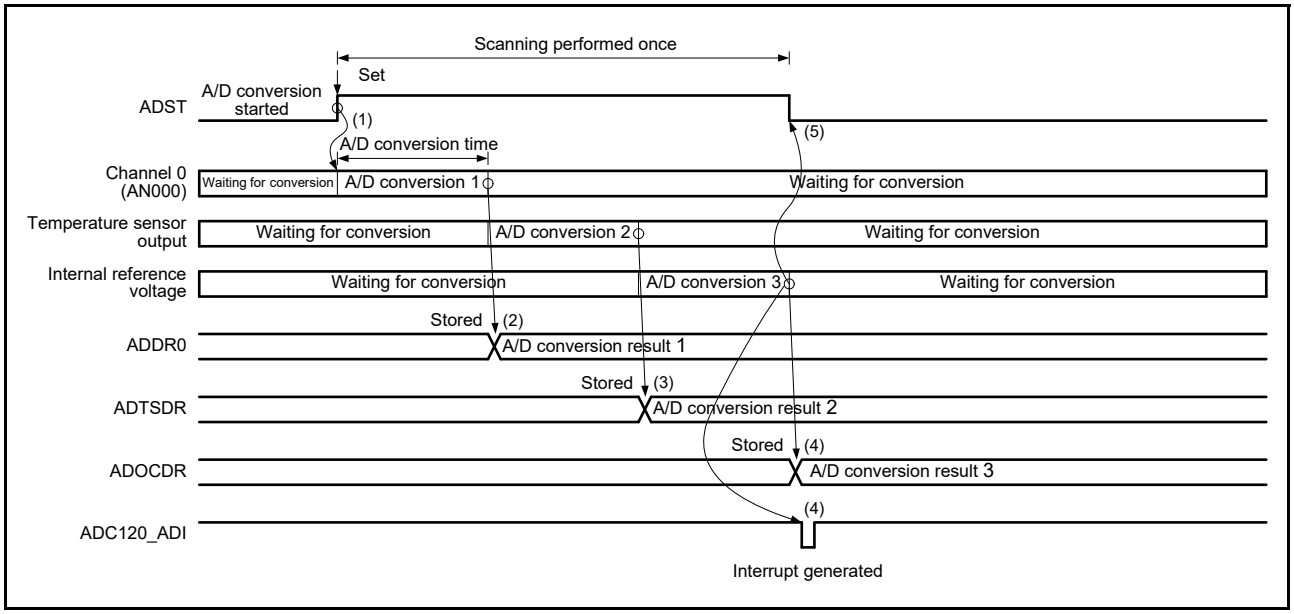


Figure 35.13 Example of basic operation in single scan mode when AN000 and temperature sensor output or internal reference voltage are selected

35.3.2.8 A/D conversion in double trigger mode

When double trigger mode is selected in single scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed in sequence.

Deselect self-diagnosis, and set the addition/average mode select bits for both temperature sensor output (ADEXICR.TSSA) and internal reference voltage (ADEXICR.OCSA) to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In double trigger mode, select a synchronous trigger (ELC) using the ADSTRGR.TRSA[5:0] bits, and in ADCSR, set the EXTRG bit to 0 and the TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
3. The ADST bit is automatically cleared to 0 and the ADC12 enters a wait state. An ADC12i_ADI (i = 0, 1) interrupt request is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input, A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the result is stored in the A/D Data Duplexing Register (ADDBLDR), which is exclusively used in double trigger mode.
6. An ADC12i_ADI (i = 0, 1) interrupt request is generated (without register setting).
7. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion completes. Then, the ADC12 enters a wait state.

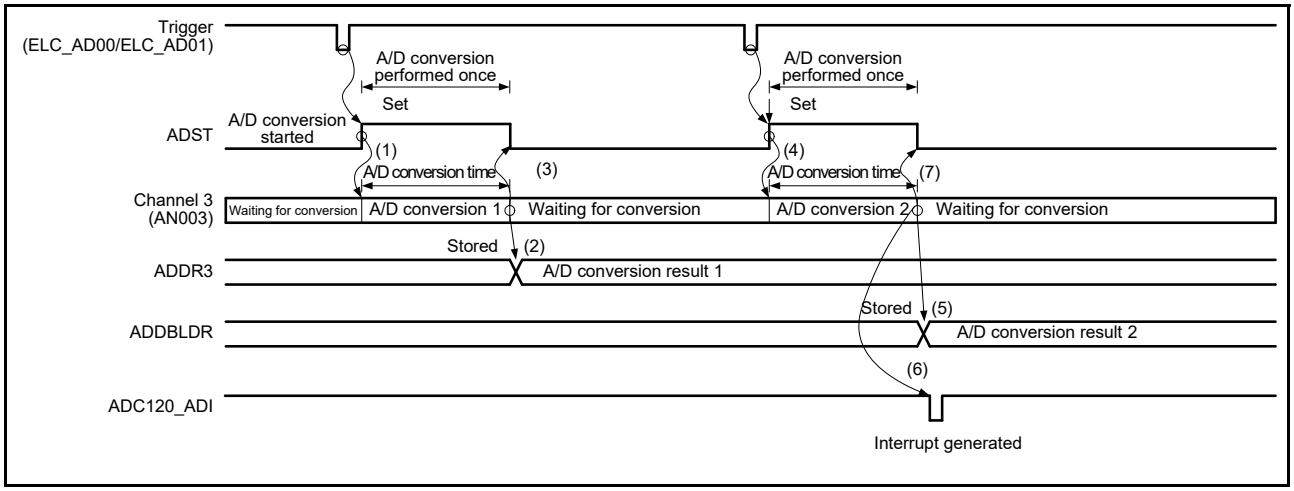


Figure 35.14 Example of operation in single scan mode when double trigger mode is selected and AN003 is duplicated

35.3.2.9 Extended operations when double trigger mode is selected

When double trigger mode is selected in single scan mode, and a synchronous trigger (ELC_AD00/ELC_AD01 (unit 0), ELC_AD10/ELC_AD11 (unit 1)) is selected as the trigger for the start of A/D conversion, two rounds of single scan operation are performed.

Deselect self-diagnosis, and set the addition/average mode select bits for both temperature sensor output (ADEXICR.TSSA and ADEXICR.TSSB) and internal reference voltage (ADEXICR.OCSA and ADEXICR.OCSB) to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits, and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In extended double trigger mode, select a synchronous trigger (ELC_AD00/ELC_AD01 (unit 0), ELC_AD10/ELC_AD11 (unit 1)) by setting the ADSTRGR.TRSA[5:0] bits to 0Bh, and in ADCSR, set the EXTRG bit to 0 and the TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC_AD00/ELC_AD01 (unit 0), ELC_AD10/ELC_AD11 (unit 1)), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. When A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D data register y (ADDRy) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the trigger of ELC_ADi0 or ELC_ADi1 is input respectively (i = 0, 1).
3. The ADCSR.ADST bit is automatically cleared to 0 and the ADC12 enters a wait state. An ADC12i_ADI (i = 0, 1) interrupt request is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input (ELC_AD00/ELC_AD01 (unit 0), ELC_AD10/ELC_AD11 (unit 1)), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the result is stored in the A/D Data Duplexing Register (ADDBLDR) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the trigger of ELC_ADi0 or ELC_ADi1 is input respectively (i = 0, 1).
6. An ADC12i_ADI (i = 0, 1) interrupt request is generated (without register setting).
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically cleared to 0 when A/D conversion completes. Then, the ADC12 enters a wait state.

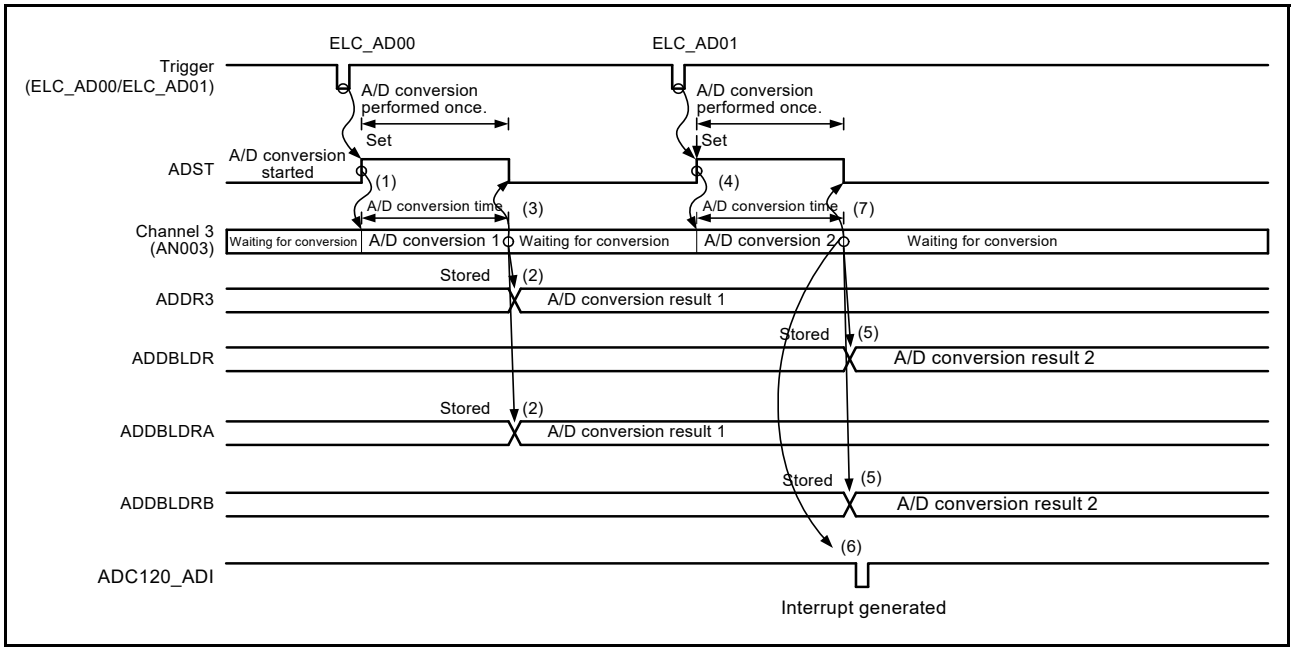


Figure 35.15 Example of extended operation in double trigger mode (1) when duplication is selected for AN003 and ELC_AD00/ELC_AD01 is selected

35.3.3 Continuous Scan Mode

35.3.3.1 Basic operation without channel-dedicated sample-and-hold circuits

In basic operation of continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0,1) interrupt request is generated (without register setting). The ADC12 sequentially starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. The ADCSR.ADST bit is not automatically cleared, and steps 2. and 3. are repeated as long as the bit remains 1 (A/D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
5. When the ADST bit is set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.

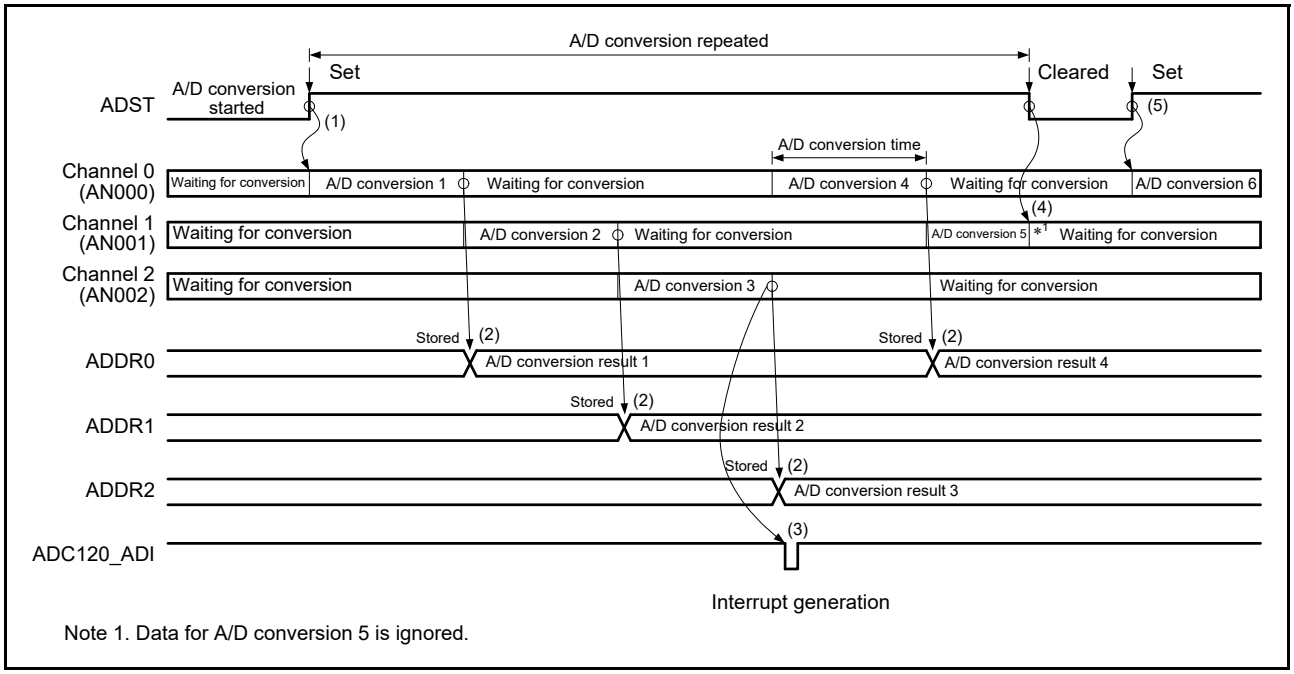


Figure 35.16 Example of basic operation in continuous scan mode when AN000 to AN002 are selected

35.3.3.2 Basic operation with channel-dedicated sample-and-hold circuits and continuous sampling disabled

When the channel-dedicated sample-and-hold circuit is used with continuous sampling disabled, sample-and-hold operation is first performed, and then A/D conversion is repeated on the analog input of all the specified channels. The channels whose dedicated sample-and-hold circuit is to be used can be selected in the SHANS[2:0] bits in ADSHCR.

The operation is as follows:

1. Analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After sample-and-hold operation, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting). At the same time, analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used.
5. The ADST bit is not automatically cleared, and steps 2. to 4. are repeated as long as the bit remains at 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops, and the ADC12 enters a wait state.
6. When the ADST bit is then set to 1 (A/D conversion start), analog input sampling starts again for all channels whose dedicated sample-and-hold circuit is to be used.

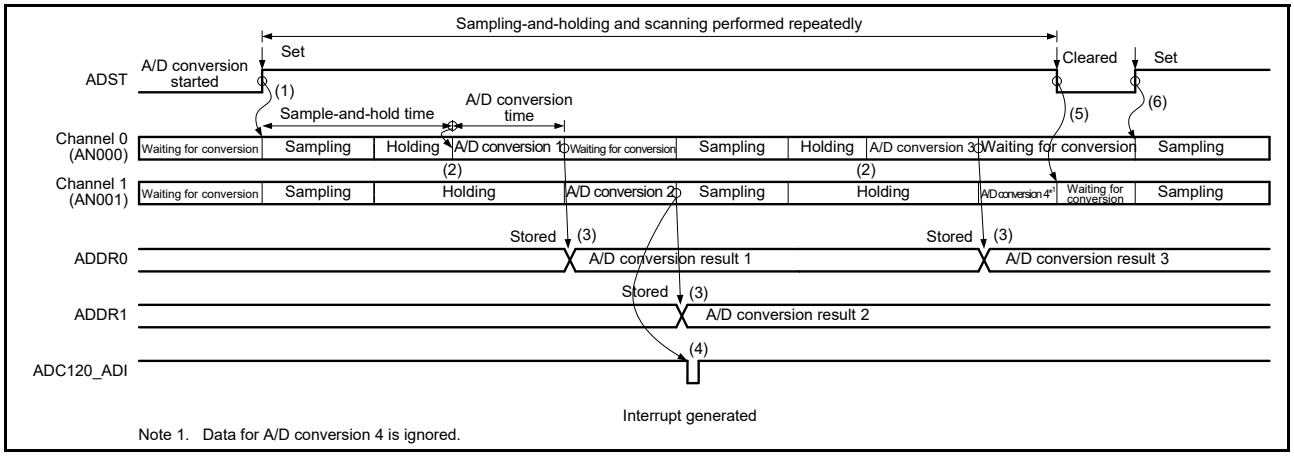


Figure 35.17 Example of operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used and AN000 and AN001 are selected

35.3.3.3 Basic operation with channel-dedicated sample-and-hold circuits and continuous sampling enabled

When a channel-dedicated sample-and-hold circuit is used with continuous sampling enabled, sample-and-hold operations are performed first, after which the analog inputs on all selected channels are A/D-converted as described in this section. The channels for which the channel-dedicated sample-and-hold circuits are to be used can be selected in the ADSHCR.SHANS[2:0] bits.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger. Set the ADCSR.ADST bit to 1 after at least 400 ns (when the permissible signal source impedance is 1 kΩ) elapse after the ADSHMSR.SHMD bit is set to 1.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
5. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (without register setting). Also, analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.
6. The ADCSR.ADST bit is not automatically cleared, and steps 3. to 5. are repeated as long as the bit remains 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
7. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.
8. When the ADSHMSR.SHMD bit is then set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
9. When the ADCSR.ADST bit is then set to 1 (A/D conversion start), analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.

Note: If continuous scanning is performed when only the channels with the sample-and-hold circuits are selected, time for continuous sampling cannot be secured in the second and subsequent continuous scans. When continuous sampling by the channel-dedicated sample-and-hold circuits is enabled for continuous scanning, select one or more channels from AN003 to AN007, AN016 to AN018, AN020, temperature sensor output, and internal reference voltage for unit 0, and AN105 to AN107, AN116, AN117, temperature sensor output, and internal reference voltage for unit 1, and set the continuous sampling time for the sample-and-hold circuits to at least 400 ns (when the permissible signal source impedance is 1 kΩ).

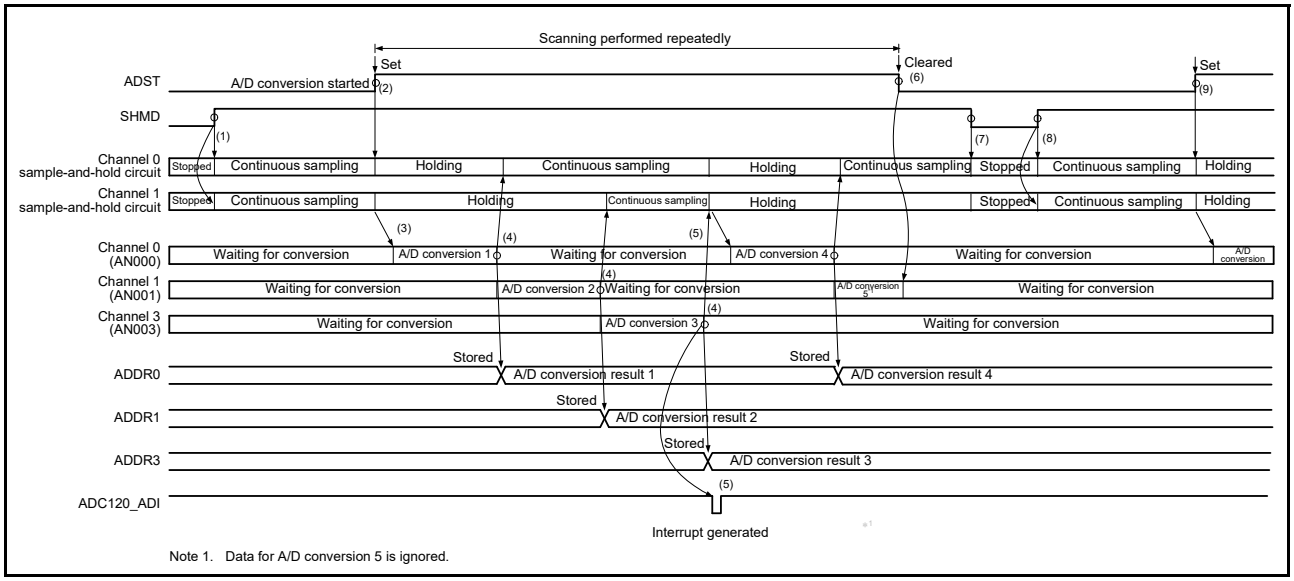


Figure 35.18 Example of operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used, AN000, AN001, and AN003 are selected, and continuous sampling is enabled

35.3.3.4 Channel selection and self-diagnosis without channel-dedicated sample-and-hold circuits

When channels and self-diagnosis are selected at the same time, A/D conversion is first performed for the reference voltage VREFH0 (unit 0) or VREFH (unit 1) (×0, ×1/2, or ×1) supplied to the ADC12, and then A/D conversion is performed on the analog input of the selected channels, this sequence is then repeated.

The operation is as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting). At the same time, the ADC12 starts A/D conversion for self-diagnosis and then starts A/D conversion on ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. The ADST bit is not automatically cleared, and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
6. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then, the ADC12 enters a wait state.

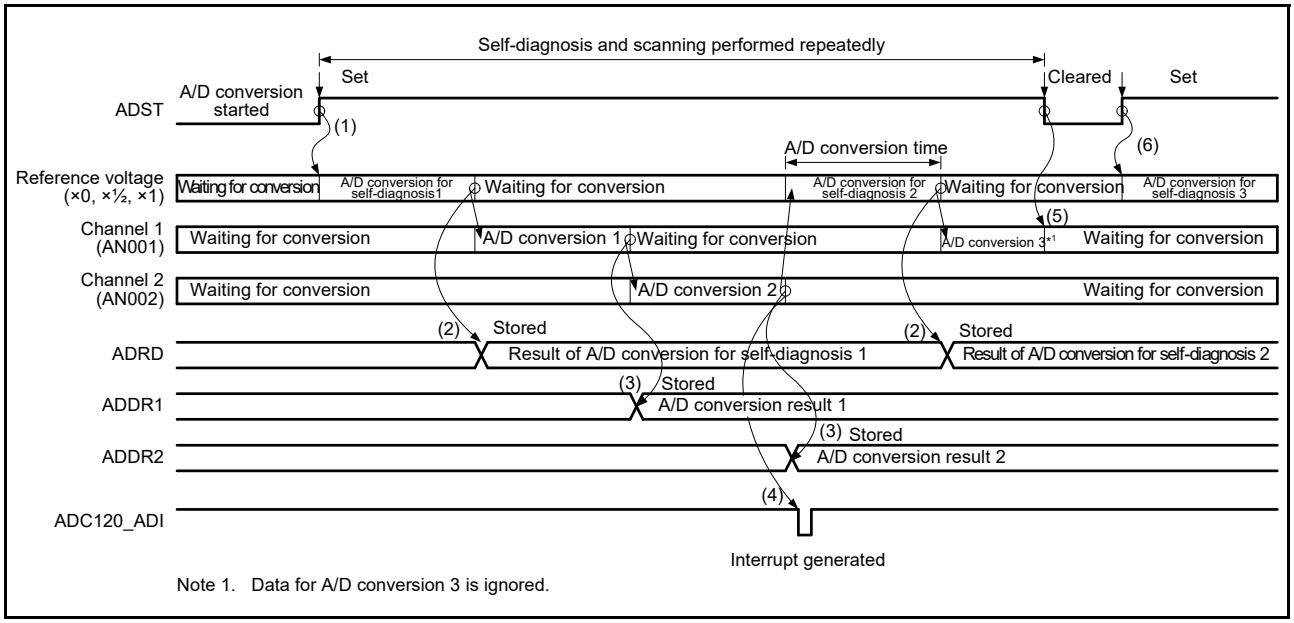


Figure 35.19 Example of basic operation in continuous scan mode when AN001 and AN002 are selected with self-diagnosis

35.3.3.5 Channel selection and self-diagnosis with channel-dedicated sample-and-hold circuits and continuous sampling disabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used with continuous sampling disabled, sample-and- hold operation is first performed, and then A/D conversion is performed for the reference voltage VREFH0 (unit 0) or VREFH (unit 1) (×0, ×1/2, or ×1) supplied to the ADC12. A/D conversion is then performed on the analog input of the selected channels, and this sequence is repeated.

The operation is as follows:

1. Analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After sample-and-hold operation, A/D conversion for self-diagnosis starts.
3. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
5. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting). At the same time, analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used.
6. The ADST bit is not automatically cleared, and steps 2. to 5. are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
7. When the ADST bit is then set to 1 (A/D conversion start), analog input sampling starts again for all channels whose dedicated sample-and-hold circuit is to be used.

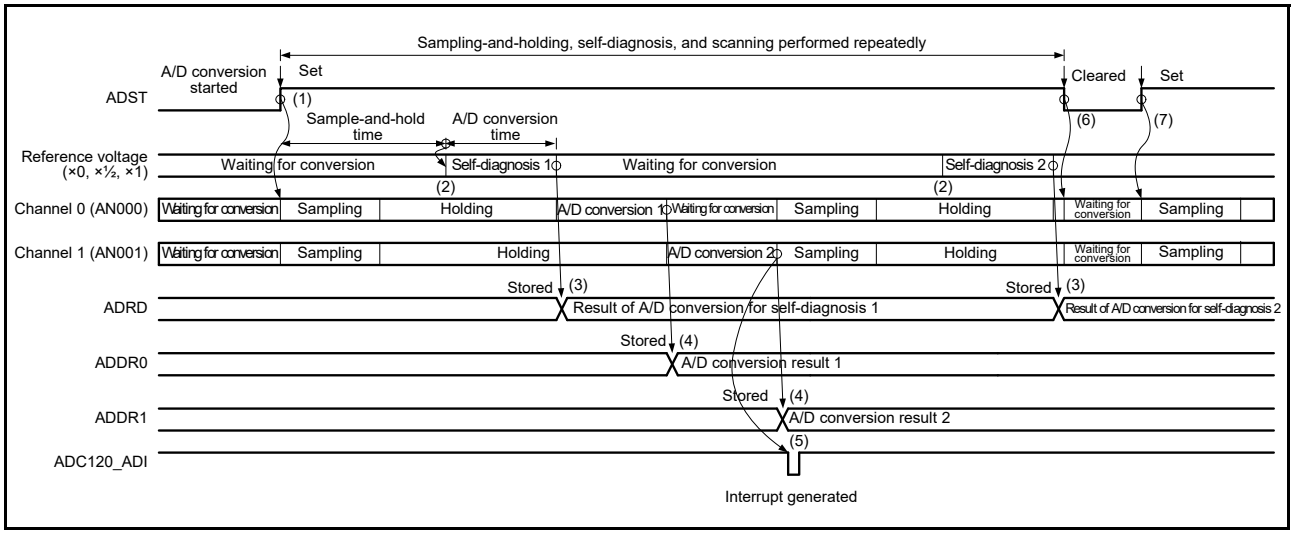


Figure 35.20 Example of operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used, and AN000 and AN001 are selected with self-diagnosis

35.3.3.6 Channel selection and self-diagnosis with channel-dedicated sample-and-hold circuits and continuous sampling enabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used with continuous sampling enabled, sample-and-hold operation is first performed, followed by A/D conversion of the reference voltage VREFH0 (unit 0) or VREFH (unit 1) (×0, ×1/2, or ×1) supplied to the ADC12. A/D conversion is then performed on the analog input of the selected channels, and this sequence is repeated.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger. Set the ADCSR.ADST bit to 1 after at least 400 ns (when the permissible signal source impedance is 1 kΩ) elapse after the ADSHMSR.SHMD bit is set to 1.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion for self-diagnosis starts.
4. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
6. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting). Also, analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.
7. The ADCSR.ADST bit is not automatically cleared, and steps 3. to 6. are repeated as long as the bit remains 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
8. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.
9. When the ADSHMSR.SHMD bit is then set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
10. When the ADCSR.ADST bit is then set to 1 (A/D conversion start), analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.

Note: If continuous scanning is performed when only the channels with the sample-and-hold circuits are selected, time for continuous sampling cannot be secured in the second and subsequent continuous scans. When continuous sampling by the channel-dedicated sample-and-hold circuits is enabled for continuous scanning, select one or more channels from AN003 to AN007, AN016 to AN018, AN020, temperature sensor output, and internal reference voltage for unit 0, and AN105 to AN107, AN116, AN117, temperature sensor output, and internal reference voltage for unit 1, and set the continuous sampling time for the sample-and-hold circuits to at least 400 ns (when the permissible signal source impedance is 1 kΩ).

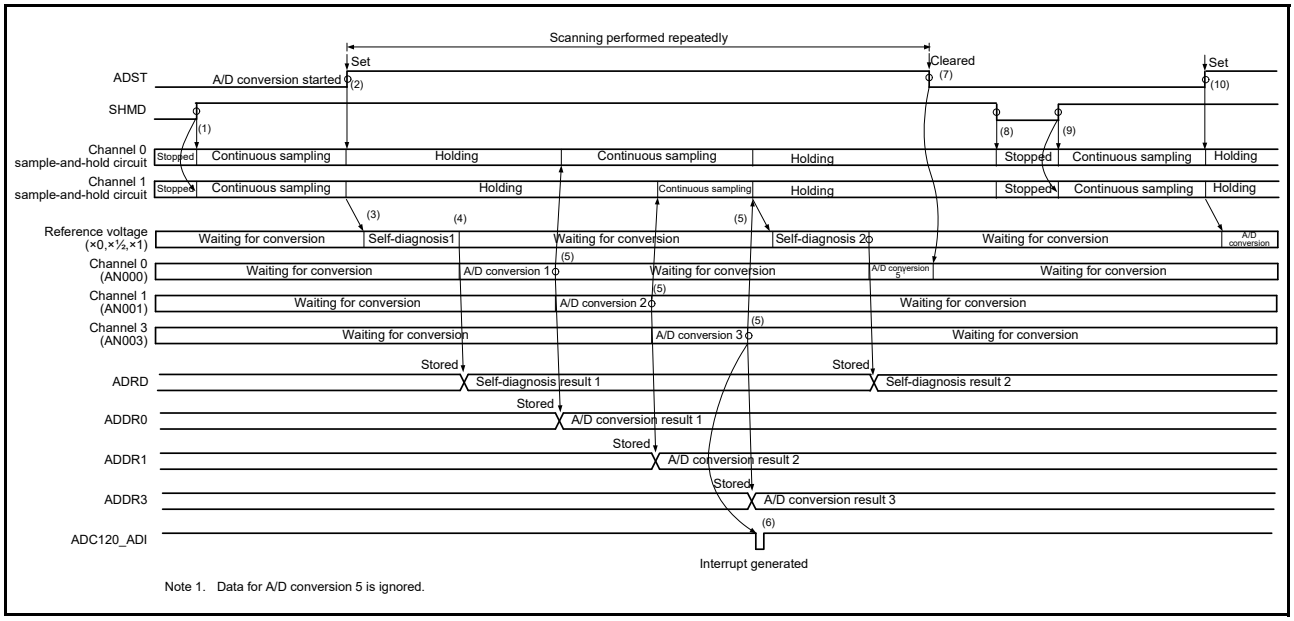


Figure 35.21 Example of operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used, AN000, AN001, and AN003 are selected with self-diagnosis, and continuous sampling is enabled

35.3.3.7 A/D conversion of temperature sensor output or internal reference voltage

When the channels and temperature sensor output or internal reference voltage are selected at the same time, A/D conversion is first performed on the analog input of the selected channels, and then A/D conversion of the temperature sensor output or internal reference voltage is repeated. When both temperature sensor output and internal reference voltage are selected, A/D conversion of the temperature sensor output and internal reference voltage is performed, in that order.

With the channels deselected, selecting only the temperature sensor output or internal reference voltage is also possible.

The operation is as follows:

1. When a software trigger, synchronous trigger (ELC), or asynchronous trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. On completion of A/D conversion on the channels, the result is stored in the associated A/D Data Register y (ADDRy), and then A/D conversion of the temperature sensor output starts.
3. On completion of A/D conversion of the temperature sensor output, the result is stored in the associated A/D Temperature Sensor Data Register (ADTSDR), and then A/D conversion of the internal reference voltage starts.
4. On completion of A/D conversion of the internal reference voltage, the result is stored in the associated A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC12i_ADI interrupt request is generated. In addition, the ADC12 continuously starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the lowest number n.
5. The ADCSR.ADST bit is not cleared automatically, and steps 2. to 4. are repeated as long as this bit remains set to 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a

wait state.

6. When the ADCSR.ADST bit is then set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the lowest number n.

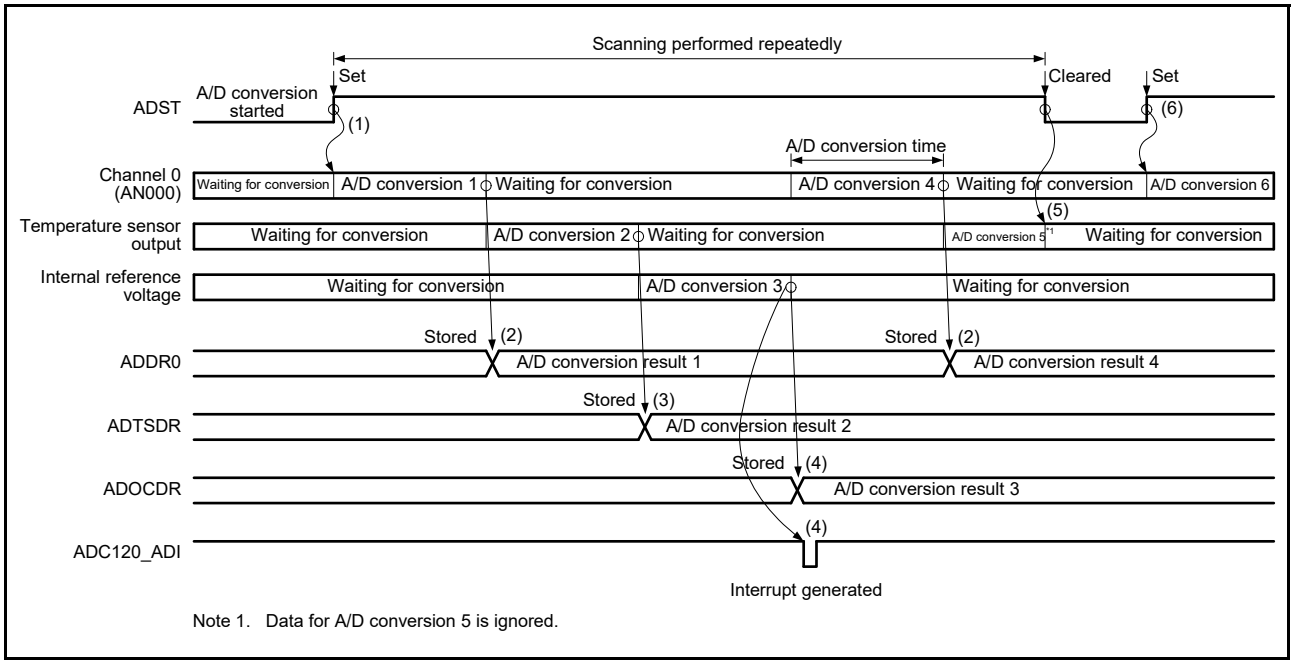


Figure 35.22 Example of basic operation in continuous scan mode when AN000 and temperature sensor output or internal reference voltage are selected

35.3.4 Group Scan Mode

35.3.4.1 Basic operation

In group scan mode, A/D conversion is performed once on the analog inputs of all the specified channels in group A and group B after scanning is started by a synchronous trigger (ELC). The scan operation of each group is similar to the scan operation in single scan mode.

The synchronous triggers can be selected in the ADSTRGR.TRSA[5:0] bits for group A and in the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for group A and group B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger.

The group A channels to be A/D-converted are selected using the ADANSA0 and ADANSA1 registers and the ADEXICR.TSSA and OCSA bits, while the group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers and the ADEXICR.TSSB and OCSB bits. Group A and group B cannot use the same channels.

When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for group A and group B.

The following example describes operation in group scan mode using a synchronous trigger from the ELC. In this example, the ELC_AD00 and ELC_AD01 (unit 0), and ELC_AD10 and ELC_AD11 (unit 1) triggers from the ELC are used to start conversion of group A and group B, respectively. Also, ELC_AD00 and ELC_AD01 (unit 0), and ELC_AD10 and ELC_AD11 (unit 1) are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group A is started by ELC_AD00 (unit 0) or ELC_AD10 (unit 1).
2. When group A scanning completes, an ADC12i_ADI (i = 0, 1) interrupt is generated (no register setting).
3. Scanning of group B is started by ELC_AD01 (unit 0) or ELC_AD11 (unit 1).
4. When group B scanning completes, an ADC12i_GBADI interrupt is generated if the ADCSR.GBADIE bit is 1 (ADC12i_GBADI interrupt when scanning completion is enabled).

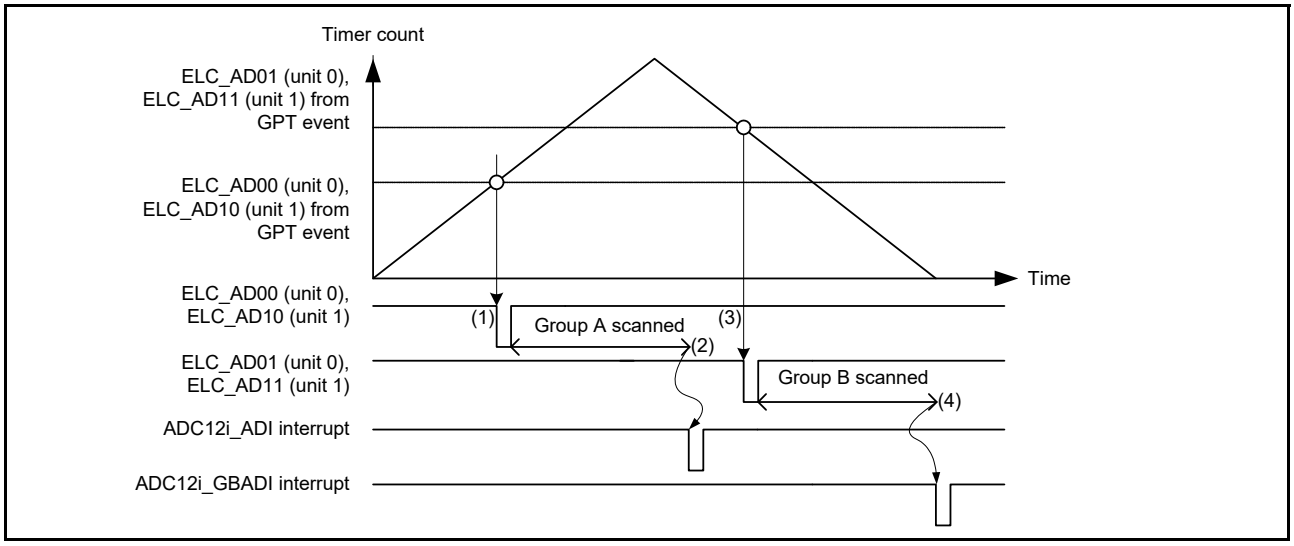


Figure 35.23 Example of basic operation in group scan mode when synchronous triggers from the ELC are used

35.3.4.2 A/D conversion in double trigger mode

When double trigger mode is selected in group scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed as a sequence for group A. For group B, single scan operation started by a synchronous trigger (ELC) is performed once.

In group scan mode, the synchronous triggers can be selected in the TRSA[5:0] bits in ADSTRGR for group A and in the TRSB[5:0] bits in ADSTRGR for group B. Use different triggers for group A and group B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger or an asynchronous trigger (ADTRGn).

When ELC_AD00/ELC_AD01 (unit 0), ELC_AD10/ELC_AD11 (unit 1) is selected as the group A synchronous triggers by setting the ADSTRGR.TRSA[5:0] bits to 0Bh, operation proceeds in extended double trigger mode.

The channels to be A/D-converted are selected in the DBLANS[4:0] bits in the ADCSR register for group A and in the ADANSB0 and ADANSB1 registers for group B. The same channels cannot be selected for both groups.

When double trigger mode is selected in group scan mode, set the A/D conversion select bits for both the temperature sensor output (ADEXICR.TSSA) and the internal reference voltage (ADEXICR.OCSA) to 0 (deselected). Self-diagnosis cannot be selected when double trigger mode is selected in group scan mode.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the DBLE bit in ADCSR to 1.

The following describes operation in group scan mode with double trigger mode using a synchronous trigger from the ELC. In this example, the ELC_AD00 and ELC_AD01 (unit 0), ELC_AD10 and ELC_AD11 (unit 1) triggers from the ELC are used to start conversion of group A and group B, respectively. Also, ELC_AD00 and ELC_AD01 (unit 0), ELC_AD10 and ELC_AD11 (unit 1) are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group B is started by the ELC_AD00 (unit 0) or ELC_AD10 (unit 1) trigger from the ELC.
2. When group B scanning completes, an ADC12i_GBADI (i = 0, 1) interrupt is generated if the GBADIE bit in ADCSR is 1 (ADC12i_GBADI interrupt when scanning completion is enabled).
3. The first scan of group A is started by the first ELC_AD01 (unit 0) or ELC_AD11 (unit 1) trigger.
4. When the first scan of group A completes, the conversion result is stored in the associated A/D Data Register y (ADDRy), an ADC12i_ADI interrupt request is not generated.
5. The second scan of group A is started by the second ELC_AD01 (unit 0) or ELC_AD11 (unit 1) trigger.
6. When the second scan of group A completes, the conversion result is stored in ADDBLDR. An ADC12i_ADI interrupt is generated.

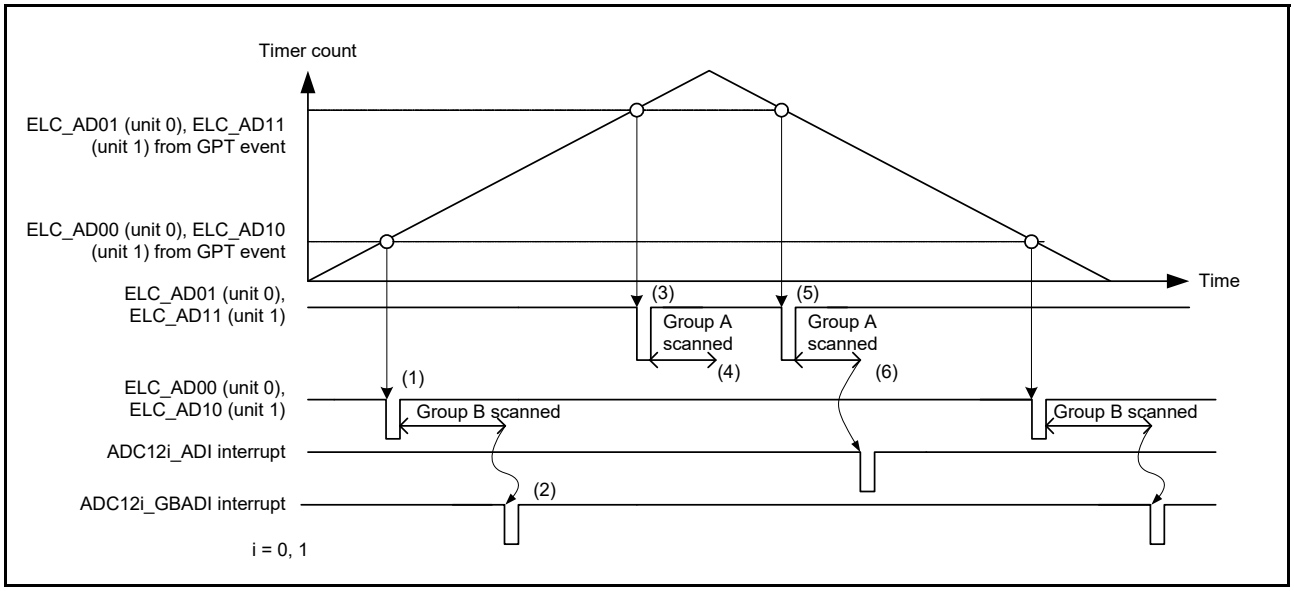


Figure 35.24 Example of basic operation in group scan mode with double trigger mode when synchronous triggers from the ELC are used

35.3.4.3 Operation with group A priority control

Setting the ADGSPCR.PGS bit to 1 in group scan mode enables operation to proceed under group A priority control. When setting the PGS bit in the ADGSPCR register to 1, follow the procedure shown in Figure 35.25. If the procedure is not followed, A/D conversion operation and stored data are not guaranteed.

In basic group scan mode, while A/D conversion is underway for group A or group B, input of the trigger for A/D conversion for the other group is ignored. Under group A priority control, if a group A trigger is input during A/D conversion for group B, A/D conversion for group B is discontinued and A/D conversion for group A proceeds. If the setting in the ADGSPCR.GBRSCN bit is 0, the ADC12 enters wait state on completion of the A/D conversion for group A. If the setting in the ADGSPCR.GBRSCN bit is 1, the ADC12 automatically restarts scanning for group B from the head of the group after completion of the A/D conversion for group A. Table 35.9 summarizes operations in response to the input of a trigger during A/D conversion with the settings in the ADGSPCR.GBRSCN bit.

Scan operations in group A or group B are the same in single scan mode. Additionally, single scanning for group B is continuously operated if the ADGSPCR.GBRP bit is set to 1.

For the trigger settings in group scan mode, select a synchronous trigger for group A using the ADSTRGR.TRSA[5:0] bits, and select a synchronous trigger for group B, different from that of group A, using the ADSTRGR.TRSB[5:0] bits. Set the ADSTRGR.TRSB[5:0] bits to 3Fh when setting the ADGSPCR.GBRP bit to 1.

Additionally, as targets for A/D conversion, select channels for group A using the ADANSA0 and ADANSA1 registers and the ADEXICR.TSSA and OCSA bits, and for group B, select channels different from those for group A using the ADANSB0 and ADANSB1 registers, and the ADEXICR.TSSB and OCSB bits.

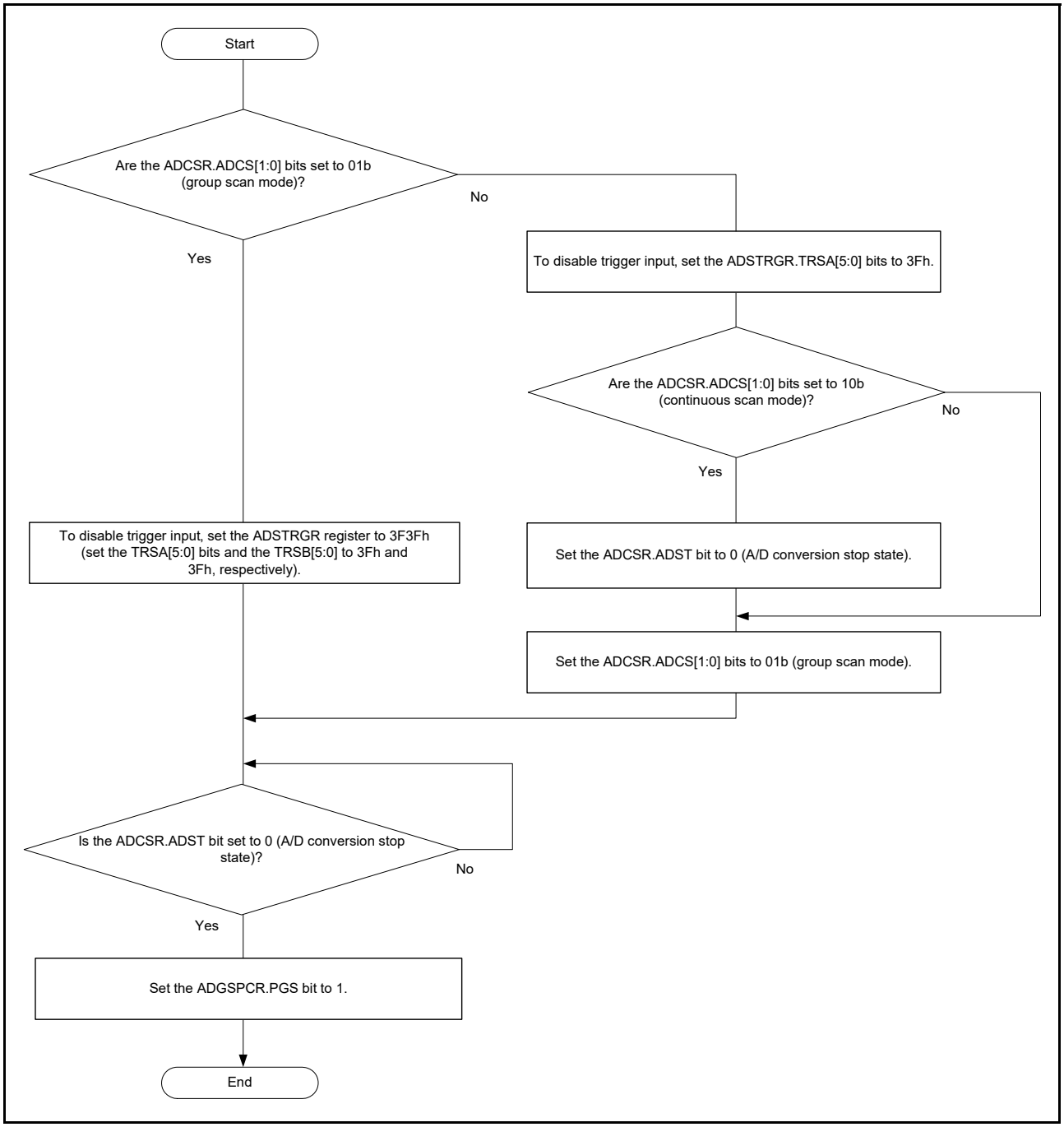


Figure 35.25 Flow for ADGSPCR.PGS bit setting

Table 35.9 Control of A/D conversion operations based on the ADGSPCR.GBRSCN bit settings

A/D conversion operation	Trigger input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group A is in progress	Input of group A trigger	Trigger input is invalid	Trigger input is invalid
	Input of group B trigger	Trigger input is invalid	Group B is converted after group A conversion completes
When A/D conversion for group B is in progress	Input of group A trigger	Group B conversion stops and group A conversion starts	• Group B conversion stops and group A conversion starts • Group B Conversion starts after group A conversion completes
	Input of group B trigger	Trigger input is invalid	Trigger input is invalid

The following example describes the operations in group scan mode under group A priority control (ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

The operation is as follows:

1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion, the result is stored in the associated A/D Data Register y (ADDRy).
3. When a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remaining 1, A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n. If A/D conversion is not complete when the AD conversion of group B is interrupted, A/D conversion result is not stored in the A/D Data Register (ADDRy).
4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
5. An ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
6. A/D conversion for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers restarts in order from the channel with the smallest number n with the ADCSR.ADST bit remaining 1.
7. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
8. An ADC12i_GBADI interrupt request is generated if the setting in the ADCSR.GBADIE bit is 1 (ADC12i_GBADI interrupt when group B scanning completion is enabled).
9. The ADCSR.ADST bit is automatically cleared, and the ADC12 enters the wait state when A/D conversion is completed.

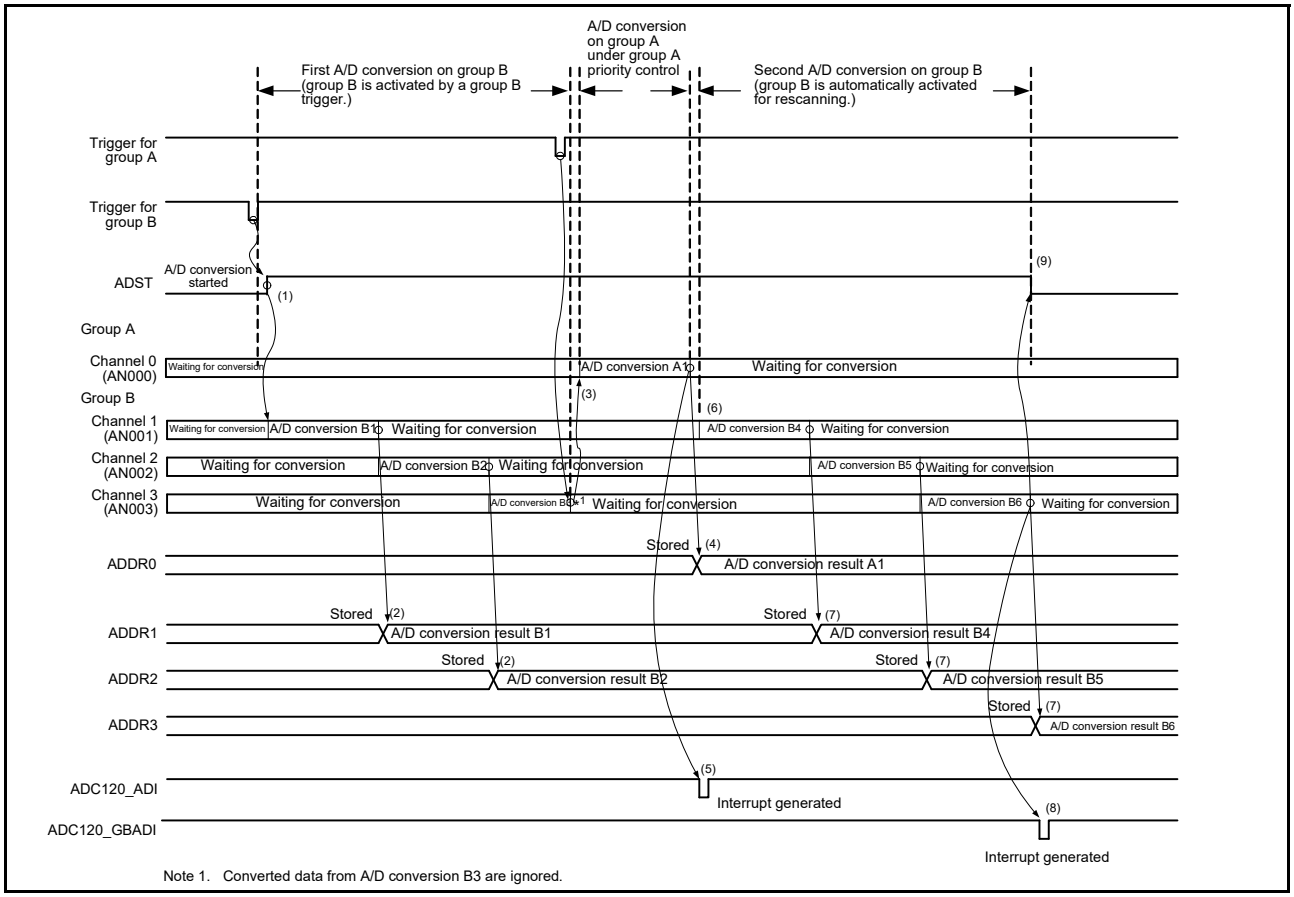


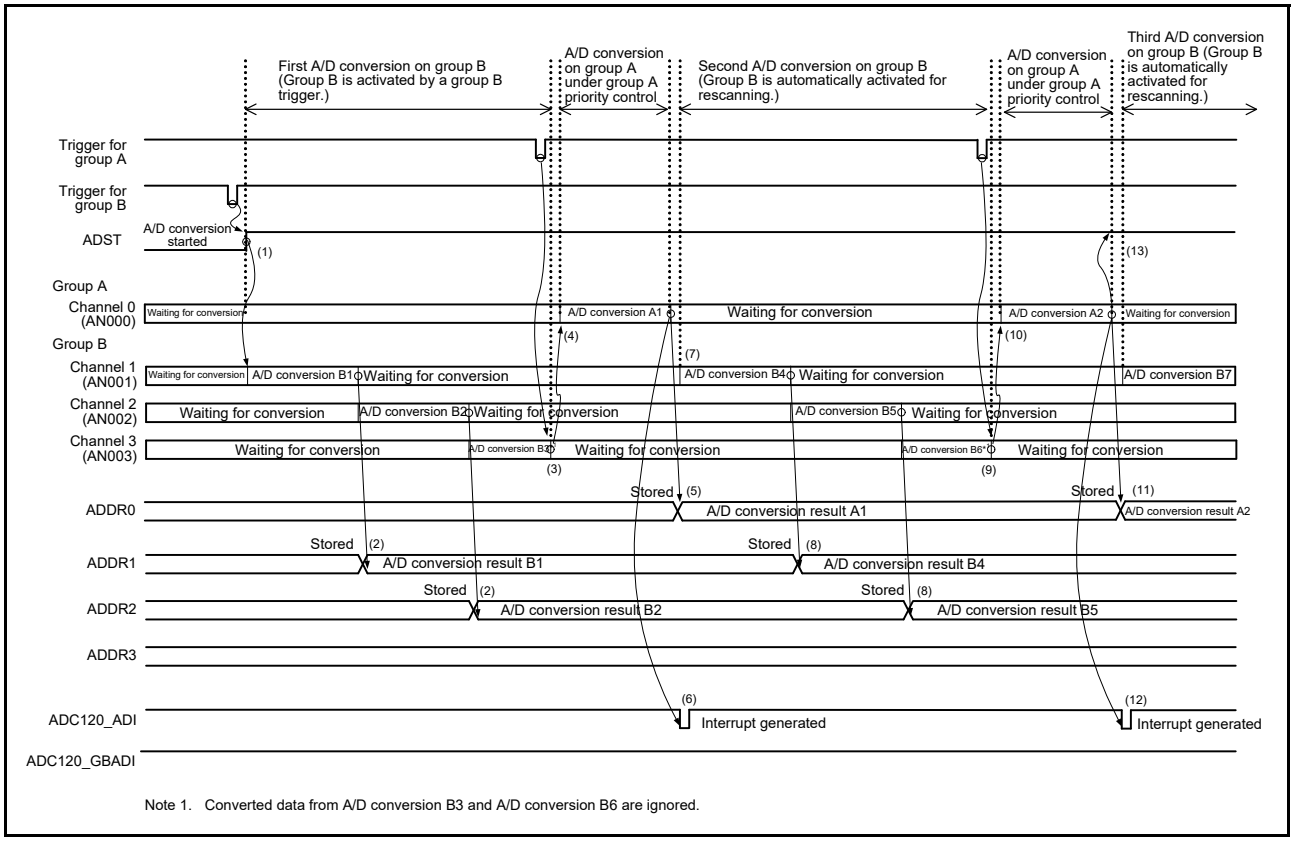
Figure 35.26 Example of operation with group A priority control (1), when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

This section provides an example of operation when a group A trigger is input again during rescanning operation on group B. In this example, channel 0 is selected for group A and channels 1 to 3 are selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0).

The operation is as follows:

1. When a group B trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. When a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remaining 1. If A/D conversion is not complete when the AD conversion of group B is interrupted, A/D conversion result is not stored in the A/D Data Register (ADDRy).
4. The A/D conversion for the ANn group A channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
5. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
6. An ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
7. If the ADGSPCR.GBRSCN bit is 1, when the A/D conversion of group A is complete, the ADCSR.ADST bit remains 1 and the group B is rescanned. A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers starts again in order from the channel with the smallest number n.
8. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).

9. If a group A trigger is input during A/D conversion on group B for rescanning, the ADCSR.ADST bit remains 1 and the ongoing A/D conversion on group B is discontinued.
10. The A/D conversion for the ANn group A channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
11. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
12. An ADC12i_ADI interrupt request is generated (no register setting).
13. If the ADGSPCR.GBRSCN bit is 1, when the A/D conversion of group A is complete, the ADCSR.ADST bit remains 1 and the group B is rescanned. A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers starts again in order from the channel with the smallest number n.
14. If a group A trigger is input during A/D conversion on group B for rescanning, steps 9. to 13. are repeated. If a group A trigger is not input, the ADCSR.ADST bit is cleared automatically on completion of A/D conversion on group B, and the ADC12 enters a wait state.



Note 1. Converted data from A/D conversion B3 and A/D conversion B6 are ignored.

Figure 35.27 Example of operation with group A priority control (2), when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

The following sequence is an example of a rescanning operation in which a group B trigger is input during A/D conversion on group A. In this example, channels 1 to 3 are selected for group A and channel 0 is selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0):

1. When input of a trigger for group A sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. If a group B trigger is input during A/D conversion on group A, A/D conversion on group B can be performed after the A/D conversion on group A completes. However, if group A triggers are input continuously, the scan operation on group B is canceled by group A and is not performed.

4. On completion of the A/D conversion on group A, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
5. On completion of the group A conversion, the ADCSR.ADST bit remains 1 and the group B is rescanned. Next, A/D conversion for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
6. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
7. On completion of the rescanning operation on group B, an ADC12i_GBADI interrupt request is generated if the setting in the ADCSR.GBADIE bit is 1 (ADC12i_GBADI interrupt when scanning completion is enabled).
8. The ADCSR.ADST bit is automatically cleared and the ADC12 enters the wait state when A/D conversion is complete.

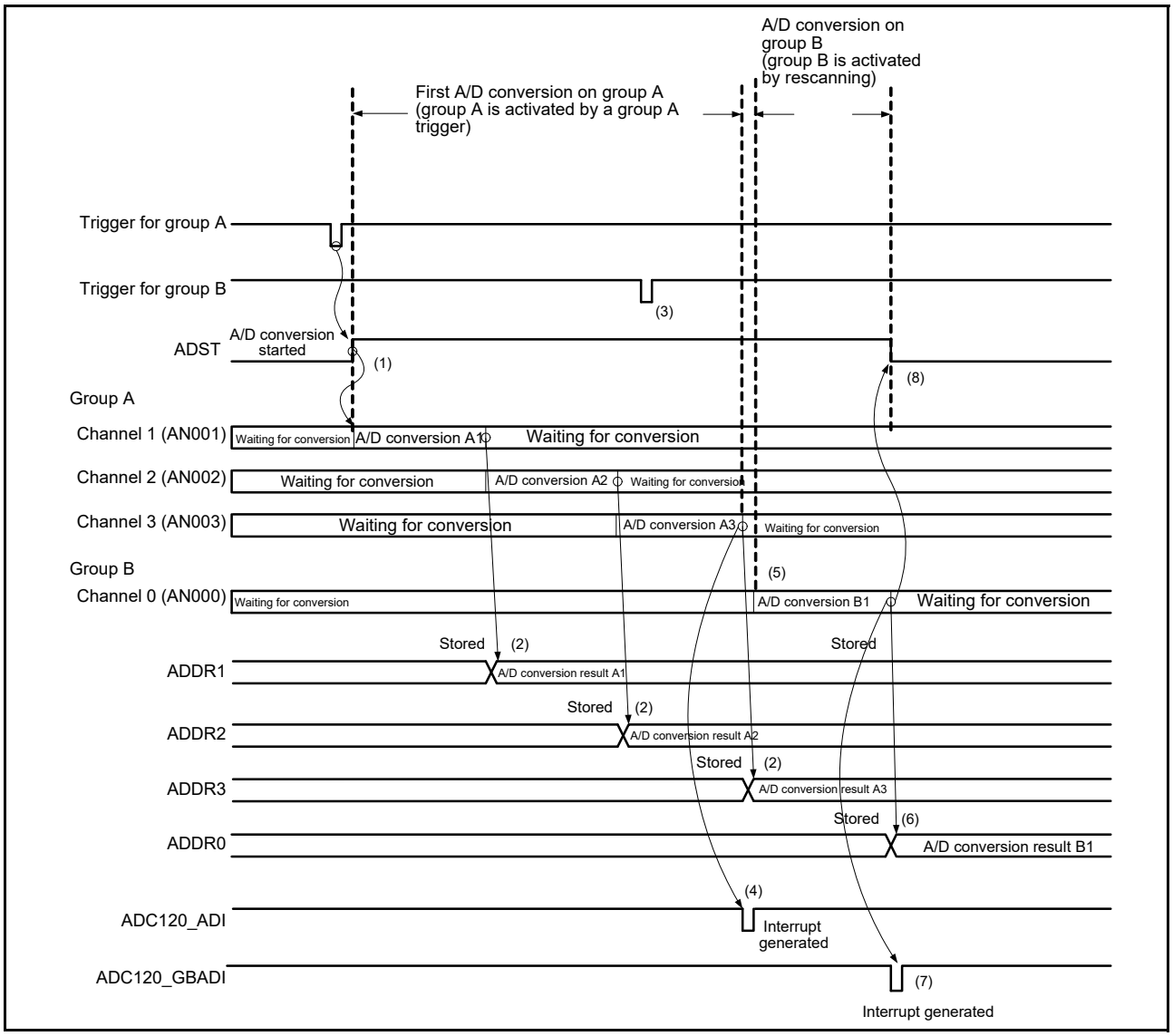


Figure 35.28 Example of operation with group A priority control (3), when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

The following sequence is an example of operation under group A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0):

1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.

2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. If a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remaining 1, A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
5. An ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
6. The ADCSR.ADST bit is automatically cleared and ADC12 enters the wait state when A/D conversion is complete.

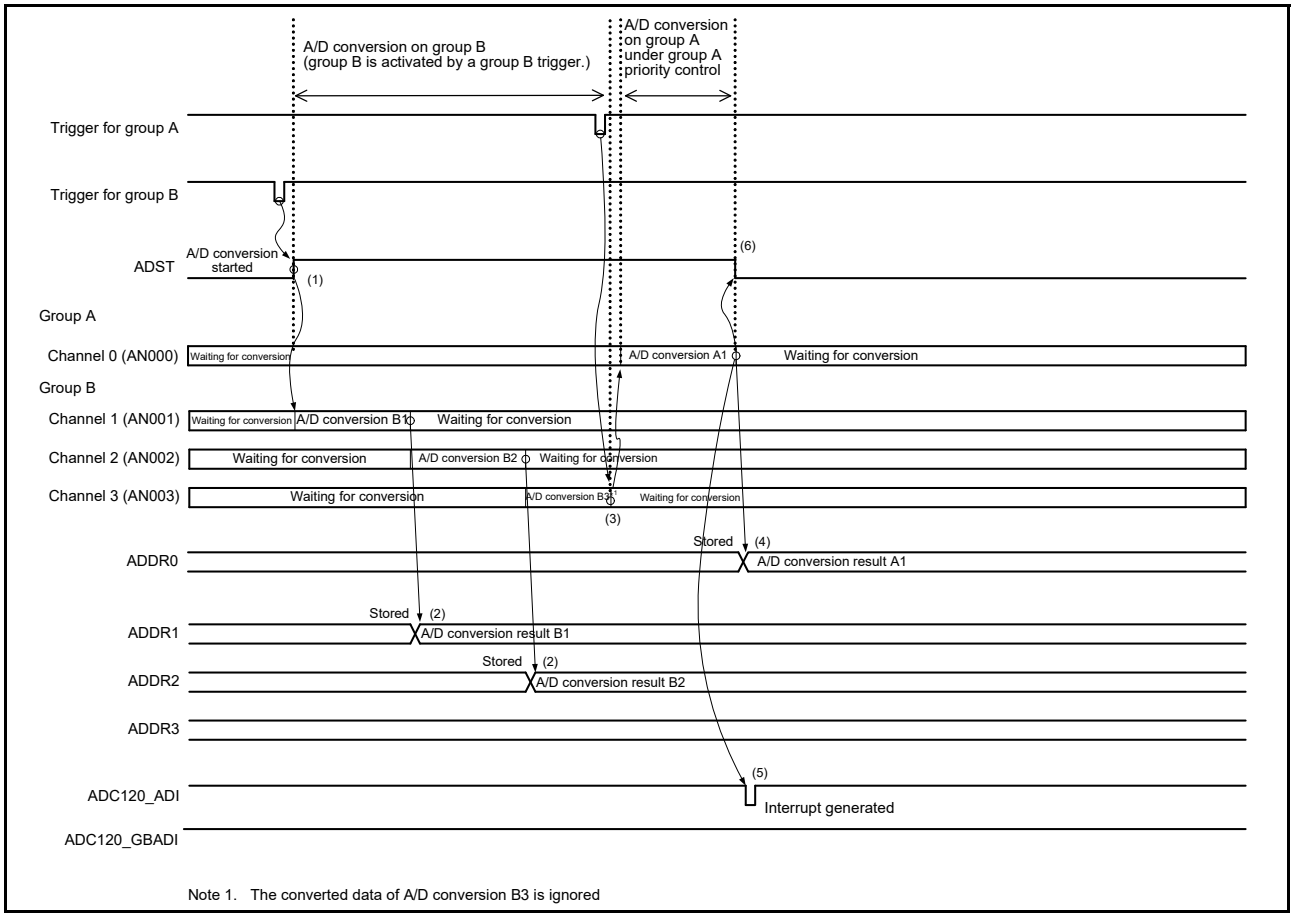


Figure 35.29 Example of operation with group A priority control (4), when ADGSPCR.GBRSCN = 0 and ADGSPCR.GBRP = 0

The following sequence is an example of operation under group A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSPCR.GBRP = 1):

1. The ADCSR.ADST bit is set to 1 (A/D conversion start) when ADGSPCR.GBRP is set to 1, and conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. If a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remaining 1, A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).

5. An ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
6. A/D conversion for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers restarts in order from the channel with the smallest number n, with the ADCSR.ADST bit remaining 1.
7. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
8. An ADC12i_GBADI interrupt request is generated if the setting in the ADCSR.GBADIE bit is 1.
9. A/D conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n. Steps 6. to 9. are repeated as long as the ADGSPCR.GBRP bit remains 1. Clearing of the ADCSR.ADST bit to 0 is prohibited while the ADGSPCR.GBRP bit is set to 1. Follow the procedure shown in Figure 35.40 for clearing the ADCSR.ADST bit operation through software, to force A/D conversion to stop while ADGSPCR.GBRP = 1.

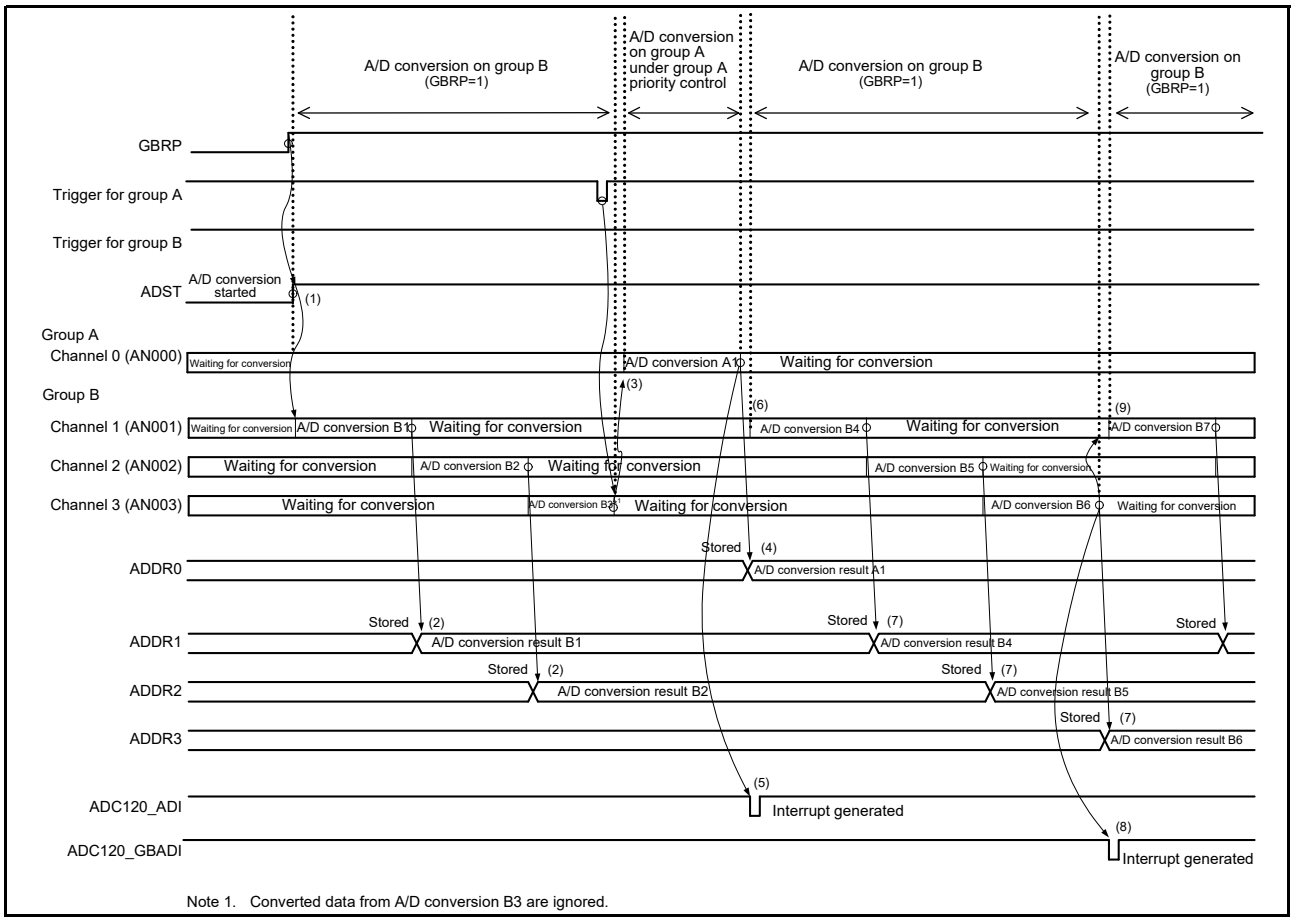


Figure 35.30 Example of operation with group A priority control (5), when ADGSPCR.GBRP = 1

35.3.5 Compare Function for Windows A and B

35.3.5.1 Compare function

The compare function compares a reference value with the A/D conversion result. The reference value can be set for window A and window B independently. When the compare function is in use, the self-diagnosis function and double trigger mode cannot be used. The main differences between window A and window B are their different interrupt output signals and the constraint on window B of only one selectable channel.

The following sequence is an example of operation that combines continuous scan mode and the compare function:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, a synchronous trigger (ELC) or an asynchronous trigger, A/D conversion starts for the selected channels, temperature sensor, and internal reference voltage.

2. On completion of A/D conversion, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy, ADTSDR, or ADOCDR). When ADCMPCR.CMPAE = 1, if bits in the ADCMPANSRy register or the ADCMPANSER register are set for window A, the A/D conversion result is compared with the set ADCMPDR0/1 register value. When ADCMPCR.CMPBE = 1, if bits in the ADCMPBNSR register are set for window B, the A/D conversion result is compared with the ADWINULB/ADWINLLB register setting.
3. As a result of the comparison, when window A meets the condition set in ADCMPLR0/1 or ADCMPLER, the Compare Window A Flag (ADCMPSR0.CMPSTCHA0n, ADCMPSR1.CMPSTCHA1n, ADCMPSER.CMPSTTSA, or ADCMPSER.CMPSTOCA) is set to 1. At this time, if the ADCMPCR.CMPAIE bit is 1, an ADC12i_CMPAI (i = 0, 1) interrupt request is generated. In the same way, when window B meets the condition set in ADCMPBNSR.CMPLB, the Compare Window B Flag (ADCMPBSR.CMPSTB) is set to 1. At this time, if the ADCMPCR.CMPBIE bit is 1, an ADC12i_CMPBI interrupt request is generated.
4. On completion of all selected A/D conversions and comparisons, scan restarts.
5. After the ADC12i_CMPAI and ADC12i_CMPBI interrupts are accepted, the ADCSR.ADST bit is set to 0 (A/D conversion stop) and processing is performed for channels for which the compare flag is set to 1.
6. When all compare flags of window A are cleared, the ADC12i_CMPAI interrupt request is canceled. Similarly, when all compare flags of window B are cleared, the ADC12i_CMPBI interrupt request is reset. To perform comparison again, restart the A/D conversion.

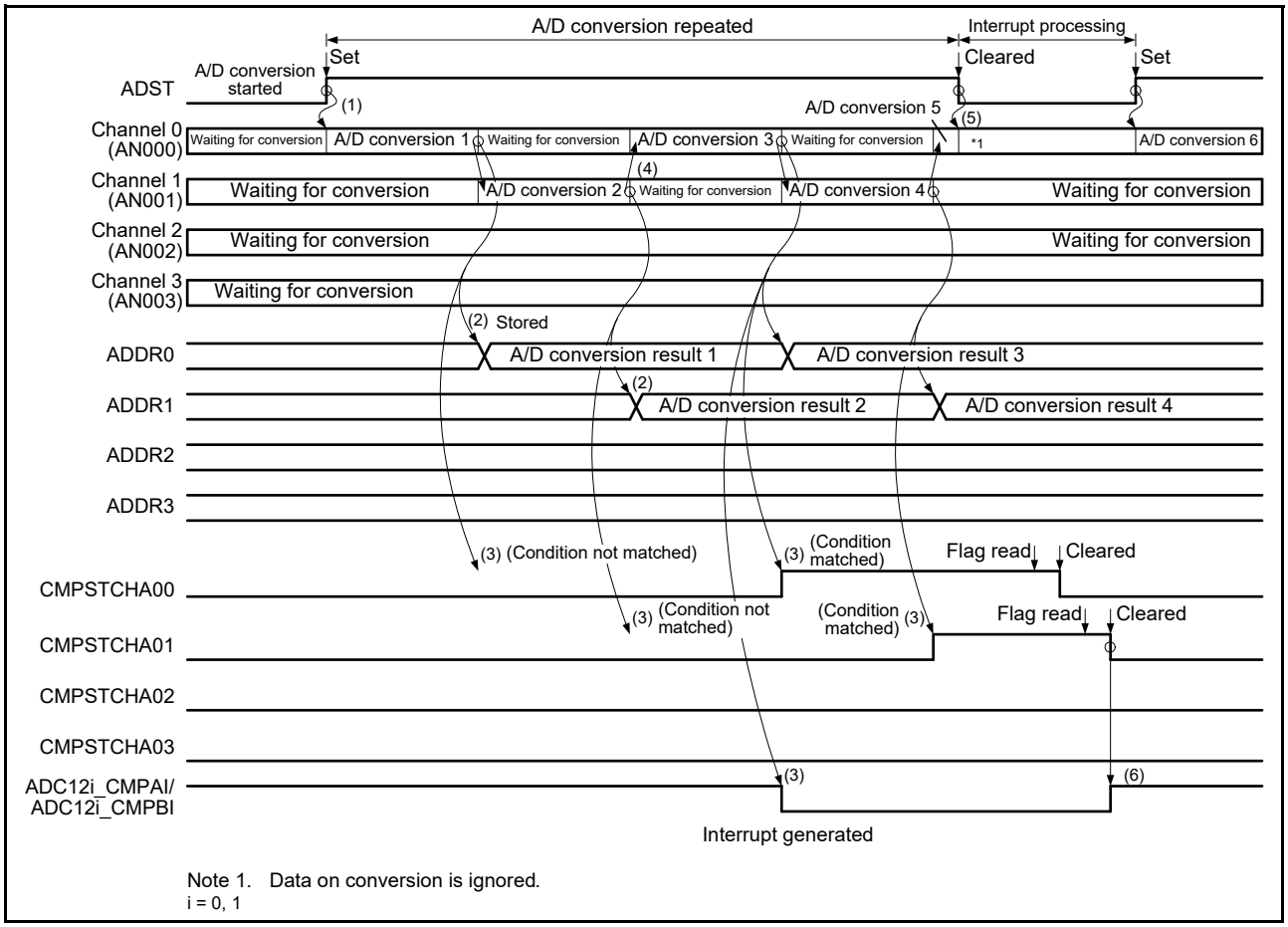


Figure 35.31 Example of compare function operation, when AN000 to AN003 are compared

35.3.5.2 Event output of compare function

Event output of the compare function specifies the upper reference voltage value for window A and the lower reference voltage value for window B, compares the A/D-converted value of the selected channel with the upper and lower reference voltage values, and then outputs the ADC12i_WCMPM and ADC12i_WCMPUM (i = 0, 1) events based on the event conditions (A OR B, A AND B, A XOR B) and comparison results of window A and window B.

If more than one channel is selected for window A, and even one channel in window A meets the comparison condition, the comparison result of window A is met. When using this function, perform A/D conversion in single scan mode. Any channels from AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020 (unit 0), and AN100 to AN102, AN105 to AN107, AN116, AN117 (unit 1), internal reference voltage, and temperature sensor output are selectable for window A.

The following sequence is an example of how to set up and use the event output of the compare function:

1. Confirm that the value in the ADCSR.ADCS bits is 00b (single scan mode).
2. Select the channel for window A in ADCMPANSR0/1 and ADCMPANSER. Set window comparison conditions in the ADCMPLR0/1 and ADCMPLER registers. Set the upper and lower reference values in the ADCMPDR0 and ADCMPDR1 registers.
3. Select the channel and comparison conditions for window B in the ADCMPBNSR register, and set the upper and lower reference values in the ADWINULB and ADWINLLB registers.
4. Set composite conditions for window A/B, window A/B operation enable, and interrupt output enable in ADCMPCR.

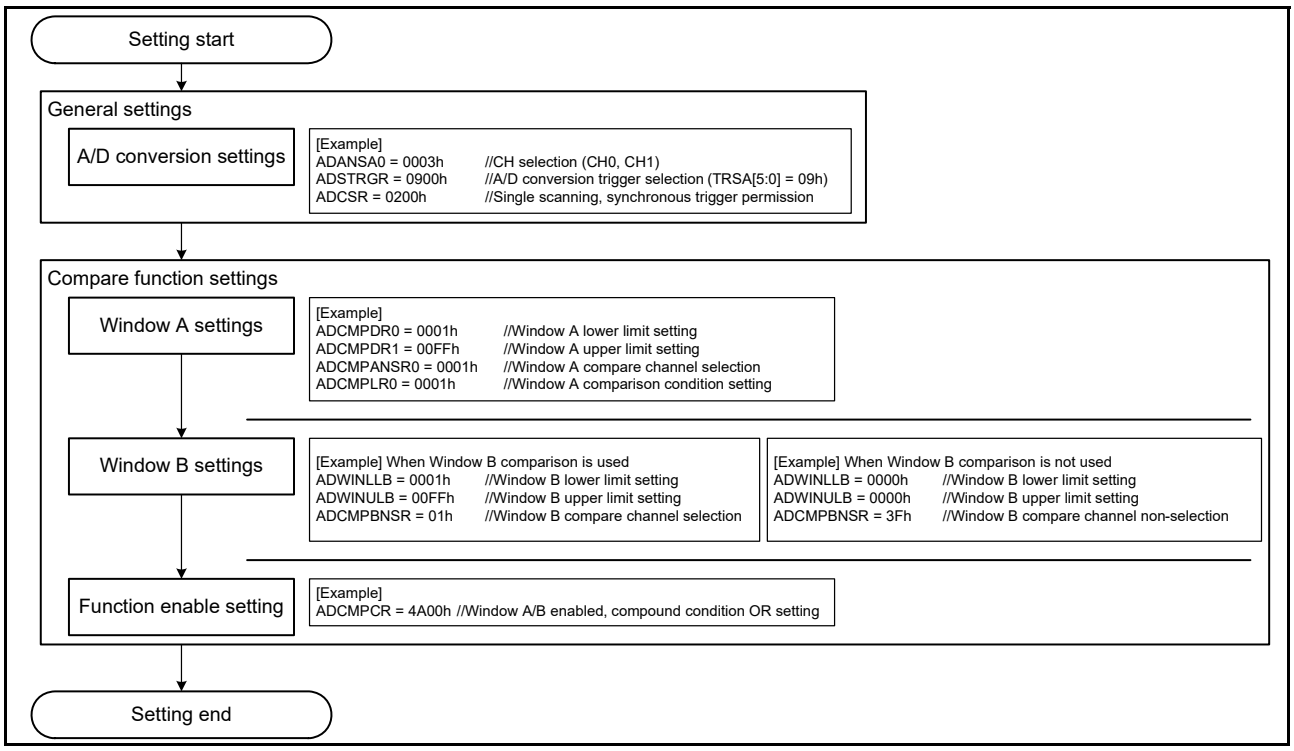


Figure 35.32 Setting example when using the event output of the compare function

Notes on the event output usage when using only window A for the compare function:

- Enable both window A and window B (ADCMPCR.CMPAE = 1, ADCMPCR.CMPBE = 1)
- Set the compound condition of window A and window B to "OR condition" (ADCMPCR.CMPAB[1:0] = 00b)
- Set the compared channel of window B to "Do not select" (ADCMPBNSR.CMPCHB[5:0] = 111111b)
- Set the compare condition of window B to "0 < results < 0 always means mismatch" (ADCMPCR.WCMPE = 1, ADWINLLB.CMPLLB[15:0] = ADWINULB.CMPULB[15:0] = 0000h, and ADCMPBNSR.CMPLB = 1).

Figure 35.33 shows the event output operation example of compare function.

A scan end event (ADC12i_ADI) is output with the same timing of one time single scan completion. A match or mismatch event (ADC12i_WCMPM or ADC12i_WCMPUM) is output delayed by 1 PCLKB depending on ADCMPCR.CMPAB[1:0] settings.

Note: The match and mismatch events are exclusive, so both events are never output simultaneously.

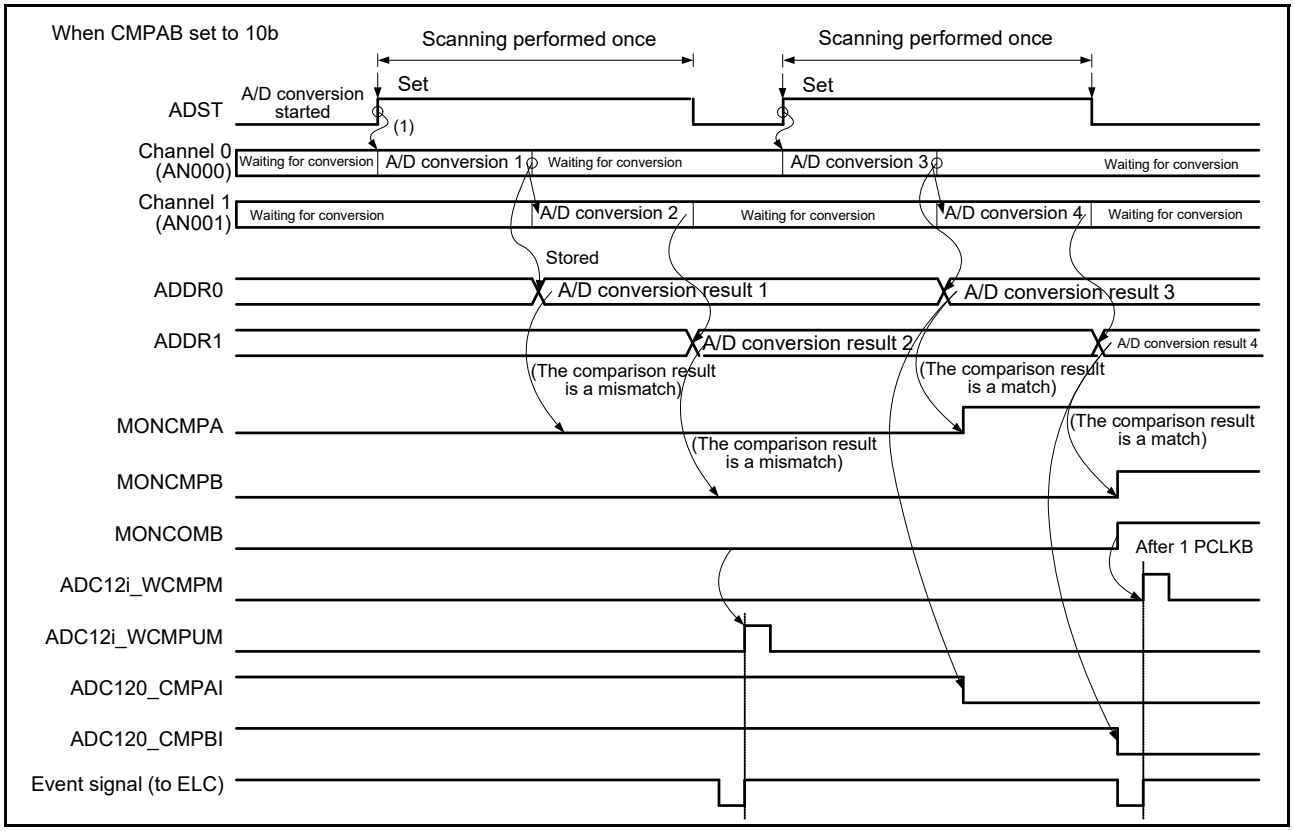


Figure 35.33 Example of the compare function event output when AN000 to AN001 are compared

Note 1. Event output of compare function outputs match/mismatch from the comparison results of window A and window B, based on the ADCMPCR.CMPAB[1:0] settings.

Note 2. The comparison result of window A is the logical addition of the comparison results of the comparison target channels of window A. The comparison results of window A and window B are updated by each A/D conversion, and are kept even when single scan ends. Set ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0 to clear the comparison results to 0.

35.3.5.3 Constraints on the compare function

The following constraints apply for the compare function:

- The compare function cannot be used together with the self-diagnosis function or double trigger mode (the compare function is not available for ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB)
- Specify single scan mode when using match/mismatch event outputs
- When the temperature sensor output or internal reference voltage is selected for window A, and window B operations are disabled
- When the temperature sensor output or internal reference voltage is selected for window B, and window A operations are disabled
- Setting the same channel for window A and window B is prohibited
- Set the reference voltage values so that the high-potential reference voltage value is equal to or larger than the low-potential reference voltage value.

35.3.6 Analog Input Sampling and Scan Conversion Time

Scan conversion can be activated by a software trigger, a synchronous trigger (ELC), or an asynchronous trigger (ADTRGn). After the start-of-scanning-delay (t_D) elapses, processing by the channel-dedicated sample-and-hold circuits, processing for disconnection detection assistance, and processing of conversion for self-diagnosis all proceed, followed by processing for A/D conversion.

Figure 35.34 shows the scan conversion timing, in which scan conversion is activated by a software trigger or a synchronous trigger (ELC). Figure 35.35 shows the scan conversion timing, in which scan conversion is activated by an asynchronous trigger, ADTRGn. The scan conversion time (t_{SCAN}) includes the start-of-scanning-delay (t_D), channel-dedicated sample-and-hold circuit processing time (t_{SPLSH}),*1 disconnection detection assistance processing time (t_{DIS}),*2 self-diagnosis A/D conversion processing time (t_{DIAG}),*3 A/D conversion processing time (t_{CONV} and t_{DSD}), channel-dedicated sample-and-hold circuit end time (t_{SHED}),*4 and end-of-scanning-delay (t_{ED}).

The A/D conversion processing time (t_{CONV}) consists of the input sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the ADC12. If there is not sufficient sampling time because of the high impedance of an analog input signal source, or if the A/D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTR register.

The time for conversion by successive approximation (t_{SAM}) is 13 ADCLK states with 12-bit accuracy selected, 11 ADCLK states with 10-bit accuracy selected, and 9 ADCLK states with 8-bit accuracy selected.

The scan conversion time (t_{SCAN}) in single scan mode for which the number of selected channels is n can be determined as follows:

$$t_{SCAN} = t_D + t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n)\ ^{*5} + t_{ED}$$

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single scan minus t_{ED} plus t_{SHED}.

The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed at $t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + t_{DSD} + (t_{CONV} \times n)\ ^{*5} + t_{SHED}$.

Note 1. When no channel-dedicated sample-and-hold circuits are used, $t_{SPLSH} = 0$.

Note 2. When disconnection detection assistance is not selected, $t_{DIS} = 0$.

Note 3. When the self-diagnosis function is not used, $t_{DIAG} = 0$, $t_{DSD} = 0$.

Note 4. When no channel-dedicated sample-and-hold circuits are used, $t_{SHED} = 0$, assuming continuous scan mode is active. In single scan mode and group scan mode, t_{SHED} is included in the end-of-scanning-delay (t_{ED}).

Note 5. When input sampling times (t_{SPL}) of all selected channels are the same, this element equals $t_{CONV} \times n$. If each channel has a different sampling time, this element equals that of t_{SPL} and t_{SAM} set to each selected channel.

Table 35.10 Conversion times during scanning (in numbers of ADCLK and PCLKB cycles)

Parameter			Symbol		Type/conditions: Synchronous trigger*4	Type/conditions: Asynchronous trigger	Type/conditions: Software trigger	Unit
Scan start processing time*1, *2	A/D conversion on group A under group A priority control	Group B is to be stopped. (group A is activated after group B is stopped by an A/D conversion source from group A).	t_D		3 PCLKB + 6 ADCLK 5 PCLKB + 3 ADCLK *5	-	-	Cycles
		Group B is not to be stopped (activation by an A/D conversion source from group A)			2 PCLKB + 4 ADCLK	-	-	
	A/D conversion when self-diagnosis is enabled	A/D conversion for self-diagnosis is to be started			2 PCLKB + 6 ADCLK	4 PCLKB + 6 ADCLK	6 ADCLK	
	All other				2 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	4 ADCLK	
Channel-dedicated sample-and-hold processing time*1	Sampling time		t_{SPLSH}	t_{SH}	Without continuous sampling: setting in ADSHCR.SSTSH[7:0] (initial value = 18h × ADCLK) With continuous sampling: 0			
	Wait time between sampling and A/D conversion			t_W	12			
Disconnection detection assistance processing time			t_{DIS}		Setting in ADNDIS[3:0] (initial value = 0h) × ADCLK			
Self-diagnosis conversion processing time*1	Sampling time		t_{DIAG}	t_{SPL}	Setting in ADSSTR00 (initial value = 0Bh) × ADCLK*3	-	-	
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	15 ADCLK	-	-	
		10-bit conversion accuracy			13 ADCLK	-	-	
		8-bit conversion accuracy			11 ADCLK	-	-	
	Wait time between self-diagnosis conversion end and analog channel sampling start			t_{DED}	2 ADCLK			
	Wait time between last channel conversion end and self-diagnosis sampling start in continuous scan mode		t_{DSD}		2 ADCLK			
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	Setting in ADSSTRn (n = 00 to 03, 05 to 07, L, T, O) (initial value = 0Bh) × ADCLK + 0.5 ADCLK			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	13 ADCLK			
		10-bit conversion accuracy			11 ADCLK			
		8-bit conversion accuracy			9 ADCLK			
Channel-dedicated sample-and-hold end processing time			t_{SHED}		2 ADCLK			
Scan end processing time*1			t_{ED}		1 PCLKB + 3 ADCLK 2 PCLKB + 3 ADCLK*5			

Note 1. See Figure 35.34 and Figure 35.35 for an illustration of times t_D, t_{SPLSH}, t_{DIAG}, t_{CONV}, and t_{ED}.
Note 2. This is the maximum time required from software writing or trigger input to A/D conversion start.
Note 3. The sampling time setting must satisfy the electrical characteristics.
Note 4. This does not include the time consumed in the path from timer output to trigger input.
Note 5. If ADCLK is faster than PCLKB (PCLKB to ADCLK frequency ratio = 1:2 or 1:4), the scan end processing time changes.

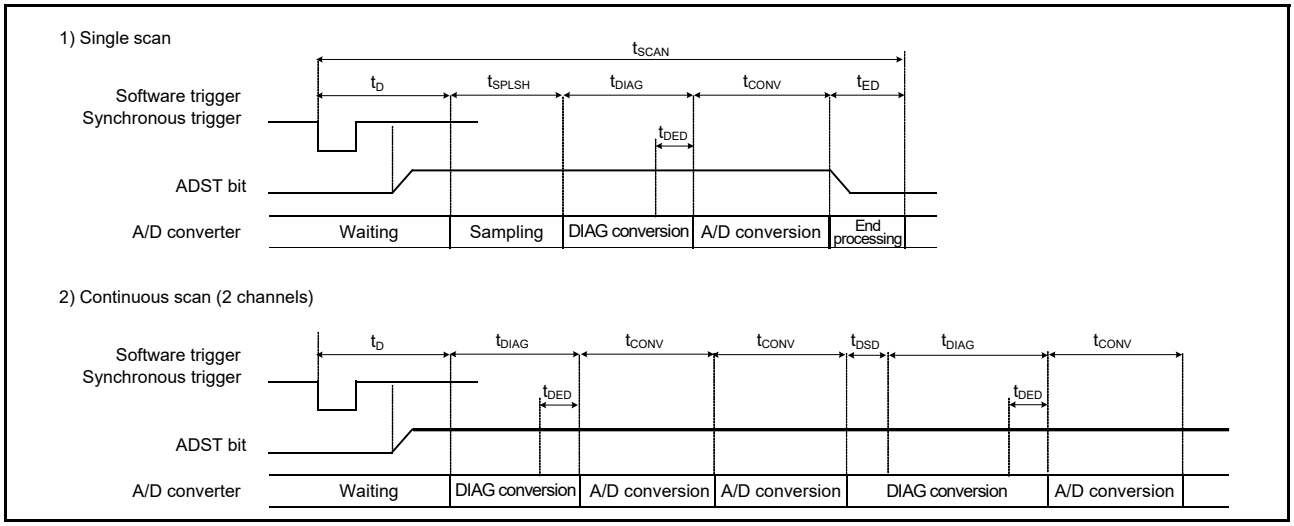


Figure 35.34 Scan conversion timing when activated by software or a synchronous trigger input (ELC)

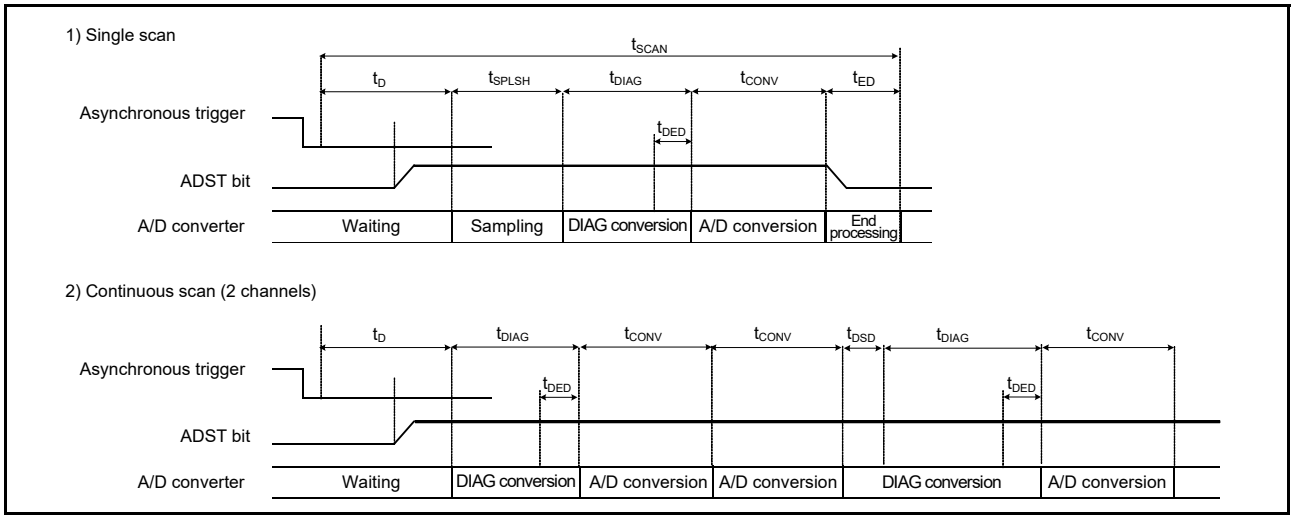


Figure 35.35 Scan conversion timing when activated by an asynchronous trigger input (ADTRG0)

35.3.7 Usage Example of A/D Data Register Automatic Clearing Function

A/D-converted value addition/average mode can be used when A/D conversion of the analog input of the selected channels, temperature sensor output, or internal reference voltage is selected.

Setting the ACE bit in ADCER to 1 automatically clears the data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, and ADOCDR) to 0000h when the data registers are read by the CPU, DTC, or DMAC. This function enables detection of update failures by the data registers.

In the following examples, the function to automatically clear the ADDRy register is enabled and disabled:

- If the ACE bit in ADCER is 0 (automatic clearing disabled), and for some reason, the A/D conversion result (0222h) is not written to the ADDRy register, the ADDRy value retains the old data (0111h). In addition, if this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, the old data (0111h) can be saved in the general-purpose register. When checking whether there is an update failure, it is necessary to frequently save the old data in SRAM or in a general-purpose register.
- If the ACE bit in ADCER is 1 (automatic clearing enabled), when ADDRy = 0111h is read by the CPU, DTC, or DMAC, ADDRy is automatically cleared to 0000h. Next, if the A/D conversion result 0222h cannot be transferred to ADDRy for some reason, the cleared data (0000h) remains as the ADDRy value. If this ADDRy value is read into a general-purpose register using an A/D scan end interrupt at this point, 0000h is saved in the general-purpose register. Occurrence of an ADDRy update failure can be determined by checking that the read data value is 0000h.

35.3.8 A/D-Converted Value Addition/Average Mode

In A/D-converted value addition mode, the same channel is A/D-converted 1, 2, 3, 4, or 16*1 consecutive times, and the sum of the converted values is stored in the data register. In A/D-converted value average mode, the same channel is A/D-converted 2 or 4 consecutive times, and the mean of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. However, this function cannot always guarantee an improvement in A/D conversion accuracy.

The A/D-converted value addition or average mode can be specified for A/D conversion of the channel select analog input, temperature sensor output, or internal reference voltage.

Note 1. The addition count can be set to 16 only when 12-bit accuracy is selected.

35.3.9 Disconnection Detection Assist Function

This converter incorporates a function that fixes the charge for sampling capacitance to the specified state (VREFH0 or VREFL0 for unit 0, VREFH or VREFL for unit 1) before the start of A/D conversion. This function enables disconnection detection in wiring of analog inputs.

When using the disconnection detection assist function for the channel-dedicated sample-and-hold circuit, select ADSHMSR.SHMD bit to 0 (select disable continuous sampling function).

If any of the following functions are used, the disconnection detection assist function should be disabled:

- Temperature sensor
- Internal reference voltage
- A/D self-diagnosis
- Programmable gain amplifier without bypass enabled.

Figure 35.36 shows the A/D conversion operation when the disconnection detection assist function is used. Figure 35.37 shows an example of disconnection detection when precharge is selected. Figure 35.38 shows an example of disconnection detection when discharge is selected.

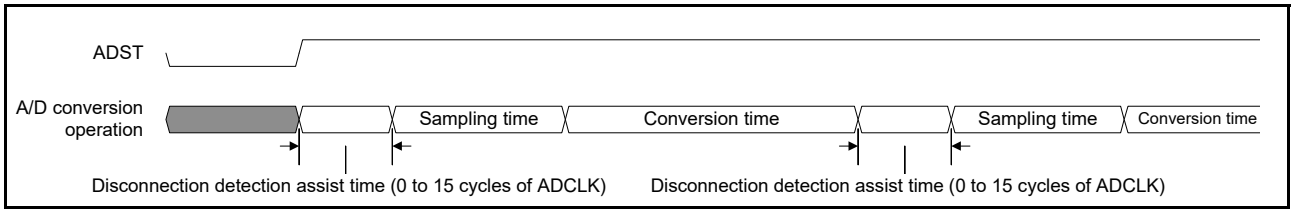
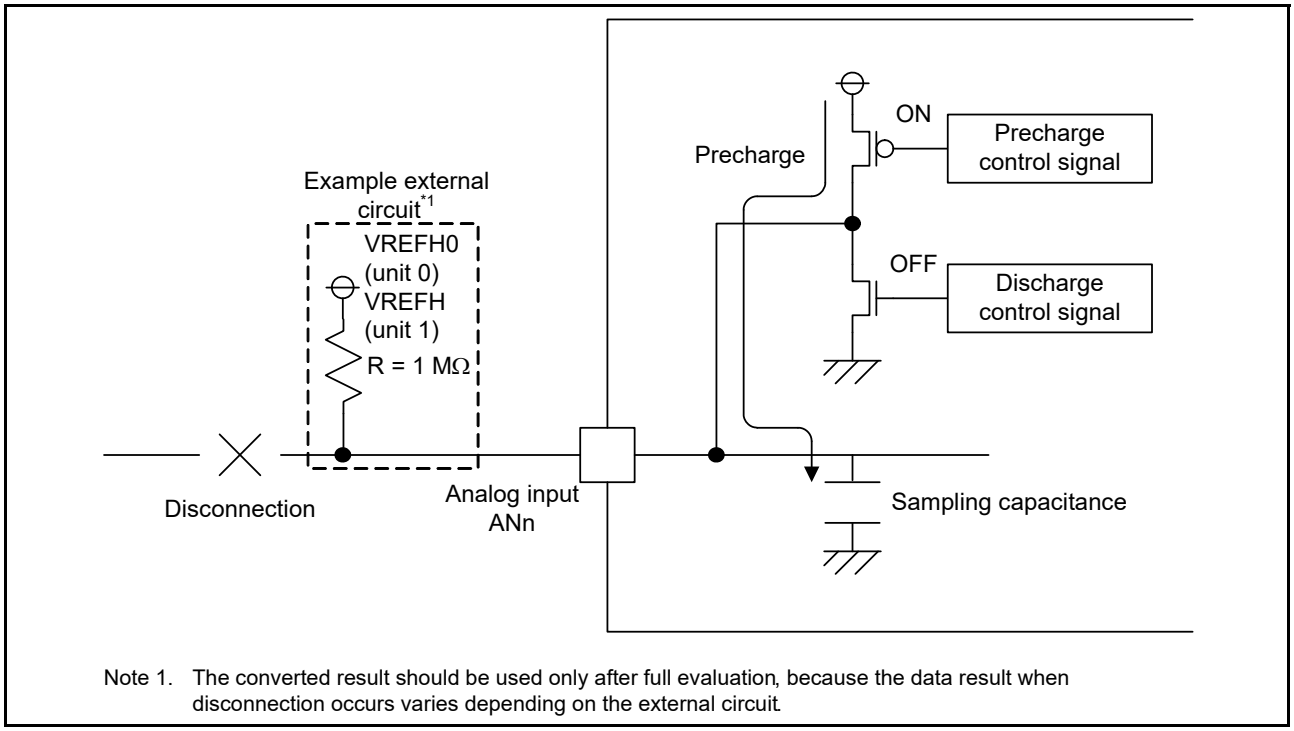
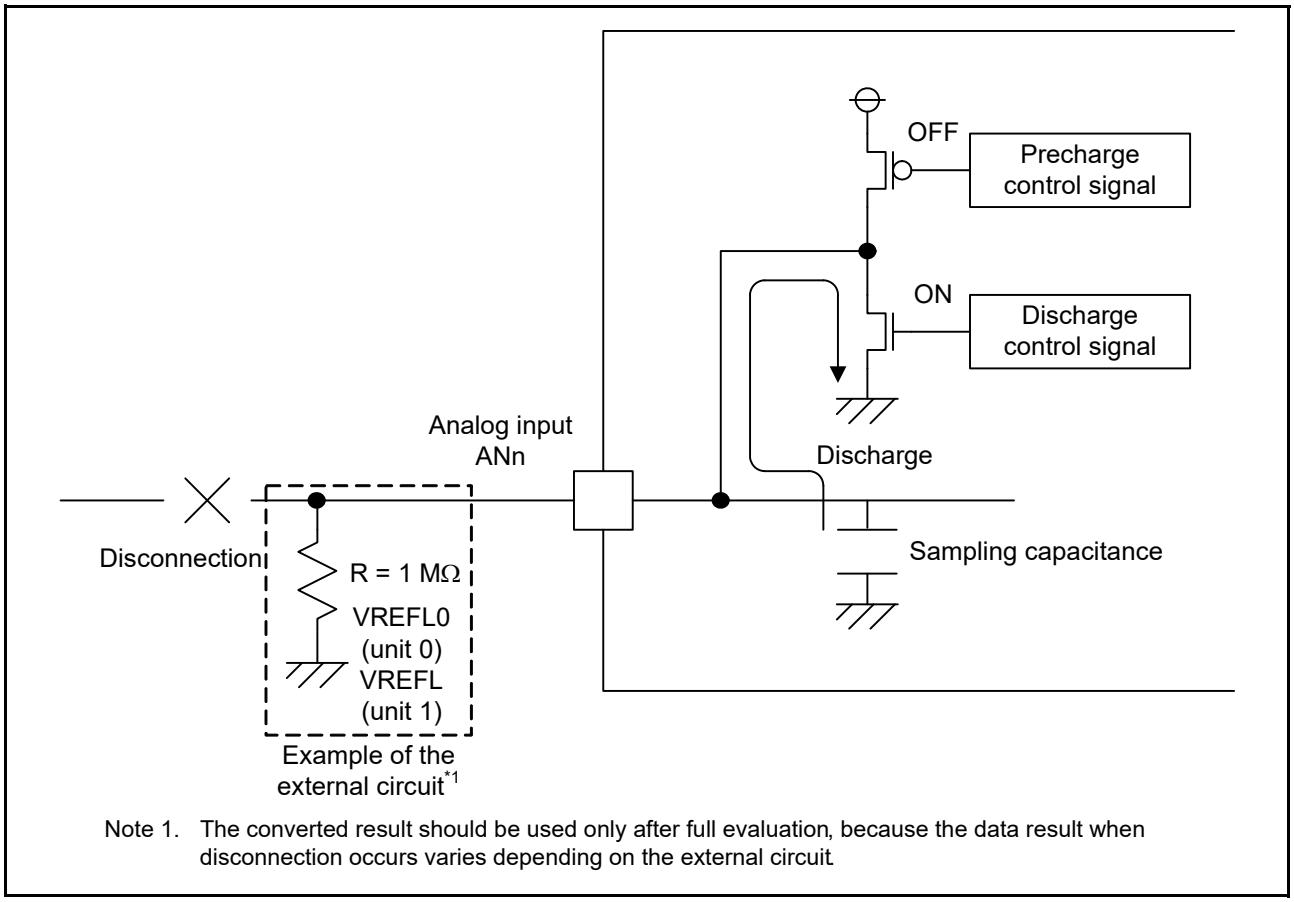


Figure 35.36 A/D conversion operation when the disconnection detection assist function is used



Note 1. The converted result should be used only after full evaluation, because the data result when disconnection occurs varies depending on the external circuit.

Figure 35.37 Example of disconnection detection when precharge is selected



Note 1. The converted result should be used only after full evaluation, because the data result when disconnection occurs varies depending on the external circuit.

Figure 35.38 Example of disconnection detection when discharge is selected

35.3.10 Starting A/D Conversion with an Asynchronous Trigger

A/D conversion can be started by the input of an asynchronous trigger. To start the A/D conversion by an asynchronous trigger, first set the pin function in the PmnPFS register, next set the A/D Conversion Start Trigger Select bits (ADSTRGR.TRSA[5:0]) to 000000b, then input a high-level signal to the asynchronous trigger (ADTRGn pin). Finally, set both the ADCSR.TRGE and ADCSR.EXTRG bits to 1. Figure 35.39 shows timing of the asynchronous trigger input.

An asynchronous trigger cannot be selected in the A/D Conversion Start Trigger Select bits (ADSTRGR.TRSB[5:0]) for group B in group scan mode. For details on setting the pin function, see section 19, I/O Ports.

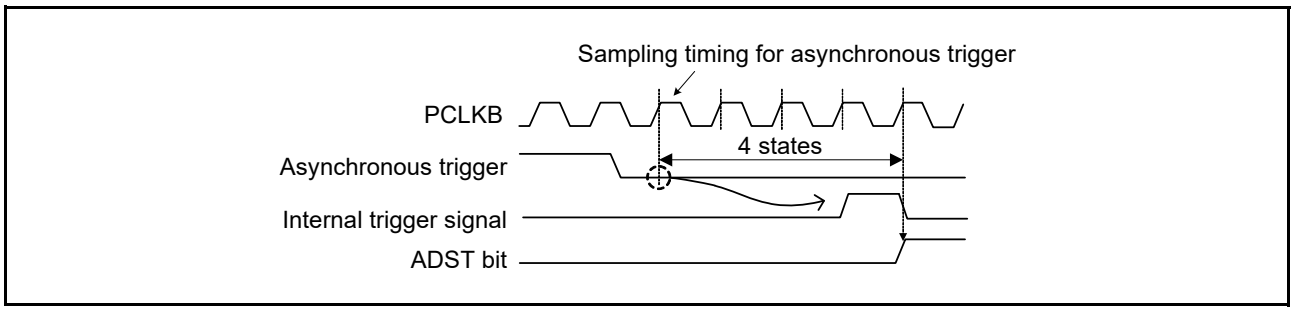


Figure 35.39 Asynchronous trigger input timing

35.3.11 Starting A/D Conversion with a Synchronous Trigger from a Peripheral Module

A/D conversion can be started by a synchronous trigger (ELC). To start the A/D conversion by a synchronous trigger, set the ADCSR.TRGE bit to 1, clear the ADCSR.EXTRG bit to 0, and select the relevant sources in the ADSTRGR.TRSA[5:0] and ADSTRGR.TRSB[5:0] bits.

35.3.12 Programmable Gain Amplifiers

Up to three programmable gain amplifiers (PGAs) can be used in each unit. Select a gain in the ADPGAGS.PnGAIN[3:0] bits (n = 000 to 002) and select an operational amplifier to be used in the ADPGACR.PnSEL bits.

These PGAs accept pseudo-differential inputs. Pins that accept pseudo-differential inputs are PGAVSS000 for AN000 to AN002 (unit 0), PGAVSS100 for AN100 to AN102 (unit 1). To use pseudo-differential inputs, set the pseudo-differential input gain in the ADPGADCR0.PnDG[2:0] bits, enable the pseudo-differential input gain setting in the ADPGADCR0.PnGEN bits, and then select the pseudo-differential input amplifier in the ADPGADCR0.PnDEN bits. The PGA register is selectable as shown in Table 35.11.

Table 35.11 Setting of PGA register and available related functions

Selectable value for each condition	Setting of corresponding register				Related function ✓: available x: unavailable			
	PmnPFS	ADPGACR	ADPGAGS0	ADPGADCR0				
		PGA P002: bits [11:8]	bits [11:8]	bits [11:8]		ACMPHS*2		
		PGA P001: bits [7:4]	bits [7:4]	bits [7:4]				
	ASEL*3	PGA P000: bit [3:0]	bit [3:0]	bit [3:0]	Ports*1	IVCMP2	IVCMP3	ADC12
When using ports	0	Leave these bits with initial values			✓	x	x	x
When using ACMPHS or ADC12 (PGA bypass)*4	1	9	0	0	x	✓	x	✓
When using PGA pseudo-differential input disabled	1	Eh	0 to Eh	0	x	✓	✓	✓
When using PGA pseudo-differential input enabled	1	Eh	1, 5, 9, Bh	8 to Bh	x	x	✓	✓

Note 1. Ports: When using input ports.
Note 2. ACMPHS IVCMP2: When using input through the PGA. ACMPHS IVCMP3: When using input of PGA output.
Note 3. For detail on the configuration of PmnPFS registers, see section 19, I/O Ports.
Note 4. Ports and ACMPHS cannot be used at the same time. Ports and ADC12 cannot be used at the same time.

Table 35.12 shows the calculation formula for the PGA output voltage.

Table 35.12 PGA output voltage

Mode	PGA output voltage
Single	Gain × Vin
Pseudo-Differential	Gain (Vin - Vs) + 0.5 × AVCC

Vin: AN000 to AN002, AN100 to AN102
Vs: PGAVSS00, PGAVSS001

35.4 Vs: PGAVSS00, PGAVSS001Interrupt Sources and DTC/DMAC Transfer Requests

35.4.1 Interrupt Requests

The ADC12 can send scan end interrupt requests, ADC12i_ADI (i = 0, 1) and ADC12i_GBADI, to the CPU. The ADC12 also generates the ADC12i_CMPAI and ADC12i_CMPBI interrupts to the CPU in response to matches with a comparison condition.

An ADC12i_ADI interrupt is always generated. An ADC12i_GBADI interrupt can be generated by setting the ADCSR.GBADIE bit to 1. Similarly, ADC12i_CMPAI and ADC12i_CMPBI interrupts can be generated by setting the ADCMPCR.CMPAIE and ADCMPCR.CMPBIE bits to 1.

In addition, the DTC or DMAC can be started when an ADC12i_ADI or ADC12i_GBADI interrupt, or ADC12i_WCMPM or ADC12i_WCMPUM event is generated. Using these interrupts or events to allow the DTC or DMAC to read the converted data enables continuous conversion without burdening the software.

For details on the DTC settings, see section 17, Data Transfer Controller (DTC), and for details on the DMAC settings, see section 16, DMA Controller (DMAC).

Table 35.13 describes the interrupt sources and ELC events available for the ADC12.

Table 35.13 ADC12 events (1 of 2)

✓: Available x: Unavailable

Operation		Interrupt request or ELC event			Inter-rupt re-quest	DTC/ DMAC activa-tion	ELC event re-quest	Function
Scan mode	Double trigger mode	Compare function win-dow A/B	Unit 0	Unit 1				
Single scan mode	Deselected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of single scan
		Selected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of single scan
			ADC120_CMPAI	ADC121_CMPAI	✓	x	x	ADC12i_CMPAI generated on a match comparison condition of window A
			ADC120_CMPBI	ADC121_CMPBI	✓	x	x	ADC12i_CMPBI generated on a match comparison condition of window B
			ADC120_WCMPM	ADC121_WCMPM	x	✓	✓	ADC12i_WCMPM generated on a match condition of the window A/B compare function
			ADC120_WCMPUM	ADC121_WCMPUM	x	✓	✓	ADC12i_WCMPUM generated on a mismatch condition of the window A/B compare function
	Selected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of scans in the even-numbered times
Continuous scan mode	Deselected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of scan of all selected channels
		Selected	ADC120_CMPAI	ADC121_CMPAI	✓	x	x	ADC12i_CMPAI generated on a match comparison condition of window A
			ADC120_CMPBI	ADC121_CMPBI	✓	x	x	ADC12i_CMPBI generated on a match comparison condition of window B

Table 35.13 ADC12 events (2 of 2)

✓: Available x: Unavailable

Operation		Interrupt request or ELC event			Inter-rupt re-quest	DTC/ DMAC activa-tion	ELC event re-quest	Function
Scan mode	Double trigger mode	Compare function win-dow A/B	Unit 0	Unit 1				
Group scan mode	Deselected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of group A scan
			ADC120_GBADI	ADC121_GBADI	✓	✓	x	ADC12i_GBADI dedicated to group B generated at the end of group B scan
		Selected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of group A scan
			ADC120_GBADI	ADC121_GBADI	✓	✓	x	ADC12i_GBADI dedicated to group B generated at the end of group B scan
			ADC120_CMPAI	ADC121_CMPAI	✓	x	x	ADC12i_CMPAI generated on a match comparison condition of window A
			ADC120_CMPBI	ADC121_CMPBI	✓	x	x	ADC12i_CMPBI generated on a match comparison condition of window B
	Selected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of group A scans in the even-numbered times
			ADC120_GBADI	ADC121_GBADI	✓	✓	x	ADC12i_GBADI dedicated to group B generated at the end of group B scan

Note: i = 0: unit 0, i = 1: unit 1.

35.5 Event Link Function

35.5.1 Event Output to the ELC

The ELC uses an ADC12i_ADI interrupt request signal as an event signal, enabling link operation for the preset module. The ADC12i_GBADI interrupt and ADC12i_CMPAI/ADC12i_CMPBI interrupts cannot be used as event signals. For details, see Table 35.13.

35.5.2 ADC12 Operation through an Event from the ELC

The ADC12 can start A/D conversion by the preset event specified in the ELSRn settings for the ELC as follows:

- Select the ELC_AD00 (unit 0) signal in the ELC.ELSR8 register
- Select the ELC_AD01 (unit 0) signal in the ELC.ELSR9 register
- Select the ELC_AD10 (unit 1) signal in the ELC.ELSR10 register
- Select the ELC_AD11 (unit 1) signal in the ELC.ELSR11 register.

If an ELC_ADi0 or ELC_ADi1 event occurs during A/D conversion, the event is disabled.

35.6 Usage Notes

35.6.1 Constraints on Reading the Data Registers

The following registers must be read in halfword units:

- A/D Data Registers
- A/D Data Duplexing Register
- A/D Data Duplexing Register A
- A/D Data Duplexing Register B
- A/D Temperature Sensor Data Register
- A/D Internal Reference Voltage Register
- A/D Self-Diagnosis Data Register.

If a register is read twice in byte units, that is, the upper byte and lower byte are read separately, the A/D-converted value initially read might not match with the A/D-converted value subsequently read. To prevent this, never read the data registers in byte units.

35.6.2 Constraints on Stopping A/D Conversion

To stop A/D conversion when an asynchronous trigger or a synchronous trigger is selected as the condition for starting A/D conversion, follow the procedure shown in Figure 35.40.

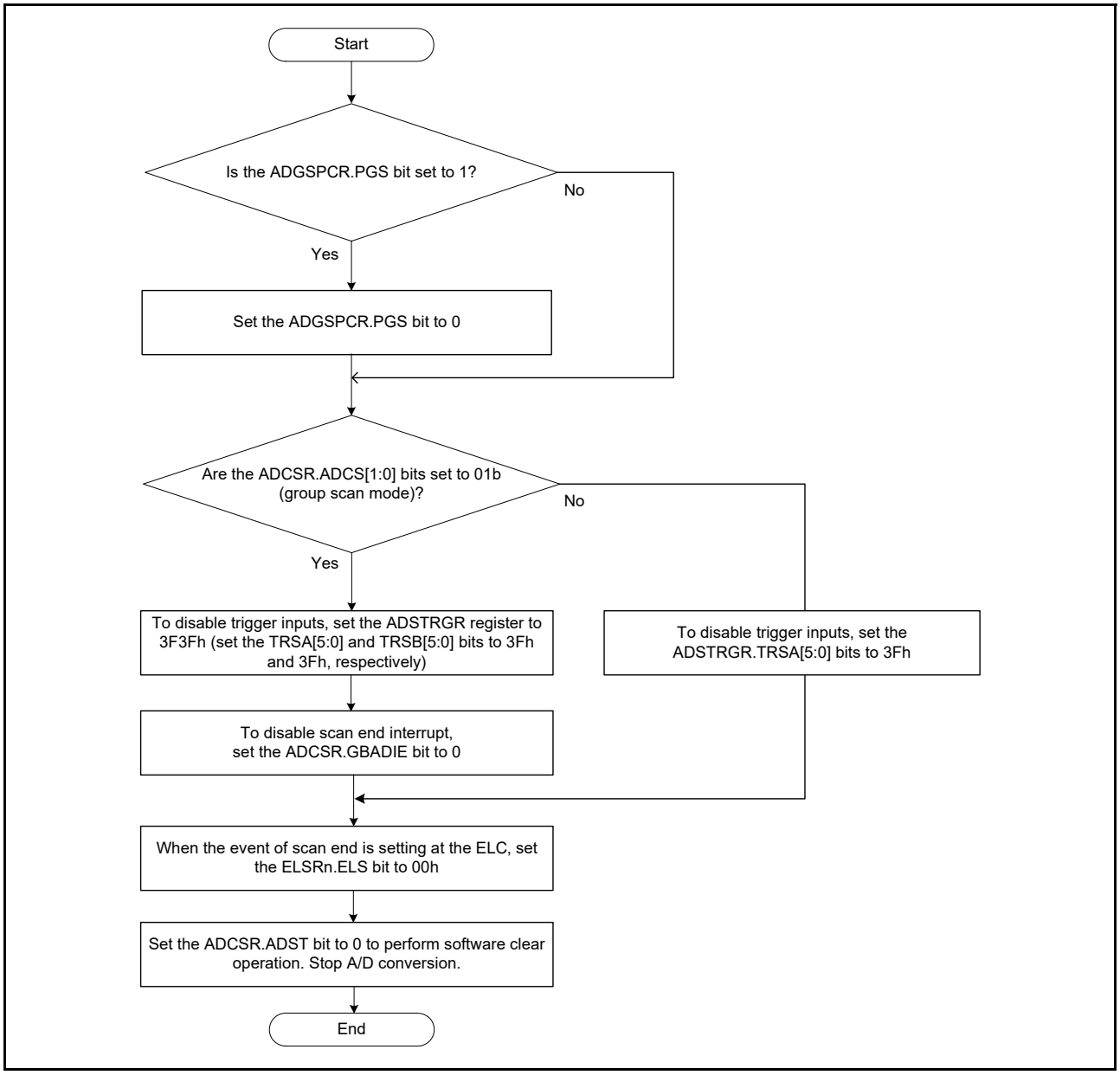


Figure 35.40 Procedure for clearing the ADCSR.ADST bit by software

35.6.3 A/D Conversion Restart and Termination Timing

A maximum of 6 ADCLK cycles is required for the idle analog unit of the ADC12 to restart on setting the ADCSR.ADST bit to 1. A maximum of 2 ADCLK cycles is required for the operating analog unit of the ADC12 to be terminate on setting the ADCSR.ADST bit to 0.

35.6.4 Constraints on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D-converted data is overwritten with the second A/D-converted data if the CPU does not finish reading the A/D-converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

35.6.5 Settings for the Module-Stop Function

The Module Stop Control Register can enable or disable ADC12 operation. The ADC12 is initially stopped after reset. Releasing the module-stop state enables access to the registers. After release from the module-stop state, wait for at least 1 µs before starting A/D conversion. For details, see section 11.4, Module-Stop Function.

35.6.6 Notes on Entering the Low Power States

Before entering the module-stop state or Software Standby mode, you must stop A/D conversion. Set the ADCSR.ADST bit to 0 and secure a period of time until the analog unit of the ADC12 stops.

To secure this time, follow the procedure shown in Figure 35.40 for clearing the ADCSR.ADST bit through software. Then, wait for 2 clock cycles of ADCLK before entering the module-stop state or Software Standby mode.

35.6.7 Error in Absolute Accuracy when Disconnection Detection Assistance Is in Use

Using disconnection detection assistance leads to an error in the absolute accuracy of the ADC12. This error arises because an erroneous voltage is input to the analog input pins because of the resistive voltage division between the pull-up or pull-down resistor (Rp) and the resistance of the signal source (Rs). This error in absolute accuracy is calculated from the following formula:

Maximum error in absolute accuracy (LSB) = $(2^{\text{Resolution - 1}}) \times Rs / (Rs + Rp)$, where Resolution = 12, 10, 8

Only use disconnection detection assistance after thorough evaluation.

35.6.8 Available functions and register settings of AN000 to AN002, AN007, AN100 to AN102, and AN107

Table 35.14 shows the available functions and register settings of AN000 to AN002, AN007, AN100 to AN102 and AN107, and Figure 35.41 shows the setting procedure of registers. To use each function, set the register value shown in Table 35.14.

When the PGA is used with pseudo-differential input enabled, a negative voltage can be input for AN000 to AN002 and PGAVSS000 for unit 0, and AN100 to AN102 and PGAVSS100 for unit 1 after setting the registers.

When the PGA is used with pseudo-differential input enabled, all PGA amplifiers in each unit must be set to pseudo-differential input in the ADPGADCR0 register.

When the PGA is used with pseudo-differential input disabled, the associated PGAVSS pin must be connected to AVSS0. When the PGA is not used, the associated PGAVSS can be used as an input port or analog input.

When transitioning to the ADC module-stop state or Software Standby mode from the state of using PGA or sample-and-hold circuit, if the corresponding bit in ADPGACR or ADSHCR register of each ADC12 is set to 0 before transitioning, power consumption can be reduced.

The initial value of the ASEL bit of P003 and P007 is 1. When these pins are not used as an analog function, to reduce the input leakage current, the ASEL bit should be set to 0.

When using a 64-pin product, the P007PFS.ASEL bit should be set to 0.

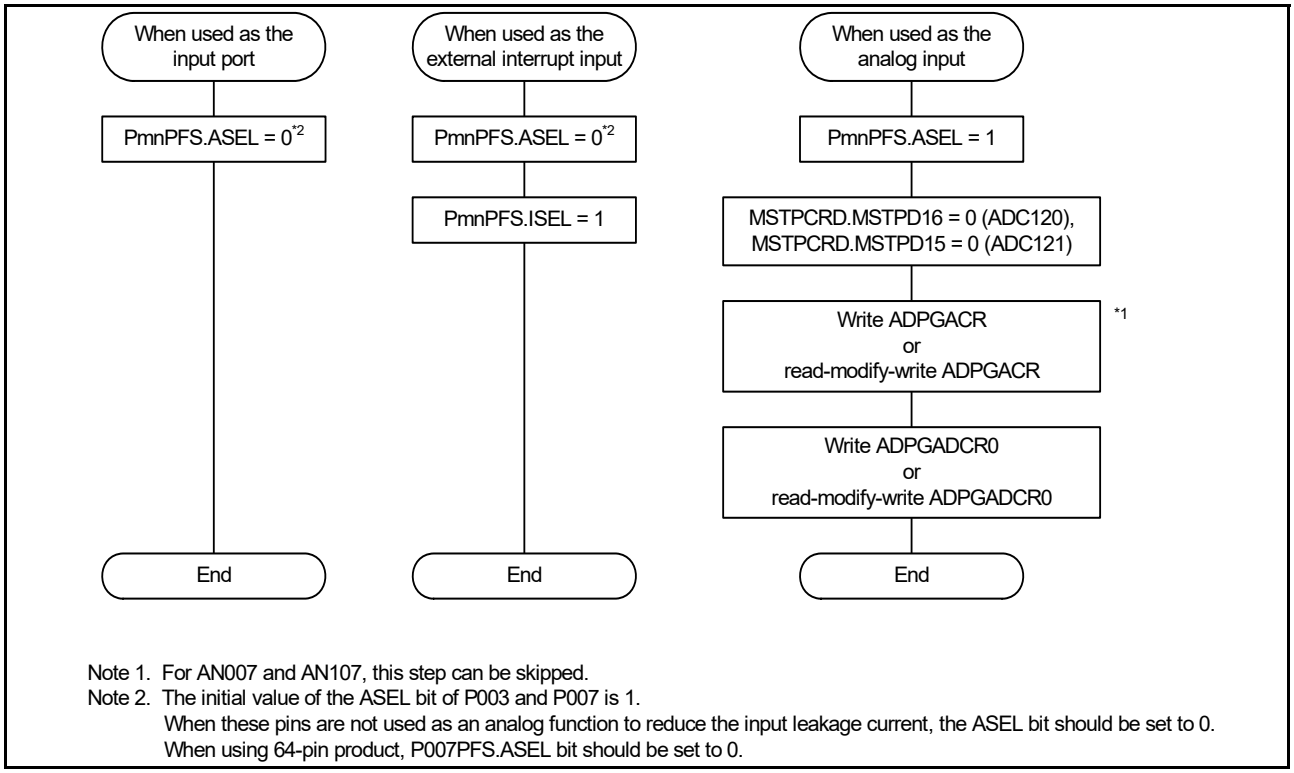
Table 35.14 Available functions and register setting

Available functions						Register setting				
						P0nPFS*6		PGA		S/H*3
Ports*1	IRQ*2	S/H*3	PGA-S*4	PGA-D*5	ADC12	ASEL	ISEL	ADPGADCR0*7	ADPGACR*8	ADSHCR*9
✓						0	0	x	x	x
	✓					0	1	x	x	x
					✓*10	1	x	0	9h	0
					✓*11	1	x	0*11	0 or 9h	0
		✓			✓	1	x	0	9h	1 (0*13)
		✓	✓		✓	1	x	0	Eh (0h*12)	1 (0*13)
		✓		✓	✓	1	x	1	Eh (0h*12)	1 (0*13)
			✓		✓	1	x	0	Eh (0h*12)	0
				✓	✓	1	x	1	Eh (0h*12)	0

✓: Available
x: Don't care

Note 1. Ports: P000 to P007 can be used as port inputs.

Note 2. IRQ: P000 to P002 and P003 to P005 can be used as IRQ pins.
Note 3. S/H: sample-and-hold circuit.
Note 4. PGA-S: When the PGA setting is "pseudo-differential input disabled". Corresponding PGAVSS must be set as ASEL set to 1, and connected to AVSS0.
Note 5. PGA-D: When the PGA setting is "pseudo-differential input enabled". Corresponding PGAVSS must be set as ASEL to 1.
Note 6. P0nPFS: Port 0n Pin Function Select register (n = 00 to 07) corresponding to the analog input pin.
Note 7. Indicates the corresponding ADPGADCR0 register, Pseudo-Differential Input Enable bit (bit [11] or bit [7] or bit [3]).
Note 8. Indicates the corresponding ADPGACR register, Amplifier Control bits (bits [11:8] or bits [7:4] or bits [3:0]).
Note 9. Indicates the corresponding ADSHCR register, Bypass Select bit (bit [10] or bit [9] or bit [8]).
Note 10. When using AN000 to AN002 or AN100 to AN102.
Note 11. When using AN007 or AN107. Set all corresponding bits (bit [11], [7], and [3] in ADPGADCR0) to 0.
Note 12. Power consumption of the PGA can be reduced by setting the corresponding bit in the ADPGACR register to 0 before transitioning to the ADC12 module-stop state or Software Standby mode.
Note 13. Power consumption of the S/H can be reduced by setting the corresponding bit in the ADSHCR register to 0 before transitioning to the ADC12 module-stop state or Software Standby mode.



Note 1. For AN007 and AN107, this step can be skipped.
Note 2. The initial value of the ASEL bit of P003 and P007 is 1.
When these pins are not used as an analog function to reduce the input leakage current, the ASEL bit should be set to 0.
When using 64-pin product, P007PFS.ASEL bit should be set to 0.

Figure 35.41 Setting procedure of registers

35.6.9 Notes on Operating Modes and Status Bits

Initialize or set again individually, if necessary, the voltage values in self-diagnosis, the determination of the first scan or second scan in double-trigger mode, the data buffer pointer, and the status monitor in the compare function.

- Select the voltage values in self-diagnosis (ADCER.DIAGVAL[1:0]) after setting ADCER.DIAGLD to 1
- Double trigger mode operates as the first scan after setting ADCSR.DBLE to 1 from 0
- The status monitor bits (MONCMPA, MONCMPB, and MONCOMB) in the compare function are initialized after ADCMPCR.CMPAE and ADCMPCR.CMPBE are set to 0
- The constant sampling function (ADSHMSR.SHMD = 1) is initialized after ADSHMSR.SHMD is set to 0. When the constant sampling function is used (setting ADSHMSR.SHMD = 1) again, wait 1 ADCLK cycle or more.

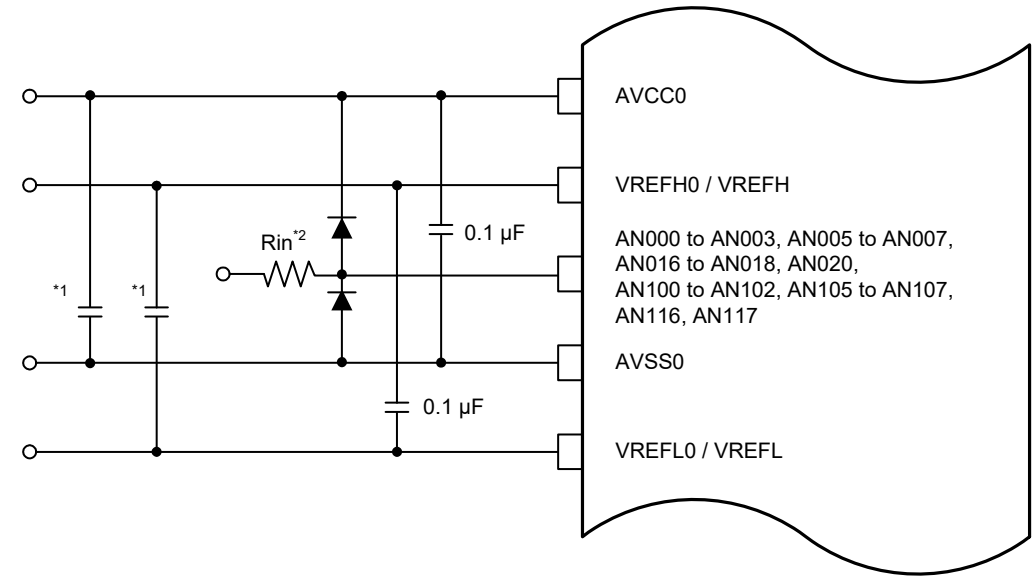
35.6.10 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or be placed near each other. If these rules are not followed, noise can occur on analog signals and A/D conversion accuracy is affected. The analog

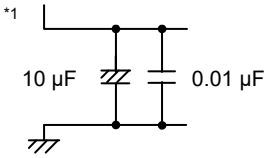
input pins (AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020, AN100 to AN102, AN105 to AN107, AN116, AN117), reference power supply pin (VREFH0/VREFH), reference ground pin (VREFL0/VREFL), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0). The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

35.6.11 Constraints on Noise Prevention

To prevent the analog input pins (AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020, AN100 to AN102, AN105 to AN107, AN116, AN117) from being destroyed by abnormal voltage such as excessive surges, insert a capacitor between AVCC0 and AVSS0, between VREFH0 and VREFL0, and between VREFH and VREFL, and connect a protection circuit to protect the analog input pins (AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020, AN100 to AN102, AN105 to AN107, AN116, AN117) as shown Figure 35.42.



Note 1. The values shown here are reference values.



Note 2. Rin: Signal source impedance

Figure 35.42 Example protection circuit for analog inputs

35.6.12 Port Settings when Using the ADC12 Input

When using the high-precision channels, do not use PORT 0 as a digital output port. Renesas also recommends not using the digital output that is also used as the A/D analog input, if normal precision channels are used. If the digital output that is also used as the A/D analog input is used for output signals, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

35.6.13 Relationship between ADC12 Units 0 and 1 and the ACMPHS

For the A/D conversion targets in Table 35.15, unit 0 and 1 cannot perform A/D conversion at the same time.

Table 35.15 A/D conversion targets that are mutually exclusive with each other

A/D conversion target	
Unit 0	**Unit 1**
Temperature sensor	
Internal reference voltage	
AN005/DA0	AN105/DA0
AN006/DA1	AN106/DA1

The A/D conversion targets in Table 35.16 should not be selected as ACMPHS input during A/D conversion, because these pins are multiplexed with the ADC12 and ACMPHS.

Table 35.16 A/D conversion targets that are mutually exclusive with ACMPHS

A/D conversion target		
Unit 0	**Unit 1**	**ACMPHS**
AN000	-	ACMPHS0.IVCMP2
AN001	-	ACMPHS1.IVCMP2
AN002	-	ACMPHS2.IVCMP2
PGA P000 output	-	ACMPHS0.IVCMP3
PGA P001 output	-	ACMPHS1.IVCMP3
PGA P002 output	-	ACMPHS2.IVCMP3
AN005/DA0	-	ACMPHS0 to ACMPHS5.IVREF3
AN006/DA1	-	ACMPHS0 to ACMPHS5.IVCMP1
AN016	-	ACMPHS0 to ACMPHS5.IVREF0
AN017	-	ACMPHS0 to ACMPHS5.IVCMP0
Internal reference voltage	-	ACMPHS0 to ACMPHS5.IVREF2
-	AN100	ACMPHS3.IVCMP2
-	AN101	ACMPHS4.IVCMP2
-	AN102	ACMPHS5.IVCMP2
-	PGA P000 output	ACMPHS3.IVCMP3
-	PGA P001 output	ACMPHS4.IVCMP3
-	PGA P002 output	ACMPHS5.IVCMP3
-	AN105/DA0	ACMPHS3 to ACMPHS5.IVREF3
-	AN106/DA1	ACMPHS3 to ACMPHS5.IVCMP1
-	AN116	ACMPHS0 to ACMPHS5.IVREF1
-	Internal reference voltage	ACMPHS0 to ACMPHS5.IVREF2

36. 12-Bit D/A Converter (DAC12)

36.1 Overview

The MCU provides a 12-bit D/A Converter (DAC12) with an output amplifier.

Table 36.1 lists the DAC12 specifications, Figure 36.1 shows a block diagram, and Table 36.2 lists the I/O pins.

Table 36.1 DAC12 specifications

Parameter	Specifications
Resolution	12 bits
Output channels	2 channels
Interference reduction between analog modules	Methods provided to minimize interference between D/A and A/D conversion: • D/A converted data update timing is controlled by the ADC12 synchronous D/A conversion enable input signal from the ADC12 (unit 1) • Degradation of A/D conversion accuracy caused by interference is reduced by controlling the DAC12 inrush current generation timing with the enable signal
Module-stop function	Module-stop state can be set to reduce power consumption
Event link function (input)	DA0 and DA1 conversion can be started when an event signal is input
D/A output amplifier control function	Controls whether the output amplifier (for both amplifier-through and amplifier-bias controls) is used

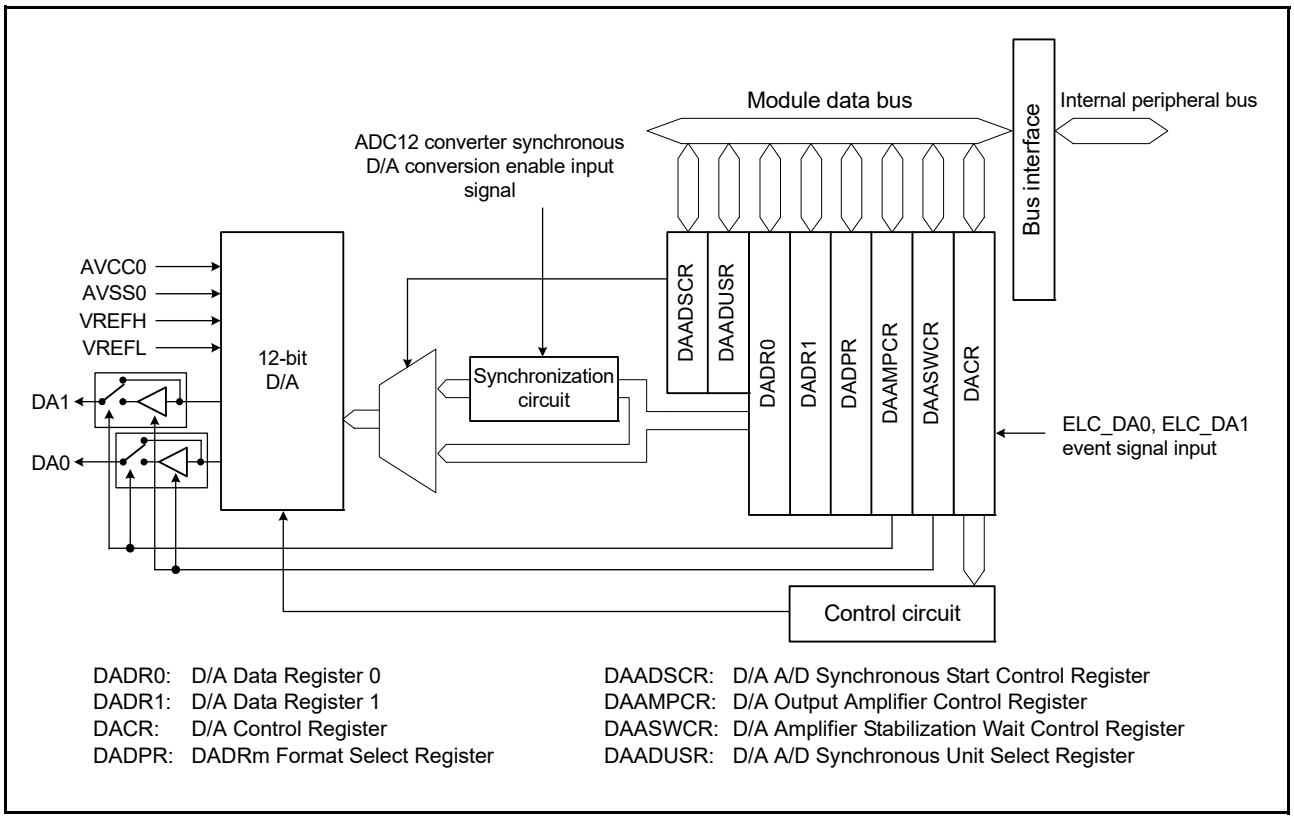


Figure 36.1 DAC12 block diagram

Table 36.2 DAC12 I/O pins (1 of 2)

Pin name	I/O	Function
AVCC0	Input	Analog power supply pin for ADC12, DAC12, and comparator. Connect to VCC when these modules are not used.

Table 36.2 DAC12 I/O pins (2 of 2)

Pin name	I/O	Function
AVSS0	Input	Analog ground pin for ADC12, DAC12, and comparator. Connect to VSS when these modules are not used.
VREFH	Input	Analog reference top voltage supply pin for the ADC12 (unit 1) and the DAC12
VREFL	Input	Analog reference ground pin for the ADC12 (unit 1) and the DAC12
DA0	Output	Channel 0 analog output pin
DA1	Output	Channel 1 analog output pin

36.2 Register Descriptions

36.2.1 D/A Data Register m (DADRm) (m = 0, 1)

Address(es): DAC12.DADR0 4005 E000h, DAC12.DADR1 4005 E002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADRm registers are 16-bit read/write registers that store data for D/A conversion. When an analog output is enabled, the values in DADRm are converted and output to the analog output pins.

12-bit data can be formatted as left- or right-justified in the DADPR.DPSEL bit setting. In right-justified format (DADPR.DPSEL = 0), the lower 12 bits, [11:0], are valid. In left-justified format (DADPR.DPSEL = 1), the upper 12 bits, [15:4], are valid.

For information on using the output amplifier, see section 36.6.5, Initialization Procedure with the Output Amplifier.

36.2.2 D/A Control Register (DACR)

Address(es): DAC12.DACR 4005 E004h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAOE1	DAOE0	DAE	—	—	—	—	—
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	DAE	D/A Enable*1	0: Control D/A conversion of channels 0 and 1 individually 1: Control D/A conversion of channels 0 and 1 collectively.	R/W
b6	DAOE0	D/A Output Enable 0	0: Disable analog output of channel 0 (DA0) 1: Enable D/A conversion of channel 0 (DA0).	R/W
b7	DAOE1	D/A Output Enable 1	0: Disable analog output of channel 1 (DA1) 1: Enable D/A conversion of channel 1 (DA1).	R/W

Note 1. This bit controls D/A conversion in combination with the DAOEi bit (i = 0, 1), which controls the output of the conversion results. For details, see Table 36.3.

Table 36.3 D/A conversion controls

b5	b7	b6	
DAE	DAOE1	DAOE0	Description
0	0	0	Disable D/A conversion and analog output pins (DA0, DA1)*1
		1	• Enable D/A conversion of channel 0 and disable D/A conversion of channel 1 • Enable analog output of channel 0 (DA0) and disable analog output of channel 1 (DA1)*1.
	1	0	• Disable D/A conversion of channel 0 and enable D/A conversion of channel 1 • Disable analog output of channel 0 (DA0)*1 and enable analog output of channel 1 (DA1).
		1	• Enable D/A conversion of channels 0 and 1 • Enable analog output of channels 0 and 1 (DA0, DA1).
1	x	x	• Enable D/A conversion of channels 0 and 1 • Collective enable analog output of channels 0 and 1 (DA0, DA1).

x: Don't care

Note 1. When analog output is disabled, the analog output signal is placed in the Hi-Z state.

Only set this register while the ADC12 is halted when the DAADSCR.DAADST bit is 1 (interference prevention between D/A and A/D conversion is enabled). Only set DACR while the ADCSR.ADST bit is 0 and after selecting the software trigger, for the ADC12 trigger to securely stop the ADC12. This MCU only supports ADC12 unit 1.

DAE bit (D/A Enable)

The DAE bit controls D/A conversion, amplifier operation, and analog output in combination with the DAOEi bit (i = 0, 1) and the DAMMPCR.DAAMPi bit (i = 0, 1). See Table 36.4.

When interference prevention between D/A and A/D conversions is enabled (DAADSCR.DAADST = 1), set the ADCSR.ADST bit of the ADC12 to 0. Then, select the software trigger for the ADC12 trigger to securely stop the ADC12.

DAOEi bit (D/A Output Enable i)

The DAOEi bit (i = 0, 1) controls D/A conversion, amplifier operation, and analog output in combination with the DAE bit and DAMMPCR.DAAMPi bit (i = 0, 1). See Table 36.4.

When both the DAOEi (i = 0, 1) and DAE bits are 0, D/A conversion of channel i (i = 0, 1) is not processed, and no conversion result is output.

When interference prevention between D/A and A/D conversions is enabled (DAADSCR.DAADST = 1), set the DAOEi bit while the ADCSR.ADST bit of the ADC12 is 0. Then, select the software trigger for the ADC12 trigger to securely stop the ADC12.

The event link function can be used to set the DAOEi bit to 1. The DAOE0 bit is set to 1 when the event specified in the ELSR12 register of the ELC (ELC_DA0 event) occurs, and output of the D/A conversion results starts. The DAOE1 bit is set to 1 when the event specified in the ELSR13 register of the ELC (ELC_DA1 event) occurs, and output of the D/A conversion results starts.

Table 36.4 D/A conversion and analog output control (1 of 2)

DACR		DAAMPCR			
DAE	DAOEi	DAAMPi	Channel i operation	Amplifier operation of channel i	Analog output of channel i
0	0	0	Stop	Stop	Hi-Z
		1	Stop	Stop	Hi-Z
	1	0	Run	Stop	Amplifier-through
		1	Run	Run	Amplifier output

Table 36.4 D/A conversion and analog output control (2 of 2)

DACR		DAAMPCR			
DAE	DAOEi	DAAMPi	Channel i operation	Amplifier operation of channel i	Analog output of channel i
1	0	0	Run	Stop	Amplifier-through
		1	Run	Run	Amplifier output
	1	0	Run	Stop	Amplifier-through
		1	Run	Run	Amplifier output

i = 0, 1

36.2.3 DADRm Format Select Register (DADPR)

Address(es): DAC12.DADPR 4005 E005h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DPSEL	DADRm Format Select	0: Right-justified format 1: Left-justified format.	R/W

36.2.4 D/A A/D Synchronous Start Control Register (DAADSCR)

Address(es): DAC12.DAADSCR 4005 E006h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAADST	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DAADST	D/A A/D Synchronous Conversion	0: Do not synchronize DAC12 operation with ADC12 (unit 1) operation (disable interference prevention between D/A and A/D conversion) 1: Synchronize DAC12 operation with ADC12 (unit 1) operation (enable interference prevention between D/A and A/D conversion).	R/W

To minimize interference between D/A and A/D conversion, the DAADSCR register enables synchronization of the start timing of D/A conversion with the ADC12 synchronous D/A conversion enable input signal.

Note: This MCU only supports ADC12 unit 1.

Only set this register while the ADC12 is halted, that is, while the ADCSR.ADST bit is 0 after selecting the software trigger as the ADC12 trigger.

Select unit 1 as the target ADC12 unit before setting the DAADST bit to 1. Set bit [1] in the DAADUSR register to 1 to select unit 1.

DAADST bit (D/A A/D Synchronous Conversion)

Setting the DAADST bit to 0 allows the DADRm register value to be converted into analog data at any time. Setting the DAADST bit to 1 allows synchronous D/A conversion with the ADC12 synchronous D/A conversion enable input signal from the ADC12. With this bit set, D/A conversion does not start until the ADC12 completes A/D conversion, even if the

DADRm register value is changed.

Set this bit while the ADCSR.ADST bit is set to 0. Then, select the software trigger for the ADC12 trigger to securely stop the ADC12. Set bit [1] in the DAADUSR register to 1 before setting the DAADST bit to 1.

The event link function cannot be used when the DAADST bit is set to 1. Stop the event link function by setting the ELSR12 and ELSR13 registers of the ELC. The setting of the DAADST bit is shared by channels 0 and 1 of the DAC12.

36.2.5 D/A Output Amplifier Control Register (DAAMPCR)

Address(es): DAC12.DAAMPCR 4005 E008h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAAMP1	DAAMP0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	DAAMP0	Amplifier Control 0	0: Do not use channel 0 output amplifier 1: Use channel 0 output amplifier.	R/W
b7	DAAMP1	Amplifier Control 1	0: Do not use channel 1 output amplifier 1: Use channel 1 output amplifier.	R/W

The DAAMPCR register selects D/A output with or without using the amplifier.

DAAMP0 bit (Amplifier Control 0)

When the DAAMP0 bit is 0, analog values are output for D/A output of channel 0 without using the amplifier. When the DAAMP0 bit is 1, analog values are output for D/A output of channel 0 through the amplifier.

When both the DAE and DAOE0 bits are 0, the amplifier is not used regardless of the setting of the DAAMP0 bit. See Table 36.4 for details.

DAAMP1 bit (Amplifier Control 1)

When the DAAMP1 bit is 0, analog values are output for D/A output of channel 1 without using the amplifier. When the DAAMP1 bit is 1, analog values are output for D/A output of channel 1 through the amplifier.

When both the DAE and DAOE1 bits are 0, the amplifier is not used regardless of the setting of the DAAMP1 bit. See Table 36.4 for details.

36.2.6 D/A Amplifier Stabilization Wait Control Register (DAASWCR)

Address(es): DAC12.DAASWCR 4005 E01Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	DAASW1	DAASW0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	DAASW0	D/A Amplifier Stabilization Wait 0	0: Amplifier stabilization wait off (output) for channel 0 1: Amplifier stabilization wait on (Hi-Z) for channel 0.	R/W
b7	DAASW1	D/A Amplifier Stabilization Wait 1	0: Amplifier stabilization wait off (output) for channel 1 1: Amplifier stabilization wait on (Hi-Z) for channel 1.	R/W

The DAASWCR register controls D/A output with the output amplifier. This register is used in the initialization

procedure to wait for stabilization of the D/A output amplifier. Each bit in DAASWCR should be set to 1 when both the DAE and the DAOEi (i = 0, 1) bits in the DACR register are 0. See section 36.6.5, Initialization Procedure with the Output Amplifier.

DAASW0 bit (D/A Amplifier Stabilization Wait 0)

Set the DAASW0 bit to 1 in the initialization procedure to wait for the stabilization of the D/A channel 0 output amplifier. When DAASW0 is set to 1, D/A conversion operates, but the conversion result of D/A is not output from channel 0. When the DAASW0 bit is 0, the stabilization wait time stops, and the D/A conversion result of channel 0 is output through the output amplifier.

DAASW1 bit (D/A Amplifier Stabilization Wait 1)

Set the DAASW1 bit to 1 in the initialization procedure to wait for the stabilization of the D/A channel 1 output amplifier. When DAASW1 is set to 1, D/A conversion operates, but the conversion result of D/A is not output from channel 1. When the DAASW1 bit is 0, the stabilization wait time stops, and the D/A conversion result of channel 1 is output through the output amplifier.

36.2.7 D/A A/D Synchronous Unit Select Register (DAADUSR)

Address(es): DAC12.DAADUSR 4005 F0C0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AMADSEL1	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	AMADSEL1	A/D Unit 1 Select	0: Do not select unit 1 1: Select unit 1.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DAADUSR register selects the target ADC12 unit for D/A and A/D synchronous conversions. Set bit [1] to 1 to select unit 1 as the target synchronous unit for the MCU. When setting the DAADSCR.DAADST bit to 1 for synchronous conversions, select the target unit in this register in advance.

Only set the DAADUSR register while the ADCSR.ADST bit of the ADC12 is 0 and the DAADSCR.DAADST bit is set to 0.

36.3 Operation

DAC12 includes D/A conversion circuits for two channels, each of which can operate independently. When the DAOEn bit (n = 0, 1) in DACR is set to 1, DAC12 is enabled and the conversion result is output.

The following example shows D/A conversion on channel 0. Figure 36.2 shows the timing of this operation.

To process D/A conversion on channel 0:

1. Set the data for D/A conversion in the DADPR.DPSEL bit and the DADR0 register.
2. Set the DACR.DAOE0 bit to 1 to start D/A conversion. The conversion result is output from the analog output pin DA0 after the conversion time tDCONV elapses. The conversion result continues to be output until DADR0 is written to again or the DAOE0 bit is set to 0. The output value (reference) is expressed by the following formula:

$$\frac{\text{Setting in DADRm}}{4096} \times \text{VREFH}$$

3. To start another conversion, write another value to DADR0. The conversion result is output after the conversion time t_{DCONV} elapses.
   When the DAADSCR.DAADST bit is 1 (interference reduction between D/A and A/D conversion is enabled), a

maximum of one A/D conversion time is required for D/A conversion to start. When ADCLK is faster than the peripheral clock, a longer time period might be required.

4. To disable analog output, set the DAOE0 bit to 0.

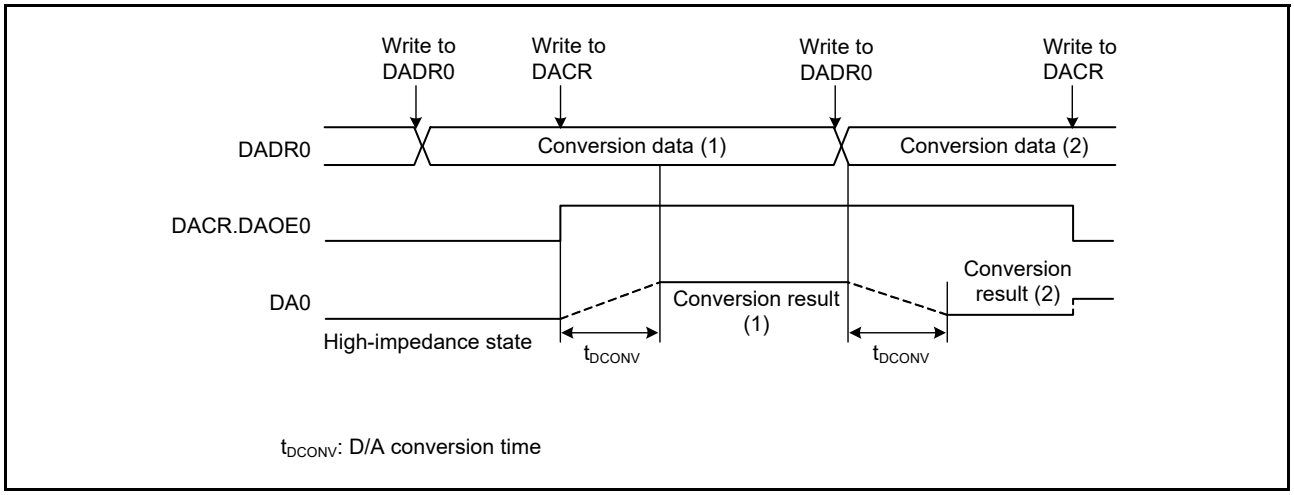


Figure 36.2 Example of DAC12 operation

36.3.1 Reducing Interference between D/A and A/D Conversion

When D/A conversion starts, the DAC12 generates inrush current. Because the DAC12 and ADC12 share the same analog power supply, the generated inrush current can interfere with ADC12 operation.

While the DAADSCR.DAADST bit is 1, even if the DADRm register data is changed during ADC12 operation, D/A conversion does not start immediately but starts synchronously with A/D conversion completion. A maximum of one A/D conversion time is required for the DADRm register data update to be reflected as the D/A conversion circuit input. Before reflection, the DADRm register value does not correspond to the analog output value.

When this function is enabled, it is not possibles to check through software whether the DADRm register value was D/A converted. When the DADRm register data is changed while the ADC12 is halted, D/A conversion starts in 1 PCLKB cycle, even if DAADSCR.DAADST is 1.

The following sequence provides an example of channel 0 D/A conversion, in which the DAC12 operates synchronously with the ADC12.

To perform D/A conversion on channel 0 in synchronization with the ADC12:

1. Confirm that the ADC12 is halted and set the DAADUSR.AMADSEL1 bit to 1.
2. Confirm that the ADC12 is halted and set the DAADSCR.DAADST bit to 1.
3. Confirm that the ADC12 is halted and set the DACR.DAOE0 bit to 1.
4. Set the DADR0 register. If ADCLK is faster than the peripheral clock, a period longer than one A/D conversion time might be required.

- If the 12-bit A/D conversion is halted (ADCSR.ADST bit = 0) when the DADR0 register is modified, D/A conversion starts in 1 PCLKB cycle
- If the 12-bit A/D conversion is in progress (ADCSR.ADST bit = 1) when the DADR0 register is modified, D/A conversion starts on A/D conversion completion. If the DADR0 register is modified twice during A/D conversion, the first update might not be converted.

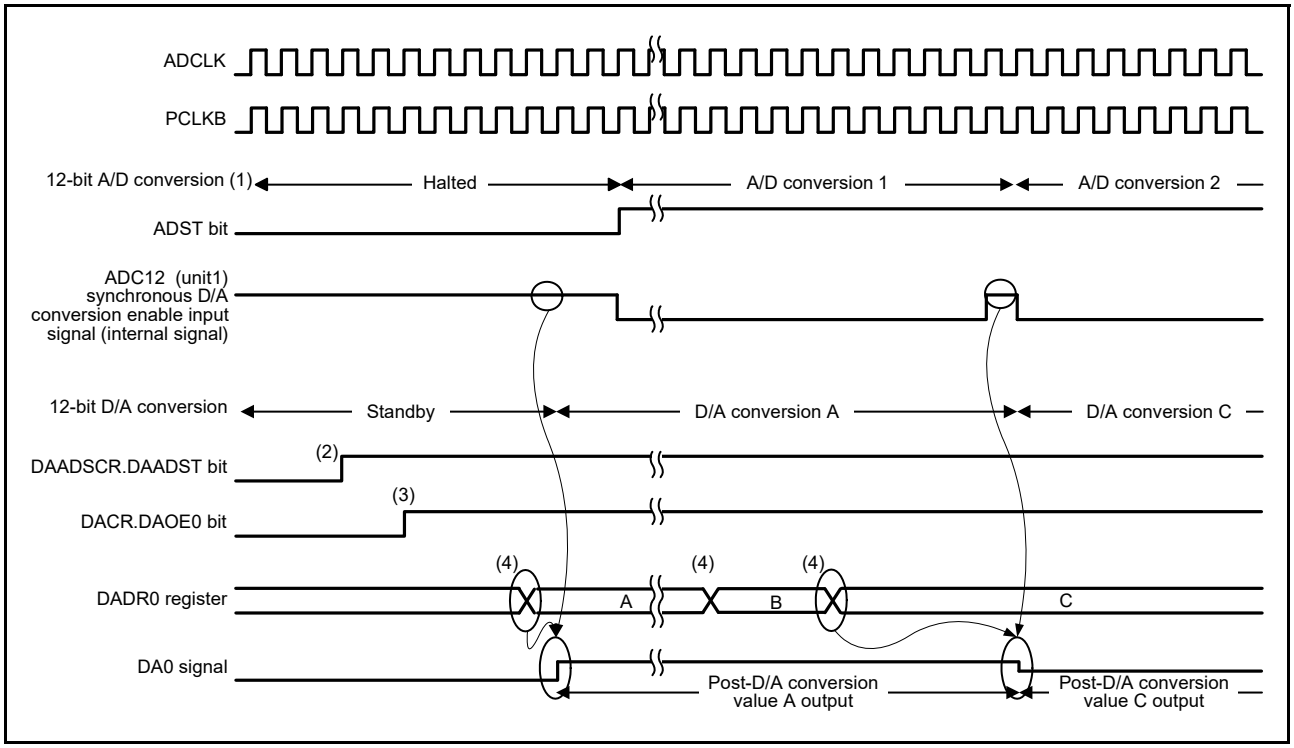


Figure 36.3 Example of conversion when the DAC12 is synchronized with the ADC12

When ADCLK is faster than PCLKB, the DAC12 might not be able to capture an ADC12 synchronous D/A conversion enable input signal during the 1 ADCLK cycle that is output between A/D conversion 1 and A/D conversion 2, as shown in Figure 36.4. In this case, post-D/A conversion value A is continuously output as the DA0 signal.

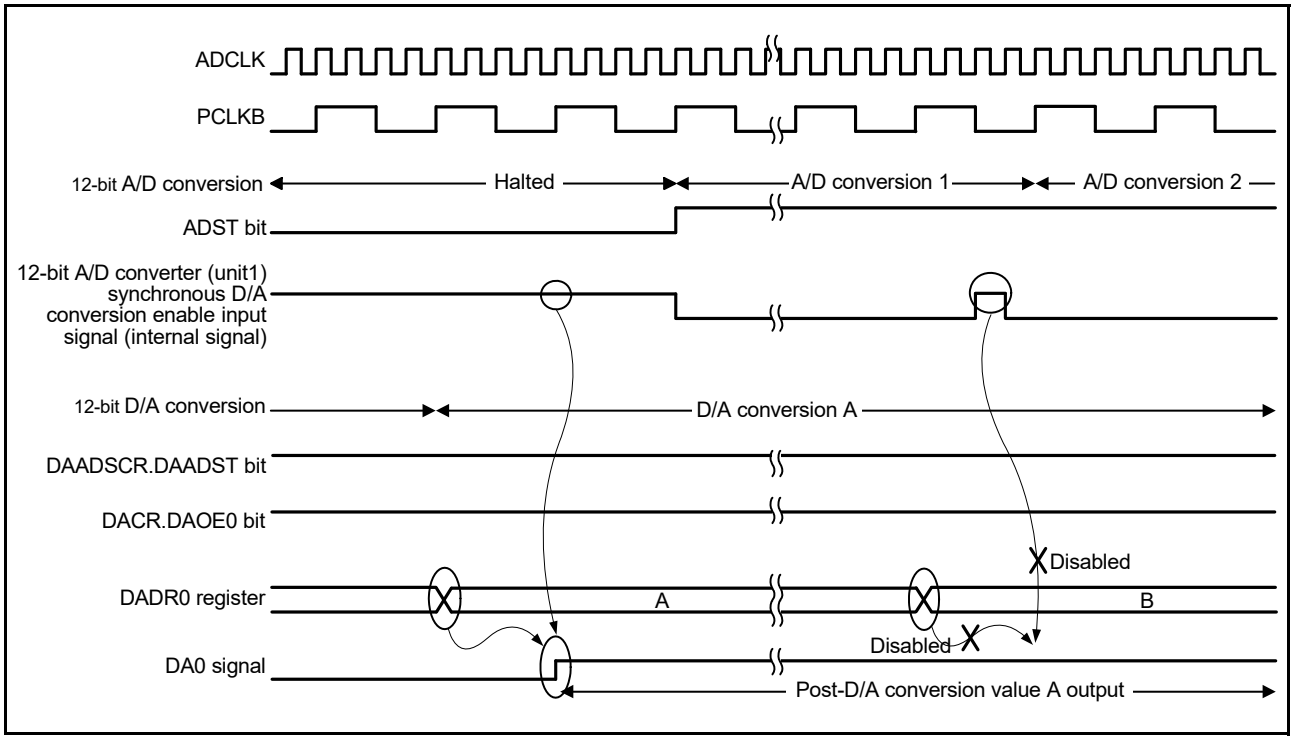


Figure 36.4 Example when the DAC12 cannot capture the synchronous D/A conversion enable input signal from the ADC12 (unit 1)

36.4 Event Link Operation Setting Procedure

This section describes the procedures used in event link operation.

36.4.1 DA0 Event Link Operation Setting Procedure

To set up DA0 event link operation:

1. Set the DADPR.DPSEL bit and the data for D/A conversion in the DADR0 register.
2. Set the ELC_DA0 event signal to be linked to each peripheral module in the ELSR12 register.
3. Set the ELCR.ELCON bit to 1. This enables event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE0 bit is set to 1, and D/A conversion starts on channel 0.
5. Set the ELSR12.ELS[8:0] bits to 000h to stop event link operation on DAC12 channel 0. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

36.4.2 DA1 Event Link Operation Setting Procedure

To set up DA1 event link operation:

1. Set the DADPR.DPSEL bit and set the data for D/A conversion in the DADR1 register.
2. Set the ELC_DA1 event signal to be linked to each peripheral module in the ELSR13 register.
3. Set the ELCR.ELCON bit to 1. This enables the event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE1 bit is set to 1, and D/A conversion starts on channel 1.
5. Set the ELSR13.ELS[8:0] bits to 000h to stop event link operation on DAC12 channel 1. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

36.5 Usage Notes on Event Link Operation

- When the event link function is used, do not use the amplifier output function.
- When the event link function is used, set the DACR.DAE bit to 0.
- When the event specified for the ELC_DA0 event signal is generated while a write to the DACR.DAOE0 bit is performed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- When the event specified for the ELC_DA1 event signal is generated while a write to the DACR.DAOE1 bit is performed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- Use of the event link function is prohibited when the DAADSCR.DAADST bit is set to 1 to reduce interference between D/A and A/D conversions.

36.6 Usage Notes

36.6.1 Settings for the Module-Stop Function

The Module Stop Control Register can enable or disable DAC12 operation. The DAC12 is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

36.6.2 DAC12 Operation in the Module-Stop State

When the MCU enters the module-stop state with D/A conversion enabled, the D/A outputs is saved, and the analog power supply current is the same as during D/A conversion. To reduce the analog power supply current in the module-stop state, disable D/A conversion by setting the DACR.DAOE1, DAOE0, and DAE bits to 0.

36.6.3 DAC12 Operation in Software Standby Mode

When the MCU enters Software Standby mode with D/A conversion enabled, the D/A outputs are saved, and the analog power supply current is the same as during D/A conversion. To reduce the analog power supply current in Software Standby mode, disable D/A conversion by setting the DACR.DAOE1, DAOE0, and DAE bits to 0.

36.6.4 Restriction on Entering Deep Software Standby Mode

When the MCU enters Deep Software Standby mode with D/A conversion enabled, the outputs of DAC12 are placed in a high impedance state.

36.6.5 Initialization Procedure with the Output Amplifier

Use the following initialization procedures with the output amplifier. The example shows the case for channel 0.

To initialize the DAC12 with the output amplifier:

1. Write 000h to the DADR0 register.
2. Set the DAASWCR.DAASW0 bit to 1.
3. Set the DAAMPCR.DAAMP0 bit to 1.
4. Set the DACR.DAE bit or the DACR.DAOE0 bit to 1 to start operation of the amplifier.
5. Set the DAASWCR.DAASW0 bit to 0 after waiting for the duration of D/A conversion time t_{CONV}.
6. Write the value to be converted in the DADR0 register.

While the amplifier is running, setting the DACR.DAE and DACR.DAOE0 bits to 0 allows the amplifier to stop operation. To use the amplifier again, repeat steps 1. to 6.

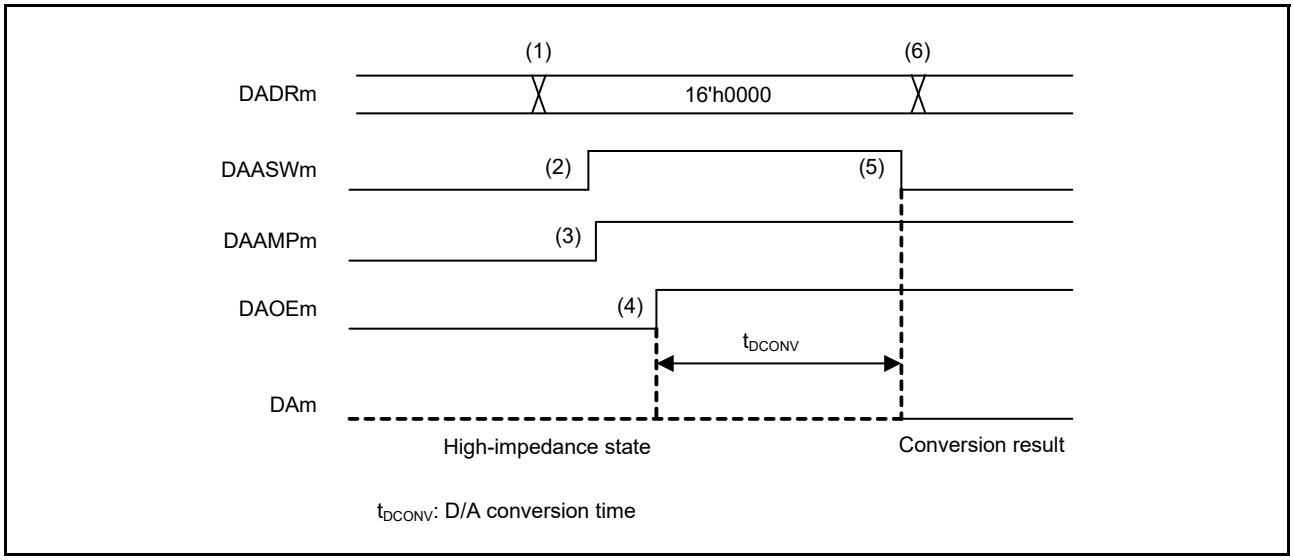


Figure 36.5 Example of the initial flow with the output amplifier in DAC12

36.6.6 Restriction on Usage when Interference Reduction between D/A and A/D Conversion is Enabled

When the DAADSCR.DAADST bit is 1, enabling interference prevention between D/A and A/D conversion, do not place the ADC12 in the module-stop state. Doing so can halt D/A conversion in addition to A/D conversion.

37. Temperature Sensor (TSN)

37.1 Overview

The on-chip temperature sensor determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application.

Table 37.1 lists the temperature sensor specifications and Figure 37.1 shows a block diagram.

Table 37.1 Temperature sensor specifications

Parameter	Specifications
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-Bit A/D Converter (ADC12)
Module-stop function	Module-stop state can be set to reduce power consumption
Temperature Sensor Calibration Data	Reference data measured for each chip at factory shipment is stored

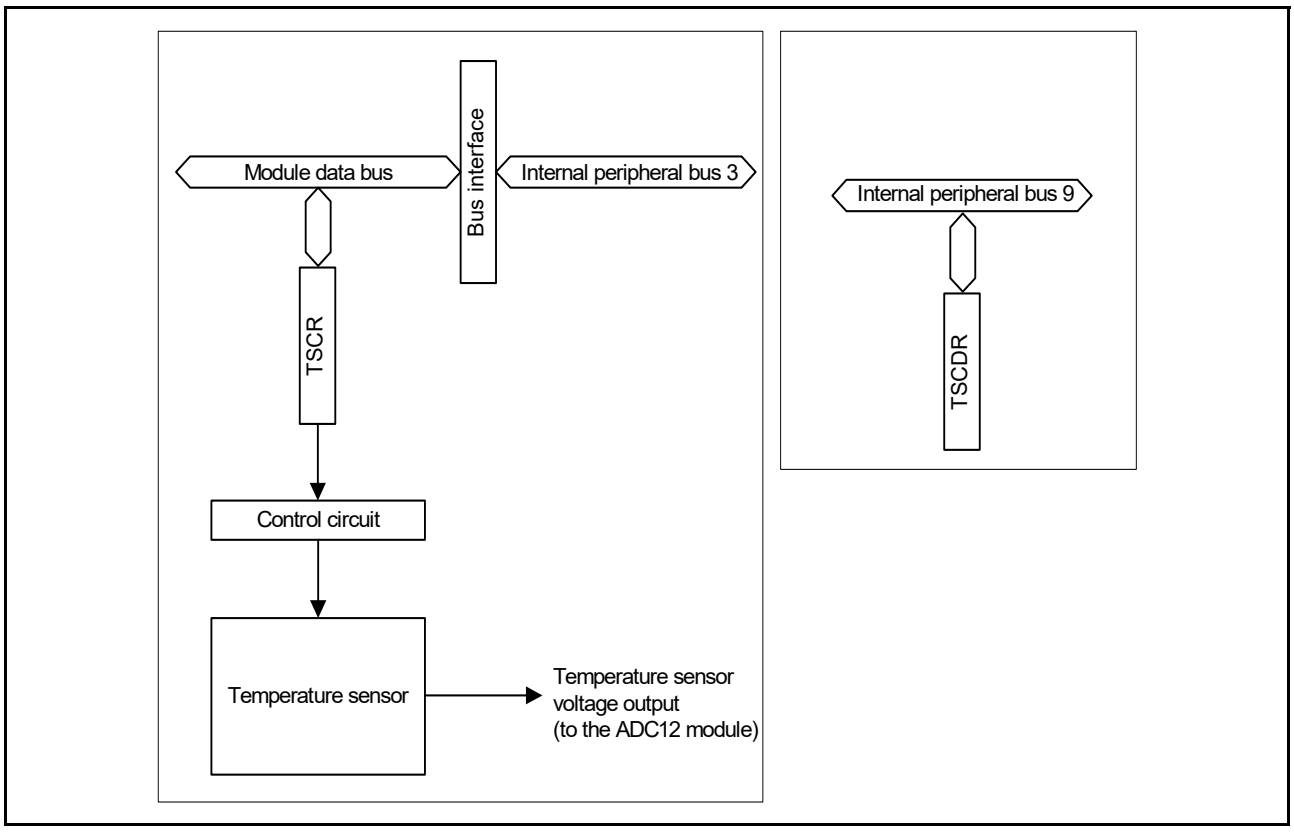


Figure 37.1 Temperature sensor block diagram

37.2 Register Descriptions

37.2.1 Temperature Sensor Control Register (TSCR)

Address(es): TSN.TSCR 4005 D000h

	b7	b6	b5	b4	b3	b2	b1	b0
	TSEN	—	—	TSOE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TSOE	Temperature Sensor Output Enable	0: Disable output from the temperature sensor to the ADC12 1: Enable output from the temperature sensor to the ADC12.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TSEN	Temperature Sensor Enable	0: Stop the temperature sensor 1: Start the temperature sensor.	R/W

The timing constraints shown in Figure 37.3 apply to the settings of the TSCR register.

37.2.2 Temperature Sensor Calibration Data Register (TSCDR)

Address(es): TSD.TSCDR 407F B17Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—												
Value after reset:	0	0	0	0	Unique value for each chip											

The TSCDR register stores temperature sensor calibration data measured for each MCU at factory shipment.

Temperature sensor calibration data is a digital value obtained using the 12-bit A/D converter unit 0 to convert the voltage output by the temperature sensor under the condition $T_a = T_j = 127°C$ and AVCC0 = 3.3 V.

The TSCDR register is a 32-bit read-only register and should be read in 32-bit units.

37.3 Using the Temperature Sensor

The temperature sensor outputs a voltage that varies with the temperature. This voltage is converted to a digital value by the ADC12. To obtain the die temperature, convert this value into the temperature.

37.3.1 Preparation for Using the Temperature Sensor

The temperature (T) is proportional to the sensor voltage output (Vs), so temperature is calculated with the following formula:

T = (Vs - V1) / slope + T1

T: Measured temperature (°C)

Vs: Voltage output by the temperature sensor when temperature is measured (V)

T1: Temperature experimentally measured at one point (°C)

V1: Voltage output by the temperature sensor when T1 is measured (V)

T2: Temperature experimentally measured at a second point (°C)

V2: Voltage output by the temperature sensor when T2 is measured (V)

Slope: Temperature gradient of the temperature sensor (V /°C), slope = (V2 - V1) / (T2 - T1)

Characteristics vary between sensors. Therefore, Renesas recommends measuring two different sample temperatures as follows:

1. Use the ADC12 to measure the voltage V1 output by the temperature sensor at temperature T1.
2. Use the ADC12 to measure the voltage V2 output by the temperature sensor at a different temperature T2. Obtain the temperature gradient (slope = (V2 - V1) / (T2 - T1)) from these results.
3. Subsequently, obtain temperatures by substituting the slope into the formula for the temperature characteristic (T = (Vs - V1) / slope + T1).

If you are using the temperature slope given in Table 43.32 of section 43, Electrical Characteristics, use the ADC12 converter unit 0 to measure the voltage V1 output by the temperature sensor at temperature T1, then calculate the temperature characteristic using the following formula:

T = (Vs - V1) / slope + T1

T: Measured temperature (°C)

Vs: Voltage output by the temperature sensor when the temperature is measured (V)

T1: Sample temperature measurement at first point (°C)

V1: Voltage output by the temperature sensor when T1 is measured (V)

Slope: Temperature slope given in Table 43.32 ÷ 1000 (V / °C)

In this MCU, the TSCDR register stores the temperature value (CAL127) of the temperature sensor measured under the condition $T_a = T_j$ = 127°C and AVCC0 = 3.3 V. By using this value as the sample measurement result at the first point, you can omit the preparation before using the temperature sensor.

V1 is calculated from CAL127 as follows:

V1 = 3.3 × CAL127 / 4096 [V]

Using this value, the measured temperature can be calculated according to the following formula:

T = (Vs - V1) / slope + 127 [°C]

T: Measured temperature (°C)

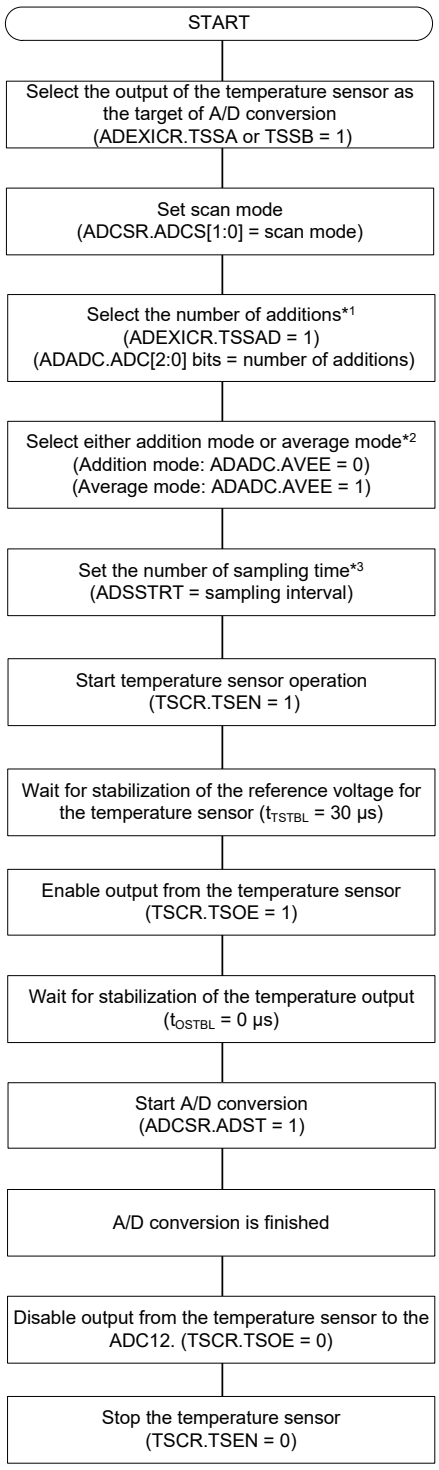
Vs: Voltage output by the temperature sensor when the temperature is measured (V)

V1: Voltage output by the temperature sensor when $T_a = T_j$ = 127°C and AVCC0 = 3.3 V (V)

Slope: Temperature slope given in Table 43.32 ÷ 1000 (V / °C)

37.3.2 Procedure for Using the Temperature Sensor

Figure 37.2 shows the procedure for using the temperature sensor. For the procedure to configure the ADC12, see section 35, 12-Bit A/D Converter (ADC12).



Note 1. The ADADC.ADC[2:0] setting is limited to some values in average mode. For details on the available ADADC.ADC[2:0] settings in average mode, see section 35.2.10, A/D-Converted Value Addition/Average Count Select Register (ADADC).
Note 2. This setting is not required if addition/average mode is not set.
Note 3. Set the sampling time to more than the value described in section 43.6, TSN Characteristics.

Figure 37.2 Procedure for using the temperature sensor

Figure 37.3 shows the timing from the start of temperature sensor operation until the completion of A/D conversion when the ADC12 is in single scan mode (the conversion target is the temperature sensor output only). The times shown in the figure are described in Table 37.2.

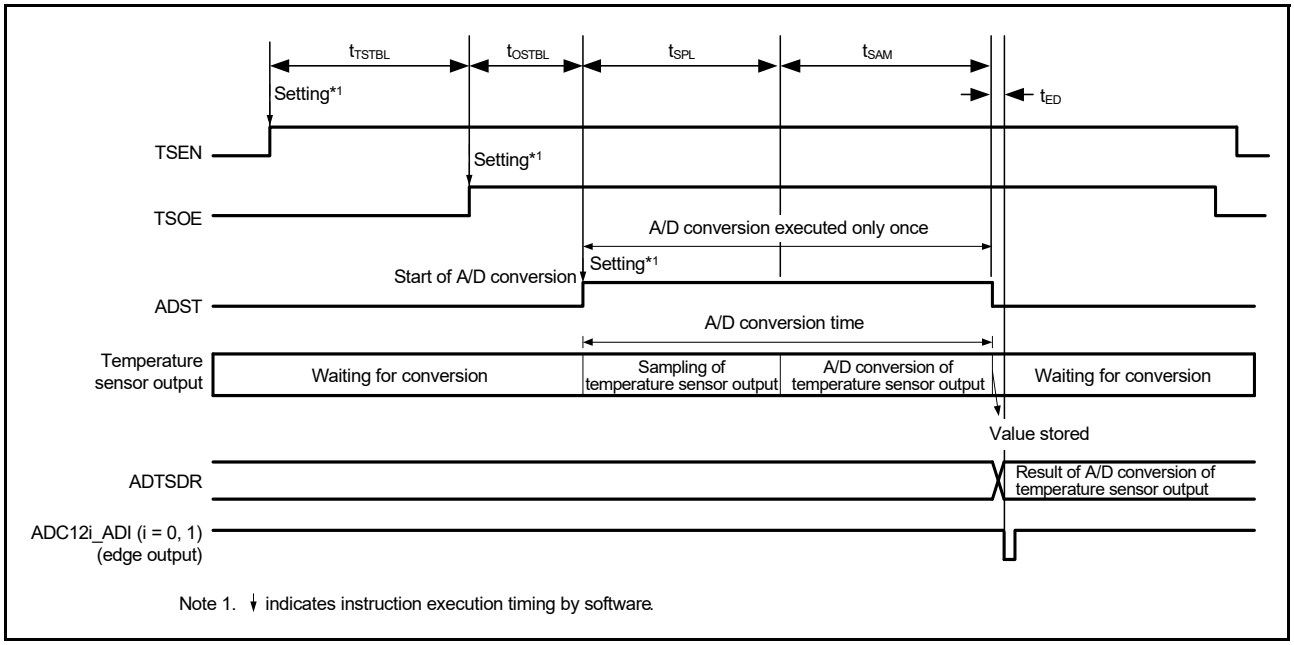


Figure 37.3 Timing from start of temperature sensor operation until completion of A/D conversion

Table 37.2 Time until completion of A/D conversion after start of temperature sensor operation

Parameter	Symbol	Time
Wait time for temperature sensor reference voltage stabilization	t_{TSTBL}	30 µs (min)
Wait time for temperature sensor output stabilization	t_{OSTBL}	0 µs (min)
ADC12 input sampling time	t_{SPL}	ADSSTRT setting × ADCLK cycles
A/D conversion time	t_{SAM}	See Table 35.10, Conversion times during scanning (in numbers of ADCLK and PCLKB cycles)
Scan conversion end delay	t_{ED}	

37.4 Usage Notes

37.4.1 Settings for the Module-Stop Function

The Module Stop Control Register D (MSTPCRD) can enable or disable temperature sensor operation. The temperature sensor is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

37.4.2 Constraints

It is prohibited to use both channels of the ADC12 simultaneously for temperature sensor measurement.

38. High-Speed Analog Comparator (ACMPHS)

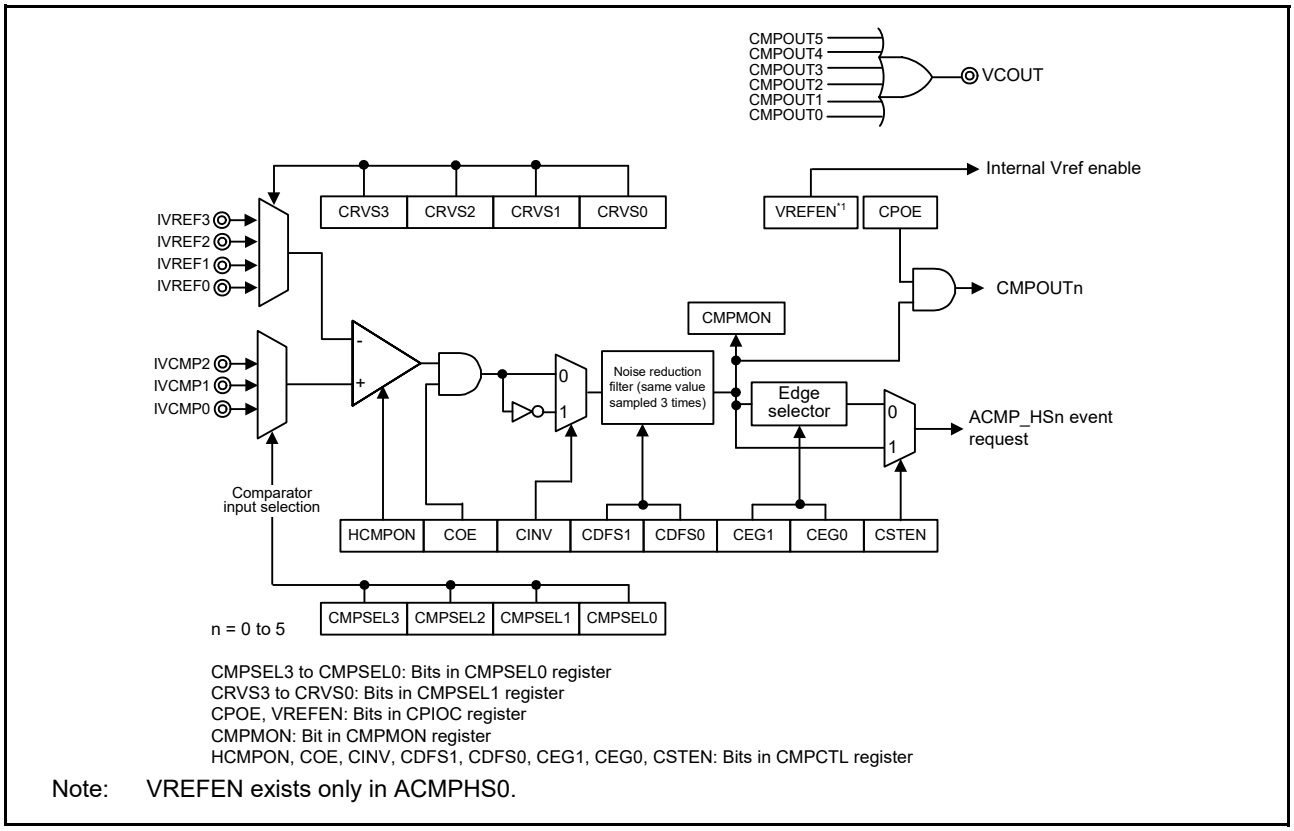
38.1 Overview

The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the result of conversion. Both the test voltage and the reference voltage can be provided to the ACMPHS from internal sources (D/A converter output and internal reference voltage) and an external source (with or without an internal PGA). Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion.

Table 38.1 lists the ACMPHS specifications, Figure 38.1 shows a block diagram, and Table 38.2 shows the input source configuration of the ACMPHS.

Table 38.1 ACMPHS 0 to 5 specifications

Parameter	Specifications
Number of channels	6 channels: ACMPHS 0 to ACMPHS 5
Analog input voltage	• Output from internal PGA • Output from internal D/A converter • Input from internal A/D converter input pin (one selectable).
Reference voltage	• Internal reference voltage (Vref) • Output from internal D/A converter • Input from internal A/D converter input pin (one selectable).
ACMPHS output	• Comparison result • Generation of ELC event output • Monitor output from register.
Interrupt request signal	• Interrupt request generated on valid edge detection from comparison result • Rising edge, falling edge, or both edges can be selected.
Digital filter function	• One of three sampling frequencies can be selected • Not using the filter function can be selected.



Note: VREFEN exists only in ACMPHS0.

Figure 38.1 ACMPHS block diagram

Table 38.2 Input source configuration of the ACMPHS

	Reference voltage input source				Analog voltage input source				
Comparator	IVREF3	IVREF2	IVREF1	IVREF0	IVCMP3	IVCMP2	IVCMP1	IVCMP0	Optput pin
ACMPHS0	DA0*1	Vref*2	AN116	AN016	PGA0 output*6	AN000*3,*6	DA1*4	AN017	VCOUT*5
ACMPHS1	DA0*1	Vref*2	AN116	AN016	PGA1 output*6	AN001*3,*6	DA1*4	AN017	
ACMPHS2	DA0*1	Vref*2	AN116	AN016	PGA2 output*6	AN002*3,*6	DA1*4	AN017	
ACMPHS3	DA0*1	Vref*2	AN116	AN016	PGA3 output*6	AN100*3,*6	DA1*4	AN017	
ACMPHS4	DA0*1	Vref*2	AN116	AN016	PGA4 output*6	AN101*3,*6	DA1*4	AN017	
ACMPHS5	DA0*1	Vref*2	AN116	AN016	PGA5 output*6	AN102*3,*6	DA1*4	AN017	

Note 1. When D/A converter 0 output is not used, the signal can be used as AN005/AN105 analog input.
Note 2. Internal voltage reference.
Note 3. Because input is through PGA, the corresponding module-stop bit, MSTPCRD.MSTPD16 (unit 0) or MSTPCRD.MSTPD15 (unit 1) should be set to 0.
Note 4. When D/A converter 1 output is not used, the signal can be used as AN006/AN106 analog input.
Note 5. ACMPHS0 to ACMPHS5 compare outputs are bundled with the VCOUT pin.
Note 6. Setting of ADC12 is required. For details, see section 35.6.8, Available functions and register settings of AN000 to AN002, AN007, AN100 to AN102, and AN107.

38.2 Register Descriptions

38.2.1 Comparator Control Register (CMPCTL)

Address(es): ACMPHS0.CMPCTL 4008 5000h,ACMPHS1.CMPCTL 4008 5100h, ACMPHS2.CMPCTL 4008 5200h, ACMPHS3.CMPCTL 4008 5300h, ACMPHS4.CMPCTL 4008 5400h, ACMPHS5.CMPCTL 4008 5500h

	b7	b6	b5	b4	b3	b2	b1	b0
	HCMPON	CDFS[1:0]		CEG1	CEG0	CSTEN	COE	CINV
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CINV	Comparator Output Polarity Selection*2, *3	0: Do not invert comparator output 1: Invert comparator output.	R/W
b1	COE	Comparator Output Enable	0: Disable comparator output (output signal is low level) 1: Enable comparator output.	R/W
b2	CSTEN	Interrupt Select*1	0: Output through the edge selector 1: Output directly.	R/W
b4, b3	CEG1/CEG0	Selection of Valid Edge (Edge Selector)	b4 b3 0 0: Do not detect edge 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges.	R/W
b6, b5	CDFS[1:0]	Noise Filter Selection*1, *2, *3, *4	b6 b5 0 0: Do not use noise filter. 0 1: Use noise filter sampling frequency of PCLKB/2^3 1 0: Use noise filter sampling frequency of PCLKB/2^4 1 1: Use noise filter sampling frequency of PCLKB/2^5.	R/W
b7	HCMPON	Comparator Operation Control*5	0: Stop operation (comparator outputs a low-level signal) 1: Enable operation (enables input to the comparator pins).	R/W

Note 1. Set the CSTEN bit to 1 and the CDFS[1:0] bits to 00b if the ACMPHS interrupt causes the release of Software Standby or Snooze modes. CTSEN is supported only by the ACMPHS0. ACMPHSn.CMPCTL.CTESN (n = 1 to 5) must be set to 0.
Note 2. Disable the ACMPHS output (COE = 0) before changing the CDFS[1:0] and CINV bits.
Note 3. If the CDFS[1:0] and CINV bits are changed, an ACMPHS interrupt request and an ELC event might be generated. Before changing these bits, set the ELSRn register to 0 (the ACMPHS output is not linked). After changing these bits, clear the IR flag in the IELSRn register to 0 to clear the interrupt status.
Note 4. If the CDFS[1:0] bits are changed from 00b (noise filter not used) to a value other than 00b (noise filter used), perform sampling

four times and update the filter output, then use the ACMPHS interrupt request or the ELC event.

Note 5. A stabilization wait time is required to permit ACMPHS operation after enabling it (HCMPON = 1). The operation stabilization wait time for ACMPHS modules 0 to 5 is 300 ns.

The CMPCTL register controls the ACMPHS operation, enables or disables the ACMPHS output, selects the noise filter, selects the valid edge of the interrupt signal, and selects the interrupt. A reset clears this register to 00h.

38.2.2 Comparator Input Select Register (CMPSEL0)

Address(es): ACMPHS0.CMPSEL0 4008 5004h, ACMPHS1.CMPSEL0 4008 5104h, ACMPHS2.CMPSEL0 4008 5204h, ACMPHS3.CMPSEL0 4008 5304h, ACMPHS4.CMPSEL0 4008 5404h, ACMPHS5.CMPSEL0 4008 5504h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CMPSEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CMPSEL[3:0]	Comparator Input Selection*1	b3 b0 0 0 0 0: Do not input 0 0 0 1: Select IVCMP0*2 0 0 1 0: Select IVCMP1*2 0 1 0 0: Select IVCMP2*2 1 0 0 0: Select IVCMP3*2. Other settings are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use the following procedure to change the CMPSEL[3:0] bits. Writing a value other than 0000 0000b while the value of the CMPSEL0 register is not 0000 0000b is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is retained.

To change the CMPSEL[3:0] bits:

1. Set the CMPCTL.COE bit to 0.
2. Set the CMPSEL0 register to 0000 0000b.
3. Set a new value in the CMPSEL[3:0] bits, with 1 set in only one of the bits.
4. Wait for the input switching stabilization wait time (200 ns).
5. Set the CMPCTL.COE bit to 1.
6. Clear the IR flag in the IELSRn register to clear the interrupt status.

Note 2. For details, see Table 38.2.

38.2.3 Comparator Reference Voltage Select Register (CMPSEL1)

Address(es): ACMPHS0.CMPSEL1 4008 5008h, ACMPHS1.CMPSEL1 4008 5108h, ACMPHS2.CMPSEL1 4008 5208h, ACMPHS3.CMPSEL1 4008 5308h, ACMPHS4.CMPSEL1 4008 5408h, ACMPHS5.CMPSEL1 4008 5508h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CRVS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CRVS[3:0]	Reference Voltage Selection*1	b3 b0 0 0 0 0: Do not input 0 0 0 1: Select IVREF0*2 0 0 1 0: Select IVREF1*2 0 1 0 0: Select IVREF2*2 1 0 0 0: Select IVREF3*2. Other settings are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use the following procedure to change the CRVS[3:0] bits. Writing a value other than 0000 0000b while the value of the CMPSEL1 register is not 0000 0000b is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is

retained.
To change the CRVS[3:0] bits:
1. Set the CMPCTL.COE bit to 0.
2. Set the CMPSEL1 register to 0000 0000b.
3. Set a new value to the CRVS[3:0] bits, with 1 set in only one of the bits.
4. Wait for the input switching stabilization wait time (200 ns)
5. Set the CMPCTL.COE bit to 1.
6. Clear the IR flag in the IELSRn register to clear the interrupt status.

Note 2. For details, see Table 38.2.

38.2.4 Comparator Output Monitor Register (CMPMON)

Address(es): ACMPHS0.CMPMON 4008 500Ch, ACMPHS1.CMPMON 4008 510Ch, ACMPHS2.CMPMON 4008 520Ch, ACMPHS3.CMPMON 4008 530Ch, ACMPHS4.CMPMON 4008 540Ch, ACMPHS5.CMPMON 4008 550Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPMON
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPMON	Comparator Output Monitor*1	0: Comparator output is low 1: Comparator output is high.	R
b7 to b1	—	Reserved	These bits are read as 0.	R

Note 1. When ACMPHS operation is enabled (HCMPON = COE = 1) but the noise filter is not in use (CDFS[1:0] = 00b), design the software application so that the CMPMON bit is read twice and the values are only used after the two consecutive values match.

38.2.5 Comparator Output Control Register (CPIOC)

Address(es): ACMPHS0.CPIOC 4008 5010h, ACMPHS1.CPIOC 4008 5110h, ACMPHS2.CPIOC 4008 5210h, ACMPHS3.CPIOC 4008 5310h, ACMPHS4.CPIOC 4008 5410h, ACMPHS5.CPIOC 4008 5510h

	b7	b6	b5	b4	b3	b2	b1	b0
	VREFEN	—	—	—	—	—	—	CPOE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CPOE	Comparator Output Selection	0: Disable VCOUT pin output of the comparator (output signal is low) 1: Enable VCOUT pin output of the comparator.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	VREFEN	Internal Vref Enable*1	0: Disable internal Vref 1: Enable internal Vref.	R/W

Note 1. For ACMPHS modules 0 to 5, VREFEN exists only in ACMPHS0.CPIOC. When using the internal Vref in COMP0 to COMP5, set the VREFEN bit in ACMPHS0.CPIOC to 1. Bit [7] in ACMPHS1.CPIOC to ACMPHS5.CPIOC registers should be 0 regardless of whether or not the internal Vref is used.

38.3 Operation

The ACMPHS compares a reference voltage to an analog input voltage. Operation is not guaranteed when the values of registers are changed during ACMPHS operation. Table 38.3 shows the procedure for setting the registers associated with ACMPHS.

Table 38.3 Procedure for setting registers associated with ACMPHSn (n = 0 to 5)

Step	Register	Bit	Setting
1	Associated MSTPCRD register	MSTPD28 to MSTPD23	0: Input clock supply.
2	Associated Pin Function Control Register (PFS)	ASEL	1: Select the function of pins IVREF and IVCMP.
3	ACMPHS0.CPIOC	VREFEN	1: When using the internal Vref.
4	Associated D/A converter		When using the D/A converter, select in the register
5	CMPSEL0, CMPSEL1	CMPSEL0 to CMPSEL3, CRVS0 to CRVS3	Select the ACMPHSn input, with 1 set in only one of the bits
6	CMPCTL	CDFS[1:0], CEG1, CEG0, and CINV	Set up ACMPHSn control
		HCMPON	1: Enable ACMPHSn operation.
7	Waiting for the ACMPHS stabilization time (minimum 300 ns).		
8	CMPCTL	COE	1: Enable ACMPHSn output.
9	CPIOC	CPOE	Set the VCOUT output
	Associated Port mn Pin Function Select register (PmnPFS)	PSEL, PMR	Select the VCOUT port function
10	IELSRn	IR, IELS[8:0]	When using an interrupt, select the interrupt status flag and the ICU event link*1
11	ELSRn	ELS[8:0]	When using an ELC, select the event link*2
12	Operation started		
13	CMPCTL	COE	0: When changing IVREF or IVCMP, to disable ACMPHSn output.
14	CMPSEL1	CRVS0 to CRVS3	Change the CMPSEL1 bits as follows: 1. Set bits CMPSEL1 to 0000 0000b. 2. Set a new value to the CMPSEL1 bits, with 1 set in only one of the bits.
	CMPSEL0	CMPSEL0 to CMPSEL3	Change the CMPSEL0 bits as follows: 1. Set bits CMPSEL0 to 0000 0000b. 2. Set a new value to the CMPSEL0 bits, with 1 set in only one of the bits.
15	Waiting for the ACMPHS switching stabilization time (minimum 200 ns)		
16	CMPCTL	COE	1: Enable ACMPHSn output.
17	Operation restarted		

Note 1. After ACMPHSn is set, an unnecessary interrupt might occur until operation becomes stable, so initialize the interrupt flag.
Note 2. After ACMPHSn is set, an unnecessary interrupt might occur until operation becomes stable, so initialize the event link select.

Figure 38.2 shows an example of ACMPHS operation. The VCOUT output becomes 1 when the analog input voltage is higher than the ACMPHS reference input voltage, and the VCOUT output becomes 0 when the analog input voltage is lower than the reference voltage. When the ACMPHS output changes, an interrupt request and an ELC event are output.

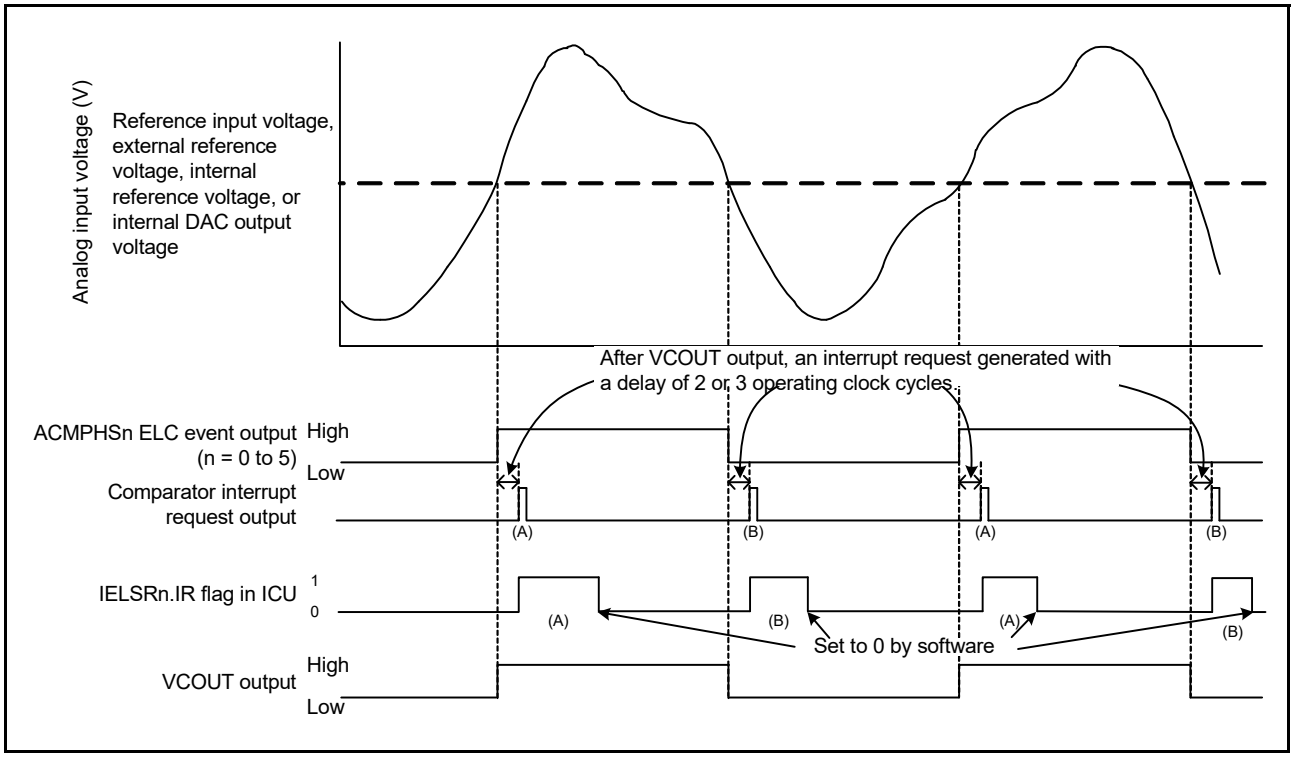


Figure 38.2 ACMPHS operation example

Figure 38.2 applies when CPOE = 1 (pin output enabled), CDFS[1:0] = 00b (filter not used), and CEG1 = CEG0 = 1 (both-edge detection selected). When CINV = 0, CEG0 = 1, and CEG1 = 0 (rising-edge detection selected for non-inversion output signal from the ACMPHS), the IELSR.IR flag changes as shown by (A) only. When CINV = 0, CEG0 = 0, and CEG1 = 1 (falling-edge detection selected for non-inversion output signal from the ACMPHS), the IR flag changes as shown by (B) only. When CPOE = 1, VCOUT directly outputs the ELC event output.

38.4 Noise Filter

The ACMPHS contains a noise filter. The sampling clock can be selected in the CMPCTL.CDFS[1:0] bits. The ACMPHS signal is sampled every sampling clock, and if the same value is sampled three times, the noise filter output at the next sampling clock cycle is used as the ACMPHS output.

Figure 38.3 shows the configuration of the noise filter and edge detector, and Figure 38.4 shows an example of the noise filter and interrupt operation.

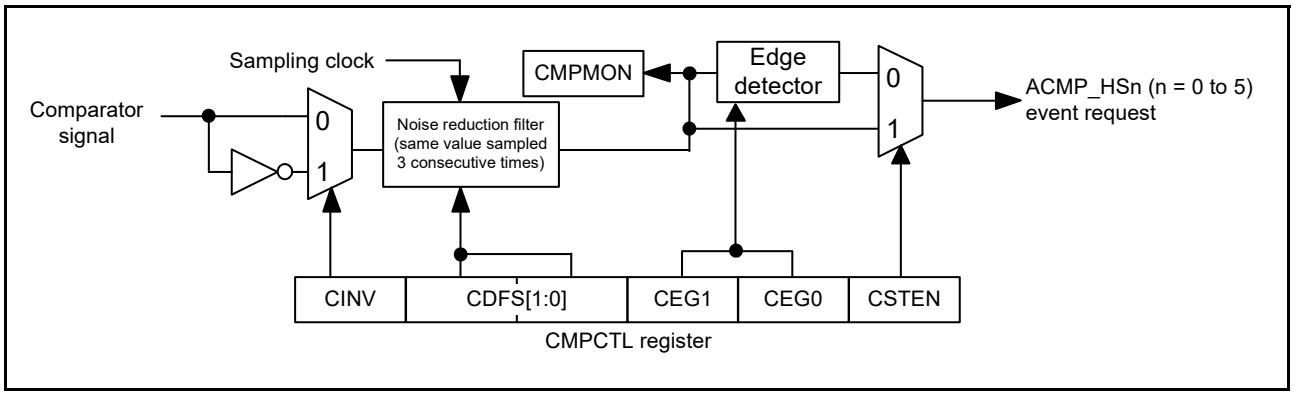


Figure 38.3 Noise filter and edge detection configuration

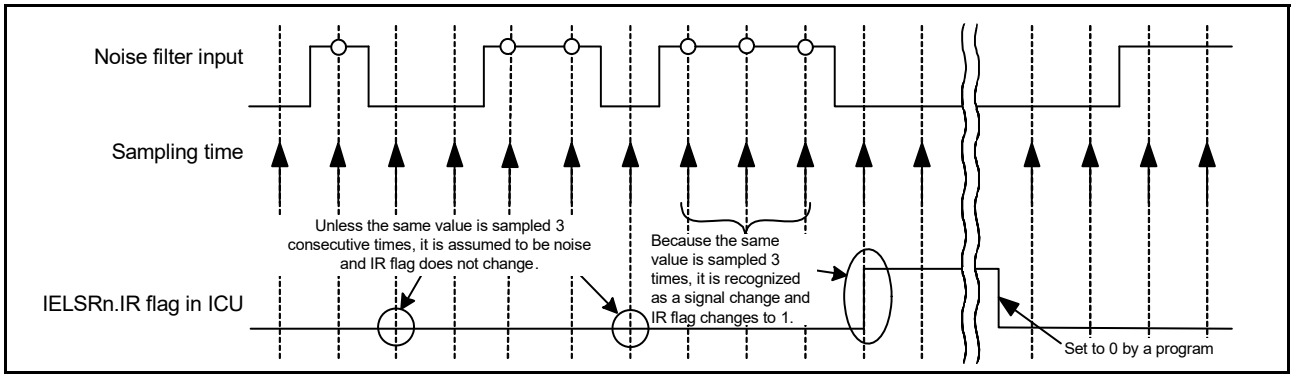


Figure 38.4 Noise filter and interrupt operation example

The operation example in Figure 38.4 applies when the CMPCTL.CDFS[1:0] bits are 01b, 10b, or 11b (noise filter used).

38.5 ACMPHS Interrupts

The ACMPHS generates six interrupt requests from sources ACMPHS0 to ACMPHS5. To use an ACMPHS interrupt, select it in the IELSR register in the Interrupt Controller Unit (ICU). Select the interrupt request in the CMPCTL.CSTEN bit, either through the edge selector, or not.

When using the ACMPHS interrupt through the edge selector, set at least one of the CMPCTL.CEG0 and CMPCTL.CEG1 bits to 1 (a value other than 00b for no edge selection). In most cases, set the CMPCTL.CSTEN bit to 0 (output through the edge selector). Set this bit to 1 only to release Software Standby mode or Snooze mode.

To use the ACMPHS interrupt in Software Standby mode or Snooze mode, set the CMPCTL.CSTEN bit to 1 (direct output), set the CMPCTL.CDFS[1:0] bits to 00b (digital noise filter not used), and set CMPCTL.CINV as follows:

- When detecting compare result 1 to 0, set CMPCTL.CINV to 0 (comparator output not inverted)
- When detecting compare result 0 to 1, set CMPCTL.CINV to 1 (comparator output inverted).

An ACMPHS0 interrupt request can be used to release Software Standby mode or Snooze mode. ACMPHS1 to ACMPHS5 cannot be used. For details on the register settings related to ACMPHS interrupt requests, see section 38.2.1, Comparator Control Register (CMPCTL).

38.6 ACMPHS Output to the Event Link Controller (ELC)

The ELC uses the ACMPHS interrupt request signal as an ELC event signal, enabling link operation for the preset module. To use the ACMPHS ELC event, select it in the ELSRn register in the ELC. When using the ELC event request, set the CMPCTL.CSTEN bit to 0 (output through the edge selector). Also, set at least one of the CMPCTL.CEG0 and CMPCTL.CEG1 bits to 1 (a value other than 00b for no edge selection).

38.7 ACMPHS Pin Output

The comparison result from the ACMPHS can be output to external pins. Use the CMPCTL.CINV and CPIOC.CPOE bits to set the output polarity (non-inverted or inverted output) and enable or disable output. To output the ACMPHS comparison result to the VCOUT output pin, set the associated Port mn Pin Function Select register (PmnPFS) in the I/O register.

38.8 Usage Notes

38.8.1 Settings for the Module-Stop Function

The Module Stop Control Register can enable or disable ACMPHS operation. The ACMPHS is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

38.8.2 Relationship with the ADC12

Restrictions apply on the simultaneous use of the ACMPHS analog input and ADC12 analog input. For details, see section 35, Relationship between ADC12 Units 0 and 1 and the ACMPHS.

39. Data Operation Circuit (DOC)

39.1 Overview

The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated.

Table 39.1 lists the DOC specifications, and Figure 39.1 shows a block diagram.

Table 39.1 DOC specifications

Parameter	Specifications
Data operation function	16-bit data comparison, addition, and subtraction
Module-stop function	Module-stop state can be set to reduce power consumption
Interrupts and event link function (DOC_DOPCI)	An interrupt is generated on the following conditions: • Compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h.

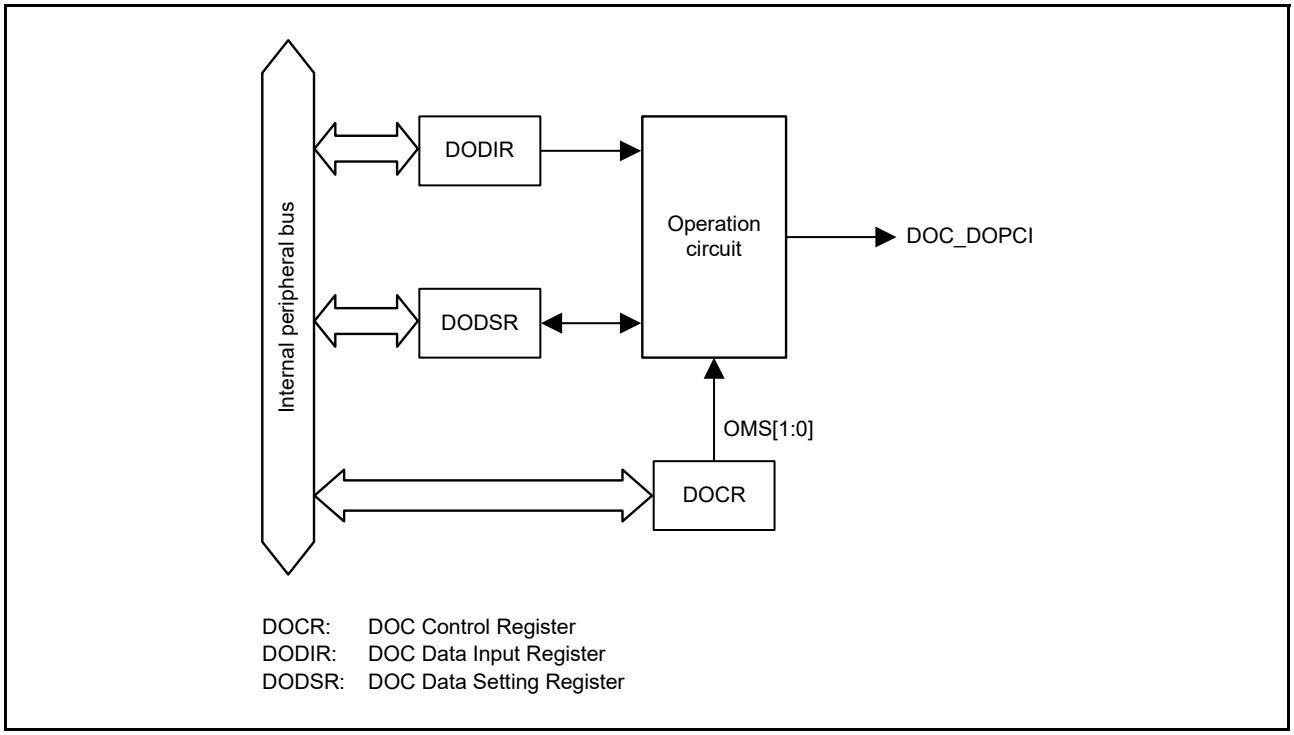


Figure 39.1 DOC block diagram

39.2 Register Descriptions

39.2.1 DOC Control Register (DOCR)

Address(es): DOC.DOCR 4005 4100h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	OMS[1:0]	Operating Mode Select	b1 b0 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited.	R/W
b2	DCSEL*1	Detection Condition Select	0: Set DOPCF when data mismatch is detected 1: Set DOPCF when data match is detected.	R/W
b4, b3	—	Reserved	There bits are read as 0. The write value should be 0.	R/W
b5	DOPCF	Data Operation Circuit Flag	Indicates the result of an operation	R
b6	DOPCFCL	DOPCF Clear	0: Save DOPCF flag state 1: Clear DOPCF flag.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Only valid when data comparison mode is selected.

OMS[1:0] bits (Operating Mode Select)

The OMS[1:0] bits select the operating mode of the DOC.

DCSEL bit (Detection Condition Select)

The DCSEL bit selects the detection condition in data comparison mode. This bit is only valid when data comparison mode is selected.

DOPCF flag (Data Operation Circuit Flag)

The DOPCF flag indicates the result of an operation.

[Setting conditions]

- The condition selected in the DCSEL bit is met
- A data addition result is greater than FFFFh
- A data subtraction result is less than 0000h.

[Clearing condition]

- Writing 1 to the DOPCFCL bit.

DOPCFCL bit (DOPCF Clear)

Setting the DOPCFCL bit to 1 clears the DOPCF flag. This bit is read as 0.

39.2.2 DOC Data Input Register (DODIR)

Address(es): DOC.DODIR 4005 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODIR is a 16-bit read/write register that stores 16-bit data used in all operations.

39.2.3 DOC Data Setting Register (DODSR)

Address(es): DOC.DODSR 4005 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODSR is a 16-bit read/write register that stores 16-bit data used as a reference in data comparison mode. This register also stores the results of operations in data addition and subtraction modes.

39.3 Operation

39.3.1 Data Comparison Mode

Figure 39.2 shows an example DOC operation in data comparison mode. The following sequence is an example of operation when DCSEL is set to 0 (data mismatch is detected as a result of data comparison):

1. Write 00b to the DOCR.OMS[1:0] bits to select data comparison mode.
2. Set 16-bit reference data in DODSR.
3. Write 16-bit data for comparison to DODIR.
4. Continue writing 16-bit data until all data to be compared is written to DODIR.
5. If a value written to DODIR does not match that in DODSR,*1 the DOCR.DOPCF flag is set to 1.

Note 1. When DOCR.DCSEL = 0

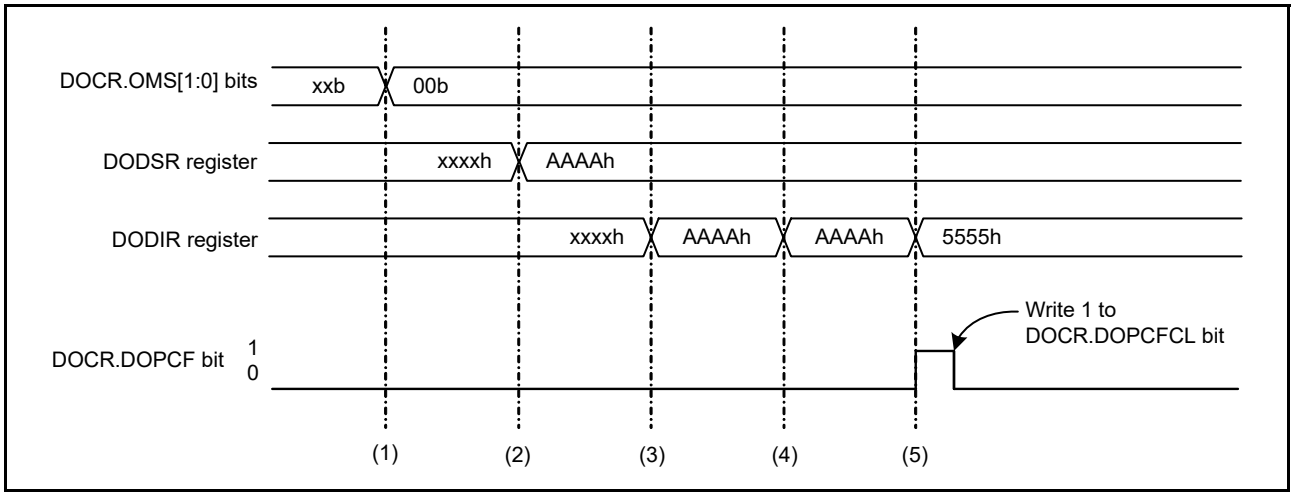


Figure 39.2 Example of operation in data comparison mode

39.3.2 Data Addition Mode

Figure 39.3 shows an example for DOC operation in data addition mode. The steps are as follows:

1. Write 01b to the DOCR.OMS[1:0] bits to select data addition mode.
2. Set 16-bit data in the DODSR register as the initial value.
3. Write 16-bit data to be added to the DODIR register. The result of the operation is stored in DODSR.
4. Continue writing 16-bit data until all data to be added is written to DODIR.
5. If the result of an operation is greater than FFFFh, the DOCR.DOPCF flag is set to 1.

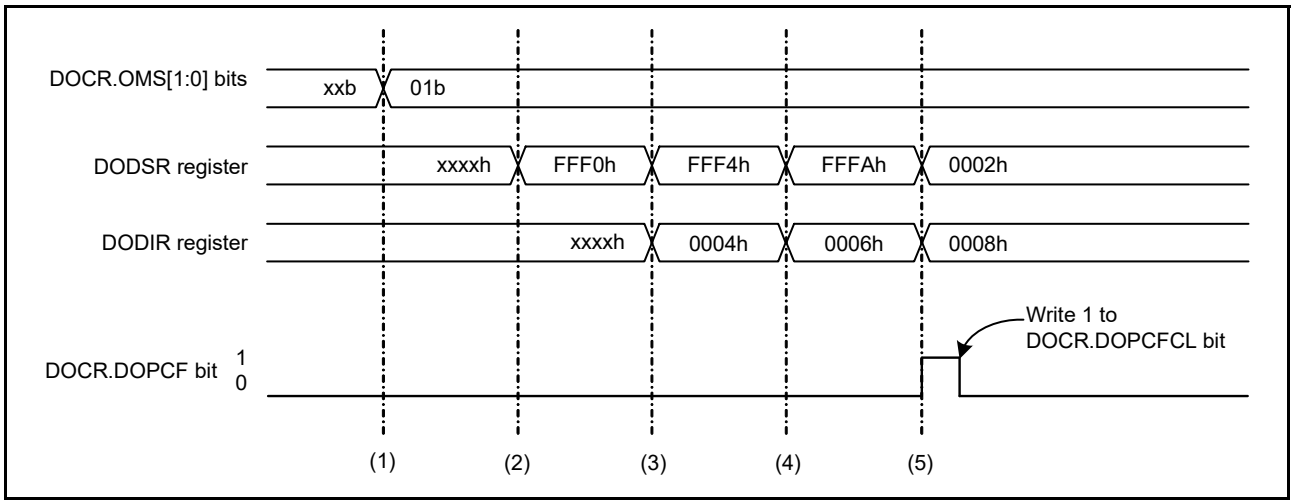


Figure 39.3 Example of operation in data addition mode

39.3.3 Data Subtraction Mode

Figure 39.4 shows an example for DOC operation in data subtraction mode. The steps are as follows:

1. Write 10b to the DOCR.OMS[1:0] bits to select data subtraction mode.
2. Set 16-bit data as the initial value in the DODSR register.
3. Write 16-bit data to be subtracted to the DODIR register. The result of the operation is stored in DODSR.
4. Continue writing 16-bit data to DODIR until all data for subtraction is written.
5. If the result of an operation is less than 0000h, the DOCR.DOPCF flag is set to 1.

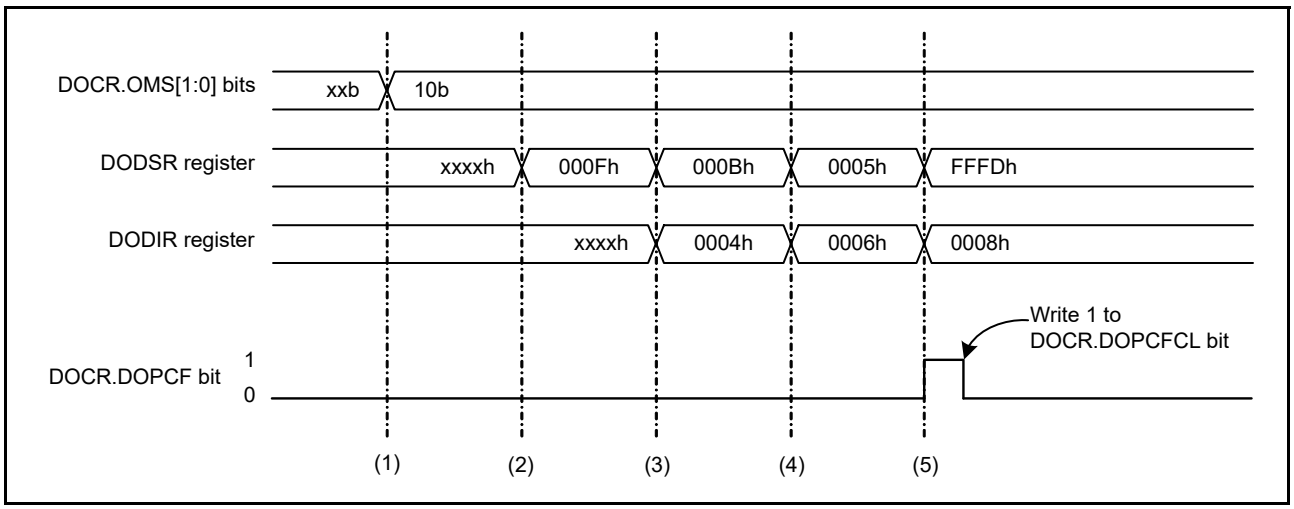


Figure 39.4 Example of operation in data subtraction mode

39.4 Interrupt Request and Output to the Event Link Controller (ELC)

The DOC outputs an event signal for the ELC under the following conditions:

- The compared values either match or mismatch
- The data addition result is greater than FFFFh
- The data subtraction result is less than 0000h.

This signal can be used to initiate operations by other modules selected in advance and can also be used as an interrupt request. When an event signal is generated, the Data Operation Circuit Flag (DOCR.DOPCF) is set to 1.

39.5 Usage Notes

39.5.1 Settings for the Module-Stop State

The Module Stop Control Register C (MSTPCRC) can enable or disable DOC operation. The DOC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

40. SRAM

40.1 Overview

The MCU provides on-chip high-speed SRAM modules with parity-bit checking.

Table 40.1 lists the SRAM specifications.

Table 40.1 SRAM specifications

Parameter	SRAMHS specifications
SRAM capacity	SRAMHS: 64 KB
SRAM address	SRAMHS: 1FFE 0000h to 1FFE FFFFh
Access*1	Access to the SRAMHS is always a no wait state
Data retention	Not available in Deep Software Standby mode
Module-stop function	Module-stop state can be set to reduce power consumption
Parity	Even-parity (data: 8 bits, parity: 1 bit)
Error checking	Even-parity error check

Note 1. For details, see section 40.3.4, Access Cycles.

40.2 Register Descriptions

40.2.1 SRAM Parity Error Operation After Detection Register (PARIOAD)

Address(es): SRAM.PARIOAD 4000 2000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation after Detection	1: Reset 0: Non-maskable interrupt.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PARIOAD register controls the operation on detection of a parity error. The SRAM Protection Register (SRAMPRCR) protects this register against writes. Always set the SRAMPRCR bit in SRAMPRCR to enabled before writing to this register. Do not write to the PARIOAD register while accessing the SRAM.

OAD bit (Operation after Detection)

The OAD bit specifies the generation of either a reset or a non-maskable interrupt when a parity error is detected.

40.2.2 SRAM Protection Register (SRAMPRCR)

Address(es): SRAM.SRAMPRCR 4000 2004h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW[6:0]							SRAMPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SRAMPRCR	Register Write Control	0: Disable writes to protected registers 1: Enable writes to protected registers.	R/W
b7 to b1	KW[6:0]	Write Key Code	These bits enable or disable writes to the SRAMPRCR bit	R/W

SRAMPRCR bit (Register Write Control)

The SRAMPRCR bit controls the write mode of the PARIOAD registers. When this bit is set to 1, writing to the PARIOAD registers is enabled. When you write to this bit, write 78h to the KW[6:0] bits simultaneously.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the SRAMPRCR bit. When you write to the SRAMPRCR bit, write 78h to the KW[6:0] bits simultaneously. When a value other than 78h is written to KW[6:0], the SRAMPRCR bit is not updated. The KW[6:0] bits are always read as 00h.

40.3 Operation

40.3.1 Low-Power Functions

Power consumption can be reduced by setting the Module Stop Control Register A (MSTPCRA) to stop the supply of the clock signal to the SRAM. The control bits for each module are as follows:

- Setting the MSTPA5 bit in MSTPCRA to 1 stops the supply of the clock signal to SRAMHS.

Stopping the clock signal supply places the SRAM in the module-stop state. The SRAM operates after a reset.

The SRAM is not accessible in the module-stop state. Do not transition to the module-stop state while accessing the SRAM. Access to the SRAM in the module-stop state is prohibited. If access is attempted, correct operation is not guaranteed. For details on the MSTPCRA register, see section 11, Low Power Modes.

40.3.2 Parity Calculation Function

The IEC60730 standard requires the checking of SRAM data. When data is written, a parity bit is added to every 8-bit data in the SRAM which has a 32-bit data width, and when data is read, the parity is checked. When a parity error occurs, a parity-error notification is generated. This function can also be used to trigger a reset. The specification for SRAMHS is even parity.

Parity error notification can be specified as a non-maskable interrupt or a reset in the OAD bit in the PARIOAD register. When the OAD bit in the PARIOAD register is set to 1, a parity error is output to the reset function. When the OAD bit is set to 0, a parity error is output to the ICU as a non-maskable interrupt.

Parity errors often occur because of noise. To confirm whether the cause of the parity error is noise or corruption, see the parity check flows in Figure 40.1 and Figure 40.2.

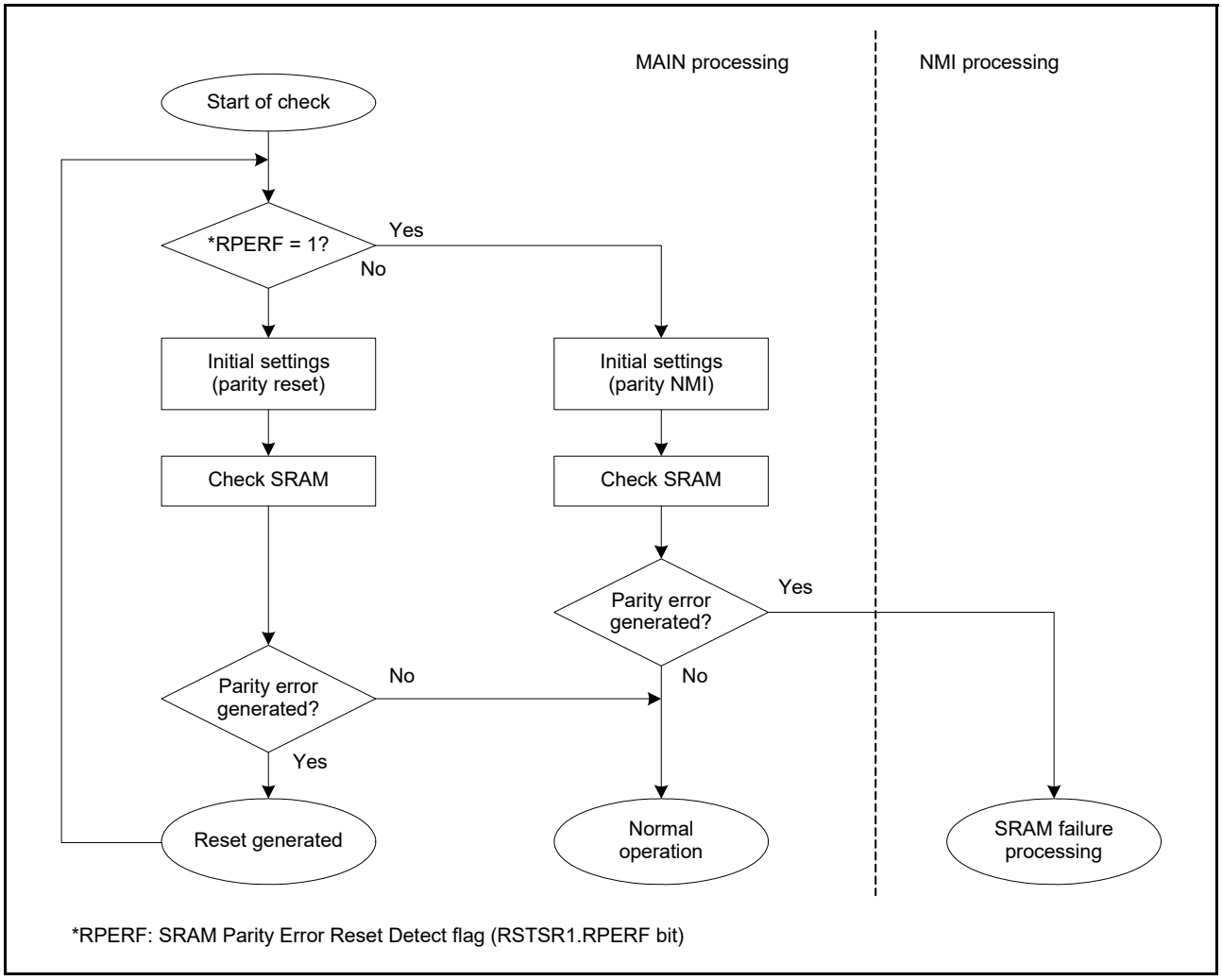


Figure 40.1 Flow of SRAM parity check when SRAM parity reset is enabled

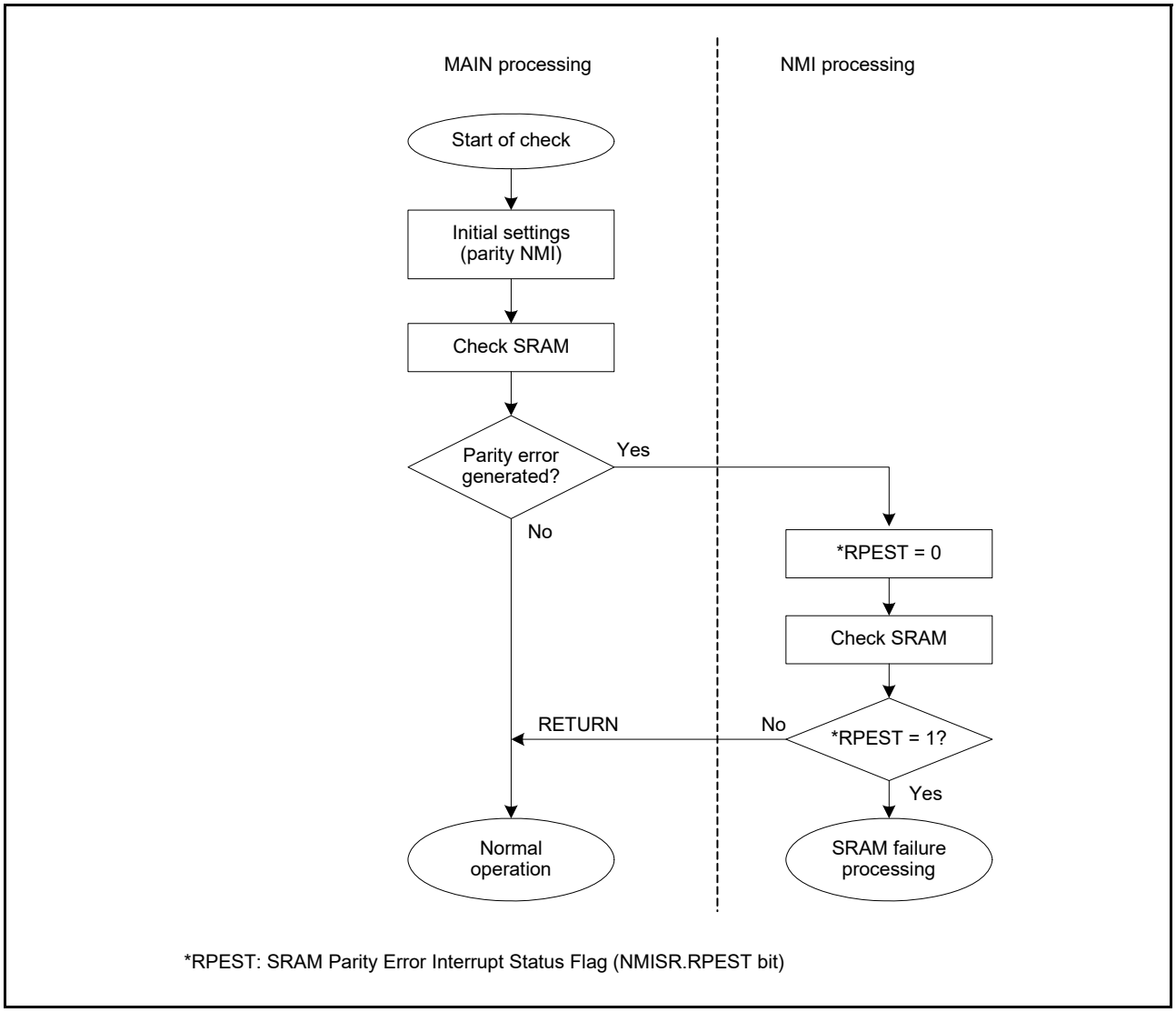


Figure 40.2 Flow of SRAM parity check when SRAM parity interrupt is enabled

40.3.3 SRAM Error Sources

An SRAM error source is a parity error and can generate either a non-maskable interrupt or a reset, as selected with the OAD bit in the PARIOAD register.

Table 40.2 SRAM error sources

Interrupt source	DTC activation	DMAC activation
Parity error (SRAMHS)	Not possible	Not possible

40.3.4 Access Cycles

Table 40.3 SRAMHS (parity area 1FFE 0000h to 1FFE FFFFh)

Read (cycles)		Write (cycles)	
Word access	Halfword/byte access	Word access	Halfword/byte access
2		2	

40.4 Usage Notes

40.4.1 Instruction Fetch from SRAM Area

When using the SRAMHS to operate a program, initialize the SRAM area so that the CPU can correctly prefetch data. If the CPU prefetches data from an SRAM area that is not initialized, a parity error might occur. Initialize the additional 12-byte area from the end address of a program with a 4-byte boundary. Renesas recommends using the NOP instruction for data initialization.

40.4.2 Store Buffer of SRAM

For fast access between the SRAM and CPU, a store buffer is used. When a load instruction is executed from the same address after a store instruction to the SRAM, the load instruction might read data from the buffer instead of data from the SRAM. To read data on the SRAM correctly, use either of the following procedures:

- After writing to the SRAM (address = A), use the NOP instruction, then read the SRAM (address = A)
- After writing to the SRAM (address = A), read data from an area other than SRAM (address = A), then read the SRAM (address = A).

41. Flash Memory

41.1 Overview

The MCU provides up to 512-KB code flash memory and 8-KB data flash memory. The Flash Control Unit (FCU) controls the programming and erasure of the flash memory. The Flash Application Command Interface (FACI) controls the FCU in accordance with the specified FACI commands.

Table 41.1 lists the specifications of the code flash memory and data flash memory, and Figure 41.1 shows a block diagram of the related modules. Figure 41.2 shows the configuration of the code flash memory, and Figure 41.3 shows the configuration of the data flash memory.

Table 41.1 Code flash memory and data flash memory specifications

Parameter	Code flash memory	Data flash memory
Memory capacity	• Up to 512 KB of user area	8 KB of data area
Read cycle	• 80 MHz < ICLK frequency ≤ 120 MHz Cache hit: 1 cycle Cache miss: 3 cycles • 40 MHz < ICLK frequency ≤ 80 MHz Cache hit: 1 cycle Cache miss: 2 cycles • ICLK frequency ≤ 40 MHz Cache hit: 1 cycle Cache miss: 1 cycle.	A read operation takes 7 FCLK cycles in words or bytes (FCLK frequency is up to 60 MHz)
Value after erasure	FFh	Undefined
Programming/erasing methods	• Programming and erasure of code and data flash memory through the FACI commands specified in the FACI command issuing area (407E 0000h) • Programming by dedicated flash-memory programmer transfer through a serial interface (serial programming) • Programming of flash memory by user program (self-programming)	
Security function	Protection against illicit tampering or reading of data in flash memory	
Protection	Protection against erroneous overwriting of flash memory	
Background operations (BGOs)	• Code flash memory can be read during data flash memory programming • Data flash memory can be read during code flash memory programming	
Units of programming and erasure	• 128-byte units for programming in user area • Block units for erasure in user area	• 4/8/16-byte units for programming in data area • 64/128/256-byte units for erasure in data area
Other functions	Interrupts accepted during self-programming	
	An expansion area of flash memory (option bytes) can be set in the initial MCU settings	
On-board programming (four types)	Programming in serial programming mode (SCI boot mode): • Asynchronous serial interface (SCI9) used • Transfer rate adjusted automatically. Programming in on-chip debug mode: • JTAG or SWD interface used • Dedicated hardware not required. Programming by a routine for code and data flash memory programming within the user program: • Allows code and data flash memory programming without resetting the system.	

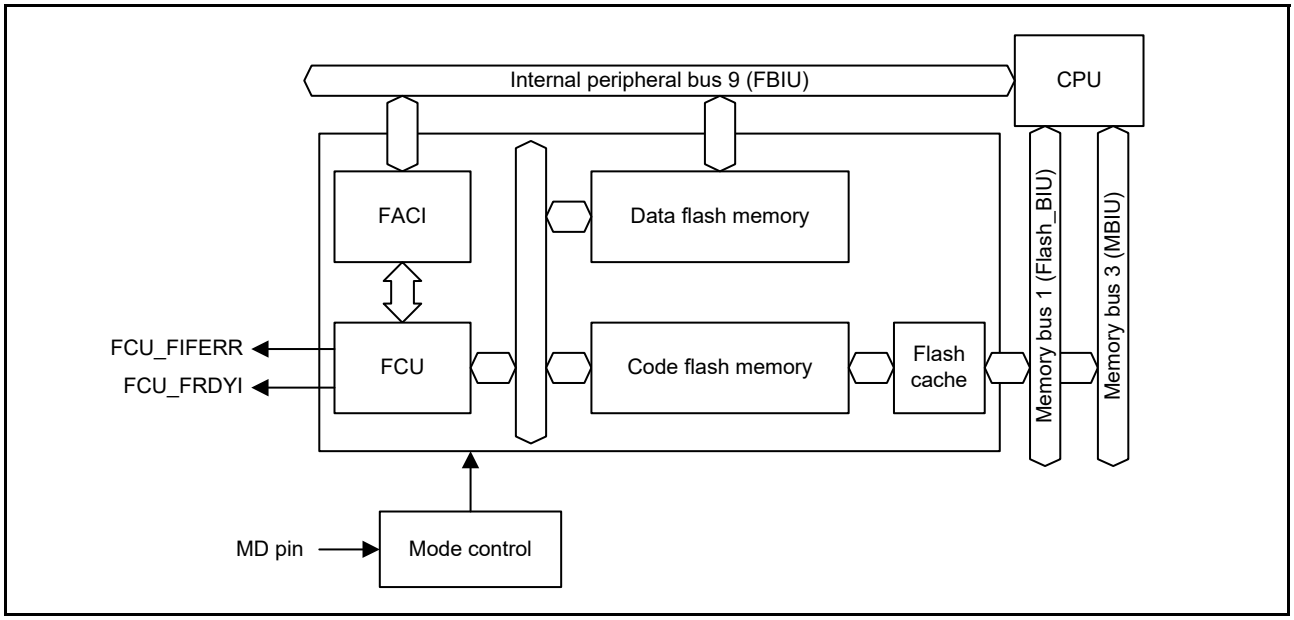


Figure 41.1 Flash memory-related modules block diagram

41.2 Memory Structure

Figure 41.2 shows the mapping of the code flash memory, and Table 41.2 shows the read and programming/erasure addresses of the code flash memory. The user space of the code flash memory is divided into 8- and 32-KB blocks, which serve as the units of erasure. The user area is available for storing the user program.

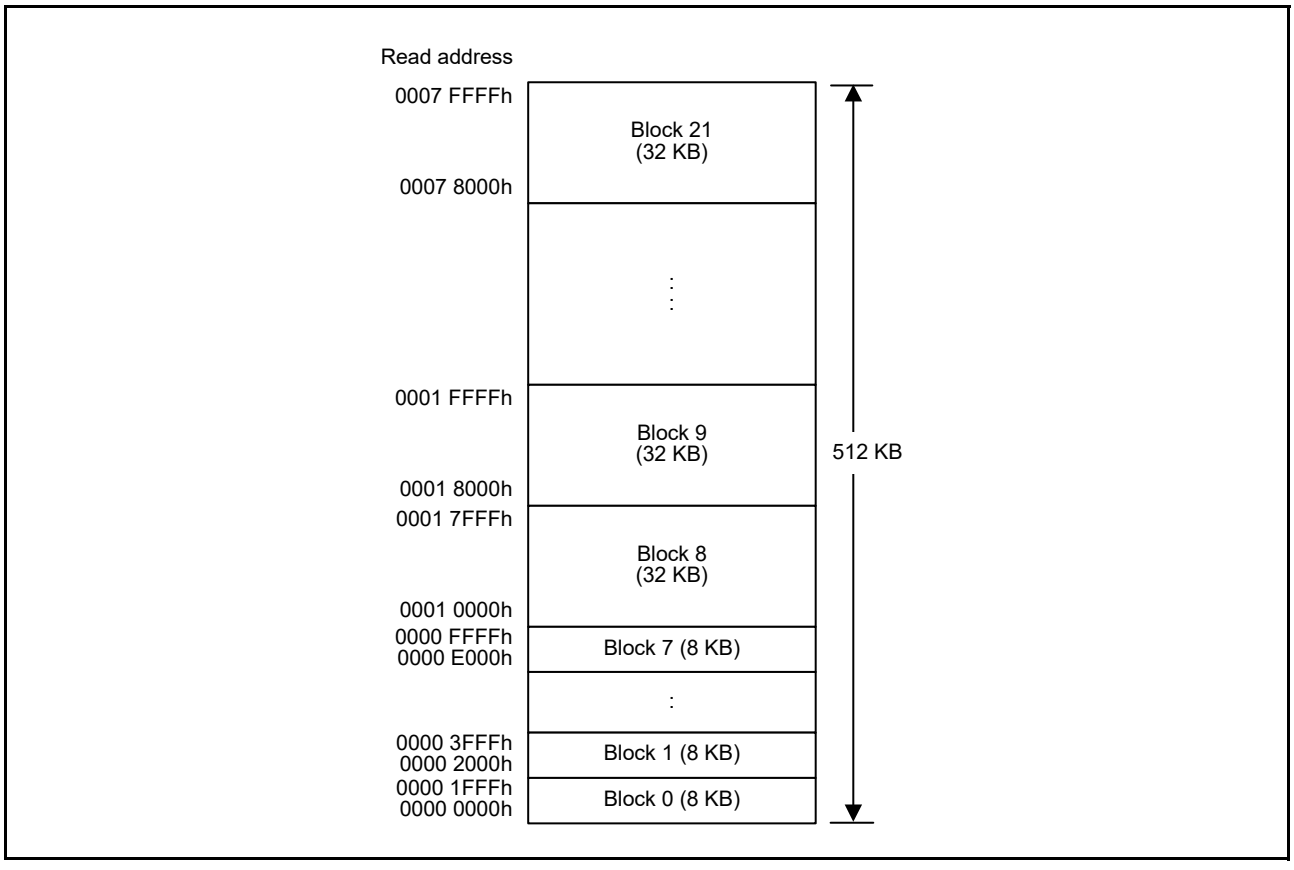


Figure 41.2 Mapping of the code flash memory

Table 41.2 Read and P/E addresses of the code flash memory

Size of code flash memory	Read address	P/E address	Number of blocks
512 KB	0000 0000h to 0007 FFFFh	0000 0000h to 0007 FFFFh	0 to 21
256 KB	0000 0000h to 0003 FFFFh	0000 0000h to 0003 FFFFh	0 to 13

The data area of the data flash memory is divided into 64-byte blocks, with each being a unit for erasure. Figure 41.3 shows the mapping of the data flash memory.

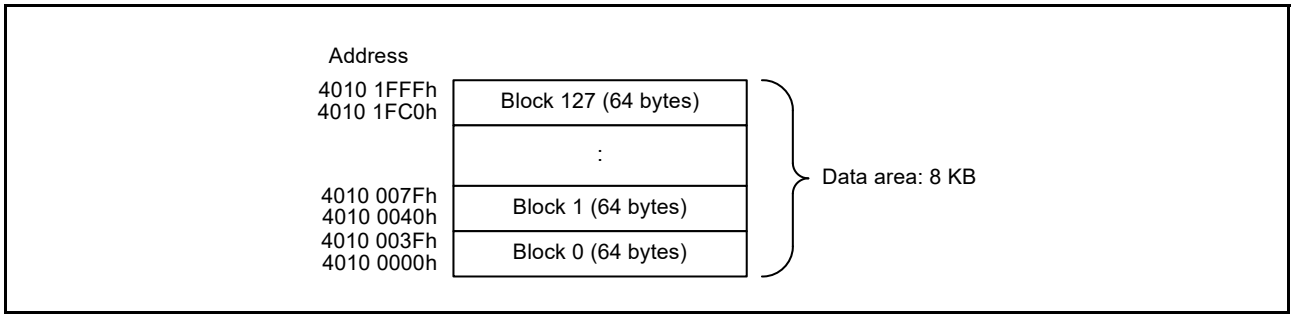


Figure 41.3 Mapping of the data flash memory

41.3 Flash Cache

41.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for the prefetch access in CPU instruction fetches.

Table 41.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	256 bytes	16 bytes	32 bytes
Associativity	• 8-way set associative • 128 bits/entry (128-bit aligned data) • 2 entries/way	• Fully associative • 128 bits/entry (128-bit aligned data) • 1 entry for FCACHE2	• Fully associative • 128 bits/entry (128-bit aligned data) • 2 entries
Access cycles	• Cache hit: 0 wait • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 wait • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 wait • Cache miss: Number of waits set in Flash Wait Cycle Register

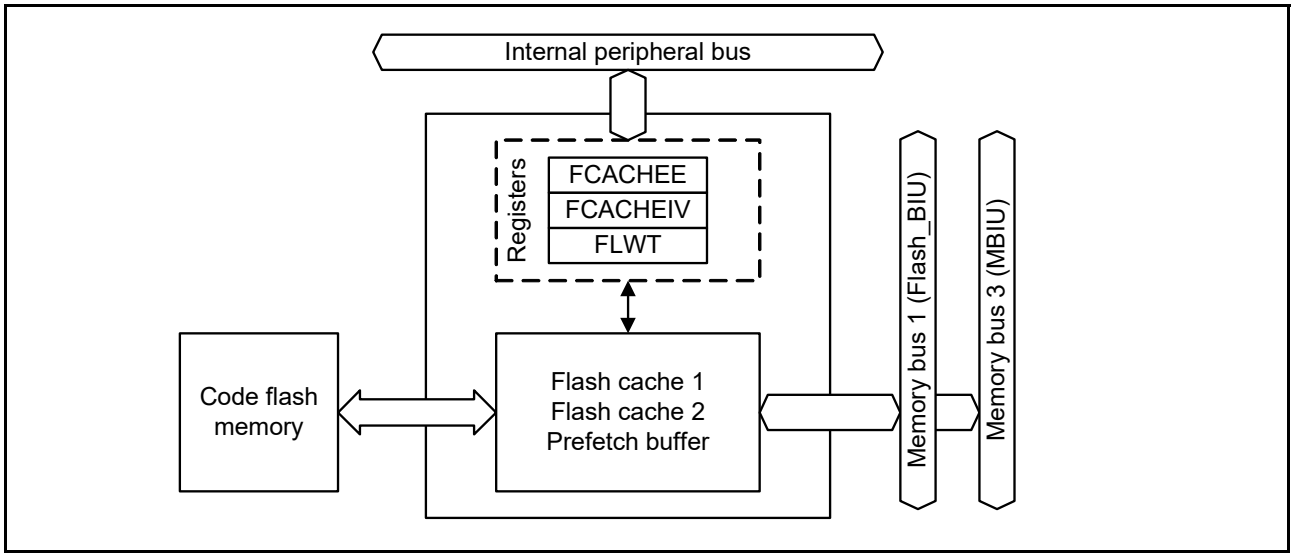


Figure 41.4 FCACHE block diagram

41.3.2 Register Descriptions

41.3.2.1 Flash Cache Enable Register (FCACHEE)

Address(es): FCACHE.FCACHEE 4001 C100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FCACHEEN	FCACHE Enable	0: Disable FCACHE 1: Enable FCACHE.	R/W
b15 to b1	—	Reserved	These bits are read as 0.	R

The FCACHEE.FCACHEEN bit enables or disables the flash cache function for FCACHE1, FCACHE2, and FLPF. This bit does not affect FCACHEIV.FCACHEIV. When FCACHE is enabled, the HPROT[3] bit setting determines whether it is cacheable or non-cacheable. See section 14.5 for details on HPROT[3].

41.3.2.2 Flash Cache Invalidate Register (FCACHEIV)

Address(es): FCACHE.FCACHEIV 4001 C104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FCACHEIV	Flash Cache Invalidate	• Reads: 0: Do not invalidate 1: Invalidate. • Writes: When write value is 1, FCACHE is invalidated. When write value is 0, this setting is ignored.	R/W
b15 to b1	—	Reserved	These bits are read as 0	R

When 1 is written to the FCACHEIV.FCACHEIV bit, the flash cache data in FCACHE1, FCACHE2, and FLPF is invalidated.

41.3.2.3 Flash Wait Cycle Register (FLWT)

Address(es): FCACHE.FLWT 4001 C11Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	FLWT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	FLWT[2:0]*1	Flash Wait Cycle	b2 b0 0 0 0: 0 wait (ICLK ≤ 40 MHz) 0 0 1: 1 wait (40 MHz < ICLK ≤ 80 MHz) 0 1 0: 2 waits (80 MHz < ICLK ≤ 120 MHz). Other settings are reserved.	R/W
b15 to b3	—	Reserved	These bits are read as 0.	R

Note 1. Settings other than 000b are prohibited in the Subosc-speed mode.

The Flash Wait Cycle Register (FLWT) sets the access wait count for the flash memory. For faster clock frequencies, set FLWT.FLWT before changing the clock frequency. For slower clock frequencies, set FLWT.FLWT after changing the clock frequency.

41.4 Operation

Use the FCACHEE register to set up and enable flash operation. To set up the flash cache and prepare to rewrite the flash memory:

1. Disable the flash cache by resetting FCACHEE.FCACHEEN.*1
2. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
3. Check that FCACHEIV.FCACHEIV is 0.
4. Enable the flash cache by setting FCACHEE.FCACHEEN.

Note 1. It is not necessary to disable the flash cache on the first setup after reset.

41.4.1 Notice to use Flash Cache

When accessing the flash cache from the CPU, Arm® MPU should also be set to cacheable.

See the *ARM®v7-M Architecture Reference Manual* and the *ARM® Cortex®-M4 Devices Generic User Guide*.

41.5 Operating Modes Associated with the Flash Memory

Figure 41.5 shows a diagram of the mode transitions associated with the flash memory. For information on setting up the modes, see section 3, Operating Modes.

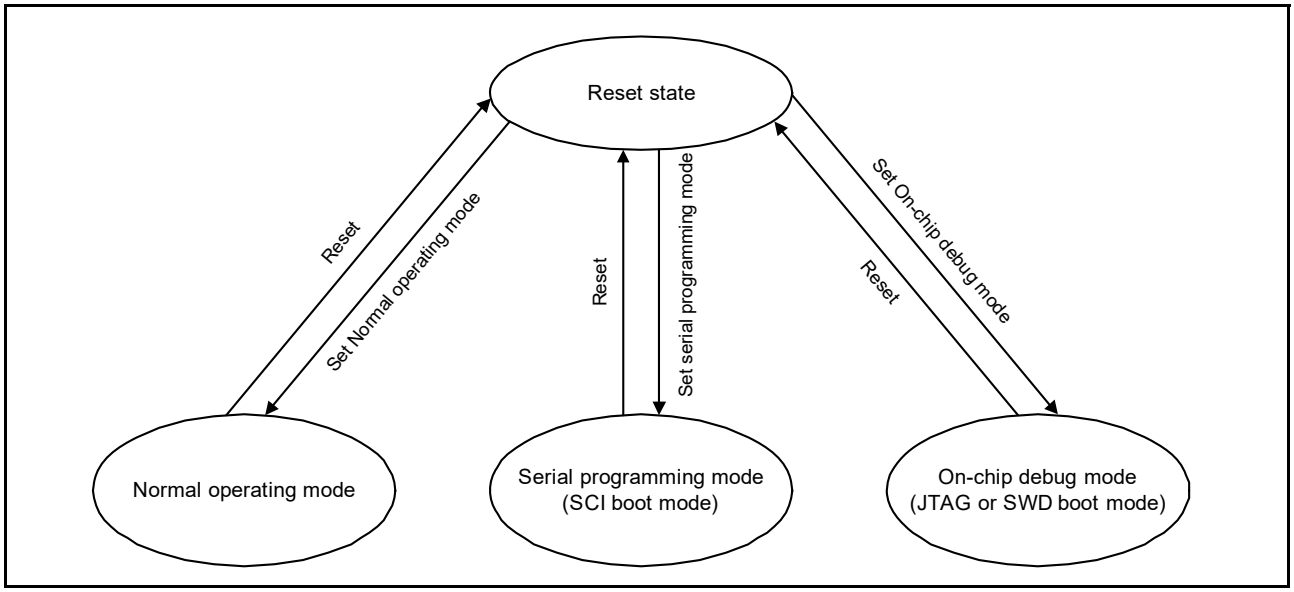


Figure 41.5 Mode transitions associated with flash memory

The flash memory areas where programming and erasure are permitted and where the boot program executes at a reset, differ with the mode. Table 41.4 shows the differences between the modes.

Table 41.4 Difference between modes

Parameter	Normal operating mode	Serial programming mode (SCI boot mode)	On-chip debug mode (JTAG or SWD boot mode)
Programmable and erasable areas	• Code flash memory • Data flash memory	• Code flash memory • Data flash memory	• Code flash memory • Data flash memory
Erasure in block units	Possible	Possible	Possible
Boot program at a reset	User area program	Embedded program for serial programming	Depends on debug command

41.5.1 ID Code Protection

The ID code protection function prohibits programming and on-chip debugging. When ID code protection is enabled, the device validates or invalidates the ID code sent from the host by comparing it with the ID code stored in the flash memory. Programming and on-chip debugging are enabled only when the two match.

The ID code in flash memory consists of four 32-bit words. ID code bits [127] and [126] determine whether ID code protection is enabled and the authentication method to use with the host.

Table 41.5 shows how the ID code determines the authentication method.

Table 41.5 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI boot mode) On-chip debug mode (JTAG/SWD boot mode)	FFh, …, FFh (All bytes are FFh)	Protection disabled	ID code validation is not performed, the ID code always matches, and connection to the programmer or the on-chip debugger is permitted.
	Bit [127] = 1, bit [126] = 1, and at least one of the 16 bytes is not FFh	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. When the ID code sent from the programmer or the on-chip debugger is ALeRASE in ASCII code (414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the contents of the user flash (code and data) area and configuration area are erased. However, forced erasure is not performed when the AWS.FSPR*1 bit is 0.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state.
	Bit [127] = 0	Protection enabled	ID code validation is not performed, the ID code is always mismatching, and connection to the programmer or the on-chip debugger is prohibited.

Note 1. For details on the AWS.FSPR bit, see section 7.2.3, Access Window Setting Register (AWS).

41.6 Overview of Functions

By using a dedicated flash-memory programmer to program the on-chip flash memory through a serial interface (serial programming) or JTAG/SWD interface (on-chip debug mode), the device can be programmed before or after it is mounted on the target system. Additionally, security functions to prohibit overwriting of the user program written to the on-chip flash memory are incorporated to prevent tampering by third parties.

Programming by the user program (self-programming) is available for applications that might require updating after system manufacturing or shipment. Protection features for safely overwriting the flash memory area are also provided. Additionally, interrupt processing during self-programming is supported so that the programming can proceed while processing external communications and other functions. Table 41.6 lists the programming methods and the associated operating modes.

Table 41.6 Programming methods (1 of 2)

Programming method	Functional overview	Operating mode
Serial programming	A dedicated flash-memory programmer connected through the SCI interface enables on-board programming of the flash memory after the device is mounted on the target system.	Serial programming mode
	A dedicated flash-memory programmer connected through the SCI interface and a dedicated programming adapter board allow off-board programming of the flash memory, before it is mounted on the target system.	

Table 41.6 Programming methods (2 of 2)

Programming method	Functional overview	Operating mode
Self-programming	A user program written to memory in advance of serial programming execution can also program the flash memory. The background operation capability makes it possible to fetch instructions or otherwise read data from the code flash memory while the data flash memory is programmed. As a result, a program resident in the code flash memory can program the data flash memory. For background operations that are not possible, instructions in the code flash memory cannot be fetched and data cannot be accessed while the code flash memory is being programmed by self-programming. In such cases, a program for programming from the internal SRAM must be transferred in advance and executed.	Normal operating mode
JTAG or SWD programming	A dedicated flash-memory programmer or an on-chip debugger connected through JTAG or SWD enables on-board programming of the flash memory after the device is mounted on the target system.	On-chip debug mode
	A dedicated flash-memory programmer or an on-chip debugger connected through JTAG or SWD and a dedicated programming adapter board allow off-board programming of the flash memory, for example, programming of the device, before it is mounted on the target system.	

Table 41.7 lists the functions of the on-chip flash memory.

Use serial programmer commands for serial programming. For self-programming, use the FACI commands to read the on-chip flash memory or run the user program.

Table 41.7 Basic functions

Function	Functional overview	Availability	
		Serial programming	Self-programming
Blank check	Checks a specified block to ensure that writing to it has not already proceeded. Results of reading from data flash memory to which nothing is written after erasure are not guaranteed, so use blank checking to confirm that writing to memory has not proceeded after erasure.	Not supported	Supported (data flash programming only)
Block erasure	Erases the memory contents in the specified block	Supported	Supported
Programming	Writes to the specified address	Supported	Supported
Read	Reads data programmed in the flash memory	Supported	Not supported (read by user program is possible)
ID code check	Compares the ID code sent by the host with the code stored in the ROM. If the two match, the FCU enters the wait state for programming and erasure commands from the host.	Supported	Not supported (ID authentication is not performed)
Security configuration	Configures the security function for serial programming	Supported with conditions (only allows switching from enabled to disabled)	Supported with conditions (only allows switching from enabled to disabled)
Protection configuration	Configures the access window for flash area protection in the code flash memory	Supported	Supported

The on-chip flash memory supports the ID code security function. Authentication of ID codes is a security function for use with serial programming and with JTAG or SWD programming. Table 41.8 lists the security functions supported by the on-chip flash memory, and Table 41.9 lists the available operations and security settings.

Table 41.8 Security functions

Function	Description
ID authentication	The result of ID authentication can be used to control the connection of a serial programmer for serial programming

Table 41.9 Available operations and security settings

Function	All security settings and erasure, programming, and read operations		Constraints on the security setting configuration
	Serial programming and on-chip debug mode	Self-programming mode	Self-programming mode
ID authentication	When ID codes do not match: • Block erasure commands: Not supported • Programming commands: Not supported • Read commands: Not supported • Security configuration commands: Not supported • Protection configuration commands: Not supported. When ID codes match: • Block erasure commands: Supported • Programming commands: Supported • Read commands: Supported • Security configuration commands: Supported • Protection configuration commands: Supported.	• ID authentication is not performed • Blank check: Supported • Block erasure: Supported • Programming: Supported • Security configuration: Supported • Protection configuration: Supported.	ID authentication is not performed

41.6.1 Configuration Area Bit Map

The bits used for ID authentication, startup area select, access window protection, and security configuration functions are mapped in Figure 41.6. The boot program must use these bits as hexadecimal data.

Base R-address: 0100 A100h
P/E-address: 0000 A100h

Bit

offset	+31	+30	+29	+28	+27	+26	+25	+24	+23	+22	+21	+20	+19	+18	+17	+16	+15	+14	+13	+12	+11	+10	+ 9	+ 8	+ 7	+ 6	+ 5	+ 4	+ 3	+ 2	+ 1	+ 0
00BCh																																
:																																
0080h																																
007Ch																																
0078h																																
0074h																																
0070h																																
006Ch																																
0068h																																
0064h	BTFLG					FAWE[10:0]											FSPR					FAWS[10:0]										
0060h																																
005Ch	ID[127:96]																															
0058h	ID[95:64]																															
0054h	ID[63:32]																															
0050h	ID[31:0]																															
004Ch																																
0048h																																
0044h																																
0040h																																

Figure 41.6 Configuration area bit map

41.6.2 Startup Area Select

The startup area select function allows the boot program to be safely updated. The startup area is 8 KB of space located in the user area. The FACI controls the address of the startup area based on the Startup Area Select flag (AWS.BTFLG) that is located in the configuration area. The startup area can be locked by the AWS.FSPR*1 bit.

Note 1. For the AWS.FSPR bit, see section 7.2.3, Access Window Setting Register (AWS).

Figure 41.7 shows an overview of the startup program protection.

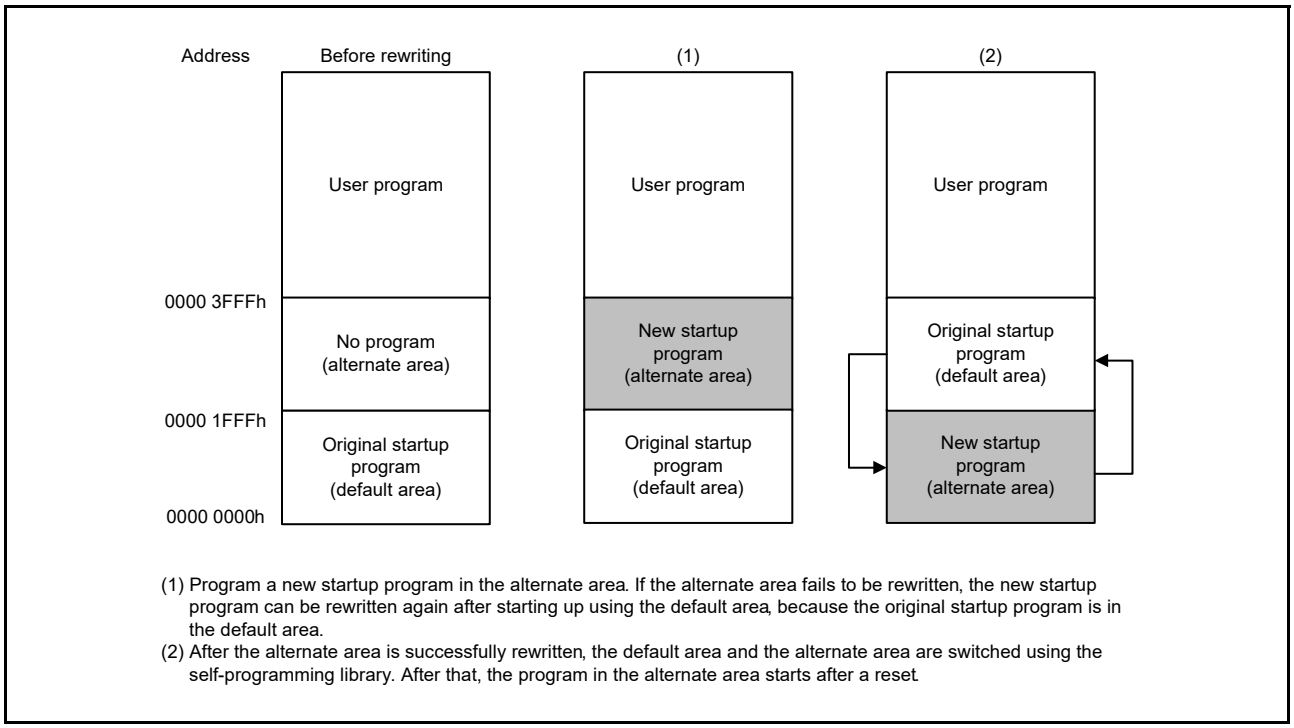


Figure 41.7 Overview of startup program protection

41.6.3 Protection by Access Window

Issuing the program or block erase command to a flash memory area outside of the access window results in the command-locked state. The access window is only valid in the user area of the code flash memory. The access window provides protection in self-programming, serial programming, and on-chip debug modes.

The access window is specified in both the AWS.FAWS[10:0] and AWS.FAWE[10:0] bits*1.

Setting of the FAWS[10:0] and the FAWE[10:0] bits in various conditions is described as follows:

- FAWE[10:0] = FAWS[10:0]: The P/E command can execute anywhere in the user area of the code flash memory
- FAWE[10:0] > FAWS[10:0]: The P/E command can only execute in the window from the block pointed to by the FAWS[10:0] bits to one block lower than the one pointed to by the FAWE bits
- FAWE[10:0] < FAWS[10:0]: The P/E command cannot execute anywhere in the user area of the code flash memory.

Note 1. For information on the AWS.FAWS[10:0] and AWS.FAWE[10:0] bits, see section 7.2.3, Access Window Setting Register (AWS).

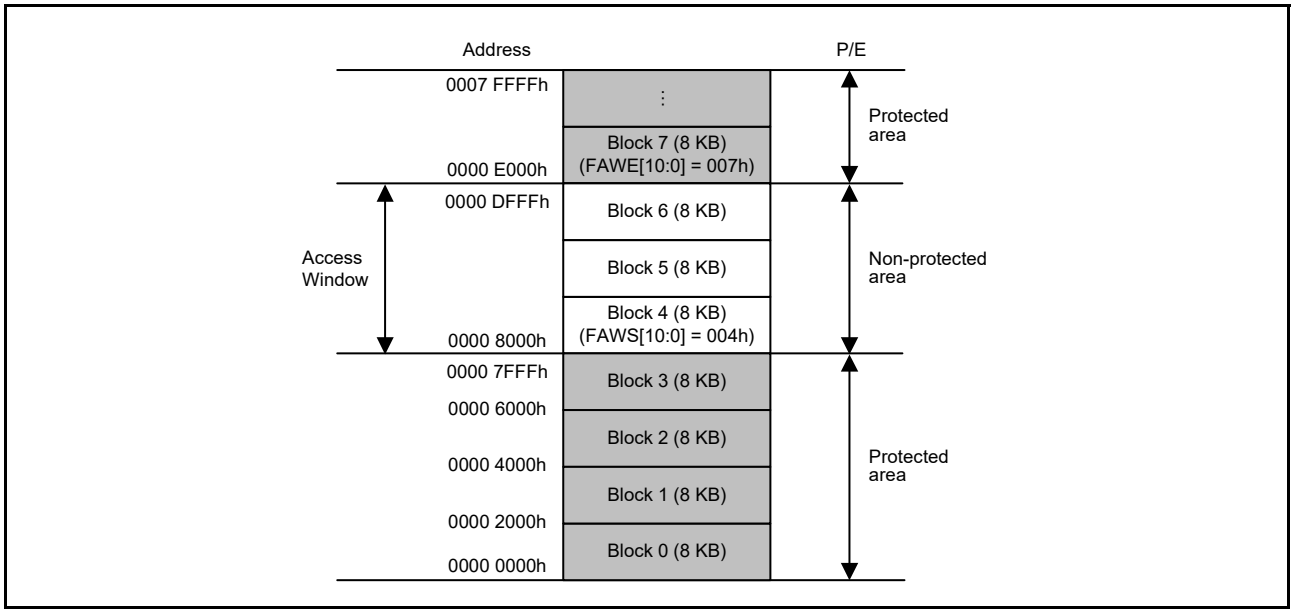


Figure 41.8 Start block address (FAWS) and end block address (FAWE) of access window when the access window only includes the 8-KB block size

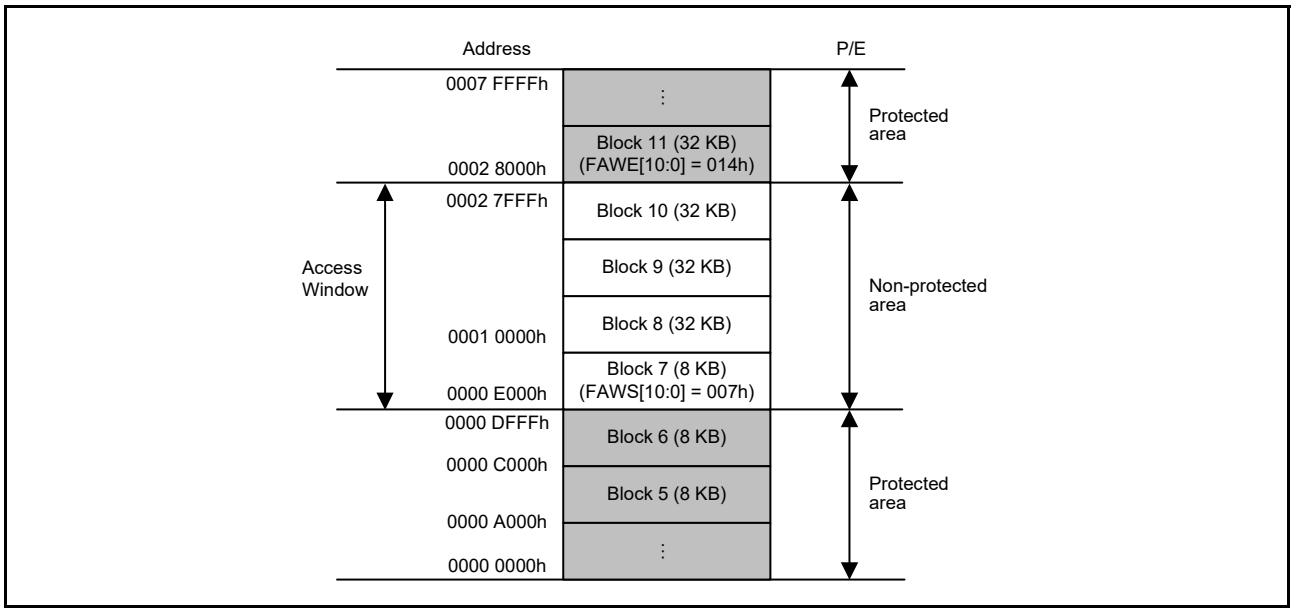


Figure 41.9 Start block address (FAWS) and end block address (FAWE) of access window when the access window includes 8-KB and 32-KB block sizes

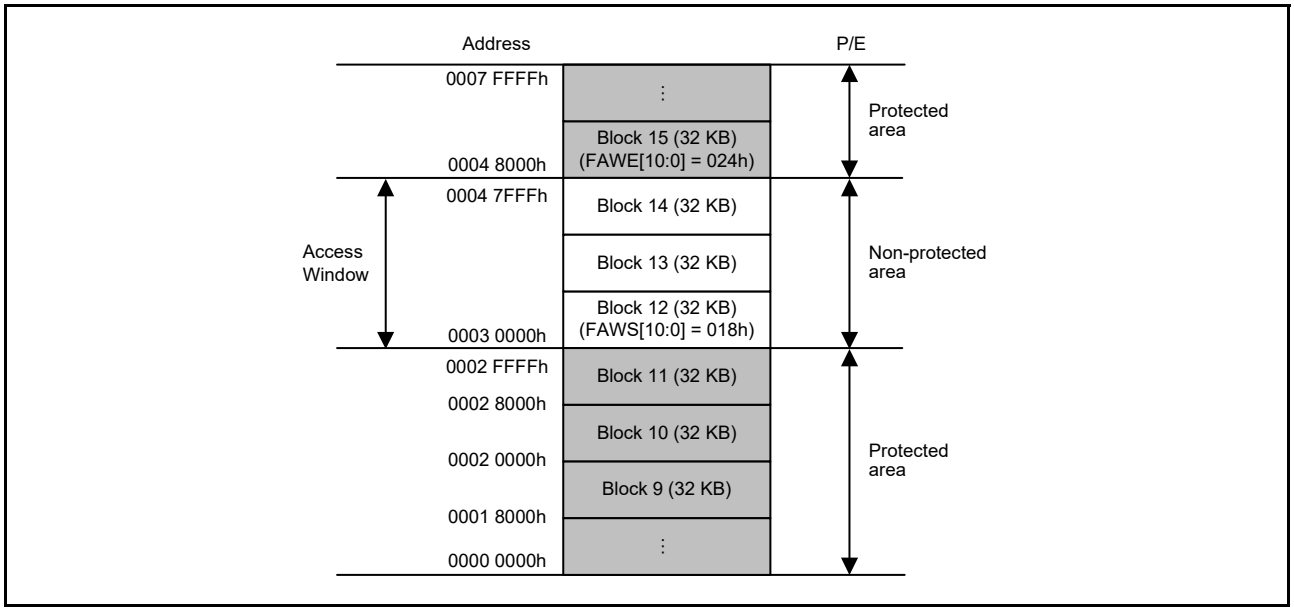


Figure 41.10 Start block address (FAWS) and end block address (FAWE) of access window when the access window only includes the 32-KB block size

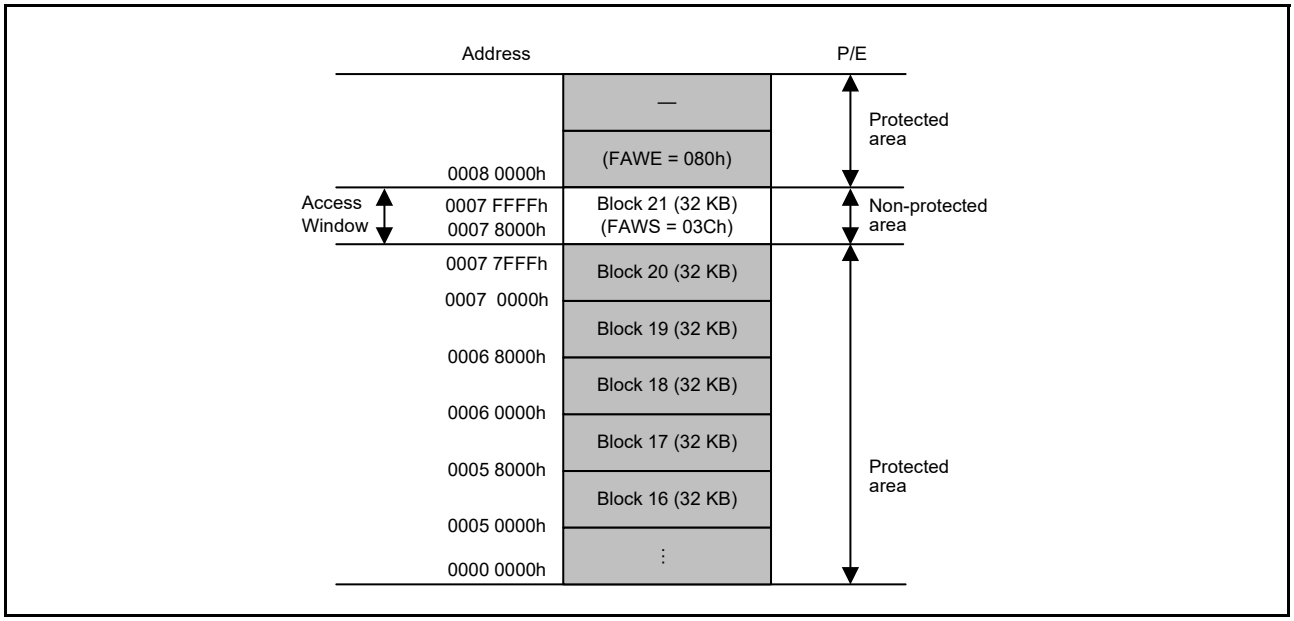


Figure 41.11 Start block address (FAWS) and end block address (FAWE) of access window when the access window only includes the final block

41.7 Programming Commands

The FACI controls the FCU in accordance with the specified FACI commands.

41.8 Suspend Operation

Reading from the code or data flash memory is not possible during programming or erasure when the address ranges do not satisfy the conditions for background operation. When a P/E suspend command is issued to suspend the programming or erasure of the code or data flash memory, reading from memory is enabled. One suspend command mode is available for programming and two suspend command modes are available for erasure (suspension priority mode and erasure priority mode). The P/E resume command is available for resuming suspended programming or erasure.

41.9 Protection

The types of protection provided include:

- Software protection
- Error protection
- Boot program protection.

41.10 Serial Programming Mode

The serial programming mode includes boot mode with SCI9.

Table 41.10 lists the I/O pins of the flash memory-related modules.

Table 41.10 I/O pins of flash memory-related modules

Pin name	I/O	Applicable modes	Function
MD	Input	SCI boot mode (serial programming mode)	Selection of operating mode
P110/RXD9	Input	SCI boot mode	For host communication, to receive data through SCI
P109/TXD9	Output		For host communication, to transmit data through SCI

41.10.1 SCI Boot Mode

In boot mode, the host sends control commands and data for programming, and the code and data flash memory area are programmed or erased accordingly. An on-chip SCI handles transfer between the host and the MCU in asynchronous mode. Tools for transmission of control commands and the data for programming must be prepared in the host.

When the MCU is activated in boot mode, the embedded program for serial programming is executed. This program automatically adjusts the bit rate of the SCI and controls programming and erasure by receiving control commands from the host.

Figure 41.12 shows the system configuration for operation in boot mode.

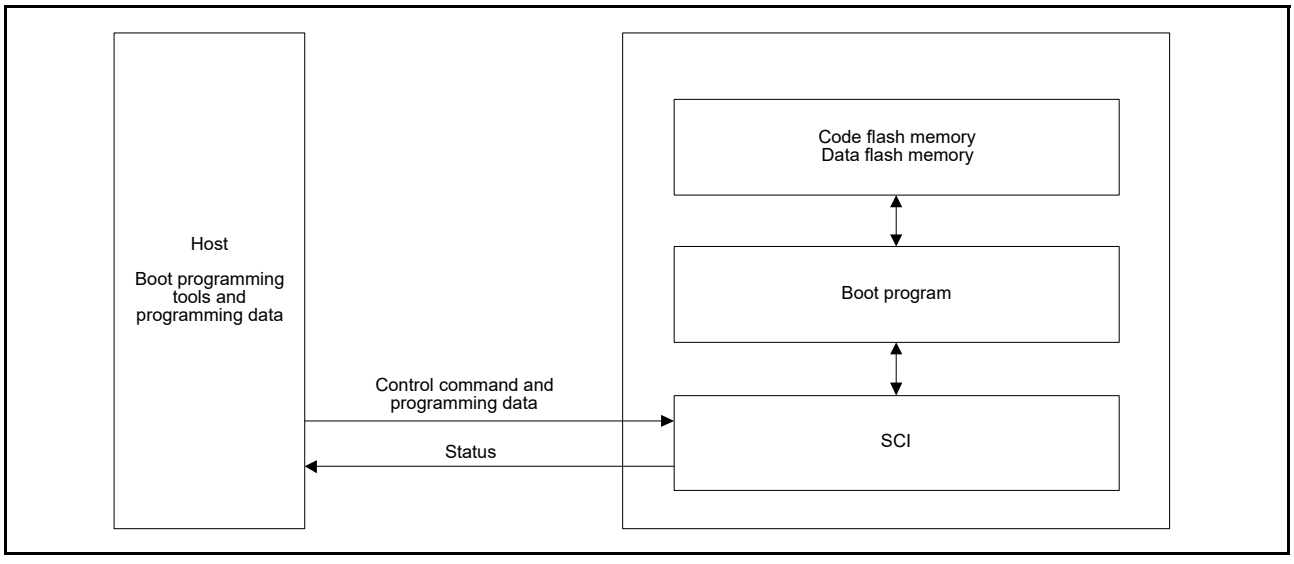


Figure 41.12 System configuration in SCI boot mode

41.11 Using a Serial Programmer

A dedicated flash memory programmer can be used to program the flash memory in serial programming mode.

41.11.1 Serial Programming

The MCU is mounted on the system board for serial programming. A connector to the board allows programming by the flash memory programmer.

41.11.2 Programming Environments

Figure 41.13 shows the environments recommended by Renesas for programming the flash memory of the MCU with data.

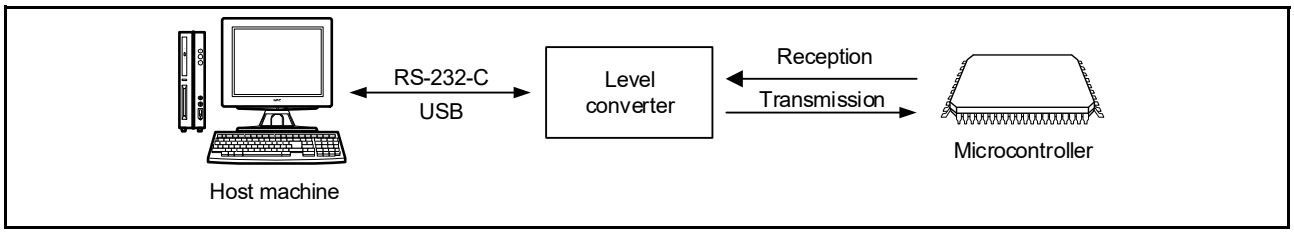


Figure 41.13 Environments for writing programs to the flash memory

41.12 Self-Programming

41.12.1 Overview

The MCU supports programming of the flash memory by the user program. The programming commands can be used with user programs for writing to the code and data flash memory. This enables upgrading of user programs and overwriting of constant data fields.

The background operation facility makes it possible to execute a program from the code flash memory to program the data flash memory under the conditions shown in Table 41.11. This program can also be copied in advance to and executed from the internal SRAM. When executing from the internal SRAM, this program can also program the code flash memory area.

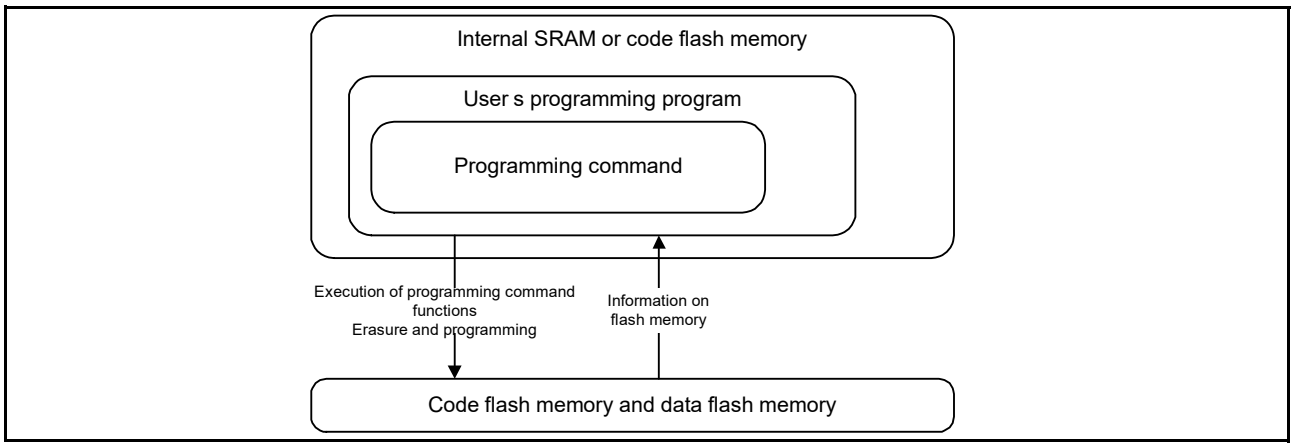


Figure 41.14 Schematic view of self-programming

41.12.2 Background Operation

Background operation can be used when a combination of the flash memory for writing and reading is as listed in Table 41.11.

Table 41.11 Conditions under which background operation is available

Product	Writable range	Readable range
All products	Data flash memory	Code flash memory
	Code flash memory	Data flash memory

41.13 Reading the Flash Memory

41.13.1 Reading the Code Flash Memory

No special settings are required to read the code flash memory in Normal mode. Data can be read by accessing addresses in the code flash memory. When reading code flash memory that was erased but not yet reprogrammed, such as code flash memory in the non-programmed state, all bits are read as 1s.

41.13.2 Reading the Data Flash Memory

No special settings are required to read the data flash memory in Normal mode. Data can be read by accessing addresses in the data flash memory. Values read from data flash memory that was erased but not yet reprogrammed, such as data flash memory in the non-programmed state, are undefined. Use the blank check function to confirm that an area is in the non-programmed state.

41.14 Usage Notes

41.14.1 Reading Areas where Programming or Erasure was Interrupted

When programming or erasure of an area of flash memory is interrupted, the data stored in the area becomes undefined. To avoid reading undefined data, which can be a source of faulty operation, do not fetch instructions or read data from areas where programming or erasure was interrupted.

41.14.2 Restrictions on Additional Writes

Other than the configuration area, no other area can be written to twice. After a write to a flash memory area is complete, erase the area before attempting to overwrite data in that area. The configuration area can be overwritten.

41.14.3 Reset during Programming and Erasure

If inputting a reset from the RES pin, release the reset after a reset input time of at least t_{RESW} (see section 43.3.3, Reset Timing) within the range of the operating voltage defined in the electrical characteristics.

41.14.4 Allocation of Vectors for Interrupts and Other Exceptions during Programming and Erasure

Generation of an interrupt or other exception during programming or erasure might lead to fetching of the vector from the code flash memory. If the vector allocation does not satisfy the conditions for using background operation, set the address for vector fetching to an address that is not in the code flash memory.

41.14.5 Restrictions during Programming and Erasure

During programming and erasure, do not:

- Permit the operating voltage from the power supply to go beyond the allowed range
- Change the frequency of the peripheral clock.

41.14.6 Abnormal Termination of Programming and Erasure

When programming or erasure ends abnormally because of the generation of a reset by the RES pin, the programming or erasure state of the flash memory with undefined data cannot be verified or checked. For the area where programming or erasure ends abnormally, the blank check function cannot determine whether the area was erased successfully. Erase the area again to ensure that the corresponding area is completely erased before use.

42. Internal Voltage Regulator

42.1 Overview

The MCU includes a linear regulator (LDO) that supplies voltage to the internal circuits and memory, except for I/O and analog.

42.2 Operation

Table 42.1 lists the LDO mode pin settings, and Figure 42.1 shows the LDO mode settings. In LDO mode, the internal voltage is generated from VCC.

Table 42.1 LDO mode pin settings

Pin	Description
All VCC pins	• Connect each pin to the system power supply • Connect each pin to VSS through a 0.1-µF multilayer ceramic capacitor. Place the capacitor close to the pin.
VCL and VCL0 pins	Connect each pin to VSS through a 0.1-µF multilayer ceramic capacitor. Place the capacitor close to the pin.

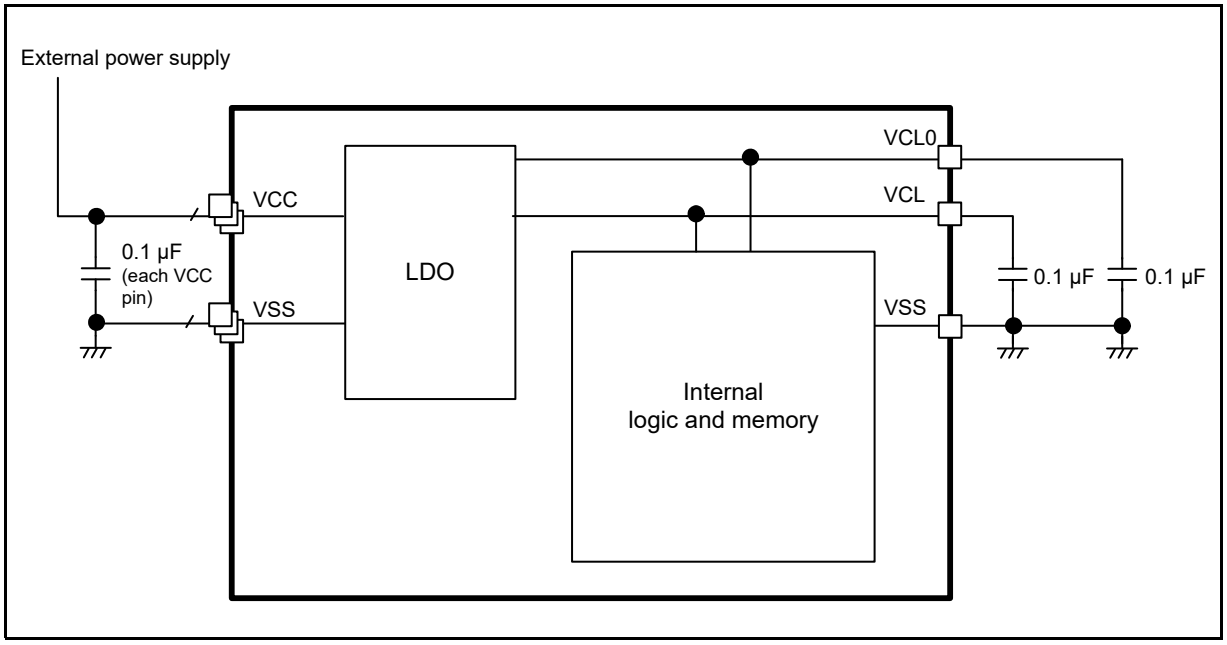


Figure 42.1 LDO mode settings

43. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 = 2.7 to 3.6 V
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL= 0 V
- $T_a = T_{opr}$.

Figure 43.1 shows the timing conditions.

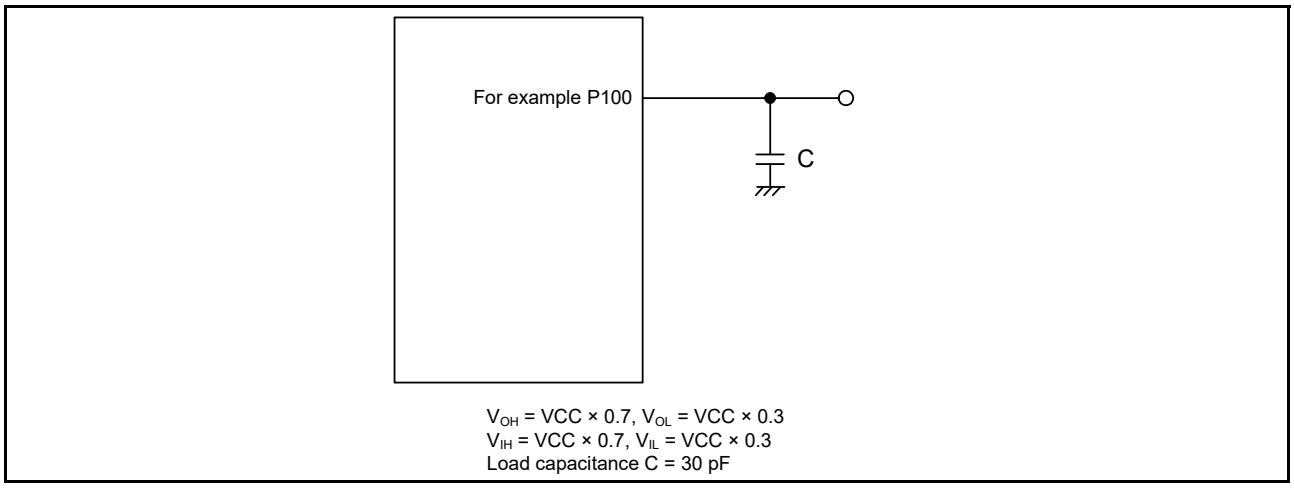


Figure 43.1 Input or output timing measurement conditions

The measurement conditions for the timing specification of each peripheral are recommended for the best peripheral operation. However, make sure to adjust the driving abilities of each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the A/C specification of each function is not guaranteed.

43.1 Absolute Maximum Ratings

Table 43.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	-0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports*1)	V_{in}	-0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports*1)	V_{in}	-0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH/VREFH0	-0.3 to AVCC0 + 0.3	V
Analog power supply voltage	AVCC0 *2	-0.3 to +4.0	V
Analog input voltage (except for P000 to P007)	V_{AN}	-0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P007) when PGA pseudo-differential input is disabled	V_{AN}	-0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P002, P004 to P006) when PGA pseudo-differential input is enabled	V_{AN}	-1.3 to AVCC0 + 0.3	V
Analog input voltage (P003, P007) when PGA pseudo-differential input is enabled	V_{AN}	-0.8 to AVCC0 + 0.3	V
Operating temperature*3, *4	T_{opr}	-40 to +105	°C
Storage temperature	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Note 1. Ports P205, P206, P400, P401, P407 to P415, and P708 are 5 V tolerant.
Note 2. Connect AVCC0 to VCC.

Note 3. See section 43.2.1, T_j/T_a Definition.

Note 4. Contact Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Table 43.2 Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltages	VCC	2.7	-	3.6	V
	VSS	-	0	-	V
Analog power supply voltages	AVCC0*1	-	VCC	-	V
	AVSS0	-	0	-	V

Note 1. Connect AVCC0 to VCC. When the A/D converter, the D/A converter, or the comparator are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

43.2 DC Characteristics

43.2.1 T_j/T_a Definition

Table 43.3 DC characteristics
Conditions: Products with operating temperature (T_a) -40 to +105°C.

Parameter		Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	100-pin LQFP 64-pin LQFP	T_j	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode.

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W),
where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

43.2.2 I/O V_{IH}, V_{IL}

Table 43.4 I/O V_{IH}, V_{IL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL(external clock input), SPI (except RSPCK)	V_{IH}	VCC × 0.8	-	-	V
			V_{IL}	-	-	VCC × 0.2	
		IIC (SMBus)*1	V_{IH}	2.1	-	-	
			V_{IL}	-	-	0.8	
		IIC (SMBus)*2	V_{IH}	2.1	-	VCC + 3.6 (max 5.8)	
			V_{IL}	-	-	0.8	
Schmitt trigger input voltage		IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	-	-	
			V_{IL}	-	-	VCC × 0.3	
			ΔV_T	VCC × 0.05	-	-	
		IIC (except for SMBus)*2	V_{IH}	VCC × 0.7	-	VCC + 3.6 (max 5.8)	
			V_{IL}	-	-	VCC × 0.3	
			ΔV_T	VCC × 0.05	-	-	
		5 V-tolerant ports*3, *7	V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	
			V_{IL}	-	-	VCC × 0.2	
			ΔV_T	VCC × 0.05	-	-	

Table 43.4 I/O V_{IH}, V_{IL} (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	P402/AGTIO0,1 P403/AGTIO0,1	V_{IH}	VCC × 0.8	-	VCC + 0.3	V
			V_{IL}	-	-	VCC × 0.2	
			ΔV_T	VCC × 0.05	-	-	
		Other input pins*4	V_{IH}	VCC × 0.8	-	-	
			V_{IL}	-	-	VCC × 0.2	
			ΔV_T	VCC × 0.05	-	-	
	Ports	5 V-tolerant ports*5, *7	V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	
			V_{IL}	-	-	VCC × 0.2	
		Other input pins*6	V_{IH}	VCC × 0.8	-	-	
			V_{IL}	-	-	VCC × 0.2	

Note 1. SCL1_B, SDA1_B (total 2 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A (total 6 pins).
Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P708 (total 15 pins).
Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. P205, P206, P400, P401, P407 to P415, P708 (total 14 pins).
Note 6. All input pins except for the ports already described in the table.
Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the breakdown voltage.

43.2.3 I/O I_{OH}, I_{OL}

Table 43.5 I/O I_{OH}, I_{OL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P008, P201	-	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P205, P206, P407 to P415, P602, P708 (total 13 pins)	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-20	mA
			I_{OL}	-	-	20	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-16	mA
			I_{OL}	-	-	16	mA

Table 43.5 I/O I_{OH}, I_{OL} (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (max value per pin)	Ports P008, P201	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P205, P206, P407 to P415, P602, P708 (total 13 pins)	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-40	mA
			I_{OL}	-	-	40	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-32	mA
			I_{OL}	-	-	32	mA
Permissible output current (max value of total of all pins)	Maximum of all output pins		$\Sigma I_{OH\ (max)}$	-	-	-80	mA
			$\Sigma I_{OL\ (max)}$	-	-	80	mA

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. Except for P000 to P007, P200, which are input ports.

43.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 43.6 I/O V_{OH}, V_{OL}, and other characteristics (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	IIC*1		V_{OL}	-	-	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			V_{OL}	-	0.4	-		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	Ports P205, P206, P407 to P415, P602, P708 (total of 13 pins)*2		V_{OH}	VCC - 1.0	-	-		I_{OH} = -20 mA VCC = 3.3 V
			V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins		V_{OH}	VCC - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
Input leakage current	RES		$\lvert I_{in} \rvert$	-	-	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Ports P000 to P002, P004 to P006, P200			-	-	1.0		V_{in} = 0 V V_{in} = VCC
	Ports P003, P007	Before initialization*3		-	-	45.0		V_{in} = 0 V V_{in} = VCC
		After initialization*4		-	-	1.0		V_{in} = 0 V V_{in} = VCC

Table 43.6 I/O V_{OH}, V_{OL}, and other characteristics (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Three-state leakage current (off state)	5 V-tolerant ports	$\|I_{TSI}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for ports P000 to P007, P200)		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0 to P7 (except for ports P000 to P007)	I_p	-300	-	-10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	Ports P003, P007, P014, P015, P400, P401	C_{in}	-	-	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	Other input pins		-	-	8		

Note 1. SCL0_A, SDA0_A (total 2 pins).
Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. P0nPFS.ASEL(n = 3 or 7) = 1
Note 4. P0nPFS.ASEL(n = 3 or 7) = 0

43.2.5 Operating and Standby Current

Table 43.7 Operating and standby current (1 of 2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current*1	High-speed mode	Maximum*2		I_{CC}*3	-	-	87	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz
		CoreMark®*5			-	17	-		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4		-	24	-		
			All peripheral clocks disabled, while (1) code executing from flash*5, *6		-	12	-		
		Sleep mode*5, *6			-	9	33.5		
		Increase during BGO operation	Data flash P/E		-	6	-		
			Code flash P/E		-	8	-		
	Low-speed mode*5				-	1.2	-		ICLK = 1 MHz
	Subosc-speed mode*5				-	1.0	-		ICLK = 32.768 kHz
	Software Standby mode				-	1.3	13		Ta ≤ 85°C
					-	1.3	21		Ta ≤ 105°C
	Deep Software Standby mode	DPSBYCR.DEEPCUT[1:0] = 00b*8			-	28	65	μA	Ta ≤ 85°C
					-	28	93		Ta ≤ 105°C
		DPSBYCR.DEEPCUT[1:0] = 01b*8			-	11.6	28		Ta ≤ 85°C
					-	11.6	32		Ta ≤ 105°C
		DPSBYCR.DEEPCUT[1:0] = 11b*8			-	4.9	21		Ta ≤ 85°C
					-	4.9	26		Ta ≤ 105°C
		Increase when the AGT is operating	When the low-speed on-chip oscillator (LOCO) is in use		-	4.4	-		-
			When a crystal oscillator for low clock loads is in use		-	1.0	-		-
			When a crystal oscillator for standard clock loads is in use		-	1.4	-		-
Analog power supply current	During 12-bit A/D conversion			AI_{CC}	-	0.8	1.1	mA	-
	During 12-bit A/D conversion with S/H amp				-	2.3	3.3	mA	-
	PGA (1ch)				-	1	3	mA	-
	ACMPHS (1 unit)				-	100	150	μA	-
	Temperature sensor				-	0.1	0.2	mA	-
	During D/A conversion (per unit)		Without AMP output		-	0.1	0.2	mA	-
			With AMP output		-	0.6	1.1	mA	-
	Waiting for A/D, D/A conversion (all units)				-	0.9	1.6	mA	-
	ADC12, DAC12 in standby modes (all units)*7				-	2	8	μA	-

Table 43.7 Operating and standby current (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)		AI_{REFH0}	-	70	120	μA	-
	Waiting for 12-bit A/D conversion (unit 0)			-	0.07	0.5	μA	-
	ADC12 in standby modes (unit 0)			-	0.07	0.5	μA	-
Reference power supply current (VREFH)	During 12-bit A/D conversion (unit 1)		AI_{REFH}	-	70	120	μA	-
	During D/A conversion (per unit)	Without AMP output		-	0.1	0.4	mA	-
		With AMP ouput		-	0.1	0.4	mA	-
	Waiting for 12-bit A/D (unit 1), D/A (all units) conversion			-	0.07	0.8	μA	-
	ADC12 unit 1 in standby modes			-	0.07	0.8	μA	-

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB:PCLKC:PCLKD = 2:2:1:1:2)
I_{CC} Max. = 0.53 x f + 23 (maximum operation in High-speed mode)
I_{CC} Typ. = 0.08 x f + 2.4 (normal operation in High-speed mode)
I_{CC} Typ. = 0.1 x f + 1.1 (Low-speed mode)
I_{CC} Max. = 0.09 x f + 23 (Sleep mode).
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).
Note 7. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-bit A/D Converter 0 Module Stop bit) and MSTPCRD.MSTPD15 (12-bit A/D Converter 1 Module Stop bit) are in the module-stop state.
See section 35.6.8, Available functions and register settings of AN000 to AN002, AN007, AN100 to AN102, and AN107.
Note 8. For more information on the DBSBYCR register, see section 11.2.11, Deep Software Standby Control Register (DPSBYCR).

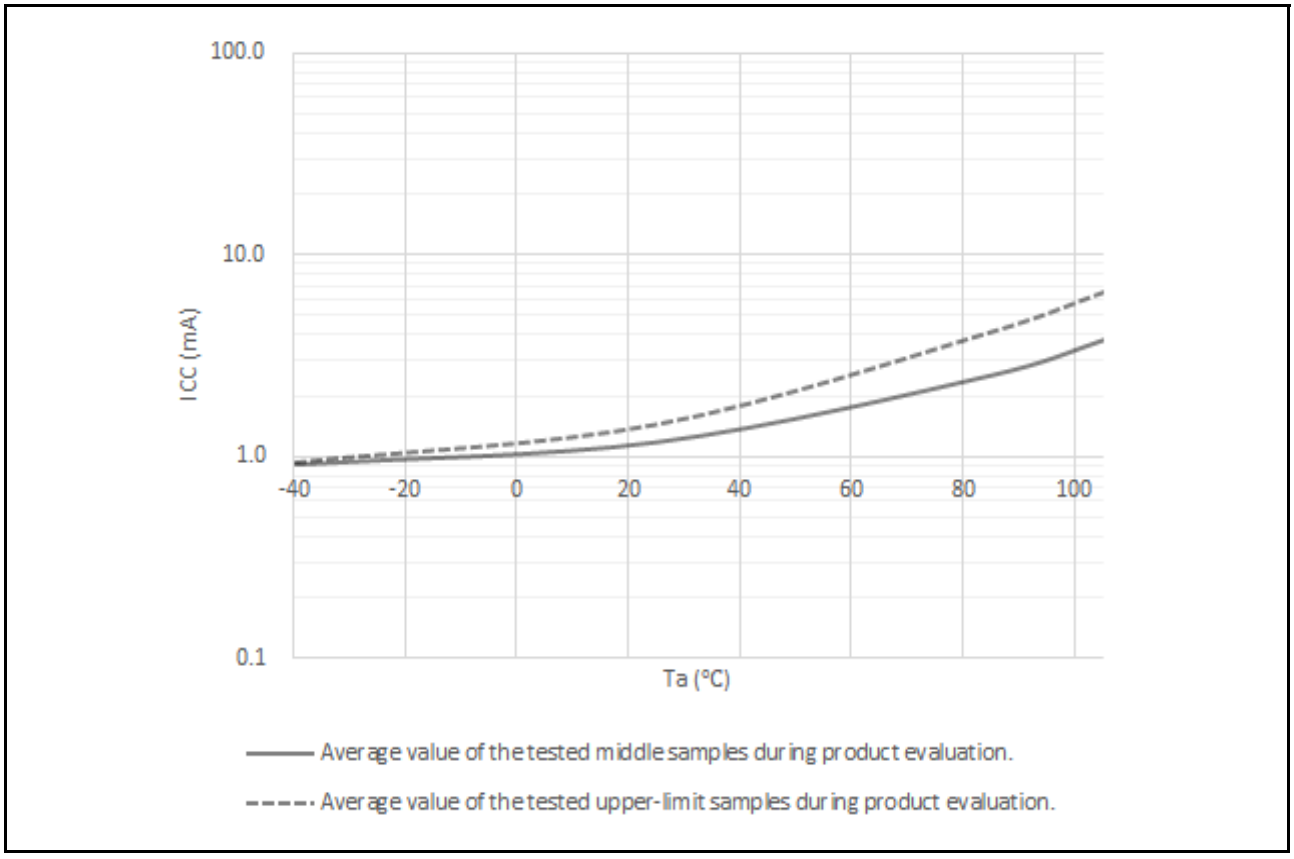


Figure 43.2 Temperature dependency in Software Standby mode (reference data)

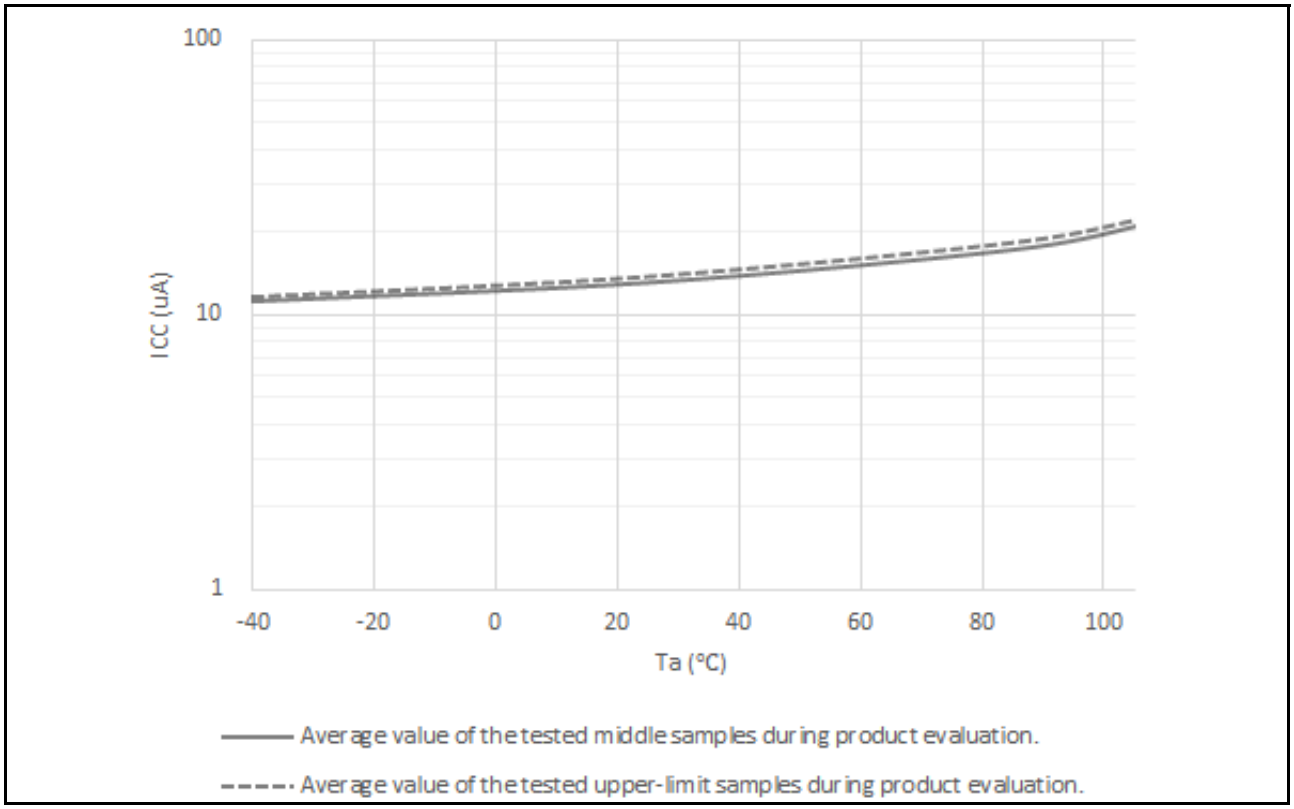


Figure 43.3 Temperature dependency in Deep Software Standby mode, power-on reset circuit low power function disabled (reference data)

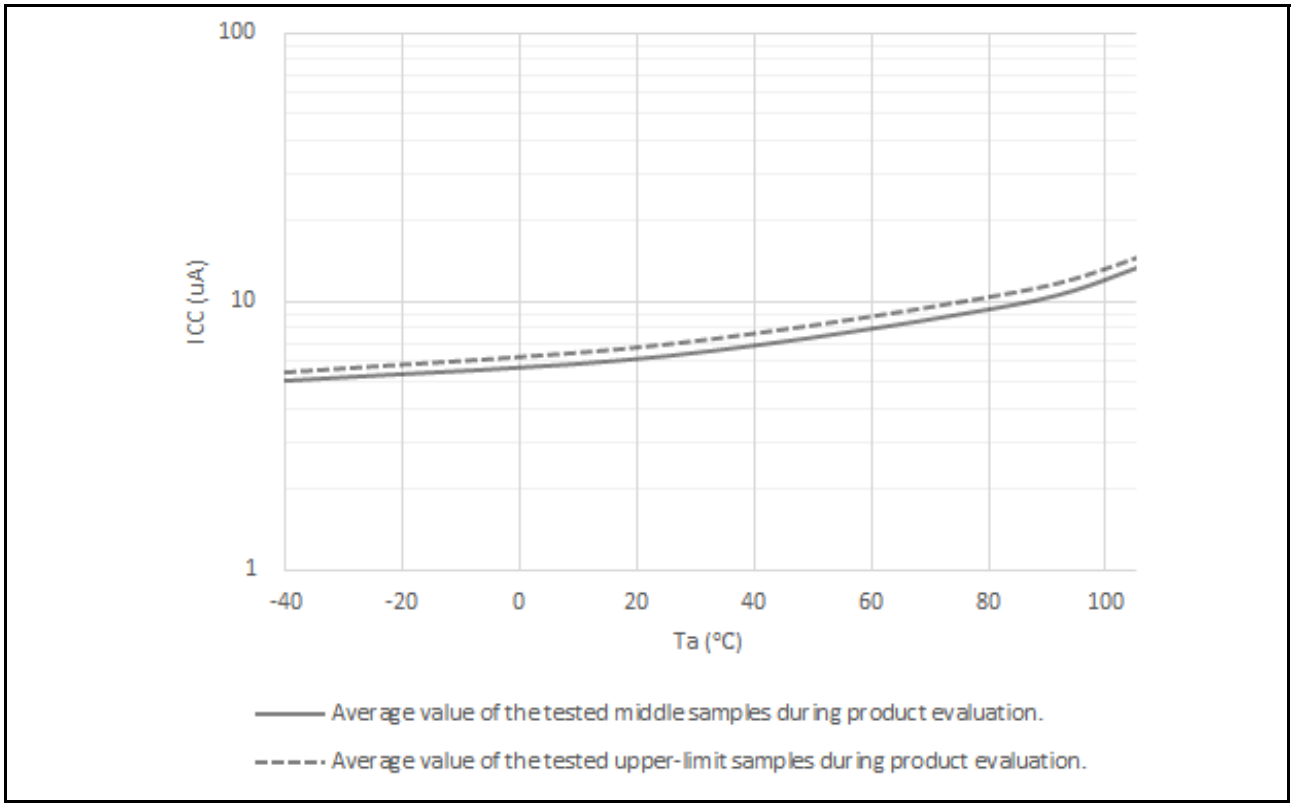


Figure 43.4 Temperature dependency in Deep Software Standby mode, power-on reset circuit low power function enabled (reference data)

43.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 43.8 Rising gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	-	20	ms/V	-
	Voltage monitor 0 reset enabled at startup		0.0084	-	-		-
	SCI boot mode*1		0.0084	-	20		-

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Table 43.9 Rise and fall gradient and ripple frequency characteristics
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	-	-	10	kHz	Figure 43.5 $V_{r\ (VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 43.5 $V_{r\ (VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 43.5 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC ±10%

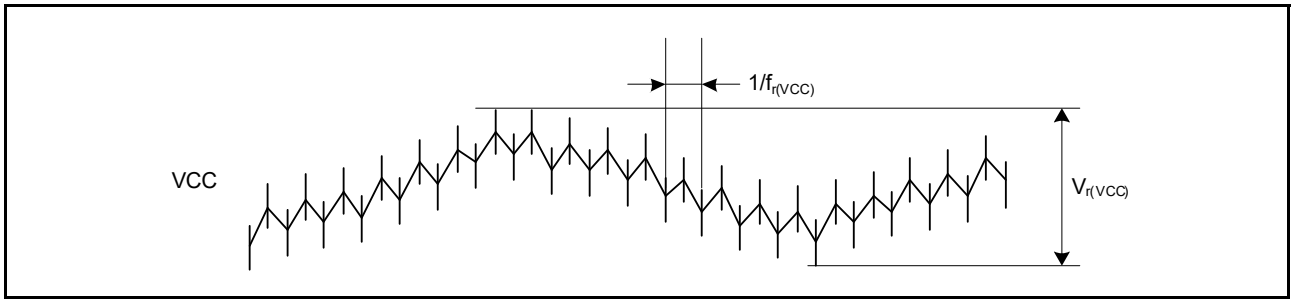


Figure 43.5 Ripple waveform

43.3 AC Characteristics

43.3.1 Frequency

Table 43.10 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK*2)	f	-	-	120	MHz
	Peripheral module clock (PCLKA)*2		-	-	120	
	Peripheral module clock (PCLKB)*2		-	-	60	
	Peripheral module clock (PCLKC)*2		-*3	-	60	
	Peripheral module clock (PCLKD)*2		-	-	120	
	Flash interface clock (FCLK)*2		-*1	-	60	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. See section 9, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 43.11 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	-	-	1	MHz
	Peripheral module clock (PCLKA)*2		-	-	1	
	Peripheral module clock (PCLKB)*2		-	-	1	
	Peripheral module clock (PCLKC)*2,*3		-*3	-	1	
	Peripheral module clock (PCLKD)*2		-	-	1	
	Flash interface clock (FCLK)*1, *2		-	-	1	

Note 1. Programming or erasing the flash memory is disabled in Low-speed mode.
Note 2. See section 9, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

Table 43.12 Operation frequency value in Subosc-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	29.4	-	36.1	kHz
	Peripheral module clock (PCLKA)*2		-	-	36.1	
	Peripheral module clock (PCLKB)*2		-	-	36.1	
	Peripheral module clock (PCLKC)*2,*3		-	-	36.1	
	Peripheral module clock (PCLKD)*2		-	-	36.1	
	Flash interface clock (FCLK)*1, *2		29.4	-	36.1	

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.
Note 2. See section 9, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.
Note 3. The ADC12 cannot be used.

43.3.2 Clock Timing

Table 43.13 Clock timing except for sub-clock oscillator (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	-	-	ns	Figure 43.6
EXTAL external clock input high pulse width	t_{EXH}	15.83	-	-	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	-	-	ns	
EXTAL external clock rise time	t_{EXr}	-	-	5.0	ns	
EXTAL external clock fall time	t_{EXf}	-	-	5.0	ns	
Main clock oscillator frequency	f_{MAIN}	8	-	24	MHz	-
Main clock oscillation stabilization wait time (crystal) *1	$t_{MAINOSCWT}$	-	-	-*1	ms	Figure 43.7
LOCO clock oscillation frequency	f_{LOCO}	29.4912	32.768	36.0448	kHz	-
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	-	-	60.4	µs	Figure 43.8
ILOCO clock oscillation frequency	f_{ILOCO}	13.5	15	16.5	kHz	-
MOCO clock oscillation frequency	F_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization wait time	t_{MOCOWT}	-	-	15.0	µs	-

Table 43.13 Clock timing except for sub-clock oscillator (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	-20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		-40 ≤ Ta ≤ -20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.955	16	16.045		-40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.949	18	18.051		
		f_{HOCO20}	19.944	20	20.056		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	-	-	64.7	µs	-
FLL stabilization wait time		t_{FLLWT}	-	-	1.8	ms	-
PLL clock frequency		f_{PLL}	120	-	240	MHz	-
PLL clock oscillation stabilization wait time		t_{PLLWT}	-	-	174.9	µs	Figure 43.9

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (fHOCO) reaches the range for guaranteed operation.

Table 43.14 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	-	-	-*1	s	Figure 43.10

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

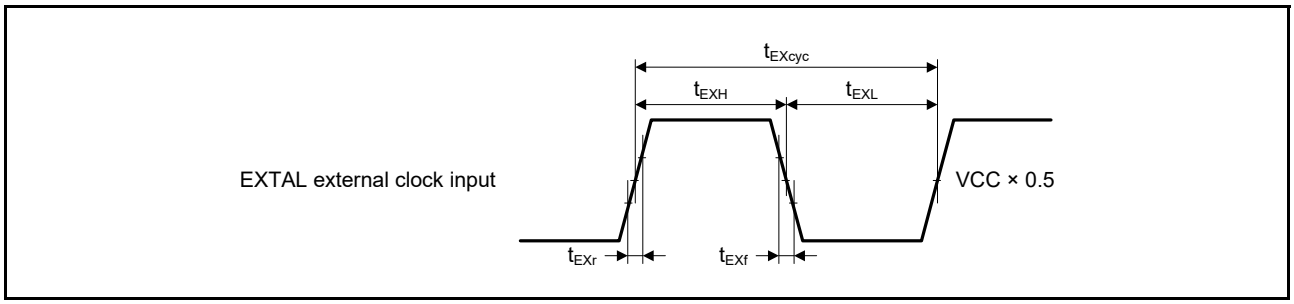


Figure 43.6 EXTAL external clock input timing

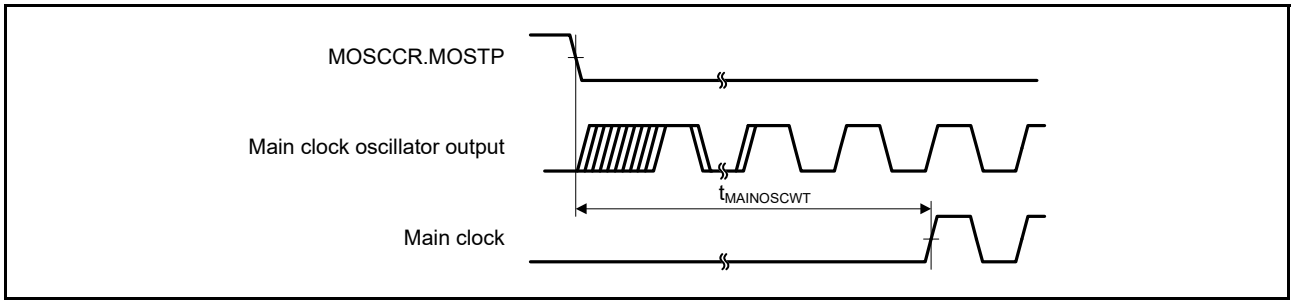


Figure 43.7 Main clock oscillation start timing

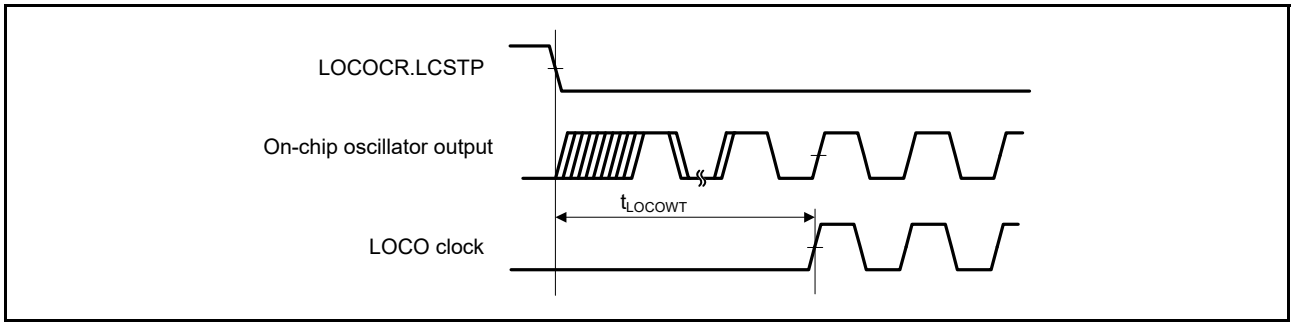


Figure 43.8 LOCO clock oscillation start timing

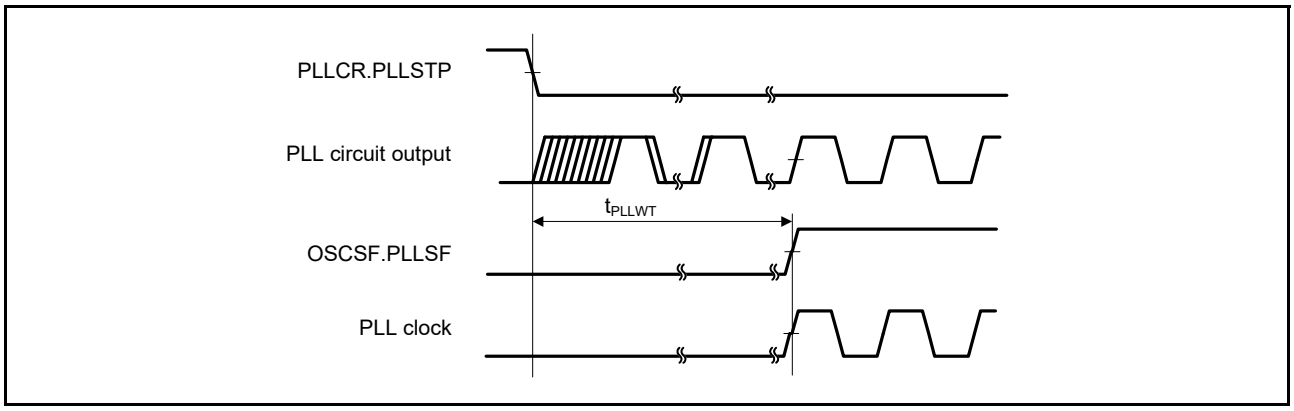


Figure 43.9 PLL clock oscillation start timing

Note: Only operate the PLL after the main clock oscillation has stabilized.

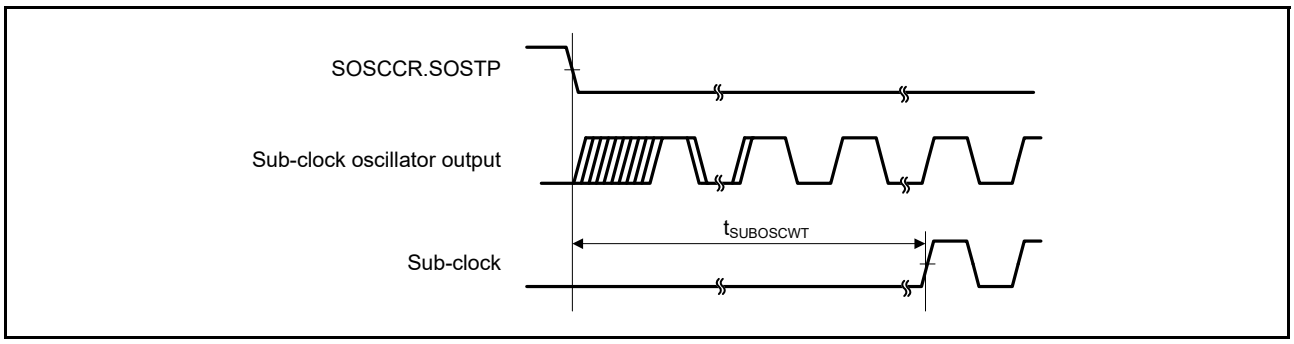


Figure 43.10 Sub-clock oscillation start timing

43.3.3 Reset Timing

Table 43.15 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	1	-	-	ms	Figure 43.11
	Deep Software Standby mode	t_{RESWD}	0.6	-	-	ms	Figure 43.12
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	-	-	ms	
	All other	t_{RESW}	200	-	-	µs	
Wait time after RES cancellation		t_{RESWT}	-	29	32	µs	Figure 43.11
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset)		t_{RESW2}	-	320	390	µs	-

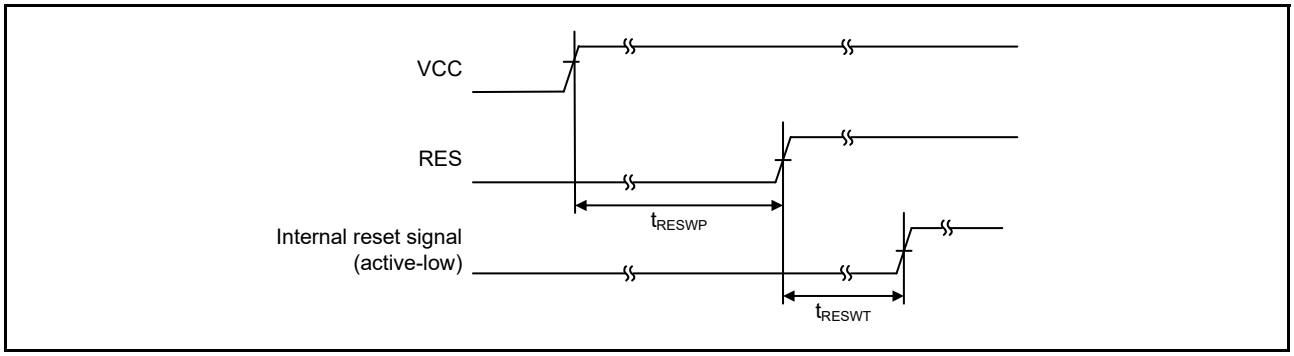


Figure 43.11 Power-on reset timing

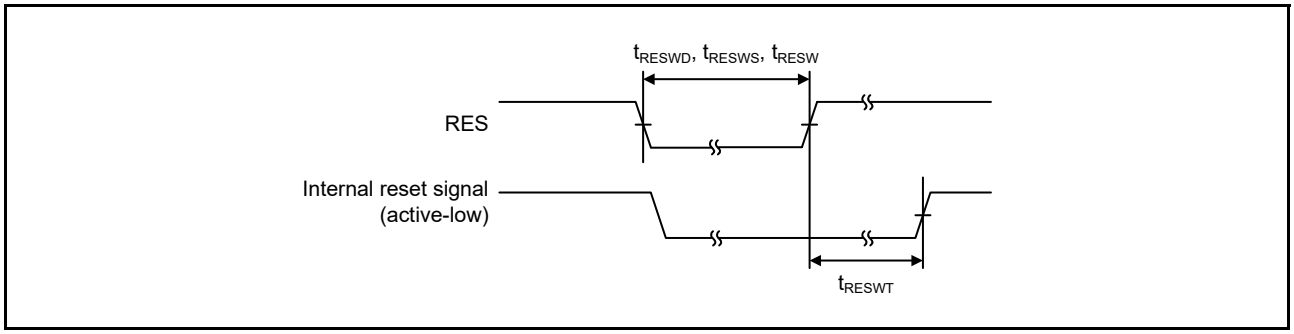


Figure 43.12 Reset input timing

43.3.4 Wakeup Timing

Table 43.16 Timing of recovery from low power modes

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}	-	2.4*9	2.8*9	ms	Figure 43.13 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}	-	2.7*9	3.2*9	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}	-	230*9	280*9	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}	-	570*9	700*9	µs	
	System clock source is sub-clock oscillator*8		t_{SBYSC}	-	1.2*9	1.3*9	ms	
	System clock source is LOCO*8		t_{SBYLO}	-	1.2*9	1.4*9	ms	
	System clock source is HOCO*6		t_{SBYHO}	-	240*9, *10	300 *9, *10	µs	
	System clock source is MOCO*7		t_{SBYMO}	-	220*9	300*9	µs	
Recovery time from Deep Software Standby mode			t_{DSBY}	-	0.65	1.0	ms	Figure 43.14
Wait time after cancellation of Deep Software Standby mode			t_{DSBYWT}	34	-	35	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)		t_{SNZ}	-	35*9, *10	70 *9, *10	µs	Figure 43.15
	High-speed mode when system clock source is MOCO (8 MHz)		t_{SNZ}	-	11*9	14*9	µs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPC0 = 0 (CAC module stop)).

Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 00h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 00h))

Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 00h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 00h))

Note 6. The HOCO frequency is 20 MHz.

Note 7. The MOCO frequency is 8 MHz.

Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.

Note 9. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time:
STCONR.STCON[1:0] = 00b:16 µs (typical), 34 µs (maximum)
STCONR.STCON[1:0] = 11b:16 µs (typical), 104 µs (maximum).

Note 10. When the SNZCR.RXDREQEN bit is set to 0, 16 µs (typical) or 18 µs (maximum) is added as the HOCO wait time.

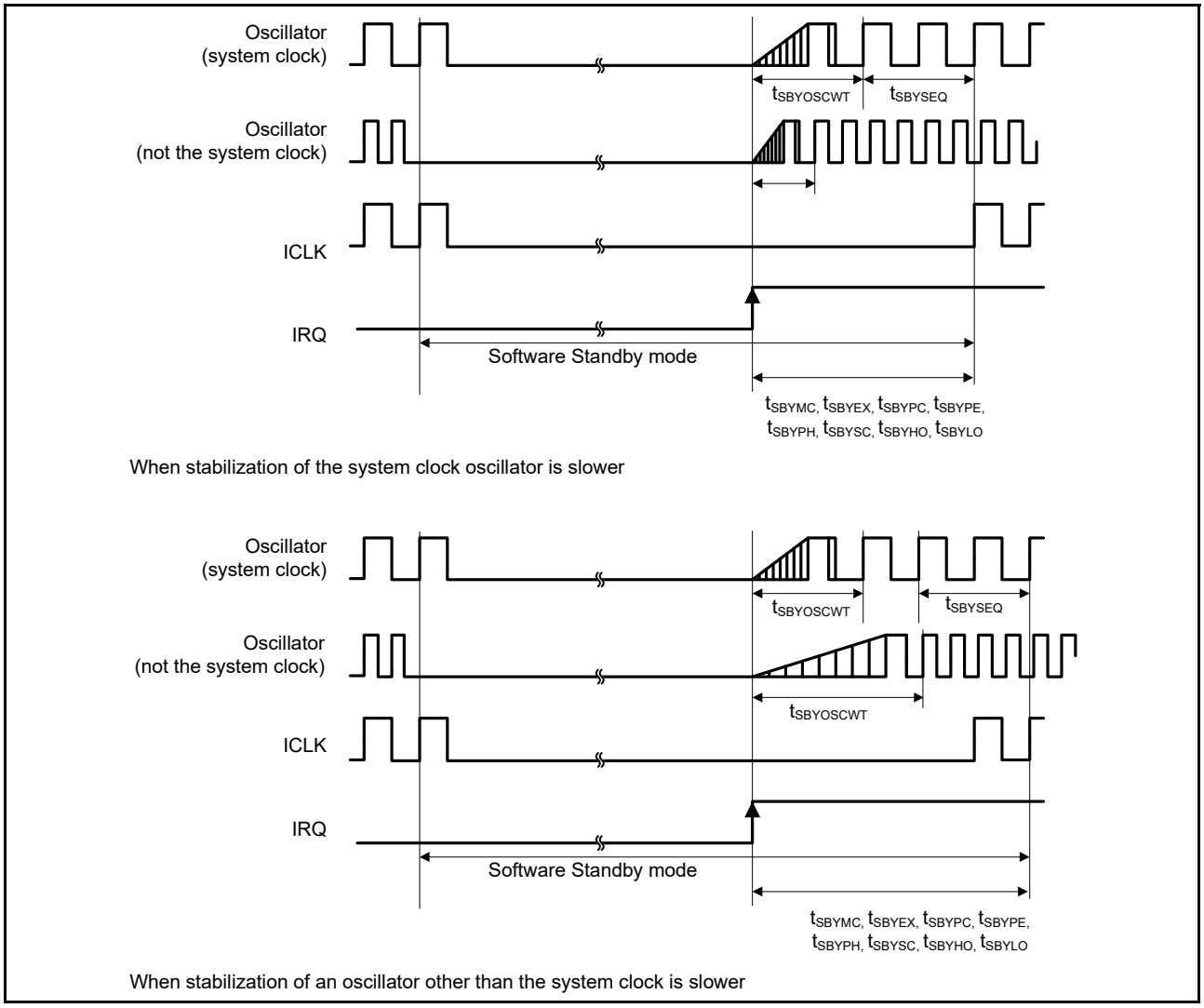


Figure 43.13 Software Standby mode cancellation timing

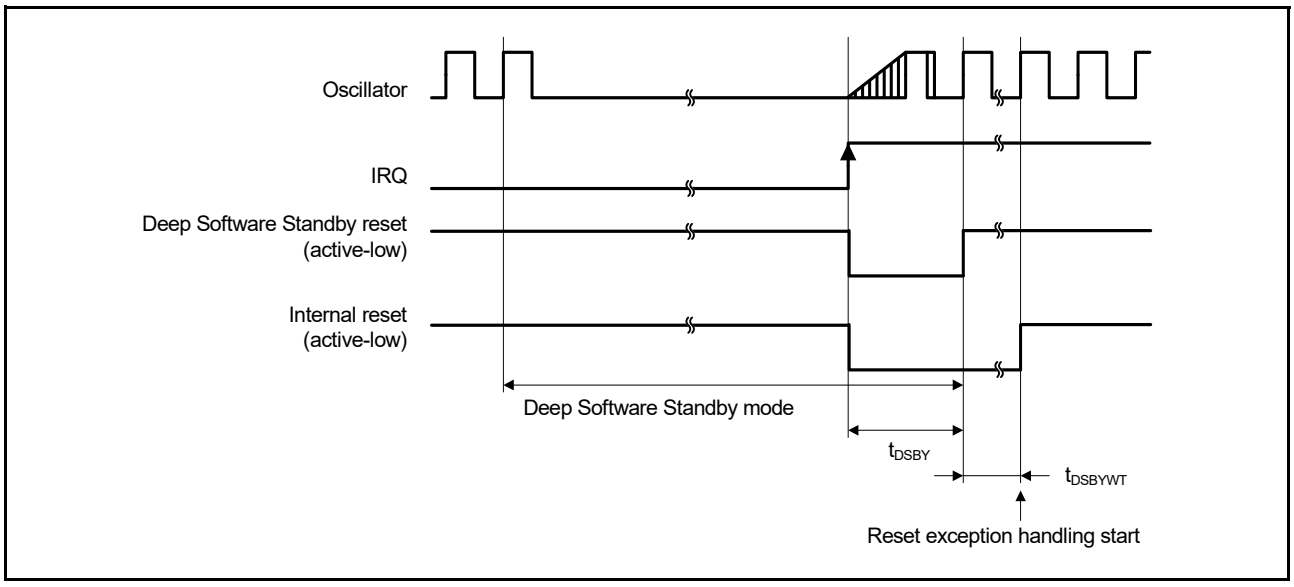
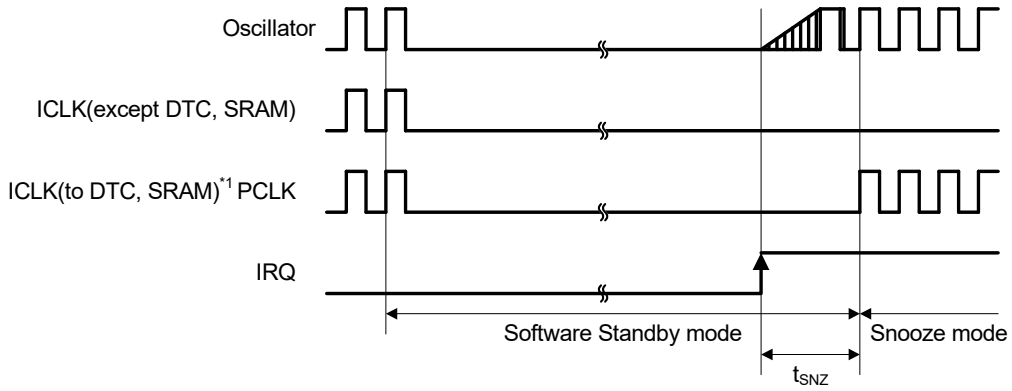


Figure 43.14 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN is set to 1, ICLK is supplied to DTC and SRAM.

Figure 43.15 Recovery timing from Software Standby mode to Snooze mode

43.3.5 NMI and IRQ Noise Filter

Table 43.17 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

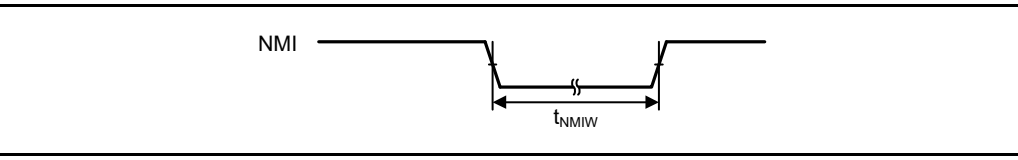


Figure 43.16 NMI interrupt input timing

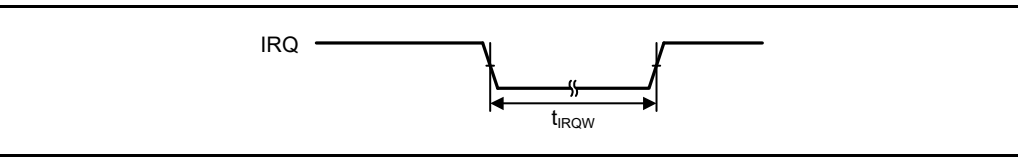


Figure 43.17 IRQ interrupt input timing

43.3.6 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

Table 43.18 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing
GPT32 conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	-	t_{Pcyc}	Figure 43.18
POEG	POEG input trigger pulse width		t_{POEW}	3	-	t_{Pcyc}	Figure 43.19
GPT32	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 43.20
		Dual edge		2.5	-		
	GTIOCxY output skew (x = 0 to 7, Y= A or B)	Middle drive buffer	t_{GTISK}*1	-	4	ns	Figure 43.21
		High drive buffer		-	4		
	GTIOCxY output skew (x = 8 to 12, Y = A or B)	Middle drive buffer		-	4		
		High drive buffer		-	4		
	GTIOCxY output skew (x = 0 to 12, Y = A or B)	Middle drive buffer		-	6		
		High drive buffer		-	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	-	5	ns	Figure 43.22
GPT (PWM Delay Generation Circuit)	GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A)		t_{HRSK}*2	-	2.0	ns	Figure 43.23
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*3	100	-	ns	Figure 43.24
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	-	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 43.25
KINT	KRn(n = 00 to 07) pulse width		t_{KR}	250	-	ns	Figure 43.26

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. The load is 30 pF.
Note 3. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

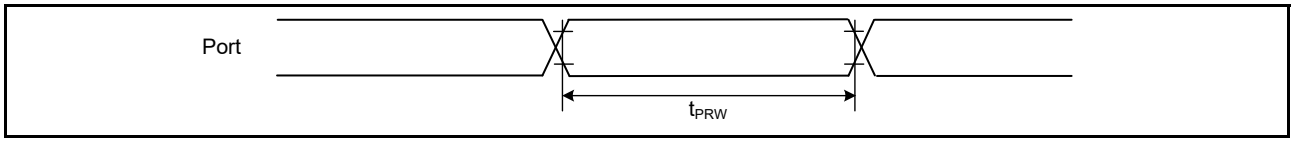


Figure 43.18 I/O ports input timing

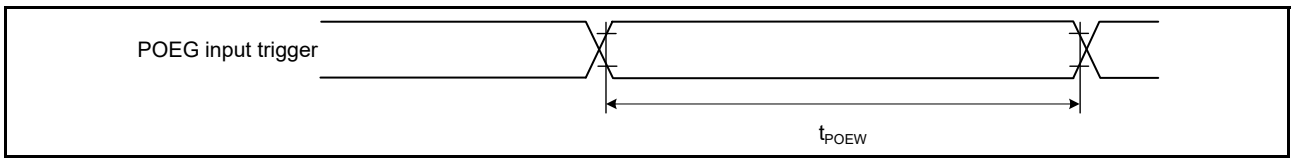


Figure 43.19 POEG input trigger timing

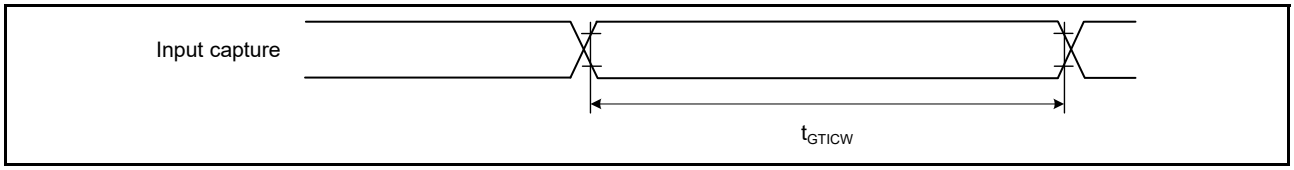


Figure 43.20 GPT32 input capture timing

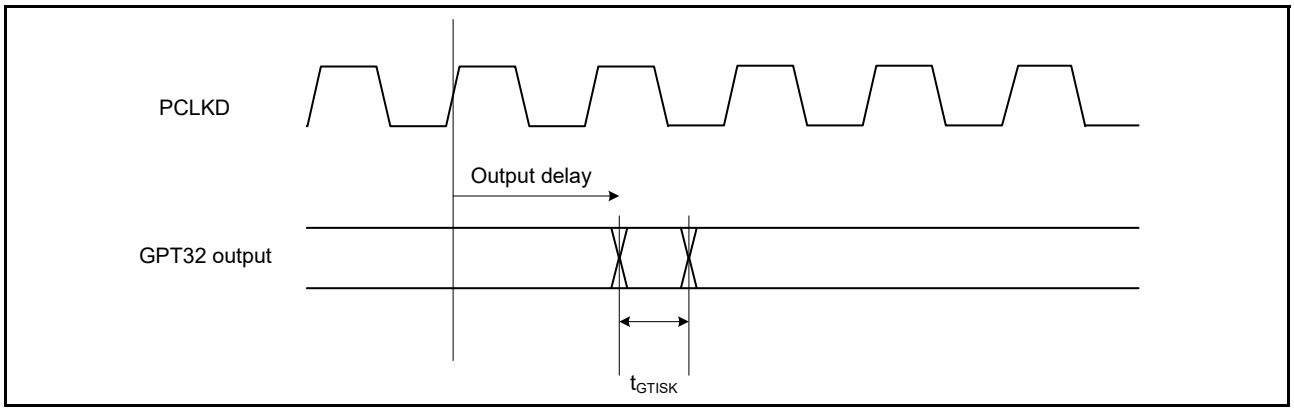


Figure 43.21 GPT32 output delay skew

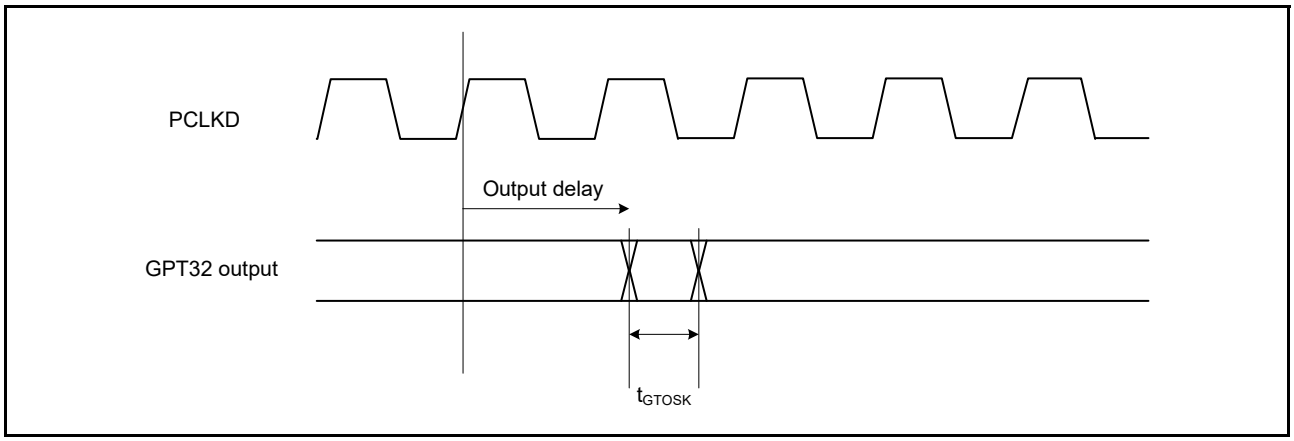


Figure 43.22 GPT32 output delay skew for OPS

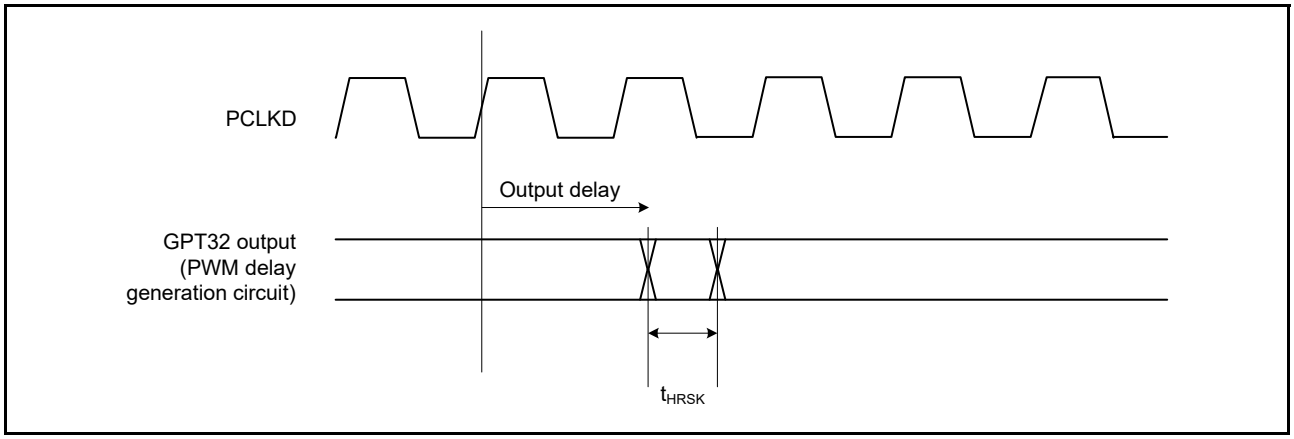


Figure 43.23 GPT32 (PWM delay generation circuit) output delay skew

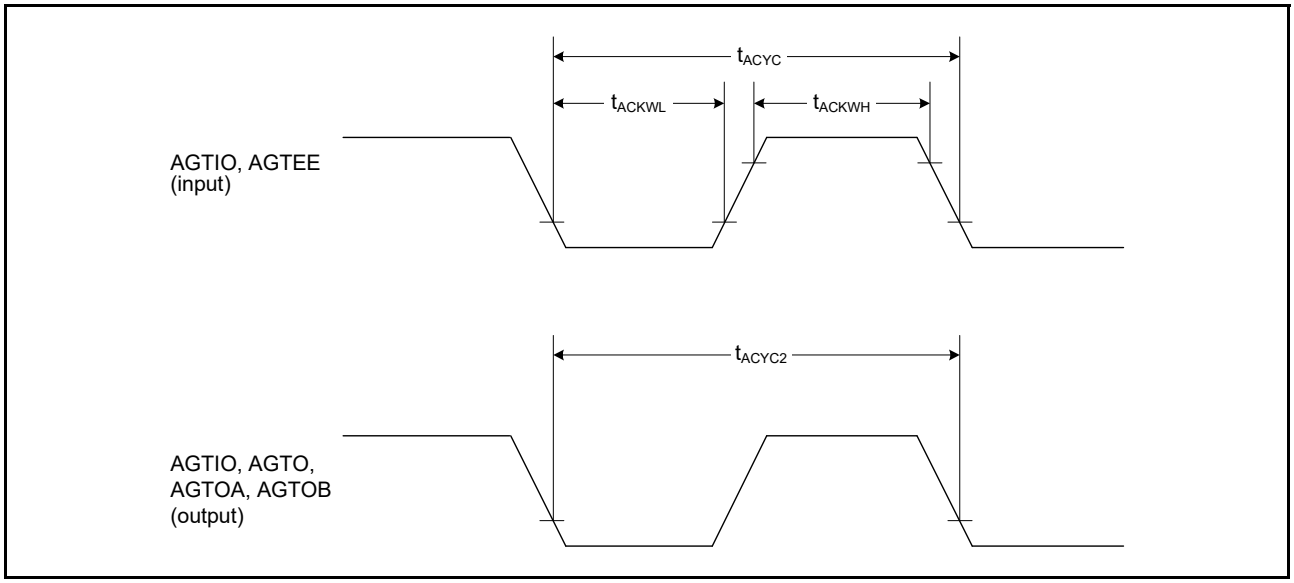


Figure 43.24 AGT input/output timing

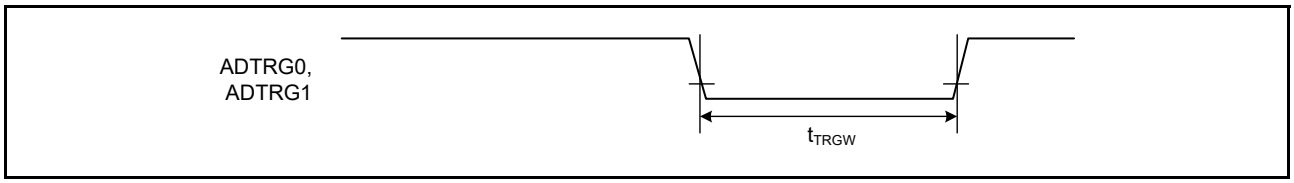


Figure 43.25 ADC12 trigger input timing

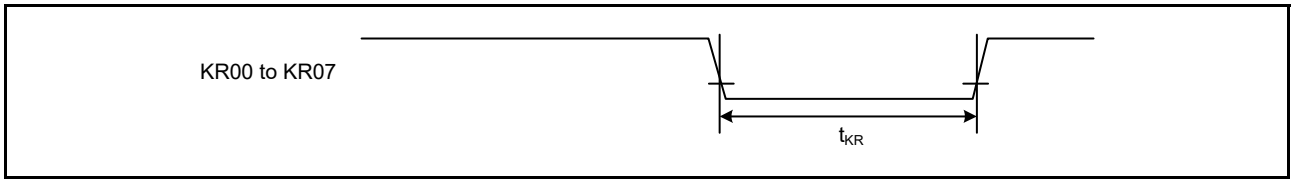


Figure 43.26 Key interrupt input timing

43.3.7 PWM Delay Generation Circuit Timing

Table 43.19 PWM Delay Generation Circuit timing

Parameter	Min	Typ	Max	Unit	Test conditions
Operation frequency	80	-	120	MHz	-
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

43.3.8 CAC Timing

Table 43.20 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > t_{cac}$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. t_{cac}: CAC count clock source cycle.

43.3.9 SCI Timing

Table 43.21 SCI timing (1)
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SCK0 to SCK4, SCK8, SCK9.
For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 43.27
		Clock synchronous		6	-		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	-	5	ns	
	Input clock fall time		t_{SCKf}	-	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous		4	-		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	-	5	ns	
	Output clock fall time		t_{SCKf}	-	5	ns	
	Transmit data delay	Clock synchronous	t_{TXD}	-	25	ns	Figure 43.28
	Receive data setup time	Clock synchronous	t_{RXS}	15	-	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

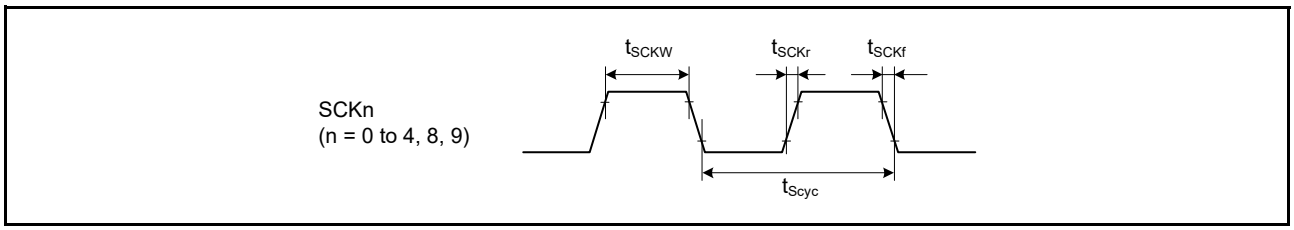


Figure 43.27 SCK clock input/output timing

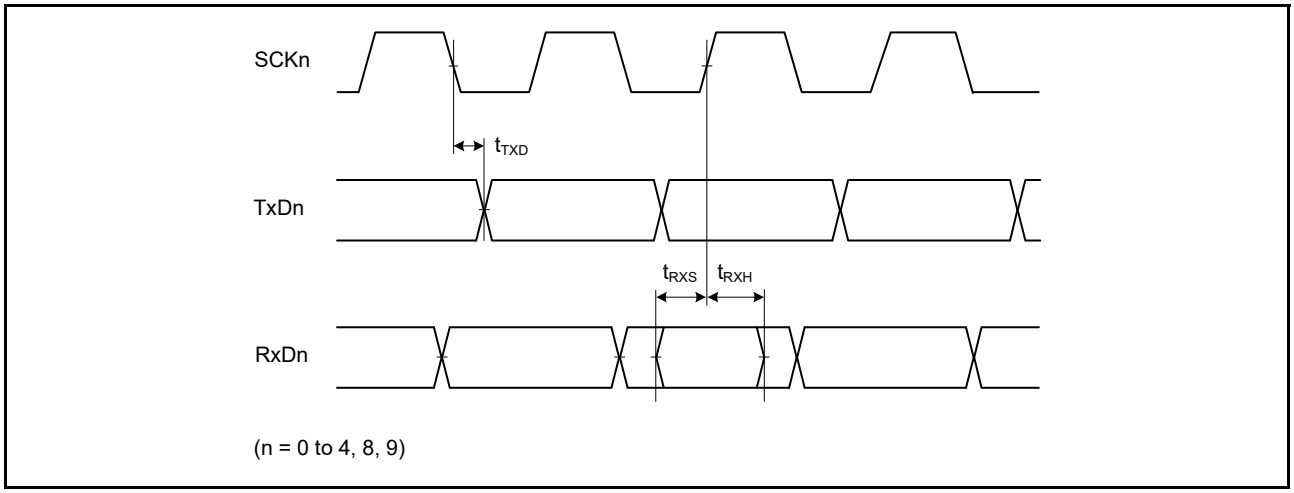


Figure 43.28 SCI input/output timing in clock synchronous mode

Table 43.22 SCI timing (2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SCK0 to SCK4, SCK8, SCK9.
For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	65536	t_{Pcyc}	Figure 43.29
	SCK clock cycle input (slave)	-	6 (PCLKA ≤ 60 MHz) 12 (PCLKA > 60 MHz)	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time	t_{SPCKr}, t_{SPCKf}	-	20	ns	
	Data input setup time	t_{SU}	33.3	-	ns	Figure 43.30 to Figure 43.33
	Data input hold time	t_{H}	33.3	-	ns	
	SS input setup time	t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	t_{OD}	-	33.3	ns	
	Data output hold time	t_{OH}	-10	-	ns	
	Data rise and fall time	t_{Dr}, t_{Df}	-	16.6	ns	
	SS input rise and fall time	t_{SSLr}, t_{SSLf}	-	16.6	ns	
	Slave access time	t_{SA}	-	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	t_{Pcyc}	Figure 43.33
	Slave output release time	t_{REL}	-	5 (PCLKA ≤ 60 MHz) 10 (PCLKA > 60 MHz)	t_{Pcyc}	

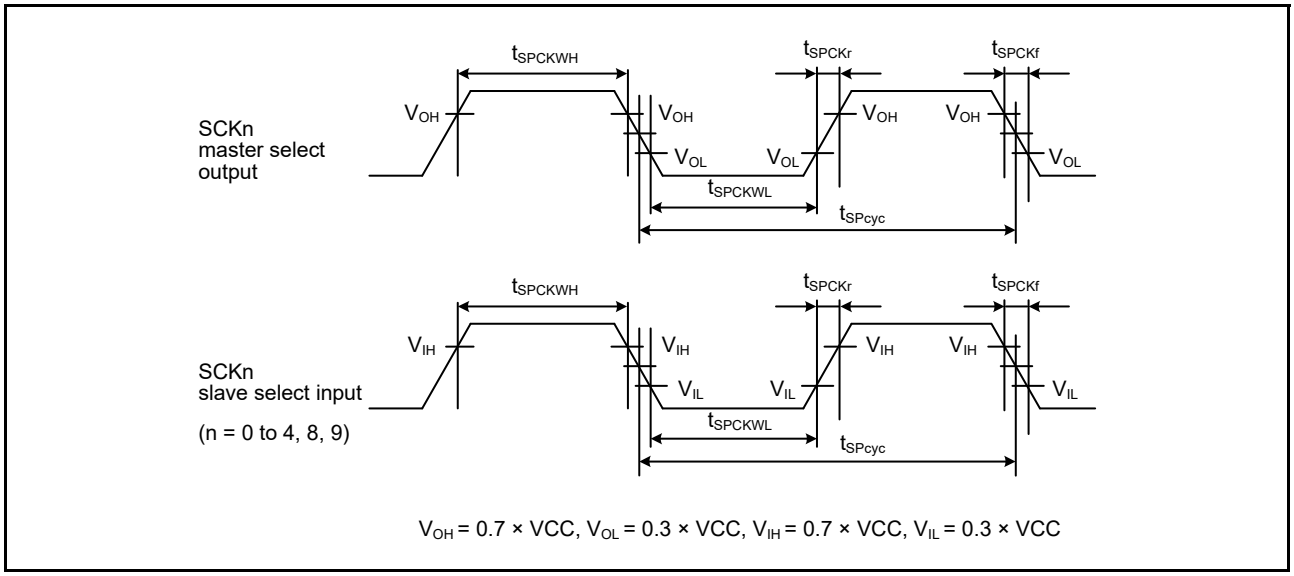


Figure 43.29 SCI simple SPI mode clock timing

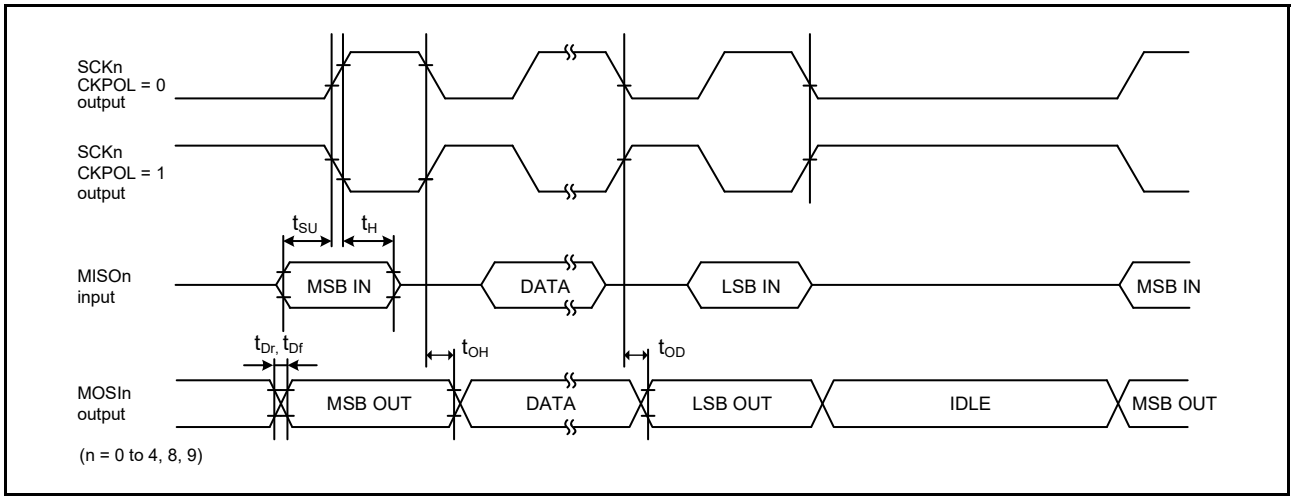


Figure 43.30 SCI simple SPI mode timing for master when CKPH = 1

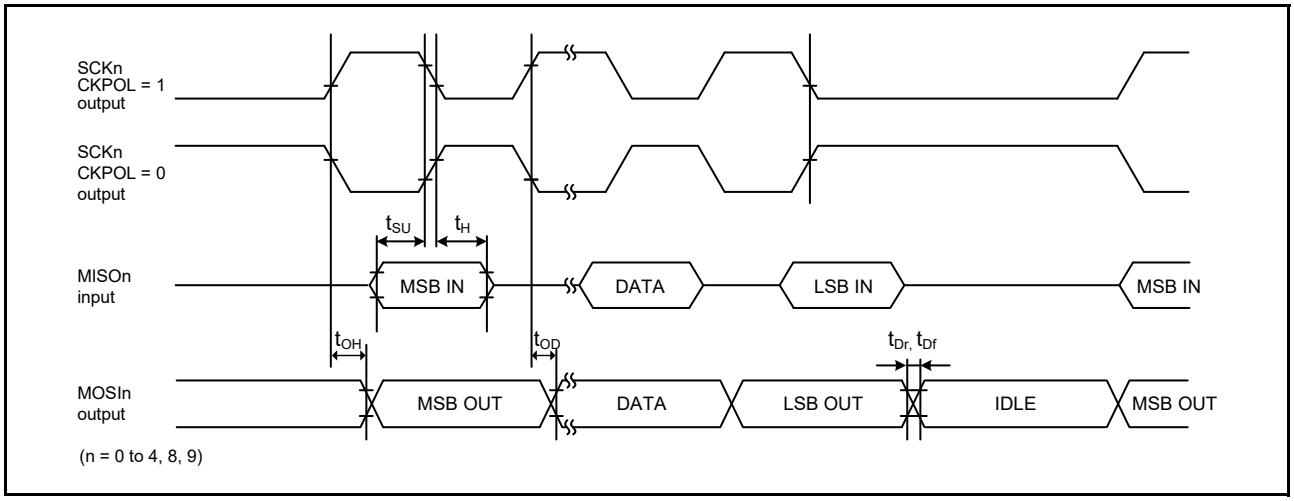


Figure 43.31 SCI simple SPI mode timing for master when CKPH = 0

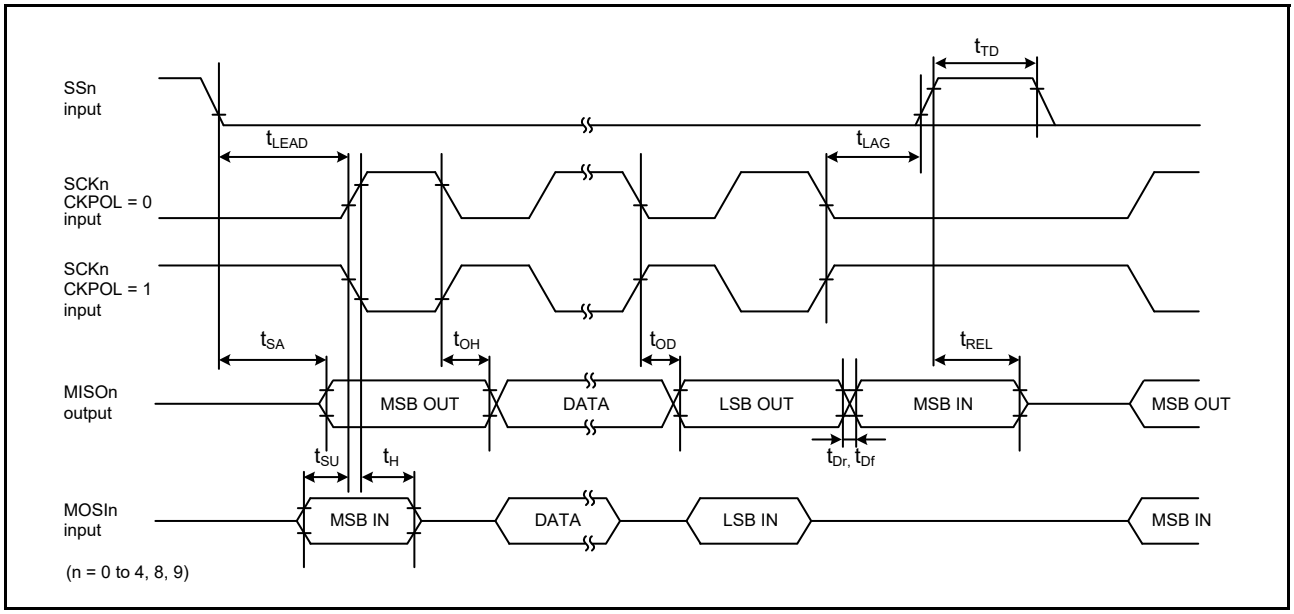


Figure 43.32 SCI simple SPI mode timing for slave when CKPH = 1

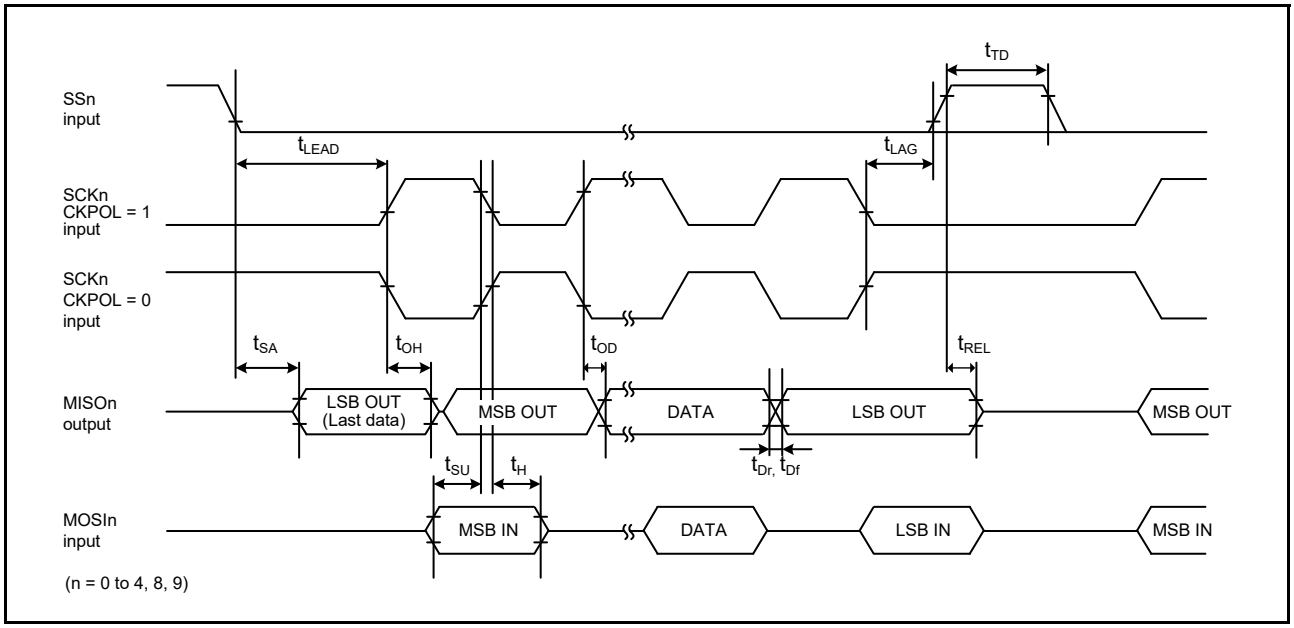


Figure 43.33 SCI simple SPI mode timing for slave when CKPH = 0

Table 43.23 SCI timing (3) (1 of 2)
Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 43.34
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Table 43.23 SCI timing (3) (2 of 2)
Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 43.34
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_{b}*1	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note 1. Cb indicates the total capacity of the bus line.

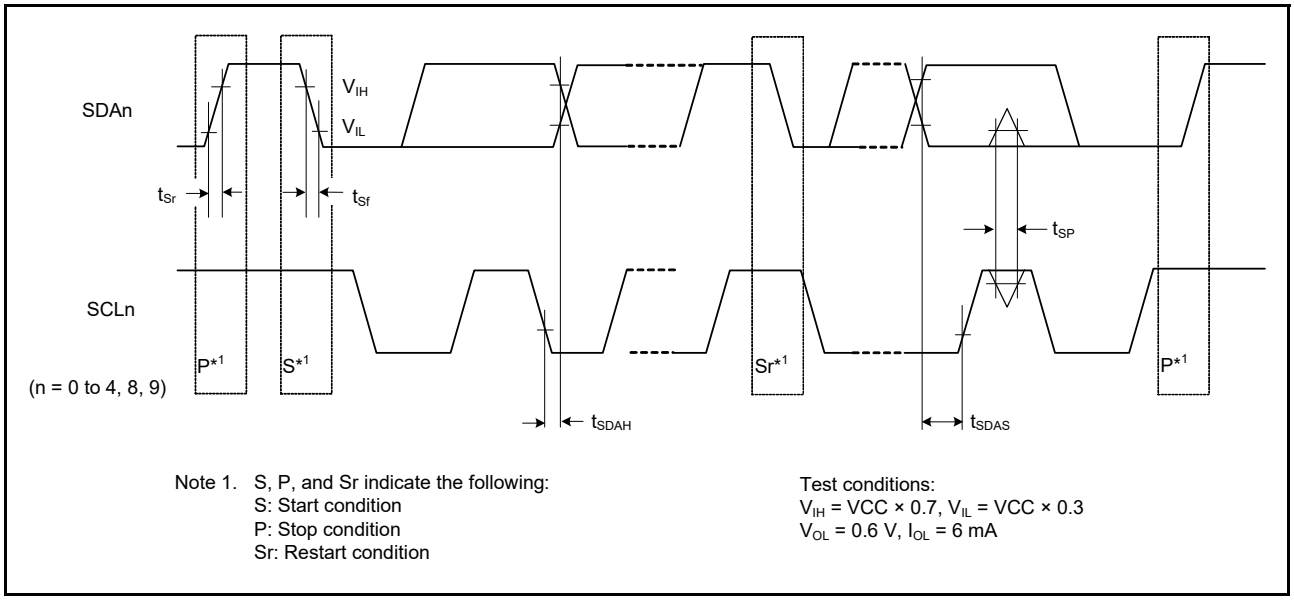


Figure 43.34 SCI simple IIC mode timing

43.3.10 SPI Timing

Table 43.24 SPI timing

Conditions:
For RSPCKA and RSPCKB pins, high drive output is selected with the Port Drive Capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit*1	Test conditions*2
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{Pcyc}	Figure 43.35 C = 30 pF
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave		2 × t_{Pcyc}	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave		2 × t_{Pcyc}	-		
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	-	5	ns	
		Slave		-	1	µs	
	Data input setup time	Master	t_{SU}	4	-	ns	Figure 43.36 to Figure 43.41 C = 30 pF
		Slave		5	-		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	-	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_{H}	t_{Pcyc}	-		
		Slave	t_{H}	20	-		
	SSL setup time	Master	t_{LEAD}	N × t_{SPcyc} - 10*3	N × t_{SPcyc} + 100*3	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	SSL hold time	Master	t_{LAG}	N × t_{SPcyc} - 10 *4	N × t_{SPcyc} + 100*4	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	Data output delay	Master	t_{OD}	-	6.3	ns	
		Slave		-	20		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay	Master	t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave		6 × t_{Pcyc}			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	-	5	ns	
		Input		-	1	µs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	-	5	ns	
		Input		-	1	µs	
	Slave access time		t_{SA}	-	2 x t_{Pcyc} + 28	ns	Figure 43.40 and Figure 43.41 C = 30pF
	Slave output release time		t_{REL}	-	2 x t_{Pcyc} + 28		

Note 1. t_{Pcyc}: PCLKA cycle.

Note 2. Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. N is set to an integer from 1 to 8 by the SPCKD register.
Note 4. N is set to an integer from 1 to 8 by the SSLND register.

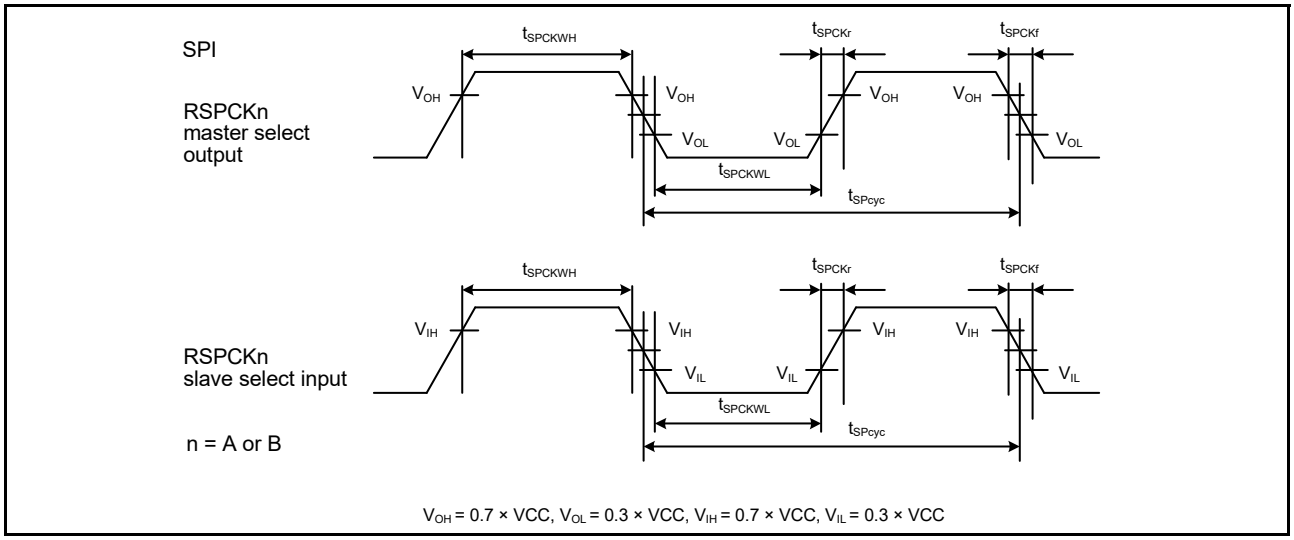


Figure 43.35 SPI clock timing

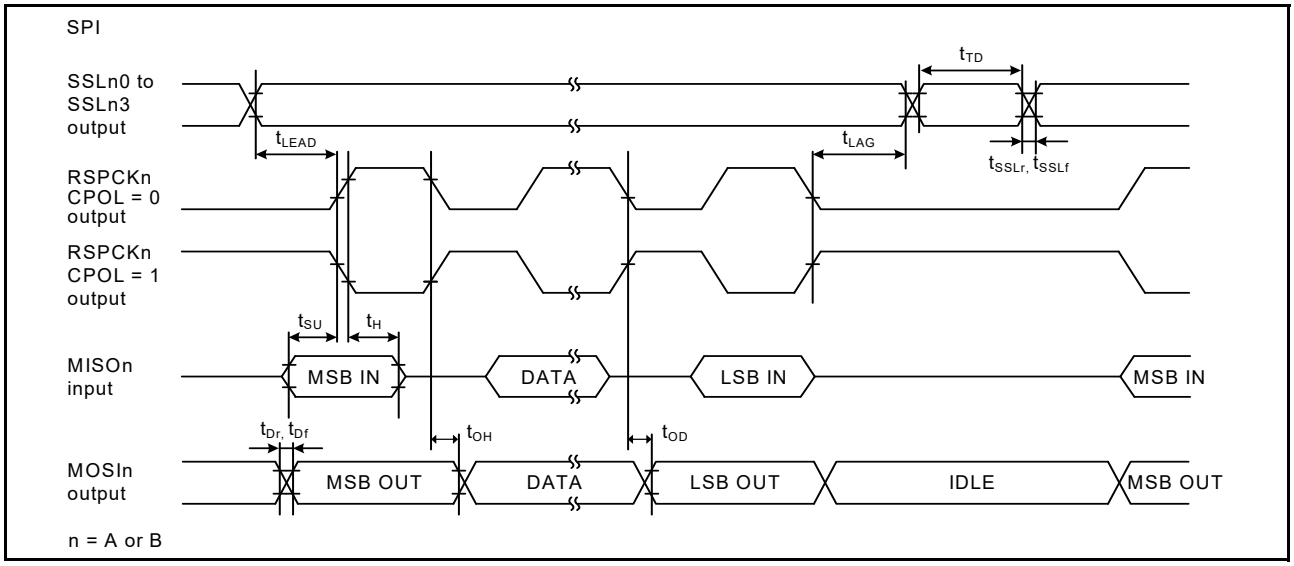


Figure 43.36 SPI timing for master when CPHA = 0

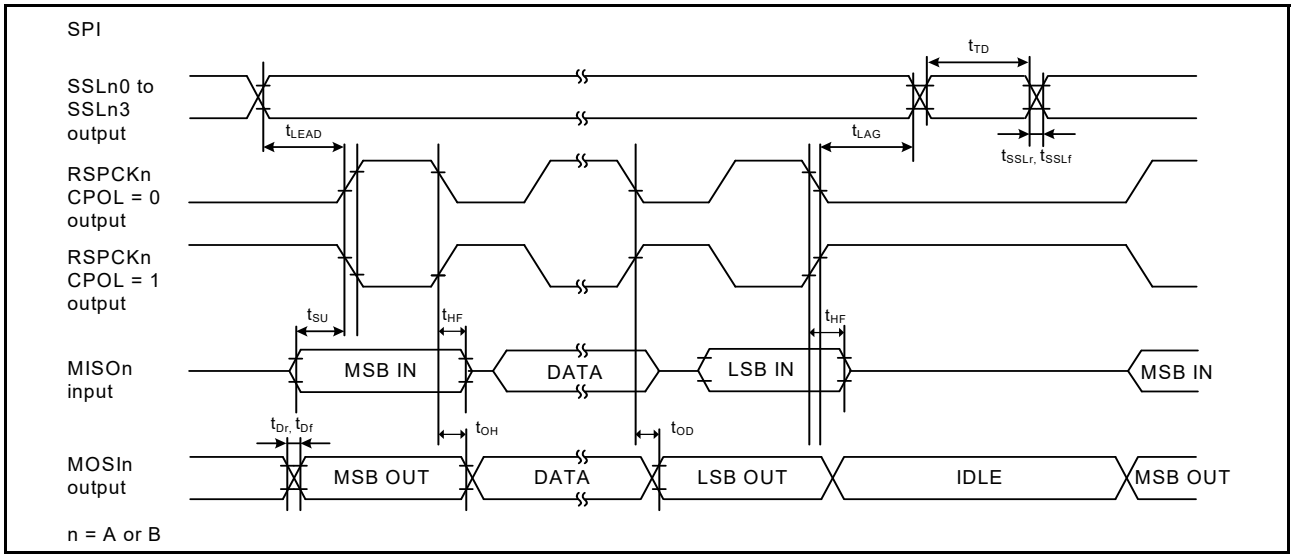


Figure 43.37 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

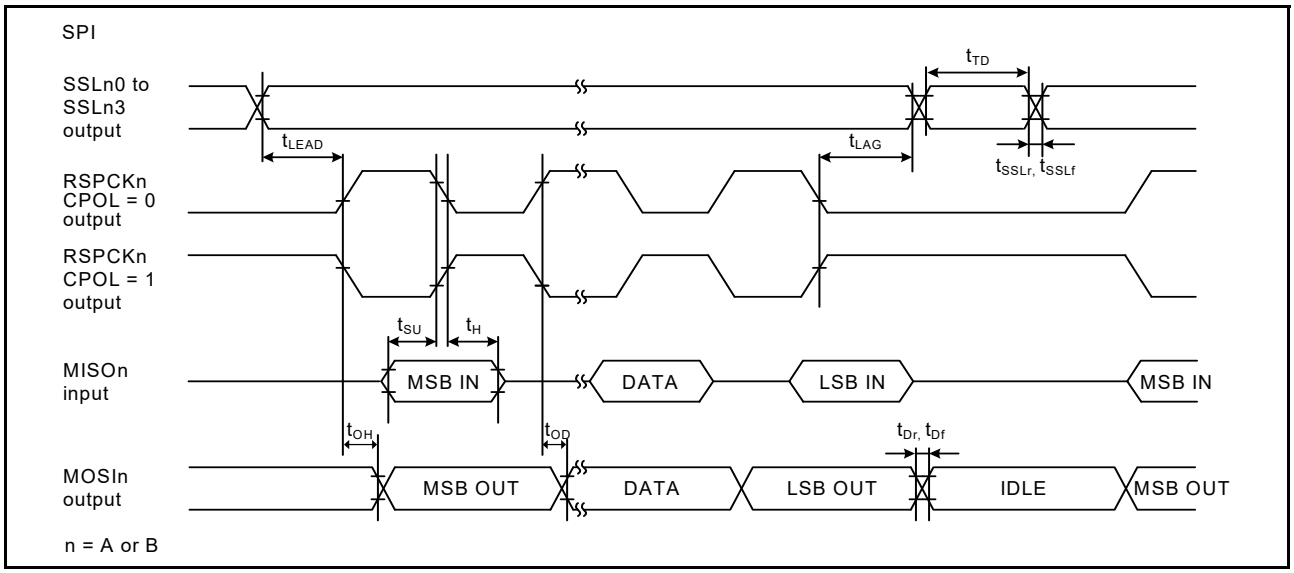


Figure 43.38 SPI timing for master when CPHA = 1

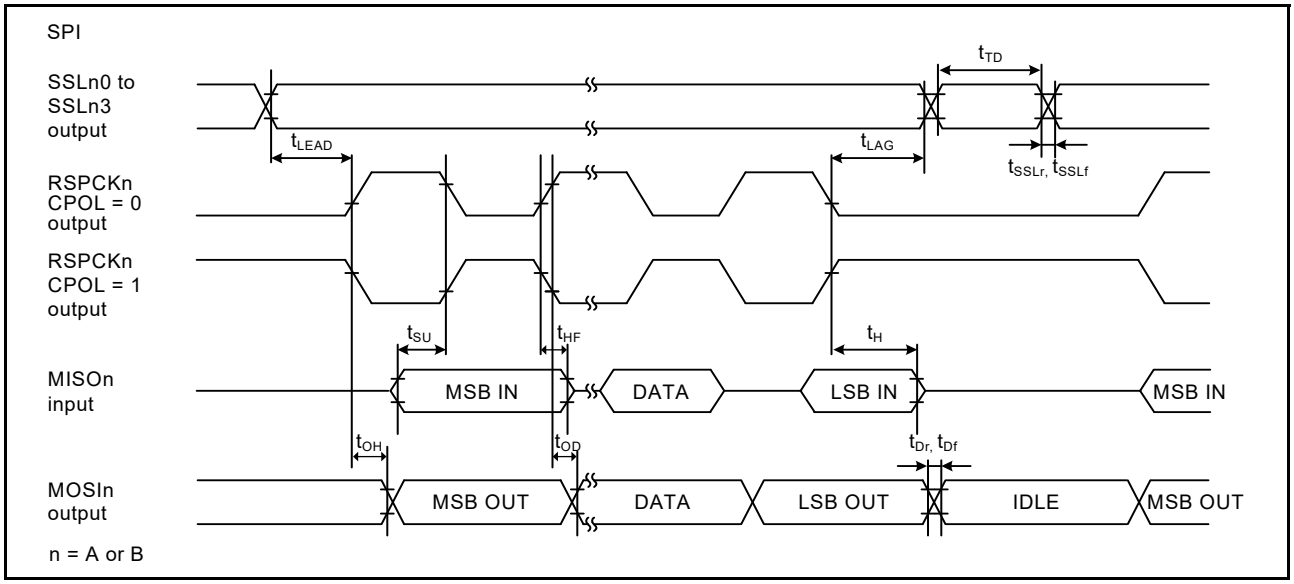


Figure 43.39 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

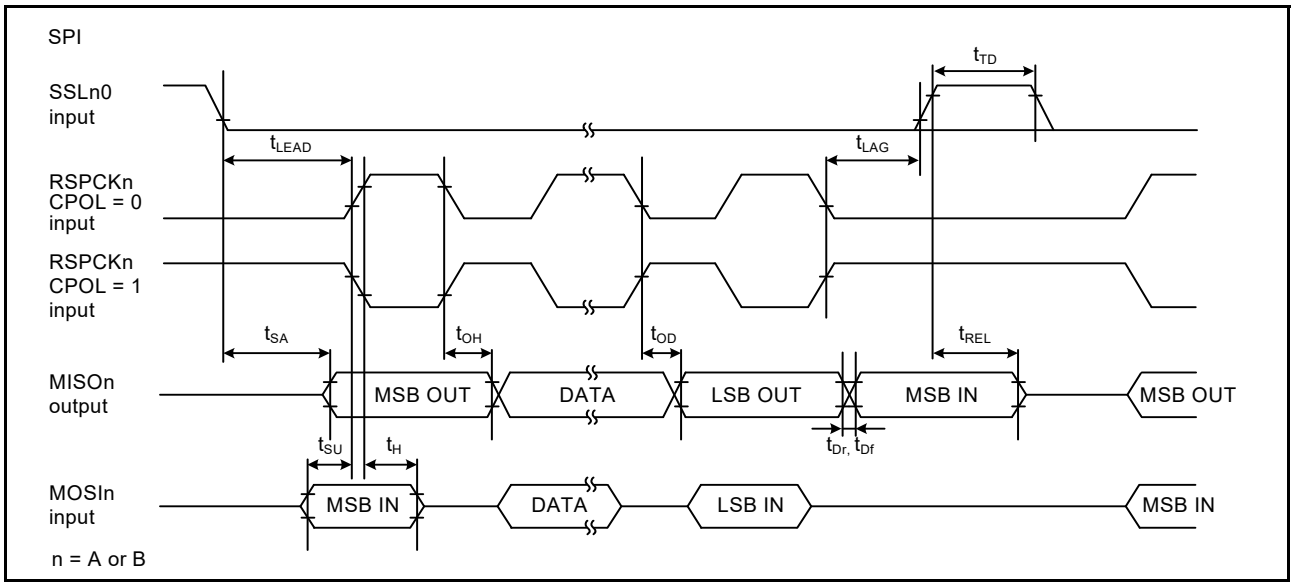


Figure 43.40 SPI timing for slave when CPHA = 0

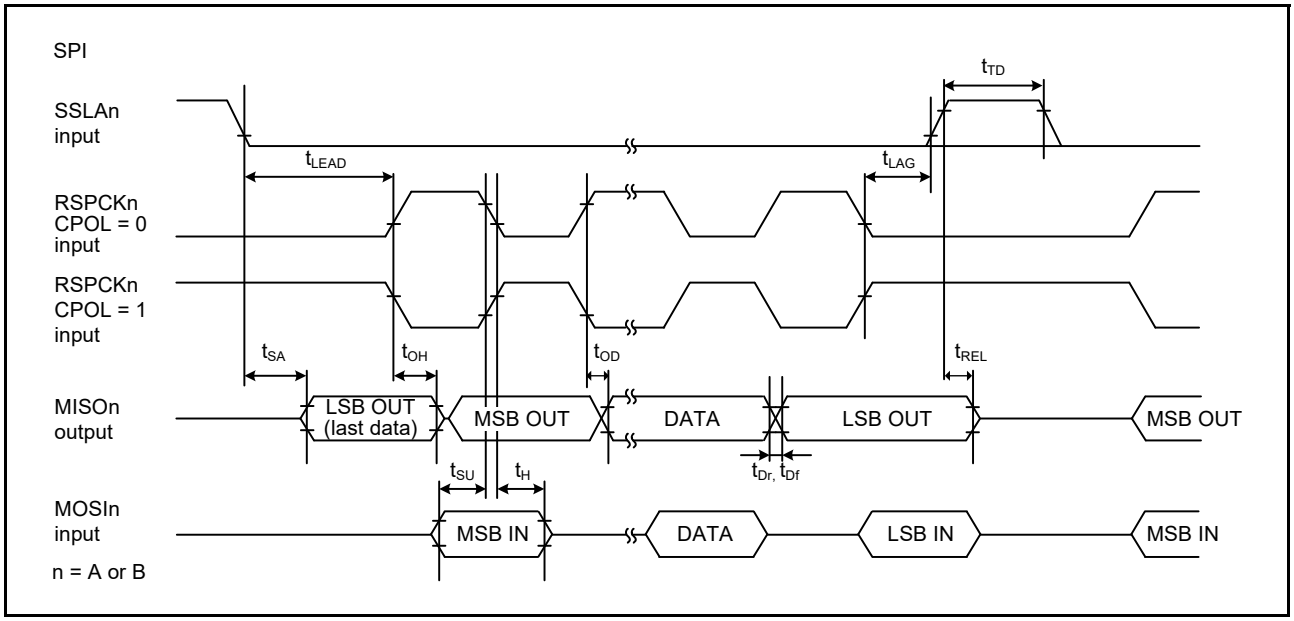


Figure 43.41 SPI timing for slave when CPHA = 1

43.3.11 IIC Timing

Table 43.25 IIC timing (1) (1 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.

(2) The following pins do not require setting: SCL0_A, SDA0_A.

(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 43.42
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Table 43.25 IIC timing (1) (2 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 43.42
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Only supported for SCL0_A, SDA0_A.
Note 3. Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Table 43.26 IIC timing (2)
Setting of the SCL0_A, SDA0_A pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min*1,*2	Max	Unit	Test conditions
IIC (Fast mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 240	-	ns	Figure 43.42
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	120	ns	
	SCL, SDA input fall time	t_{Sf}	-	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 120	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	-	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 120	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	-	ns	
	Restart condition input setup time	t_{STAS}	120	-	ns	
	Stop condition input setup time	t_{STOS}	120	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Cb indicates the total capacity of the bus line.

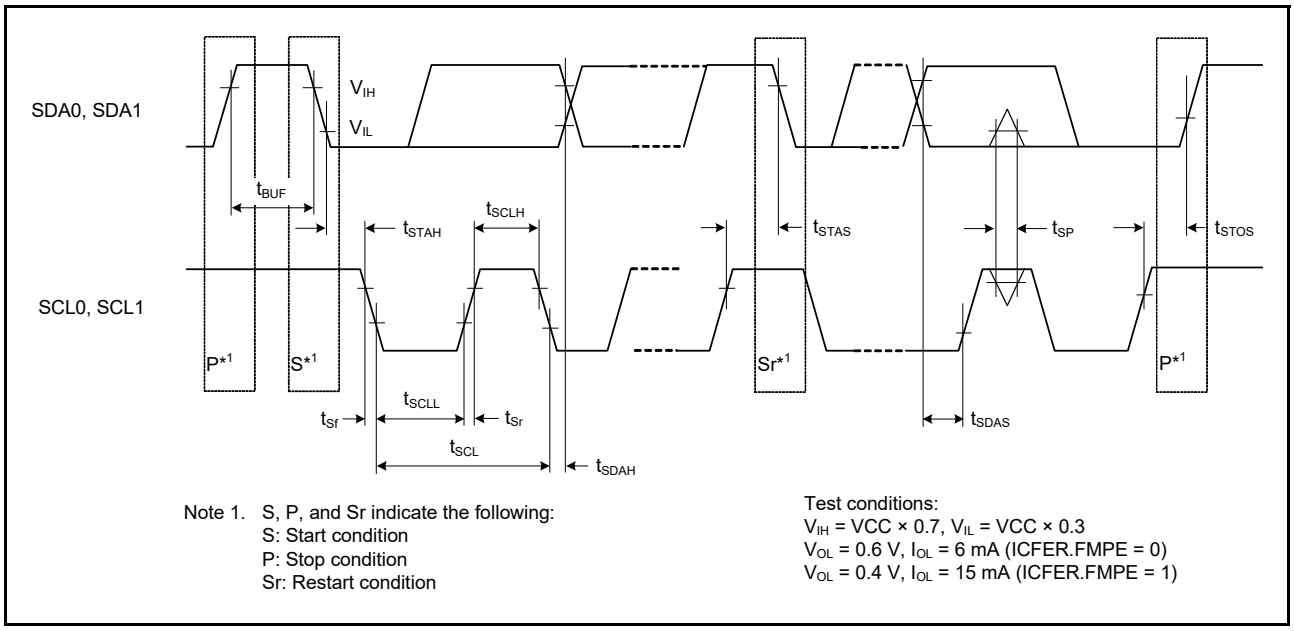


Figure 43.42 I²C bus interface input/output timing

43.4 ADC12 Characteristics

Table 43.27 A/D conversion characteristics for unit 0 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use*3 (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL pseudo-differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	µs	-
	Dynamic range		0.25	-	VREFH0 - 0.25	V	-
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL pseudo-differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN003, AN005, AN006)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL pseudo-differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN007)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.75 (0.533)*2	-	-	µs	Sampling in 32 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL pseudo-differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-

Table 43.27 A/D conversion characteristics for unit 0 (2 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Normal-precision channels (AN016 to AN018, AN020)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL pseudo-differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, the values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.
Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.
Note 2. Values in parentheses indicate the sampling time.
Note 3. When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, see Table 43.29.

Table 43.28 A/D conversion characteristics for unit 1 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use*3 (AN100 to AN102)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN100 to AN102 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL pseudo-differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	µs	-
	Dynamic range		0.25	-	VREFH - 0.25	V	-
Channel-dedicated sample-and-hold circuits not in use (AN100 to AN102)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL pseudo-differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-

Table 43.28 A/D conversion characteristics for unit 1 (2 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
High-precision channels (AN105, AN106)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL pseudo-differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN107)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.75 (0.533)*2	-	-	µs	Sampling in 32 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL pseudo-differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN116, AN117)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL pseudo-differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, the values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.
Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.
Note 2. Values in parentheses indicate the sampling time.
Note 3. When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, see Table 43.29.

Table 43.29 A/D conversion characteristics for simultaneous use of channel-dedicated sample-and-hold circuits in unit 0 and unit 1
Conditions: PCLKC = 30/60 MHz

Parameter		Min	Typ	Max	Test conditions
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±5.0	• PCLKC = 60 MHz • Sampling in 15 states
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±5.0	
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±3.5	• PCLKC = 30 MHz • Sampling in 7 states
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	+4.5/-6.5	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±3.5	
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	+4.5/-6.5	

Note: When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, setting the ADSHMSR.SHMD bit to 1 is recommended.

Table 43.30 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	-
Sampling time	4.15	-	-	µs	-

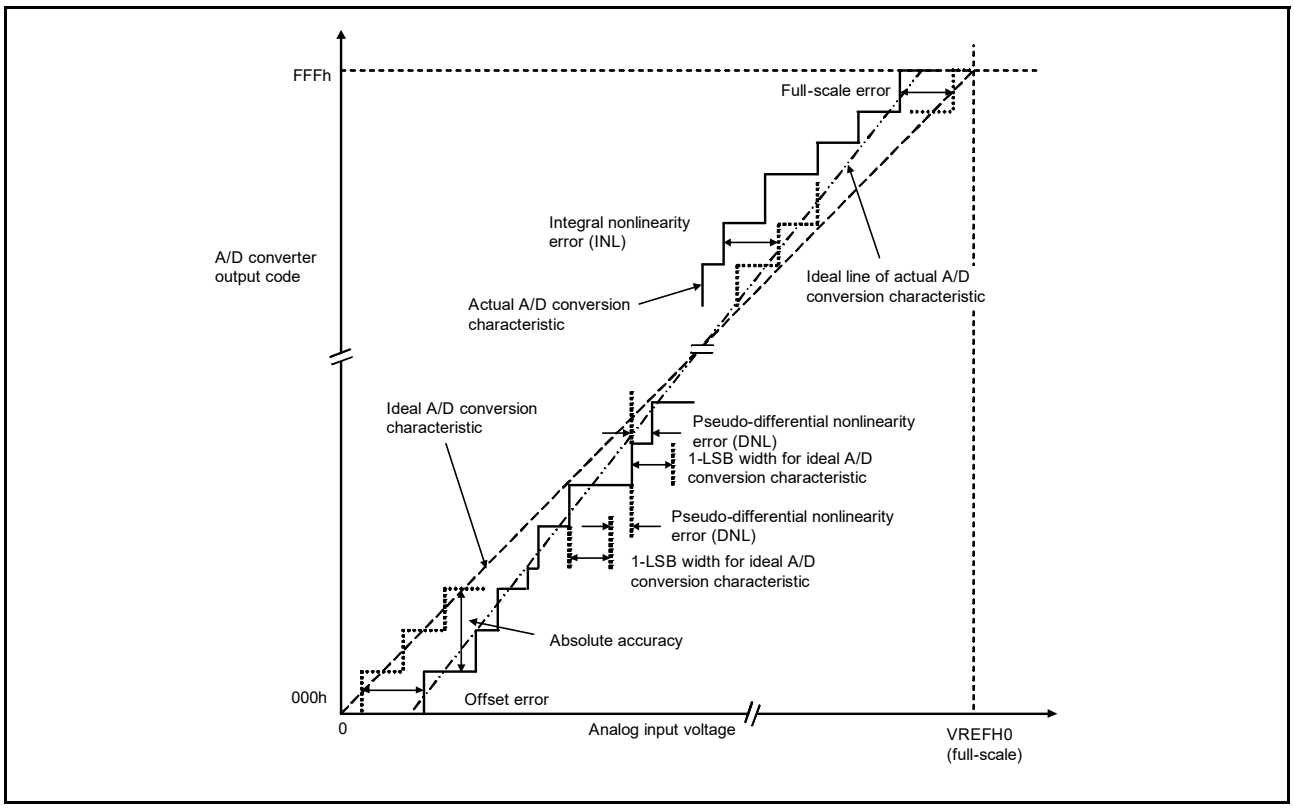


Figure 43.43 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 is 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Pseudo-differential nonlinearity error (DNL)

Pseudo-differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

43.5 DAC12 Characteristics

Table 43.31 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	Bits	-
Without output amplifier					
Absolute accuracy	-	-	±24	LSB	Resistive load 2 MΩ
INL	-	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	-	±1.0	±2.0	LSB	-
Output impedance	-	8.5	-	kΩ	-
Conversion time	-	-	3.0	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	-	VREFH	V	-
With output amplifier					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
Conversion time	-	-	4.0	µs	-
Resistive load	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.2	-	VREFH - 0.2	V	-

43.6 TSN Characteristics

Table 43.32 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.0	-	°C	-
Temperature slope	-	-	4.0	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.24	-	V	-
Temperature sensor start time	t_{START}	-	-	30	µs	-
Sampling time	-	4.15	-	-	µs	-

43.7 OSC Stop Detect Characteristics

Table 43.33 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 43.44

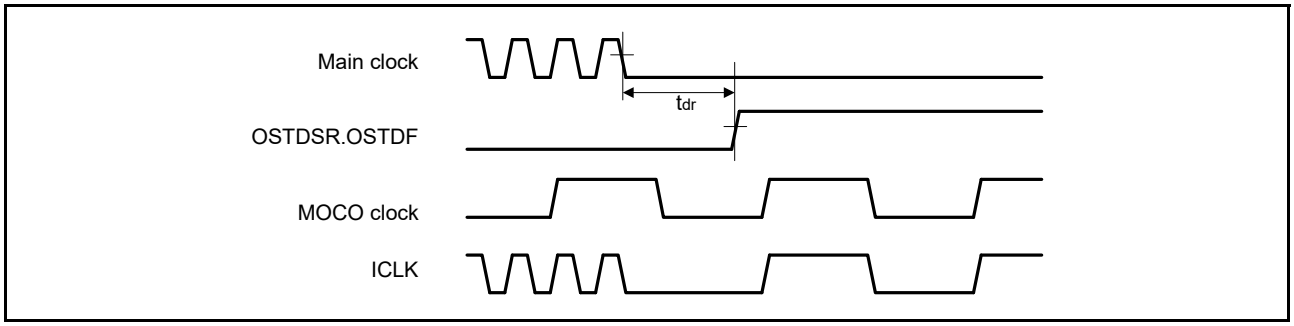


Figure 43.44 Oscillation stop detection timing

43.8 POR and LVD Characteristics

Table 43.34 Power-on reset circuit and voltage detection circuit characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b	V_{POR}	2.5	2.6	2.7	V	Figure 43.45
		DPSBYCR.DEEPCUT[1:0] = 11b		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 43.46
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 43.47
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 43.48
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	-	4.5	-	ms	Figure 43.45
	LVD0 reset time		t_{LVD0}	-	0.51	-		Figure 43.46
	LVD1 reset time		t_{LVD1}	-	0.38	-		Figure 43.47
	LVD2 reset time		t_{LVD2}	-	0.38	-		Figure 43.48
Minimum VCC down time*1			t_{VOFF}	200	-	-	µs	Figure 43.45, Figure 43.46
Response delay			t_{det}	-	-	200	µs	Figure 43.45 to Figure 43.48
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	-	-	10	µs	Figure 43.47, Figure 43.48
Hysteresis width (LVD1 and LVD2)			V_{LVH}	-	70	-	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for POR and LVD.

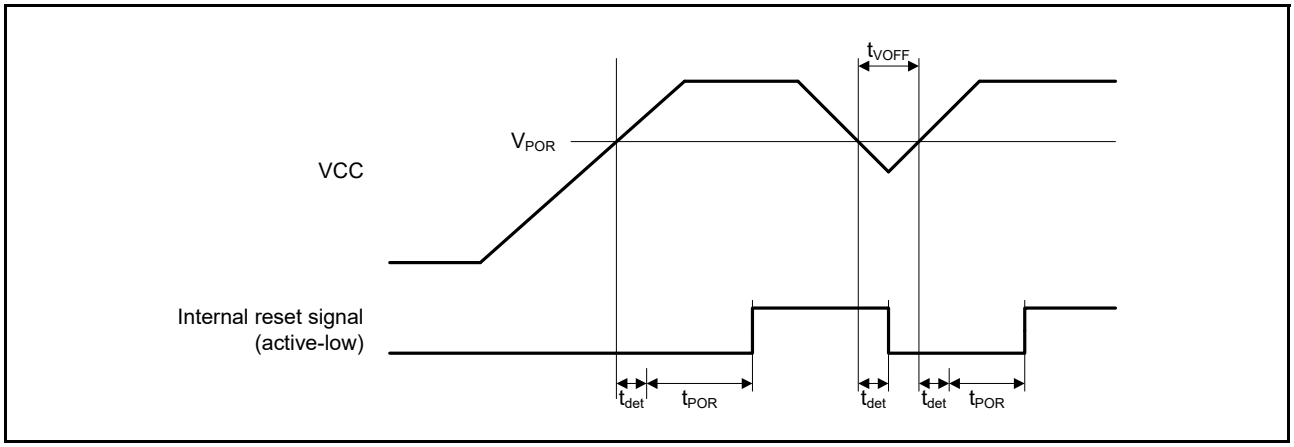


Figure 43.45 Power-on reset timing

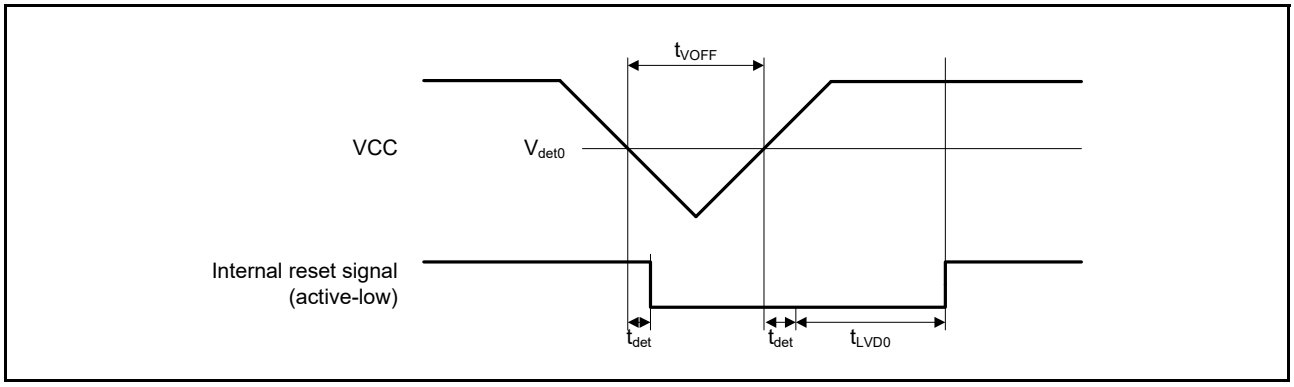


Figure 43.46 Voltage detection circuit timing (V_{det0})

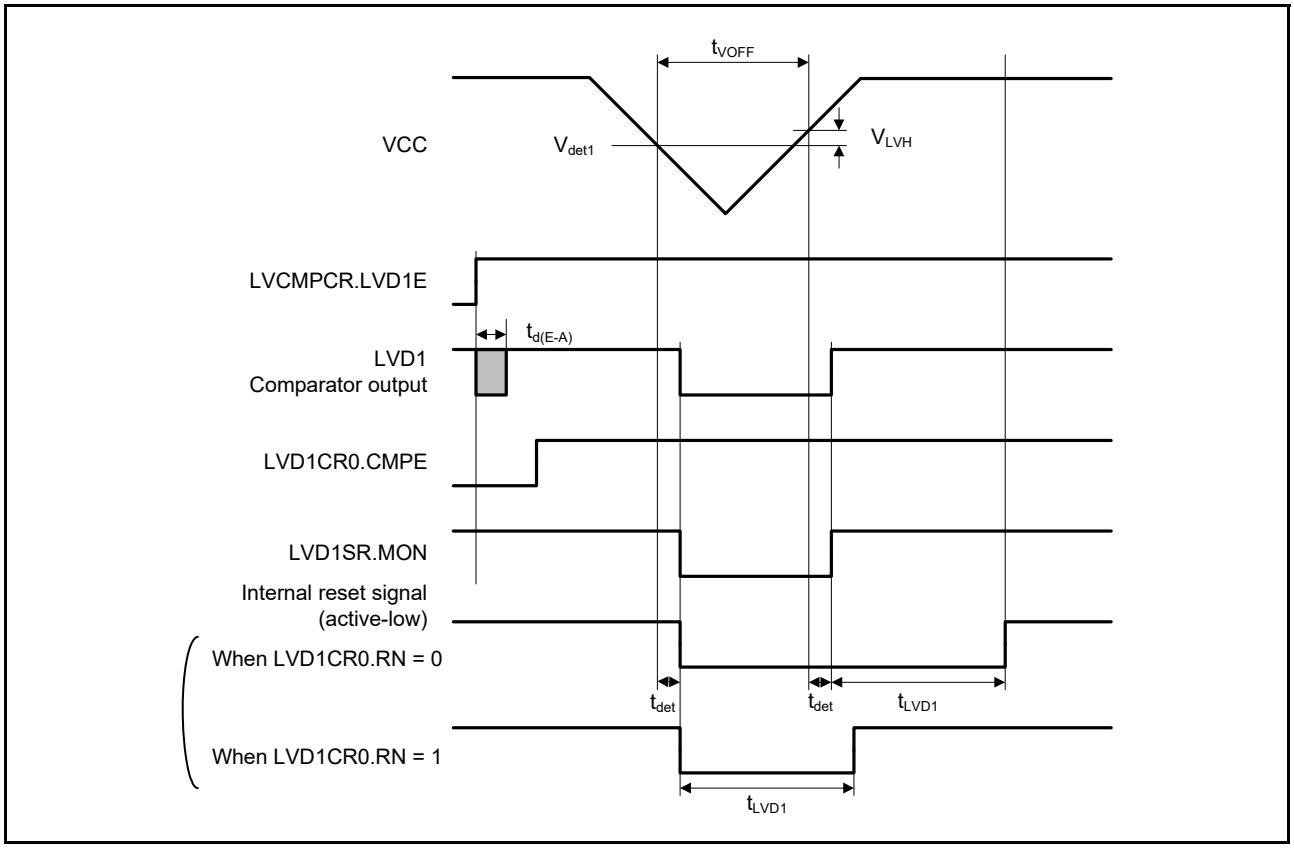


Figure 43.47 Voltage detection circuit timing (V_{det1})

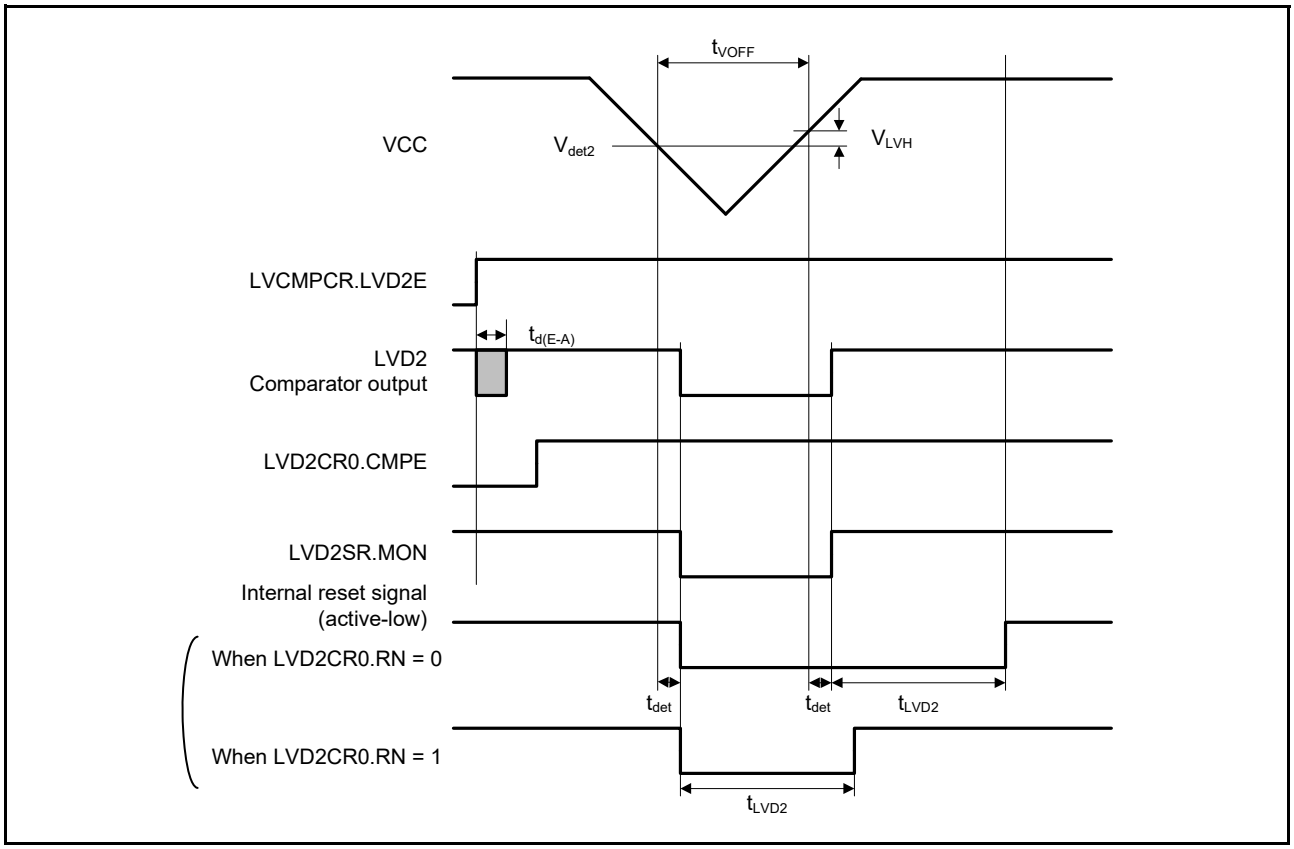


Figure 43.48 Voltage detection circuit timing (V_{det2})

43.9 ACMPHS Characteristics

Table 43.35 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	VREF	0	-	AVCC0	V	-
Input voltage range	VI	0	-	AVCC0	V	-
Output delay*1	Td	-	50	100	ns	VI = VREF ± 100 mV
Internal reference voltage	Vref	1.13	1.18	1.23	V	-

Note 1. This value is the internal propagation delay.

43.10 PGA Characteristics

Table 43.36 PGA characteristics in single mode

Parameter	Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range	PGAVSS	0	-	0	V
	AIN0 (G = 2.000)	0.050 × AVCC0	-	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	-	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	-	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	-	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	-	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	-	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	-	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.040 × AVCC0	-	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	-	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	-	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	-	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	-	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	-	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	-	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	-	0.06 × AVCC0	V
Gain error	Gerr0 (G = 2.000)	-1.0	-	1.0	%
	Gerr1 (G = 2.500)	-1.0	-	1.0	%
	Gerr2 (G = 2.667)	-1.0	-	1.0	%
	Gerr3 (G = 2.857)	-1.0	-	1.0	%
	Gerr4 (G = 3.077)	-1.0	-	1.0	%
	Gerr5 (G = 3.333)	-1.5	-	1.5	%
	Gerr6 (G = 3.636)	-1.5	-	1.5	%
	Gerr7 (G = 4.000)	-1.5	-	1.5	%
	Gerr8 (G = 4.444)	-2.0	-	2.0	%
	Gerr9 (G = 5.000)	-2.0	-	2.0	%
	Gerr10 (G = 5.714)	-2.0	-	2.0	%
	Gerr11 (G = 6.667)	-2.0	-	2.0	%
	Gerr12 (G = 8.000)	-2.0	-	2.0	%
	Gerr13 (G = 10.000)	-2.0	-	2.0	%
	Gerr14 (G = 13.333)	-2.0	-	2.0	%
Offset error	Voff	-8	-	8	mV

Table 43.37 PGA characteristics in pseudo-differential mode

Parameter		Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range		PGAVSS	-0.5	-	0.3	V
Pseudo-differential input voltage range	G = 1.500	AIN-PGAVSS	-0.5	-	0.5	V
	G = 2.333		-0.4	-	0.4	V
	G = 4.000		-0.2	-	0.2	V
	G = 5.667		-0.15	-	0.15	V
Gain error	G = 1.500	Gerr	-1.0	-	1.0	%
	G = 2.333		-1.0	-	1.0	
	G = 4.000		-1.0	-	1.0	
	G = 5.667		-1.0	-	1.0	

43.11 Flash Memory Characteristics

43.11.1 Code Flash Memory Characteristics

Table 43.38 Code flash memory characteristics
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	-	0.75	13.2	-	0.34	6.0	ms	
	8-KB	t_{P8K}	-	49	176	-	22	80	ms	
	32-KB	t_{P32K}	-	194	704	-	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	-	0.91	15.8	-	0.41	7.2	ms	
	8-KB	t_{P8K}	-	60	212	-	27	96	ms	
	32-KB	t_{P32K}	-	234	848	-	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	-	78	216	-	43	120	ms	
	32-KB	t_{E32K}	-	283	864	-	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	-	94	260	-	52	144	ms	
	32-KB	t_{E32K}	-	341	1040	-	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	-	-	10000*1	-	-	Times	
Suspend delay during programming		t_{SPD}	-	-	264	-	-	120	µs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	-	-	216	-	-	120	µs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	-	-	1.7	-	-	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	-	-	1.7	-	-	1.7	ms	
Forced stop command		t_{FD}	-	-	32	-	-	20	µs	
Data hold time*2		t_{DRP}	10*2, *3	-	-	10*2, *3	-	-	Years	
			30*2, *3	-	-	30*2, *3	-	-		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

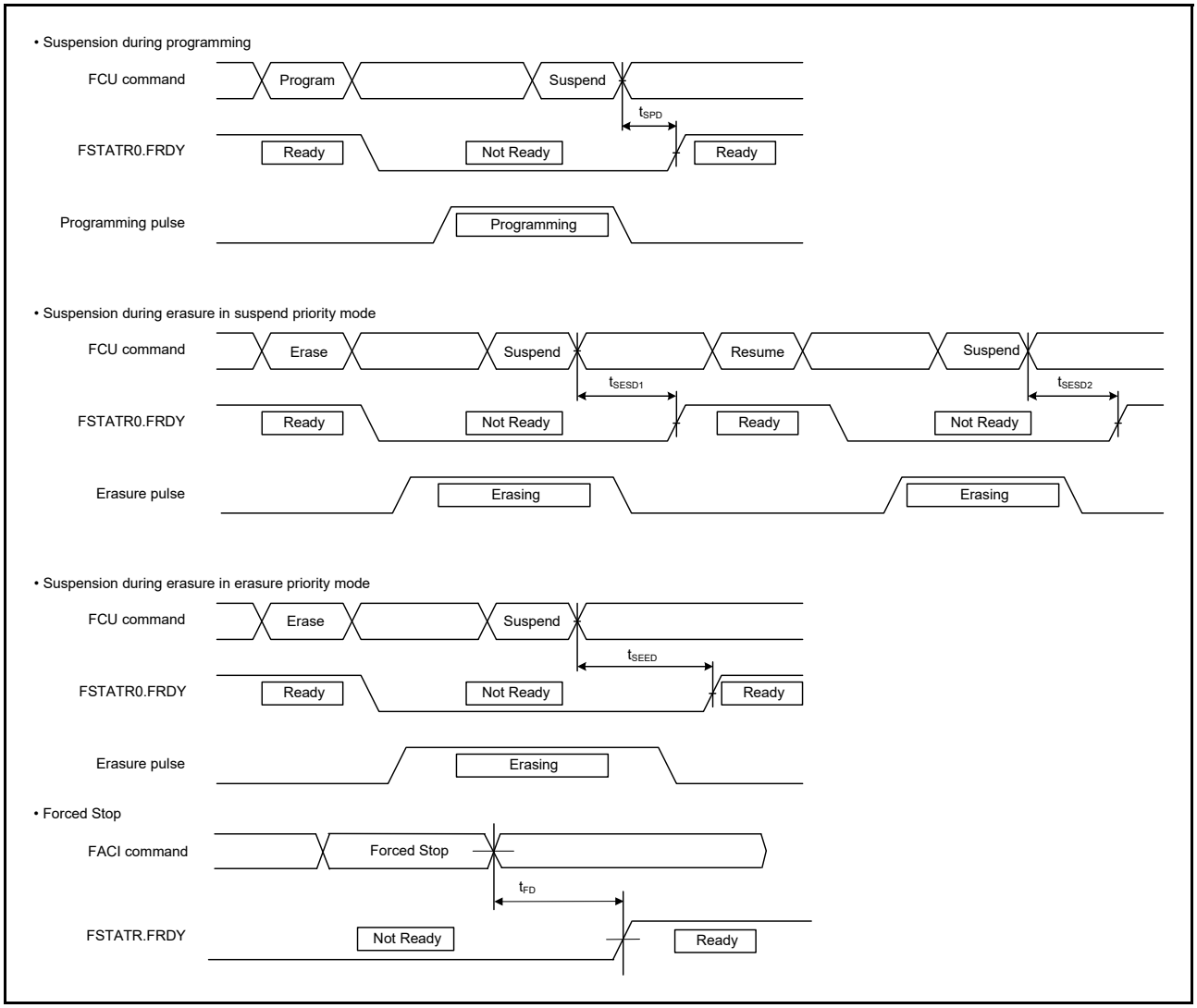


Figure 43.49 Suspension and forced stop timing for flash memory programming and erasure

43.11.2 Data Flash Memory Characteristics

Table 43.39 Data flash memory characteristics
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time	4-byte	t_{DP4}	-	0.36	3.8	-	0.16	1.7	ms	
	8-byte	t_{DP8}	-	0.38	4.0	-	0.17	1.8		
	16-byte	t_{DP16}	-	0.42	4.5	-	0.19	2.0		
Erasure time	64-byte	t_{DE64}	-	3.1	18	-	1.7	10	ms	
	128-byte	t_{DE128}	-	4.7	27	-	2.6	15		
	256-byte	t_{DE256}	-	8.9	50	-	4.9	28		
Blank check time	4-byte	t_{DBC4}	-	-	84	-	-	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	-	-	125000*2	-	-	-	
Suspend delay during programming	4-byte	t_{DSPD}	-	-	264	-	-	120	µs	
	8-byte		-	-	264	-	-	120		
	16-byte		-	-	264	-	-	120		
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	-	-	216	-	-	120	µs	
	128-byte		-	-	216	-	-	120		
	256-byte		-	-	216	-	-	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Forced stop command		t_{FD}	-	-	32	-	-	20	µs	
Data hold time*3		t_{DRP}	10*3,*4	-	-	10*3,*4	-	-	Year	
			30*3,*4	-	-	30*3,*4	-	-		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.

43.12 Boundary Scan

Table 43.40 Boundary scan characteristics (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	-	-	ns	Figure 43.50
TCK clock high pulse width	t_{TCKH}	45	-	-	ns	
TCK clock low pulse width	t_{TCKL}	45	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	

Table 43.40 Boundary scan characteristics (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TMS setup time	t_{TMSS}	20	-	-	ns	Figure 43.51
TMS hold time	t_{TMSH}	20	-	-	ns	
TDI setup time	t_{TDIS}	20	-	-	ns	
TDI hold time	t_{TDIH}	20	-	-	ns	
TDO data delay	t_{TDOD}	-	-	40	ns	
Boundary scan circuit startup time*1	T_{BSSTUP}	t_{RESWP}	-	-	-	Figure 43.52

Note 1. Boundary scan does not function until the power-on reset becomes negative.

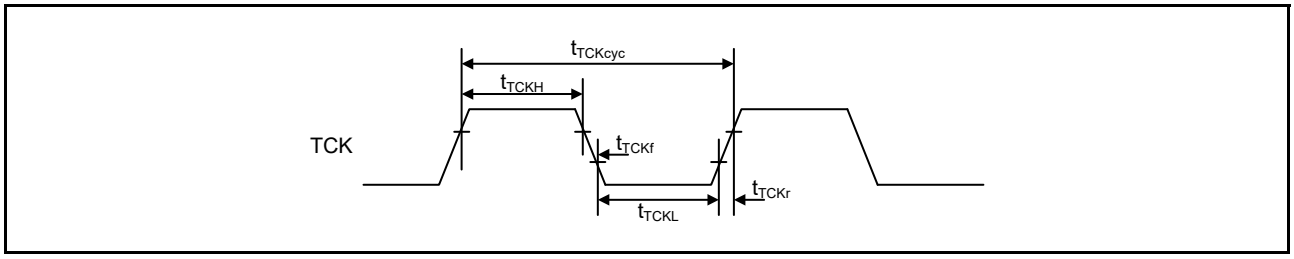


Figure 43.50 Boundary scan TCK timing

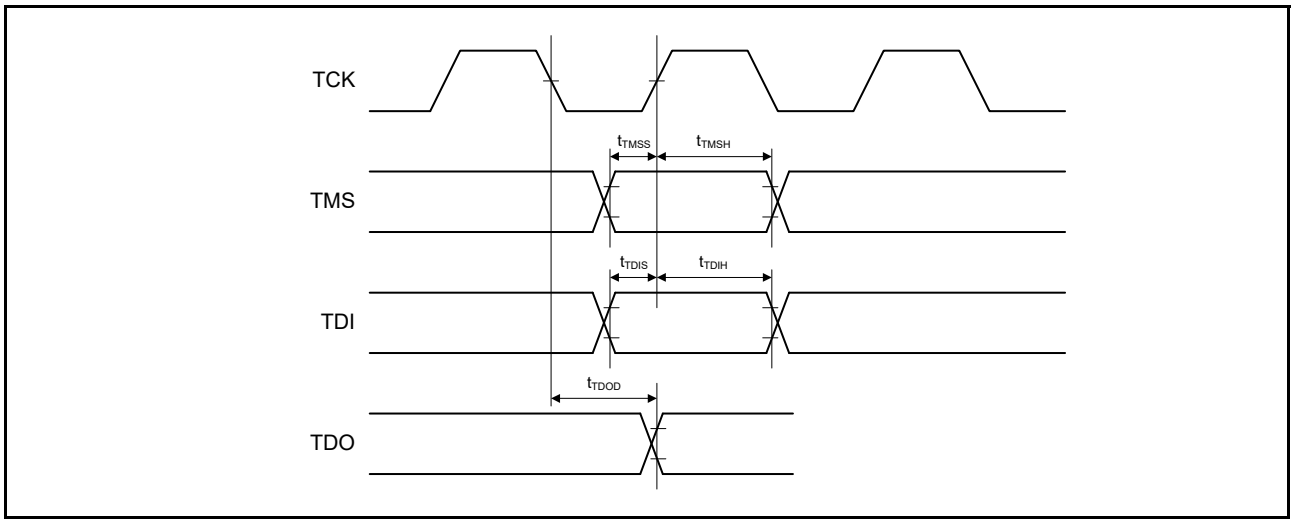


Figure 43.51 Boundary scan input/output timing

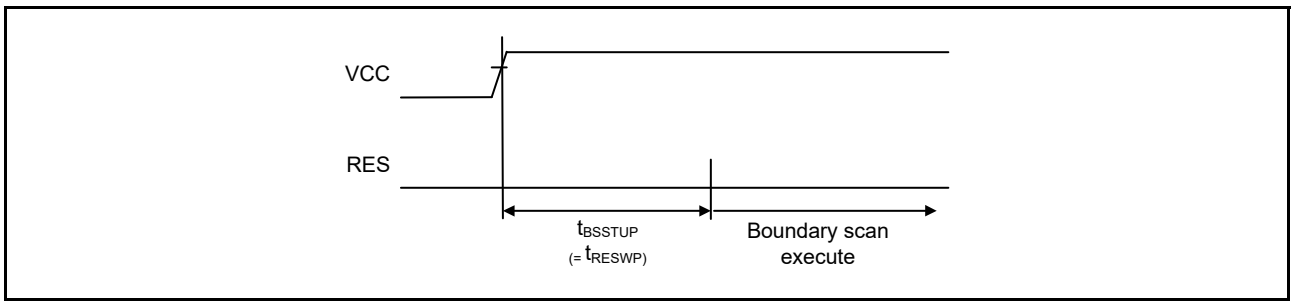


Figure 43.52 Boundary scan circuit startup timing

43.13 Joint Test Action Group (JTAG)

Table 43.41 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	40	-	-	ns	Figure 43.50
TCK clock high pulse width	t_{TCKH}	15	-	-	ns	
TCK clock low pulse width	t_{TCKL}	15	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	8	-	-	ns	Figure 43.51
TMS hold time	t_{TMSH}	8	-	-	ns	
TDI setup time	t_{TDIS}	8	-	-	ns	
TDI hold time	t_{TDIH}	8	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	20	ns	

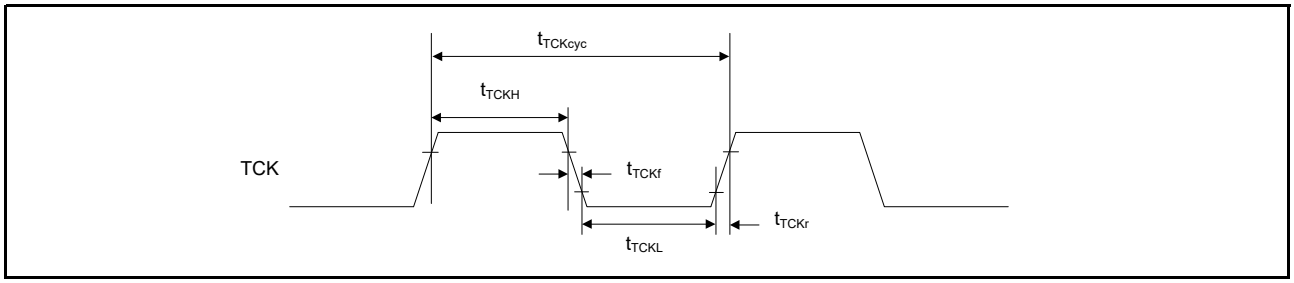


Figure 43.53 JTAG TCK timing

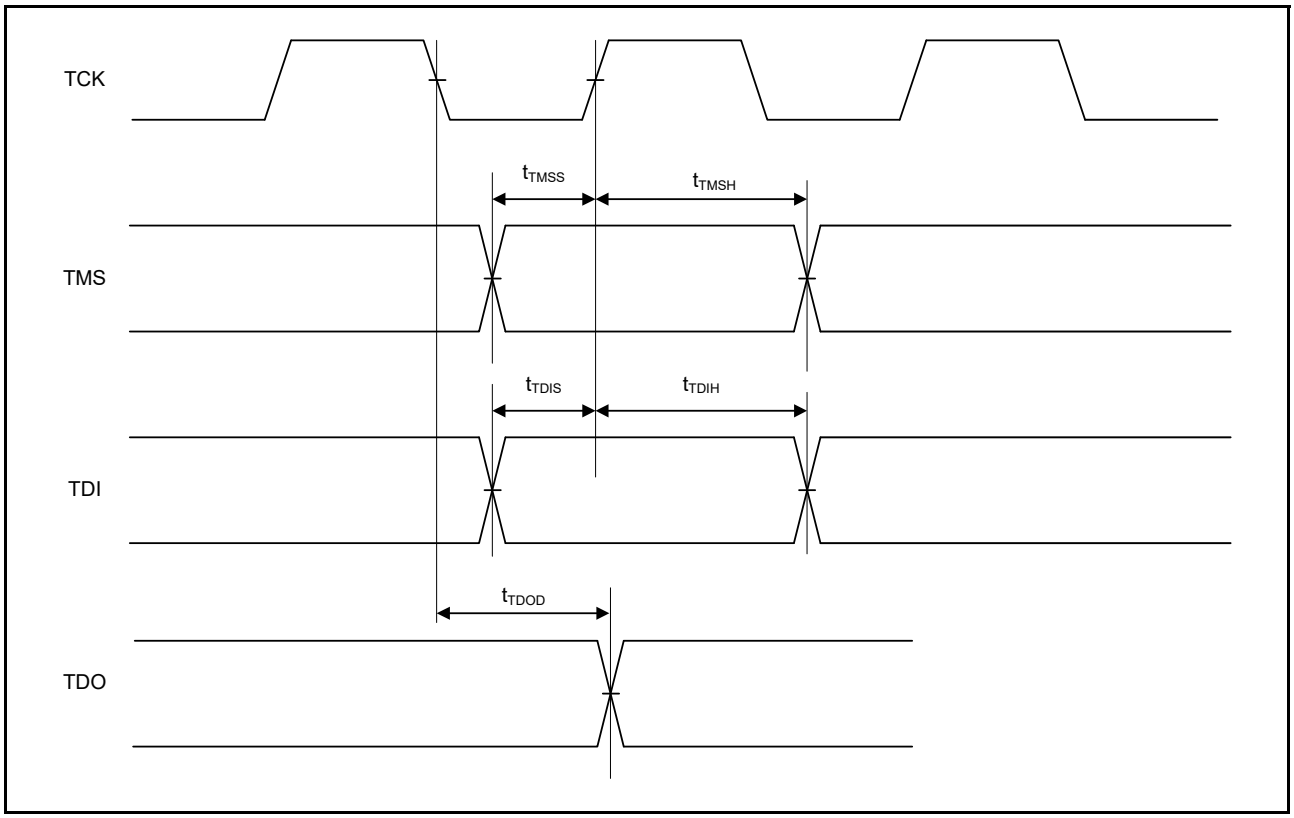


Figure 43.54 JTAG input/output timing

43.14 Serial Wire Debug (SWD)

Table 43.42 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	-	-	ns	Figure 43.55
SWCLK clock high pulse width	t_{SWCKH}	15	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	8	-	-	ns	Figure 43.56
SWDIO hold time	t_{SWDH}	8	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	28	ns	

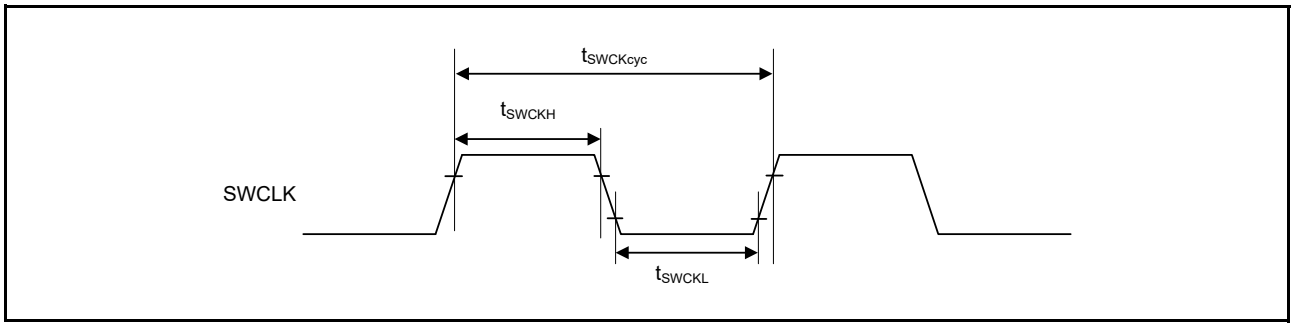


Figure 43.55 SWD SWCLK timing

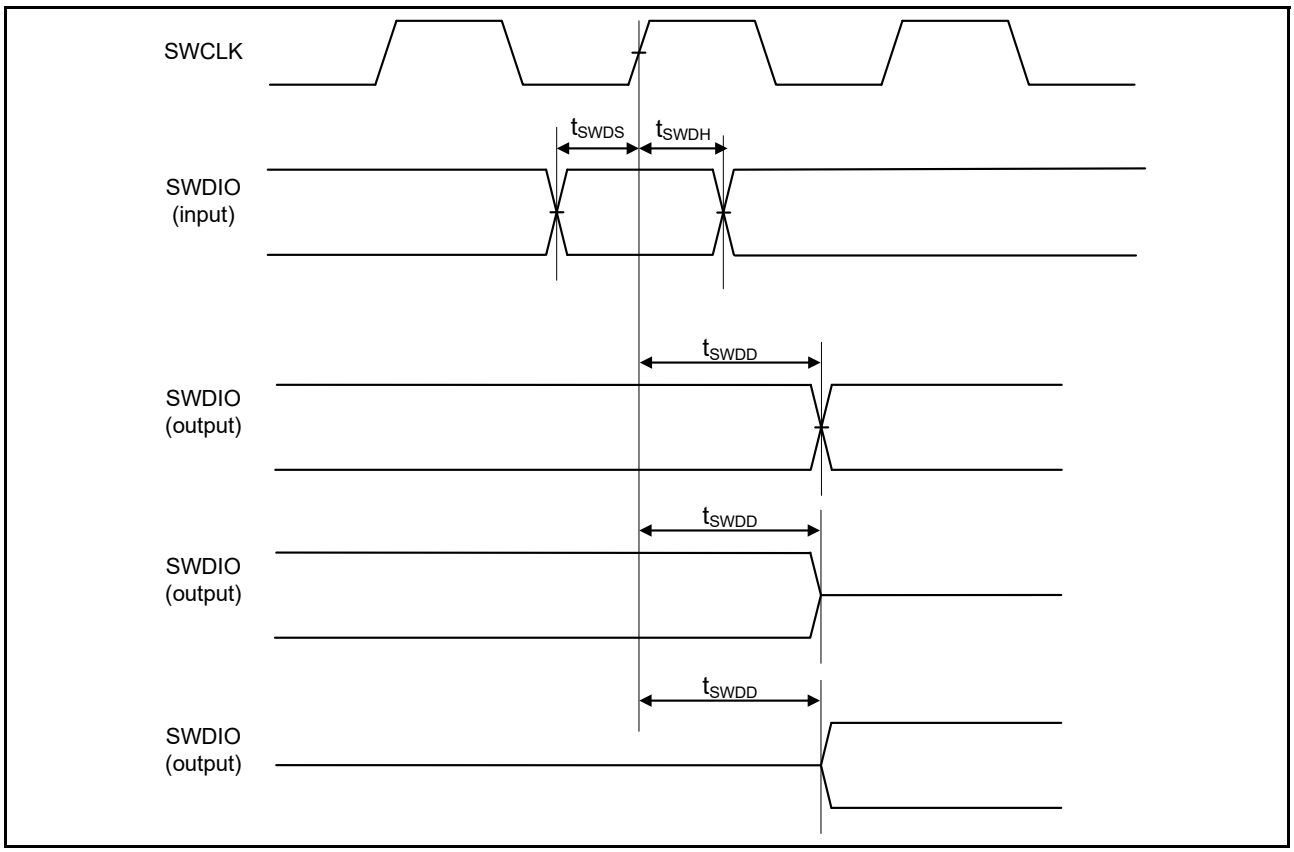


Figure 43.56 SWD input/output timing

43.15 Embedded Trace Macro Interface (ETM)

Table 43.43 ETM
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	$t_{TCLKcyc}$	33.3	-	-	ns	Figure 43.57
TCLK clock high pulse width	t_{TCLKH}	13.6	-	-	ns	
TCLK clock low pulse width	t_{TCLKL}	13.6	-	-	ns	
TCLK clock rise time	t_{TCLKr}	-	-	3	ns	
TCLK clock fall time	t_{TCLKf}	-	-	3	ns	
TDATA[3:0] output setup time	t_{TRDS}	3.5	-	-	ns	Figure 43.58
TDATA[3:0] output hold time	t_{TRDH}	2.5	-	-	ns	

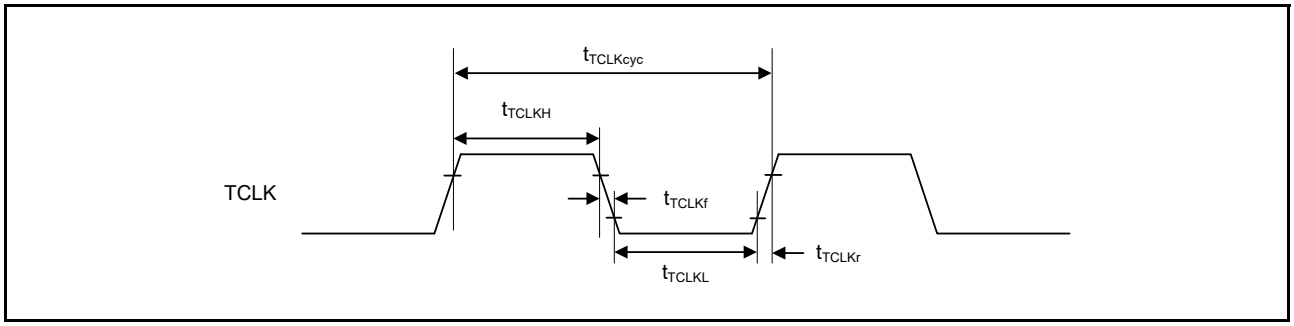


Figure 43.57 ETM TCLK timing

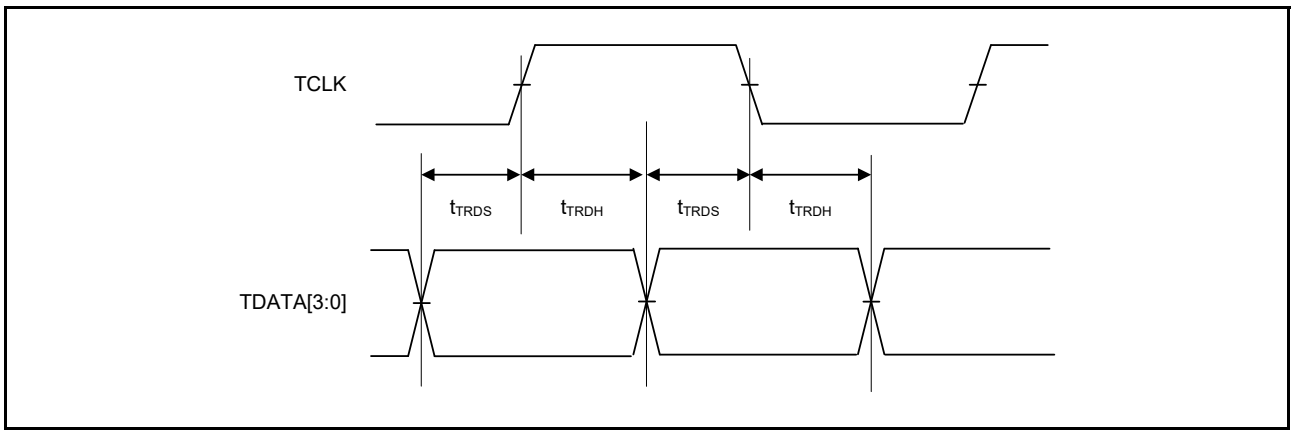


Figure 43.58 ETM output timing

Appendix 1. Port States in Each Processing Mode

Table 1.1 Port states in each processing state (1 of 3)

Port name	Reset	Software Standby mode		Deep SoftwareStandby mode	After Deep Software Standby mode is canceled (return to startup mode)	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P000/IRQ6-DS, P001/IRQ7-DS, P002/IRQ8-DS	Hi-Z	Hi-Z*2		Keep-O*3	Hi-Z	Keep
P003	Hi-Z	Hi-Z		Keep	Hi-Z	Keep
P004/IRQ9-DS, P005/IRQ10-DS, P006/IRQ11-DS	Hi-Z	Hi-Z*2		Keep-O*3	Hi-Z	Keep
P007	Hi-Z	Hi-Z		Keep	Hi-Z	Keep
P008/IRQ12-DS	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
P014/DA0	Hi-Z	[DA0 output (DAOE0 = 1)] D/A output retained [All other (DAOE0 = 0)] Keep-O		Keep	Hi-Z	Keep
P015/IRQ13/DA1	Hi-Z	[DA1 output (DAOE1 = 1)] D/A output retained [All other (DAOE1 = 0)] Keep-O*2		Keep	Hi-Z	Keep
P100/D00[A00/D00]/KR00/ AGTIO0/RXD0/IRQ2	Hi-Z	[D00 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P101/D01[A01/D01]/KR01/IRQ1	Hi-Z	[D01 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P102/D02[A02/D02]/KR02	Hi-Z	[D02 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P103/D03[A03/D03]/KR03	Hi-Z	[D03 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P104/D04[A04/D04]/KR04/IRQ1	Hi-Z	[D04 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P105/D05[A05/D05]/KR05/IRQ0	Hi-Z	[D05 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P106/D06[A06/D06]/KR06	Hi-Z	[D06 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P107/D07[A07/D07]/KR07	Hi-Z	[D07 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P108/TMS	Pull-up	Keep-O		Keep	Pull-up	Keep
P109/TDO/CLKOUT	TDO output	[CLKOUT selected] CLKOUT output [All other] Keep-O		[TDO output] TDO output retained [All other] Keep	[TDO output] TDO output retained [All other] Hi-Z	[TDO output] TDO output retained [All other] Keep
P110/IRQ3/TDI/VCOUT	Pull-up	[ACMPHS selected] VCOUT output [All other] Keep-O*2		Keep	Pull-up	Keep
P111/A05/IRQ4	Hi-Z	[A05 output] Hi-Z [All other] Keep-O*2	[A05 output] Address output retained [All other] Keep-O*2	Keep	Hi-Z	Keep
P112/A04	Hi-Z	[A04 output] Hi-Z [All other] Keep-O	[A04 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep

Table 1.1 Port states in each processing state (2 of 3)

Port name	Reset	Software Standby mode		Deep SoftwareStandby mode	After Deep Software Standby mode is canceled (return to startup mode)	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P113/A03	Hi-Z	[A03 output] Hi-Z [All other] Keep-O	[A03 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P114/A02	Hi-Z	[A02 output] Hi-Z [All other] Keep-O	[A02 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P115/A01	Hi-Z	[A01 output] Hi-Z [All other] Keep-O	[A01 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P200/NMI	Hi-Z	Hi-Z		Keep	Hi-Z	Keep
P201	Pull-up	Keep-O		Keep	Pull-up	Keep
P205/CLKOUT/IRQ1-DS	Hi-Z	[CLKOUT selected] CLKOUT output [All other] Keep-O*2	[CLKOUT selected] CLKOUT output [All other] Keep-O*2	Keep-O*3	Hi-Z	Keep
P206/WAIT/IRQ0-DS	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
P207	Hi-Z	Keep-O	Keep-O	Keep	Hi-Z	Keep
P208/CS4	Hi-Z	[CS4 output] Hi-Z [All other] Keep-O	[CS4 output] H [All other] Keep-O	Keep	Hi-Z	Keep
P209/CS5	Hi-Z	[CS5 output] Hi-Z [All other] Keep-O	[CS5 output] H [All other] Keep-O	Keep	Hi-Z	Keep
P210/CS6	Hi-Z	[CS6 output] Hi-Z [All other] Keep-O	[CS6 output] H [All other] Keep-O	Keep	Hi-Z	Keep
P211/CS7	Hi-Z	[CS7 output] Hi-Z [All other] Keep-O	[CS7 output] H [All other] Keep-O	Keep	Hi-Z	Keep
P212/IRQ3/EXTAL, P213/IRQ2/XTAL	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P214	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P300/TCK	Pull-up	Keep-O		Keep	Pull-up	Keep
P301/A06/AGTIO0/IRQ6	Hi-Z	[A06 output] Hi-Z [All other] Keep-O*2	[A06 output] Address output retained [All other] Keep-O*2	Keep	Hi-Z	Keep
P302/A07/IRQ5	Hi-Z	[A07 output] Hi-Z [All other] Keep-O*2	[A07 output] Address output retained [All other] Keep-O*2	Keep	Hi-Z	Keep
P303/A08	Hi-Z	[A08 output] Hi-Z [All other] Keep-O	[A08 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P304/A09/IRQ9	Hi-Z	[A09 output] Hi-Z [All other] Keep-O*2	[A09 output] Address output retained [All other] Keep-O*2	Keep	Hi-Z	Keep
P305/A10/IRQ8	Hi-Z	[A10 output] Hi-Z [All other] Keep-O*2	[A10 output] Address output retained [All other] Keep-O*2	Keep	Hi-Z	Keep
P306/A11	Hi-Z	[A11 output] Hi-Z [All other] Keep-O	[A11 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P307/A12	Hi-Z	[A12 output] Hi-Z [All other] Keep-O	[A12 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P400/AGTIO1/SCL0_A/IRQ0	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep

Table 1.1 Port states in each processing state (3 of 3)

Port name	Reset	Software Standby mode		Deep SoftwareStandby mode	After Deep Software Standby mode is canceled (return to startup mode)	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P401/SDA0_A/IRQ5-DS, P402/IRQ4-DS/AGTIO0/ AGTIO1, P403/AGTIO0/AGTIO1, P404	Hi-Z	Keep-O		Keep-O*3	Hi-Z	Keep
P405, P406	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P407/AGTIO0/SDA0_B	Hi-Z	Keep-O		Keep-O*3	Hi-Z	Keep
P408/SCL0_B/IRQ7, P409/IRQ6, P410/RXD0/IRQ5, P411/IRQ4	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P412, P413	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P414/IRQ9, P415/IRQ8	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P500	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P501/IRQ11, P502/IRQ12	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P503	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P504/ALE	Hi-Z	[ALE output] Hi-Z [All other] Keep-O	[ALE output] L [All other] Keep-O	Keep	Hi-Z	Keep
P508	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P600/RD/CLKOUT	Hi-Z	[RD output] Hi-Z [CLKOUT selected] CLKOUT output [All other] Keep-O	[RD output] H [CLKOUT selected] CLKOUT output [All other] Keep-O	Keep	Hi-Z	Keep
P601/WR0	Hi-Z	[WR0 output] Hi-Z [All other] Keep-O	[WR0 output] H [All other] Keep-O	Keep	Hi-Z	Keep
P602	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P608/A00	Hi-Z	[A00 output] Hi-Z [All other] Keep-O	[A00 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P708/IRQ11	Hi-Z	Keep-O		Keep	Hi-Z	Keep

H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.

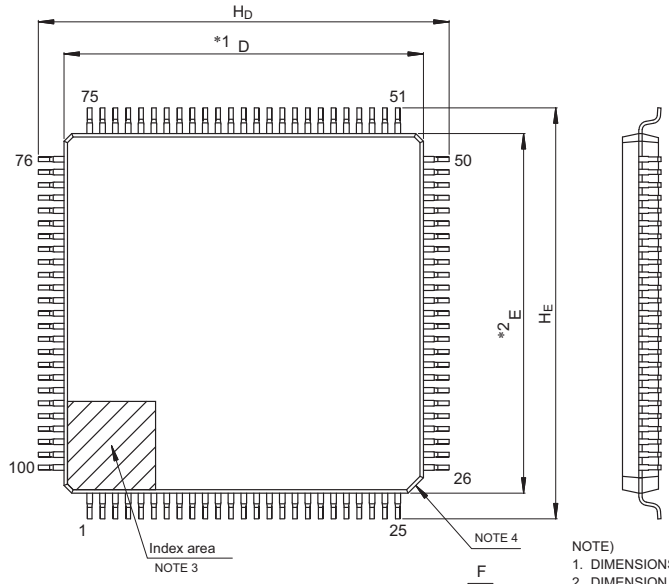
Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is set to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.
Note 4. Input is enabled while the pin is used as an input.

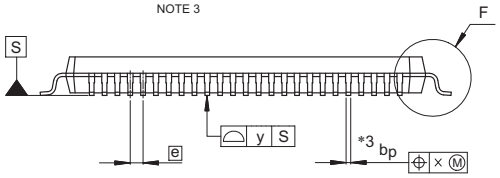
Appendix 2.Package Dimensions

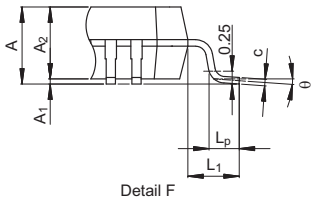
Information on the latest version of the package dimensions or mountings is shown in "Packages" on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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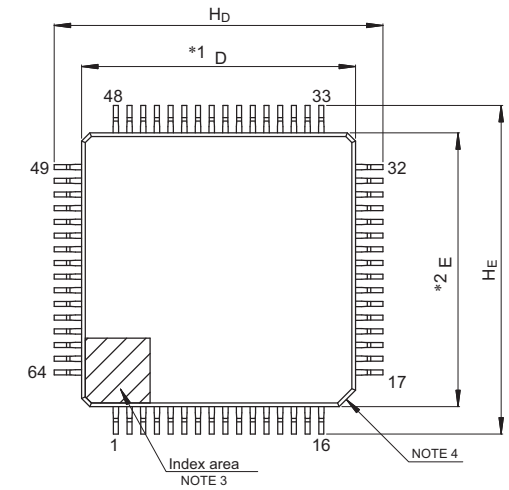
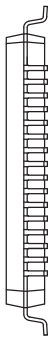
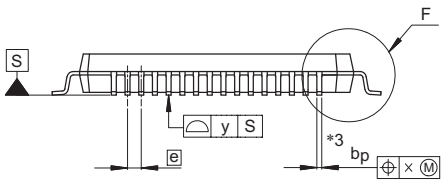
Figure 2.1 100-pin LQFP

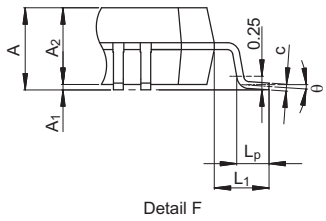
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm









NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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Figure 2.2 64-pin LQFP

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
MMPU	Bus Master MPU	0x40000000
SMPU	Bus Slave MPU	0x40000C00
SPMON	CPU Stack Pointer Monitor	0x40000D00
MMF	Memory Mirror Function	0x40001000
SRAM	SRAM Control	0x40002000
BUS	BUS Control	0x40003000
DMAC0	Direct Memory Access Controller 0	0x40005000
DMAC1	Direct Memory Access Controller 1	0x40005040
DMAC2	Direct Memory Access Controller 2	0x40005080
DMAC3	Direct Memory Access Controller 3	0x400050C0
DMAC4	Direct Memory Access Controller 4	0x40005100
DMAC5	Direct Memory Access Controller 5	0x40005140
DMAC6	Direct Memory Access Controller 6	0x40005180
DMAC7	Direct Memory Access Controller 7	0x400051C0
DMA	DMAC Module Activation	0x40005200
DTC	Data Transfer Controller	0x40005400
ICU	Interrupt Controller	0x40006000
DBG	Debug Function	0x4001B000
FCACHE	Flash Cache	0x4001C000
SYSTEM	System Control	0x4001E000
PORT0	Port 0 Control Registers	0x40040000
PORT1	Port 1 Control Registers	0x40040020
PORT2	Port 2 Control Registers	0x40040040
PORT3	Port 3 Control Registers	0x40040060
PORT4	Port 4 Control Registers	0x40040080
PORT5	Port 5 Control Registers	0x400400A0
PORT6	Port 6 Control Registers	0x400400C0
PORT7	Port 7 Control Registers	0x400400E0
PFS	Pmn Pin Function Control Register	0x40040800
PMISC	Miscellaneous Port Control Register	0x40040D00
ELC	Event Link Controller	0x40041000
POEG	Port Output Enable Module for GPT	0x40042000
INIT	Register to be initialized after reset release	0x40044000
WDT	Watchdog Timer	0x40044200
IWDT	Independent Watchdog Timer	0x40044400
CAC	Clock Frequency Accuracy Measurement Circuit	0x40044600
MSTP	Module Stop Control B, C, D	0x40047000
CAN0	CAN0 Module	0x40050000

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
IIC0	Inter-Integrated Circuit 0	0x40053000
IIC1	Inter-Integrated Circuit 1	0x40053100
DOC	Data Operation Circuit	0x40054100
ADC120	12-bit A/D Converter 0	0x4005C000
ADC121	12-bit A/D Converter 1	0x4005C200
TSN	Temperature Sensor	0x4005D000
DAC12	12-bit D/A Converter	0x4005E000
SCI0	Serial Communication Interface 0	0x40070000
SCI1	Serial Communication Interface 1	0x40070020
SCI2	Serial Communication Interface 2	0x40070040
SCI3	Serial Communication Interface 3	0x40070060
SCI4	Serial Communication Interface 4	0x40070080
SCI8	Serial Communication Interface 8	0x40070100
SCI9	Serial Communication Interface 9	0x40070120
IRDA	Infrared Data Association	0x40070F00
SPI0	Serial Peripheral Interface 0	0x40072000
SPI1	Serial Peripheral Interface 1	0x40072100
CRC	CRC Calculator	0x40074000
GPT32EH0	General PWM Timer 0 (32-bit Enhanced High Resolution)	0x40078000
GPT32EH1	General PWM Timer 1 (32-bit Enhanced High Resolution)	0x40078100
GPT32EH2	General PWM Timer 2 (32-bit Enhanced High Resolution)	0x40078200
GPT32EH3	General PWM Timer 3 (32-bit Enhanced High Resolution)	0x40078300
GPT32E4	General PWM Timer 4 (32-bit Enhanced)	0x40078400
GPT32E5	General PWM Timer 5 (32-bit Enhanced)	0x40078500
GPT32E6	General PWM Timer 6 (32-bit Enhanced)	0x40078600
GPT32E7	General PWM Timer 7 (32-bit Enhanced)	0x40078700
GPT328	General PWM Timer 8	0x40078800
GPT329	General PWM Timer 9	0x40078900
GPT3210	General PWM Timer 10	0x40078A00
GPT3211	General PWM Timer 11	0x40078B00
GPT3212	General PWM Timer 12	0x40078C00
GPT_OPS	Output Phase Switching Controller	0x40078FF0
GPT_ODC	PWM Delay Generation Circuit	0x4007B000
KINT	Key Interrupt Function	0x40080000
AGT0	Low Power Asynchronous General-purpose Timer 0	0x40084000
AGT1	Low Power Asynchronous General-purpose Timer 1	0x40084100
ACMPHS0	High-Speed Analog Comparator 0	0x40085000
ACMPHS1	High-Speed Analog Comparator 1	0x40085100
ACMPHS2	High-Speed Analog Comparator 2	0x40085200
ACMPHS3	High-Speed Analog Comparator 3	0x40085300
ACMPHS4	High-Speed Analog Comparator 4	0x40085400
ACMPHS5	High-Speed Analog Comparator 5	0x40085500
TSD	Temperature Sensor Data	0x407FB17C

Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table 3.2:

- Registers are grouped by associated module
- The number of access cycles indicates the number of cycles based on the specified reference clock
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DMAC or DTC.

Table 3.2 shows the access cycles for the I/O registers.

Table 3.2 Access cycles for I/O registers (1 of 2)

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MMPU, SMPU, SPMON, MMF, SRAM, BUS, DMACn, DMA, DTC, ICU, DBG, FCACHE	4000 0000h	4001 CFFFh	4				ICLK	Memory Protection Unit, Memory Mirror Function, SRAM, Buses, DMA Controller Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
SYSTEM	4001 E000h	4001 E3FFh	5				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
SYSTEM	4001 E400h	4001 E6FFh	9		5 to 8		PCLKB	Low Power Modes, Resets, Low Voltage Detection, AGT Input Control
PORTn, PFS, PMISC, ELC, POEG, INIT, WDT, IWDT, CAC, MSTP	4004 0000h	4004 7FFFh	3		2 to 3		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Register to be initialized after reset release, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control
CANn, IICn, DOC, ADC12n, TSN, DAC12	4004 E000h	4005 FFFFh	3		2 to 3		PCLKB	Controller Area Network Module, I2C Bus Interface, Data Operation Circuit, 12-Bit A/D Converter, Temperature Sensor, 12-Bit D/A Converter
SCIn	4007 0000h	4007 0EFFh	3*2		2 to 3*2		PCLKA	Serial Communications Interface

Table 3.2 Access cycles for I/O registers (2 of 2)

Peripherals	Address		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*1		Cycle unit	Related function
	From	To	Read	Write	Read	Write		
IRDA	4007 0F00h	4007 0FFFh	3		2 to 3		PCLKA	IrDA Interface
SPI0, SPI1	4007 2000h	4007 2FFFh	3*3		2 to 3*3		PCLKA	Serial Peripheral Interface
CRC	4007 4000h	4007 4FFFh	3		2 to 3		PCLKA	CRC Calculator
GPT32EHi, GPT32Ej, GPT32k, GPT_OPS	4007 8000h	4007 8FFFh	5	3	4 to 5	2 to 3	PCLKA	General PWM Timer
			2		1 to 2			
GPT_ODC	4007 B000h	4007 BFFFh	2		1 to 2		PCLKA	PWM Delay Generation Circuit
KINT	4008 0000h	4008 1FFFh	2		1 to 2		PCLKB	Key interrupt Function
AGTn	4008 4000h	4008 4FFFh	5	3	4 to 5	2 to 3	PCLKB	Asynchronous General Purpose Timer
ACMPHSn	4008 5000h	4008 5FFFh	2		1 to 2		PCLKB	High-Speed Analog Comparator
TSD	407FB17Ch	407FB17Ch	2	-	2	-	ICLK	Temperature Sensor

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.

Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.

Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

3.3 Register Descriptions

This section provides information associated with registers described in this manual.

Table 3.3 shows a list of registers including address offsets, address sizes, access rights, and reset values.

Table 3.3 Register description (1 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
MMPU	-	-	-	MMPUCTLA	Bus Master MPU Control Register	0x000	16	read-write	0x0000	0xFFFF
				MMPUPTA	Group A Protection of Register	0x102	16	read-write	0x0000	0xFFFF
	32	0x010	0-31	MMPUACA%s	Group A Region %s Access Control Register	0x200	16	read-write	0x0000	0xFFFF
	32	0x010	0-31	MMPUSA%s	Group A Region %s Start Address Register	0x204	32	read-write	0x0000 0000	0x00000 003
	32	0x010	0-31	MMPUEA%s	Group A Region %s End Address Register	0x208	32	read-write	0x0000 0003	0x00000 003
SMPU	-	-	-	SMPUCTL	Slave MPU Control Register	0x00	16	read-write	0x0000	0xFFFF
				SMPUMBIU	Access Control Register for MBIU	0x10	16	read-write	0x2000	0xFFFF
				SMPUFBIU	Access Control Register for FBIU	0x14	16	read-write	0x0000	0xFFFF
	3	0x4	0,2,6	SMPUP%sBIU	Access Control Register for P%sBIU	0x20	16	read-write	0x0000	0xFFFF

Table 3.3 Register description (2 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SPMON	-	-	-	MSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0x00	16	read-write	0x0000	0xFFFF
				MSPMPUCTL	Stack Pointer Monitor Access Control Register	0x04	16	read-write	0x0000	0xFEFF
				MSPMPUPT	Stack Pointer Monitor Protection Register	0x06	16	read-write	0x0000	0xFFFF
				MSPMPUSA	Main Stack Pointer Monitor Start Address Register	0x08	32	read-write	0x0000 0000	0x00000 003
				MSPMPUEA	Main Stack Pointer Monitor End Address Register	0x0C	32	read-write	0x0000 0003	0x00000 003
				PSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0x10	16	read-write	0x0000	0xFFFF
				PSPMPUCTL	Stack Pointer Monitor Access Control Register	0x14	16	read-write	0x0000	0xFEFF
				PSPMPUPT	Stack Pointer Monitor Protection Register	0x16	16	read-write	0x0000	0xFFFF
				PSPMPUSA	Process Stack Pointer Monitor Start Address Register	0x18	32	read-write	0x0000 0000	0x00000 003
				PSPMPUEA	Process Stack Pointer Monitor End Address Register	0x1C	32	read-write	0x0000 0003	0x00000 003
MMF	-	-	-	MMSFR	MemMirror Special Function Register	0x00	32	read-write	0x0000 0000	0xFFFF FFFF
				MMEN	MemMirror Enable Register	0x04	32	read-write	0x0000 0000	0xFFFF FFFF
SRAM	-	-	-	PARIOAD	SRAM Parity Error Operation After Detection Register	0x00	8	read-write	0x00	0xFF
				SRAMPRCR	SRAM Protection Register	0x04	8	read-write	0x00	0xFF
BUS	2	0x4	M4I, M4D	BUSMCNT%s	Master Bus Control Register %s	0x1000	16	read-write	0x0000	0xFFFF
	-	-	-	BUSMCNTSYS	Master Bus Control Register SYS	0x1008	16	read-write	0x0000	0xFFFF
	-	-	-	BUSMCNTDMA	Master Bus Control Register DMA	0x100C	16	read-write	0x0000	0xFFFF
	2	0x4	FLI,RAMH	BUSSCNT%s	Slave Bus Control Register %s	0x1100	16	read-write	0x0000	0xFFFF
	-	-	-	BUSSCNTMBIU	Slave Bus Control Register MBIU	0x1108	16	read-write	0x0000	0xFFFF
	4	0x4	P0B, P2B, P3B, P4B	BUSSCNT%s	Slave Bus Control Register %s	0x1114	16	read-write	0x0000	0xFFFF
	-	-	-	BUSSCNTP6B	Slave Bus Control Register P6B	0x1128	16	read-write	0x0000	0xFFFF
	3	0x4	FBU	BUSSCNT%s	Slave Bus Control Register %s	0x1130	16	read-write	0x0000	0xFFFF
	4	0x10	1-4	BUS%sERRADD	Bus Error Address Register %s	0x1800	32	read-only	0x0000 0000	0x00000 000

Table 3.3 Register description (3 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
BUS	4	0x10	1-4	BUS%sERRSTAT	Bus Error Status Register %s	0x1804	8	read-only	0x00	0xFE
DMAC0-7	-	-	-	DMSAR	DMA Source Address Register	0x00	32	read-write	0x0000 0000	0xFFFF FFFF
				DMDAR	DMA Destination Address Register	0x04	32	read-write	0x0000 0000	0xFFFF FFFF
				DMCRA	DMA Transfer Count Register	0x08	32	read-write	0x0000 0000	0xFFFF FFFF
				DMCRB	DMA Block Transfer Count Register	0x0C	16	read-write	0x0000	0xFFFF
				DMTMD	DMA Transfer Mode Register	0x10	16	read-write	0x0000	0xFFFF
				DMINT	DMA Interrupt Setting Register	0x13	8	read-write	0x00	0xFF
				DMAMD	DMA Address Mode Register	0x14	16	read-write	0x0000	0xFFFF
				DMOFR	DMA Offset Register	0x18	32	read-write	0x0000 0000	0xFFFF FFFF
				DMCNT	DMA Transfer Enable Register	0x1C	8	read-write	0x00	0xFF
				DMREQ	DMA Software Start Register	0x1D	8	read-write	0x00	0xFF
				DMSTS	DMAC Module Activation Register	0x1E	8	read-write	0x00	0xFF
DMA	-	-	-	DMAST	DMA Module Activation Register	0x00	8	read-write	0x00	0xFF
DTC	-	-	-	DTCCR	DTC Control Register	0x00	8	read-write	0x08	0xFF
				DTCVBR	DTC Vector Base Register	0x04	32	read-write	0x0000 0000	0xFFFF FFFF
				DTCST	DTC Module Start Register	0x0C	8	read-write	0x00	0xFF
				DTCSTS	DTC Status Register	0x0E	16	read-only	0x0000	0xFFFF
ICU	14	0x1	0-13	IRQCR%s	IRQ Control Register %s	0x000	8	read-write	0x00	0xFF
	-	-	-	NMICR	NMI Pin Interrupt Control Register	0x100	8	read-write	0x00	0xFF
				NMIER	Non-Maskable Interrupt Enable Register	0x120	16	read-write	0x0000	0xFFFF
				NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	write-only	0x0000	0xFFFF
				NMISR	Non-Maskable Interrupt Status Register	0x140	16	read-only	0x0000	0xFFFF
				WUPEN	Wakeup Interrupt Enable Register	0x1A0	32	read-write	0x0000 0000	0xFFFF FFFF
				SELSR0	SYS Event Link Setting Register	0x200	16	read-write	0x0000	0xFFFF
	8	0x4	0-7	DELSR%s	DMAC Event Link Setting Register %s	0x280	32	read-write	0x0000	0xFFFF
	96	0x4	0-95	IELSR%s	INT Event Link Setting Register %s	0x300	32	read-write	0x0000 0000	0xFFFF FFFF

Table 3.3 Register description (4 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
DBG	-	-	-	DBGSTR	Debug Status Register	0x000	32	read-only	0x0000 0000	0xFFFF FFFF
				DBGSTOPCR	Debug Stop Control Register	0x010	32	read-write	0x0000 0003	0xFFFF FFFF
				TRACECTR	Trace Control Register	0x020	32	read-write	0x0000 0000	0xFFFF FFFF
FCACHE	-	-	-	FCACHEE	Flash Cache Enable Register	0x100	16	read-write	0x0000	0xFFFF
				FCACHEIV	Flash Cache Invalidate Register	0x104	16	read-write	0x0000	0xFFFF
				FLWT	Flash Wait Cycle Register	0x11C	8	read-write	0x00	0xFF
SYSTEM	-	-	-	SBYCR	Standby Control Register	0x00C	16	read-write	0x4000	0xFFFF
				MSTPCRA	Module Stop Control Register A	0x01C	32	read-write	0xFFBF FF1C	0xFFFF FFFF
				SCKDIVCR	System Clock Division Control Register	0x020	32	read-write	0x2202 2222	0xFFFF FFFF
				SCKSCR	System Clock Source Control Register	0x026	8	read-write	0x01	0xFF
				PLLCCR	PLL Clock Control Register	0x028	16	read-write	0x1300	0xFFFF
				PLLCR	PLL Control Register	0x02A	8	read-write	0x01	0xFF
				MOSCCR	Main Clock Oscillator Control Register	0x032	8	read-write	0x01	0xFF
				HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	read-write	0x00	0xFE
				MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	read-write	0x00	0xFF
				FLLCR1	FLL Control Register 1	0x039	8	read-write	0x00	0xFF
				FLLCR2	FLL Control Register 2	0x03A	16	read-write	0x0000	0xFFFF
				OSCSF	Oscillation Stabilization Flag Register	0x03C	8	read-only	0x00	0xFE
				CKOCR	Clock Out Control Register	0x03E	8	read-write	0x00	0xFF
				TRCKCR	Trace Clock Control Register	0x03F	8	read-write	0x01	0xFF
				OSTDCR	Oscillation Stop Detection Control Register	0x040	8	read-write	0x00	0xFF
				OSTDSR	Oscillation Stop Detection Status Register	0x041	8	read-write	0x00	0xFF
				MOCOUTCR	MOCO User Trimming Control Register	0x061	8	read-write	0x00	0xFF
				HOCOUTCR	HOCO User Trimming Control Register	0x062	8	read-write	0x00	0xFF
				SNZCR	Snooze Control Register	0x092	8	read-write	0x00	0xFF

Table 3.3 Register description (5 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SYSTEM	-	-	-	SNZEDCR	Snooze End Control Register	0x094	8	read-write	0x00	0xFF
				SNZREQCR	Snooze Request Control Register	0x098	32	read-write	0x00000000	0xFFFFFFFF
				OPCCR	Operating Power Control Register	0x0A0	8	read-write	0x00	0xFF
				MOSCWTCR	Main Clock Oscillator Wait Control Register	0x0A2	8	read-write	0x05	0xFF
				HOCOWTCR	High-speed on-chip oscillator wait control register	0x0A5	8	read-write	0x02	0xFF
				SOPCCR	Sub Operating Power Control Register	0x0AA	8	read-write	0x00	0xFF
				RSTSR1	Reset Status Register 1	0x0C0	16	read-write	0x0000	0xE0F8
	2	0x2	1,2	LVD%sCR1	Voltage Monitor %s Circuit Control Register 1	0x0E0	8	read-write	0x01	0xFF
	2	0x2	1,2	LVD%sSR	Voltage Monitor %s Circuit Status Register	0x0E1	8	read-write	0x02	0xFF
	-	-	-	PRCR	Protect Register	0x3FE	16	read-write	0x0000	0xFFFF
				DPSBYCR	Deep Standby Control Register	0x400	8	read-write	0x01	0xFF
				DPSIER0	Deep Standby Interrupt Enable Register 0	0x402	8	read-write	0x00	0xFF
				DPSIER1	Deep Standby Interrupt Enable Register 1	0x403	8	read-write	0x00	0xFF
				DPSIER2	Deep Standby Interrupt Enable Register 2	0x404	8	read-write	0x00	0xFF
				DPSIER3	Deep Standby Interrupt Enable Register 3	0x405	8	read-write	0x00	0xFF
				DPSIFR0	Deep Standby Interrupt Flag Register 0	0x406	8	read-write	0x00	0xFF
				DPSIFR1	Deep Standby Interrupt Flag Register 1	0x407	8	read-write	0x00	0xFF
				DPSIFR2	Deep Standby Interrupt Flag Register 2	0x408	8	read-write	0x00	0xFF
				DPSIFR3	Deep Standby Interrupt Flag Register 3	0x409	8	read-write	0x00	0xFF
				DPSIEGR0	Deep Standby Interrupt Edge Register 0	0x40A	8	read-write	0x00	0xFF
				DPSIEGR1	Deep Standby Interrupt Edge Register 1	0x40B	8	read-write	0x00	0xFF
				DPSIEGR2	Deep Standby Interrupt Edge Register 2	0x40C	8	read-write	0x00	0xFF
				SYOCDCR	System Control OCD Control Register	0x40E	8	read-write	0x00	0xFE
				STCONR	Standby Condition Register	0x40F	8	read-write	0xC3	0xFF
				RSTSR0	Reset Status Register 0	0x410	8	read-write	0x00	0x70
				RSTSR2	Reset Status Register 2	0x411	8	read-write	0x00	0xFE

Table 3.3 Register description (6 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SYSTEM	-	-	-	MOMCR	Main Clock Oscillator Mode Oscillation Control Register	0x413	8	read-write	0x00	0xFF
				FWEPROR	Flash P/E Protect Register	0x416	8	read-write	0x02	0xFF
				LVCMPCR	Voltage Monitor Circuit Control Register	0x417	8	read-write	0x00	0xFF
				LVDLVLR	Voltage Detection Level Select Register	0x418	8	read-write	0xF3	0xFF
	2	0x1	1, 2	LVD%sCR0	Voltage Monitor %s Circuit Control Register 0	0x41A	8	read-write	0x8A	0xF7
	-	-	-	SOSCCR	Sub-clock oscillator control register	0x480	8	read-write	0x00	0xFF
				SOMCR	Sub Clock Oscillator Mode Control Register	0x481	8	read-write	0x00	0xFD
				LOCOCR	Low-Speed On-Chip Oscillator Control Register	0x490	8	read-write	0x00	0xFF
				LOCOUTCR	LOCO User Trimming Control Register	0x492	8	read-write	0x00	0xFF
				VBTICTLR	AGT Input Control Register	0x4BB	8	read-write	0x00	0xF8
PORT0, 5-7	-	-	-	PCNTR1	Port Control Register 1	0x00	32	read-write	0x0000 0000	0xFFFF FFFF
				PODR	Output data register	0x00	16	read-write	0x0000	0xFFFF
				PDR	Data direction register	0x02	16	read-write	0x0000	0xFFFF
				PCNTR2	Port Control Register 2	0x04	32	read-only	0x0000 0000	0xFFFF 0000
				PIDR	Input data register	0x06	16	read-only	0x0000	0x0000
				PCNTR3	Port Control Register 3	0x08	32	write-only	0x0000 0000	0xFFFF FFFF
				PORR	Output reset register	0x08	16	write-only	0x0000	0xFFFF
				POSR	Output set register	0x0A	16	write-only	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR1	Port Control Register 1	0x00	32	read-write	0x0000 0000	0xFFFF FFFF
				PODR	Output data register	0x00	16	read-write	0x0000	0xFFFF
				PDR	Data direction register	0x02	16	read-write	0x0000	0xFFFF
				PCNTR2	Port Control Register 2	0x04	32	read-only	0x0000 0000	0xFFFF 0000
				EIDR	Event input data register	0x04	16	read-only	0x0000	0x0000
				PIDR	Input data register	0x06	16	read-only	0x0000	0x0000
				PCNTR3	Port Control Register 3	0x08	32	write-only	0x0000 0000	0xFFFF FFFF

Table 3.3 Register description (7 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PORT1-4	-	-	-	PORR	Output set register	0x08	16	write-only	0x0000	0xFFFF
				POSR	Output reset register	0x0A	16	write-only	0x0000	0xFFFF
				PCNTR4	Port Control Register 4	0x0C	32	read-write	0x0000 0000	0xFFFF FFFF
				EORR	Event output set register	0x0C	16	read-write	0x0000	0xFFFF
				EOSR	Event output reset register	0x0E	16	read-write	0x0000	0xFFFF
PFS	-	-	-	P000PFS	P000 Pin Function Control Register	0x000	32	read-write	0x0000 8000	0xFFFF FFFD
				P000PFS_HA	P000 Pin Function Control Register	0x002	16	read-write	0x8000	0xFFFD
				P000PFS_BY	P000 Pin Function Control Register	0x003	8	read-write	0x00	0xFD
	7	0x4	1-7	P00%sPFS	P00%s Pin Function Control Register	0x004	32	read-write	0x0000 8000	0xFFFF FFFD
	7	0x4	1-7	P00%sPFS_HA	P00%s Pin Function Control Register	0x006	16	read-write	0x8000	0xFFFD
	7	0x4	1-7	P00%sPFS_BY	P00%s Pin Function Control Register	0x007	8	read-write	0x00	0xFD
	-	-	-	P008PFS	P008 Pin Function Control Register	0x020	32	read-write	0x0000 0000	0xFFFF FFFD
				P008PFS_HA	P008 Pin Function Control Register	0x022	16	read-write	0x0000	0xFFFD
				P008PFS_BY	P008 Pin Function Control Register	0x023	8	read-write	0x00	0xFD
	2	0x4	14-15	P0%sPFS	P0%s Pin Function Control Register	0x038	32	read-write	0x0000 0000	0xFFFF FFFD
	2	0x4	14-15	P0%sPFS_HA	P0%s Pin Function Control Register	0x03A	16	read-write	0x0000	0xFFFD
	2	0x4	14-15	P0%sPFS_BY	P0%s Pin Function Control Register	0x03B	8	read-write	0x00	0xFD
	-	-	-	P100PFS	P100 Pin Function Control Register	0x040	32	read-write	0x0000 0000	0xFFFF FFFD
				P100PFS_HA	P100 Pin Function Control Register	0x042	16	read-write	0x0000	0xFFFD
				P100PFS_BY	P100 Pin Function Control Register	0x043	8	read-write	0x00	0xFD
	7	0x4	1-7	P10%sPFS	P10%s Pin Function Control Register	0x044	32	read-write	0x0000 0000	0xFFFF FFFD
	7	0x4	1-7	P10%sPFS_HA	P10%s Pin Function Control Register	0x046	16	read-write	0x0000	0xFFFD
	7	0x4	1-7	P10%sPFS_BY	P10%s Pin Function Control Register	0x047	8	read-write	0x00	0xFD
	-	-	-	P108PFS	P108 Pin Function Control Register	0x060	32	read-write	0x0001 0410	0xFFFF FFFD
				P108PFS_HA	P108 Pin Function Control Register	0x062	16	read-write	0x0410	0xFFFD
				P108PFS_BY	P108 Pin Function Control Register	0x063	8	read-write	0x10	0xFD

Table 3.3 Register description (8 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PFS	-	-	-	P109PFS	P109 Pin Function Control Register	0x064	32	read-write	0x0001 0410	0xFFFF FFFD
				P109PFS_HA	P109 Pin Function Control Register	0x066	16	read-write	0x0410	0xFFFD
				P109PFS_BY	P109 Pin Function Control Register	0x067	8	read-write	0x10	0xFD
				P110PFS	P110 Pin Function Control Register	0x068	32	read-write	0x0001 0010	0xFFFF FFFD
				P110PFS_HA	P110 Pin Function Control Register	0x06A	16	read-write	0x0010	0xFFFD
				P110PFS_BY	P110 Pin Function Control Register	0x06B	8	read-write	0x10	0xFD
	5	0x4	11-15	P1%sPFS	P1%s Pin Function Control Register	0x06C	32	read-write	0x0000 0000	0xFFFF FFFD
	5	0x4	11-15	P1%sPFS_HA	P1%s Pin Function Control Register	0x06E	16	read-write	0x0000	0xFFFD
	5	0x4	11-15	P1%sPFS_BY	P1%s Pin Function Control Register	0x06F	8	read-write	0x00	0xFD
	-	-	-	P200PFS	P200 Pin Function Control Register	0x080	32	read-write	0x0000 0000	0xFFFF FFFD
				P200PFS_HA	P200 Pin Function Control Register	0x082	16	read-write	0x0000	0xFFFD
				P200PFS_BY	P200 Pin Function Control Register	0x083	8	read-write	0x00	0xFD
				P201PFS	P201 Pin Function Control Register	0x084	32	read-write	0x0000 0010	0xFFFF FFFD
				P201PFS_HA	P201 Pin Function Control Register	0x086	16	read-write	0x0010	0xFFFD
				P201PFS_BY	P201 Pin Function Control Register	0x087	8	read-write	0x10	0xFD
	5	0x4	5-9	P20%sPFS	P20%s Pin Function Control Register	0x094	32	read-write	0x0000 0000	0xFFFF FFFD
	5	0x4	5-9	P20%sPFS_HA	P20%s Pin Function Control Register	0x096	16	read-write	0x0000	0xFFFD
	5	0x4	5-9	P20%sPFS_BY	P20%s Pin Function Control Register	0x097	8	read-write	0x00	0xFD
	5	0x4	10-14	P2%sPFS	P2%s Pin Function Control Register	0x0A8	32	read-write	0x0000 0000	0xFFFF FFFD
	5	0x4	10-14	P2%sPFS_HA	P2%s Pin Function Control Register	0x0AA	16	read-write	0x0000	0xFFFD
	5	0x4	10-14	P2%sPFS_BY	P2%s Pin Function Control Register	0x0AB	8	read-write	0x00	0xFD
	-	-	-	P300PFS	P300 Pin Function Control Register	0x0C0	32	read-write	0x0001 0010	0xFFFF FFFD
				P300PFS_HA	P300 Pin Function Control Register	0x0C2	16	read-write	0x0010	0xFFFD
				P300PFS_BY	P300 Pin Function Control Register	0x0C3	8	read-write	0x10	0xFD
	7	0x4	1-7	P30%sPFS	P30%s Pin Function Control Register	0x0C4	32	read-write	0x0000 0000	0xFFFF FFFD
	7	0x4	1-7	P30%sPFS_HA	P30%s Pin Function Control Register	0x0C6	16	read-write	0x0000	0xFFFD

Table 3.3 Register description (9 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PFS	7	0x4	1-7	P30%sPFS_BY	P30%s Pin Function Control Register	0x0C7	8	read-write	0x00	0xFD
	10	0x4	0-9	P40%sPFS	P40%s Pin Function Control Register	0x100	32	read-write	0x0000 0000	0xFFFF FFFD
	10	0x4	0-9	P40%sPFS_HA	P40%s Pin Function Control Register	0x102	16	read-write	0x0000	0xFFFD
	10	0x4	0-9	P40%sPFS_BY	P40%s Pin Function Control Register	0x103	8	read-write	0x00	0xFD
	6	0x4	10-15	P4%sPFS	P4%s Pin Function Control Register	0x128	32	read-write	0x0000 0000	0xFFFF FFFD
	6	0x4	10-15	P4%sPFS_HA	P4%s Pin Function Control Register	0x12A	16	read-write	0x0000	0xFFFD
	6	0x4	10-15	P4%sPFS_BY	P4%s Pin Function Control Register	0x12B	8	read-write	0x00	0xFD
	5	0x4	0-4	P50%sPFS	P50%s Pin Function Control Register	0x140	32	read-write	0x0000 0000	0xFFFF FFFD
	5	0x4	0-4	P50%sPFS_HA	P50%s Pin Function Control Register	0x142	16	read-write	0x0000	0xFFFD
	5	0x4	0-4	P50%sPFS_BY	P50%s Pin Function Control Register	0x143	8	read-write	0x00	0xFD
	-	-	-	P508PFS	P508 Pin Function Control Register	0x160	32	read-write	0x0000 0000	0xFFFF FFFD
				P508PFS_HA	P508 Pin Function Control Register	0x162	16	read-write	0x0000	0xFFFD
				P508PFS_BY	P508 Pin Function Control Register	0x163	8	read-write	0x00	0xFD
	3	0x4	0-2	P60%sPFS	P60%s Pin Function Control Register	0x180	32	read-write	0x0000 0000	0xFFFF FFFD
	3	0x4	0-2	P60%sPFS_HA	P60%s Pin Function Control Register	0x182	16	read-write	0x0000	0xFFFD
	3	0x4	0-2	P60%sPFS_BY	P60%s Pin Function Control Register	0x183	8	read-write	0x00	0xFD
	2	0x4	8-9	P60%sPFS	P60%s Pin Function Control Register	0x1A0	32	read-write	0x0000 0000	0xFFFF FFFD
	2	0x4	8-9	P60%sPFS_HA	P60%s Pin Function Control Register	0x1A2	16	read-write	0x0000	0xFFFD
	2	0x4	8-9	P60%sPFS_BY	P60%s Pin Function Control Register	0x1A3	8	read-write	0x00	0xFD
	-	-	-	P610PFS	P610 Pin Function Control Register	0x1A8	32	read-write	0x0000 0000	0xFFFF FFFD
				P610PFS_HA	P610 Pin Function Control Register	0x1AA	16	read-write	0x0000	0xFFFD
				P610PFS_BY	P610 Pin Function Control Register	0x1AB	8	read-write	0x00	0xFD
				P708PFS	P708 Pin Function Control Register	0x1E0	32	read-write	0x0000 0000	0xFFFF FFFD
				P708PFS_HA	P708 Pin Function Control Register	0x1E2	16	read-write	0x0000	0xFFFD
				P708PFS_BY	P708 Pin Function Control Register	0x1E3	8	read-write	0x00	0xFD
PMISC	-	-	-	PWPR	Write-Protect Register	0x03	8	read-write	0x80	0xFF

Table 3.3 Register description (10 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ELC	-	-	-	ELCR	Event Link Controller Register	0x00	8	read-write	0x00	0xFF
	2	0x2	0,1	ELSEGR%s	Event Link Software Event Generation Register %s	0x02	8	read-write	0x80	0xFF
	19	0x4	0-18	ELSR%s	Event Link Setting Register %s	0x10	16	read-write	0x0000	0xFFFF
POEG	4	0x100	A,B,C,D	POEGG%s	POEG Group %s Setting Register	0x00	32	read-write	0x0000 0000	0xFFFF FFFF
INIT	-	-	-	RCR1	Reset Control Register 1	0x22	8	read-write	0x00	0x0A
				RCR2	Reset Control Register 2	0x24	8	read-write	0x00	0x0E
				RCR4	Reset Control Register 4	0x28	8	read-write	0x00	0xFE
WDT	-	-	-	WDTRR	WDT Refresh Register	0x00	8	read-write	0xFF	0xFF
				WDTCR	WDT Control Register	0x02	16	read-write	0x33F3	0xFFFF
				WDTSR	WDT Status Register	0x04	16	read-write	0x0000	0xFFFF
				WDTRCR	WDT Reset Control Register	0x06	8	read-write	0x80	0xFF
				WDTCSTPR	WDT Count Stop Control Register	0x08	8	read-write	0x80	0xFF
IWDT	-	-	-	IWDTRR	IWDT Refresh Register	0x00	8	read-write	0xFF	0xFF
				IWDTSR	IWDT Status Register	0x04	16	read-write	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC Control Register 0	0x00	8	read-write	0x00	0xFF
				CACR1	CAC Control Register 1	0x01	8	read-write	0x00	0xFF
				CACR2	CAC Control Register 2	0x02	8	read-write	0x00	0xFF
				CAICR	CAC Interrupt Control Register	0x03	8	read-write	0x00	0xFF
				CASTR	CAC Status Register	0x04	8	read-only	0x00	0xFF
				CAULVR	CAC Upper-Limit Value Setting Register	0x06	16	read-write	0x0000	0xFFFF
				CALLVR	CAC Lower-Limit Value Setting Register	0x08	16	read-write	0x0000	0xFFFF
				CACNTBR	CAC Counter Buffer Register	0x0A	16	read-only	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	Module Stop Control Register B	0x00	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				MSTPCRC	Module Stop Control Register C	0x04	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				MSTPCRD	Module Stop Control Register D	0x08	32	read-write	0xFFFF FFFF	0xFFFF FFFF
CAN0	32	0x10	0-31	MB%s_ID	Mailbox Register	0x200	32	read-write	0x0000 0000	0x00000 000

Table 3.3 Register description (11 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
CAN0	32	0x10	0-31	MB%s_DL	Mailbox Register	0x204	16	read-write	0x0000	0x0000
	32	0x10	0-31	MB%s_D0	Mailbox Register	0x206	8	read-write	0x00	0x00
	32	0x10	0-31	MB%s_D1	Mailbox Register	0x207	8	read-write	0x00	0x00
	32	0x10	0-31	MB%s_D2	Mailbox Register	0x208	8	read-write	0x00	0x00
	32	0x10	0-31	MB%s_D3	Mailbox Register	0x209	8	read-write	0x00	0x00
	32	0x10	0-31	MB%s_D4	Mailbox Register	0x20A	8	read-write	0x00	0x00
	32	0x10	0-31	MB%s_D5	Mailbox Register	0x20B	8	read-write	0x00	0x00
	32	0x10	0-31	MB%s_D6	Mailbox Register	0x20C	8	read-write	0x00	0x00
	32	0x10	0-31	MB%s_D7	Mailbox Register	0x20D	8	read-write	0x00	0x00
	32	0x10	0-31	MB%s_TS	Mailbox Register	0x20E	16	read-write	0x0000	0x0000
	8	0x4	0-7	MKR[%s]	Mask Register	0x400	32	read-write	0x00000000	0x00000000
	2	0x4	0,1	FIDCR%s	FIFO Received ID Compare Registers	0x420	32	read-write	0x00000000	0x00000000
	-	-	-	MKIVLR	Mask Invalid Register	0x428	32	read-write	0x00000000	0x00000000
				MIER	Mailbox Interrupt Enable Register	0x42C	32	read-write	0x00000000	0x00000000
				MIER_FIFO	Mailbox Interrupt Enable Register for FIFO Mailbox Mode	0x42C	32	read-write	0x00000000	0x00000000
	32	0x1	0-31	MCTL_TX[%s]	Message Control Register for Transmit	0x820	8	read-write	0x00	0xFF
	32	0x1	0-31	MCTL_RX[%s]	Message Control Register for Receive	0x820	8	read-write	0x00	0xFF
	-	-	-	CTLR	Control Register	0x840	16	read-write	0x0500	0xFFFF
				STR	Status Register	0x842	16	read-only	0x0500	0xFFFF
				BCR	Bit Configuration Register	0x844	32	read-write	0x00000000	0xFFFFFFFF
				RFCR	Receive FIFO Control Register	0x848	8	read-write	0x80	0xFF
				RFPCR	Receive FIFO Pointer Control Register	0x849	8	write-only	0x00	0x00
				TFCR	Transmit FIFO Control Register	0x84A	8	read-write	0x80	0xFF
				TFPCR	Transmit FIFO Pointer Control Register	0x84B	8	write-only	0x00	0x00
				EIER	Error Interrupt Enable Register	0x84C	8	read-write	0x00	0xFF
				EIFR	Error Interrupt Factor Judge Register	0x84D	8	read-write	0x00	0xFF

Table 3.3 Register description (12 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
CAN0	-	-	-	RECR	Receive Error Count Register	0x84E	8	read-only	0x00	0xFF
				TECR	Transmit Error Count Register	0x84F	8	read-only	0x00	0xFF
				ECSR	Error Code Store Register	0x850	8	read-write	0x00	0xFF
				CSSR	Channel Search Support Register	0x851	8	read-write	0x00	0x00
				MSSR	Mailbox Search Status Register	0x852	8	read-only	0x80	0xFF
				MSMR	Mailbox Search Mode Register	0x853	8	read-write	0x00	0xFF
				TSR	Time Stamp Register	0x854	16	read-only	0x0000	0xFFFF
				AFSR	Acceptance Filter Support Register	0x856	16	read-write	0x0000	0x0000
				TCR	Test Control Register	0x858	8	read-write	0x00	0xFF
IIC0	-	-	-	ICCR1	I2C Bus Control Register 1	0x00	8	read-write	0x1F	0xFF
				ICCR2	I2C Bus Control Register 2	0x01	8	read-write	0x00	0xFF
				ICMR1	I2C Bus Mode Register 1	0x02	8	read-write	0x08	0xFF
				ICMR2	I2C Bus Mode Register 2	0x03	8	read-write	0x06	0xFF
				ICMR3	I2C Bus Mode Register 3	0x04	8	read-write	0x00	0xFF
				ICFER	I2C Bus Function Enable Register	0x05	8	read-write	0x72	0xFF
				ICSER	I2C Bus Status Enable Register	0x06	8	read-write	0x09	0xFF
				ICIER	I2C Bus Interrupt Enable Register	0x07	8	read-write	0x00	0xFF
				ICSR1	I2C Bus Status Register 1	0x08	8	read-write	0x00	0xFF
				ICSR2	I2C Bus Status Register 2	0x09	8	read-write	0x00	0xFF
	3	0x2	0-2	SARL%s	Slave Address Register L%s	0x0A	8	read-write	0x00	0xFF
	3	0x2	0-2	SARU%s	Slave Address Register U%s	0x0B	8	read-write	0x00	0xFF
	-	-	-	ICBRL	I2C Bus Bit Rate Low-Level Register	0x10	8	read-write	0xFF	0xFF
				ICBRH	I2C Bus Bit Rate High-Level Register	0x11	8	read-write	0xFF	0xFF
				ICDRT	I2C Bus Transmit Data Register	0x12	8	read-write	0xFF	0xFF
				ICDRR	I2C Bus Receive Data Register	0x13	8	read-only	0x00	0xFF
				ICWUR	I2C Bus Wake Up Unit Register	0x16	8	read-write	0x00	0xFF

Table 3.3 Register description (13 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
IIC0	-	-	-	ICWUR2	I2C Bus Wake Up Unit Register 2	0x17	8	read-only	0x03	0xFF
IIC1	-	-	-	ICCR1	I2C Bus Control Register 1	0x00	8	read-write	0x1F	0xFF
				ICCR2	I2C Bus Control Register 2	0x01	8	read-write	0x00	0xFF
				ICMR1	I2C Bus Mode Register 1	0x02	8	read-write	0x08	0xFF
				ICMR2	I2C Bus Mode Register 2	0x03	8	read-write	0x06	0xFF
				ICMR3	I2C Bus Mode Register 3	0x04	8	read-write	0x00	0xFF
				ICFER	I2C Bus Function Enable Register	0x05	8	read-write	0x72	0xFF
				ICSER	I2C Bus Status Enable Register	0x06	8	read-write	0x09	0xFF
				ICIER	I2C Bus Interrupt Enable Register	0x07	8	read-write	0x00	0xFF
				ICSR1	I2C Bus Status Register 1	0x08	8	read-write	0x00	0xFF
				ICSR2	I2C Bus Status Register 2	0x09	8	read-write	0x00	0xFF
	3	0x2	0-2	SARL%s	Slave Address Register L%s	0x0A	8	read-write	0x00	0xFF
	3	0x2	0-2	SARU%s	Slave Address Register U%s	0x0B	8	read-write	0x00	0xFF
	-	-	-	ICBRL	I2C Bus Bit Rate Low-Level Register	0x10	8	read-write	0xFF	0xFF
				ICBRH	I2C Bus Bit Rate High-Level Register	0x11	8	read-write	0xFF	0xFF
				ICDRT	I2C Bus Transmit Data Register	0x12	8	read-write	0xFF	0xFF
				ICDRR	I2C Bus Receive Data Register	0x13	8	read-only	0x00	0xFF
DOC	-	-	-	DOCR	DOC Control Register	0x00	8	read-write	0x00	0xFF
				DODIR	DOC Data Input Register	0x02	16	read-write	0x0000	0xFFFF
				DODSR	DOC Data Setting Register	0x04	16	read-write	0x0000	0xFFFF
ADC120	-	-	-	ADCSR	A/D Control Register	0x000	16	read-write	0x0000	0xFFFF
				ADANSA0	A/D Channel Select Register A0	0x004	16	read-write	0x0000	0xFFFF
				ADANSA1	A/D Channel Select Register A1	0x006	16	read-write	0x0000	0xFFFF
				ADADS0	A/D-Converted Value Addition/Average Channel Select Register 0	0x008	16	read-write	0x0000	0xFFFF
				ADADS1	A/D-Converted Value Addition/Average Channel Select Register 1	0x00A	16	read-write	0x0000	0xFFFF

Table 3.3 Register description (14 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC120	-	-	-	ADADC	A/D-Converted Value Addition/Average Count Select Register	0x00C	8	read-write	0x00	0xFF
				ADCER	A/D Control Extended Register	0x00E	16	read-write	0x0000	0xFFFF
				ADSTRGR	A/D Conversion Start Trigger Select Register	0x010	16	read-write	0x0000	0xFFFF
				ADEXICR	A/D Conversion Extended Input Control Register	0x012	16	read-write	0x0000	0xFFFF
				ADANSB0	A/D Channel Select Register B0	0x014	16	read-write	0x0000	0xFFFF
				ADANSB1	A/D Channel Select Register B1	0x016	16	read-write	0x0000	0xFFFF
				ADDBLDR	A/D Data Duplication Register	0x018	16	read-only	0x0000	0xFFFF
				ADTSDR	A/D Temperature Sensor Data Register	0x01A	16	read-only	0x0000	0xFFFF
				ADOCDR	A/D Internal Reference Voltage Data Register	0x01C	16	read-only	0x0000	0xFFFF
				ADRD	A/D Self-Diagnosis Data Register	0x01E	16	read-only	0x0000	0xFFFF
	4	0x2	0-3	ADDR%s	A/D Data Register %s	0x020	16	read-only	0x0000	0xFFFF
	3	0x2	5-7	ADDR%s	A/D Data Register %s	0x02A	16	read-only	0x0000	0xFFFF
	3	0x2	16-18	ADDR%s	A/D Data Register %s	0x040	16	read-only	0x0000	0xFFFF
				ADDR20	A/D Data Register 20	0x048	16	read-only	0x0000	0xFFFF
	-	-	-	ADSHCR	A/D Sample and Hold Circuit Control Register	0x066	16	read-write	0x0018	0xFFFF
				ADDISCR	A/D Disconnection Detection Control Register	0x07A	8	read-write	0x00	0xFF
				ADSHMSR	A/D Sample and Hold Operation Mode Select Register	0x07C	8	read-write	0x00	0xFF
				ADGSPCR	A/D Group Scan Priority Control Register	0x080	16	read-write	0x0000	0xFFFF
				ADDBLDRA	A/D Data Duplication Register A	0x084	16	read-only	0x0000	0xFFFF
				ADDBLDRB	A/D Data Duplication Register B	0x086	16	read-only	0x0000	0xFFFF
				ADWINMON	A/D Compare Function Window A/B Status Monitor Register	0x08C	8	read-only	0x00	0xFF
				ADCMPCR	A/D Compare Function Control Register	0x090	16	read-write	0x0000	0xFFFF
				ADCMPANSER	A/D Compare Function Window A Extended Input Select Register	0x092	8	read-write	0x00	0xFF

Table 3.3 Register description (15 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC120	-	-	-	ADCMPLER	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	0x093	8	read-write	0x00	0xFF
				ADCMPANSR0	A/D Compare Function Window A Channel Select Register 0	0x094	16	read-write	0x0000	0xFFFF
				ADCMPANSR1	A/D Compare Function Window A Channel Select Register 1	0x096	16	read-write	0x0000	0xFFFF
				ADCMPLR0	A/D Compare Function Window A Comparison Condition Setting Register 0	0x098	16	read-write	0x0000	0xFFFF
				ADCMPLR1	A/D Compare Function Window A Comparison Condition Setting Register 1	0x09A	16	read-write	0x0000	0xFFFF
				ADCMPDR0	A/D Compare Function Window A Lower-Side Level Setting Register	0x09C	16	read-write	0x0000	0xFFFF
				ADCMPDR1	A/D Compare Function Window A Upper-Side Level Setting Register	0x09E	16	read-write	0x0000	0xFFFF
				ADCMPSR0	A/D Compare Function Window A Channel Status Register 0	0x0A0	16	read-write	0x0000	0xFFFF
				ADCMPSR1	A/D Compare Function Window A Channel Status Register 1	0x0A2	16	read-write	0x0000	0xFFFF
				ADCMPSER	A/D Compare Function Window A Extended Input Channel Status Register	0x0A4	8	read-write	0x00	0xFF
				ADCMPBNSR	A/D Compare Function Window B Channel Selection Register	0x0A6	8	read-write	0x00	0xFF
				ADWINLLB	A/D Compare Function Window B Lower-Side Level Setting Register	0x0A8	16	read-write	0x0000	0xFFFF
				ADWINULB	A/D Compare Function Window B Upper-Side Level Setting Register	0x0AA	16	read-write	0x0000	0xFFFF
				ADCMPBSR	A/D Compare Function Window B Status Register	0x0AC	8	read-write	0x00	0xFF
				ADSSTRL	A/D Sampling State Register L	0x0DD	8	read-write	0x0B	0xFF
				ADSSTRT	A/D Sampling State Register T	0x0DE	8	read-write	0x0B	0xFF
				ADSSTRO	A/D Sampling State Register O	0x0DF	8	read-write	0x0B	0xFF
	4	0x1	0-3	ADSSTR0%s	A/D Sampling State Register %s (Corresponding Channel is AN00%s)	0x0E0	8	read-write	0x0B	0xFF

Table 3.3 Register description (16 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC120	3	0x1	5-7	ADSSTR0%s	A/D Sampling State Register %s (Corresponding Channel is AN00%s)	0x0E5	8	read-write	0x0B	0xFF
	-	-	-	ADPGACR	A/D Programmable Gain Amplifier Control Register	0x1A0	16	read-write	0x0000	0xFFFF
				ADPGAGS0	A/D Programmable Gain Amplifier Gain Setting Register 0	0x1A2	16	read-write	0x0000	0xFFFF
				ADPGADCR0	A/D Programmable Gain Amplifier Pseudo-Differential Input Control Register	0x1B0	16	read-write	0x8888	0xFFFF
ADC121	-	-	-	ADCSR	A/D Control Register	0x000	16	read-write	0x0000	0xFFFF
				ADANSA0	A/D Channel Select Register A0	0x004	16	read-write	0x0000	0xFFFF
				ADANSA1	A/D Channel Select Register A1	0x006	16	read-write	0x0000	0xFFFF
				ADADS0	A/D-Converted Value Addition/Average Channel Select Register 0	0x008	16	read-write	0x0000	0xFFFF
				ADADS1	A/D-Converted Value Addition/Average Channel Select Register 1	0x00A	16	read-write	0x0000	0xFFFF
				ADADC	A/D-Converted Value Addition/Average Count Select Register	0x00C	8	read-write	0x00	0xFF
				ADCER	A/D Control Extended Register	0x00E	16	read-write	0x0000	0xFFFF
				ADSTRGR	A/D Conversion Start Trigger Select Register	0x010	16	read-write	0x0000	0xFFFF
				ADEXICR	A/D Conversion Extended Input Control Register	0x012	16	read-write	0x0000	0xFFFF
				ADANSB0	A/D Channel Select Register B0	0x014	16	read-write	0x0000	0xFFFF
				ADANSB1	A/D Channel Select Register B1	0x016	16	read-write	0x0000	0xFFFF
				ADDBLDR	A/D Data Duplication Register	0x018	16	read-only	0x0000	0xFFFF
				ADTSDR	A/D Temperature Sensor Data Register	0x01A	16	read-only	0x0000	0xFFFF
				ADOCDR	A/D Internal Reference Voltage Data Register	0x01C	16	read-only	0x0000	0xFFFF
				ADRD	A/D Self-Diagnosis Data Register	0x01E	16	read-only	0x0000	0xFFFF
	3	0x2	0-2	ADDR%s	A/D Data Register %s	0x020	16	read-only	0x0000	0xFFFF
	3	0x2	5-7	ADDR%s	A/D Data Register %s	0x02A	16	read-only	0x0000	0xFFFF

Table 3.3 Register description (17 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC121	2	0x2	16,17	ADDR%s	A/D Data Register %s	0x040	16	read-only	0x0000	0xFFFF
	-	-	-	ADSHCR	A/D Sample and Hold Circuit Control Register	0x066	16	read-write	0x0018	0xFFFF
				ADDISCR	A/D Disconnection Detection Control Register	0x07A	8	read-write	0x00	0xFF
				ADSHMSR	A/D Sample and Hold Operation Mode Select Register	0x07C	8	read-write	0x00	0xFF
				ADGSPCR	A/D Group Scan Priority Control Register	0x080	16	read-write	0x0000	0xFFFF
				ADDBLDRA	A/D Data Duplication Register A	0x084	16	read-only	0x0000	0xFFFF
				ADDBLDRB	A/D Data Duplication Register B	0x086	16	read-only	0x0000	0xFFFF
				ADWINMON	A/D Compare Function Window A/B Status Monitor Register	0x08C	8	read-only	0x00	0xFF
				ADCMPCR	A/D Compare Function Control Register	0x090	16	read-write	0x0000	0xFFFF
				ADCMPANSER	A/D Compare Function Window A Extended Input Select Register	0x092	8	read-write	0x00	0xFF
				ADCMPLER	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	0x093	8	read-write	0x00	0xFF
				ADCMPANSR0	A/D Compare Function Window A Channel Select Register 0	0x094	16	read-write	0x0000	0xFFFF
				ADCMPANSR1	A/D Compare Function Window A Channel Select Register 1	0x096	16	read-write	0x0000	0xFFFF
				ADCMPLR0	A/D Compare Function Window A Comparison Condition Setting Register 0	0x098	16	read-write	0x0000	0xFFFF
				ADCMPLR1	A/D Compare Function Window A Comparison Condition Setting Register 1	0x09A	16	read-write	0x0000	0xFFFF
				ADCMPDR0	A/D Compare Function Window A Lower-Side Level Setting Register	0x09C	16	read-write	0x0000	0xFFFF
				ADCMPDR1	A/D Compare Function Window A Upper-Side Level Setting Register	0x09E	16	read-write	0x0000	0xFFFF
				ADCMPSR0	A/D Compare Function Window A Channel Status Register 0	0x0A0	16	read-write	0x0000	0xFFFF
				ADCMPSR1	A/D Compare Function Window A Channel Status Register 1	0x0A2	16	read-write	0x0000	0xFFFF

Table 3.3 Register description (18 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC121	-	-	-	ADCMPSER	A/D Compare Function Window A Extended Input Channel Status Register	0x0A4	8	read-write	0x00	0xFF
				ADCMPBNSR	A/D Compare Function Window B Channel Selection Register	0x0A6	8	read-write	0x00	0xFF
				ADWINLLB	A/D Compare Function Window B Lower-Side Level Setting Register	0x0A8	16	read-write	0x0000	0xFFFF
				ADWINULB	A/D Compare Function Window B Upper-Side Level Setting Register	0x0AA	16	read-write	0x0000	0xFFFF
				ADCMPBSR	A/D Compare Function Window B Status Register	0x0AC	8	read-write	0x00	0xFF
				ADSSTRL	A/D Sampling State Register L	0x0DD	8	read-write	0x0B	0xFF
				ADSSTRT	A/D Sampling State Register T	0x0DE	8	read-write	0x0B	0xFF
				ADSSTRO	A/D Sampling State Register O	0x0DF	8	read-write	0x0B	0xFF
	3	0x1	0-2	ADSSTR0%s	A/D Sampling State Register %s (Corresponding Channel is AN10%s)	0x0E0	8	read-write	0x0B	0xFF
	3	0x1	5-7	ADSSTR0%s	A/D Sampling State Register %s (Corresponding Channel is AN10%s)	0x0E5	8	read-write	0x0B	0xFF
	-	-	-	ADPGACR	A/D Programmable Gain Amplifier Control Register	0x1A0	16	read-write	0x0000	0xFFFF
				ADPGAGS0	A/D Programmable Gain Amplifier Gain Setting Register 0	0x1A2	16	read-write	0x0000	0xFFFF
				ADPGADCR0	A/D Programmable Gain Amplifier Pseudo-Differential Input Control Register	0x1B0	16	read-write	0x8888	0xFFFF
TSN	-	-	-	TSCR	Temperature Sensor Control Register	0x00	8	read-write	0x00	0xFF
DAC12	2	0x2	0,1	DADR%s	D/A Data Register %s	0x00	16	read-write	0x0000	0xFFFF
	-	-	-	DACR	D/A Control Register	0x0004	8	read-write	0x1F	0xFF
				DADPR	DADRm Format Select Register	0x0005	8	read-write	0x00	0xFF
				DAADSCR	D/A-A/D Synchronous Start Control Register	0x0006	8	read-write	0x00	0xFF
				DAAMPCR	D/A Output Amplifier Control Register	0x0008	8	read-write	0x00	0xFF
				DAASWCR	D/A Amplifier Stabilization Wait Control Register	0x101C	8	read-write	0x00	0xFF

Table 3.3 Register description (19 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
DAC12	-	-	-	DAADUSR	D/A A/D Synchronous Unit Select Register	0x10C0	8	read-write	0x00	0xFF
SCI0-4,8,9	-	-	-	SMR	Serial Mode Register (SCMR.SMIF = 0)	0x00	8	read-write	0x00	0xFF
				SMR_SMCI	Serial mode register (SCMR.SMIF = 1)	0x00	8	read-write	0x00	0xFF
				BRR	Bit Rate Register	0x01	8	read-write	0xFF	0xFF
				SCR	Serial Control Register (SCMR.SMIF = 0)	0x02	8	read-write	0x00	0xFF
				SCR_SMCI	Serial Control Register (SCMR.SMIF =1)	0x02	8	read-write	0x00	0xFF
				TDR	Transmit Data Register	0x03	8	read-write	0xFF	0xFF
				SSR	Serial Status Register (SCMR.SMIF = 0 and FCR.FM=0)	0x04	8	read-write	0x84	0xFF
				SSR_FIFO	Serial Status Register (SCMR.SMIF = 0 and FCR.FM=1)	0x04	8	read-write	0x80	0xFD
				SSR_SMCI	Serial Status Register (SCMR.SMIF = 1)	0x04	8	read-write	0x84	0xFF
				RDR	Receive Data Register	0x05	8	read-only	0x00	0xFF
				SCMR	Smart Card Mode Register	0x06	8	read-write	0xF2	0xFF
				SEMR	Serial Extended Mode Register	0x07	8	read-write	0x00	0xFF
				SNFR	Noise Filter Setting Register	0x08	8	read-write	0x00	0xFF
				SIMR1	I2C Mode Register 1	0x09	8	read-write	0x00	0xFF
				SIMR2	I2C Mode Register 2	0x0A	8	read-write	0x00	0xFF
				SIMR3	I2C Mode Register 3	0x0B	8	read-write	0x00	0xFF
				SISR	I2C Status Register	0x0C	8	read-only	0x00	0xCB
				SPMR	SPI Mode Register	0x0D	8	read-write	0x00	0xFF
				TDRHL	Transmit 9-bit Data Register	0x0E	16	read-write	0xFFFF	0xFFFF
				FTDRHL	Transmit FIFO Data Register HL	0x0E	16	write-only	0xFFFF	0xFFFF
				FTDRH	Transmit FIFO Data Register H	0x0E	8	write-only	0xFF	0xFF
				FTDRL	Transmit FIFO Data Register L	0x0F	8	write-only	0xFF	0xFF
				RDRHL	Receive 9-bit Data Register	0x10	16	read-only	0x0000	0xFFFF
				FRDRHL	Receive FIFO Data Register HL	0x10	16	read-only	0x0000	0xFFFF
				FRDRH	Receive FIFO Data Register H	0x10	8	read-only	0x00	0xFF

Table 3.3 Register description (20 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SCI0-4,8,9	-	-	-	FRDRL	Receive FIFO Data Register L	0x11	8	read-only	0x00	0xFF
				MDDR	Modulation Duty Register	0x12	8	read-write	0xFF	0xFF
				DCCR	Data Compare Match Control Register	0x13	8	read-write	0x40	0xFF
				FCR	FIFO Control Register	0x14	16	read-write	0xF800	0xFFFF
				FDR	FIFO Data Count Register	0x16	16	read-only	0x0000	0xFFFF
				LSR	Line Status Register	0x18	16	read-only	0x0000	0xFFFF
				CDR	Compare Match Data Register	0x1A	16	read-write	0x0000	0xFFFF
				SPTR	Serial Port Register	0x1C	8	read-write	0x03	0xFF
IRDA	-	-	-	IRCR	IrDA Control Register	0x00	8	read-write	0x00	0xFF
SPI0,1	-	-	-	SPCR	SPI Control Register	0x00	8	read-write	0x00	0xFF
				SSLP	SPI Slave Select Polarity Register	0x01	8	read-write	0x00	0xFF
				SPPCR	RSPI Pin Control Register	0x02	8	read-write	0x00	0xFF
				SPSR	SPI Status Register	0x03	8	read-write	0x20	0xFF
				SPDR	SPI Data Register	0x04	32	read-write	0x0000 0000	0xFFFF FFFF
				SPDR_HA	SPI Data Register (halfword access)	0x04	16	read-write	0x0000	0xFFFF
				SPSCR	SPI Sequence Control Register	0x08	8	read-write	0x00	0xFF
				SPSSR	SPI Sequence Status Register	0x09	8	read-only	0x00	0xFF
				SPBR	SPI Bit Rate Register	0x0A	8	read-write	0xFF	0xFF
				SPDCR	SPI Data Control Register	0x0B	8	read-write	0x00	0xFF
				SPCKD	SPI Clock Delay Register	0x0C	8	read-write	0x00	0xFF
				SSLND	SPI Slave Select Negation Delay Register	0x0D	8	read-write	0x00	0xFF
				SPND	SPI Next-Access Delay Register	0x0E	8	read-write	0x00	0xFF
				SPCR2	SPI Control Register 2	0x0F	8	read-write	0x00	0xFF
	8	0x2	0-7	SPCMD%s	SPI Command Register %s	0x10	16	read-write	0x070D	0xFFFF
	-	-	-	SPDCR2	SPI Data Control Register 2	0x20	8	read-write	0x00	0xFF
CRC	-	-	-	CRCCR0	CRC Control Register0	0x00	8	read-write	0x00	0xFF

Table 3.3 Register description (21 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
CRC	-	-	-	CRCCR1	CRC Control Register1	0x01	8	read-write	0x00	0xFF
				CRCDIR	CRC Data Input Register	0x04	32	read-write	0x0000 0000	0xFFFF FFFF
				CRCDIR_BY	CRC Data Input Register (byte access)	0x04	8	read-write	0x00	0xFF
				CRCDOR	CRC Data Output Register	0x08	32	read-write	0x0000 0000	0xFFFF FFFF
				CRCDOR_HA	CRC Data Output Register (halfword access)	0x08	16	read-write	0x0000	0xFFFF
				CRCDOR_BY	CRC Data Output Register (byte access)	0x08	8	read-write	0x00	0xFF
				CRCSAR	Snoop Address Register	0x0C	16	read-write	0x0000	0xFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	read-write	0x0000 0000	0xFFFF FFFF
				GTSTR	General PWM Timer Software Start Register	0x04	32	read-write	0x0000 0000	0xFFFF FFFF
				GTSTP	General PWM Timer Software Stop Register	0x08	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTCLR	General PWM Timer Software Clear Register	0x0C	32	write-only	0x0000 0000	0xFFFF FFFF
				GTSSR	General PWM Timer Start Source Select Register	0x10	32	read-write	0x0000 0000	0xFFFF FFFF
				GTPSR	General PWM Timer Stop Source Select Register	0x14	32	read-write	0x0000 0000	0xFFFF FFFF
				GTCSR	General PWM Timer Clear Source Select Register	0x18	32	read-write	0x0000 0000	0xFFFF FFFF
				GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	read-write	0x0000 0000	0xFFFF FFFF
				GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	read-write	0x0000 0000	0xFFFF FFFF
				GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	read-write	0x0000 0000	0xFFFF FFFF
				GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	read-write	0x0000 0000	0xFFFF FFFF
				GTCR	General PWM Timer Control Register	0x2C	32	read-write	0x0000 0000	0xFFFF FFFF
				GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	read-write	0x0000 0001	0xFFFF FFFF
				GTIOR	General PWM Timer I/O Control Register	0x34	32	read-write	0x0000 0000	0xFFFF FFFF
				GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	read-write	0x0000 0000	0xFFFF FFFF

Table 3.3 Register description (22 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT32EH0-3,GPT32E4-7	-	-	-	GTST	General PWM Timer Status Register	0x3C	32	read-write	0x00008000	0xFFFFFFFF
				GTBER	General PWM Timer Buffer Enable Register	0x40	32	read-write	0x00000000	0xFFFFFFFF
				GTITC	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	0x44	32	read-write	0x00000000	0xFFFFFFFF
				GTCNT	General PWM Timer Counter	0x48	32	read-write	0x00000000	0xFFFFFFFF
				GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTPR	General PWM Timer Cycle Setting Register	0x64	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTPDBR	General PWM Timer Cycle Setting Double-Buffer Register	0x6C	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTADTRA	A/D Converter Start Request Timing Register A	0x70	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTADTBRA	A/D Converter Start Request Timing Buffer Register A	0x74	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTADTDBRA	A/D Converter Start Request Timing Double-Buffer Register A	0x78	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTADTRB	A/D Converter Start Request Timing Register B	0x7C	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTADTBRB	A/D Converter Start Request Timing Buffer Register B	0x80	32	read-write	0xFFFFFFFF	0xFFFFFFFF
				GTADTDBRB	A/D Converter Start Request Timing Double-Buffer Register B	0x84	32	read-write	0xFFFFFFFF	0xFFFFFFFF

Table 3.3 Register description (23 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT32EH0-3,GPT32E4-7	-	-	-	GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	read-write	0x0000 0000	0xFFFF FFFF
				GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTDVD	General PWM Timer Dead Time Value Register D	0x90	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTDBU	General PWM Timer Dead Time Buffer Register U	0x94	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTDBD	General PWM Timer Dead Time Buffer Register D	0x98	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTSOS	General PWM Timer Output Protection Function Status Register	0x9C	32	read-only	0x0000 0000	0xFFFF FFFF
				GTSOTR	General PWM Timer Output Protection Function Temporary Release Register	0xA0	32	read-write	0x0000 0000	0xFFFF FFFF
GPT328-GPT3212	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	read-write	0x0000 0000	0xFFFF FFFF
				GTSTR	General PWM Timer Software Start Register	0x04	32	read-write	0x0000 0000	0xFFFF FFFF
				GTSTP	General PWM Timer Software Stop Register	0x08	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTCLR	General PWM Timer Software Clear Register	0x0C	32	write-only	0x0000 0000	0xFFFF FFFF
				GTSSR	General PWM Timer Start Source Select Register	0x10	32	read-write	0x0000 0000	0xFFFF FFFF
				GTPSR	General PWM Timer Stop Source Select Register	0x14	32	read-write	0x0000 0000	0xFFFF FFFF
				GTCSR	General PWM Timer Clear Source Select Register	0x18	32	read-write	0x0000 0000	0xFFFF FFFF
				GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	read-write	0x0000 0000	0xFFFF FFFF
				GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	read-write	0x0000 0000	0xFFFF FFFF
				GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	read-write	0x0000 0000	0xFFFF FFFF
				GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	read-write	0x0000 0000	0xFFFF FFFF
				GTCR	General PWM Timer Control Register	0x2C	32	read-write	0x0000 0000	0xFFFF FFFF

Table 3.3 Register description (24 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT328-GPT3212	-	-	-	GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	read-write	0x0000 0001	0xFFFF FFFF
				GTIOR	General PWM Timer I/O Control Register	0x34	32	read-write	0x0000 0000	0xFFFF FFFF
				GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	read-write	0x0000 0000	0xFFFF FFFF
				GTST	General PWM Timer Status Register	0x3C	32	read-write	0x0000 8000	0xFFFF FFFF
				GTBER	General PWM Timer Buffer Enable Register	0x40	32	read-write	0x0000 0000	0xFFFF FFFF
				GTCNT	General PWM Timer Counter	0x48	32	read-write	0x0000 0000	0xFFFF FFFF
				GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTPR	General PWM Timer Cycle Setting Register	0x64	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	read-write	0xFFFF FFFF	0xFFFF FFFF
				GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	read-write	0x0000 0000	0xFFFF FFFF
				GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	read-write	0xFFFF FFFF	0xFFFF FFFF
GPT32EH0-3,GPT32E4-7	-	-	-	OPSCR	Output Phase Switching Control Register	0x00	32	read-write	0x0000 0000	0xFFFF FFFF
GPT_ODC	-	-	-	GTDLYCR	PWM Output Delay Control Register	0x00	16	read-write	0x0000	0xFFFF
				GTDLYCR2	PWM Output Delay Control Register2	0x02	16	read-write	0x0000	0xFFFF
	4	0x4	0-3	GTDLYR%sA	GTIOC%sA Rising Output Delay Register	0x18	16	read-write	0x0000	0xFFFF
	4	0x4	0-3	GTDLYR%sB	GTIOC%sB Rising Output Delay Register	0x1A	16	read-write	0x0000	0xFFFF

Table 3.3 Register description (25 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT_ODC	4	0x4	0-3	GTDLYF%sA	GTIOC%sA Falling Output Delay Register	0x28	16	read-write	0x0000	0xFFFF
	4	0x4	0-3	GTDLYF%sB	GTIOC%sB Falling Output Delay Register	0x2A	16	read-write	0x0000	0xFFFF
KINT	-	-	-	KRCTL	KEY Return Control Register	0x00	8	read-write	0x00	0xFF
				KRF	KEY Return Flag Register	0x04	8	read-write	0x00	0xFF
				KRM	KEY Return Mode Register	0x08	8	read-write	0x00	0xFF
AGT0,1	-	-	-	AGT	AGT Counter Register	0x00	16	read-write	0xFFFF	0xFFFF
				AGTCMA	AGT Compare Match A Register	0x02	16	read-write	0xFFFF	0xFFFF
				AGTCMB	AGT Compare Match B Register	0x04	16	read-write	0xFFFF	0xFFFF
				AGTCR	AGT Control Register	0x08	8	read-write	0x00	0xFF
				AGTMR1	AGT Mode Register 1	0x09	8	read-write	0x00	0xFF
				AGTMR2	AGT Mode Register 2	0x0A	8	read-write	0x00	0xFF
				AGTIOC	AGT I/O Control Register	0x0C	8	read-write	0x00	0xFF
				AGTISR	AGT Event Pin Select Register	0x0D	8	read-write	0x00	0xFF
				AGTCMSR	AGT Compare Match Function Select Register	0x0E	8	read-write	0x00	0xFF
				AGTIOSEL	AGT Pin Select Register	0x0F	8	read-write	0x00	0xFF
ACMPHS0	-	-	-	CMPCTL	Comparator Control Register	0x000	8	read-write	0x00	0xFF
				CMPSEL0	Comparator Input Select Register	0x004	8	read-write	0x00	0xFF
				CMPSEL1	Comparator Reference Voltage Select Register	0x008	8	read-write	0x00	0xFF
				CMPMON	Comparator Output Monitor Register	0x00C	8	read-only	0x00	0xFF
				CPIOC	Comparator Output Control Register	0x010	8	read-write	0x00	0xFF
ACMPHS1-5	-	-	-	CMPCTL	Comparator Control Register	0x000	8	read-write	0x00	0xFF
				CMPSEL0	Comparator Input Select Register	0x004	8	read-write	0x00	0xFF
				CMPSEL1	Comparator Reference Voltage Select Register	0x008	8	read-write	0x00	0xFF
				CMPMON	Comparator Output Monitor Register	0x00C	8	read-only	0x00	0xFF
				CPIOC	Comparator Output Control Register	0x010	8	read-write	0x00	0xFF
TSD	-	-	-	TSCDR	Temperature Sensor Calibration Data Register	0x00	32	read-only	0x0000 0000	0xFFFF F000

Peripheral name = Name of peripheral
Dim = Number of elements in an array of registers
Dim inc = Address increment between two simultaneous registers of a register array in the address map
Dim index = Sub string that replaces the %s placeholder within the register name
Register name = Name of register
Description = Register description
Address offset = Address of the register relative to the base address defined by the peripheral of the register
Size = Bit width of the register
Access = Register access rights:
Read-only: Read access is permitted. Write operations have undefined results.
Write-only: Write access is permitted. Read operations have undefined results.
Read-write: Both read and write accesses are permitted. Writes affect the state of the register and reads return a value related to the register.
Reset value = Default reset value of a register
Reset mask = Identifies which register bits have a defined reset value

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