SCT3258

Abridged Datasheet

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Change History

Version	Date	Change Descriptions
1.0	201308/05	Initial version
1.1	2013/10/23	Add DMR T2 support
1.2	2013/11/25	Update description for PLL
1.3	2013/12/16	Remove Pin HSTS
1.4	1/14/2014	Update the HPI Timing
1.5	10/27/2014	Add support for AMBE+2 Add support for TDMA direct mode， and input clock requirement for TDMA direct mode Add support the non-standard 55 Hz CTCSS tail tone Update naming conventions
1.6	01/09/2015	Add vocoder support information
1.7	02/06/2015	Update PIN definition
1.8	05/09/2016	Editorial changes
1.9	05/27/2016	Editorial changes
2.0	02/22/2018	Added footnotes for supply options, contact details for CML Microcircuits Ltd.
2.1	07/04/2018	Editorial changes for CML website publication

Contents:

Note: Content shown below in grey is only available in the full unabridged Datasheet.

1 Overview

SCT3258 is a low power high performance base band processor supporting DPMR and DMR protocol. With an external codec (audio band ADC and DAC), it completes the entire physical layer and data link layer, and most of the call control layer processing of DPMR and DMR protocol. In DPMR mode, SCT3258 complies with ETSI TS 102 490 and ETSI TS 102 658. In DMR mode, it complies with ETSI TS 102 361. Figure 1-1 shows SCT3258 used in a DPMR or DMR system with conventional RF circuits. Figure 1-2 shows SCT3258 used with SCT3700. SCT3258 is designed for easy migration from analog radios. The system designer can start with a typical analog radio, replacing the analog base band processor with SCT3258 together with an external codec, to obtain the simplest form of a DPMR or DMR radio. To achieve the full potential of DPMR or DMR, application level software programming is required on the host processor.

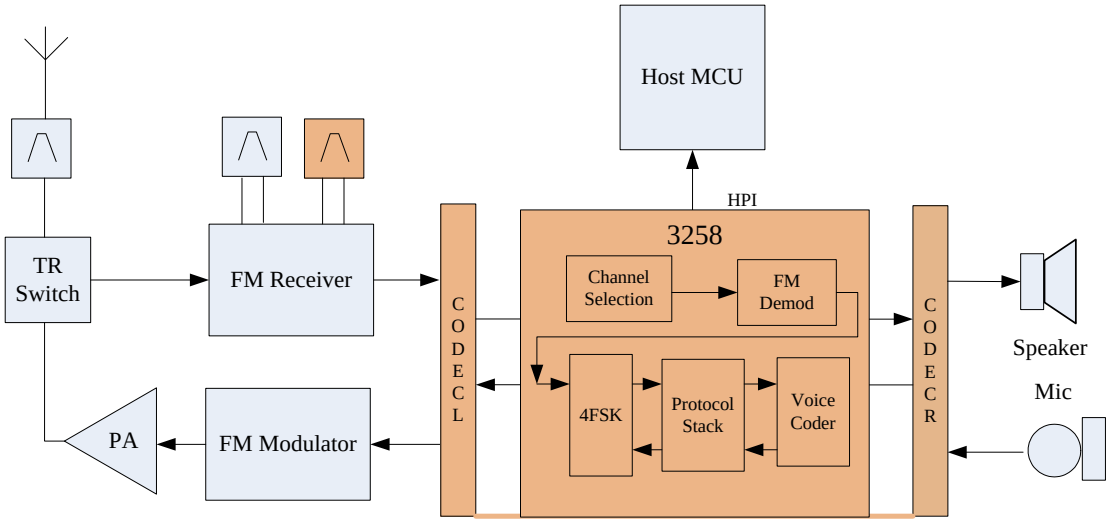


Figure 1-1 DPMR / DMR System Diagram with Conventional RF

SCT3258 contains two high-speed serial ports, a single 8-bit processor interface (HPI), and a 4-pin programmable I/O port. The two serial ports are used for connection with external codec and external vocoder.

SCT3258 communicates with host processor with 8 bit HPI port (Intel Mode or Motorola Mode).

The firmware of SCT3258 is stored on chip. At the start of the system, the host processor downloads a small boot loader to SCT3258 to get SCT3258 started. SCT3258 then loads the entire firmware and starts execution.

SCT3258 core logic operates at 1.2 V, and the I/O operates at 2.5-3.3V.

SCT3258 is packaged in QFN64.

2 Features

DPMR

- Support DPMR Tier 1 (ETSI TS 102 490)
- Support DPMR Tier 2 (ETSI TS 102 658) Mode 1 and Mode 2
- Air interface physical layer (layer 1)
- Air interface data link layer (layer 2)
- Air interface call control layer (layer 3)
- Full Annex A support, with BCD addressing and automatic call match

DMR

- Support DMR Tier1 and Tier 2 (ETSI TS 102 361)
- Air interface physical layer (layer 1)
- Air interface data link layer (layer 2)
- Air interface call control layer (layer 3)
- Annex C (TS 102 361-2 Annex C) support, with BCD addressing and automatic call match
- Transmit in slotted or continuous mode
- Receive in slotted or continuous mode
- Support TDMA direct mode

4 FSK Modem

- 4800 bps data rate for DPMR and 9600 bps for DMR
- Automatic frame sync detection
- Programmable modulation index
- Support two point modulation, and I/Q modulation
- BER Test Mode complied with ITU O.153

Vocoder[1]

- Build-in AMBE + 2 vocoder from DVSI (no security key)
- Support 1031 Hz Tone and Silence Test Mode
- Automatic vocoder switching at the receiver in DPMR mode

[1] Internal AMBE+2 is the default vocoder supported for DPMR/DMR operation, refer to CML sales representatives for the availability of other vocoder options.

Analog Mode Support

- Support voice channel filters (LPF/HPF/Limiter), as well as pre-emphasis and de-emphasis filters.
- Support CTCSS/DCS generation and detection
- Support arbitrary CTCSS/DCS code, and blind detection
- Support the non-standard 55 Hz CTCSS tail tone
- Support compander
- Automatic analog/digital mode detection (analog/DPMR or analog/DMR) in receiver mode

I/O

- Two high-speed TDM serial ports
- 8-bit HPI
- 4-pin PIO port

PLL

- On chip PLL circuit which provide system clock of up to 110.592MHz.

Technology

- QFN64 package
- Low power process, 38 mW in DPMR mode and 64 mW in DMR mode

3 Hardware Architecture

As shown in the diagram below, SCT3258 hardware architecture consists 4FSK modem, DSP core, on-chip instruction and data memory, Boot RAM, two high-speed serial ports (configured as I2S and McBSP port), the host processor interface (HPI), direct memory access (DMA) controller, PIOs, and a phase-locked loop (PLL).

The voice coder/decoder and DPMR / DMR protocol stack are implemented internally in SCT3258.

I2S is used for connection to an external codec, e.g. TLV320AIC3204 from TI or WM8758B from Wolfson. The HPI is used for connection to an external MCU for control. The SCT3258 has on chip flash to stores its firmware. At the start of the system, the host processor downloads a small boot loader to SCT3258 to get it started. SCT3258 then loads the entire firmware and starts execution.

SCT3258 also have an option to connect to an external vocoder (e.g. AMBE 3000) through serial port 0.

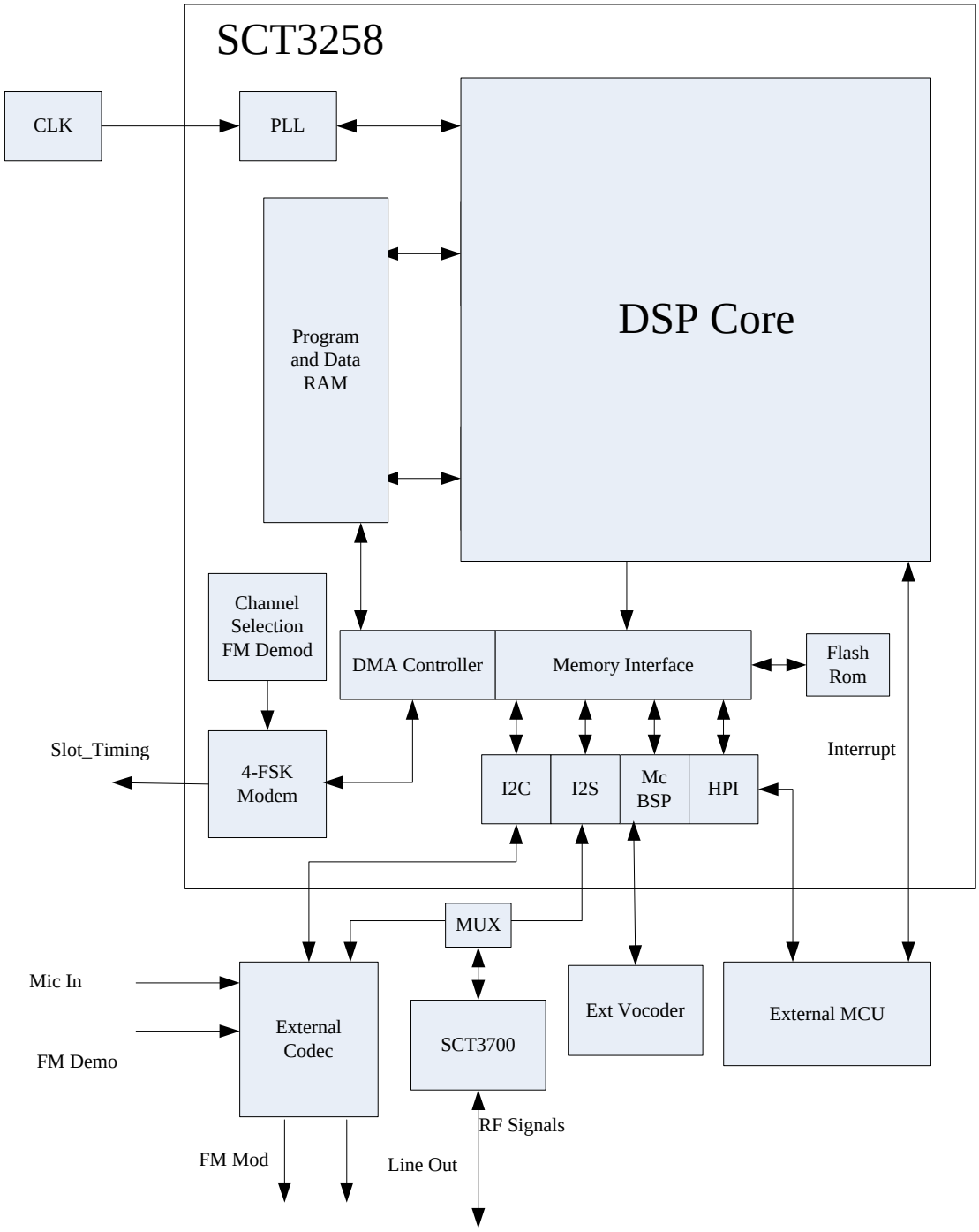


Figure 3-1 SCT3258 Architecture

4 Pin Configurations

SCT3258 is packaged in QFN64 package. The PINOUT of SCT3258 is described in Table 4-1.

PIN No.	PIN Name	I/O	Function
1	VDDIO33	P	I/O Device power
2	S1DO	O	Serial Port 1 Data Output
3	S1XFS	I/O	Serial Port 1 Transmit Frame Sync
4	S1CLK	I/O	Serial Port 1 Transmit or Receive Clock
5	S1RFS	I	Serial Port 1 Receive Frame Sync
6	S1DI	I	Serial Port 1 Data Input
7	VDD2	P	Core Power (1.2V)
8	VDDIO33	P	I/O Device power
9	S0DO	O	Serial Port 0 Data Output, connect to Pin19 FLASH_SI
10	S0XFS	I/O	Serial Port 0 Transmit Frame Sync, tie together with Pin13 S0RFS
11	S0XCLK	I/O	Serial Port 0 Transmit Clock
12	S0RCLK	I	Serial Port 0 Receive Clock
13	S0RFS	I	Serial Port 0 Receive Frame Sync, tie together with Pin10 S0XFS
14	S0DI	I	Serial Port 0 Data Input, connect to Pin42 FLASH_SO
15	PIO3/RF_TIMING	I/O	GPIO 3, RF_TIMING for DMR
16	PIO2	I/O	GPIO 2, connect to Pin40 /FLASH_CS
17	PIO1	I/O	GPIO 1
18	PIO0	I/O	GPIO0
19	FLASH_SI	I	SI for flash(refer to Pin9)
20	VDD2	P	Core Power (1.2V)
21	FLASH_SCK	I	SCK for flash
22	VDDIO33	P	I/O Device power
23	VDD2	P	Core Power (1.2V)
24	NC	-	No Connection
25	NC	-	No Connection
26	VDDIO33	P	I/O Device power
27	VDDIO33	P	I/O Device power
28	VDDIO33	P	I/O Device power
29	VDD2	P	Core Power (1.2V)
30	VDDIO33	P	I/O Device power
31	VDDIO33	P	I/O Device power
32	VDD2	P	Core Power (1.2V)
33	VDD2	P	Core Power (1.2V)

34	NC	-	No Connection
35	NC	-	No Connection
36	NC	-	No Connection
37	VDDIO33	P	I/O Device power
38	VDD2	P	Core Power (1.2V)
39	VDDIO33	P	I/O Device power
40	/FLASH_CS	I	/CS for flash(refer to Pin16)
41	VDD2	P	Core Power (1.2V)
42	FLASH_SO	O	SO for flash(refer to Pin14)
43	VDDIO33	P	I/O Device power
44	CLKOUT	O	Clock Out (Reflects the Processor Clock)
45	PLLBYPASS	I	PLL Bypass
46	CLKIN	I	Master Clock Input
47	PLLVDD	P	PLL Power (1.2V). We recommends the use of a ferrite bead to isolate VDD2 from PLLVDD
48	PLLSEL2	I	PLL Multiplier Select
49	VDD2	P	Core Power (1.2V)
50	HPIDATA7	I/O	HPI Data Bus
51	HPIDATA6	I/O	HPI Data Bus
52	HPIDATA5	I/O	HPI Data Bus
53	HPIDATA4	I/O	HPI Data Bus
54	HPIDATA3	I/O	HPI Data Bus
55	HPIDATA2	I/O	HPI Data Bus
56	HPIDATA1	I/O	HPI Data Bus
57	HPIDATA0	I/O	HPI Data Bus
58	NMI	I	Non-maskable Interrupt
59	RSTN	I	Device Reset
60	HOBIB	O	HPI Output Status
61	HRDN	I	Intel Mode Read Strobe / Motorola Mode Data Strobe.
62	HWRN	I	Intel Mode Host Write Strobe / Motorola Data Direction.
63	HCSN	I	Host Chip Select.
64	INT0	I	External Hardware Interrupt
65	GND	P	Package ground slug. Must be connect to GND

Table 4-1 PIN List for SCT3258

5 DPMR and DMR Implementation

SCT3258 supports the physical layer (layer 1), data link layer (layer 2), and call control layer (layer 3) of DPMR and DMR. Annex A of TS 102 490 / TS 102 658 and Annex C of TS 102 361-2 are also implemented. The user is expected to develop the application layer on the external MCU. This is illustrated in the diagram below.

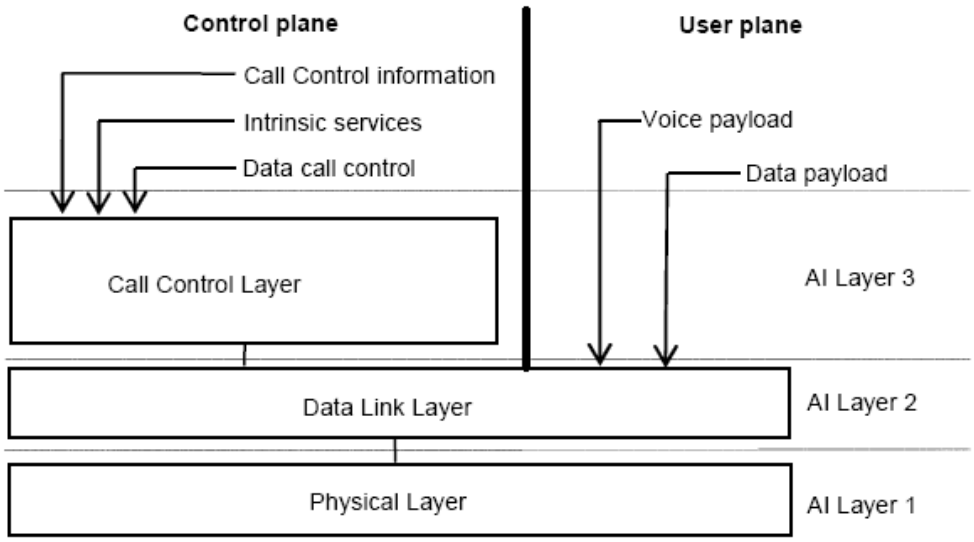


Figure 5-1 DPMR / DMR Protocol Structure

More specifically, the following are implemented in SCT3258 for each of the air interface layer.

Air Interface Physical Layer (Layer 1)

1. 4FSK modulation and demodulation, with programmable modulation index
2. Bit and Symbol definition
3. Frequency and symbol synchronization
4. Transmission burst building and splitting
5. BER test mode complied with O.153

Air Interface Data Link Layer (Layer 2)

1. Channel coding (FEC, CRC)
2. Interleaving, de-interleaving and bit ordering
3. Framing, super frame building and synchronization
4. Burst and parameter definition
5. Link addressing (source and destination)
6. Interfacing of voice applications (vocoder data) with PL
7. Data bearer services
8. Exchange signaling and user data with the CCL

Air Interface Call Control Layer (Layer 3)

1. Establishing, maintaining and termination of calls
2. Individual or group call transmission and receptions
3. Destination addressing
4. Automatic matching of Called ID of incoming call to own ID and group ID
5. Late entry call support

DPMR CSF (Annex A) Support

1. Full support of Standard User Interface (defined in Annex A of TS 102 490/TS 102 658)
2. Allows wild character dialing with "*"
3. Allows abbreviated dialing
4. Allows mask dialing
5. Syntax checking of dialed digits

DMR Dialing Number (Annex C) Support

1. Support of dialing number plan (defined in Annex C of TS 102 361-2)
2. Allows group calls with wild character "*"
3. Syntax checking of dialed digits

5.1 Signal Flow for DPMR / DMR Transmitter

The signal flow of the DPMR / DMR transmitter is shown in the diagram below.

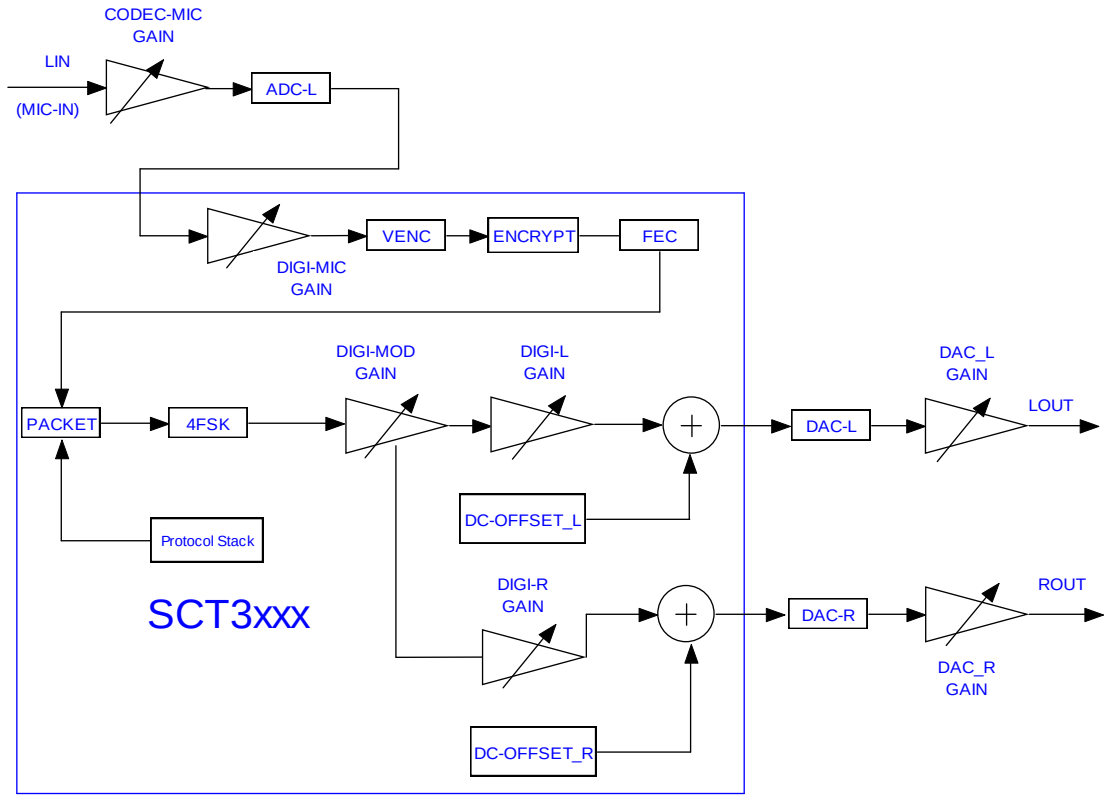


Figure 5-2 Signal Flow for DPMR / DMR Transmitter

The microphone signals are amplified by the VGA (variable gain amplifier) of the codec, and converted into digital form by the external codec and store in the left input channel buffer of SCT3258. The following steps are applied to the digitized signals:

1. Digital microphone gain, which provide a digital gain to the microphone. It is usually an attenuation to prevent microphone being saturated.
2. VENC, the voice encoder, which compress the voice signals into 2400 bps encoded signals
3. ENCRYPT, optional encryption block with configurable key
4. FEC, channel coding block, which adds 1200 bps to form 3600 bps signals for protecting of bit error
5. PACKET, which adds header and control information to form 4800 bps signals
6. 4FSK modulator
7. DIGI_MOD_GAIN, a gain block with linear 16 bit gain, for adjusting the modulation index

The resulting signals are split into left channel and right channel signals for two point modulation. Independent DC offsets and analog and digital gains are applied to the left and the right channels. The left channel control and the right channel control are identical, except that the left channel is multiplexed as speaker output in the RX mode. If DC coupling is used, the right channel is to be connected to VCTCXO input, while the left channel is connected to VCO. If AC coupling is used for VCTCXO control, either left or right channel can be connected to TCXO or VCO.

5.2 Signal Flow for DPMR / DMR Receiver

The signal flow of the DPMR / DMR receiver is shown in the diagram below.

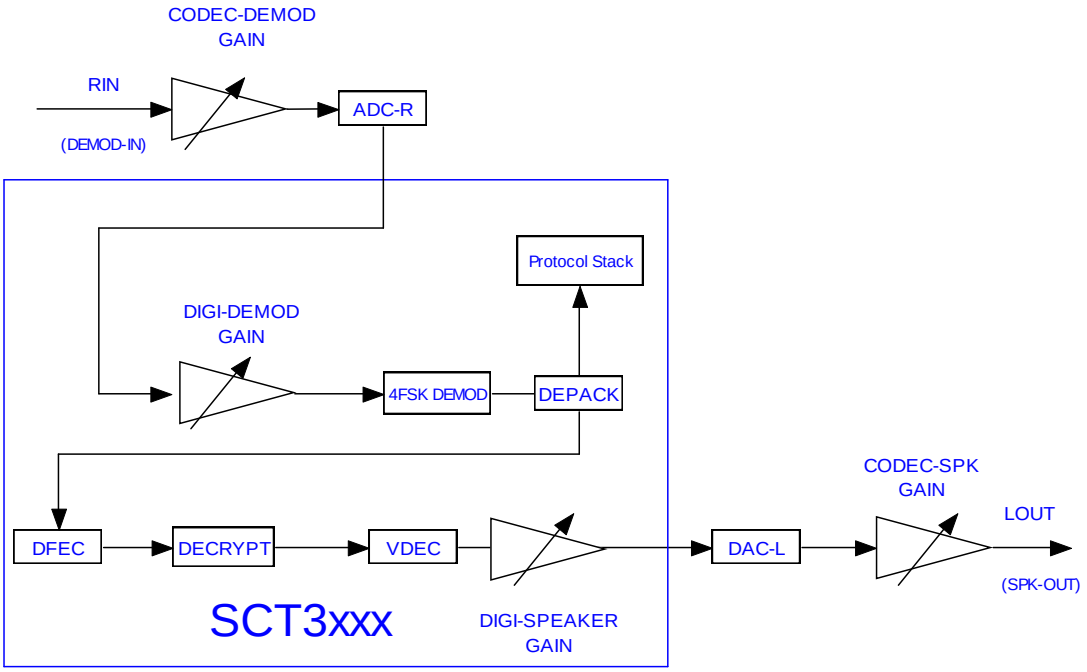


Figure 5-3 Signal Flow for DPMR / DMR Receiver for FM Demodulated Signal Input

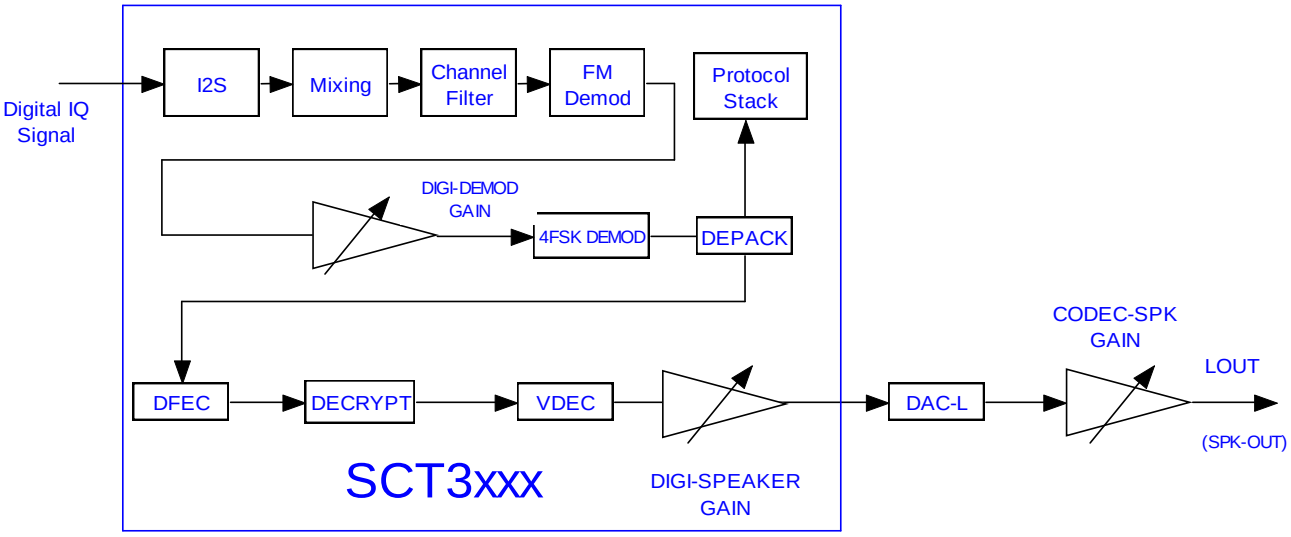


Figure 5-4 Signal Flow for DPMR/DMR Receiver for I/Q Signal Input

The FM demodulated signals are amplified by the VGA (variable gain amplifier) of the codec, and converted into digital form by the external codec and store in the right input channel buffer of SCT3258. The following steps are applied to the digitized signals:

1. DIGI_DEMOD_GAIN, a gain block with linear 16 bit gain
2. 4FSK demodulator
3. DEPACK, which removes header and extracts control and voice information
4. DFEC, channel decoding block, which recovers the encoded voice bits
5. DECRYPT, the optional decryption block with configurable key
6. VDEC, the voice decoder, which reconstructs voice signals
7. Digital Speaker Gain

The reconstructed voice signals are converted into analog form by the external codec and then amplified by the DAC analog gain block CODEC_SPK_GAIN before feeding to the audio PA.

For the I/Q signal case, the I/Q signal can be from digital interface or through an ADC. Additional processing is requires, such as IQ mixing, channel selection filter and FM demodulation. The rest of the process is the same as the demodulated case.

5.3 RF Timing Control for DMR

DMR signal is a two time slot TDMA signal, each slot occupying 30 milliseconds. In the RX mode, SCT3258 acquires timing from the synchronization pattern of the far end base station or mobile station. SCT3258 has an internal Slot Timing Signal (as shown in the diagram below) that is aligned with the FM demodulated signals or the I/Q signals at the input. In the TX mode,

SCT3258 controls the timing of the 4FSK modulation signals so that they are aligned with this internal RF timing signal. At the same time, an external signal is derived from the Slot Timing Signal and output through the RF_TIMING port to control the opening of the RF circuit and PA. The RF_TIMING signal is a square wave signals, with a period of 60 milliseconds. It can be exactly the same as the internal Slot Timing Signal, or offset from the Slot Timing Signal through MCU programming. The high level of RF_TIMING signal corresponds to RF circuit on, while the low level corresponds to RF circuit off. The MCU can derive the timing control signal to drive the RF transceiver or PA through the RF_TIMING signal from SCT3258.

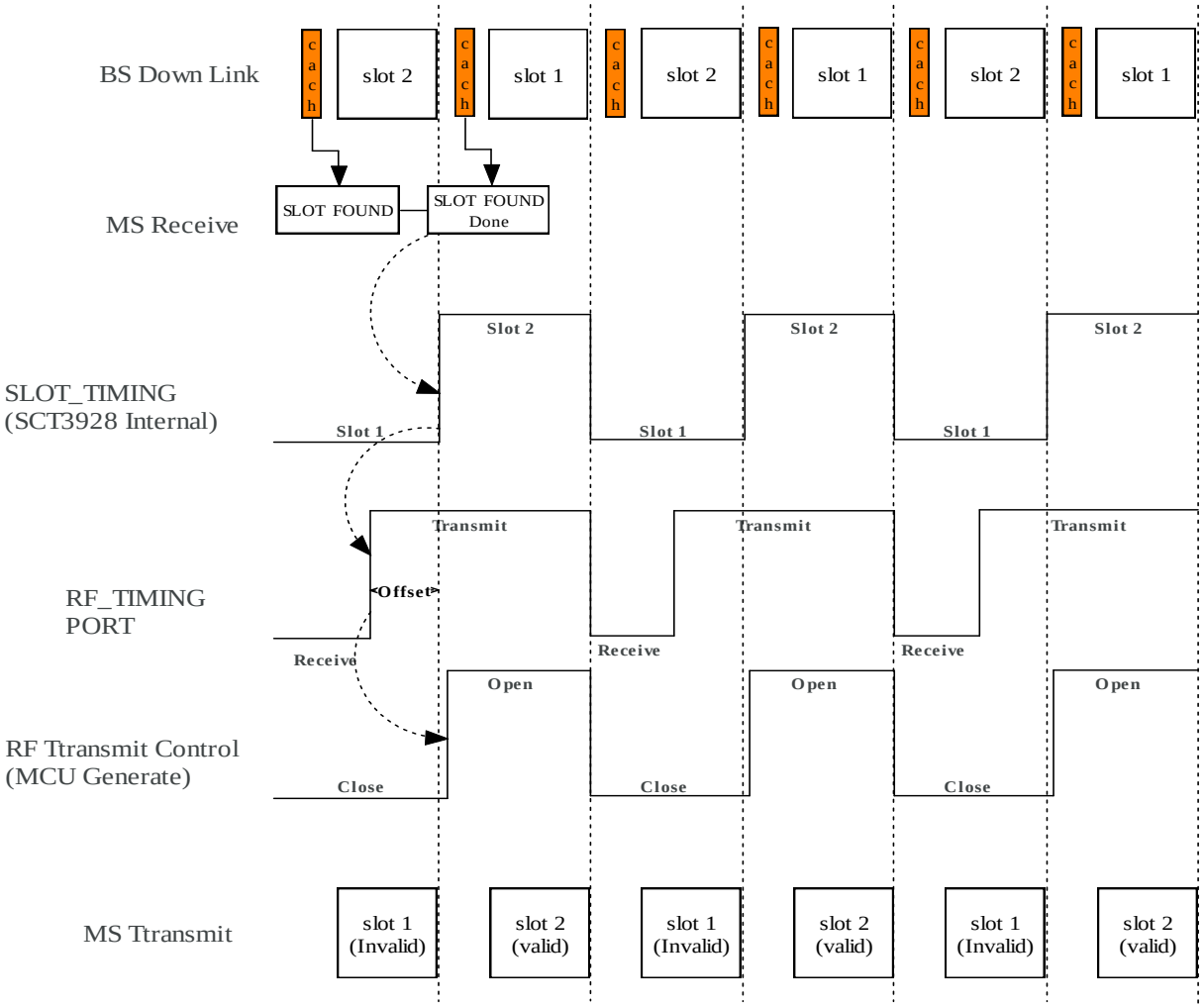


Figure 5-5 TDMA Timing Control of SCT3258

6 Vocoder Support[2]

SCT3258 supports the following vocoders:

- Build-in AMBE + 2 vocoder from DVSI (no security key)
- Support 1031 Hz Tone and Silence Test Mode

SCT3258 also supports external vocoder connection through its high speed serial port, and is pre-configured to support AMBE3000 from DVSI.

In DPMR mode, the receiver can be configured as automatic vocoder selection mode. In this mode, the receiver check the “Version” bit in the incoming DMPR bit stream and load the correct vocoder accordingly.

[2] Internal AMBE+2 is the default vocoder supported for DPMR/DMR operation, refer to CML sales representatives for the availability of other vocoder options.

7 Analog Radio Support

SCT3258 supports tri-mode operation with DPMR, DMR and analog radio. For analog radio, it complies with related standards for analog radio including TIA 603C and ETSI EN-300296.

SCT3258 analog processing blocks include:

- HPF, with stop band at 255 Hz and pass band at 300 Hz
- LPF, with pass band at 2550 Hz or 3000 Hz, and stop band at 6000 Hz
- Compander
- Pre-emphasis filter and de-emphasis filter at 6 dB/octave
- Limiter to limit the maximum frequency deviation
- Sub audio filter with pass band at 255 Hz and stop band at 300 Hz
- CTCSS/DCS generation and detection supporting 38/51 CTCSS code and 83/107 DCS code
- Support blind CTCSS/DCS detection
- Support automatic polarity detection for DCS code
- Support arbitrary CTCSS/DCS code

7.1 Signal Flow for Analog Transmitter

The signal flow of the analog transmitter is shown in the diagram below.

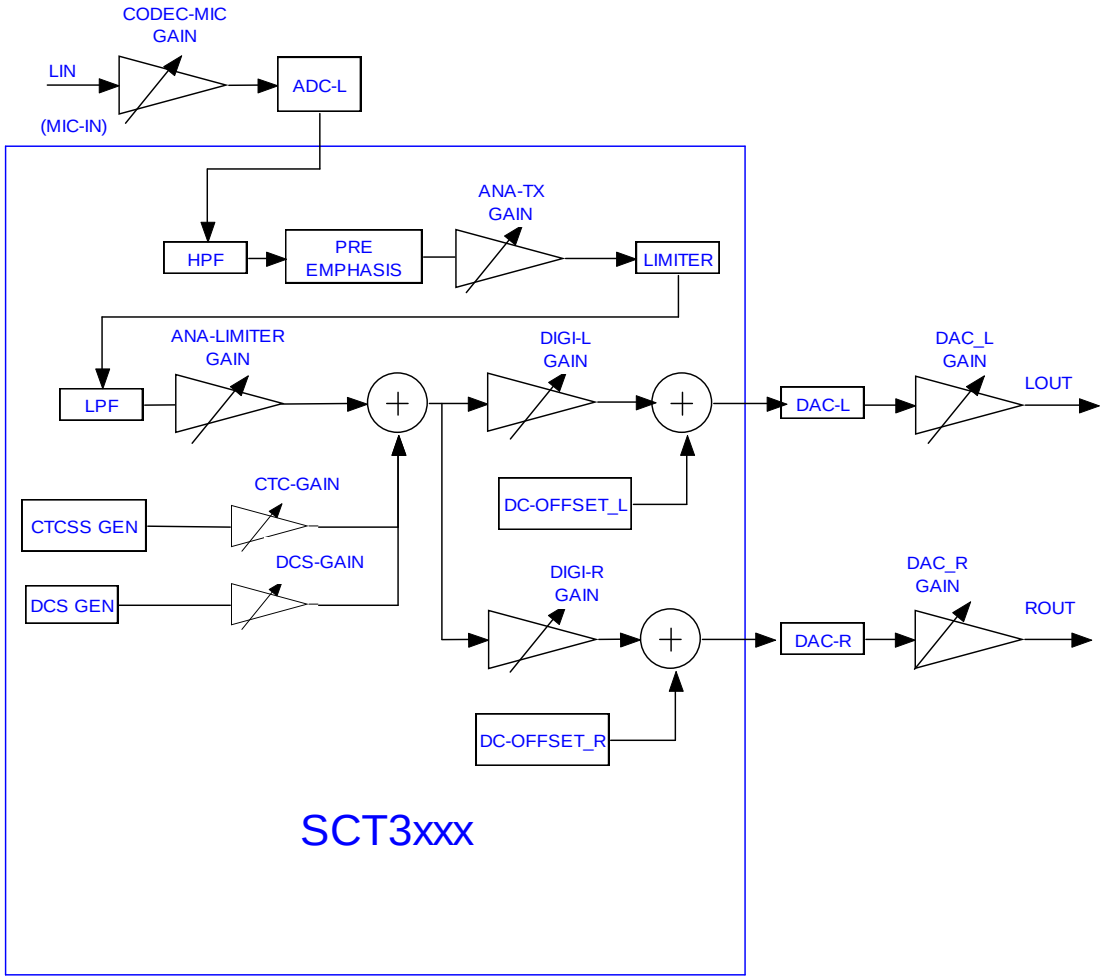


Figure 8-1 Signal Flow for Analog Transmitter

The microphone signals are amplified by the VGA (variable gain amplifier) of the codec, and converted into digital form by the external codec and store in the left input channel buffer of SCT3258. The following steps are applied to the digitized analog signals:

1. HPF, with pass band at 300 Hz, and stop band of 255 Hz.
2. Compressor
3. Pre-emphasis filter, with 6 dB/Octave
4. ANA_TX_GAIN, a gain block with linear 16 bit gain
5. Limiter for limiting the frequency deviation for large signals
6. LPF, with selectable corner of 2.55 kHz or 3kHz.
7. ANA_MOD_GAIN, a gain block with 16 bit gain after the limiter.

Beside the gain blocks, analog features that can be configured in the transmitter include:

1. BYPASS_FILTER: when enabled, all analog filters are by passed. A flat frequency response from 0-12 kHz results.
2. BYPASS_EMP: when enabled, pre-emphasis filter is by passed. A flat frequency response from 300 Hz to 2.55/3 kHz results.
3. CH_SEL: when enabled, the low pass corner is 3 kHz; when disabled, the low pass corner is 2.55 kHz.

The following table shows the composite frequency responses of channel filters based for different settings of BYPASS_FILTER, BYPASS_EMP and CH_SEL.

Frequencies (Hz)	BYPASS_ FILTER = 1 (in dB)	BYPASS_FILTER = 0 (in dB)			
		BYPASS_EMP = 0		BYPASS_EMP = 1	
		CH_SEL = 0	CH_SEL = 1	CH_SEL = 0	CH_SEL = 1
100	0.0	-49.6	-48.6	-46.3	-46.8
250	0.0	-49.6	-47.6	-49.3	-50.3
300	0.0	-10.0	-9.9	0.5	0.5
350	0.0	-8.8	-8.6	0.5	0.5
500	0.0	-5.6	-5.6	0.4	0.4
700	0.0	-2.9	-2.9	0.2	0.2
1000	0.0	0.0	0.0	0.0	0.0
1500	0.0	3.8	3.7	0.3	0.2
2000	-0.1	6.2	6.4	0.3	0.5
2500	0.0	8.1	8.0	0.4	0.2
3000	-0.1	-12.0	9.3	-21.2	0.0
3500	-0.1	-46.1	-21.4	-49.3	-31.3
6000	-0.2	-50.6	-47.6	-50.3	-49.3

Table 8-1 Frequency Response of the Analog Transmitter

An example of frequency response is also shown in the figure below.

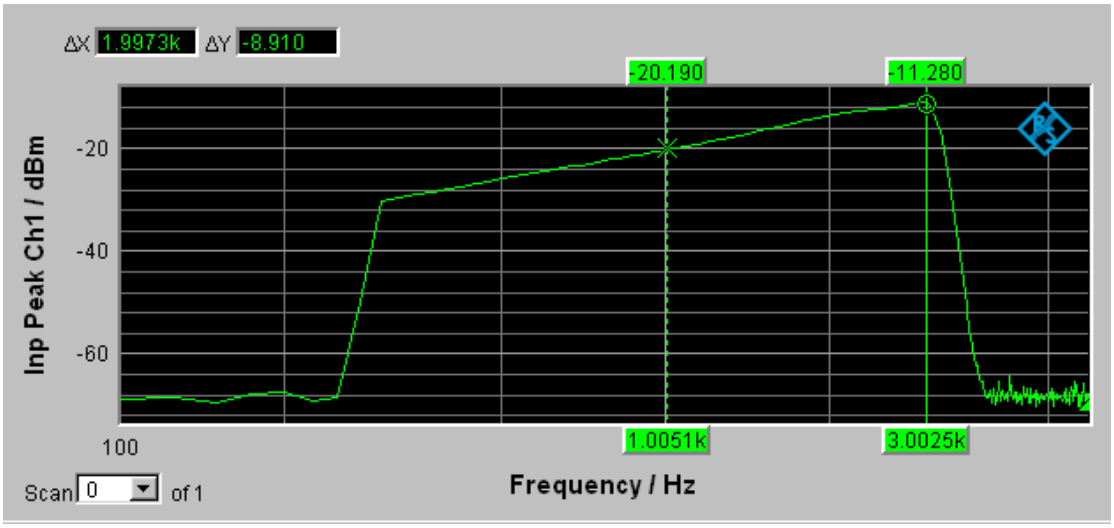


Figure 8-2 Frequency Response of the Transmitter with CH_SEL=0, BYPASS_EMP = 0, BYPASS_FILTER = 0

If CTCSS/DCS is enabled, the internally generated CTCSS/DCS signals are added to the voice signals. The amplitude of the CTCSS/DCS can be modified by CTC_GAIN or DCS_GAIN block.

The resulting signals are split into left channel and right channel signals for two point modulation.

Independent DC offsets and analog and digital gains are applied to the left and the right channels. The left channel control and the right channel control are identical, except that the left channel is multiplexed as speaker output in the RX mode. If DC coupling is used for TCXO control, the right channel is to be connected to VCTCXO input, while the left channel is connected to VCO. If AC coupling is used for VCTCXO control, either left or right channel can be connected to TCXO or VCO.

7.2 Signal Flow for Analog Receiver

The signal flow of the analog receiver is shown in the diagram below.

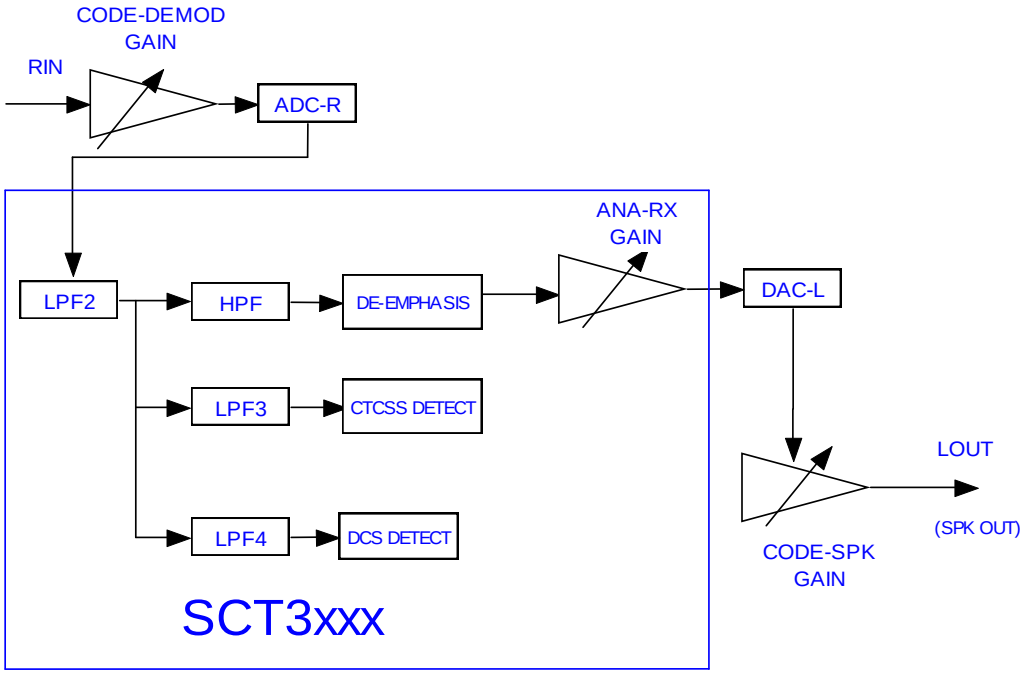


Figure 8-3 Signal Flow for Analog Receiver with FM Demodulated Signal Input

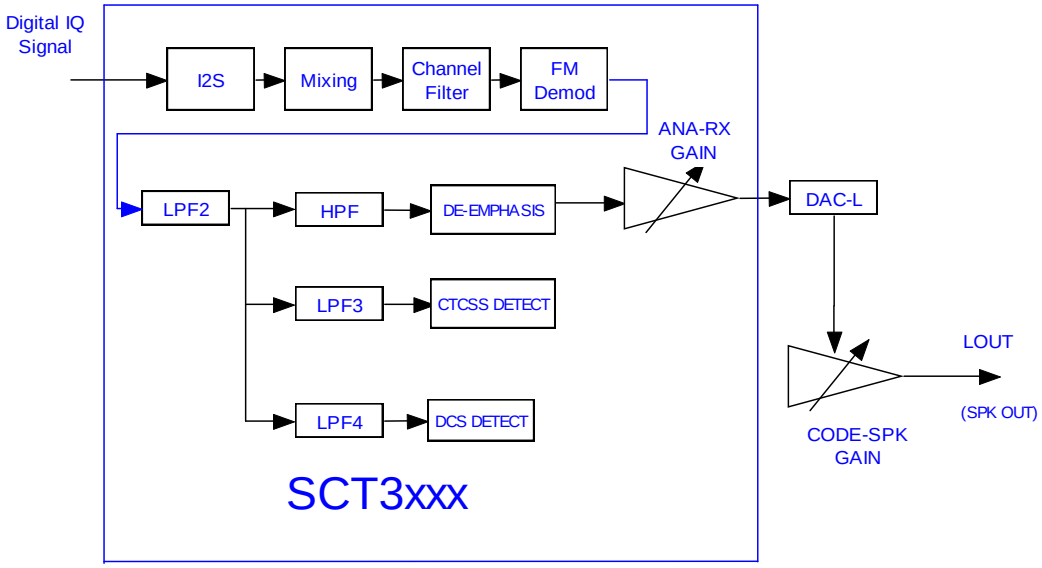


Figure 8-4 Signal Flow for Analog Receiver with IQ Signal Input

The FM demodulated signals are amplified by the VGA (variable gain amplifier) of the codec, and converted into digital form by the external codec and store in the right input channel buffer of SCT3258. The following steps are applied to the digitized analog signals:

1. LPF2, with low pass corner at 3000 Hz
2. HPF, with pass band at 300 Hz, and stop band of 255 Hz.
3. De-emphasis filter, with 6 dB/Octave
4. Expander
5. ANA_RX_GAIN, linear 16 bit gain

The filtered digital signals are converted into analog form by the external codec and then amplified by the DAC analog gain block CODEC_SPK_GAIN before feeding to the audio PA.

Beside the gain blocks, analog features that can be configured in the receiver include:
1. BYPASS_FILTER: when enabled, all analog filters are by passed. A flat frequency response from 0-12 kHz results.
2. BYPASS_EMP: when enabled, de-emphasis filter is by passed. A flat frequency response from 300 Hz to 2.55/3 kHz results.

The following table shows the composite frequency responses of channel filters based for different settings of BYPASS_EMP.

Frequencies (Hz)	BYPASS_ FILTER = 1 (in dB)	BYPASS_FILTER = 0 (in dB)	
		BYPASS_EMP = 0	BYPASS_EMP = 1
100	0.0	-39.9	-47.9
250	0.0	-53	-54.3
300	0.0	8.4	0.5
350	0.0	7.6	0.5
500	0.0	5.5	0.4
700	0.0	3.0	0.2
1000	0.0	0.0	0.0
1500	0.0	-3.2	0.2
2000	0.0	-5.4	0.5
2500	-0.1	-7.7	0.2
3000	-0.1	-9.6	0.0
3500	-0.3	-41.6	-31.6
6000	-0.4	-53.5	-54.3

Table 8-2 Frequency Response of the Analog Receiver

An example of frequency response is also shown in the figure below.

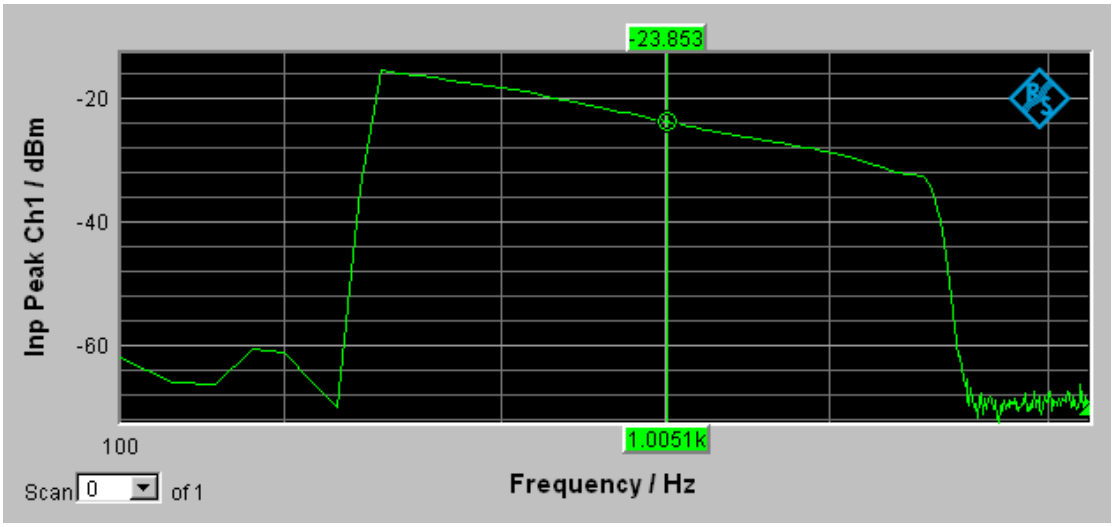


Figure 8-5 Frequency Response of the Transmitter with BYPASS_EMP=0, BYPASS_FILTER=0

Two additional low pass filters are applied to the output of LPF2 to extract CTCSS and DCS signals for detection. The detection results are reported to the MCU though HPI interface.

For the I/Q signal case, the I/Q signal can be from digital interface or through an ADC. Additional processing is requires, such as IQ mixing, channel selection filter and FM demodulation. The rest of the process is the same as the demodulated case.

10 Power Management

This section describes the power management features of the SCT3258.
The SCT3258 employs four levels of operations: normal, idle, sleep and halt mode. Table 10-3 summarizes the four modes. In addition, the HPI can be put to sleep separately.

Power level	Description
Normal	All units and clocks active
Idle	DSP device inactive, peripherals active. Any enabled interrupt, NMI, or reset wakes device. PLL retains lock.
Sleep	System clock and peripherals inactive. Any enabled external interrupt (INT0), NMI, or reset wakes device. PLL retains lock.
Halt	System clock and peripheral is inactive. Only NMI or reset wakes device. PLL retains lock.

Table 10-1 SCT3258 Power Levels

In normal mode and all power saving modes, PLL remains locked, which reduces the latency of returning to full-speed operation. While in any power saving modes, memory and register contents remain intact.

10.1.1 Normal Mode

In normal mode, the processor executes at full speed and all peripherals are active.

10.1.2 Idle Mode

In idle mode, the processor clock is halted, but the I/O clock continues to run. When an interrupt occurs and is serviced, execution begins with the next instruction following the idle instruction.

The host can set SCT3258 into IDLE mode by using HPI command CHIP_LOW_PWR, with Low Power Mode 4. To return to normal mode, the host can send command CHIP_LOW_PWR with Low Power Mode 0. Details can be found in “SCT3258 Packet Interface”.

10.1.3 Sleep Mode

In sleep mode, the processor clock and all I/O activity stop. After INT0 or NMI occurs and is serviced, execution resumes with the instruction following the Sleep instruction.

The host can set SCT3258 into SLEEP mode by using HPI command CHIP_LOW_PWR, with Low Power Mode 5. To return to normal mode, the host need to sends an external INT0 interrupt to SCT3258, and then sends command CHIP_LOW_PWR with Low Power Mode 0. Details can

be found in “SCT3258 Packet Interface”.

10.1.4 Halt Mode

In halt mode, the processor clock and all I/O activity stop. While halted, memory and register contents remain intact, but previous program execution cannot resume. If an NMI wakes up the device from halt mode, a full software reset of SCT3258 is performed without re-downloading the firmware.

The host can set SCT3258 into HALT mode by using HPI command CHIP_LOW_PWR, with Low Power Mode 6. Details can be found in “SCT3258 Packet Interface”.

13 Specifications

13.1 DC Characteristics

Table 13-1 lists the DC characteristics for the SCT3258.

Parameter	Symbol	V_{DD2}=1.2V, PLLVDD=1.2V, V_{DDIO}=2.5-3.3V	
		Minimum	Maximum
Input Voltage Low	V_{IL}	0V	0.8V
Input Voltage High (2.8V I/O Supply)	V_{IH}	2.0V	5.5V
Input Current	I_{IN}	-10uA	10uA
PLL Input Voltage Low	$VPLL_{IL}$	VSS	0.24V
PLL Input Voltage High	$VPLL_{IH}$	0.96V	VDD2
Output LOW Voltage @+2mA(LOW)	V_{OL}	—	0.4
Output High Voltage@-2mA	V_{OH}	2.4	—
Output 3-State Current Low	L_{OZL}	-10uA	10uA
Output 3-State Current High	L_{OZH}	-10uA	10uA

Table 13-1 DC Electrical Characteristics

13.2 Power Consumption

Table 13-2 lists the power dissipation characteristics of SCT3258. Sicomm recommends an I/O supply current rating of 200 mA or greater.

Work Mode	Frequency (MHz)	Power Voltage	Current Dissipation (Typical)
Full Duplex	110.592	1.2 V(Core)	37 mA
		3.3 V (IO)	5.3 mA
Half Duplex	61.44	1.2 V (Core)	22 mA
		3.3 V (IO)	3.3 mA
Idle	110.592	1.2 V (Core)	21 mA
		3.3 V (IO)	5.3 mA
	61.44	1.2 V (Core)	13 mA
		3.3 V (IO)	3.3 mA
	12.288	1.2 V (Core)	3.0 mA
		3.3 V (IO)	1.3 mA
Sleep/Halt	110.592	1.2 V (Core)	3.3 mA
		3.3 V (IO)	4.6 mA
	61.44	1.2 V (Core)	2.8 mA
		3.3 V (IO)	2.9 mA

	12.288	1.2 V (Core)	0.9 mA
		3.3 V (IO)	1.2 mA

Table 13-2 SCT3258 Power Dissipation

13.3 Recommended Operating Conditions

Table 13-3 lists the recommended operating conditions for SCT3258.

Parameter	Symbol	V_{DD2}=1.2V, PLLVDD=1.2V, V_{DDIO}=2.5-3.3V	
		Minimum	Maximum
Core Supply Voltage	V_{DD2}	1.1V	1.3V
PLL Supply Voltage	PLLVDD	1.1V	1.3V
I/O Supply Voltage	V_{DDIO}	2.5V	3.6V
Input Voltage	V_I	0V	V_{DDIO}
Output Voltage	V_O	0V	V_{DDIO}
CLKIN Input Voltage	Vclk	1.2 Vpp	V_{DDIO}
Ambient Temperature (Industrial Operating Conditions)	T_A	-40℃	85℃

Table 13-3 Recommended Operating Conditions

Table 13-4 lists ESD ratings for SCT3258.

CDM	HBM
500V	1000V

Table 13-4 ESD Ratings

13.4 Parametric Performance

All voltage levels given in the table below are given in relative to the full scale value of the ADC. The absolution voltage level can be calculated from the full scale voltage of the ADC. For example, with WM8758B, the full scale ADC voltage with 3.3v analog power supply is 3 Vpp. With Demod input value of -14.5 dBFS, the absolute value is around 560 mVpp.

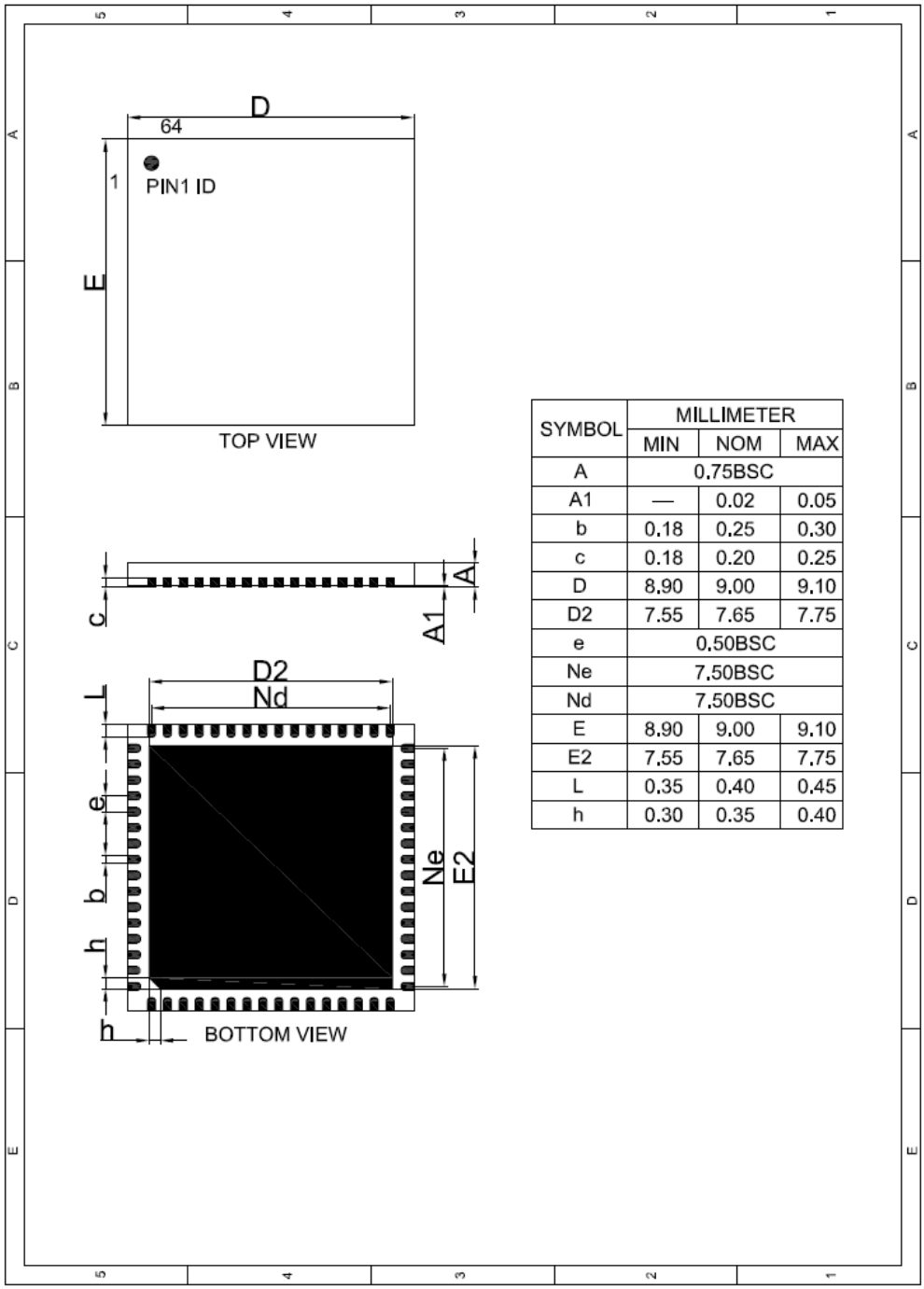
Parameters	Notes	Minimum	Typical	Maximum	Unit
Route Trip Delay	1		150		Ms
4FSK Input	2, 3,4	-60	-14.5	-1.5	dBFS
4FSK Input Auto calibration Range	2, 3	-37.5		-5.5	dBFS
4FSK Output for VCO	2, 5	-60	-14.5	-1.5	dBFS
4FSK Output for TCXO	2, 5	-60	-14.5	-1.5	dBFS

DPMR Call Match report time with Header Frame	6	75		120	milliseconds
DPMR Call Match report time with Late Entry Time	6	260		520	milliseconds
DPMR Sensitivity Gain over analog call	7		2	3	dB
DMR Call Match report time with FLC Data Frame	6		80		milliseconds
DMR Call Match report time with Late Entry Time	6	380		740	milliseconds
DMR Sensitivity Gain over analog call	7		2	3	dB

Table 13-5 Parametric Performance

1). Route trip delay includes algorithm delays (for vocoders) and buffer delays.
2). Obtained when +3, -3 symbols are transmitted or received,
3). When the analog and digital gain of the ADC are all set to 0 dB.
4). When the analog and digital gain of the ADC are all set to 0 dB. Auto calibration is enabled when DIGI_DEMOD_GAIN = 0;
5). When the analog and digital gain of the DAC are all set to 0 dB. Typical Value are obtained when MOD_GAIN=2048
6). Assume no bit error.
7). Assume 12.5 kHz channel spacing. 4FSK uses frequency deviation of 1944 Hz with +3,-3 symbol patterns. Analog sensitivity uses 12 dB SINAD. Digital Sensitivity uses 5% raw BER.

15 Packaging Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A		0.75BSC	
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	8.90	9.00	9.10
D2	7.55	7.65	7.75
e		0.50BSC	
Ne		7.50BSC	
Nd		7.50BSC	
E	8.90	9.00	9.10
E2	7.55	7.65	7.75
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Dimensions shown in millimeters

Figure 15-1 SCT3258 QFN64 Package

