SiFive Performance P400-Series

The **SiFive® Performance™** P400-Series is a family of 64-bit RISC-V ISA, three-issue, out-of-order, vector capable processors. This high-performance family has been carefully tuned to achieve a high level of throughput within a carefully balanced power envelope, ensuring best-in-class power and compute efficiency.

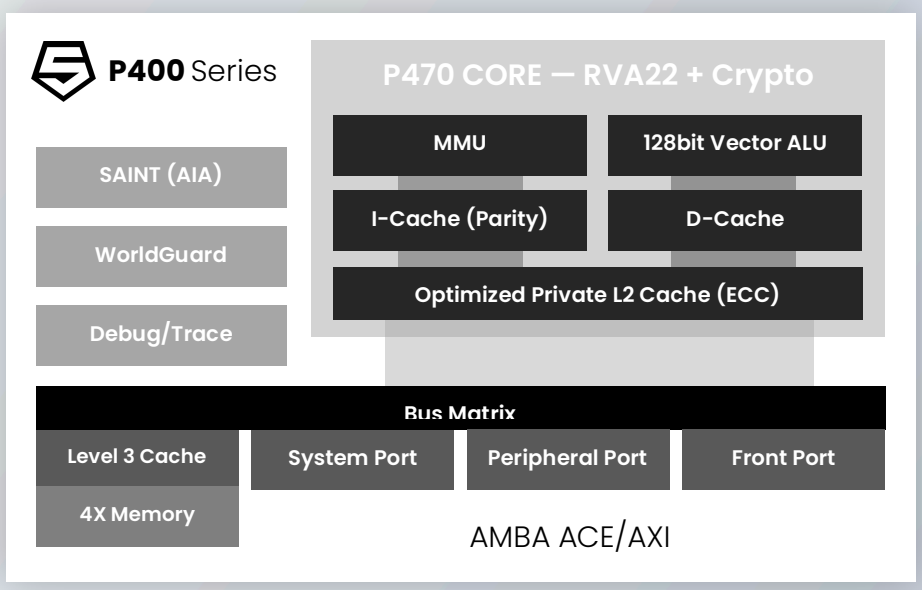
With a SPECInt2k6/GHz score of >8, the **SiFive® Performance™** P400-Series, multi-core, multi-cluster, fully coherent processors are designed for high levels of throughput for applications such as wearables and smart home consumer devices, where power efficiency is a key feature.

The SiFive Performance P470 and SiFive Performance P450 processors both offer an industry-leading feature set, incorporating the latest RISC-V technology extensions and standards including: virtualization, with a separate IOMMU offering for accelerating virtualized device IO, and a new advanced interrupt controller with better support for MSI style interrupts and virtualization.

The P470 also offers a fully integrated out-of-order enabled 128-bit RISC-V Vector ALU (compliant with the ratified RISC-V Vector 1.0 specification) along with the latest RISC-V Vector Cryptography extension. The P450 is optimized for compute-dense applications, as a smaller, area-efficient alternative for applications that do not require vector compute.

Building on the robust and comprehensive foundation of the silicon-proven SiFive Performance P550, the P400-series enhances the power efficiency capability with a feature set designed to offer the required design flexibility while targeting applications requiring a balanced performance-to-power efficiency ratio.

The P400-series was designed to also serve as a companion to the P600-series for demanding applications that require a sharing of compute resources while optimizing power consumption.



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SiFive Performance P400-Series Key Features

- 64-bit RISC-V ISA
- Three issue, out-of-order pipeline tuned for scalable performance
- Multi-core, multi-cluster processor configuration options, with up to 16 cores
- RISC-V Hypervisor Extension
- 128-bit RISC-V Vector ALU (compliant with the ratified RISC-V Vector 1.0 specification) (P470 only)
- RISC-V Vector Cryptography extension (P470 only)
- RVA22 Compliant
- Enhanced Power Management and Monitoring Interface
- RISC-V Advanced Interrupt Architecture (AIA) compliant interrupt controller
- Multi-layer caching support for optimum data movement
- Optional private Level 2 cache and stride prefetcher for improved memory performance
- Non-Inclusive, Level 3 cache architecture for improved performance density
    - Cache logic capable of higher frequencies with the ability to operate asynchronously to the cores
    - Slices (similar to banks) offer memory parallelism to provide cache miss tolerance
- Cache stashing to level 3 cache for tightly coupled accelerators
- High-performance memory subsystem
- Virtual memory support, with up to 57-bit addressing, with precise exceptions
- High performance, flexible connectivity to SoC peripherals
- WorldGuard system security
- SiFive Insight debug and trace

P470 RISC-V Vectors (RVV)

The RISC-V Vector (V) ISA standard extension enables processor cores based on the RISC-V instruction set architecture to process data arrays alongside traditional scalar operations, unifying vector and scalar capabilities into a single application processor. The P470 processor implements a 128-bit vector length (VLEN) architecture, fully supporting the RISC-V Vector extension standard, with dynamic variable vector length operations. The vector ALU and load/store architecture data width (DLEN) is 128-bits.

With RISC-V vectors, P470 offers:

- A single Vector ISA (ratified at version 1.0 by RISC-V International in 2021), which greatly simplifies software development across the full range of vector processors
- A vector-length-agnostic architecture, which allows library and application code investment to be reused across multiple generations and broad ranges of processor implementations
- Dynamic (runtime) modification of vector parameters for the most efficient computation on a processor, enabling better targeting for market application computation needs
- Support of LMUL (vector Length MULtiplier), the ability to concatenate multiple vector hardware computations for a single instruction, giving more efficient vector throughput with a smaller number of software instructions. P470 supports LMUL up to 8, thus a 1024-bit software vector length per vector ALU.
- Extensive range of vector data types and sizes supporting a wide range of application requirements

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Memory System and Caches

The P400-Series memory system has been tuned for high-performance workloads. The instruction memory system consists of a dedicated 16 or 32KB 4-way set-associative Level 1 instruction cache with a line size of 64 bytes. The data memory subsystem has a 2 or 4-way set-associative 16 or 32KB write-back Level 1 data cache that supports 64-byte cache lines.

The optional private Level 2 cache is a 128KB or 256KB 8-way set-associative cache, with a line size of 64 bytes, with two cache banks.

A flexible non-inclusive Level 3 cache can be configured to be either 256KB, 512KB, 1MB, 2MB, or 4MB, with multi-cluster options of 8MB, 16 MB, and 32 MB.

P400-Series Ports

For maximum flexibility in moving data in and out of the processor for general-purpose I/O or other more demanding system components like DMA, there are several ports within the bus matrix that are available. These ports provide connection interfaces to external system memories and peripherals and are shared across all processors in a multi-core, multi-cluster configuration.

Memory Port Up to 4 ports	Arm® AMBA® AXI4™ ACE4 128-bit, 256-bit	• High-performance port used for cached transactions • Connects cacheable region of memory for both data and instructions accesses • Supports up to 256 outstanding transfers per memory port
System Port 1 or 2 ports	AXI4 128-bit	• Used typically for high-bandwidth, uncached memory or devices
Peripheral Port 1 port	AXI4 64-bit	• Interface with lower speed peripherals • Supports code execution • Supports the RISC-V standard Atomic (A) extension
Front Port 1 or 2 ports	AXI4 128-bit, 256-bit	• External Initiators for accessing on Core Complex devices and ports • Transactions through the Front Port are coherent with Level 1 Data Caches

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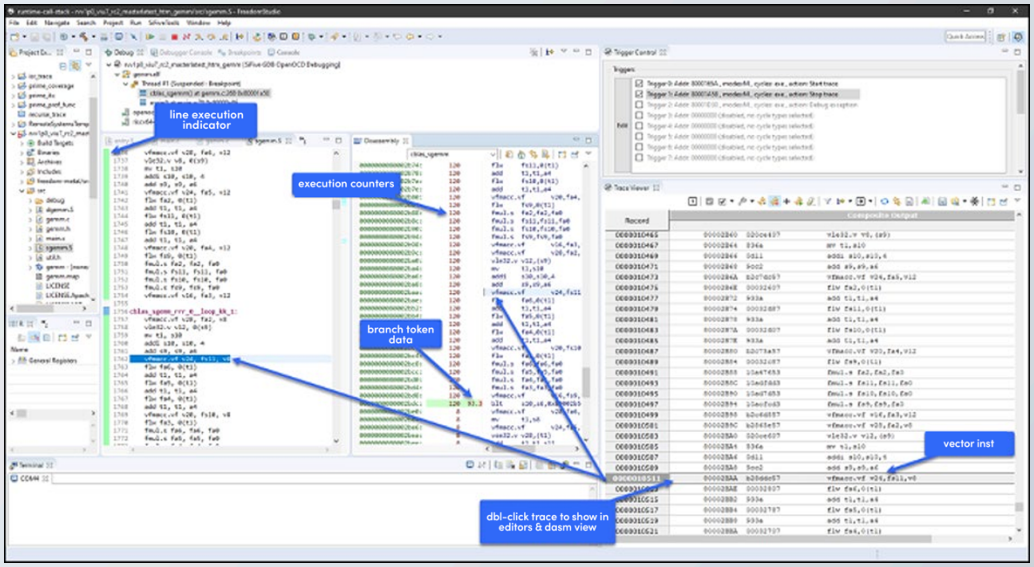
Advanced Software Development Capabilities

SiFive Freedom Studio, built on top of the popular Eclipse IDE, is the fastest way to get started with programming of your SiFive hardware. Freedom Studio is packaged with a pre-built tool suite, example projects, and includes comprehensive support for SiFive Insight Advanced Trace and Debug capabilities.

Multiple execution targets are supported by Freedom Studio, including simulation models and a variety of FPGA platforms, in addition to fully featured silicon-based development boards. Freedom Studio is supported on Windows, macOS, and Linux host computers.



Broad Application Coverage

The P400-Series enables greater innovation and flexibility in the broadest range of high-performance, power-efficient applications for wearables, consumer, and smart home:

Wearables

- Smartwatch
- Sport watch
- Fitness tracker

Consumer

- Digital imaging
- Feature phone
- Security camera
- AR, VR, MR

Smart Home

- Smart doorbell
- Smart home assistant
- Smart thermostat
- Smart TV / Set Top Box

For more information contact SiFive at **www.sifive.com/contact-sales**