TPS63810 2.5-A Buck-Boost Converter with I²C Interface

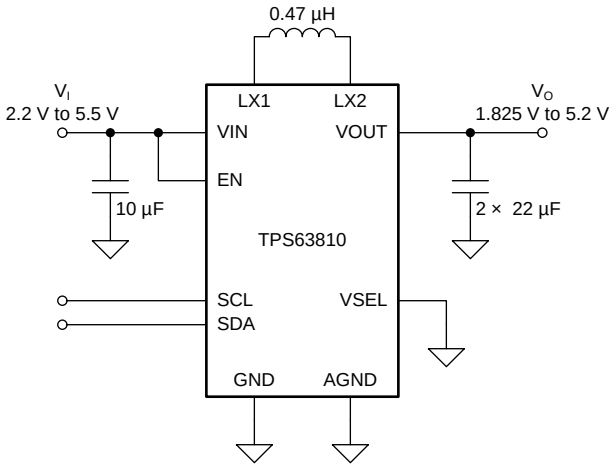
1 Features

- Input voltage range: 2.2 V to 5.5 V
- Output voltage range:
  - 1.825 V to 5.2 V
- Output current:
  - Up to 2.5 A for $V_I \geq 2.5$ V, $V_O = 3.3$ V
  - Up to 2.5 A for $V_I \geq 2.8$ V, $V_O = 3.5$ V
  - Up to 2 A for $V_I \geq 2.5$ V, $V_O = 3.5$ V
- Typical efficiency >90% for I_O = 1 mA to 2 A
  - Typical supply current of 11 µA
  - Power-save mode (user-selectable)
- Real buck, boost and buck-boost operation with automatic mode transition
- I²C Interface (up to 1 MHz)
- Robust operation:
  - Soft-start
  - Input overvoltage
  - Output overcurrent
  - Thermal shutdown
  - True shutdown function with load disconnect and active output discharge
- 15-ball, 0.4-mm pitch DSBGA package

2 Applications

- Smartphones and tablets
  - Preregulators and USB VCONN supplies
- TWS earbud chargers
- General-purpose point-of-load regulators

Simplified Schematic



3 Description

The TPS63810 device is an I²C programmable buck-boost converter intended primarily for applications supplied from a single-cell Li-Ion battery. It uses a novel control scheme with three distinct operating modes: buck, boost and buck-boost. Compared with traditional average-current control schemes, the TPS63810 device has a more predictable behavior during buck-boost operation.

With a quiescent current of only 11 µA, the TPS63810 device achieves efficiencies greater than 90% for output currents from 1 mA to 2 A. It also has a fast dynamic response, which enables it to maintain tight regulation of the output voltage even in the presence of load transients.

Two VOUT registers set the output voltage, and a VSEL pin selects which output voltage register is active. Thus the device can support dynamic voltage scaling; for example, to support applications with low-power and high-power modes of operation. When the logic level on the VSEL pin changes, the TPS63810 device ramps linearly to the new output voltage setting.

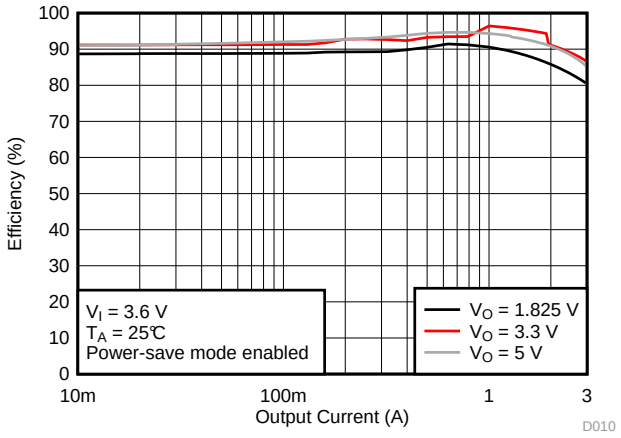
The TPS63810 device requires only five external components and can be implemented with an active PCB area of only 39 mm².

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS63810	DSBGA (15)	2.3 mm × 1.4 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Efficiency vs Output Current



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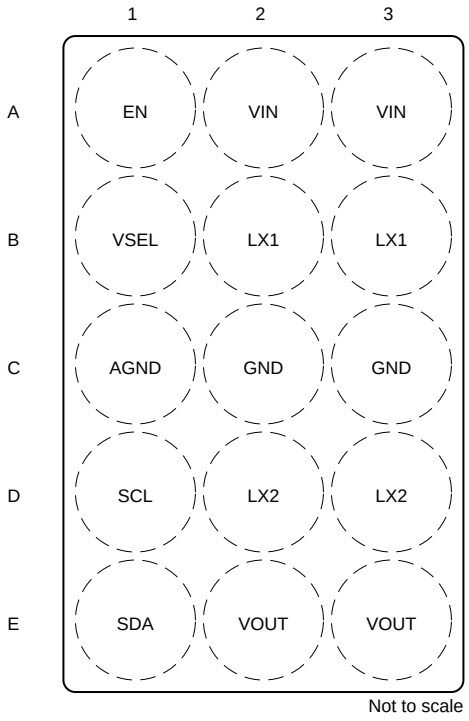
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2019	*	Initial release

5 Pin Configuration and Functions

YFF Package
15-Ball DSBGA
Top View



Not to scale

BGA Package (YFF) Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	EN	I	Device enable. A high logic level on this pin enables the device; a low logic level on this pin disables the device.
A2	VIN	—	Supply voltage for power stage
A3	VIN	—	Supply voltage for power stage
B1	VSEL	I	This pin selects which VOUT register is active. When a low logic level is applied to this pin the VOUT1 register sets the output voltage. When a high logic level is applied to this pin the VOUT2 register sets the output voltage.
B2	LX1	—	Inductor connection
B3	LX1	—	Inductor connection
C1	AGND	—	Analog ground
C2	GND	—	Power ground
C3	GND	—	Power ground
D1	SCL	I/O	I^2C serial interface clock. Pull this pin up to the I^2C bus voltage with a resistor or a current source.
D2	LX2	—	Inductor connection
D3	LX2	—	Inductor connection
E1	SDA	I/O	I^2C serial interface data. Pull this pin up to the I^2C bus voltage with a resistor or a current source.
E2	VOUT	—	Converter output
E3	VOUT	—	Converter output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage (VIN, L1, L2, VOUT, SCL, SDA, EN, VSEL)(2)	–0.3	6	V
	Input voltage for less than 10 ns (L1, L2)(2)	–3	9	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		2.2		5.5	V
V_O	Output voltage		1.825		5	V
V_{IH}	High-level input voltage	SCL, SDA, VSEL	1.3		V_I	V
V_{IL}	Low-level input voltage	SCL, SDA, VSEL	0		0.3	V
V_I	Input voltage	EN	0		V_I	V
I_O	Output current(1)	V_O = 3.3 V, V_I ≥ 2.5 V			2.5	A
		V_O = 3.5 V, V_I ≥ 2.5 V			2	A
		V_O = 3.5 V, V_I ≥ 2.8 V			2.5	A
C_I	Input capacitance(2)	V_I = 2.5 V to 5 V, V_O = 3.3 V, I_O = 2.5 A	5			µF
C_O	Output capacitance(2)	V_I = 2.5 V to 5 V, V_O = 3.3 V, I_O = 2.5 A	16			µF
L	Inductance		390	470	560	nH
T_A	Operating free-air temperature range		–40		85	°C
T_J	Operating junction temperature range		–40		125	°C

(1) The device can sustain the maximum recommended output current only for short durations before its junction temperature gets too hot. Users must verify that the thermal performance of the end application can support the maximum output current.
(2) Effective capacitance after DC bias effects have been considered.

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6.4 Thermal Information

THERMAL METRIC(1)		TPS63810 YFF (DSBGA) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report SPRA953

6.5 Electrical Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 3.3 V and T_J = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
	Supply current into VIN		V_I = 3.6 V, V_O = 3.3 V, $V_{(EN)}$ = 3.6 V, not switching T_J = 25°C		11		µA
	Shutdown current into VIN		V_I = 3.6 V, V_O = 0 V, $V_{(EN)}$ = 0 V T_J = 25°C		0.35		µA
V_{IT+}	Positive-going UVLO threshold voltage			2.00	2.10	2.20	V
V_{IT-}	Negative-going UVLO threshold voltage			1.80	1.90	1.98	V
V_{hys}	UVLO threshold voltage hysteresis				200		mV
I/O SIGNALS							
V_{IT+}	Positive-going input threshold voltage	SCL, SDA, VSEL				1.2	V
		EN		1.07	1.10	1.13	
V_{IT-}	Negative-going input threshold voltage	SCL, SDA, VSEL		0.4			V
		EN		0.97	1.00	1.03	
V_{hys}	Hysteresis voltage	EN		40			mV
I_{IH}	High-level input current	SCL, SDA, VSEL	$V_{(SCL)}$ = $V_{(SDA)}$ = $V_{(VSEL)}$ = 1.8 V, no pullup resistor		±0.01	±0.1	µA
I_{IL}	Low-level input current	SCL, SDA, VSEL	$V_{(SCL)}$ = $V_{(SDA)}$ = $V_{(VSEL)}$ = 0 V, no pullup resistor		±0.01	±0.1	µA
I_{IB}	Input bias current	EN	$V_{(EN)}$ = 0 V to 5.5 V		±0.01	±0.1	µA
POWER STAGE							
	Output voltage range			1.825		5.000	V
	Output voltage accuracy		PWM operation	–1.5		1.5	%
			PSM operation (OOA = 0)	–1.5		3.5	%
			PSM operation (OOA = 1)	–1.5		3.5	%
	Default output voltage		VSEL = low		3.30		V
			VSEL = high		3.45		
	Switch current limit		V_I = 2.5 V, V_O = 3.3 V, boost operation, output sourcing current	5.2		6.5	A
			V_I = 3.6 V, V_O = 3.3 V, buck operation, output sourcing current	3.8	4.3	5.2	
			V_I = 3.6 V, V_O = 3.3 V, reverse-boost operation, output sinking current	0.35		1.3	
$I_{T-(PSM)}$	PSM entry threshold (peak) current				0.7		A
	Output discharge resistance		V_O = 3.5 V		23		Ω
V_{T+}	Positive-going power-good threshold voltage				95		%

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Electrical Characteristics (continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 3.3 V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{T-}	Negative-going power-good threshold voltage			90		%
	Positive-going input overvoltage threshold		5.5	5.7	5.8	V
I2C INTERFACE						
	7-Bit slave address			75h		
THERMAL SHUTDOWN						
	Thermal shutdown threshold temperature	T_J rising		150		°C
	Thermal shutdown hysteresis			20		°C

6.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus	0		1000	
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
$t_{SU:STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{HD:STA}$	Hold time (repeated) START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{SU:DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
		Fast mode plus	50			
$t_{HD:DAT}$	Data hold time	Standard mode	0			µs
		Fast mode	0			
		Fast mode plus	0			
t_r	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus			120	
t_f	Fall time of both SDA and SCL signals	Standard mode			300	ns
		Fast mode	$20\times V_{DD}/5.5$		300	
		Fast mode plus	$20\times V_{DD}/5.5$		120	
$t_{su:STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{VD;DAT}$	Data valid time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus			0.45	

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Timing Requirements (continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VD;ACK}$	Data valid acknowledge time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus			0.45	
C_b	Capacitive load for each bus line	Standard mode			400	
		Fast mode			400	
		Fast mode plus			550	
$t_{w(VSEL)}$	VSEL pulse duration	VSEL = high or low	5			µs

6.7 Switching Characteristics

Over operating junction temperature range and recommended input voltage range (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 3.3 V, and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of the output voltage ramp	T_J = 25°C, V_I = 3.6 V		229	440	µs
$t_{d(PG)}$	Power-good delay	V_O falling		50		µs
SR	Slew rate of internal ramp during dynamic voltage scaling	SLEW = 00b, forced-PWM operation		±1		V/ms
		SLEW = 01b, forced-PWM operation		±2.5		
		SLEW = 10b, forced-PWM operation		±5		
		SLEW = 11b, forced-PWM operation		±10		
	Switching frequency	PWM operation, I_O = 100 mA	0.5		3.1	MHz
$t_{d(VSEL)}$	Delay between rising edge of VSEL and start of DVS ramp	Measured from rising edge of VSEL to start of ramp.			5	µs

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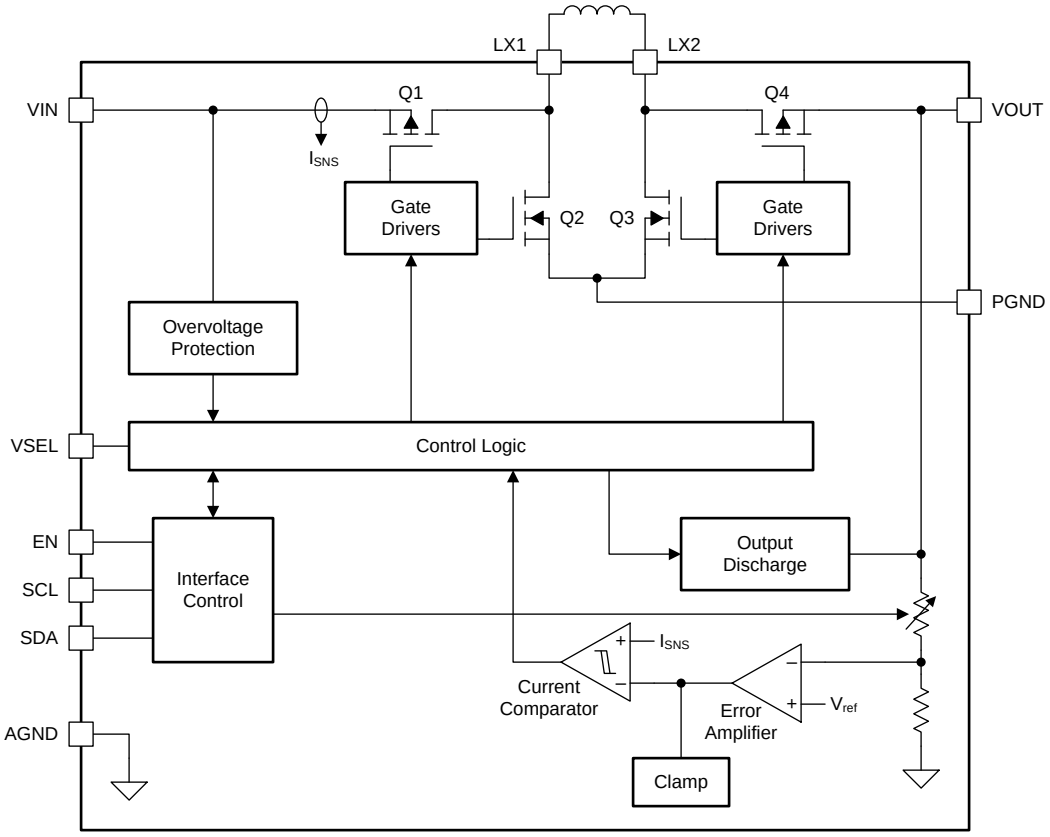
7 Detailed Description

7.1 Overview

The TPS63810 device is a high-efficiency buck-boost converter. The device uses four switches to maintain synchronous power conversion under all operating conditions, so that it achieves high efficiency power conversion over a wide range of input voltages and output currents. The device automatically switches between buck, boost and buck-boost operation as required by the operating conditions. The device operates as a true buck converter when $V_I > V_O$ and as a true boost converter when $V_I < V_O$. When $V_I \approx V_O$, the device operates in a 4-cycle buck-boost mode. The RMS current through the switches and the inductor is thus kept to a minimum, to minimize switching and conduction losses. Controlling the switches this way lets the converter to achieve high efficiency over the whole input voltage range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Scheme

The device automatically selects the best switching scheme for the operating conditions. To make sure of stable operation, the selection logic includes hysteresis (see Figure 1).

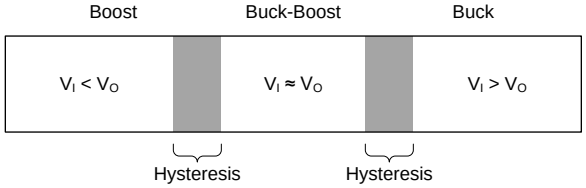


Figure 1. Switching Scheme Selection

Feature Description (continued)

7.3.1.1 Buck Operation

When $V_I > V_O$, the device switches like a buck converter: Q1 is the switch, Q2 is the rectifier, Q3 is permanently off, and Q4 is permanently on (see Figure 2). During buck operation, one switching cycle comprises two phases: on–off.

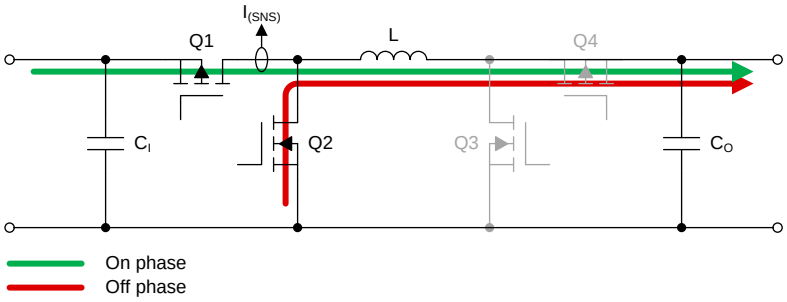


Figure 2. Buck Switch Configuration

7.3.1.2 Boost Operation

When $V_I < V_O$, the device switches like a boost converter: Q1 is permanently on, Q2 is permanently off, Q3 is the switch, and Q4 is the rectifier (see Figure 3). During boost operation, one switching cycle comprises two phases: on–off.

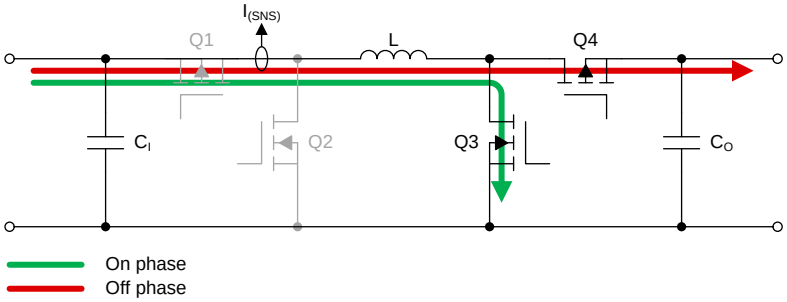


Figure 3. Boost Switch Configuration

7.3.1.3 Buck-Boost Operation

When $V_I \approx V_O$, all four transistors switch continuously (see Figure 4). During buck-boost operation, one switching cycle comprises four phases: on–commutate–off–commutate.

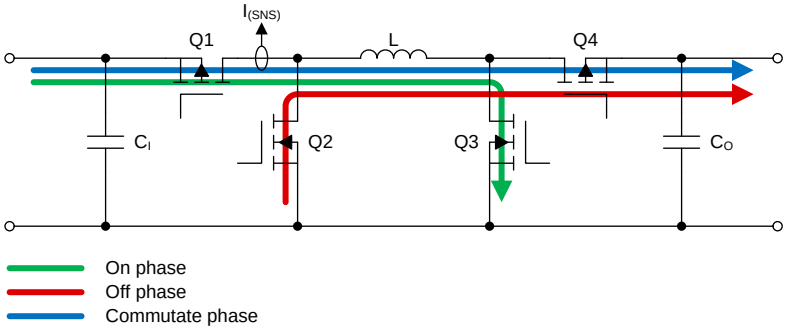


Figure 4. Buck-Boost Switch Configuration

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Feature Description (continued)

7.3.2 Control Scheme

The device uses a constant-off-time, peak-current-mode control scheme, in which an outer voltage control loop generates the demand signal for an inner current control loop. During the on time, the inner current control loop monitors the inductor current, and when the inductor current equals the demand signal from the error amplifier the on time stops and the next part of the switching cycle starts.

The off time is a function of V_I and V_O and the operating mode (buck, boost or buck-boost) of the converter.

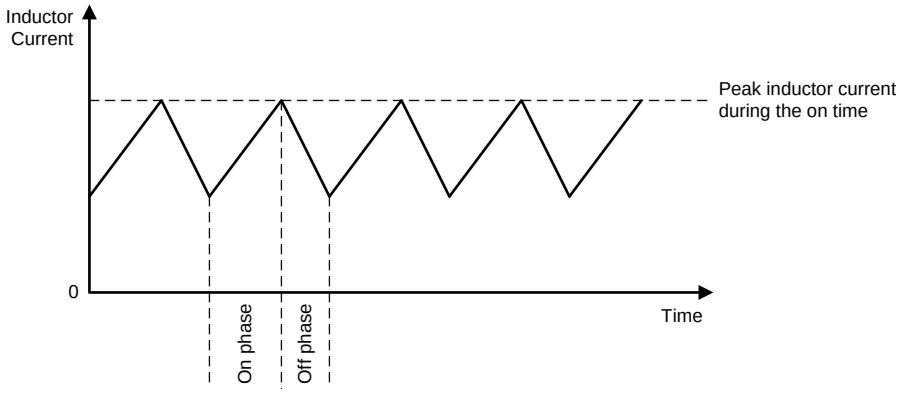

Figure 5. Peak Current Control (Buck and Boost Operation)

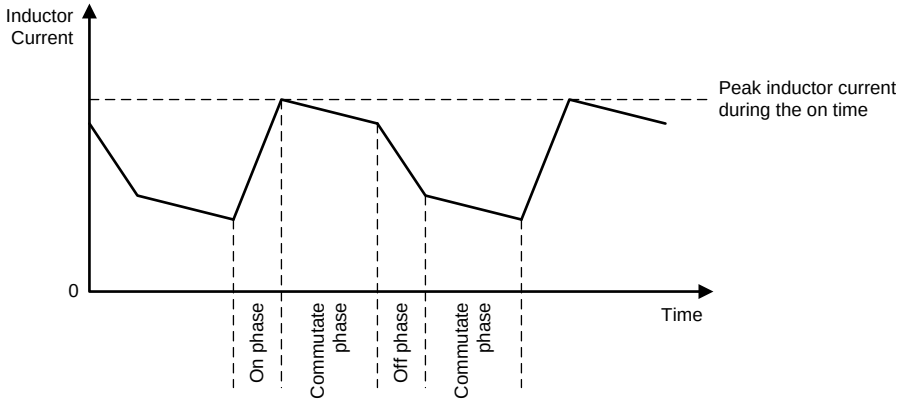

Figure 6. Peak Current Control – Buck-Boost Operation with $V_I < V_O$

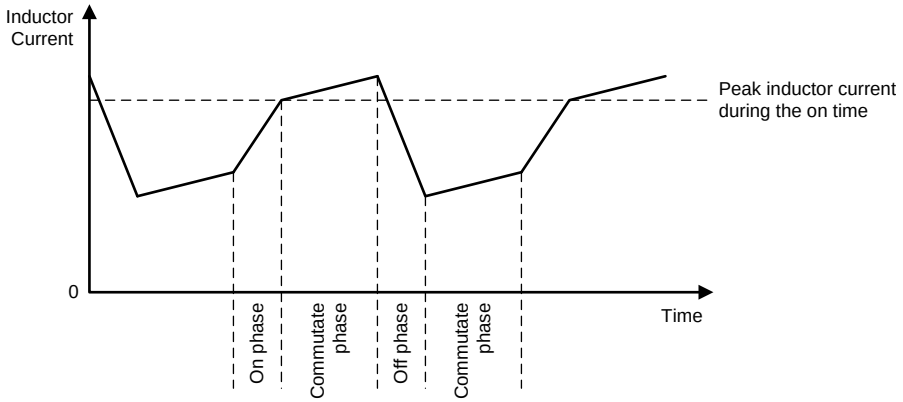

Figure 7. Peak Current Control – Buck-Boost Operation with $V_I > V_O$

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Feature Description (continued)

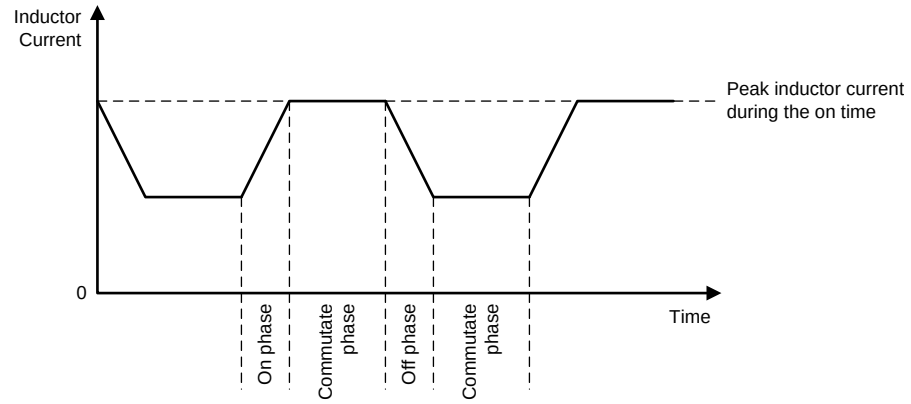

Figure 8. Peak Current Control – Buck-Boost Operation, with $V_I = V_O$

During PWM operation, current can flow in the reverse direction (from output to input). In this case, the error amplifier provides a negative peak current target. Note that the average reverse current is greater (more negative) than the peak current (see Figure 9 and Figure 10).

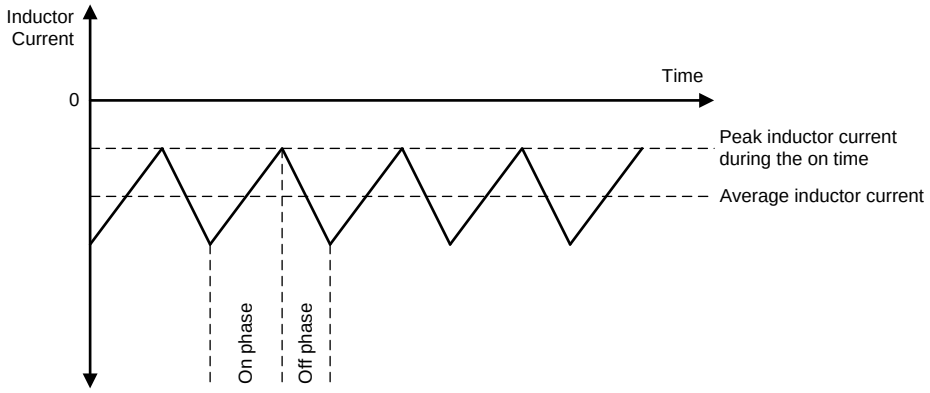

Figure 9. Reverse Peak Current Control – Buck and Boost Operation

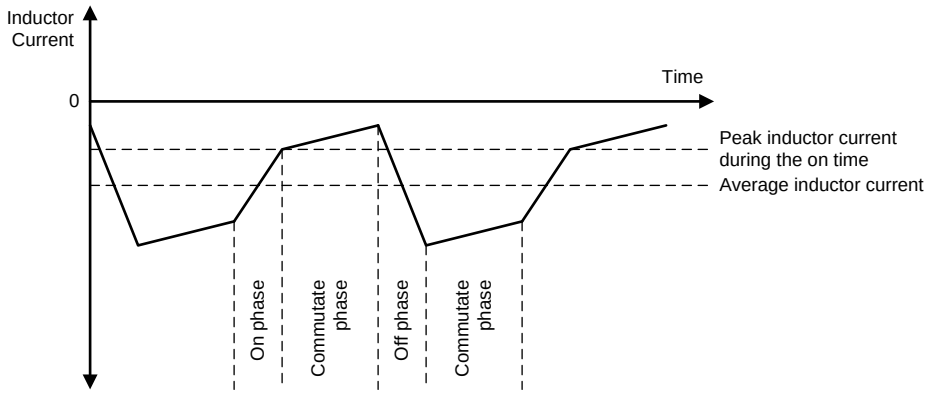

Figure 10. Reverse Peak Current Control – Buck-Boost Operation, with $V_I > V_O$

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Feature Description (continued)

7.3.3 Power-Save Mode Operation

To increase efficiency across a wide range of operating conditions, the device automatically changes from pulse-width modulation (PWM) at medium and high output currents to pulse-frequency modulation (PFM) at low output currents.

- During PWM operation, the devices switch continuously and adjust the duty cycle of each switching cycle to regulate the output voltage.
- During PFM operation, the device switches in bursts of a few switching cycles, separated by periods when the device does not switch (see Figure 11). PFM operation increases efficiency at low output currents, because when the device does not switch there are no switching losses and most of the internal circuitry is disabled, which reduces quiescent power consumption. A comparator with hysteresis compares the output voltage of the error amplifier to a predefined PFM threshold voltage. When the output voltage of the error amplifier is greater than the burst threshold voltage, the device starts switching. When the output voltage of the error amplifier is less than the burst threshold voltage, the device stops switching. This scheme automatically adjusts the frequency and the duration of the switching bursts to regulate the output voltage. During PFM operation the output voltage ripple can be higher and the transient response not as good as during PWM operation (see Table 1).

To enable power-save mode, clear the FPWM bit in the Control register to 0.

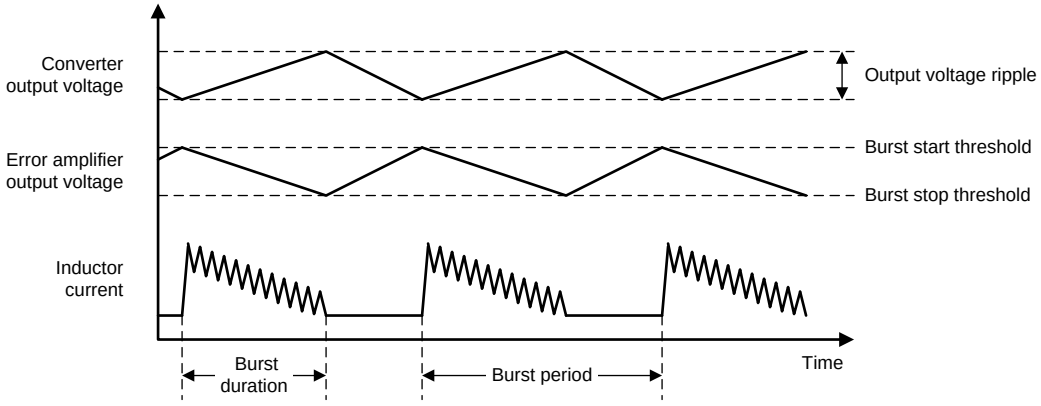

Figure 11. Pulse-Frequency Modulation

Table 1. Forced-PWM vs Power-Save Mode Performance Comparison

PERFORMANCE PARAMETER	BEST OPERATING MODE
Low-power efficiency	Power-Save Mode
Medium- and high-power efficiency	No difference
DC Output voltage accuracy	Forced-PWM
Transient response	Forced-PWM
Output voltage ripple	Forced-PWM

7.3.4 Forced-PWM Operation

NOTE

Some of the early pre-production samples (XPS63810) have a bug which can prevent correct Forced-PWM operation. We recommend that you do not operate XPS63810 devices with Forced-PWM enabled—see TPS63810 EVM User Guide for more details.

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During forced-PWM operation, the device uses PWM for all operating conditions. Forced-PWM operation has lower output voltage ripple and better transient response than power-save mode operation but lower efficiency at low output currents (see Table 1).

Note that the device inhibits forced-PWM operation during start-up (that is, until the converter output has reached power-good for the first time).

To enable forced-PWM operation, set the FPWM bit in the Control register to 1.

7.3.5 Ramp-PWM Operation

NOTE

Some of the early pre-production samples (XPS63810) have a bug which can prevent correct Ramp-PWM operation. We recommend that you do not operate XPS63810 devices with Ramp-PWM enabled—see TPS63810 EVM User Guide for more details.

If Ramp-PWM operation is enabled, the device operates in forced-PWM when it ramps from one output voltage to another during dynamic voltage scaling. This function is useful if you want the device to operate in power-save mode but you want to make sure that dynamic voltage scaling ramps the output voltage up and down in a controlled way. If the device operates in power-save mode and Ramp-PWM is disabled, the devices cannot always control the ramp from a higher output voltage to a lower output voltage, because in power-save mode the devices cannot sink current (see Figure 12).

To enable Ramp-PWM operation, set the RAMP bit in the Control register to 1. To disable Ramp-PWM operation, clear the RAMP bit in the Control register to 0.

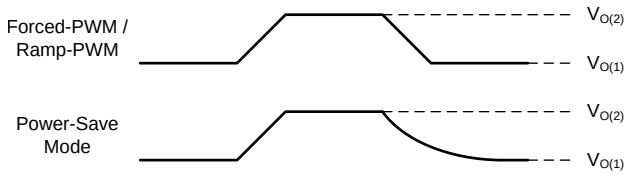


Figure 12. Ramp-PWM Operation

7.3.6 Device Enable (EN)

The EN pin enables and disables the device.

- When the EN pin is high, the device is enabled
- When the EN pin is low, the device is disabled

You can also use the ENABLE bit in the Control register to enable and disable the output of the converter (see *Register Map*).

7.3.7 Undervoltage Lockout (UVLO)

The device has an undervoltage lockout function that disables the device when the supply voltage is too low for correct operation.

7.3.8 Soft Start

To minimize inrush current and output voltage overshoot during start-up, the device has a soft-start function. At turn on, the switch current limit ramps gradually to its maximum value and the device starts up in a controlled way. The gradual increase of the current limit generates the smallest inrush current for no-load conditions. It is also possible to start into a high load as long as the load does not exceed the device current limit.

The rise time of the output voltage changes with the application circuit and the operating conditions. The output voltage rise time increases if

- The output capacitance is large
- The load current is large
- The device operates in boost mode

See *Application and Implementation* for output voltage rise times in a typical application.

ADVANCE INFORMATION

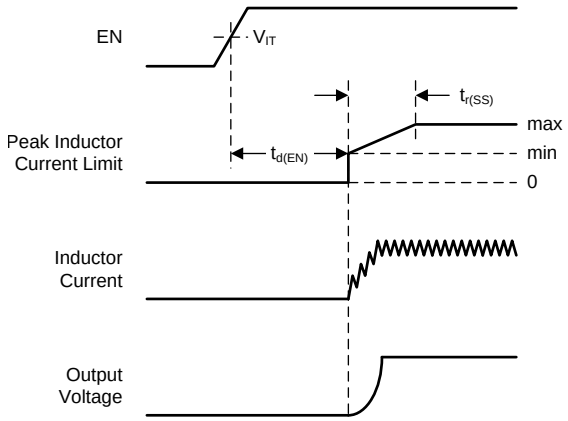


Figure 13. Device Start-Up

7.3.9 Output Voltage Control

The device can generate output voltages from 1.825 V to 5 V with a resolution of 25 mV:

- V_O = (VOUT[6:0] × 0.025) + 1.825 V

where VOUT[6:0] is the 7-bit value in the VOUT1 register or VOUT2 register, whichever is active.

The VSEL pin selects which VOUT register is active:

- When VSEL = low, the VOUT1 register sets the output voltage
- When VSEL = high, the VOUT2 register sets the output voltage

NOTE

To prevent output voltage transients, we recommend that you do not change the output voltage range while the converter is in operation. Instead, clear the ENABLE bit in the Control register to 0 to disable the DC/DC converter before you change the RANGE bit.

7.3.9.1 Dynamic Voltage Scaling

The device has a dynamic voltage scaling (DVS) function which lets you change the output voltage in a controlled way during operation. Figure 14 shows a simplified block diagram of the DVS function. The VSEL pin controls a multiplexer which selects either the VOUT1 register or the VOUT2 register to control the set voltage. The ramp control block detects when the target output voltage is different from the actual output voltage and ramps the output voltage to the target voltage in 25-mV steps. You can use the 2-bit SLEW parameter in the Control register to select one of four slew rates from 0.5 V/ms to 10 V/ms.

The device starts a DVS ramp when you change the logic level on the VSEL pin or program a new value in the active VOUT register.

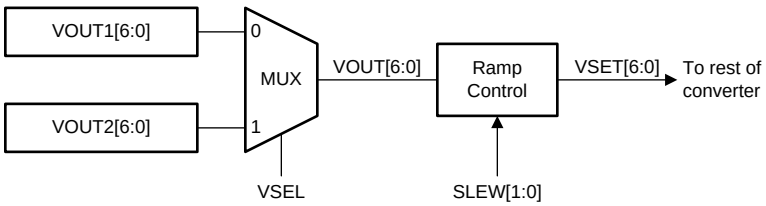
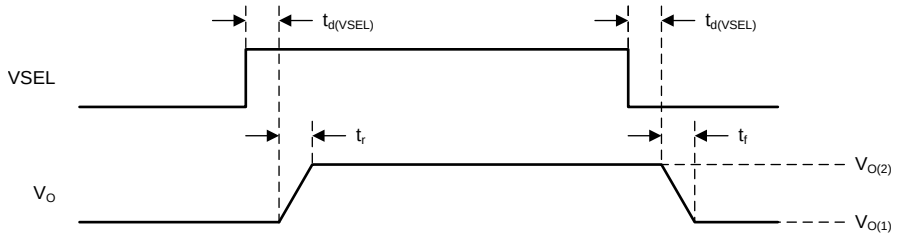


Figure 14. Dynamic Voltage Scaling Block Diagram

ADVANCE INFORMATION

Note that if you change the contents of the active VOUT register or change the state of the VSEL pin during start-up (that is, before the end of the soft-start), the converter uses the new value immediately and does not ramp gradually to the final value.

Figure 15 shows the timing diagram when you use the VSEL pin to change between the output voltage values in the VOUT1 and VOUT2 registers.



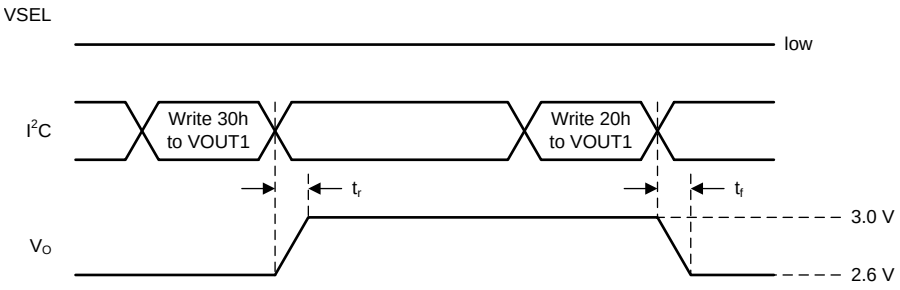
$$t_r = t_f = \frac{|V_{O(1)} - V_{O(2)}|}{SR}$$

Where

- $V_{O(1)}$ is the output voltage set by the VOUT1 register
- $V_{O(2)}$ is the output voltage set by the VOUT2 register
- SR is the slew rate set by the SLEW bits in the CONTROL register

Figure 15. DVS Timing Diagram Using the VSEL Pin

Figure 16 shows the timing diagram when you use the I^2C interface to change the output voltage value in one of the VOUT registers.



$$t_r = t_f = \frac{|3.0 - 2.6|}{SR}$$

Where SR is the slew rate set by the SLEW bits in the CONTROL register.

Figure 16. DVS Timing Using the I^2C Interface

7.3.10 Protection Functions

7.3.10.1 Input Voltage Protection (IVP)

Under certain operating conditions current can flow from the output of the device to the input. For example, this can occur during dynamic voltage scaling when the output ramps down to a lower voltage and the VOUT pin sinks current from the output capacitor. Under such conditions, if the voltage source supplying the device cannot sink current, the voltage on the VIN pin can rise uncontrollably.

To make sure the input voltage stays within the permitted range, the device stops switching if the voltage on the VIN pin is greater than 5.7 V. The device automatically starts to switch again when the voltage on the VIN pin is less than 5.7 V.

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The device sets the $\overline{PG}$ bit in the Status register when an input overvoltage event occurs. The device clears the $\overline{PG}$ bit is cleared if the Status register is read when the power-not-good condition no longer exists.

7.3.10.2 Current Limit Mode and Overcurrent Protection

The device has a clamp circuit which limits the peak inductor current in the event of an overload. The exact value of the output current during an overload changes with the operating conditions (V_I and V_O) and the switching mode (buck, buck-boost or boost) – see Figure 45.

Overloads increase the power dissipation in the device, which increases its temperature. If the device becomes too hot, the thermal shutdown function turns off the converter. When the device cools down, the thermal shutdown function automatically turns on the converter again. Thus, under a permanent overload condition, the device can periodically turn on and off, as it cools down and then heats up.

7.3.10.3 Thermal Shutdown

The device has a thermal shutdown function which turns off the converter if the junction temperature is greater than 150°C. The device automatically turns on the converter again when the junction temperature is less than 130°C. You can still use the I^2C interface to read and write to the registers when the device is in an over-temperature condition.

When the device detects an over-temperature condition, it sets the TSD bit in the Status register to 1. The device clears the TSD bit to 0 if you read the Status register when the junction temperature of the device is less than 130°C.

7.3.11 Power Good

The device has a power-good function which indicates if the output of the DC/DC converter is in regulation or not. The device detects a power-good condition when the output voltage is greater than 95% of its nominal value, and detects a power-not-good condition when the output voltage is less than 90% of its nominal value.

When a power-not-good condition occurs, the device sets the $\overline{PG}$ bit in the Status register to 1. The device clears the $\overline{PG}$ bit to 0 if you read the Status register when a power-good condition exists.

7.3.12 Load Disconnect

During device shutdown, the input is disconnected from the output. This prevents any current flow from the output to the input or from the input to the output.

7.3.13 Output Discharge

The device actively discharges the output when the EN pin is low.

7.4 Device Functional Modes

The device has two functional modes: off and on. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

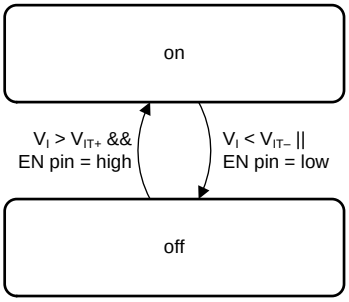

Figure 17. Device Functional Modes

ADVANCE INFORMATION

7.5 Programming

7.5.1 Serial Interface Description

I²C™ is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see UM10204: I²C-bus specification and user manual, revision 6). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The device works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: Standard-mode (100 kbps), Fast-mode (400 kbps) and Fast-mode Plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.1 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore it is referred to as F/S-mode in this document. The device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is 75h (1110101b).

To make sure that the I²C function in the device is correctly reset, it is recommended that the I²C master initiates a STOP condition on the I²C bus after the initial power up of SDA and SCL pull-up voltages.

7.5.2 Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 18. All I²C-compatible devices should recognize a start condition.

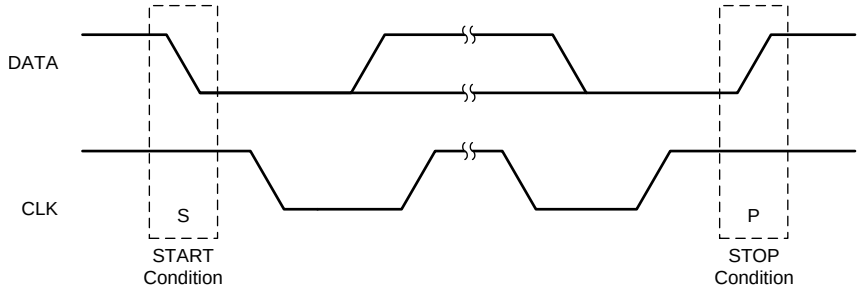

Figure 18. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 19). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 20) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

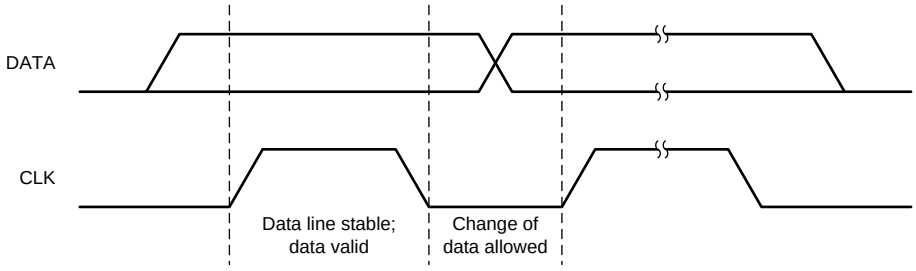

Figure 19. Bit Transfer on the Serial Interface

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Programming (continued)

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 18). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

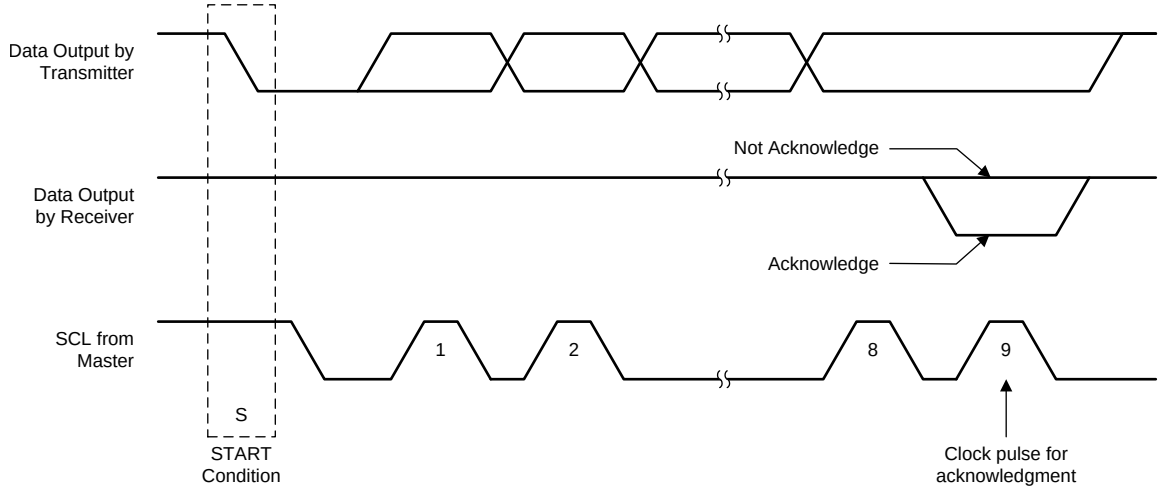

Figure 20. Acknowledge on the I^2C Bus

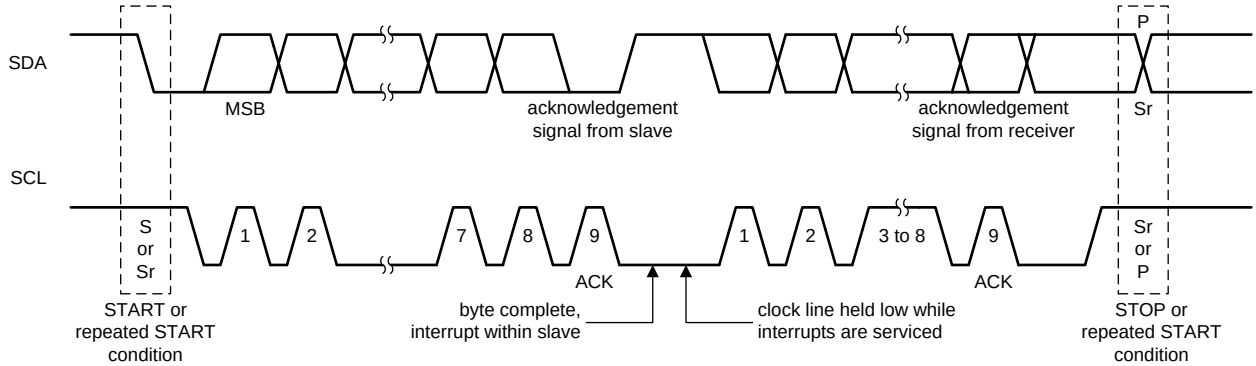

Figure 21. Bus Protocol

7.5.3 I^2C Update Sequence

A single update requires a start condition, a valid I^2C slave address, a register address, and a data byte. To acknowledge the receipt of each byte, the device pulls the SDA line low during the high period of a single clock pulse. The device performs an update on the falling edge of the acknowledge signal that follows the last byte.

ADVANCE INFORMATION

Programming (continued)

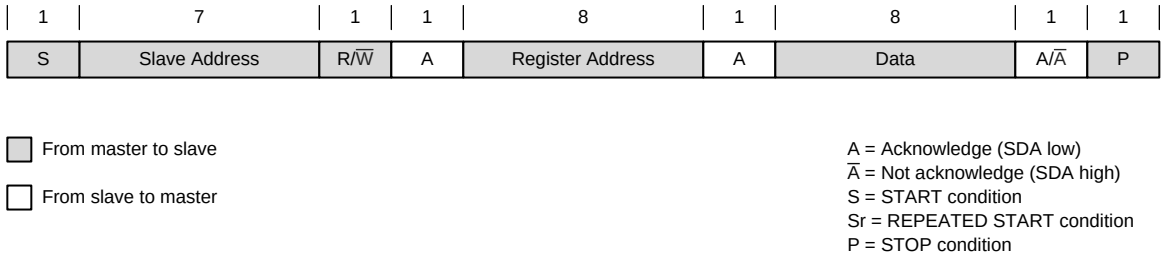

Figure 22. "Write" Data Transfer Format in Standard, Fast and Fast-Plus Modes

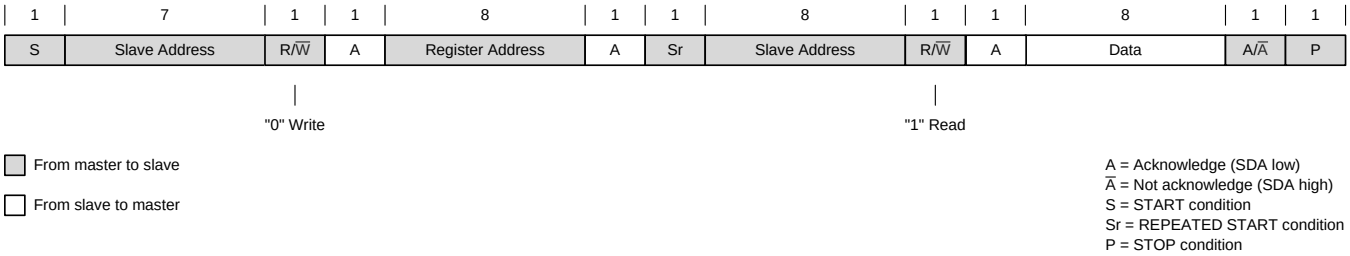

Figure 23. "Read" Data Transfer Format in Standard, Fast and Fast-Plus Modes

ADVANCE INFORMATION

7.6 Register Map

Table 2 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 2 should be considered as reserved locations and the register contents should not be modified.

Table 2. Device Registers

Address	Acronym	Register Name	Section
1h	CONTROL	Control	Go
2h	STATUS	Status	Go
3h	DEVID	Device Identity	Go
4h	VOUT1	Output Voltage 1	Go
5h	VOUT2	Output Voltage 2	Go

7.6.1 CONTROL Register (Address = 1h) [reset = 0h]

CONTROL is shown in Table 3.

Return to Summary Table.

This register configures the device. This register is volatile: it loses its contents if the voltage on the VIN pin becomes less than the UVLO threshold or a low logic level is applied to the EN pin.

Table 3. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	RESERVED	R	0b	Reserved
5	RESERVED	R	0b	Reserved
4	RESERVED	R	0b	Reserved
3	FPWM	R/W	0b	This bit controls forced-PWM operation. Not recommended for use in A0 silicon. 0b = forced-PWM operation disabled 1b = forced-PWM operation enabled
2	RPWM	R/W	0b	This bit controls ramp-PWM operation. Not recommended for use in A0 silicon. 0b = ramp-PWM disabled 1b = ramp-PWM enabled
1-0	SLEW	R/W	00b	These bits control the slew rate of the converter when the output voltage setting is changed to a new value. 00b = 1 V/ms 01b = 2.5 V/ms 10b = 5 V/ms 11b = 10 V/ms

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7.6.2 STATUS Register (Address = 2h) [reset = 0h]

STATUS is shown in Table 4.

Return to Summary Table.

This register contains the device status. A read operation to this register clears the status bits. This register is volatile: it loses its contents if the voltage on the VIN pin becomes less than the UVLO threshold or a low logic level is applied to the EN pin.

Table 4. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved
1	TSD	R	0b	This bit shows the status of the thermal shutdown function. This bit is cleared if the STATUS register is read when the overtemperature condition no longer exists. 0b = temperature good 1b = an overtemperature event was detected
0	$\overline{PG}$	R	0b	This bit shows the status of the output power good comparator. This bit is cleared if the STATUS register is read when the power-not-good condition no longer exists. 0b = power good 1b = a power-not-good event was detected

7.6.3 DEVID Register (Address = 3h) [reset = 0h]

DEVID is shown in Table 5.

Return to Summary Table.

This register identifies the die revision of the device.

Table 5. DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	MANUFACTURER	R	0000b	These bits identify the manufacturer (0000b = Texas Instruments).
3-2	MAJOR	R	00b	These bits identify the major die revision. 00b = A (initial silicon) 01b = B (first major revision) 10b = C (second major revision) 11b = D (third major revision)
1-0	MINOR	R	00b	These bits identify the minor die revision. 00b = 0 (initial silicon) 01b = 1 (first minor revision) 10b = 2 (second minor revision) 11b = 3 (third minor revision)

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7.6.4 VOUT1 Register (Address = 4h) [reset = 3Ch]

VOUT1 is shown in Table 6.

Return to Summary Table.

This register sets the device output voltage when the VSEL pin is low. This register is volatile: it loses its contents if the voltage on the VIN pin becomes less than the UVLO threshold or a low logic level is applied to the EN pin.

Table 6. VOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6-0	VOUT1	R/W	0111100b	These bits set the output voltage of the converter when the VSEL pin is low. The output voltage in volts is 1.825 + (VOUT1 × 0.025)

7.6.5 VOUT2 Register (Address = 5h) [reset = 42h]

VOUT2 is shown in Table 7.

Return to Summary Table.

This register sets the device output voltage when the VSEL pin is high. This register is volatile: it loses its contents if the voltage on the VIN pin becomes less than the UVLO threshold or a low logic level is applied to the EN pin.

Table 7. VOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6-0	VOUT2	R/W	1000010b	These bits set the output voltage of the converter when the VSEL pin is high. The output voltage in volts is 1.825 + (VOUT2 × 0.025)

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS63810 device is a high efficiency, high current buck-boost converter, suitable for applications where the input voltage is higher, lower, or equal to the output voltage. The maximum peak current in the switches is limited to a typical value of 6 A.

8.2 Typical Applications

8.2.1 1.825-V to 5-V Output Smartphone Power Supply

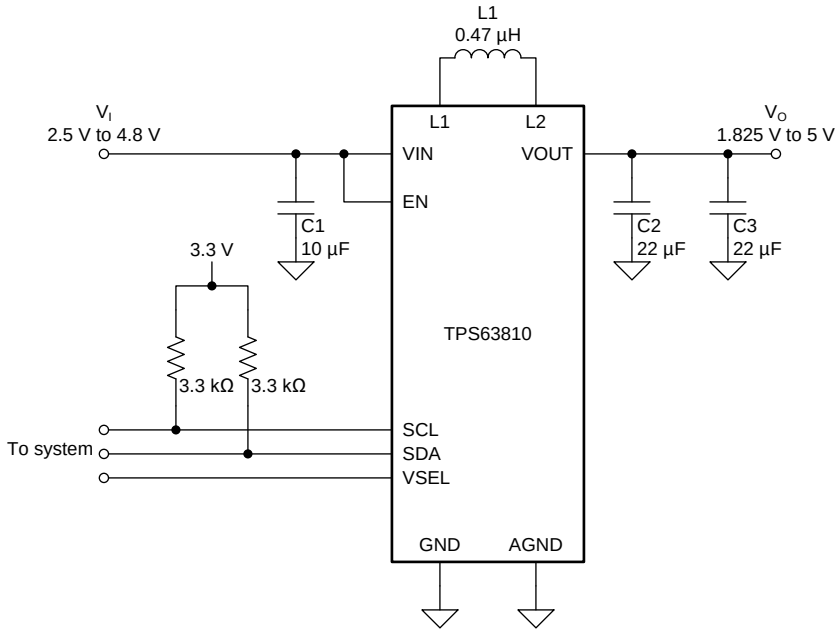

Figure 24. Typical Application Schematic

8.2.1.1 Design Requirements

This example uses the design parameters listed in Table 8.

Table 8. Design Parameters

DESIGN PARAMETER	SYMBOL	EXAMPLE VALUE
Input voltage	V_I	2.5 V to 4.8 V
Output voltage	V_O	1.825 V to 5 V
Output current	I_O	2 A
I^2C bus voltage	V_{BUS}	3.3 V
I^2C bus capacitance	C_b	100 pF
I^2C bus speed		Fast-mode (400 kHz)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Input Capacitor Selection

We recommend a minimum input capacitance (including DC bias effects) of 5 µF. A 10-µF, 6.3-V ceramic capacitor is suitable for typical applications. If the input supply is located more than a few centimeters from the converter, you may need to add additional bulk capacitance (a 47-µF electrolytic or tantalum capacitor is a typical choice).

The output capacitance does not have an upper limit: you can make it as big as you want.

8.2.1.2.2 Inductor Selection

We recommend you use the TPS63810 device with 0.47-µH inductors. For high efficiencies, use an inductor with a low DC resistance (DCR) and low core losses.

The saturation current of the inductor must be greater than the maximum inductor current in your application. To include sufficient margin for worst-case and transient operating conditions, we recommend you use an inductor whose saturation current is at least 20% higher than the maximum inductor current in your application. The maximum current in the inductor occurs when the device operates in boost mode and:

- The input voltage is at its minimum value
- The output voltage is at its maximum value
- The output current is at its maximum value

To calculate the maximum inductor current, first, use Equation 1 to calculate the maximum duty cycle during boost operation (which is when the maximum inductor current occurs).

$$D = \frac{V_O - V_I}{V_O} \quad (1)$$

where

- D is the duty cycle
- V_I is the input voltage
- V_O is the output voltage

$$D = \frac{5\ V - 2.5\ V}{5\ V} = 0.5$$

Next, use Equation 2 to calculate the maximum inductor current.

$$I_{LM} = \frac{I_O}{\eta(1 - D)} + \frac{DV_I}{2fL} \quad (2)$$

where

- I_{LM} is the peak inductor current
- I_O is the output current
- η is the converter efficiency (use the value from the application curves or assume 90%)
- D is the duty cycle (calculated with Equation 1)
- V_I is the input voltage
- f is the switching frequency (assume 2 MHz)
- L is the inductance (use 0.47 µH)

$$I_{LM} = \frac{2\ A}{(0.9)(1 - 0.5)} + \frac{(0.5)(2.5\ V)}{(2)(2\ MHz)(0.47\ \mu H)} = 5.1\ A$$

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To include enough margin for transient conditions, we recommend you use an inductor with a saturation current rating at least 20% higher than the calculated maximum current. Thus, in this example, we recommend an inductor with a saturation current of at least 6.1 A.

8.2.1.2.3 *Output Capacitor Selection*

We recommend a minimum output capacitance (including DC bias effects) of 16 µF. Two 22-µF, 6.3-V ceramic capacitors are suitable for typical applications. If you want to minimize switching noise on the output, connect a small ceramic capacitor (100 nF is a typical value) in parallel to the two main output capacitors and place it closest to the VOUT pin. (Smaller capacitors have lower parasitic inductance and are more effective at filtering high frequencies than the two main output capacitors.)

The output capacitance does not have an upper limit; however very large values of output capacitance will make the transient response of the converter slower.

8.2.1.2.4 I^2C Pullup Resistor Selection

Refer to the I^2C Specification and User Manual for the specifications relevant to your application.

Use Equation 3 to calculate the maximum permitted pullup resistor value for the bus speed used in the application.

$$R_P(max) = \frac{t_r}{0.8473 \times C_b}$$

where

- t_r is the maximum permitted rise time (300 ns for Fast-mode)
- C_b is the capacitive load on each bus line (3)

$$R_P(max) = \frac{300\ ns}{0.8473 \times 100\ pF} = 3.541\ k\Omega$$

If you do not know what the bus capacitance is in your application, start with a 1-kΩ pullup resistor and measure the rise time with an oscilloscope. You can then use Equation 3 to calculate the bus capacitance and thus the maximum permitted pullup resistor.

You can use Equation 4 to calculate the minimum permitted pullup resistor value for different bus speeds.

$$R_P(min) = \frac{V_{BUS} - V_{OL}}{I_{OL}}$$

where

- V_{BUS} is the I^2C bus pullup voltage
- V_{OL} is the low-level output voltage (0.4 V)
- I_{OL} is the low-level output current (3 mA for Fast-mode) (4)

$$R_P(min) = \frac{3.3\ V - 0.4\ V}{3\ mA} = 967\ \Omega$$

A pullup resistor value of 3.3 kΩ meets both of these requirements.

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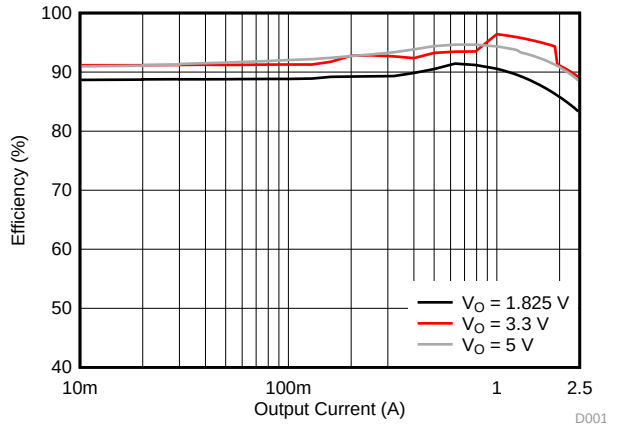
8.2.1.3 Application Curves

Table 9 lists the components that were used for the measurements contained in the following pages.

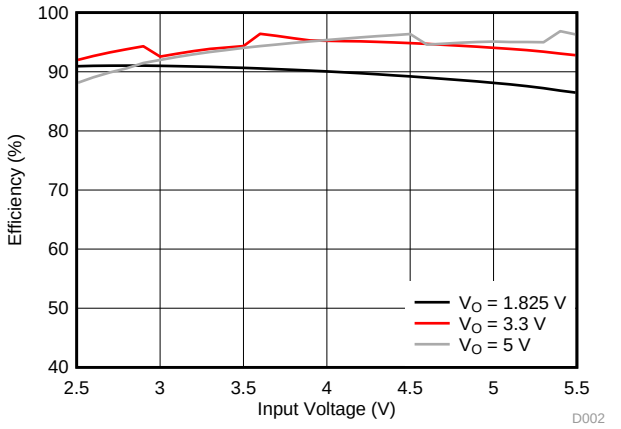
Table 9. Components for Application Characteristic Curves

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER
C1	Capacitor, 10 µF, 6.3 V, 0603, ceramic	GRM155R60J106ME15	Murata
C2, C3	Capacitor, 22 µF, 6.3 V, 0603, ceramic	GRM188R61A226ME15	Murata
L1	Inductor, 0.47 µH	XFL4015-471MEC	Coilcraft
U1	Integrated circuit	TPS63810YFF	Texas Instruments



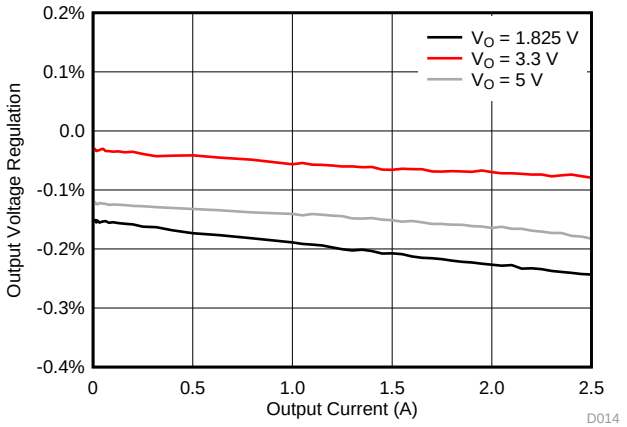
V_I = 3.6 V PFM T_A = 25°C

Figure 25. Efficiency vs Output Current



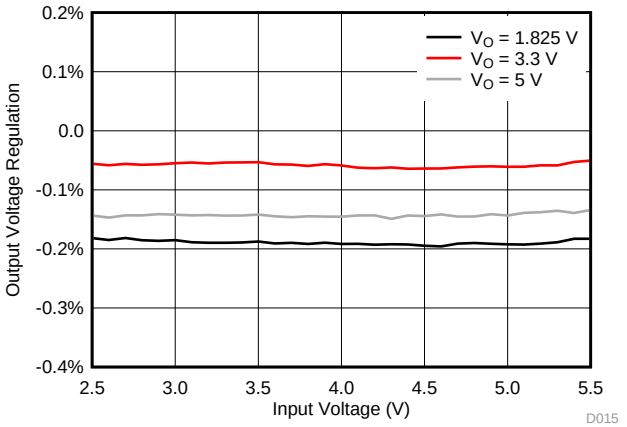
I_O = 1 A PFM T_A = 25°C

Figure 26. Efficiency vs Input Voltage



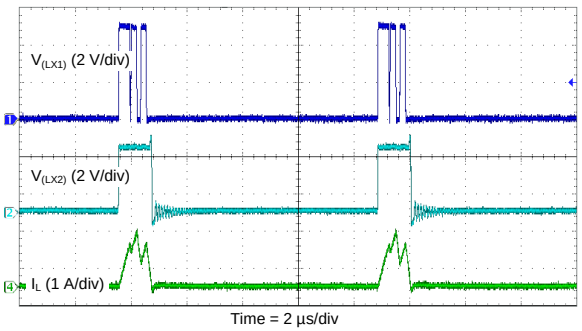
V_I = 3.6 V FPWM T_A = 25°C

Figure 27. Load Regulation



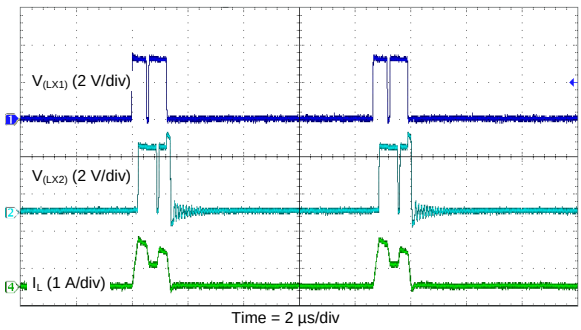
I_O = 1 A FPWM T_A = 25°C

Figure 28. Line Regulation



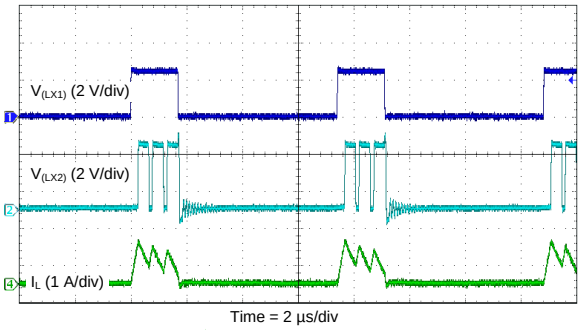
V_I = 5 V PFM T_A = 25°C
V_O = 3.3 V
I_O = 100 mA

Figure 29. PFM Switching Waveforms (Buck Operation)



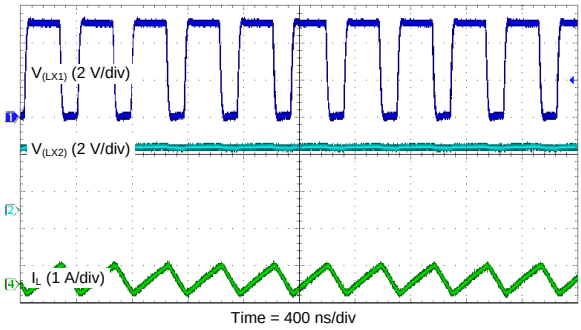
V_I = 3.3 V PFM T_A = 25°C
V_O = 3.3 V
I_O = 100 mA

Figure 30. PFM Switching Waveforms (Buck-Boost Operation)



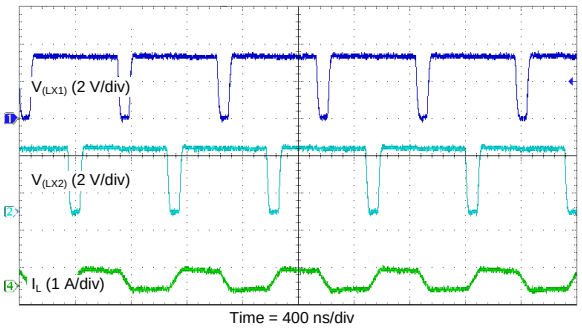
V_I = 2.5 V PFM T_A = 25°C
V_O = 3.3 V
I_O = 100 mA

Figure 31. PFM Switching Waveforms (Boost Operation)



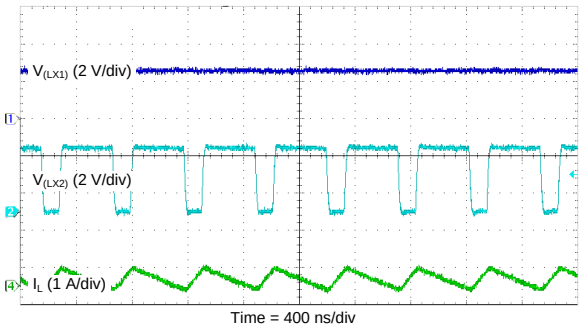
V_I = 5 V PWM T_A = 25°C
V_O = 3.3 V
I_O = 100 mA

Figure 32. PWM Switching Waveforms (Buck Operation)



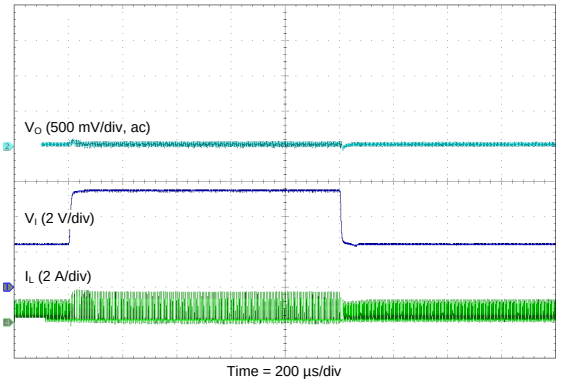
V_I = 3.3 V PWM T_A = 25°C
V_O = 3.3 V
I_O = 100 mA

Figure 33. PWM Switching Waveforms (Buck-Boost Operation)



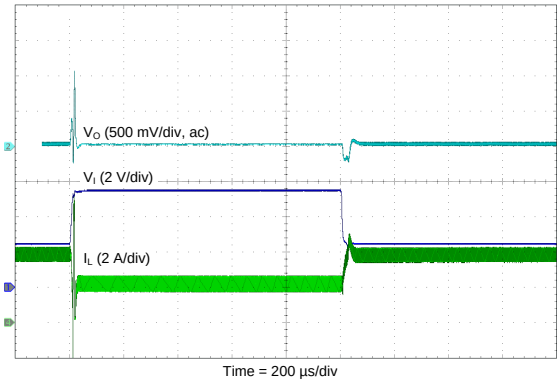
V_I = 2.5 V PWM T_A = 25°C
V_O = 3.3 V
I_O = 100 mA

Figure 34. PWM Switching Waveforms (Boost Operation)



V_I = 2.5 V to 5.5 V PSM T_A = 25°C
V_O = 3.3 V
I_O = 200 mA

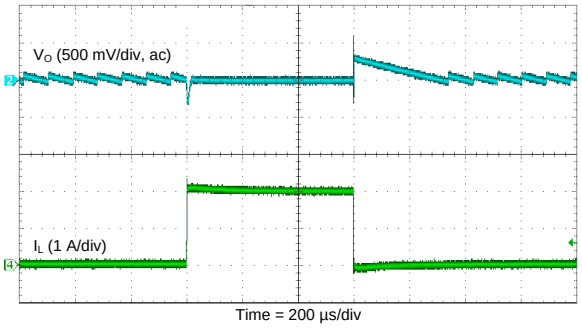
Figure 35. Line Transient Response



V_I = 2.5 V to 5.5 V PSM T_A = 25°C
V_O = 3.3 V
I_O = 2 A

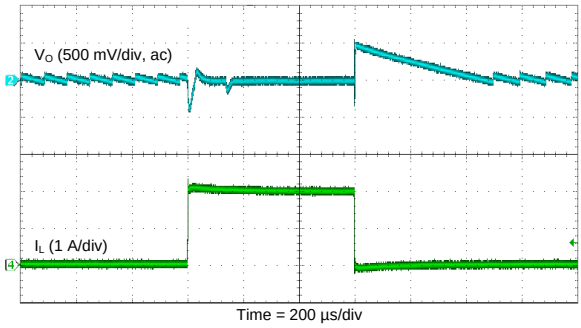
Figure 36. Line Transient Response

ADVANCE INFORMATION



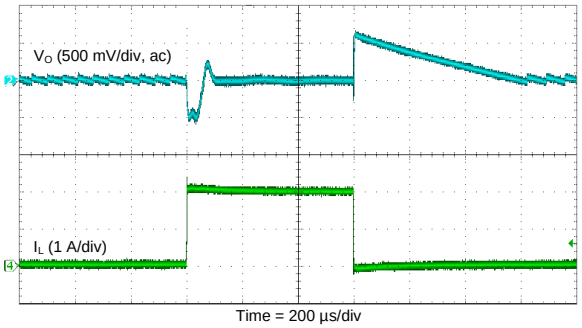
V_I = 4.2 V PSM T_A = 25°C
V_O = 3.3 V
I_O = 10 mA to 2 A

Figure 37. Load Transient Response (Buck)



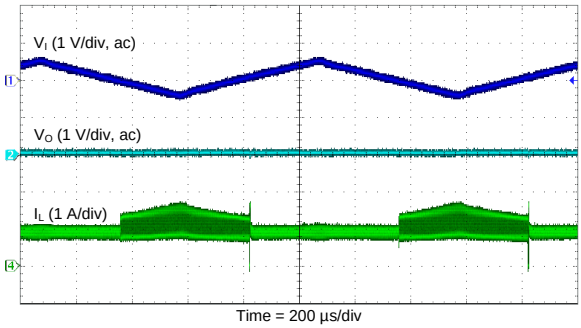
V_I = 3.3 V PFM T_A = 25°C
V_O = 3.3 V
I_O = 10 mA to 2 A

Figure 38. Load Transient Response (Buck-Boost)



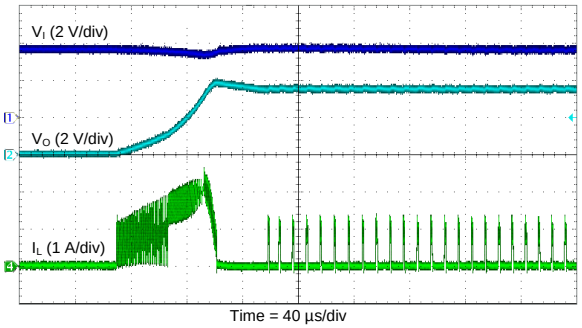
V_I = 2.6 V PFM T_A = 25°C
V_O = 3.3 V
I_O = 10 mA to 2 A

Figure 39. Load Transient Response (Boost)



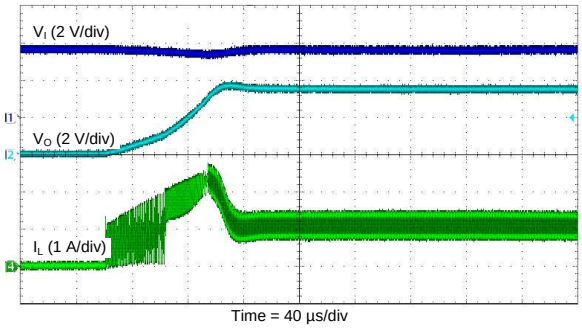
V_I = 3.3 V ±0.9 V PWM T_A = 25°C
V_O = 3.3 V
R_L = 3 Ω

Figure 40. Line Sweep (PWM)



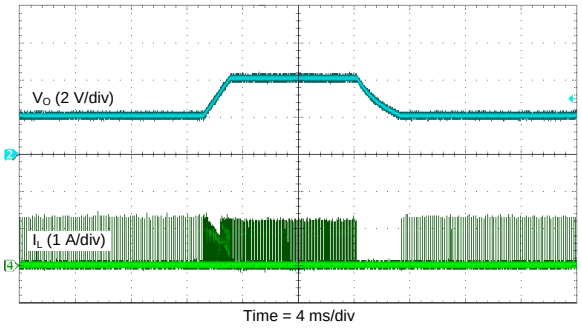
V_I = 3.6 V PFM T_A = 25°C
V_O = 3.3 V
R_L = 33 Ω

Figure 41. Start-Up Waveforms (Light Load)



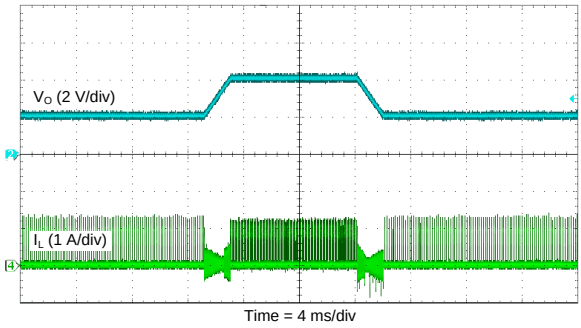
V_I = 3.6 V PFM T_A = 25°C
V_O = 3.3 V
R_L = 3.3 Ω

Figure 42. Start-Up Waveforms (Heavy Load)



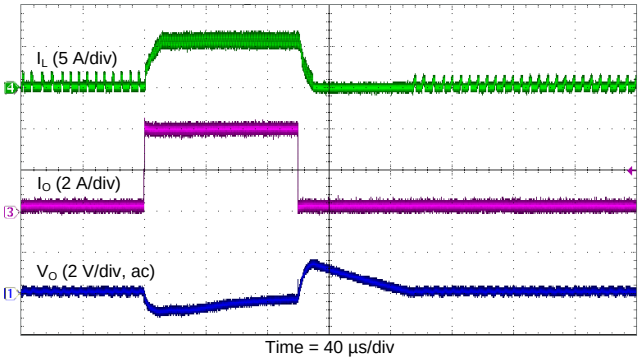
V_I = 3.6 V
V_O = 2 V to 4 V
R_L = 330 Ω
PFM
T_A = 25°C

Figure 43. Dynamic Voltage Scaling (PFM)



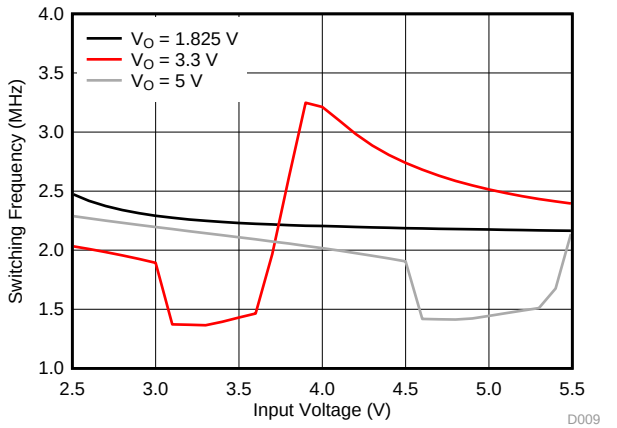
V_I = 3.6 V
V_O = 2 V to 4 V
R_L = 330 Ω
PFM
RPWM
T_A = 25°C

Figure 44. Dynamic Voltage Scaling (RPWM)



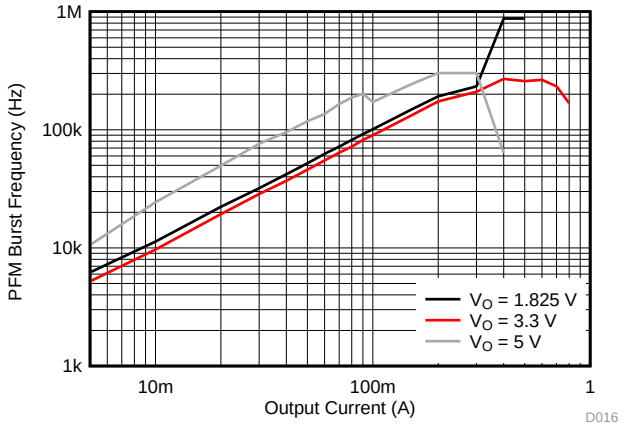
V_I = 3.6 V
V_O = 3.3 V
PFM
T_A = 25°C

Figure 45. Overcurrent Protection



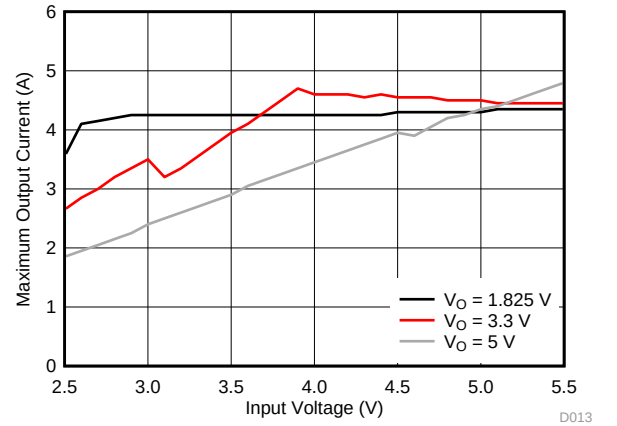
I_O = 1 A
V_I rising
FPWM
T_A = 25°C

Figure 46. Switching Frequency vs Input Voltage



V_I = 3.6 V
PFM
T_A = 25°C

Figure 47. Burst Switching Frequency vs Input Voltage



PFM
T_A = 25°C

Figure 48. Maximum Output Current vs Input Voltage

ADVANCE INFORMATION

9 Power Supply Recommendations

The device is designed to operate with a DC supply voltage in the range 2.2 V to 5.5 V. If the input supply is more than a few centimeters from the device, we recommend you add some bulk capacitance to the ceramic bypass capacitors. A 47-µF electrolytic capacitor is a typical selection for the bulk capacitance.

10 Layout

10.1 Layout Guidelines

Correct PCB layout is necessary to obtain the full performance from the device. We recommend you follow these basic principles:

- Place input and output capacitors close to the device to minimize the input and output loop areas.
- If you combine different-sized capacitors to make up the total input capacitance, place the smallest capacitor closest to the device. The same applies to the output capacitance.
- Keep PCB traces short and wide to minimize parasitic resistance and inductance.
- Use the following PCB layer stack (or something similar):
  - Layer 1 (top): all components and all power traces
  - Layer 2 (inner): signals
  - Layer 3 (inner): signals
  - Layer 4 (bottom): ground plane

Figure 49 shows an example of the PCB layout used for all of the measurement data in *Application Curves*.

10.2 Layout Example

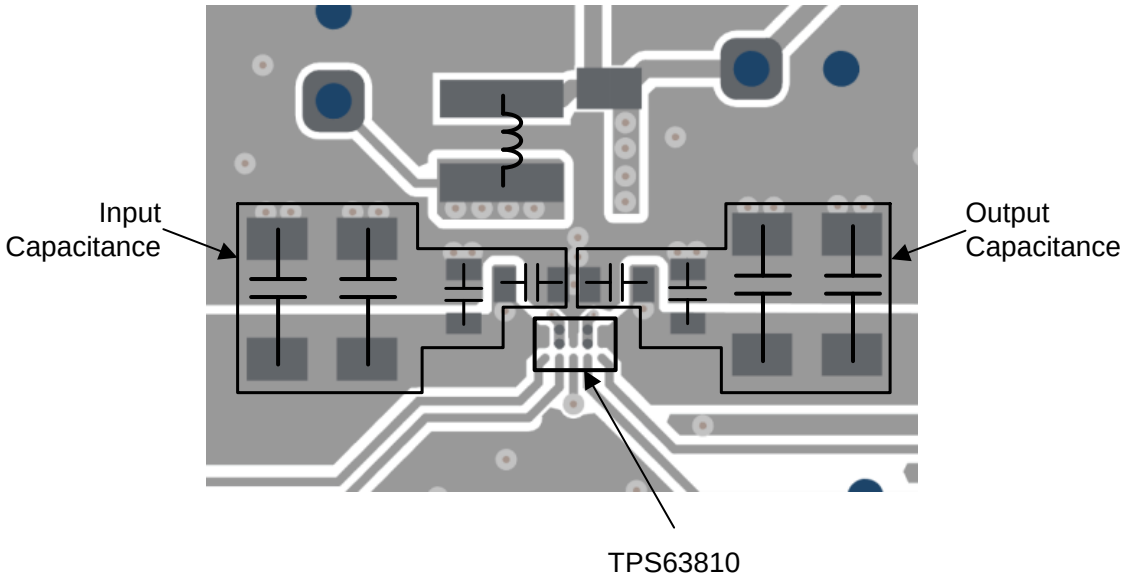


Figure 49. Recommended PCB Layout for the TPS63810 Device

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- NXP Semiconductors, UM10204 – I^2C-Bus Specification and User Manual
- TPS63810 EVM User Guide

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022– *TI Glossary*

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63810YFFR	PREVIEW	DSBGA	YFF	15	3000	TBD	Call TI	Call TI	-40 to 85		
XPS63810YFFT	ACTIVE	DSBGA	YFF	15	250	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

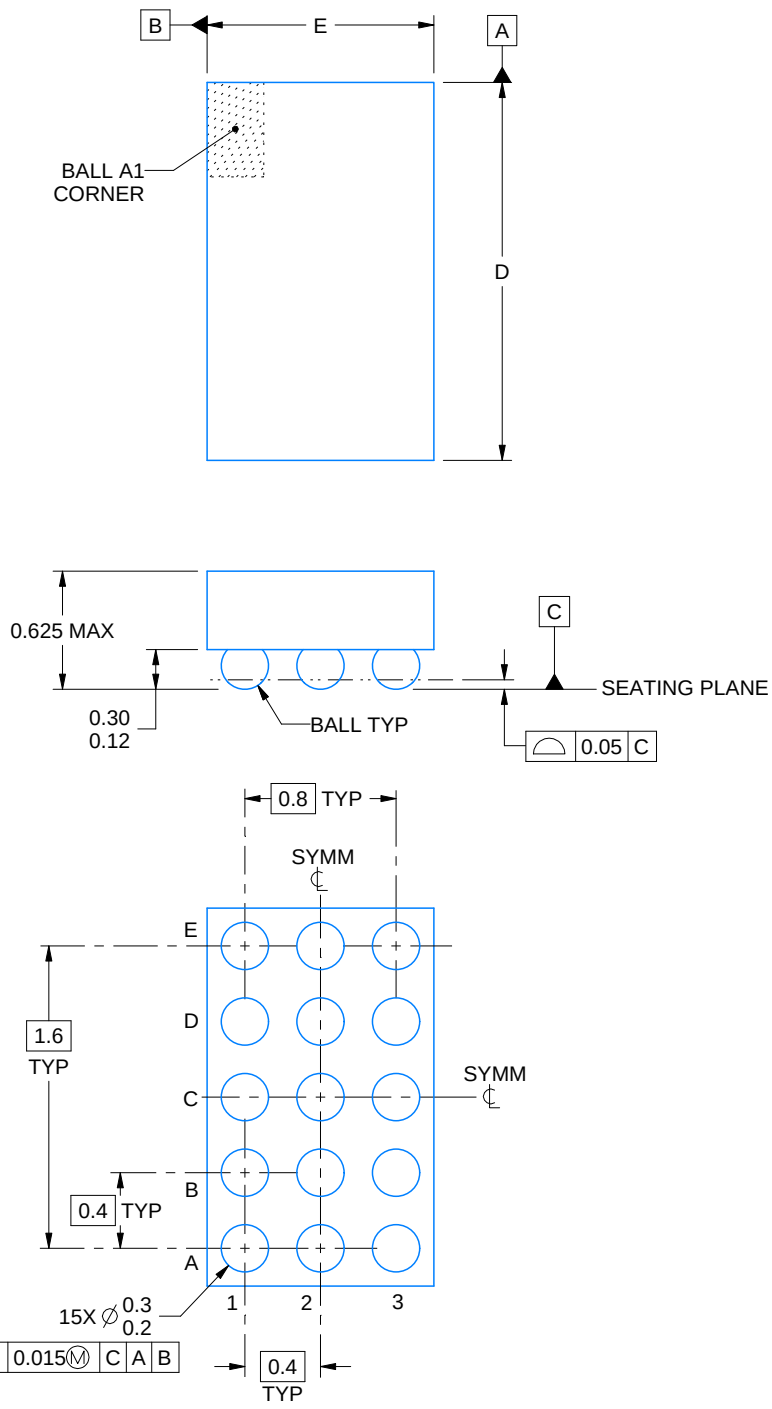
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

YFF0015

DSBGA - 0.625 mm max height

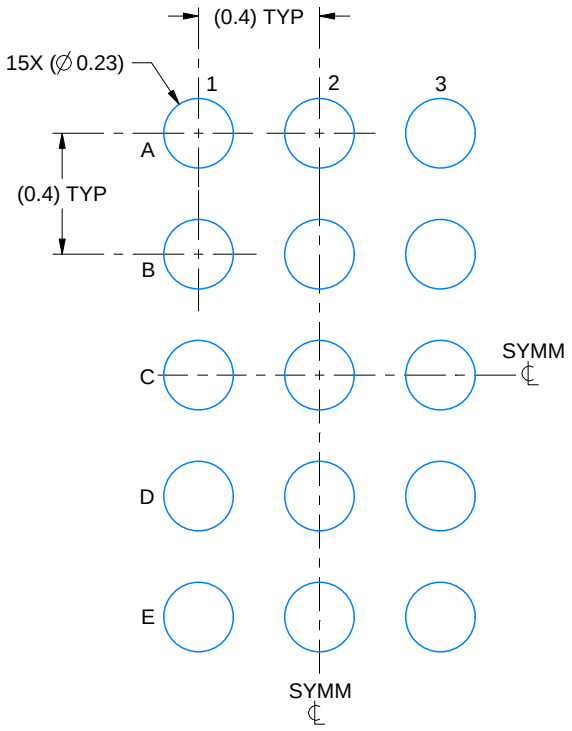
DIE SIZE BALL GRID ARRAY



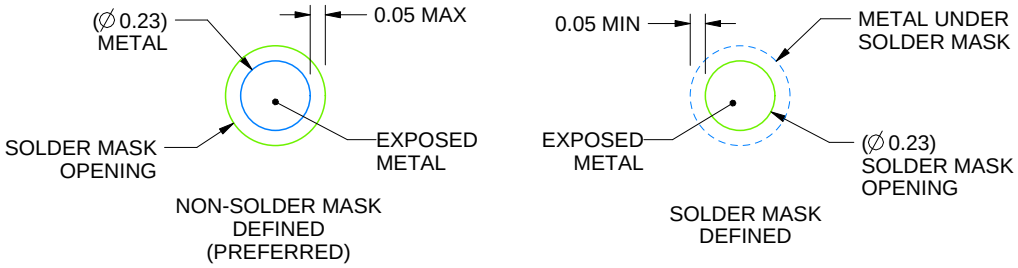
4219378/A 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

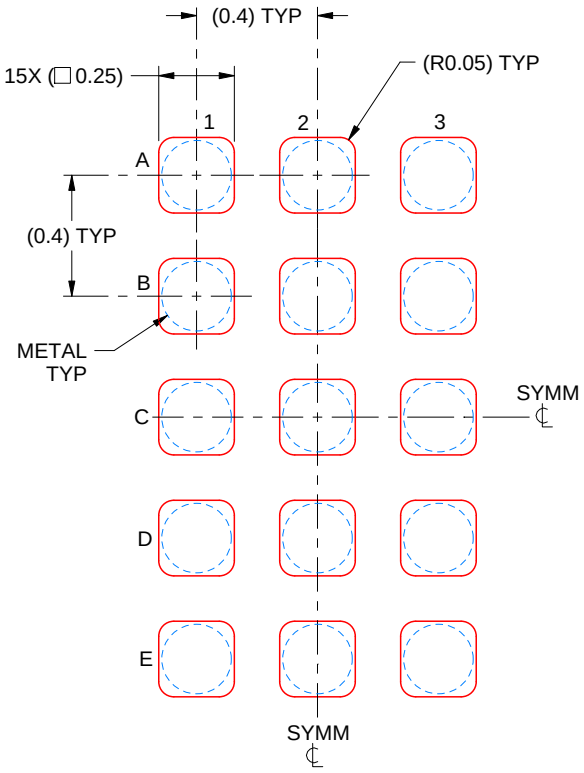
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0015

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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